DESIGN OF TIME BASED ANALOG TO DIGITAL CONVERTER (TB-ADC): NEW DESIGN METHODOLOGY FOR VOLTAGE-TO-TIME-CONVERTER (VTC) CIRCUITS

By

Mohammed Wagih Emam Ismail

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfilment of the
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MASTER OF SCIENCE
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Electronics and Communications Engineering

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Title of Thesis:

Design of Time Based Analog to Digital Converter (TB-ADC): New Design Methodology for Voltage-to-Time-Converter (VTC) Circuits

Key Words:
Voltage to Time Converter (VTC); Time to Digital Converter (TDC); Analog to Digital Converter (ADC); Software Deifned Radio (SDR)

Summary:
In this thesis, we introduce a new design methodology for Voltage-to-Time Converters (VTCs) Circuits suitable for Time-Based Analog-to-Digital Converters (TB-ADC). This new methodology has been tested by designing an 8-bit low power TB-ADC as one of the alternatives to the traditional ADCs. The proposed ADC consists of two stages. The first stage is the VTC and the second stage is the Time to Digital Converter (TDC). The percentage of digital to analog part is greater than the traditional ADC and it is an Op-Amp-less design.

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Dedication

I dedicate this dissertation to my family for the unceasing encouragement, support and attention. I want to thank them for the continuous supply of love and care. I own them every single achievement in my life.

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List of Symbols and Abbreviations

Symbols	Description
ϵ	the linearity error.
σ	signal sensitivity.
DR	Dynamic Range.
f_s	sampling frequency.
Tf_{th}	fall threshold time .
$Tmeth_{th}$	the new design methodology threshold time .
Tr_{th}	rise threshold time .

Abbreviations	Description
ADC	Analog To Digital Converter.
AFC	Analog to Frequency Converters.
ATC	Analog to Time Converters.
CR	Coarse Resolution.
CVDL	Coarse Vernier Delay Line.
DAC	Digital to Analog Converters.
DNL	Differential Non-Linearity.
DSP	Digital Signal Processing.
ENOB	Effective Number Of Bits.
EOC	End Of Conversion.
FDC	Frequency to Digital Converters.
FVDL	Fine Vernier Delay Line.
ICW	Ideal Code Width.
INL	Integral Non-Linearity.
LSB	Least Significant Bit.
MSB	Most Significant Bit.
OH2B	One Hot to Binary.

PWM	Pulse Width Modulation.
SAR-ADC	Successive Approximation Register ADC.
SDR	Software Defined Radio.
SNDR	Signal to Noise and Distortion Ratio.
SNR	Signal to Nise Ration.
TB-ADC	Time Based Analog to Digital Converter.
TH2OH	THermal to One Hot.
THD	Total Harmonic Distortion.
UWB	Ultra Wide Band.
VCOs	Voltage Controlled Oscillators.
VDL	Vernier Delay Line.
VTC	Voltage to Time Converter.

List of Publications

Published:

[1] M. Wagih Ismail and H. Mostafa, "A new design methodology for voltage-to-time converters (vtcs) circuits suitable for time-based analog-to-digital converters (t-adc)," in *System-on-Chip Conference (SOCC), 2014 27th IEEE International*, Sep. 2014, pp. 103–108.

[2] A. Hassan, M. Ali, N. Mohammed, A. Ali, M. Hassoubh, M. Ismail, M. Refky, and H. Mostafa, "A 500 ms/s 6 bits delay line adc with inherit sample hold," in *Microelectronics (ICM), 2014 26th International Conference on*, Dec. 2014, pp. 96–99.

[3] A. Hussein, M. Fawzy, M. Ismail, M. Refky, and H. Mostafa, "A 4-bit 6gs/s time-based analog-to-digital converter," in *Microelectronics (ICM), 2014 26th International Conference on*, Dec. 2014, pp. 92–95.

Submitted:

[2] M. Wagih Ismail and H. Mostafa, "8-bit tb-adc using new design methodology for voltage-to-time converters (vtcs) circuits," in *System-on-Chip Conference (SOCC), 2015 28th IEEE International*, Sep. 2015, pp. 103–108.

Abstract

The analog to Digital Converter (ADC) is considered one of the most essential blocks in Software Defined Radio (SDR), Ultra Wide Band (UWB) receivers, biomedical applications, and embedded systems. The majority of the Integrated Circuits (ICs) today are mixed analog/digital systems to get benefit from the growing capabilities in Digital Signal Processing (DSP). The DSP is preferred to the analog signal processing in many different ways such as: power consuming and processing speed. Thus, the main target is to decrease the analog processing blocks and increase the digital processing blocks in the aforementioned systems.

There are various types of ADC to cope with different systems requirements. The eminent performance factors are speed, power, area, and resolution. Based on applications needs the correct ADC can be designed. We can find in literature several types like flash ADC, successive approximation register ADC, sigma-delta ADC, pipelined ADC, and ramp ADC. Mainly, all the aforementioned ADCs depend on operational amplifiers.

Decreasing the percentage of the analog part and increasing the percentage of the digital part in integrated circuits is the current trend and is highly recommended to maximize the benefit of the unceasing CMOS technology scaling. The unceasing CMOS technology scaling makes transistors channel length shorter and increases transistors integration density leading to supply voltage reduction. This reduction in supply voltage increases the difficulties imposed on the analog circuit design because the threshold voltage and the noise level do not scale with the same factor as the supply voltage. As smaller the $V_{dd} - V_{th}$-headroom - becomes, as difficult the cascoding (transistor stacking) becomes because of the overdrive voltage required and the noise effect. Therefore, the digital circuits are preferred to the analog circuits in deep sub-micron technology. The switching time becomes smaller and the circuits that depend on time resolution get a superior accuracy over the analog circuits.

In this thesis proposal, we introduce Time Based Analog to Digital Converter (TB-ADC) as an alternative solution to traditional ADC in SDR and UWB systems. The basic benefit from the TB-ADC is that the percentage of digital to analog circuits is grater than the traditional one and it is Op-Amp less design. This type of ADCs gets benefit from the time resolution where time resolution increases as technology node scales. Moreover, it has its inherited sample & hold circuit.

Chapter 1

Introduction

We are living in an analog world and all the signals around us are continuous analog signals. The understanding and processing of these signals are vital to our lives. The electronics industrial trend, nowadays, tends to monitor, sense, and control everything around us. The remarkable advance in the digital signal processing domain drives the scientific community to design different types of analog to digital converters to satisfy the needs of the consumer market. The analog to digital converters appeared to shorten the gap between the analog world and the digital processing domain by converting the analog signal to digital signal. Therefore, the majority of integrated circuits today are mixed analog/digital circuits that need ADCs.

The most important parameters in ADCs are sampling frequency, resolution, power, and area. Different types of ADCs exist to satisfy the requirements of different systems because each system has a different critical parameter. Software defined radio, wireless communications, biomedical systems and sensors, and internet of things are examples for the systems that need ADCs and each one of them has specific constraints on power, speed, and resolution. For example, sensors impose restrictions on the consumed power. Sensors are used to sense and measure different physical quantities like viscosity, speed, pressure, and flexibility. All these quantities are analog and need to be processed by DSP circuits. However, sensors have restrictions on the power consumed. This emphasizes the need for new ADC types.

The classification process for ADCs is either based on the sampling rate or the conversion type. We have two main categories based on the sampling frequency. The first one is Nyquist rate ADCs and the second one is oversampling ADCs. Flash ADC, pipelined ADC, and Successive Approximation Register ADC (SAR-ADC) are examples of the Nyquist rate type and Sigma-Delta modulator is an example of the over sampling ADCs [1].

The other type of classification is based on the conversion way. We can discuss two kind of conversions. The first one is the traditional conversion and it is called Direct Conversion. In the direct conversion ADCs, the voltage is converted to code directly. The second way of conversion is Indirect Conversion. The indirect conversion converts the voltage signal to an intermediate form like time or frequency then this form is converted

to code. This thesis proposal introduces the indirect conversion by converting the voltage to time then converting the time to code [2].

1.1 Motivation

With technology scaling, the improvement in the digital circuits surpasses the improvement in the analog circuits. There are two main reasons. First, the supply voltage scales down with the technology leading to decreasing the voltage swing. However, the noise does not scale with technology leading to smaller signal to noise ratio that makes the analog system less immune to the noise. Second, the threshold voltage does not scale with the same factor as the supply voltage. Therefore, the cascoding technique becomes harder and more difficult [1, 3].

Meanwhile, with technology scaling the time-based processing gains popularity because of the increasing time resolution that can be observed from the deep sub-micron CMOS technology switching time. As said by Staszewski in [4] and confirmed by Macpherson in [3] " in a deep CMOS process, time domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals". Also, the time processing consumes less power because it depends on the digital circuits that is normally minimum size and its reduced power supply dissipates limited power [2, 5, 6]. Moreover, a good portion of TB-ADC designs have an inherited sample and hold, so the need of the sample and hold circuit can be reduced up to certain frequency based on the design.

1.2 Proposed work

In this thesis proposal, a time based analog to digital converter that does not use an external sample and hold circuit and depends on the indirect conversion from voltage to code through the Pulse Width Modulation (PWM) is introduced. This work mainly depend on Voltage-to-Time-Converter (VTC) followed by Time-to-Digital-Converter (TDC).

Eliminating the use of Sample and Hold (S/H) circuit decreases the hardware and decreases the dissipated power. Using the VTC and TDC techniques makes the digital portion of the circuit is much larger than the analog circuits.

1.3 Organization of the thesis

The remainder of this thesis is organized as follows: Chapter 2 introduces a literature review and basic concepts for the conventional and time based analog to digital converters. Chapter 3 presents detailed analysis for the VTC circuit used in this proposal and its simulation results. Chapter 4 introduces the TDC circuit and its simulation results. Chapter 5 discusses the overall TB-ADC and introduces a conclusion for the thesis. Finally, the appendices illustrate how to deal with the simulators and the used matlab codes.

Chapter 2

Literature Review

2.1 Analog to Digital Converter

Analog to digital converters are used to convert the continuous time and amplitude signal to code that is discrete in both amplitude and time. Each code represents a specific sampling instance and its corresponding quantized amplitude that introduces the quantization error, that will be illustrated later in this thesis. This quantization error could be reduced by using higher resolution, higher number of bits ADCs. The opposite operation is carried out using Digital to Analog Converters (DAC). Figure 2.1 shows three bit ADC sampling instances and values[1].

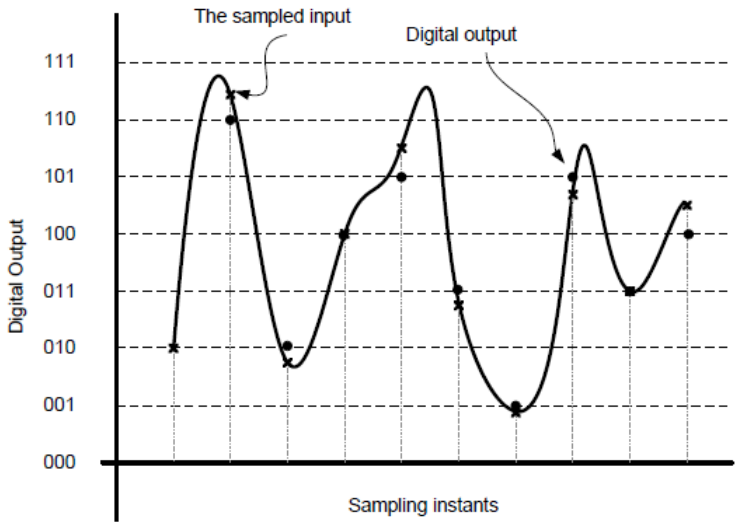

Figure 2.1: Example of a 3-bit ADC [1]

2.1.1 Sampling

ADCs sample the input analog signal with a frequency called the sampling frequency f_s. The sampling frequency should satisfy the Nyquist rate sampling with $f_s \geq 2 * Fmax$, where $Fmax$ is the maximum frequency in the spectrum of the input signal[7]. Figure 2.4

(a) illustrates a signal in time domain and illustrates its shape in the frequency domain. Sampling in time domain is equivalent to multiplication with impulse train. In frequency domain multiplication is equivalent to convolution and the impulse train in time domain becomes impulse train in the frequency domain like in Figure 2.4 (b). Figure 2.4 (c) illustrates the multiplication in time domain, convolution in the frequency domain, that form the sampled signal.

To reconstruct the original, unsampled signal, we need a reconstruction filter, low pass filter, like the one shown in Figure 2.4 (d) as a time and frequency domains. As much as the f_s is grater than the $2 * F_{max}$ as easier as the design of low pass filter. If the signal reconstructed correctly it will be like Figure 2.4 (e). However, if the sampling frequency does not satisfy the Nyquist criteria, the signal will not be reconstructed correctly and aliasing will occur. Figure 2.2 illustrates the sampled signal, in frequency domain, that satisfies the Nyquist criteria. Thus, the original signal could be reconstructed with a low pass filter. In contradiction , Figure 2.3 illustrates the sampled signal, in frequency domain, that does not satisfy the Nyquist rate. The aliasing, kind of frequency interference, occurs and the original signal will not be extracted by the low pass filter [7].

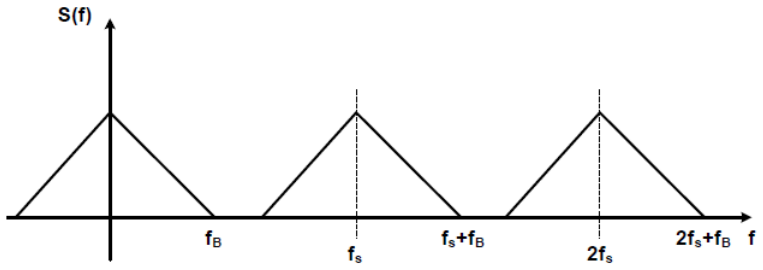

Figure 2.2: **Frequency domain representation for sampled signal with** $f_s \geq 2F_{max}$**[1]**

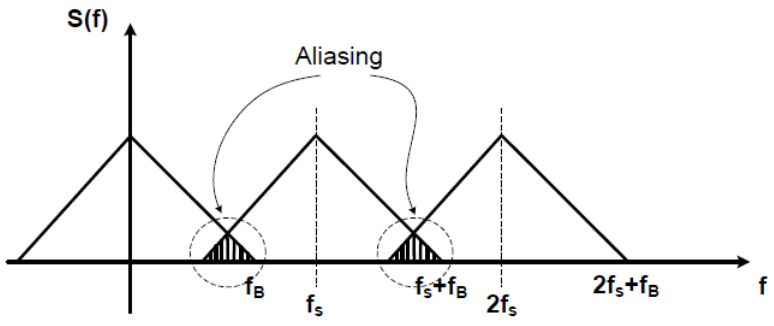

Figure 2.3: **Frequency domain representation for sampled signal with** $f_s \leq 2F_{max}$**[1]**

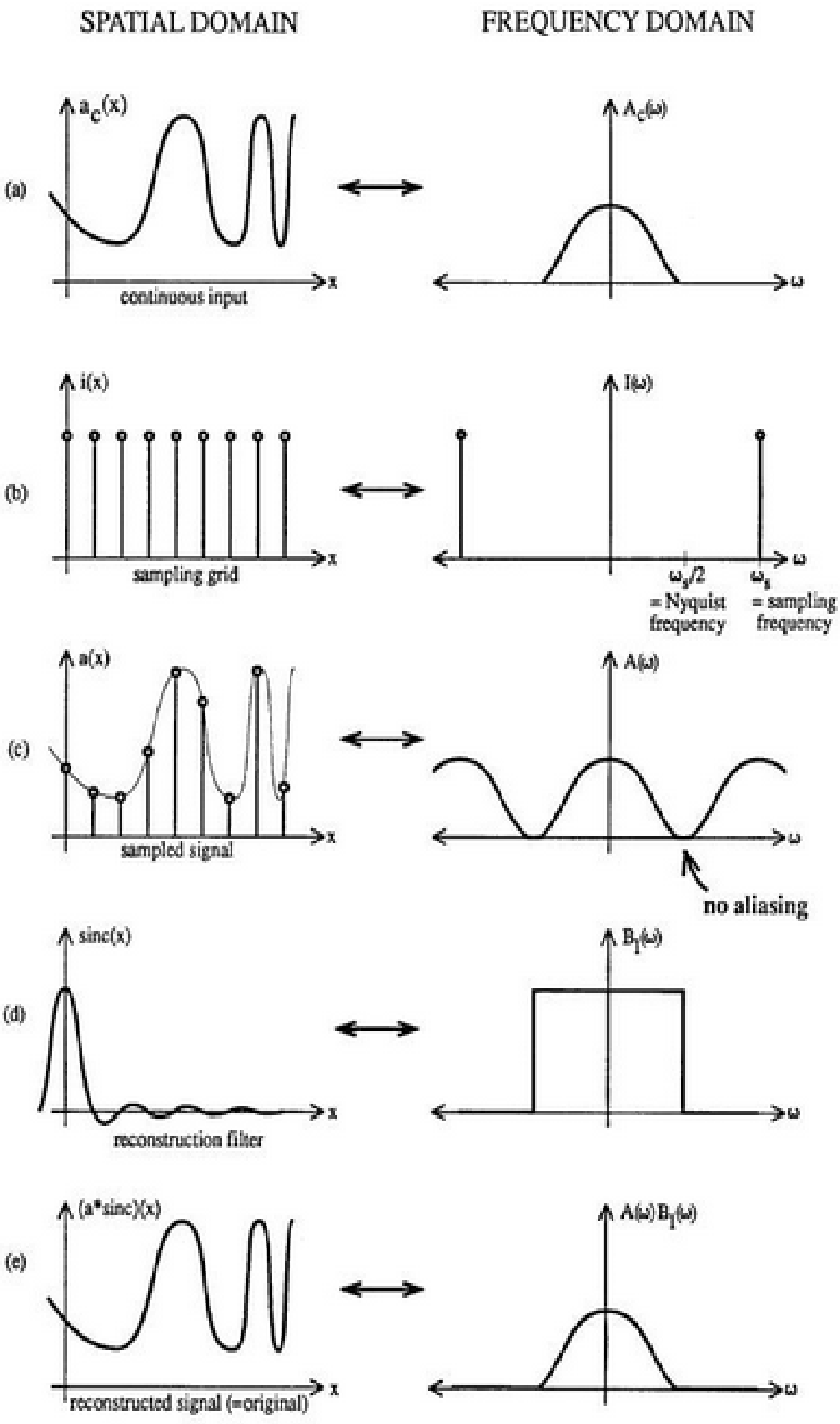

Figure 2.4: Sampling theory in time and frequency domain [8]

2.1.2 Quantization

Quantization happens when a continuous range of inputs is translated to the same output code as shown in Figure 2.5. The quantization process leads to quantization error or what is denoted by quantization noise. Thus, the quantization process has an undesired effect. Quantization noise is the main source of error in the ideal ADCs. The quantization error can be defined as the difference between the original signal and the quantized version of it as shown in Figure 2.6 and it ranges from $-0.5 * LSB : 0.5 * LSB$ as shown in Figure 2.7, where LSB is the Least Significant Bit (LSB). However, the quantization error can be reduced, but not eliminated, by using higher resolution ADC [1].

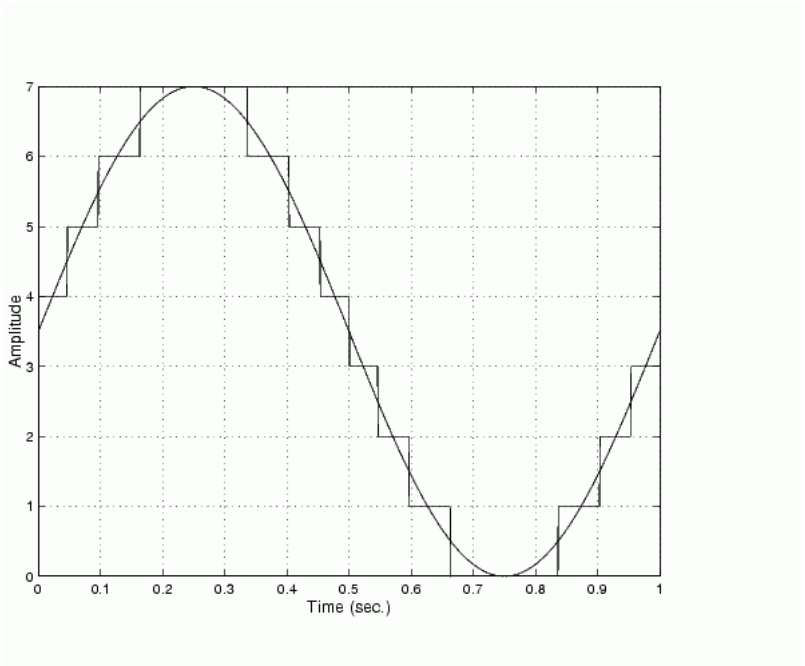

Figure 2.5: Original and Quantized signal

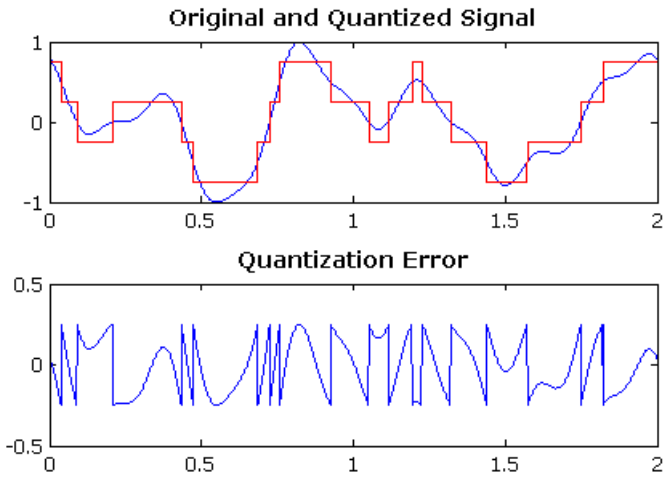

Figure 2.6: Quantization error

Figure 2.7: Quantization error

The resolution of an ADC can be measured by LSB as

$$LSB = \frac{FS}{2^n} \tag{2.1}$$

where the n is the number of bits and FS is the full scale input of the ADC. Therefore, to reduce the quantization noise power, we have to increase the resolution by increasing the number of bits.

2.2 ADC characteristic and performance metrics

Deep understanding of the ADC characteristics and performance metrics helps to pick up the correct ADC for the target application. Moreover, understanding these characteristics is vital to know the limiting factors in your design to achieve optimal performance.

2.2.1 Static specifications and definitions

Due to non idealities in circuit implementations some errors, other than the quantization error, are introduced. These errors are time independent. In this section, we are going to illustrate some of these non idealities and how it affects the ADC and how it could be calculated.

2.2.1.1 ADC transfer curves

The ADC converts the input voltages into the corresponding output codes. Ideally, the curve describing this behavior is the ideal transfer function. The ideal transfer function is completely linear and any change in the input voltage has the same effect on the output code. However, this does not happen and the actual curve describing this behavior is the actual transfer function. Some calibration techniques are used to help shorten the gap between the actual and the ideal transfer functions [9].

2.2.1.2 Ideal transfer function

The ideal transfer function represents the ideal line that expands from the minimum input voltage, V_{refl}, to the maximum input voltage, V_{refh}, and this transfer function is quantized through dividing by the number of available output codes, 2^n, where n is the

number of bits. The input voltage range is divided to equivalent code width. Ideal Code Width (ICW) is the portion of the continuous input voltage that can be defined as follow

$$ICW = LSB = \frac{V_{refh} - V_{refl}}{2^n} \tag{2.2}$$

$$Code = \frac{V_{in} - V_{refl}}{LSB} \tag{2.3}$$

where V_{in} is the input voltage [9].

2.2.1.3 Offset error

The offset error can be defined as the deviation of the actual characteristic line from the ideal characteristic line as shown in Figure 2.8. The actual characteristic line can be shifted from the ideal one to the right or to the left [1, 9, 10]. This offset error is introduced by the offset voltage between the positive and negative terminals of the operational amplifier due to the mismatch between both terminals [11].

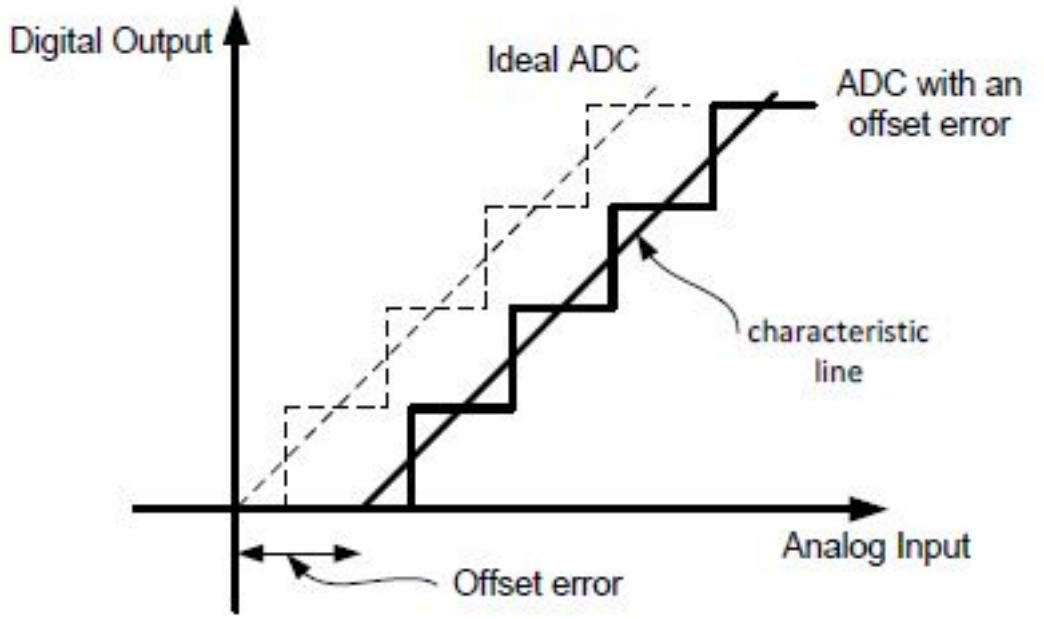

Figure 2.8: ADC offset error [1]

2.2.1.4 Gain error

The gain error is defined as the deviation between the ideal characteristic line slope and the actual characteristic line slope as shown in Figure 2.9 after removing the offset error[1, 9, 10].

2.2.1.5 Differential non-linearity

The Differential Non-Linearity (DNL) is defined as the deviation of the ICW from 1 LSB. Figure 2.10 illustrates *n* bit ADC with DNL. DNL for code k can be calculated as follow

$$DNL_k = \frac{C_k - 1LSB}{1LSB} \tag{2.4}$$

where $C_k$is the actual code width for code K.

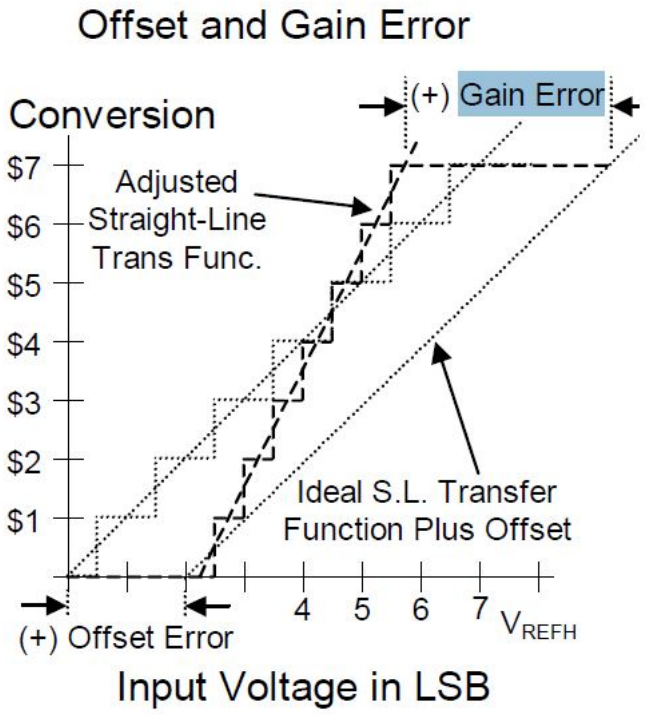

Figure 2.9: Gain and Offset Error [9]

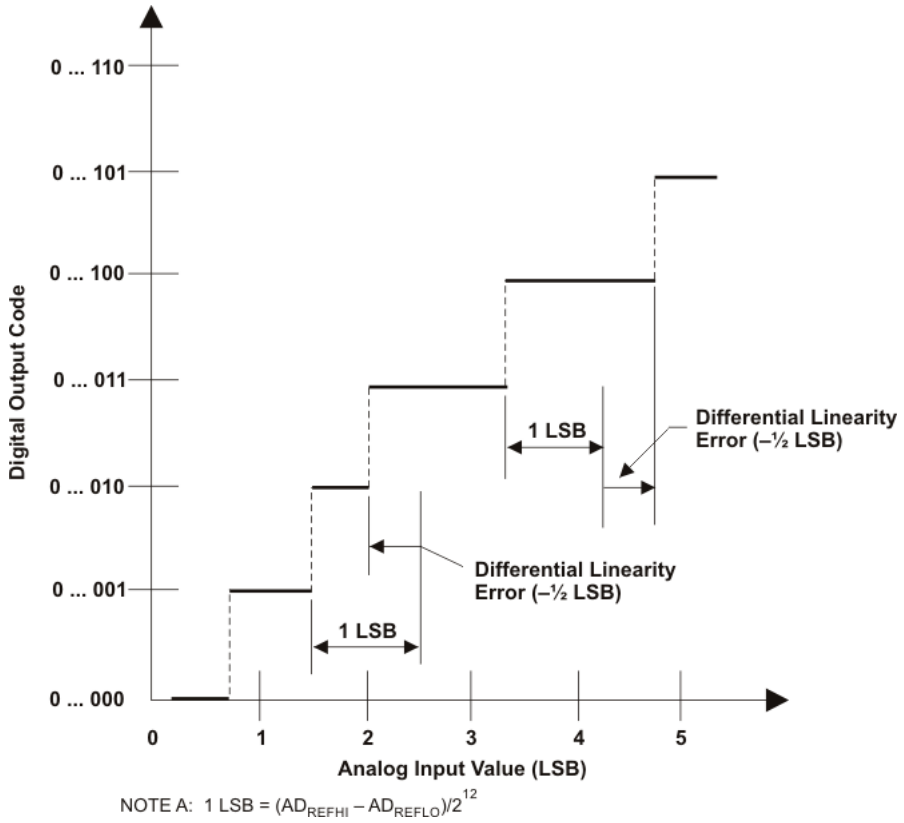

Figure 2.10: Example on differential non-linearity

2.2.1.6 Integral non-linearity

The integral non-linearity (INL) is the deviation of the actual transfer function from the straight line as shown in Figure 2.11. The INL is given by

$$INL(k) = \sum_{i=0}^{k} DNL \tag{2.5}$$

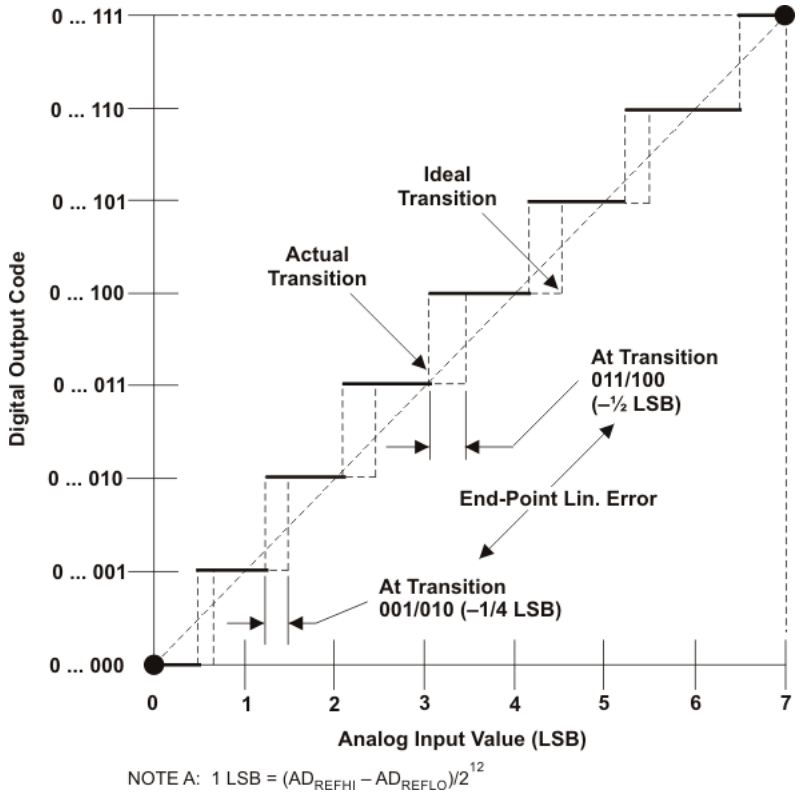

Figure 2.11: Example on integral non-linearity

2.2.1.7 Missing codes

ADC might skip one of its output codes such as in Figure 2.12. Missing some of the output codes is an undesired phenomenon. This phenomenon affects the overall linearity of the ADC badly. If the maximum DNL is smaller than 1 LSB or the maximum INL is smaller than 0.5 LSB, then the ADC is guaranteed not to have a missing codes [1]. So, the INL and DNL are important measures for any ADC.

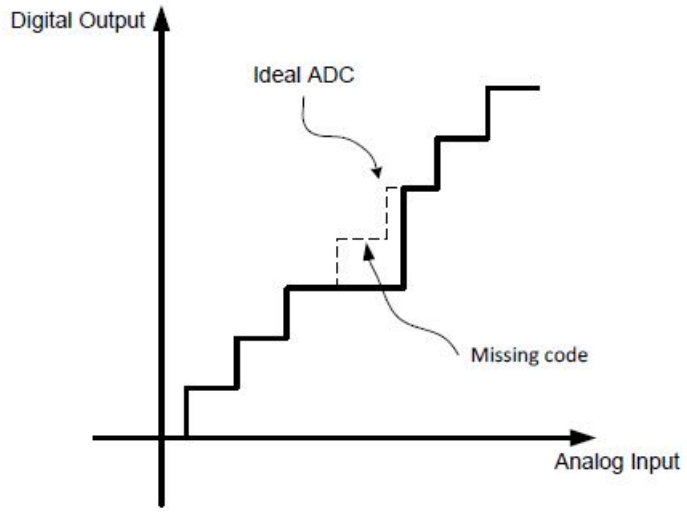

Figure 2.12: Example of Missing Codes [1]

2.2.2 Dynamic specifications

In this section we are going to introduce dynamic, time dependent, specifications for ADCs.

2.2.2.1 ADC conversion time and maximum sampling rate

ADCs have an important metric called conversion time. Conversion time is the time required to acquire an analog input and convert it to a corresponding output code. If conversion time is small, then more samples are converted at the same time interval. The inverse of the conversion time is the maximum sampling rate that is defined as the maximum number of samples that can be converted continuously [1].

2.2.2.2 Signal to noise ratio

Signal to Noise Ration (SNR) is the ratio between the input signal power to the noise power at the output. However, the output noise consists of circuit noise and quantization error [1].

$$SNR = 10 * log(\frac{Full\ scale\ input\ power}{Quantization\ noise\ power\ +\ Circuit\ noise\ power}) dB \tag{2.6}$$

Ignoring the circuit noise power and taking into account the quantization noise power only the SNR is given by:

$$SNR = 6.02 * n + 1.76 \quad (dB) \tag{2.7}$$

As shown in (2.7), as the number of bits, n, increases, the SNR increases.

2.2.2.3 Signal to noise and distortion ratio

Signal to Noise and Distortion Ratio (SNDR) is the ratio of the full scale input power to the noise and distortion power.

$$SNDR = 10 * log(\frac{Full\ scale\ input\ power}{noise\ power + distortion\ power}) dB \tag{2.8}$$

Figure illustrates first, second and third harmonic distortion for an input signal.

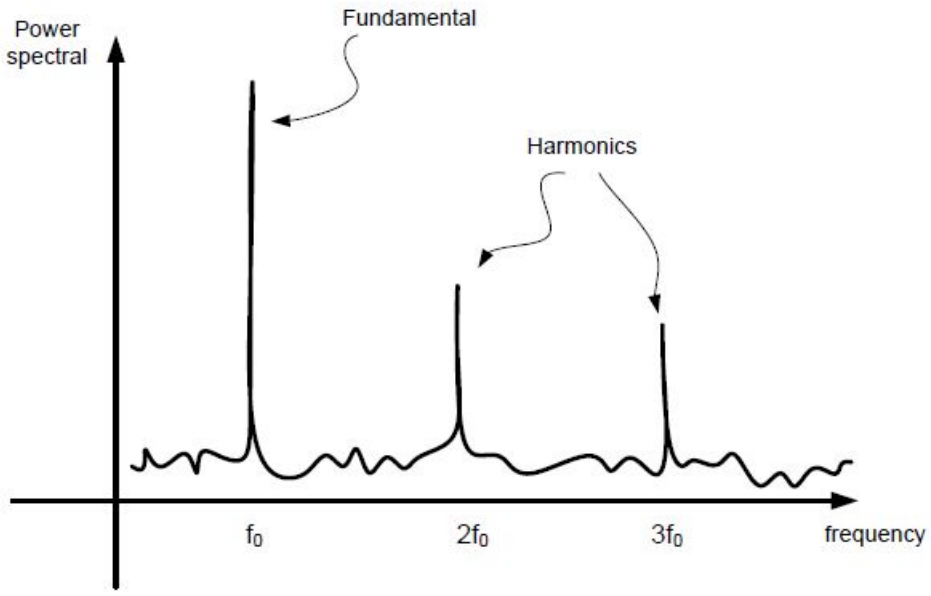

Figure 2.13: Harmonic distortion

2.2.2.4 Effective number of bits

The SNDR of the ADC system is not equal to the ideal SNR. The number of bits directly affected by the ideal SNR as in (2.7).Therefore, the effective number of bits is obtained by the following equation:

$$ENOB = \frac{SNDR\,(dB) - 1.76}{6.02} \tag{2.9}$$

2.3 Linearity Analysis

Linearity is an essential property for any converter. Linearity has to be measured for ADCs, VTCs, TDCs, and Voltage Controlled Oscillators (VCOs). INL, DNL, Total Harmonic Distortion (THD), SNDR, and ENOB are important alternative metrics to measure system linearity. Mainly, ENOB is the most intuitive measure for ADCs [3].

2.4 Traditional ADC types

ADCs are divided into two main categories as shown in Figure 2.14. The first category is direct conversion ADCs; these ADCs convert the analog input voltage directly to output codes. The second category is indirect conversion ADCs. Indirect conversion ADCs convert the analog input voltage to intermediate form like time or frequency. Then, this intermediate form is converted to digital code by digital circuits.

In consonance with sampling frequency each category can be subcategory into two subcategories, Nyquist rate ADCs subcategory and Oversample ADCs. Nyquist rate ADCs sample at rate equal to double the maximum input frequency in order to satisfy Nyquist criteria [7], to reconstruct the sampled signal correctly. Oversample ADCs sample at a rate much higher than Nyquist rate. Thus, this kind of ADCs is suitable for small input frequencies and high resolution[1, 7].

Flash ADC and Successive Approximation register ADC (SAR-ADC) are examples on Nyquist rate direct conversion ADCs and Sigma-Delta modulator ADC is an example on oversampling direct conversion ADC. Single and dual slope ADCs are example on Nyquist rate indirect conversion ADCs. Voltage controlled oscillator ADC is an example on Oversample indirect conversion ADC. In the following subsections the aforementioned examples will be illustrated [1, 2].

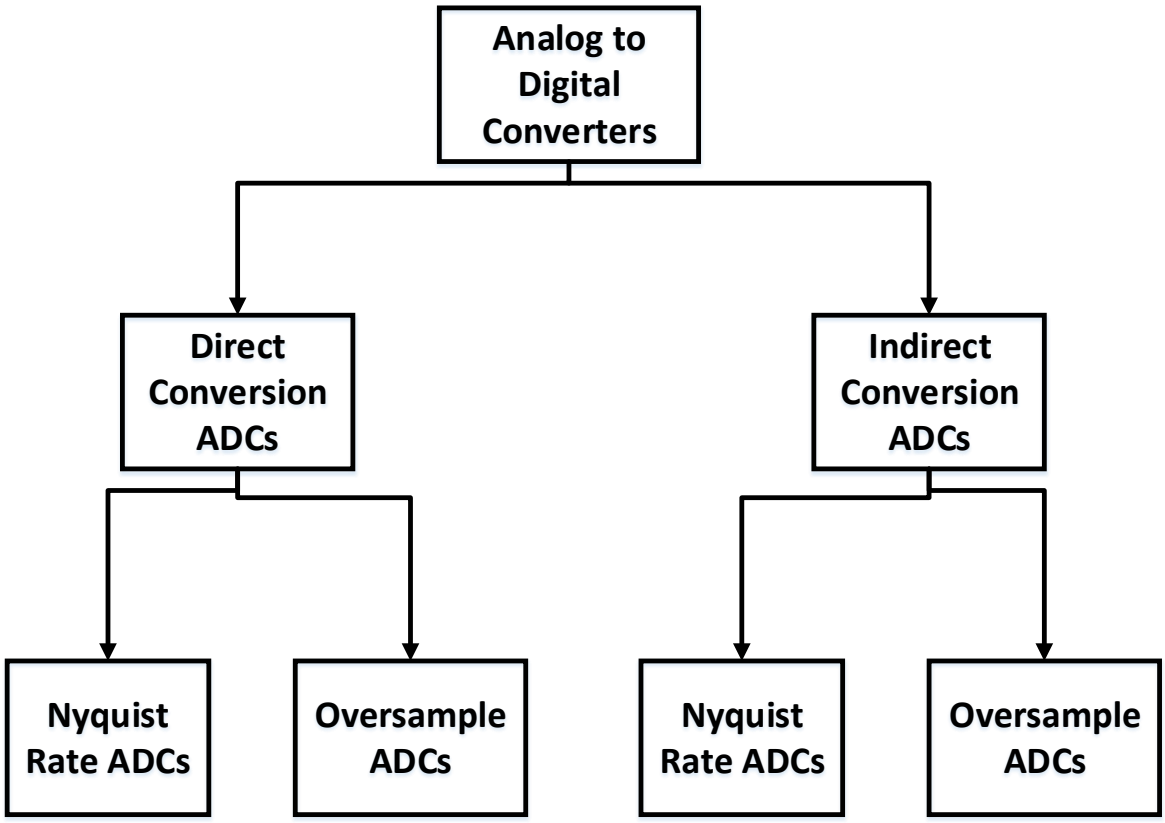

Figure 2.14: ADC Types

2.4.1 Nyquist rate ADCs

2.4.1.1 Flash ADC

Flash ADC is one of the fastest ADCs. N-bit Flash ADC consists of 2^N resistors and 2^{N-1} comparator. The input voltage instantaneously compared to a group of reference voltages, 2^{N-1} reference voltages, each reference voltage is greater than its previous reference voltage by LSB. Resistors are used as a resistive ladder to generate the reference voltages and comparators are used to compare the analog input voltage with the reference voltages. Comparators' outputs are a thermometer code that is converted to a binary code by thermometer to binary decoder.

This ADC has two major drawbacks for this type of ADCs. This ADC contains large number of Op-Amps compared to other types of ADCs. Thus, it consumes large area and power. Nonetheless, this type of ADCs is typically used for low resolution(i.e., less than 8-bit). If the higher resolution is required, the speed of the flash ADC is degraded by the loading effect of the large number of comparators [1].

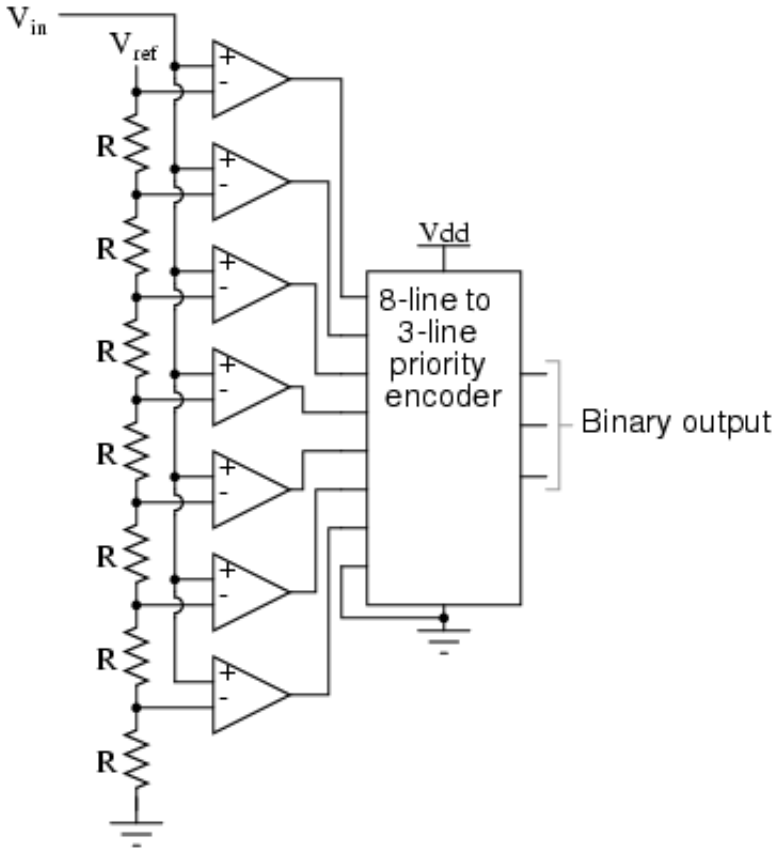

Figure 2.15: Flash ADC

2.4.1.2 Successive Approximation Register ADC

Successive Approximation Register (SAR-ADC) is one of the most successful ADCs and it represents a considerable portion of the market [12]. As shown in Figure 2.16, the basic SAR-ADC consists of comparator, DAC, and Successive Approximation Register (SAR). SAR-ADC takes an iterative approach to determine the input voltage. This iterative approach start from the MSB to the LSB with rate equals to 1 bit/clock. First, the Most Significant Bit (MSB) in SAR starts with one "logic 1". The DAC converts this value to its corresponding voltage, which is the mid-scale voltage, then the comparator compares the input voltage with the reference voltage. If the comparator output is one, then the MSB will be erased. Otherwise, the MSB will remain one. After that, the next bit to the MSB will be one and the whole process is repeated, until all bits in SAR are known and the End Of Conversion (EOC) signal becomes one [1].

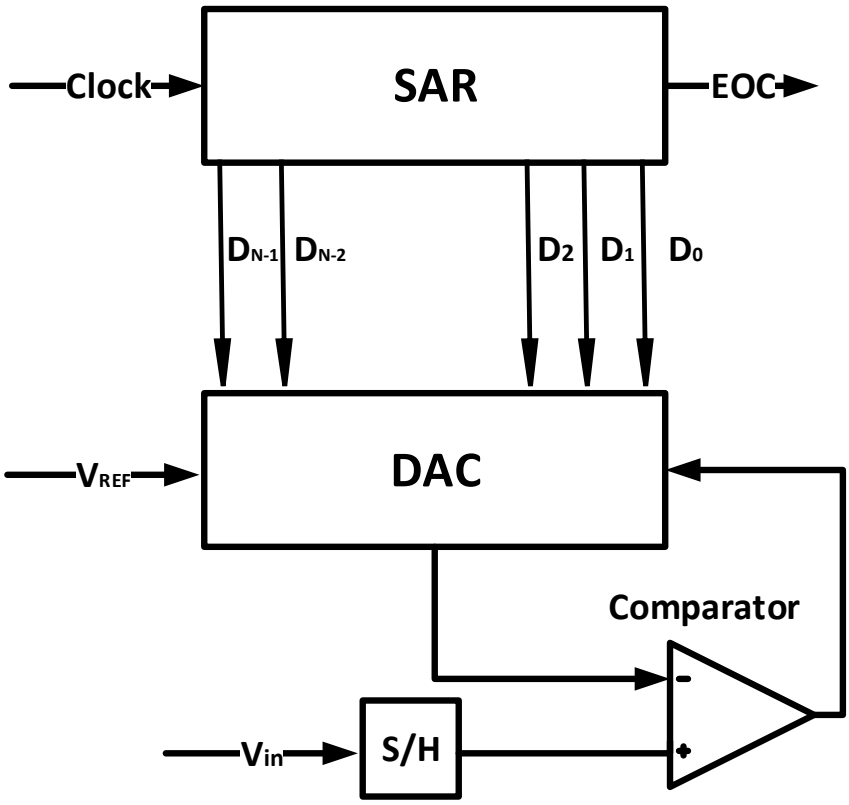

Figure 2.16: Successive Approximation Register ADC

SAR-ADC implements the binary search algorithm as shown in Figure 2.17 and Figure2.18. SAR-ADC works on two different clocks. The internal clock, which works on several Megahertz, and slower external clock. The external frequency is slower than the internal frequency by N, where N is the number of bits. This reduction in external frequency is the main drawback in this ADC [12].

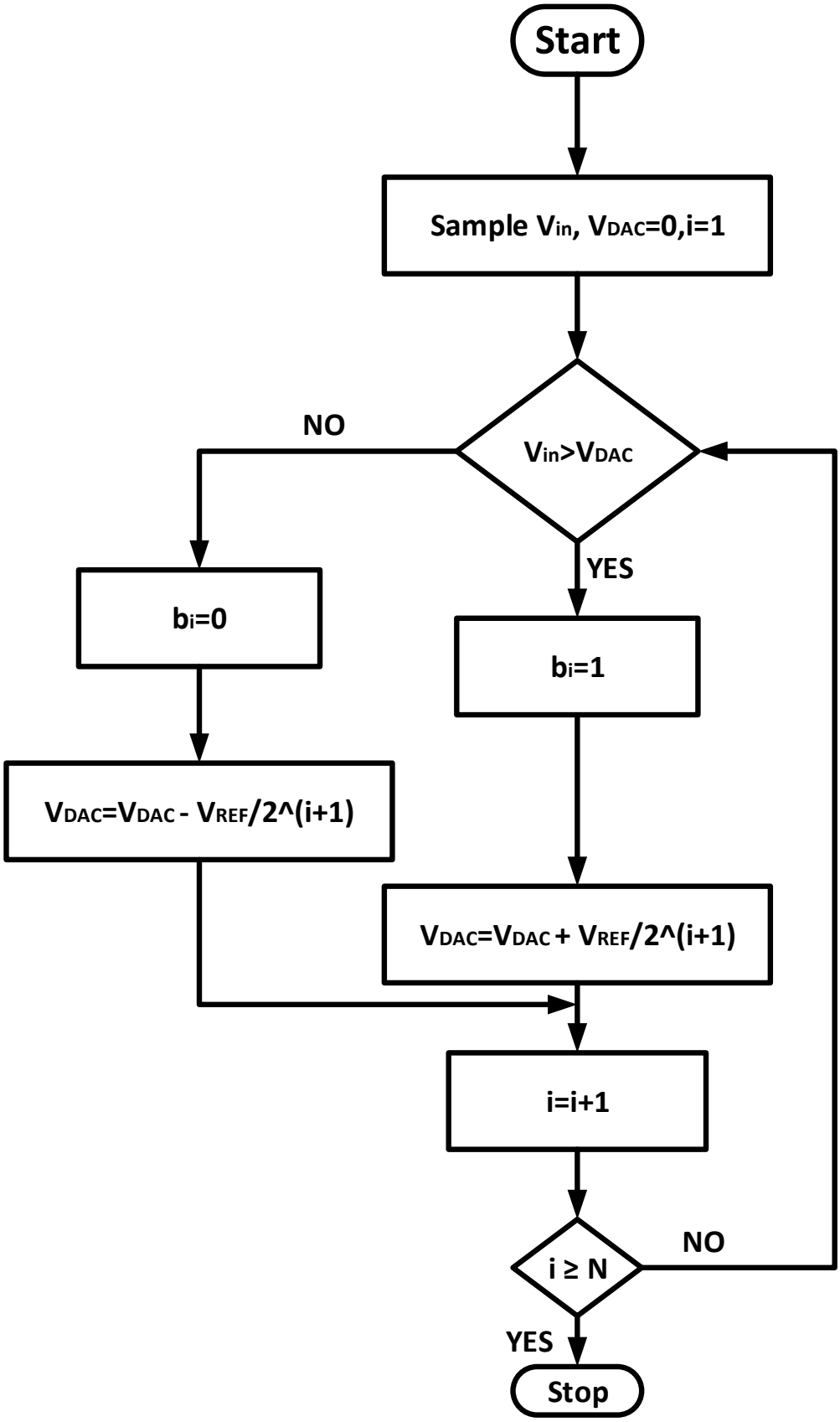

Figure 2.17: SAR-ADC binary search algorithm

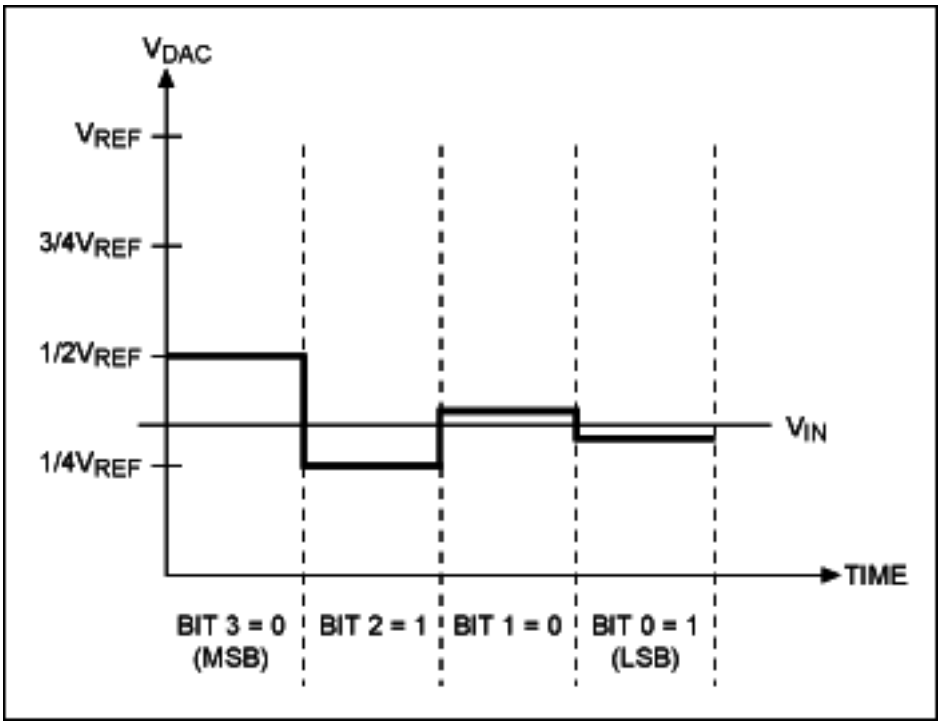

Figure 2.18: Binary Search Algorithm for 4-bit ADC

2.4.1.3 Pipelined ADC

Pipelined ADC is comparable to flash ADC from the throughput perspective and comparable to the SAR-ADC from the resolution perspective. However, the pipelined ADC consume less power and area than the flash ADC.

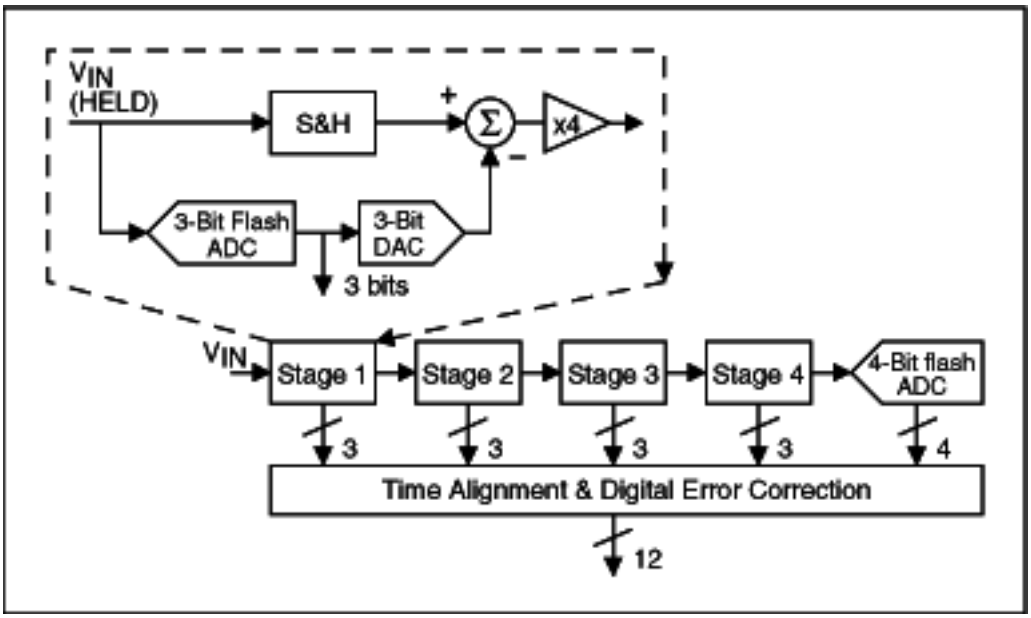

Figure 2.19: System block diagram for pipelined ADC

As shown in Figure 2.19, pipelined ADC consists of K stages. Each stage, except the last stage, consists of n bits flash ADC, n bits DAC, S&H, subtractor, and amplifier. The last stage is a flash ADC. In the first stage the S&H block samples and hold the analog input. Then, this input is fed to the n-bits flash ADC to convert it to n-bit code. Afterwards, the n-bits are fed to n-bits DAC to get intermediate analog voltage. Then, the intermediate analog voltage is subtracted from the original analog input to this stage to produce a residual voltage. This residual voltage will by amplified by 2^nthen fed to the next stage to get new n-bits resolution and so on. while stage number two is working on the first analog voltage stage number one samples new analog input; this pipelining is the main reason for the high throughput. Finaly, all the N-bits have to be aligned because they were generated at different time [1, 12].

2.4.2 Oversampling ADCs

Oversampling ADCs become popular recently because they avoid some of the challenges imposed by Nyquist rate ADCS like the anti-aliasing analog filter [1].

2.4.2.1 Sigma-Delta Modulator

The basic concept of Sigma-Delta modulator is the use of high sampling rate with respect to the Nyquist rate and using the feedback system do decrease the error. The ratio between the sampling frequency and the Nyquist frequency is called the oversampling ratio and it is an important factor at Sigma-Delta modulator design.

Figure 2.20 illustrates first order Sigma-Delta modulator, this is the simplest sigma-delta ADC. The main idea is converting the input voltage to code. Then through the feedback, a DAC is used to convert the code to voltage to be subtracted from the input signal to produce error. If the error term become zero, then we will have a perfect n-bit conversion.

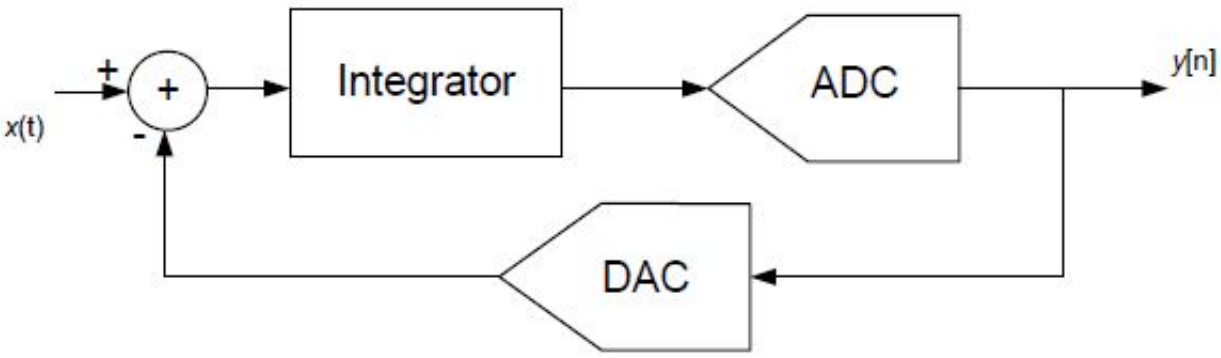

Figure 2.20: Sigma-Delta Modulator [1]

2.5 Time-based ADC types

Time-based ADCs are one form of indirect conversion. First, a converter converts the analog input to intermediate form. Then, a digital circuit converts this intermediate form to output code. For instance, the VTC converts the analog input voltage into a Pulse Width Modulation (PWM) or Pulse Position Modulation (PPM). Afterwards, the TDC converts the pulse width to an equivalent code.

2.5.1 Nyquist rate TB-ADC

2.5.1.1 Single Slop ADC (Integrating ADC)

Single slope ADC or Integrating ADC is one of Nyquist rate time based ADCs. As shown in Figure 2.21 integrating ADC samples , holds the analog input and uses a constant current source to discharge the sample and hold output. After time t the comparator indicates that the discharging is complete. The discharging time, t, the difference between start and stop signals, is proportional to the analog input voltage. The start signal starts a digital counter to count the number of cycles until the stop signal.

Integrating ADC is a simple ADC that consumes small power and provides high resolution. However, its main disadvantage is the sampling rate. It works at low sampling rate and it is suitable for low speed applications [3].

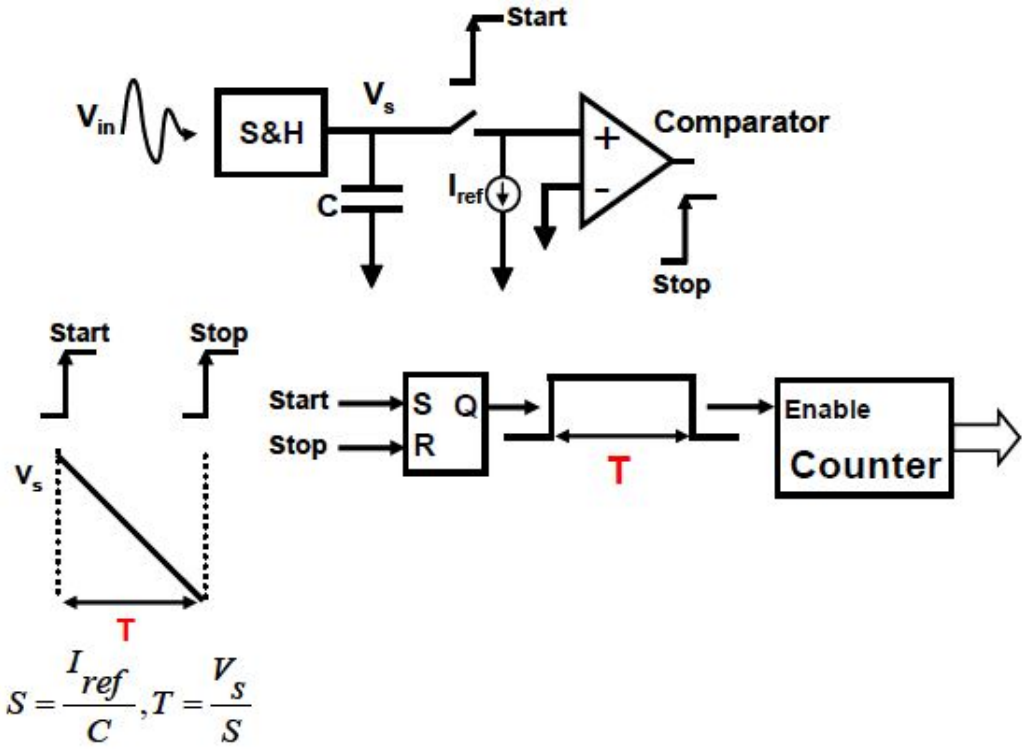

Figure 2.21: Single Slope ADC [3]

2.5.1.2 Dual Slope TB-ADC

Figure 2.22 illustrates dual slope TB-ADC, also denoted by integrating converter TB-ADC, as an example of Nyquist rate ADCs. It is used in high resolution, but low data rates applications. Dual slope TB-ADC has a small offset and gain error comparable to other ADC types[1]. Moreover, it needs a simple circuitry. Dual slope ADC consists of comparator, integrator, counter, and control logic.

First, the analog input, namely V_{in}, is integrated to produce the output voltage, namely$Vout$, in the first part of the clock cycle. V_{out} value depends on the analog input voltage as in equation 2.10. Afterwards, the switch converts from $-V_{in}$to V_{ref} and at this point the discharging starts until the V_{out}reach zero voltage. The discharging time depends on V_{out} that depends on V_{in}. Then, the discharging time will depend on V_{in}as in equation 2.13.

$$V_{out} = \int_0^t -\frac{-Vin}{RC} dt = \frac{V_{in} t}{RC} \tag{2.10}$$

$$V_{out} = \frac{Vin * T_1}{RC} \tag{2.11}$$

$$V_{out} = -\int_{T1}^{t} \frac{V_{ref}}{RC} dt + \frac{V_{in}}{RC} \tag{2.12}$$

$$V_{out} = \frac{V_{in} T_1}{RC} + \frac{V_{ref}(T_1 - t)}{RC} \tag{2.13}$$

The discharging will continue until V_{out}becomes zero. Substituting $V_{out}$by zero in 2.13 leads to equation 2.14 where $T_2 = t - T1$.

$$T_2 = \frac{V_{in}}{V_{ref}} T_1 \tag{2.14}$$

Now, the input voltage is related to the pulse width as shown in equation 2.14. The next step is to convert the time $T_2$to digital code using any ordinary method like the different types of TDCs or counters. One of the main difference between the single and dual slope ADCs is that the dual slope ADC does not depend on the RC in contrast with the single slope ADC[1].

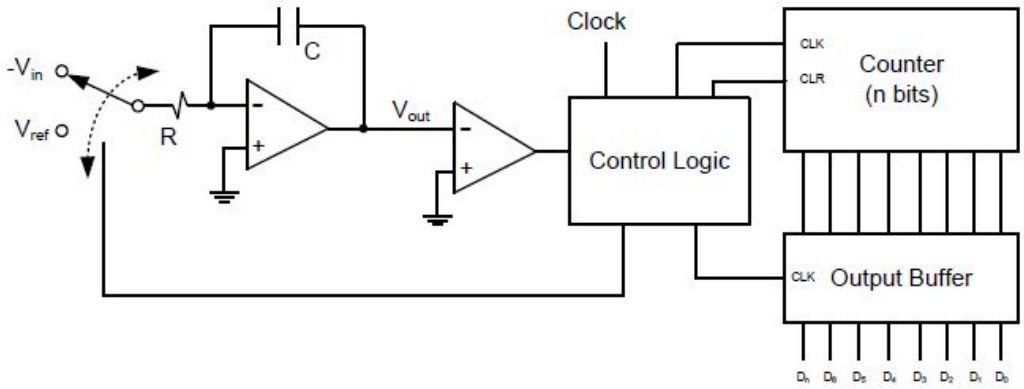

Figure 2.22: Dual Slope ADC [1]

2.5.2 Oversampling TB-ADC

Oversampling TB-ADC depends mainly on angular modulation like frequency or phase modulation [1]. In the following subsections we will introduce exaple on both the frequency and phase modulation.

2.5.2.1 Pulse Width Modulation ADC

Pulse Width Modulation ADC is one of the oldest time-based ADC. PWM ADC shown in Figure 2.23 exists from more than 70-years [2]. It depends on pulse width modulating for the analog input, then converting the PWM to time through a digital counter. This technique depend on converting the amplitude to pulse width. Normally, the PWM distort the signal and to avoid this distortion we have to sample with a rate 8 times grater than the Nyquist rate [2].

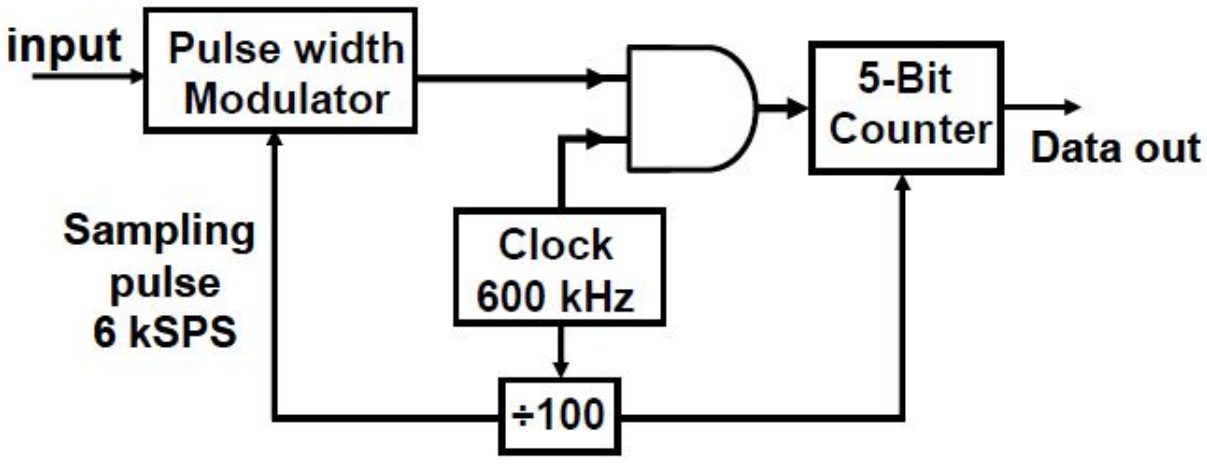

Figure 2.23: Pulse Width Modulation ADC [2]

2.5.2.2 Analog to Time Converter followed by Time to Digital Converter

In this kind of TB-ADC, two steps are required to convert the analog input to digital output code. First, Analog to Time Converters (ATC) convert the analog input to pulse width by phase modulation a reference input clock. Second, the time is quantized using TDCs that convert the pulse width to digital code, many designs applied the aforementioned steps like designs in [13]. Figure 2.24 illustrates the general block diagram for the ATC/TDC systems.

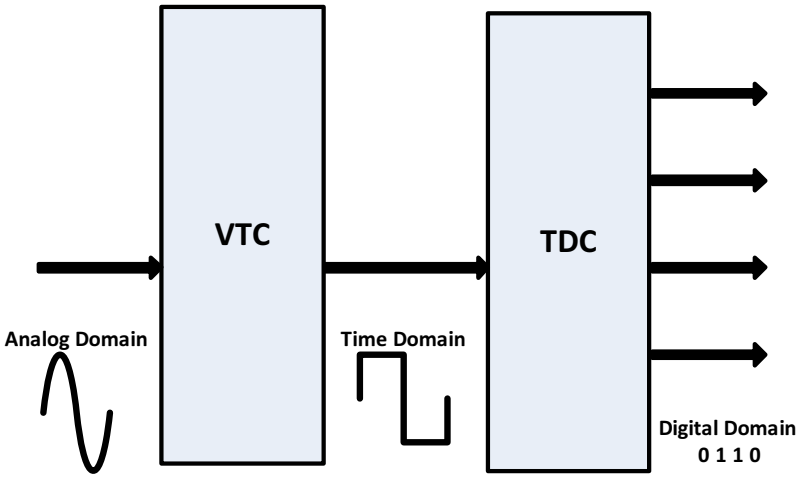

Figure 2.24: System Block Diagram

2.5.2.3 Analog to Frequency Converter followed by Frequency to Digital Converter

In this kind of TB-ADC, two steps are required to convert the analog input to digital output code. First, Analog to Frequency Converters (AFC) convert the analog input to frequency change by Voltage Controlled Oscillator. Second, the frequency is converted to digital code using Frequency to Digital Converters (FDC). Figure illustrates the system block diagram for AFC/FDC systems, this systems were addressed in a lot of publication [1].

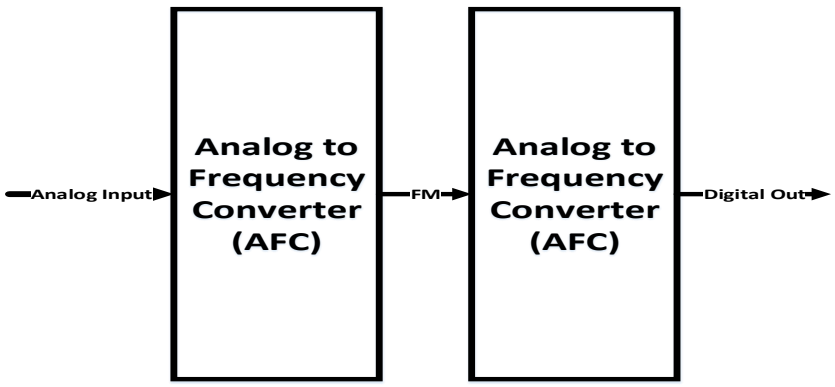

Figure 2.25: AFC/FDC system block diagram

Chapter 3

VTC Analysis and A New Design Methodology for VTC Circuits Suitable for TB-ADCT

Voltage-to-Time Converter (VTC) circuit is considered one of the essential blocks in the design of Time-Based Analog-to-Digital Converters (TB-ADCs). TB-ADC is a promising candidate for Software Defined Radio (SDR) receivers that require wide band and high resolution ADC circuits. TB-ADC circuits provide higher speed and lower power dissipation compared to conventional ADCs. The proposed design methodology increases the dynamic range of the VTC circuits. Moreover, the adoption of this new methodology results in increasing the VTC circuit sensitivity and improving the VTC linearity. In one of the proposed case study, the dynamic range increases up to 550mV with maximum linearity error of 3% and sensitivity of 2.13 ps/mV in TSMC 65nm CMOS technology, with a supply voltage of 1.2V.

3.1 Introduction

SDR receiver becomes an important target for industrial and scientific community. It is one of the most important blocks in UWB receivers. High-speed, high accuracy, and low power ADC is one of the most important blocks in SDR receivers. These requirements of SDR systems cannot be satisfied by the currently available conventional ADC circuits because these conventional ADCs require unaffordable power budget to achieve the wide band and high resolution requirements. Time-based ADCs depend on indirect conversion that needs intermediate step between the analog and the digital domains. The analog voltage is first converted to a pulse width time, by using the VTC circuit, and then this time is converted to a digital word using a TDC circuit as shown in figure 3.1. This type of ADCs consumes less power and occupies less die area than conventional ADC architectures that use direct conversion. In addition, TB-ADCs operate at higher frequency ranges without the sample and hold circuits [14, 15]. In addition, biomedical sensor applications have grown dramatically, and these sensors require low-power and low voltage analog-to-digital converters [16]. For these biomedical sensors requirements, TB-ADC is the best candidate.

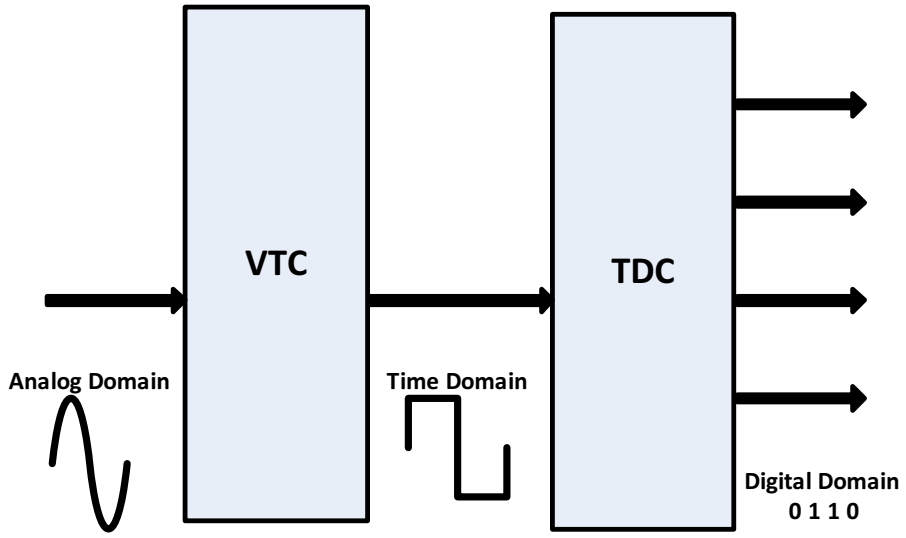

Figure 3.1: TB-ADC block diagram.

As the CMOS technology continues to scale down to the nanometer regime, the supply voltage decreases at a higher rate than the threshold voltage which results in reducing the overdrive voltage (i.e., the difference between the supply voltage and the threshold voltage). However, the noise does not scale down at the same pace like the supply voltage and correspondingly, the ADC experiences Signal-to-Noise Ratio (SNR) degradation [14]. Due to the aforementioned reasons, conventional ADCs do not get any benefits from the CMOS technology scaling. In contrast with conventional ADCs, the time-based ADCs performance is improved as technology scales because one of the main blocks of the T-ADCs is the TDC circuit that is implemented completely by using digital circuits [1].

Several VTCs have been reported in the last few years [14, 15, 17] and [18]. The basic building block in these VTC circuits is the current starved inverter displayed in figure 3.2. In this basic circuit, the fall time depends on the analog input voltage, Vin, applied on transistor M1 gate. The value of this input voltage controls the fall time that makes the pulse width of the output inversely proportional to Vin. The previously published circuits are facing several limitations and design trade-offs. For example, all VTC circuits exhibit a trade-off between linearity and dynamic range (i.e., increasing the dynamic range results in higher non-linearity effects and vice versa). Also, they suffer from limited sensitivity which is defined as the slope of the pulse width versus Vin curve. The proposed design methodology improves the VTC linearity, dynamic range, total harmonic distortion and sensitivity, at the expense of extra area/power overheads.

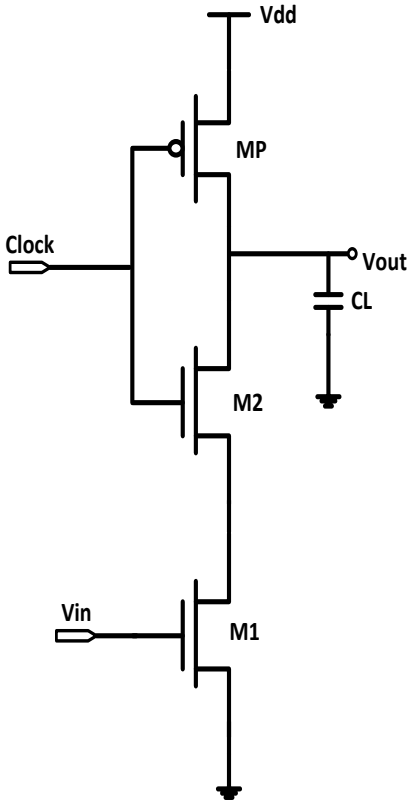

Figure 3.2: Basic current starved inverter.

3.2 Traditional VTC

Each VTC circuit can be implemented using N type transistor as the main transistors, P type transistor as the main transistors, or a hybrid circuit. Traditional VTCs suffer from non-linearity over wide input range.

3.2.1 N-type VTC

Figure 3.5 illustrates the ordinary N-type VTC. The main idea is about making the fall delay at the output of the current starved inverter linear with the input voltage as much as possible.

3.2.1.1 Operation Explanation

N_{a1}, N_{a2}, N_{a3} , and P_{b1} form normal current starved inverter. The input voltage control N_{a2} transistor and the clock controls N_{a3} and P_{b1}. The clock start at logic low where N_{a2} is ideally open circuit and P_{b1} is ideally short circuit. With the rising edge of the clock

signal, P_{b1} transistor becomes open circuit and N_{a1}, N_{a2} , and N_{a3} start to control the inverter output which is a falling edge in contrast with the input clock's rising edge.

Initially, the clock equals to logic low and the output volt, V_{out}, equals to V_{dd}. The transistors namely P_{b1}, N_{a1}, and N_{a2}in figure 3.5 are initially in deep triode region and N_{a3} is in cut-off. With the rising edge of the clock, transistor P_{b1}enter the cut-off region and transistor N_{a3} enters the saturation region driving $N_{a1}$and N_{a2} to enter the saturation region as well.

Afterwards, the voltage at the drain of $N_{a1}$and N_{a2}will increase rapidly driving both transistor to be in saturation region. This makes the current flowing through N_{a3} transistor maximum and constant as $I_{tot} = I_{Na1} + I_{Na2}$ where N_{a1} and N_{a2} are in saturation region. The slope of the discharging ramp will be $S_{ramp} = \frac{C_{out}}{I_{tot}}$ where $I_{max} = \frac{1}{2}\mu_n C_{ox}\frac{W_{Na1}}{L}[V_{in} - V_{th}]^2 + \frac{1}{2}\mu_n C_{ox}\frac{W_{Na2}}{L}[V_{dc} - V_{th}]^2$.

Then N_{a3} drain voltage will decrease as the output voltage decrease and N_{a3} region of operation becomes triode. However, N_{a1} and N_{a2} are saturation and their current is maximum. The linearity of the ramp are affected by N_{a1} and N_{a2} because N_{a3} does not affect the discharging current.

Finally, one of the two main transistors N_{a1}or N_{a2}will enter the triode first leading to non-linear ramp and soon the second transistor will enter the triode also until reaching the steady state where N_{a1}, N_{a2}, and $Na3$ are in deep triode; so the threshold of the state driven by the current starved inverter should be reached before entering the triode region [3].

Figure 3.3 shows the important phases at wich the relation between the input voltage and the discharging current has to be linear, afterwards one of the main transistors enters the triode and the discharging time becomes non-linear.

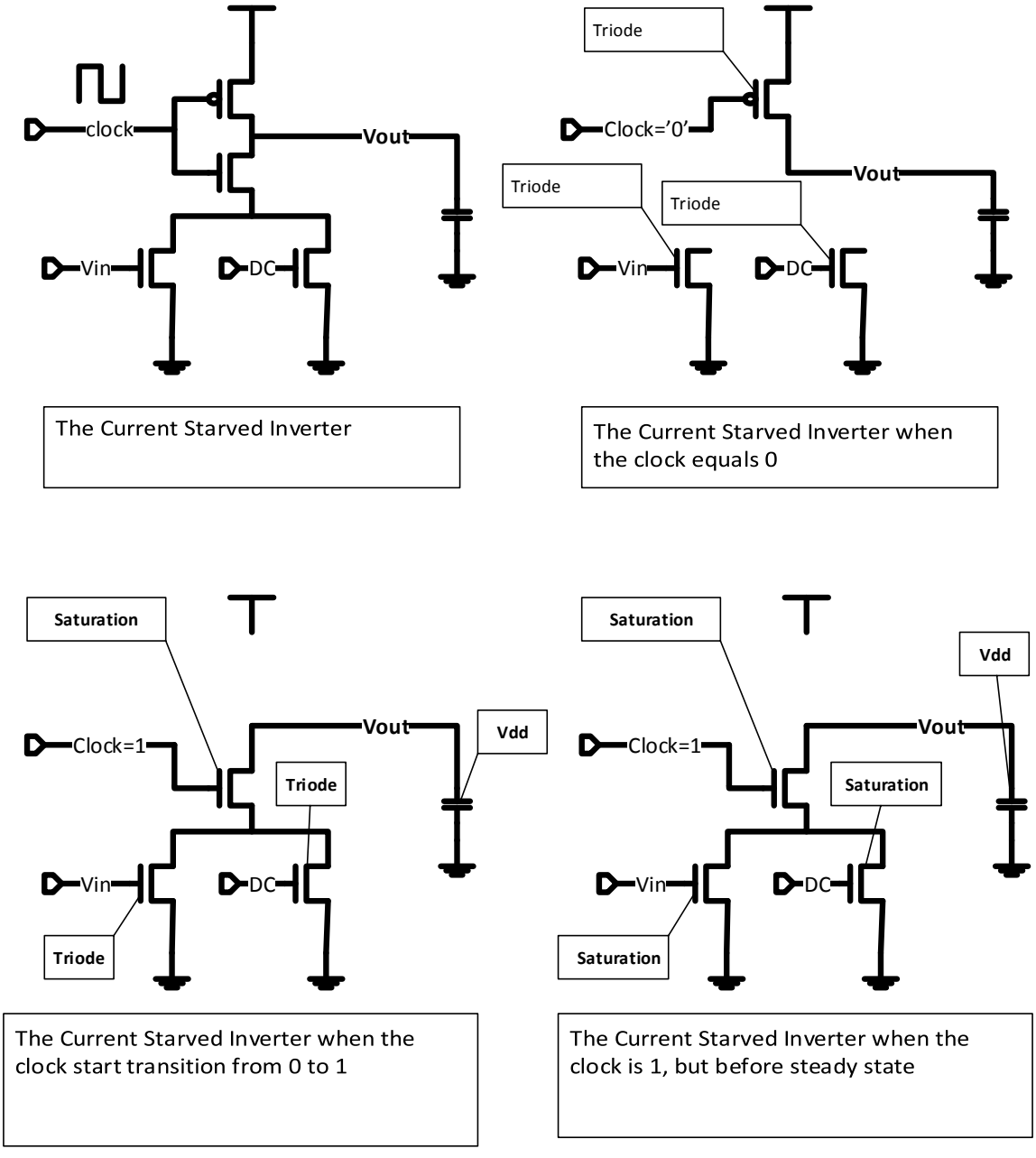

Figure 3.3: The Current sturved inverter linear phases

3.2.2 The inheret sample and hold for the N-type VTC

The time based ADC that contains VTC can illuminate the use of Sample and Hold (S/H) circuit up to certain frequency f_{MAX}, after this frequency the used of the sample and hold circuit becomes a must. In the proposed VTC the circuit has an inherited S/H unlike the designs in [13].

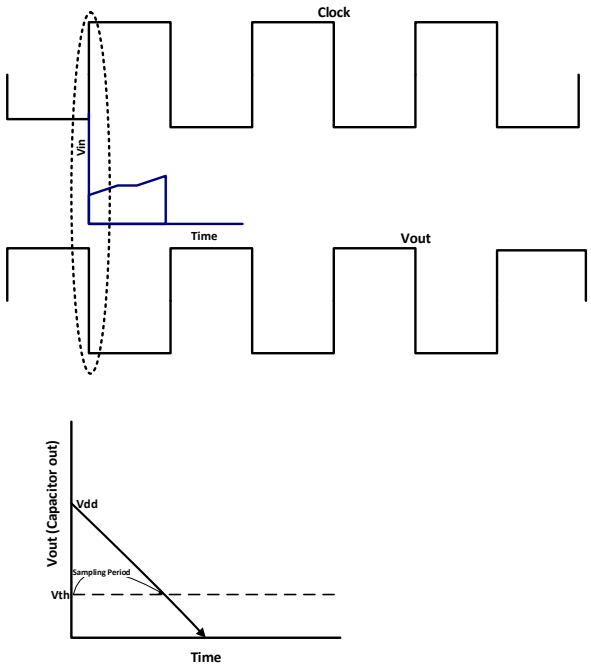

Figure 3.4: The inherent Sample and Hold operation in VTC

Figure 3.4 illustrates the basic S/H operation. With the rising of the clock edge the output starts to fall down with rate dependent on the input voltage. If the input signal is slow relative to the clock as in figure 3.4 the input voltage at the rising clock can be considered constant and the discharging will be linear as in the zoomed part in the figure. The output discharge until reaching the threshold voltage of the next stage, normally equals to $\frac{V_{dd}}{2}$, after that the discharging curve is not effective. The hole operation repeats itself again with the next rising edge. For further investigation refer to [1].

3.3 Proposed Design Methodology

This Methodology is based on the complementary behavior between the pull-down network and the pull-up network. This makes the proposed design methodology similar to the CMOS logic design methodology as portrayed in figure 3.5 and figure 3.6. The pull-down network consists of n-channel transistors, carrying a current that is proportional to Vin. Thus, the required time to discharge the output capacitor ,denoted by the fall time Tf_{th}, is inversely proportional to Vin. The pull-up network exhibits opposite behavior, where the required time to charge the output capacitor is denoted by the rise time, Tr_{th}.

The difference between Tf_{th} and Tr_{th} have to be maximized to improve the ADC dynamic range; Thus, the pull-down network is designed to be faster to increase the dynamic range.

It is shown mathematically that the subtraction of the Tr_{th} and Tf_{th} curves have a more linear behavior than each curve of them due to the non-linearity error cancellation between the two curves, which extends the dynamic range of the proposed methodology circuit, and provides a lower Total Harmonic Distortion (THD) as illustrated in the following sections.

This new methodology can be applied on any current-starved inverter based VTC circuit available in the literature. To apply the proposed methodology, a complementary VTC circuit is designed (For example, if the original VTC circuit depends on controlling the fall delay by Vin, the complementary circuit should be designed such that the rise delay is controlled by Vin, and vice versa). Following that, the outputs of both VTC circuits (i.e., the original VTC and the complementary VTC) are applied as inputs to an XNOR gate to get the difference between the rise delay and the fall delay as illustrated in Figures 3.7 and 3.8.

3.3.1 Circuit Description

In this subsection, the proposed methodology is applied on a selected VTC circuit from literature as a case study. Figure 3.5 illustrates the basic current starved inverter, denoted by the falling circuit or the original VTC circuit. An NMOS transistor, Na1, is added to limit the maximum discharge time in case Vin is lower than the threshold voltage of transistor Na2. Figure 3.6 displays the complementary VTC circuit of the original VTC circuit portrayed in figure 3.5, this complementary circuit is denoted by the rising circuit. This circuit uses an inverted delayed version of the original clock signal applied to the original VTC circuit. Similarly, if the difference between the source of transistor Pb2 and its gate is less than the threshold voltage, transistor Pb3 is used to limit the rise time of the complementary circuit.

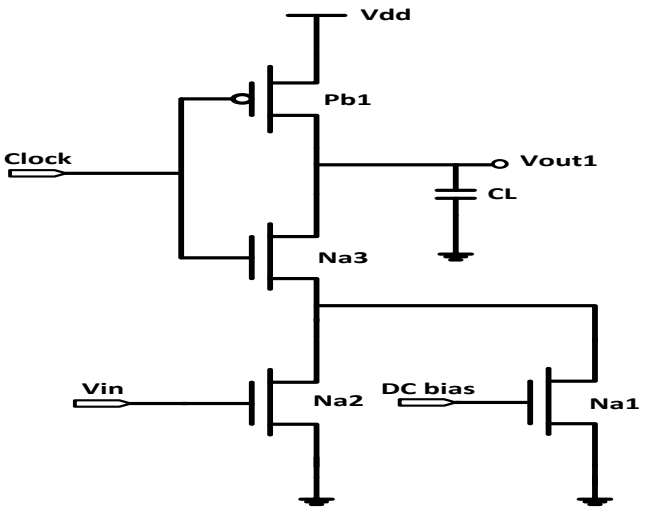

Figure 3.5: Original VTC circuit.

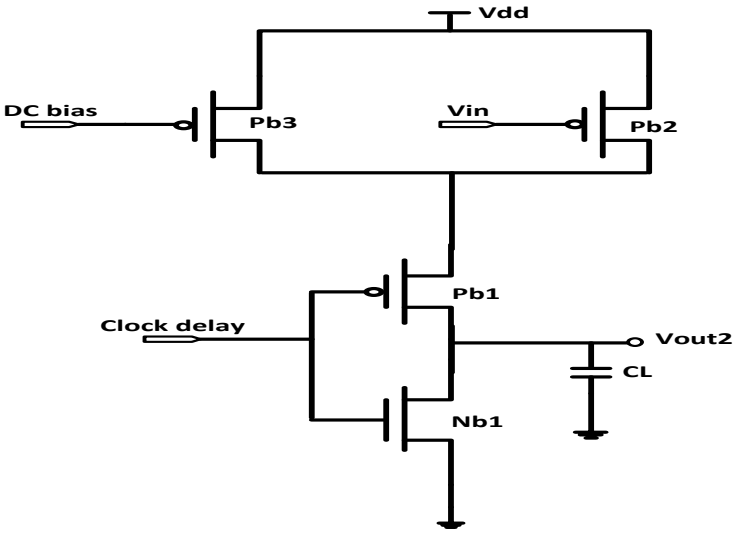

Figure 3.6: Complementary VTC circuit.

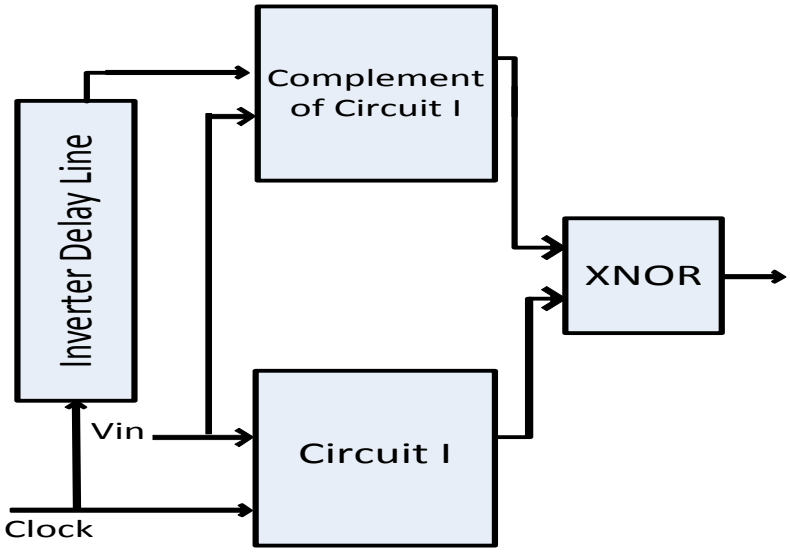

Figure 3.7: Proposed methodology block diagram.

In Tables 3.1 and 3.2, all the transistor sizes and the dc bias voltages, selected based on the analytical analysis given in the following subsection, are tabulated. Figure 3.8 shows the corresponding timing diagram of the proposed new methodology. For a given input voltage, the pulse width of the output signal is $\Delta + Tr_{th} - Tf_{th}$, where Tr_{th} is the rising circuit delay, Tf_{th} is the falling circuit delay, and Δ is the delay of the inverted clock version applied on the complementary VTC circuit. The sizing of the transistors is carried out to maximize the term $Tr_{th} - Tf_{th}$. To maximize the rising time, Tr_{th}, the effective transistor,

Pb_2, in the rising circuit is designed to be minimum size but greater than the DC biased transistor, Pb_3, to dominate the rising time. To minimize the falling time, Tf_{th}, the falling circuit is designed to discharge rapidly the load capacitor by increasing the width of the input transistor Na_2.

Parameter	Value
W_{Na1}	120 nm
W_{Na2}	1.44 µm
W_{Na3}	1.2 µm
W_{Pa1}	2.4 µm
L	80 nm
DC_{bias}	600 mV

Table 3.1: Falling circuit parameters

Parameter	Value
W_{Pb3}	120 nm
W_{Pb2}	240 nm
W_{Pb1}	2.4 µm
W_{Nb1}	1.2 µm
L	80 nm
DC_{bias}	600 mV

Table 3.2: Rising circuit parameters

3.3.2 Analytical Analysis

The VTC circuits displayed in figure 3.5 and figure 3.6 are analyzed and compared with the proposed new methodology to show the strength of the proposed methodology. The load capacitance, C_L, is 30 fF in all cases representing the FO4 load capacitor. In the falling circuit, when the clock signal is zero, the load capacitor is charged to Vdd, transistors Na_1, Na_2, and $Pb_1$are in the deep triode region, and transistor Na_3 is in the cut-off region. When the clock goes high, transistor Na_3turns on and the capacitor discharges through transistors Na_1, Na_2, and Na_3 based on equation (3.1). The objective is to find the threshold fall time required to discharge the capacitor to the threshold voltage of the next state (i.e., $0.5 * Vdd$) as given by the following equations, where more details are provided in [1, 3].

$$I_f = -C_L \frac{dV_{out1}}{dt} \tag{3.1}$$

$$I_f = I_{Na1} + I_{Na2} \tag{3.2}$$

$$I_f = \frac{1}{2}\mu_n C_{ox} \frac{W_{Na1}}{L}[V_{DC} - V_{th}]^{\alpha_n} + \frac{1}{2}\mu_n C_{ox} \frac{W_{Na2}}{L}[V_{in} - V_{th}]^{\alpha_n} \tag{3.3}$$

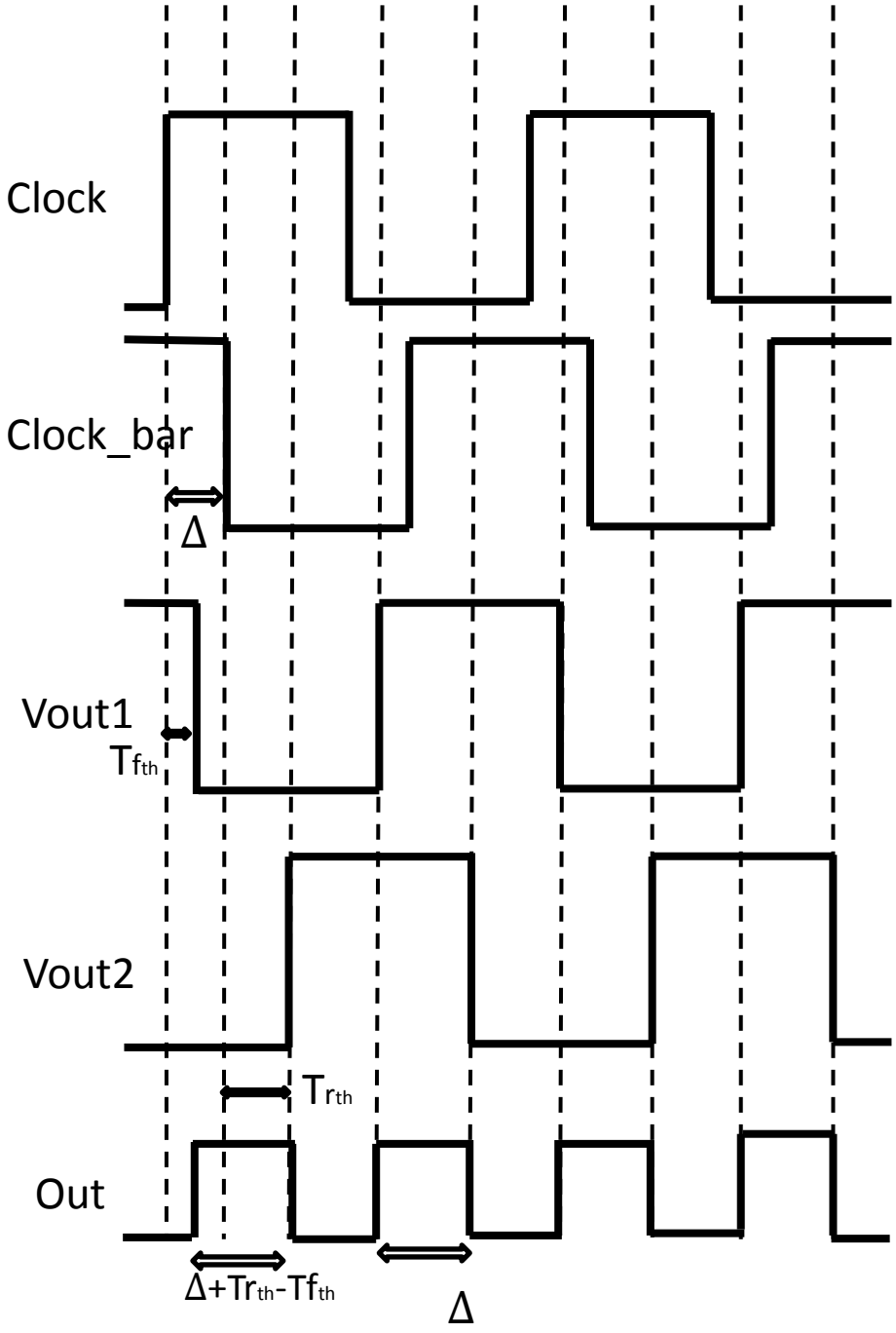

Figure 3.8: Timing diagram for the VTC circuit [14]

$$-C_L\frac{dV_{out1}}{dt} = \frac{1}{2}\mu_n C_{ox}\frac{W_{Na1}}{L}[V_{DC}-V_{th}]^{\alpha_n} + \frac{1}{2}\mu_n C_{ox}\frac{W_{Na2}}{L}[V_{in}-V_{th}]^{\alpha_n} \tag{3.4}$$

$$\int_{V_{dd}}^{0.5V_{dd}} -C_L dV_{out1} = \int_{0}^{Tf_{th}} (I_f)\,dt \tag{3.5}$$

$$Tf_{th} = \frac{C_L Vdd}{2 * I_f} \tag{3.6}$$

The same analysis is performed for the rising VTC circuit (i.e., the complementary circuit) to determine the rise threshold time as in (3.8). The pulse width of the rising circuit, falling circuit, and the proposed methodology is $\mathrm{Tr_{th}}$, $\mathrm{Tf_{th}}$, and $\mathrm{Tmeth_{th}}$ respectively. Where $\mathrm{Tmeth_{th}}$ is the difference between the rising and the falling times, in addition to a constant delay from the inverted delay line as in figure 3.8.

$$I_r = \frac{1}{2}\mu_p C_{ox}\frac{W_{Pb3}}{L}[Vdd-V_{DC}-V_{th}]^{\alpha_p} + \frac{1}{2}\mu_p C_{ox}\frac{W_{Pb2}}{L}[Vdd-V_{in}-V_{th}]^{\alpha_p} \tag{3.7}$$

$$Tr_{th} = \frac{Vdd * C_L}{2 * I_r} \tag{3.8}$$

$$Tmeth_{th} = \Delta + Tr_{th} - Tf_{th} \tag{3.9}$$

where I_f, I_r, I_{Na1}, and I_{Na2} are the capacitor current in the falling circuit, the capacitor current in the rising circuit, the transistor $Na1$ current, and the transistor $Na2$ current, respectively; and V_{DC}, V_{th}, $\mu_n C_{ox}$, W_{Nai}, and L are the DC bias voltage, the threshold voltage, the electrons mobility multiplied by the oxide capacitance, the width of the i_{th} transistor, and the channel length, respectively. α_n and α_p represent the effect of short channel in modern technologies and they are called the velocity saturation indices. As mentioned in [19], α_n and α_p decreased from 2 to about 1 monotonically based on whether the transistor is in velocity saturation or pinch off saturation.

The following equations represent the Taylor series expansions for Tf_{th}, Tr_{th}, and $Tmeth_{th}$. They help in illustrating the most effective parameters in the linearity error curve displayed in figure 3.12. This linearity error curve is optimized based on these coefficients, and proves the higher linearity nature for the proposed new methodology.

$$Tf_{th} = a_0 + a_1(V_{in}) + a_2(V_{in}-V_{const})^2 + \cdots + a_n(V_{in}-V_{const})^n \tag{3.10}$$

$$Tr_{th} = b_0 + b_1(V_{in}) + b_2(V_{in}-V_{const})^2 + \cdots + b_n(V_{in}-V_{const})^n \tag{3.11}$$

$$Tmeth_{th} = c_0 + c_1(V_{in}) + c_2(V_{in}-V_{const})^2 + \cdots + c_n(V_{in}-V_{const})^n \tag{3.12}$$

where a_i, b_i, and c_i are the i_{th} terms of the Taylor coefficients for Tf_{th},Tr_{th}, and $Tmeth_{th}$ respectively and V_{const} is the point at which the Taylor expansion is centered. These coefficients in (3.10), (3.11), and (3.12) are used to calculate the THD and their corresponding dynamic ranges as in [20]. Also, they are used in optimizing the VTC.

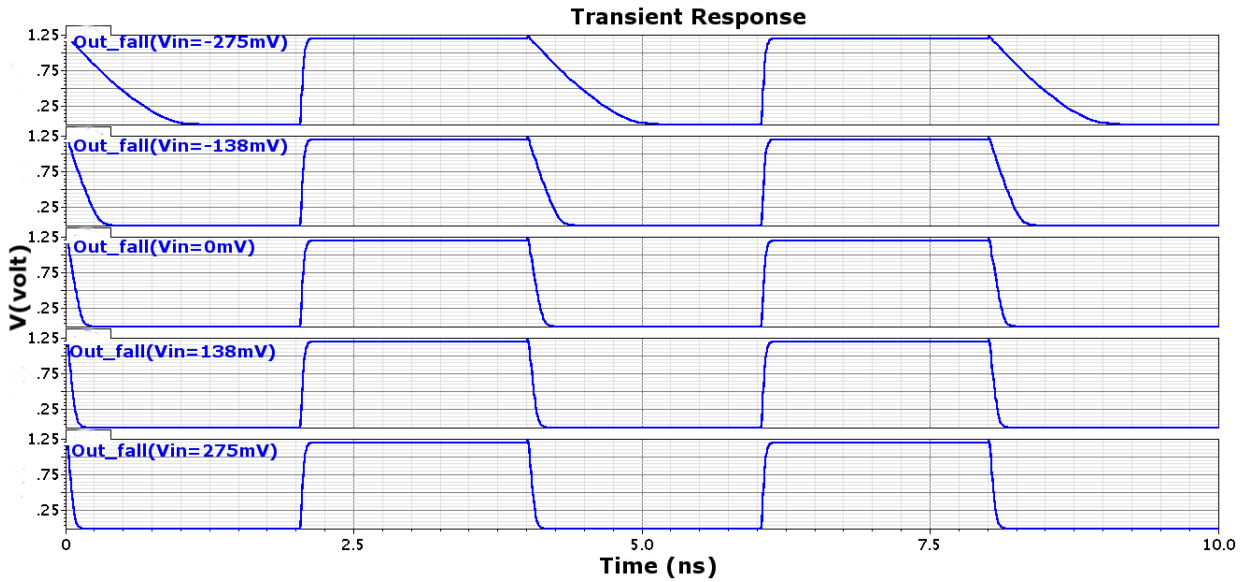

Figure 3.9: Sample of the output of the original falling VTC circuit at different input voltage values.

Our objective is to get a linear relation between the pulse width, namely Tr_{th}, $Tf_{th}, or \quad Tr_{th} - Tf_{th}$, and the input voltage, Vin, over the largest possible dynamic range with the highest sensitivity. The proposed methodology, that results from the difference between the rise time and the fall time, exhibits better linearity over the same dynamic range compared to the original VTC circuit or the complementary circuit as shown in figure 3.12.

3.3.3 Simulation Results and Discussions

The VTC specifications parameters such as sensitivity, linearity, dynamic range, and power dissipation are calculated by sweeping the input voltage. The simulations are carried out on Cadence Virtuoso using industrial hardware-calibrated TSMC 65nm CMOS technology, with supply voltage of 1.2V. Figures 3.9, 3.10, and 3.11 show the outputs of the circuits displayed in Figures 3.5, 3.6, and 3.7, respectively by sweeping the input analog voltage from $-275mV$ to $275mV$ superimposed on $675mV$ dc voltage.

For the original falling VTC circuit, the pulse width decreases as the input voltage increases. However, the pulse width of the complementary rising VTC circuit increases as the input voltage increases. This results in an overall pulse width that increases at a rate approximately equal to both the rise and falling VTC circuits rates. It is clear from Tables 3.3, 3.5, and 3.4 that the proposed methodology provides higher sensitivity than that of the original falling VTC. Moreover, the proposed methodology exhibits higher linearity as demonstrated in Figure 3.12. As shown in Figure 3.12, the maximum linearity error in the original falling VTC circuit is 33.87%, and in the complementary rising VTC circuit is 5.85%. However, the maximum linearity error in the proposed new methodology is 3%. The sensitivity of the original falling VTC circuit, the complementary rising VTC

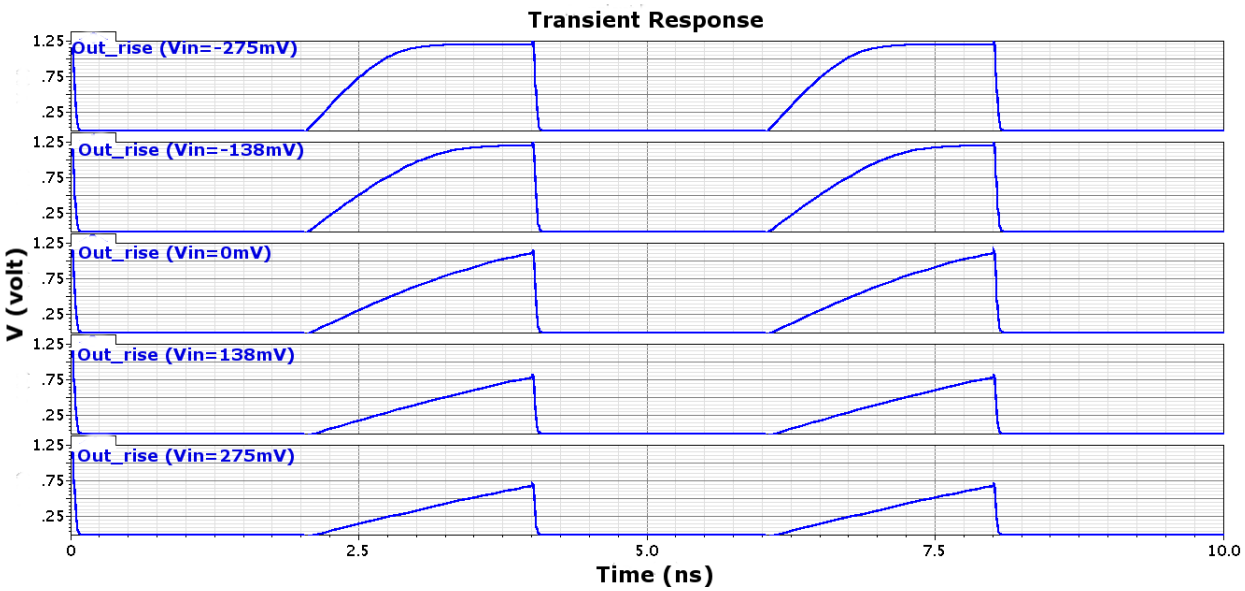

Figure 3.10: Sample of the output of the complementary rising VTC circuit at different input voltage values.

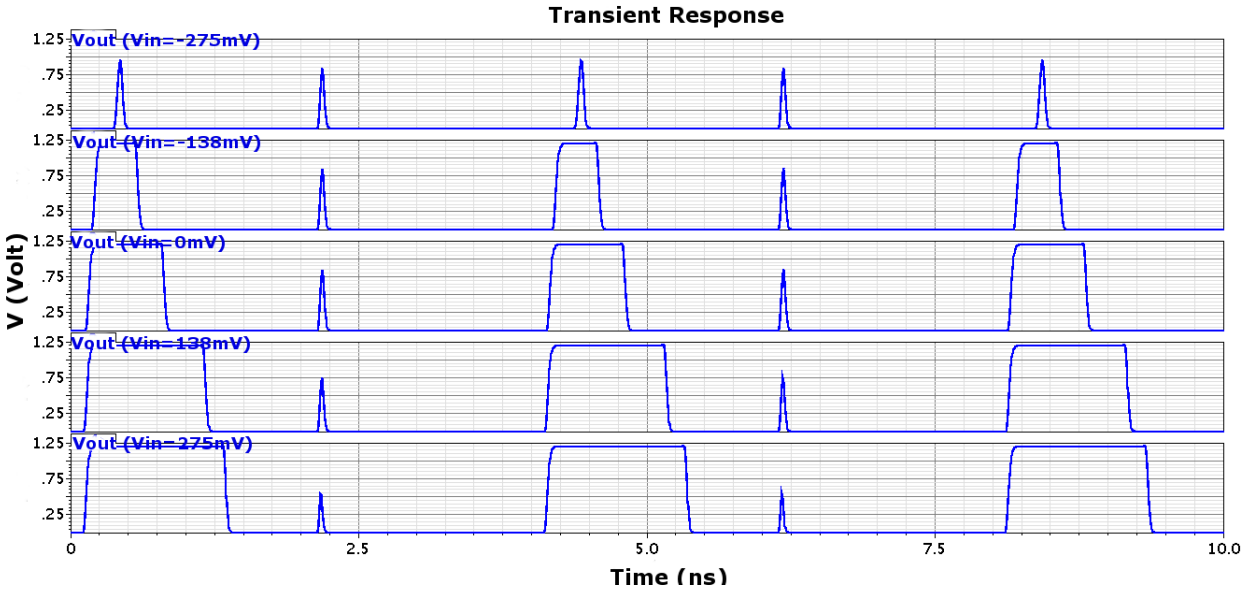

Figure 3.11: Sample of the output of the proposed methodology VTC circuit at different input voltage values.

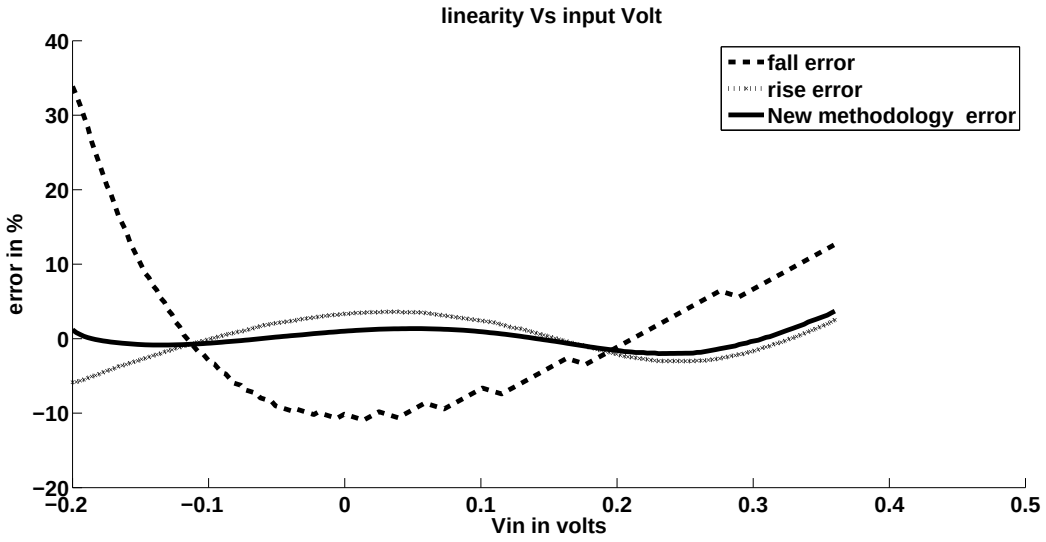

Figure 3.12: Linearity error for the falling, rising, and the new methodology as input change from $-275mV$ **to** $275mV$**.**

Parameter	Falling	Rising	Methodology
ϵ	33.87%	5.85%	3%
THD	$-4.77dB$	$-11.87dB$	$-20dB$
σ	$0.64mV/ps$	$2.45mV/ps$	$2.13mV/ps$

Table 3.3: Comparison between the three circuits for a fixed dynamic range $550mV$

circuit, and the proposed new methodology is $0.64ps/mV$, $2.45mV/ps$, and $2.13mV/ps$, respectively.

Tables 3.3, 3.4,and 3.5 tabulate some of the simulation results. In both tables the Dynamic Range (DR), the sensitivity (σ), and the linearity error (ϵ) are given. The main drawbacks of the proposed new methodology is the area and power overheads. However, this overhead is still small compared to the overall T-ADC power and area and compared to conventional ADCs. The XNOR gate used in this proposed methodology designed by using transmission gate transistor logic to reduce the power and area overhead.

The small glitch on the proposed methodology output at figure 3.11 can be eliminated by two technique. The first one is by masking it with the clock signal. The second one is performed through the digital TDC part. Optimization of the proposed methodology is our active current research work as well as adopting this design methodology on other current-starved inverter based VTC circuits in the literature and investigating how the new methodology act under PVT variation compared to the falling and the rising VTCs.

The Total Harmonic Distortion (THD) is calculated for the three VTC circuits to show the strength of the proposed new methodology. For a fixed dynamic range of 550mV, the new methodology exhibits smaller THD compared to the original VTC and the complementary VTC by 15dB and 8.2dB, respectively as illustrated in table 3.3. Moreover, table 3.3 illustrates the improvement in the linearity error over the falling and rising circuits.

Parameter	Falling	Rising	Methodology
DR	$80mV$	$140mV$	$550mV$
ϵ	10.14%	3.6%	3%
σ	$0.64ps/mV$	$2.45ps/mV$	$2.13mV/ps$

Table 3.4: Comparison between the three circuits For the same maximum THD $-20 dB$

Parameter	Falling	Rising	Methodology
DR	$240mV$	$400mV$	$550mV$
THD	$-9.9dB$	$-12.45dB$	$-20dB$
σ	$0.64mV/ps$	$2.45mV/ps$	$2.13mV/ps$

Table 3.5: Comparison between the three circuits for a fixed maximum error 3%**.**

Table 3.4 shows the dynamic range of the new methodology and the original complementary VTC circuits for a fixed THD of -20dB. The dynamic range of the proposed new methodology is improved by factors of 6.9X and 3.9X over the original and complementary circuits, respectively for the same THD of -20dB. In addition, the maximum dynamic range is 2.75X wider than [15] and 3.7X wider than [14].

The dynamic range of the proposed new methodology is improved by factors of 2.3X and 1.4X over the original and complementary circuits, respectively for a fixed maximum linearity error of 3% as in table 3.5.

Table 3.6 shows the power dissipation and gate area of the falling, rising, and the new design methodology circuits. The large difference in power and area, between the new methodology and the other circuits, is due to the large buffer at the XNOR gate that consumes a short circuit power. This short circuit power reduction is our current research work.

Walden in [21] defined a Figure Of Merit (FOM) to be used in the ADCs which is $FOM = \frac{DR^2 * f}{P}$. Where DR, f, and P are the dynamic range, the maximum frequency of operation, and the power dissipation. The FOM represents the efficiency of using the power to increase the DR and/or the maximum frequency. The maximum frequency range for the falling, rising, and the proposed new methodology are 1600 MHz, 285 MHz, and 700 MHz respectively calculated for the dynamic ranges in table 3.4. The FOM for the falling circuit, rising circuit, and the new design methodology are $1 * 10^{12}$, $0.14 * 10^{12}$, and $3.4 * 10^{12}$ respectively. The aforementioned FOM shows the strength of the new design methodology over both the falling and rising VTC circuits.

Parameter	Falling	Rising	Methodology
$Area$	$0.4128\mu m^2$	$0.3168\mu m^2$	$4.2872\mu m^2$
$Power$	$9.65\mu W$	$9.138\mu W$	$61.86\mu W$

Table 3.6: Comparison between the three circuits for Area and Power.

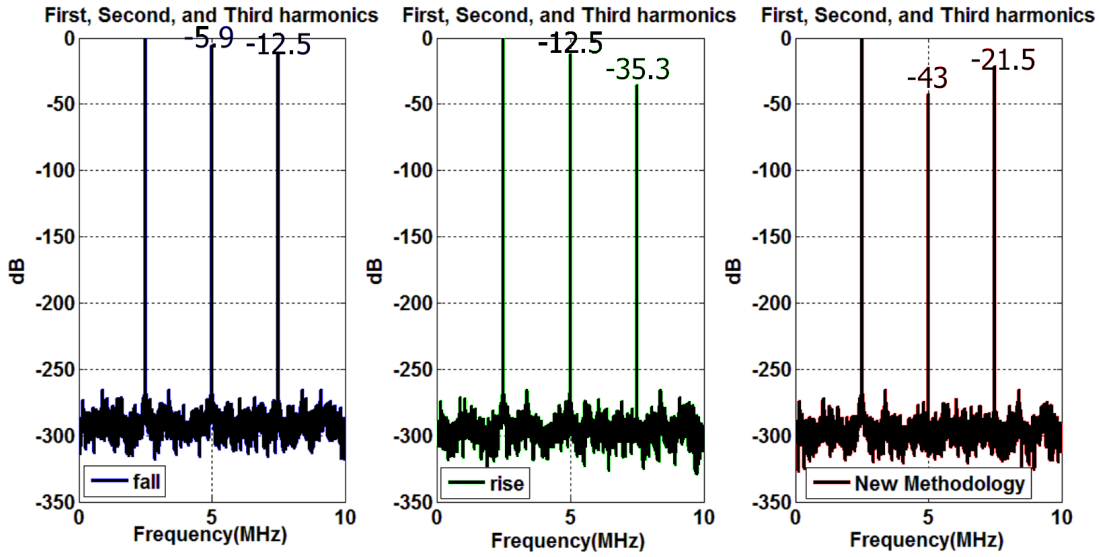

Figure 3.13: Fast Fourier Transform

The THD is calculated based on [20] and [2]. Fast Fourier Transform (FFT) is applied to (3.6), (3.8), and (3.9) as shown in Figure \ref{fig:THD}, and then applying the following equation:

$$THD = 20 * Log(\frac{\sqrt{a_2^2 + a_3^2 + a_4^2}}{a_1}) \tag{3.13}$$

where a_1, a_2, a_2, a_3, and a_4 are the fundamental, second, third, and fourth harmonics.

3.3.4 Methodology Conclusion

In this chapter, a new design methodology is proposed that improves the dynamic range, the linearity, the sensitivity, and the total harmonic distortion of the current-starved based VTC circuits. The proposed methodology depends on increasing the slope of the delay-input voltage curve that relates the pulse width time to the input voltage. This occurs by using a complementary VTC circuit for the original VTC circuit and combining both of them as shown in figure 3.7. The proposed new methodology improves the sensitivity, the dynamic range, and the linearity error by factors of 3.3X, 6.9X, and 3.4X, compared to the original VTC circuit for the same THD. In addition, the new methodology results in improving the THD by 8dB. Moreover, the corresponding power and area overhead of the proposed new methodology is under research to be minimized. However, it is still small compared to the overall TB-ADC power and area. However the figure of merit shows the superiority of the new design methodology.

Applying the proposed methodology on the basic VTC circuit results in a new circuit with the parameters in table \ref{table:new_par} showing the strength of the new methodology.

Parameter	Value
DR	$550mV$
THD	$-20dB$
σ	$2.13mV/ps$
ϵ	3%
$Area$	$4.2872\mu m^2$
$Power$	61.86μ

Table 3.7: The new performance parameters after applying the new methodology

3.4 VTC for 8-bit TB-ADC

In order to achieve 8-bits resolution TB-ADC, the VTC circuit has to achieve an accepted sensitivity with SNDR equals to $50dB$, approximately. The previous VTC circuit achieves $550mv$ dynamic range giving a sensitivity of $2.13\,ps/mv$, but it provides poor SNDR. So, the dynamic range have to be reduced to increase the SNDR to achieve high resolution with accepted sensitivity. However, reducing the dynamic range will affect the TDC design badly. As a solution for this dilemma, first the supply voltage for the VTC circuit was increased to $1.3\ V$ and the dynamic range was reduced to $460mv$ with a new optimization parameters. The new parameters are listed in Tables 3.8 and 3.9. These new parameters give a sensitivity of $2.6\,ps/mv$ and SNDR equals to $42dB$ as shown in figure 3.14 approach the required results.

Parameter	Value
W_{Na1}	200 nm
W_{Na2}	5 µm
W_{Na3}	15 µm
W_{Pa1}	30 µm
L_{Pa1}	500 nm
L_{Na3}	60 nm
L_{Na2}	60 nm
L_{Na1}	60 nm
DC_{bias}	1.2V

Table 3.8: Fall Circuit Parameters

Parameter	Value
W_{Pb1}	30 µm
W_{Pb2}	1 µm
W_{Pb3}	200 nm
W_{Nb1}	15 µm
L_{Pb1}	500 nm
L_{Pb2}	400 nm
L_{Pb3}	250 nm
L_{Nb1}	60 nm
DC_{bias}	0 V

Table 3.9: Rise Circuit Parameters

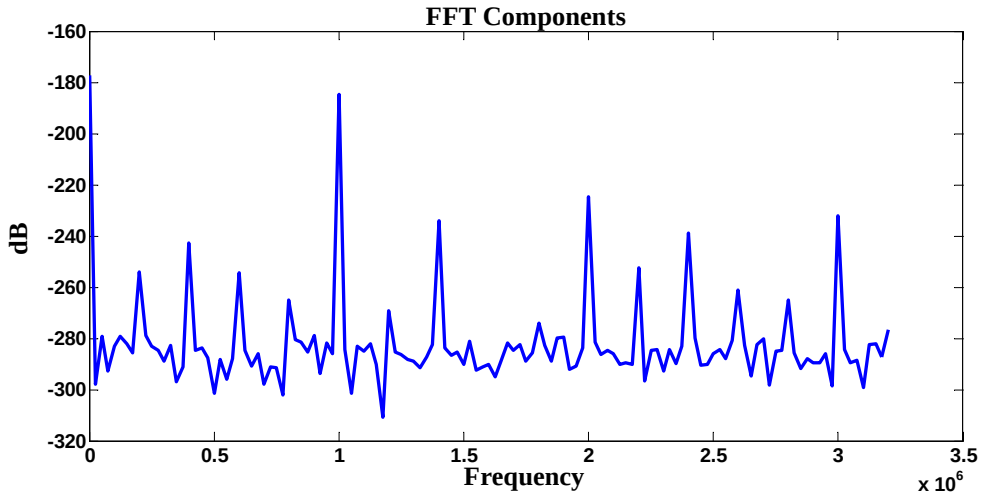

Figure 3.14: FFT for input sine wave sampled at rate50 MHz

Figures 3.15, 3.16, 3.17, 3.18, 3.19 and 3.20 illustrate the linearity of the VTC at 100 KHz, 500 KHz, 2 MHz, 10 MHz, 25 KHz, and 50 MHz, respectively, with a sampling rate equals to 200 MHz without the use of an external Sample and Hold circuit. If higher input frequency is needed, an external Sample and Hold circuit will be used.

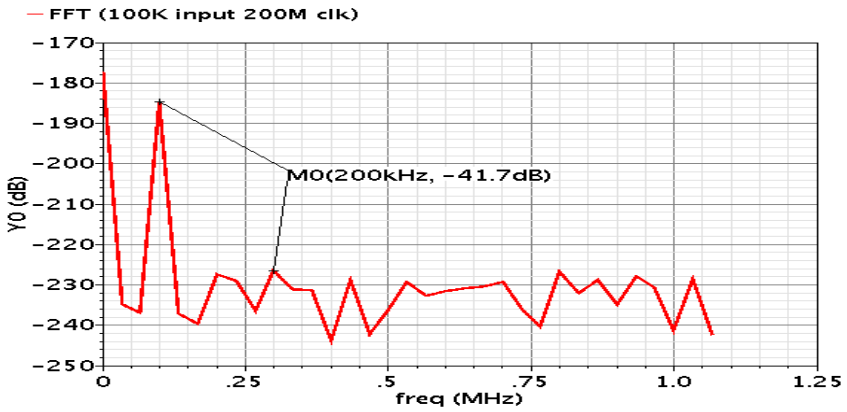

Figure 3.15: Output frequency spectrum for input sine ave with 100 KHz frequency

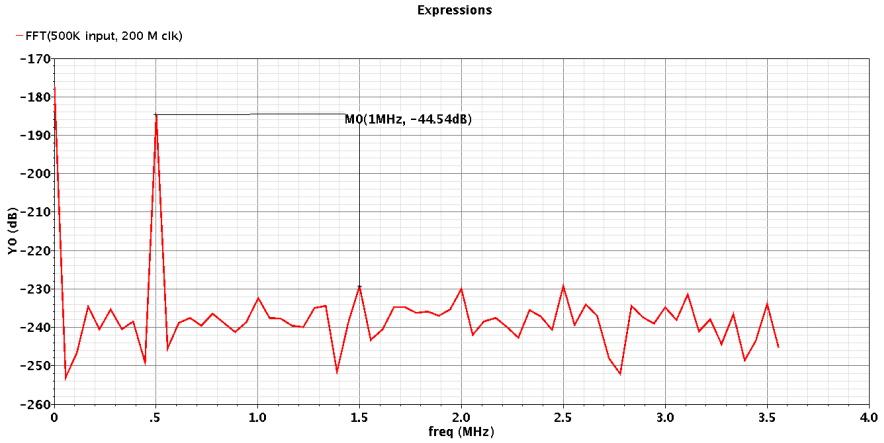

Figure 3.16: Output frequency spectrum for input sine ave with 500 KHz frequency

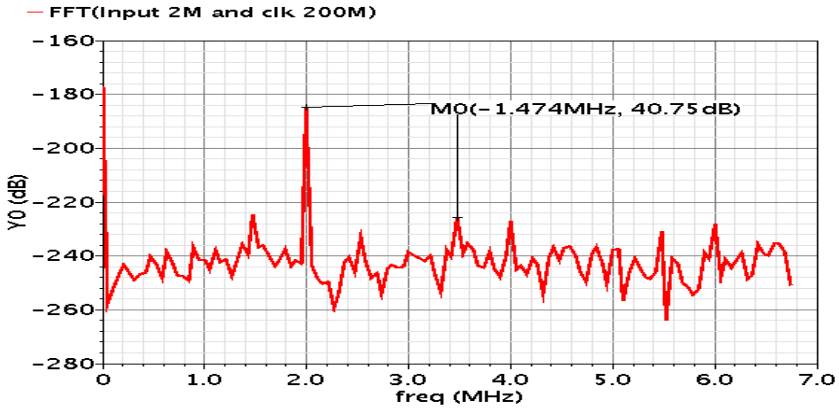

Figure 3.17: Output frequency spectrum for input sine ave with 2 MHz frequency

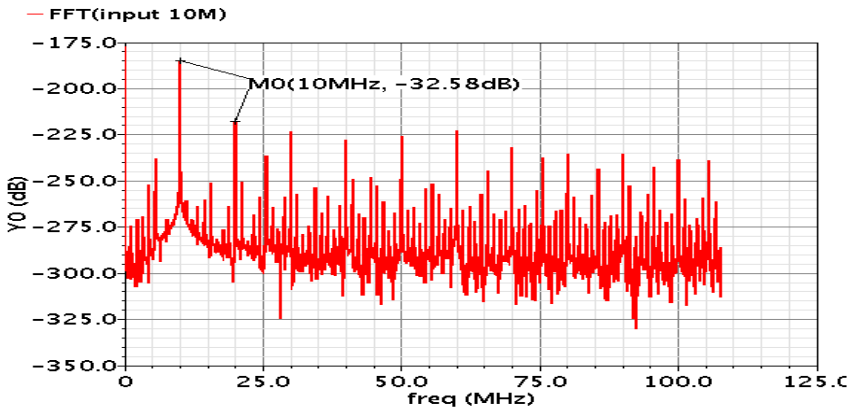

Figure 3.18: Output frequency spectrum for input sine ave with 10 MHz frequency

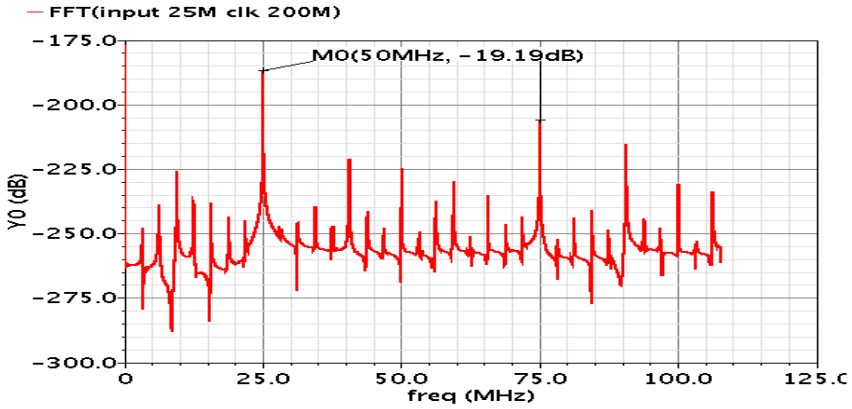

Figure 3.19: Output frequency spectrum for input sine ave with 25 KHz frequency

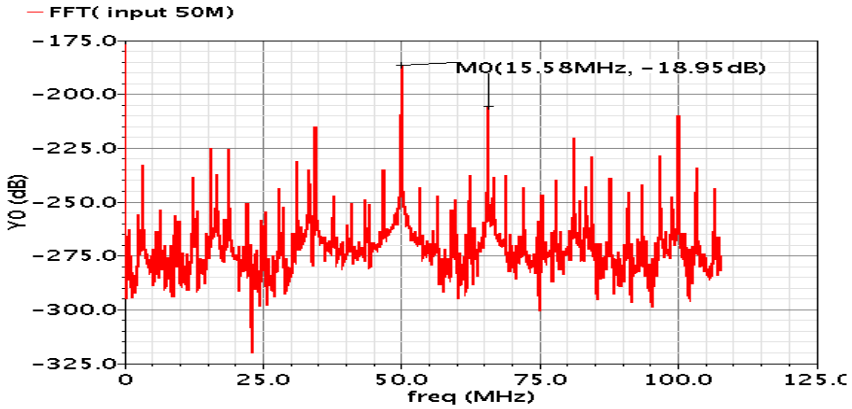

Figure 3.20: Output frequency spectrum for input sine ave with 50 MHz frequency

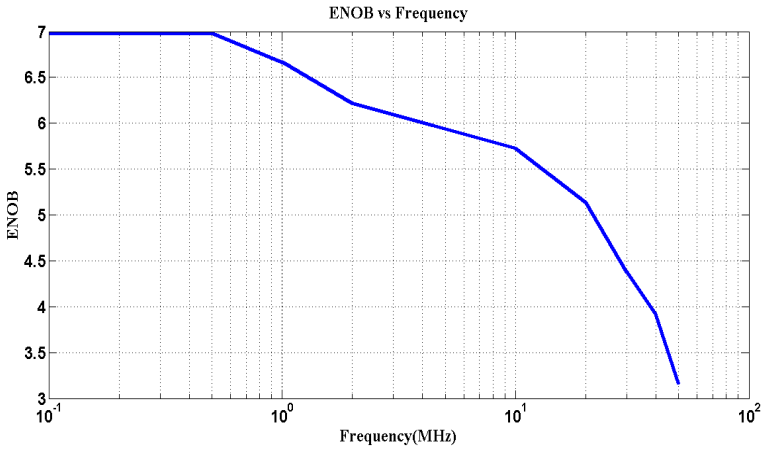

Figure 3.21: ENOB vs input frequency

As illustrated by Figure 3.21, the maximum SQNR is 42.5 dB and the SQNR decreases as the input frequency increases. The maximum SQNR achieved by the proposed circuit is not adequate. Hence, the 8-bit accuracy is not applicable in this situation. Moreover, for an input frequency higher than 5 MHza sample and hold circuit is needed to maintain the ENOB.

3.4.1 Differential VTC

Analog systems usually use differential input differential output to increase the SQNR. Thus, we tried to make a differential VTC to increase the SQNR , hence, increase the ENOB. The input to the TB-ADC will be differential. The positive terminal of the input is $V^+$and the negative terminal is V^-. This idea duplicates the size and the power of the VTC, but gives a better SQNR as shown in Figure 3.22. However, we face a problem at the Differential VTC output. The output is represented as two start and two stop signal, these signals need to be subtracted as following:

$$(Start1 - Stop1) - (Start2 - Stop2) \tag{3.14}$$

This simple equation normally can be achieved using XOR gate. However, this solution is not suitable in our case because the $(Start1 - Stop1)$ signal and $(Start2 - Stop2)$ are not synchronized. We used the single ended VTC in our design until solving this problem.

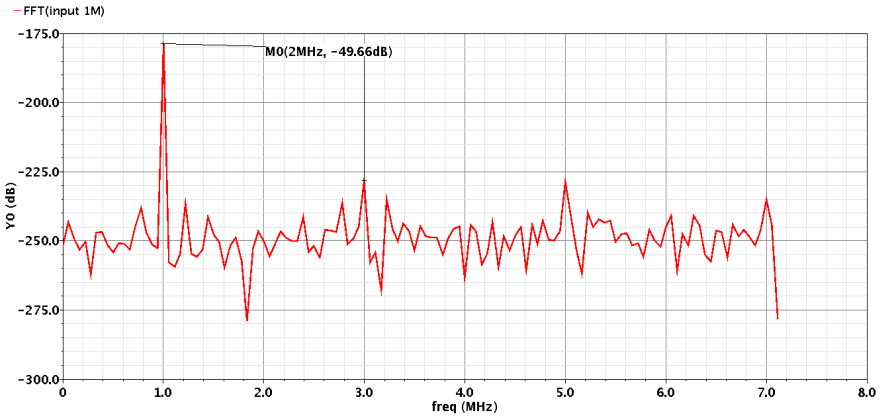

Figure 3.22: FFT components for the Differential VTC

Chapter 4

Time to Digital Converter

4.1 Introduction

Time to digital converter is a basic building block in a lot of applications that need time measurement systems. For instance, time of flight particle detector, logic analyzer, medical imaging, time-based ADC, spectrometry systems, All Digital PLL (ADPLL), and laser ranging. In modern applications and systems the TDC required small resolution starting from $1ps$ up to $1ns$ in 65nm CMOS technology [22, 23].

4.2 TDC types

There are a lot of TDCs to satisfy the different systems requirements. System requirements can be divided into main metrics such as: time rang, resolution, power, area, linearity, and speed where, TDC time range is the difference between the largest time input and the smallest time input and TDC resolution is the smallest time difference that can be detected.

Selecting the correct TDC is a function of the aforementioned parameters. Various types of TDC exist such as: Vernier delay line, two level Vernier delay line, stochastic delay line, Vernier ring delay line,cyclic based, counter based, and flash TDC. The TDC can be designed as a full custom digital design or using standard cells [23].

4.2.1 Counter based TDC

Digital counter based TDC is one of the basic TDCs. Counter based TDC is a simple counter that count the number of complete cycle of a refrence clock between the start and stop signal. Then, this couniting is captured in output buffer. However, it consumes small area, to achieve high resolution a high frequency counter is used to avoid errors such as in figure 4.1. Moreover, this kind of TDCs might consume large power because of the high frequency counter [2].

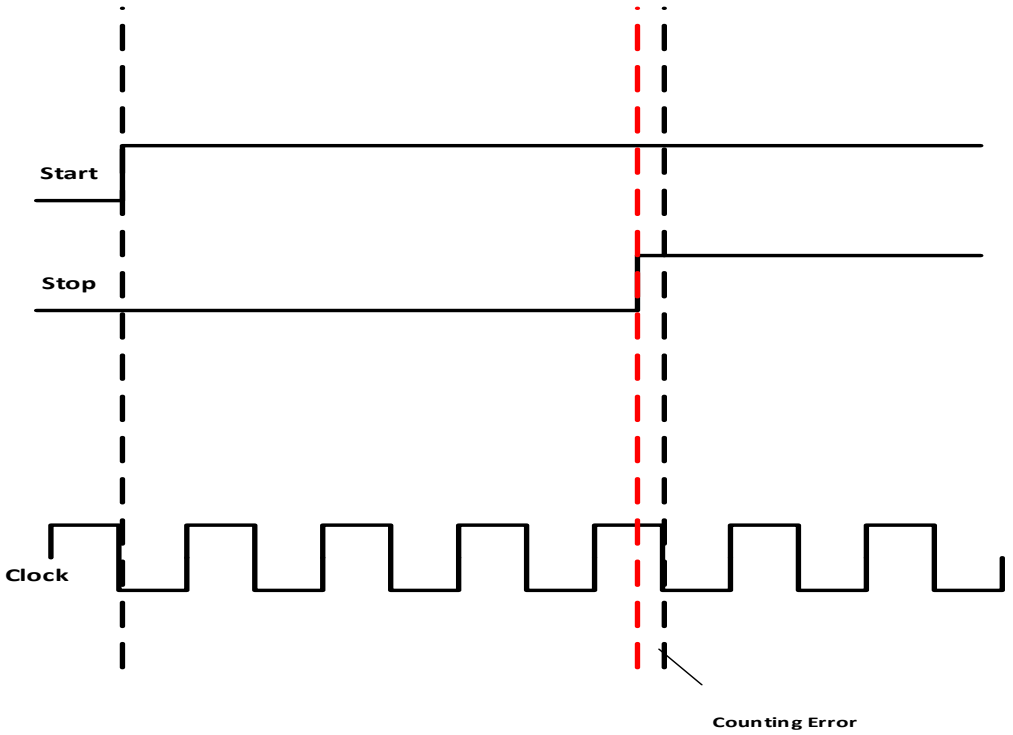

Figure 4.1: Theory of Operation for Counter based TDC

4.2.2 Flash TDC

Flash TDC is one of the fastest and the finest resolution TDCs. As illustrated in figure [Flash_TDC] the flash TDC consists of D-flipflobs, basic delay elements - mainly a buffer - each has a delay grater than its previous one by Δ , and a group of capacitors each has grater capacitance than its previous one to increase the delay of the basic delay element. The flash TDC has a very fine resolution that approaches a fraction of pico seconds in 65nm technology and using standard cell technology as in [#Abbas]. The flash TDC consumes large area and power, but the main drawback is the tolerance in the fabrication. The main delay factor is the capacitor and the flash TDC depend on a series of capacitors with values C, $2C$, $3C$,... . If each one of this capacitor has a variance equal to $10 \sim 20$, which is accepted at IC manufacturing, the resolution linearity will be distorted. So, in modern designs for flash TDC, instead of using single capacitor as a delay source; designers are using a bank of digitally controllable capacitor to make a calibration for the TDC, such as in [24] and as shown in figure 4.3, to calibrate the process variation.

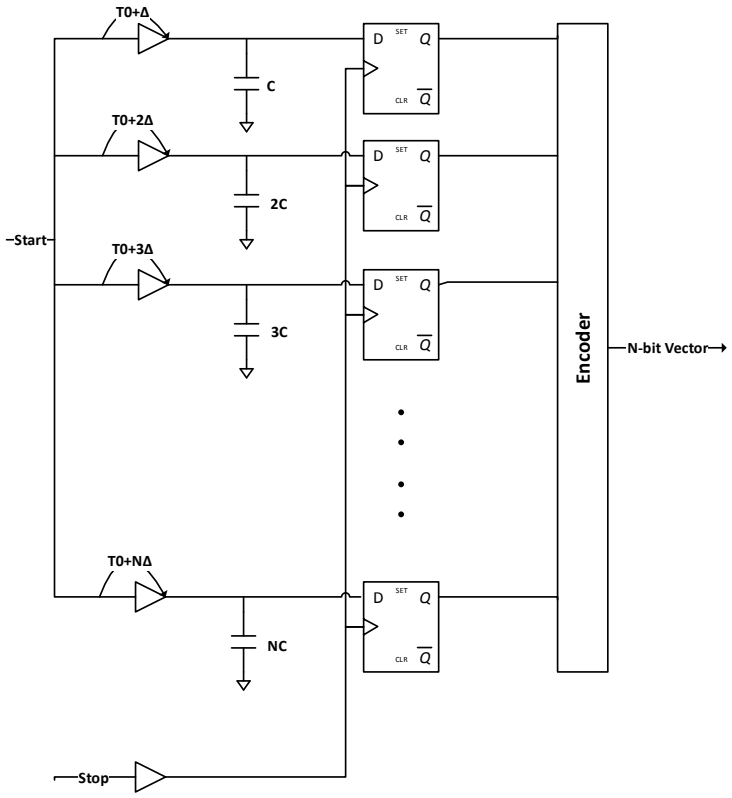

Figure 4.2: Flash TDC

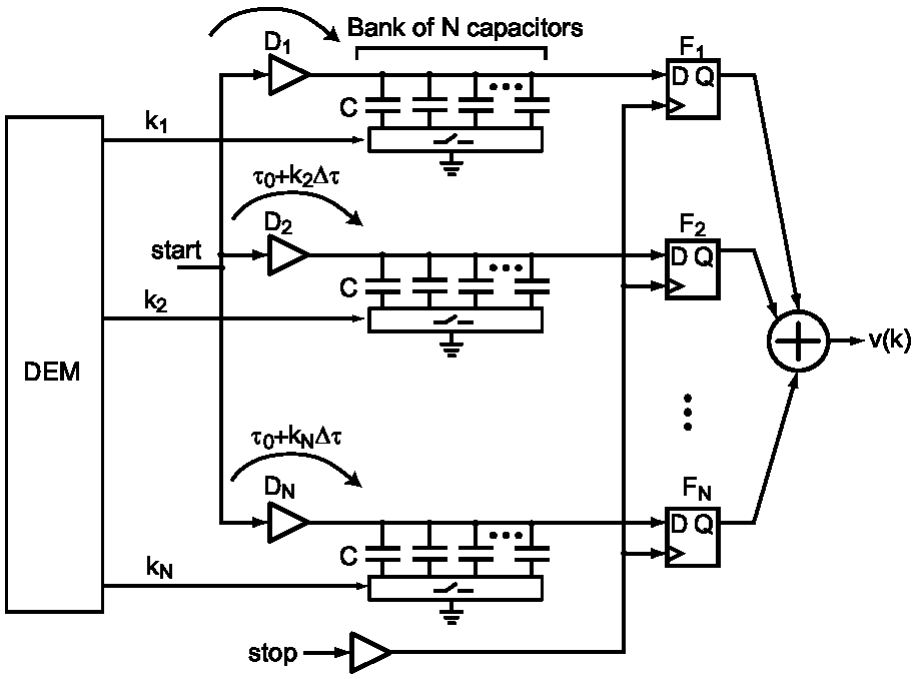

Figure 4.3: Advanced Flash TDC [24]

4.2.3 Delay line based TDC

Delay line based TDC is an appealing approach in high resolution TDCs circuit design and implementation [2]. Figure 4.4 illustrates the delay line TDC theory of operation. Delay line based TDC can measure a time interval between two events where the first event lunches Start signal and the second event lunches Stop signal. The Start signal propagates through series of buffer, each buffer delay the start signal by τ_d and the Stop signal samples the delayed version from the Start signal after each buffer. D-flipflobs output is a thermometer code where each D-flipflob out is logic one until catch up occurs. The thermometer code is then converted to binary code through a thermometer to binary encoder [2].

However, this TDC is a good candidate for high resolution, it couldn't be used for measuring long intervals with high resolution because of the required length of the delay line will be very long. Also, this TDC can used digital standard cells, this TDC cannot achieve resolution less than the buffer resolution. So, the Vernier delay line based TDC and the hybrid TDC appeared.

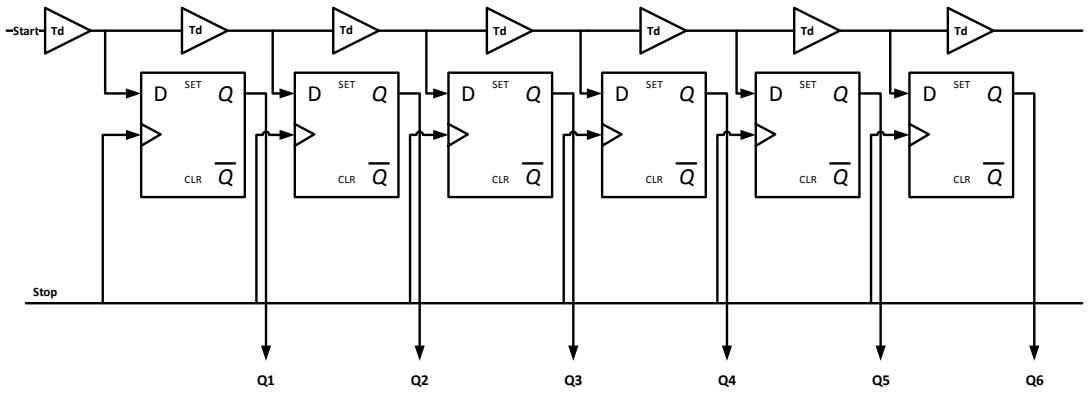

Figure 4.4: Delay Line Based TDC

4.2.4 Hybrid delay line based TDC

The aforementioned TDCs can measure small intervals with high resolution or large intervals with small resolutions. Hybrid delay line TDC consists of counter and delay line combined together in order to cover large time intervals with high resolution. The theory of operation is to make the counter calculate the time and afterwards the delay line calculate the error time only not the whole time. The error time is a fraction of the counter clock cycle. The delay line calculate the error time then this error time is subtracted from the main time to get a higher resolution. Figure 4.5 illustrates the theory of operation where the counter calculates the time interval with error. Then, refinement is done by the delay line to increase the accuracy, resolution, of the TDC. There are several types of hybrid and cyclic TDCs[25].

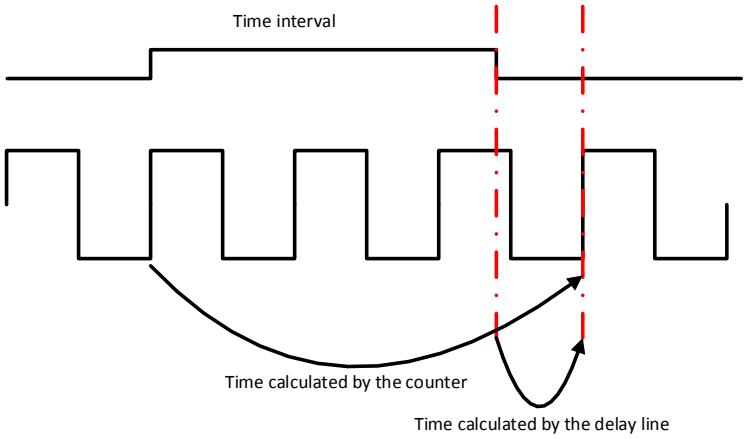

Figure 4.5: Residual time error

4.3 Implementation of Two level Vernier Delay line based TDC

Figure 4.6 illustrate the system block diagram for the TDC. It cosists of Two Vernier delay line, two interface circuit, two THermal to One Hot (TH2OH) encoders, two One Hot to Binary (OH2B) encoders. First the VTC works to produce a pulse width. Then, the pulse width is converted to start and stop signals. Afterwards, the start and stop signals are issued to the Vernier delay line.

Vernier delay line is an improved delay line to support higher resolution. The traditional delay line, in figure 4.4 can not achieve resolution higher than the buffer delay, it depend on the delay of a specific buffer. For instance if the buffer delay is $10\,ps$ then the maximum resolution is identical to this number, in contrast with Vernier Delay Line (VDL). Figure 4.7 shows the basic VDL that depends on the time difference between two delay elements. The start signal is delayed by T_{d1} and the stop signal is delayed by T_{d2}, but D-flipflobs sense the time difference only as shown in figure 4.7. However, this technique increase the area, it increase the resolution of the TDC as well.

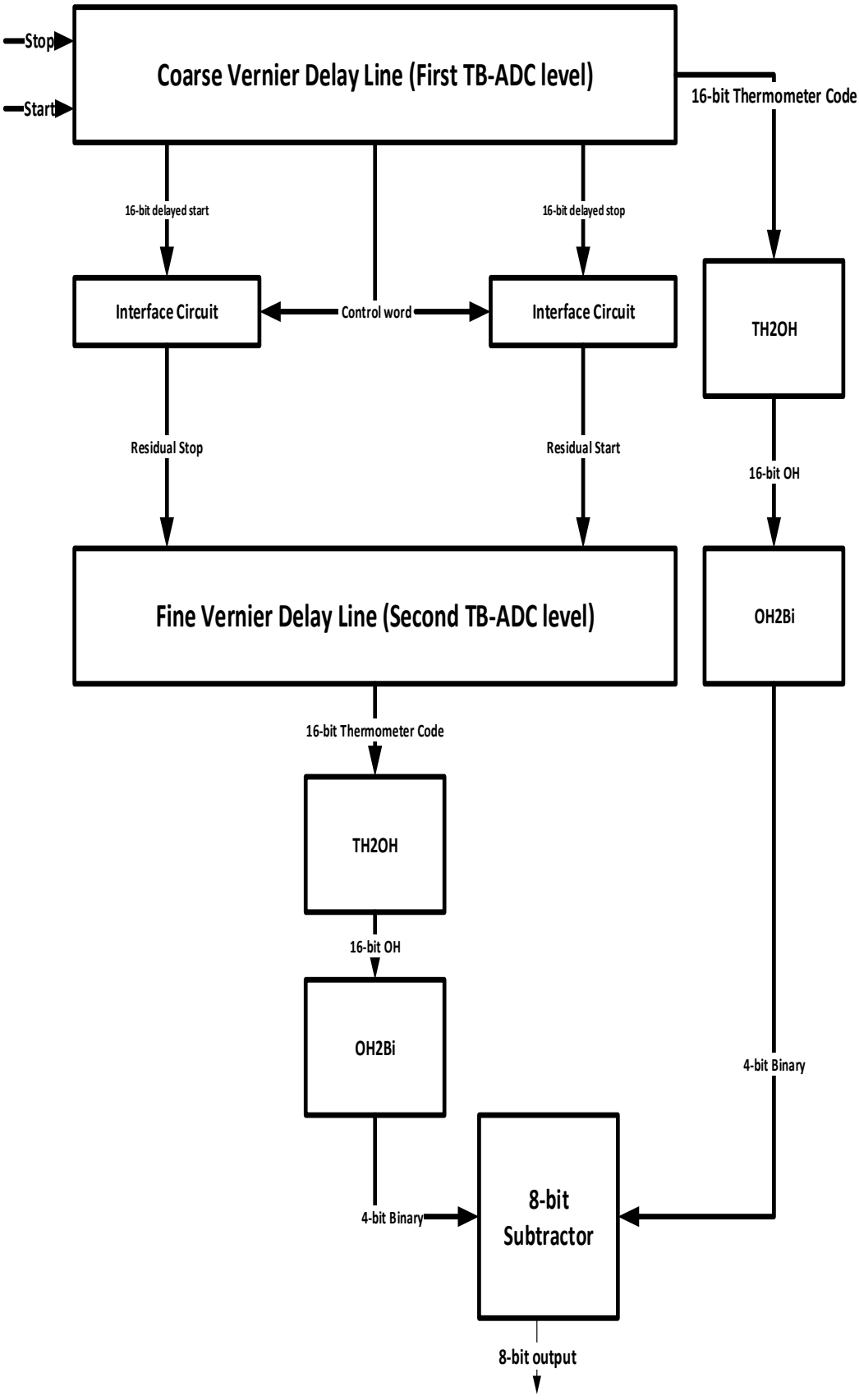

Figure 4.6: TDC Block Diagram

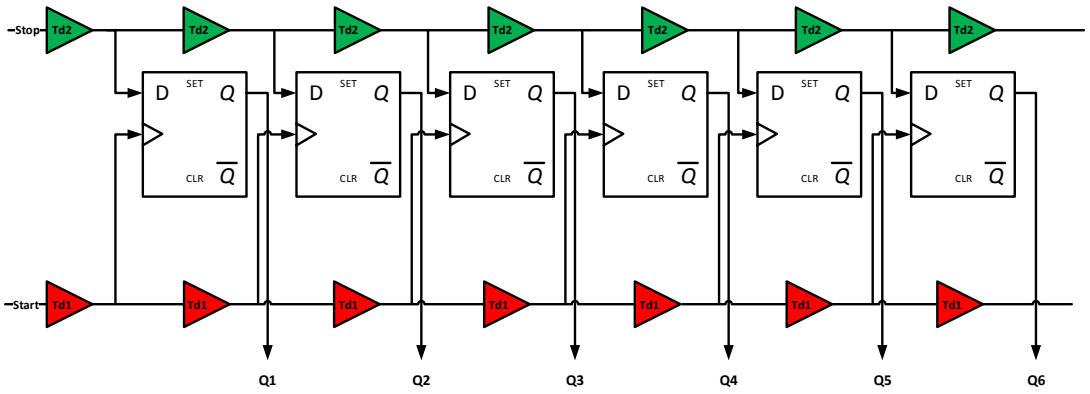

Figure 4.7: Vernier Delay Line

Generally speaking, the high resolution problem has been solved by the VDL technique. On the other hand, the problem of converting wide range of times still exist. There are different solutions like two level VDL or cyclic based VDL. In our proposed TDC we selected the two level VDL technique instead of the VDL as shown in figure 4.6. For $n-bit$ TDC, VDL needs 2^nVernier delay cell which consume large area and power. However, in two level Vernier Delay Line, $2^{\frac{n}{2}}$ Vernier delay cells, are required for each level. The dashed part of figure 4.8 illustrates one Vernier delay cell.

In our case we need dynamic time range equal to $1.2\,ns$ and our TDC target is 8 bit, so we need $2^{\frac{8}{2}}$Vernier delay cell in the coarse Vernier delay line and another $2^{\frac{8}{2}}$Vernier delay cell in the fine Vernier delay line. The resolution of our coarse delay line is $\frac{1195\,ps}{2^4} = 74.6875\,ps$ and the resolution of the fine Vernier delay line is $\frac{74.6875}{2^4} = 4.668\,ps$.

4.3.1 Operation Theory

The time interval to be measured starts with "Start" signal and end by "Stop" signal. As shown in figure 4.8 the start and stop signals are feed to the Coarse Vernier Delay Line (CVDL) to calculate the Coarse Resolution (CR). The binary output vector, C, indicate the filpflops output, which is thermometer code. After each Vernier delay cell the start signal; approaches the stop signal until a catch up occurred. The thermometer code indicates where the catch up occurs.

Once the catch up occurred, the thermometer code , vector C, will control interface circuit such as in figure 4.15 to fed the residual start and stop to the Fine Vernier Delay Line (FVDL). The FVDL will decrease the difference between the residual start and the residual stop signals until a catch up occurs. The output thermometer code will be used to fine tune the CVDL result through subtracting this part from the previous one.

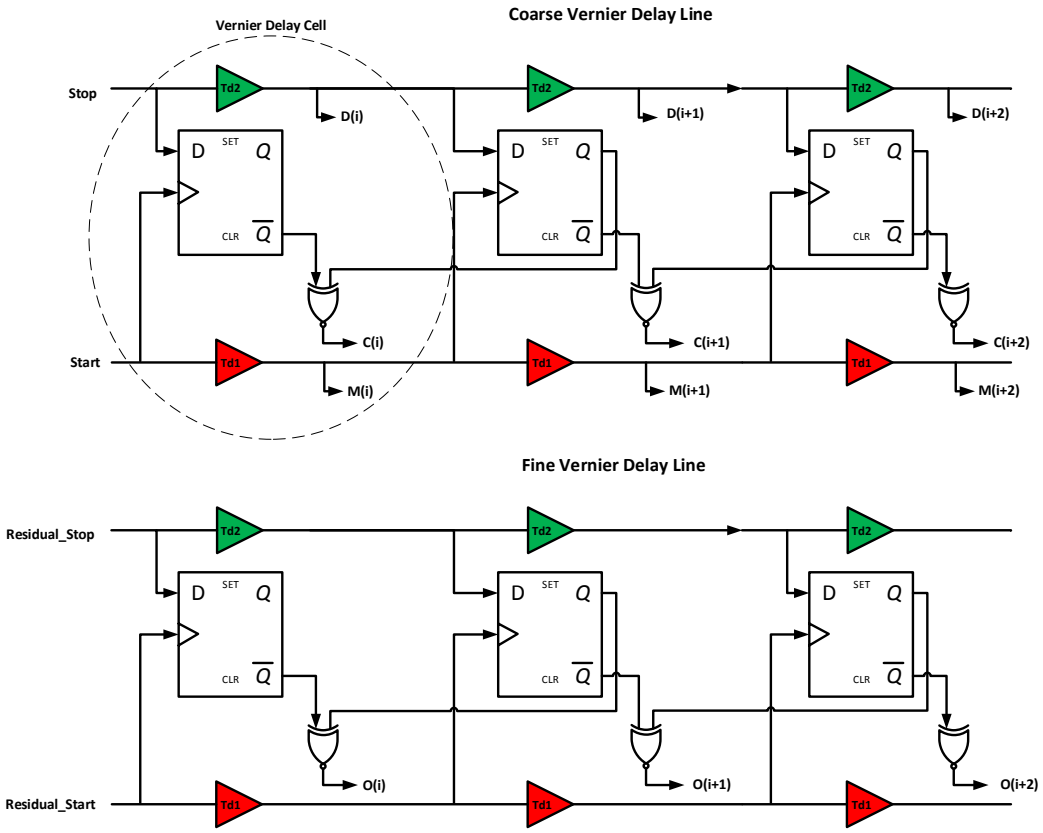

Figure 4.8: Two Level Vernier Delay Line

4.3.2 Coarse Delay Line

Figure 4.8 illustrates the Coarse Delay line. The VTC generate a pulse width modulated signal then this signal is feed to PWM to start/stop converter as if figure 4.9. The start and stop signals are feed to the CVDL then the thermometer code are generated. Figure 4.9 illustrate the connections between the VTC and the PWM to start/stop converter.

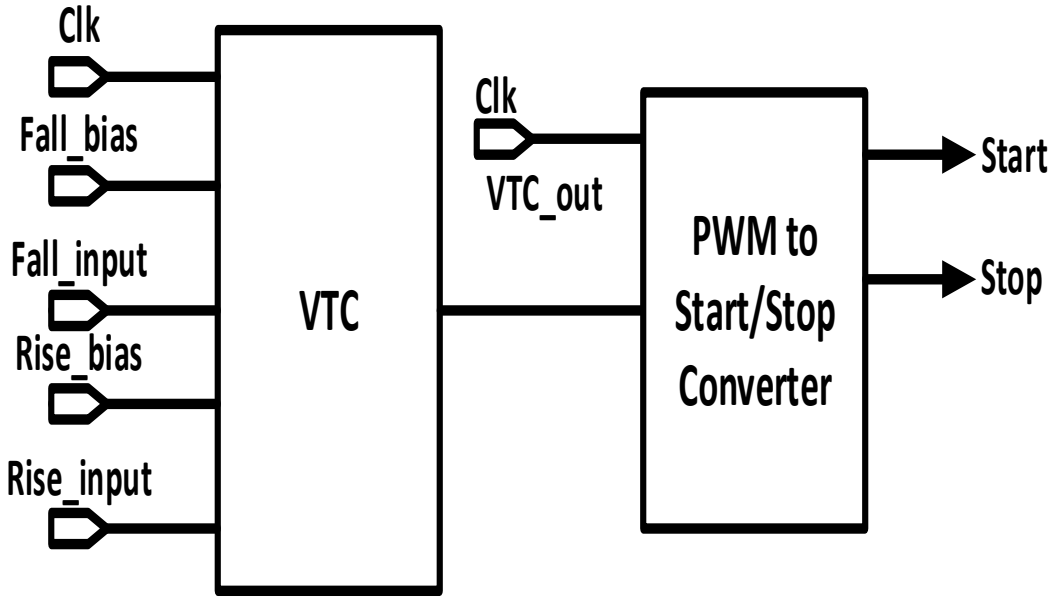

Figure 4.9: VTC and start/stop converter connections

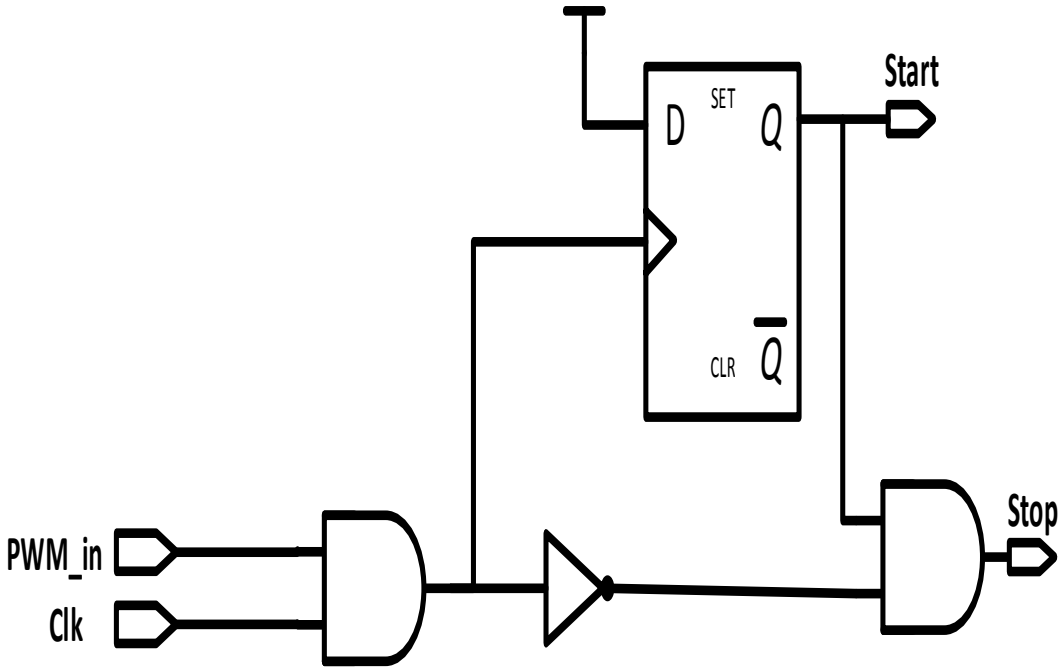

Figure 4.10: Pulse Wdith to Start/Stop Converter

The output of the VCDL, the thermometer code, is converted to logic one at the catch up position and the rest of outputs becaome logic zeros, which is called one hot code. This operation is carried out through the XNOR gates at figure 4.8. However, the output is not ideal the output looks like figure 4.11.

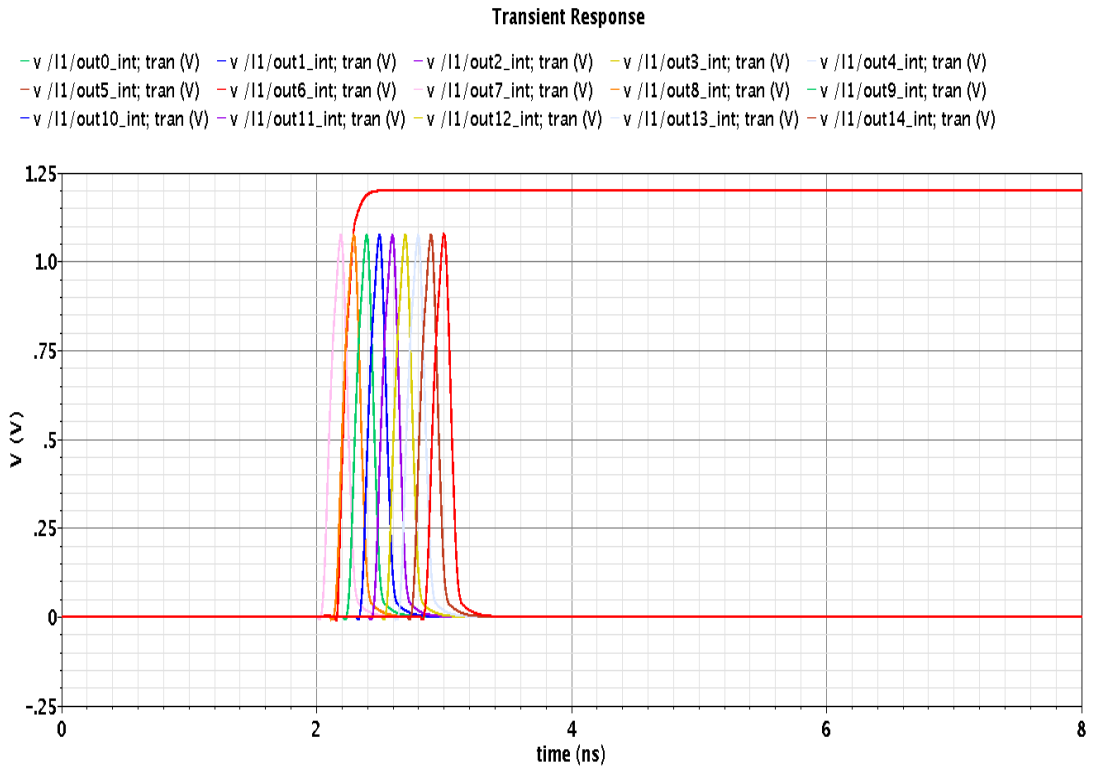

Figure 4.11: Thermometer to one hot code output example at vin=0 V.

After the catch up at the output of the flipflop namely$n$, the $\bar{Q}_n$signal will be zero and the Q_{n+1}signal will be one. However, Q_{n+1} takes T_{clk2Q} delay time until it becomes a one. During this delay the Q_{n+1} is zero which leads to output logic one at the XNOR gate until the correct value of Q_{n+1}appears. Then the correct output appears as shown in figure4.11. This phenomena makes a problem for the interface circuit where some switches are randomly opened and closed based on the catch up location. This phenomena leads to different seen input capacitance leading to time distortion between the residual start and the residual stop signal. So, each output from the one hot converter was masked by a delayed version from itself to get a more suitable output such as in figure 4.12. However, this solution add more area and power dissipation to the over all system, this part is very critical to prevent the time distortion imposed by the variable input capacitor seen by residual start and residual stop.

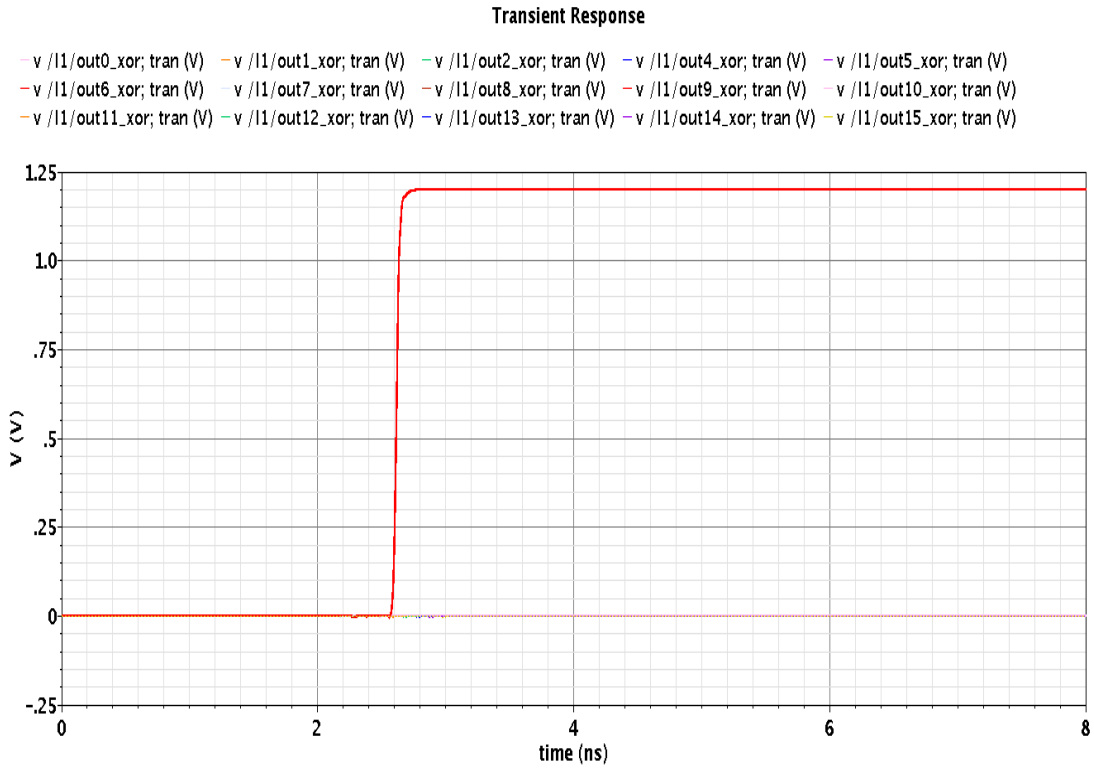

Figure 4.12: Corrected Thermometer to one hot code output example at vin=0 V.

4.3.2.1 Coarse and fine cells at CVDL

As mentioned before the coarse delay line resolution is 74.6 ps, this resolution is achieved by using a course delay element as in figure 4.13 with a resolution of 101 ps and a fine delay element as in figure 4.14 with a resolution equals to 26.4. Table 4.1 indicated the transistor sizing.

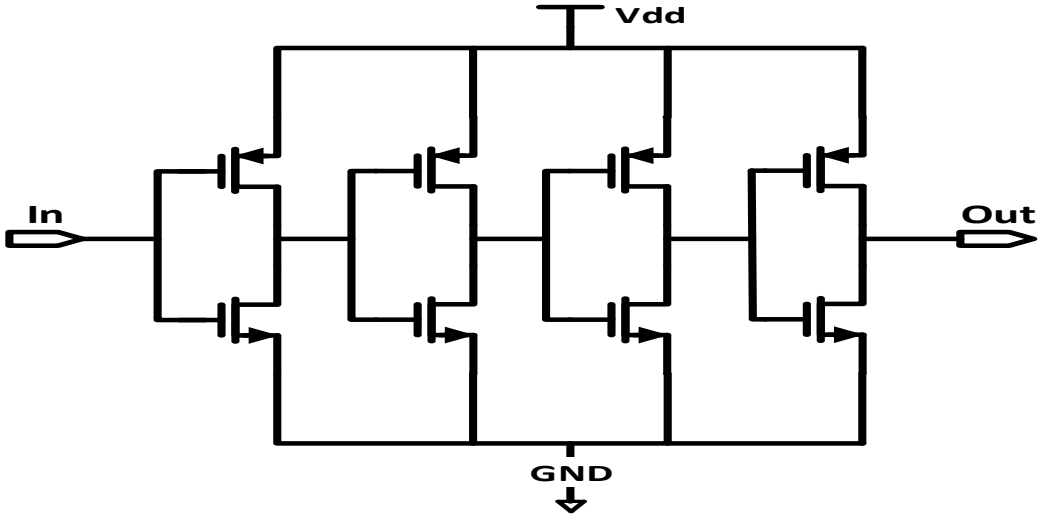

Figure 4.13: Coarse Cell

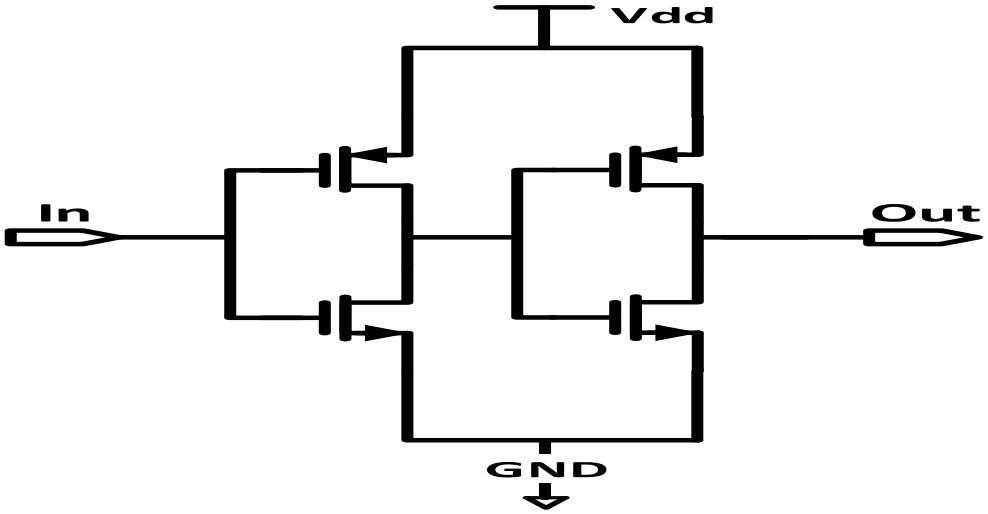

Figure 4.14: Fine Cell

Symbol	Value
W_CR	$1\,\mu m$
L_CR	$173.5\,nm$
W_FR	$240\,nm$
L_FR	$60\,nm$

Table 4.1: Coarse and Fine cell sizing in CVDL

4.3.3 Interface Circuit

The interface circuit is a multiplexer based circuit as shown in figure 4.15. The main purpose of the Interface circuit is to properly transfer the signals without affecting the time differences between the signals. The first interface circuit is used with the start signal and the second one is used with the stop signal. Also, the interface circuit is controlled by the one hot code from the thermal to one hot converter associated with Coarse Vernier delay line.

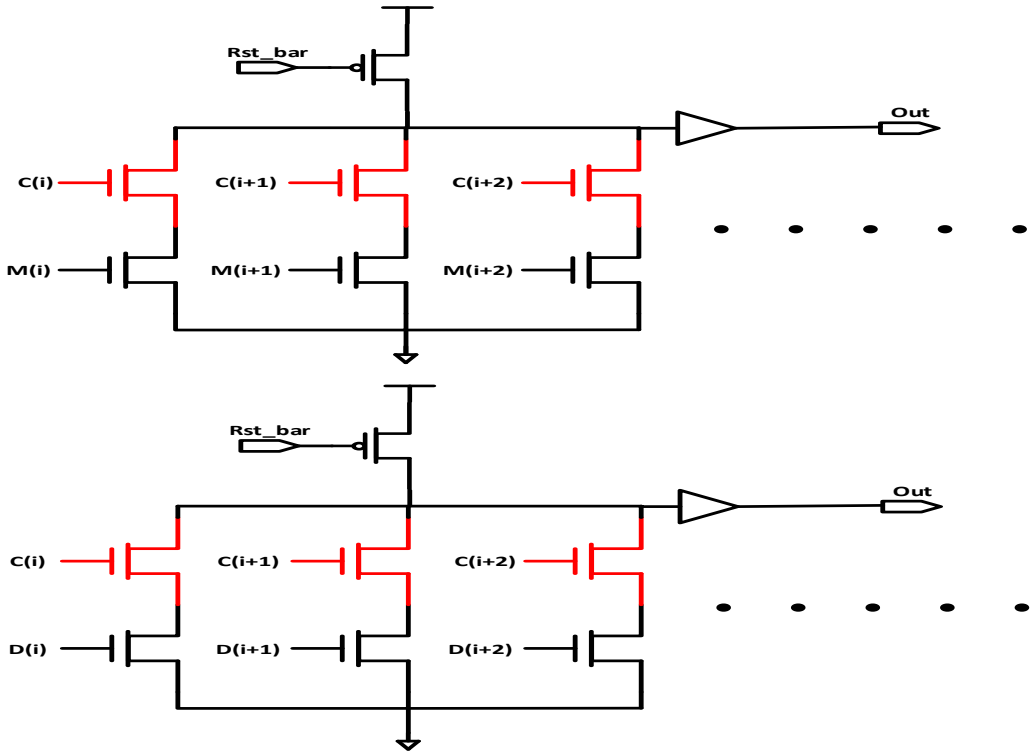

Figure 4.15: Interface Circuit

4.3.4 Fine Delay Line

Figure 4.8 illustrates the Fine Delay line. The fine delay line is similar to the coarse delay line, but it has a higher resolution. The required resolution here is 4.6 ps. After the catch up at the CVDL the signals transfer to the fine vernier delay line to calculate the residual error in the time interval calculated by the CVDL.

4.3.4.1 Coarse and fine cells at FVDL

The coarse and fine cells at FVDL have to achieve 4.6 ps. This high resolution can be achieved by using coarse cells with delay equals to 15.23 ps as shown in figure 4.16 and fine cells with delay equals to10.64 as shown in figure 4.17. Table 4.2 illustrate the transistor sizing for the coarse and fine cells. Figure 4.18 illustrates an example for the start and stop signal before and after crossing from caorse and fine cell at FVDL.

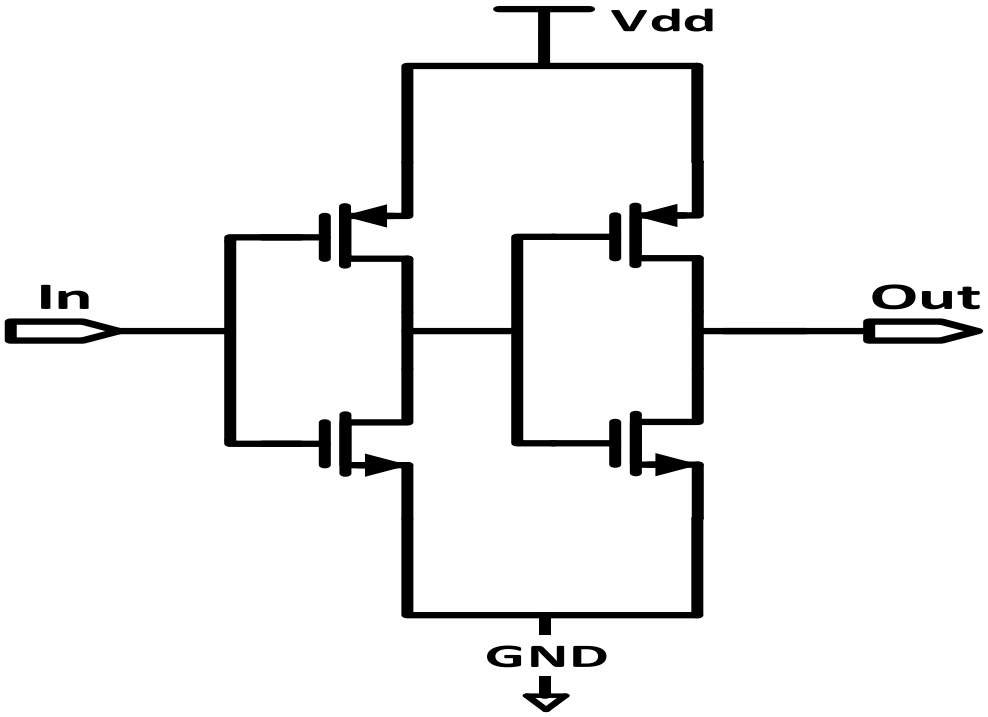

Figure 4.16: Coarse Delay Cell at FVDL

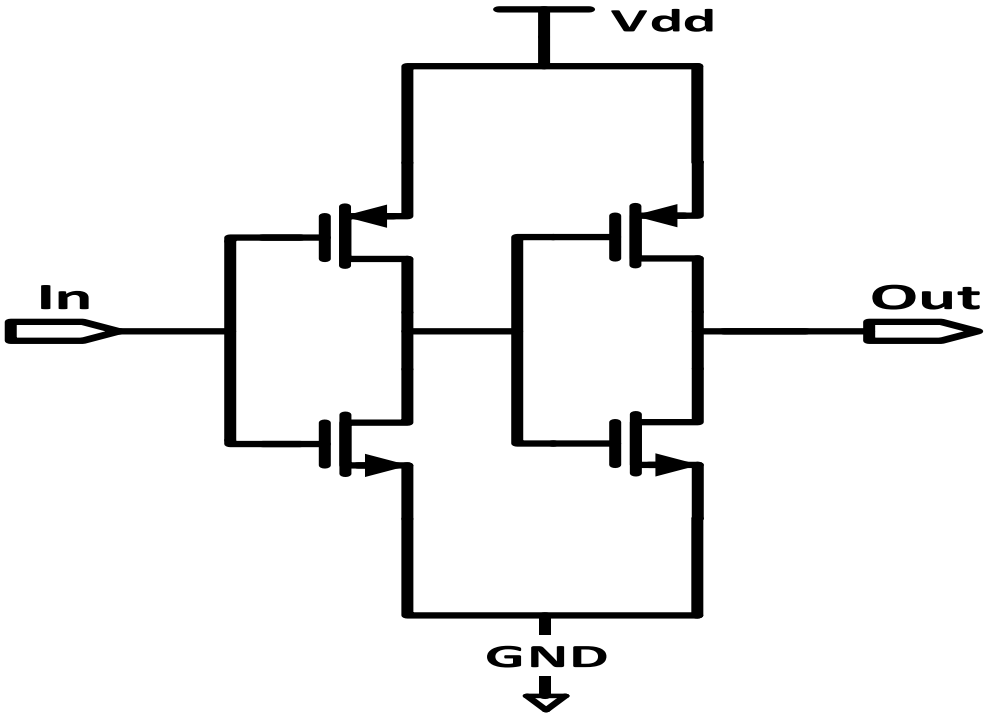

Figure 4.17: Fine Delay Cell at FVDL

Symbol	Value
W_FV_C	$2\mu m$
L_FV_C	$80nm$
W_FL_FC	$2\mu m$
L_FL_FC	$60nm$

Table 4.2: Coarse and Fine cell sizing in FVDL

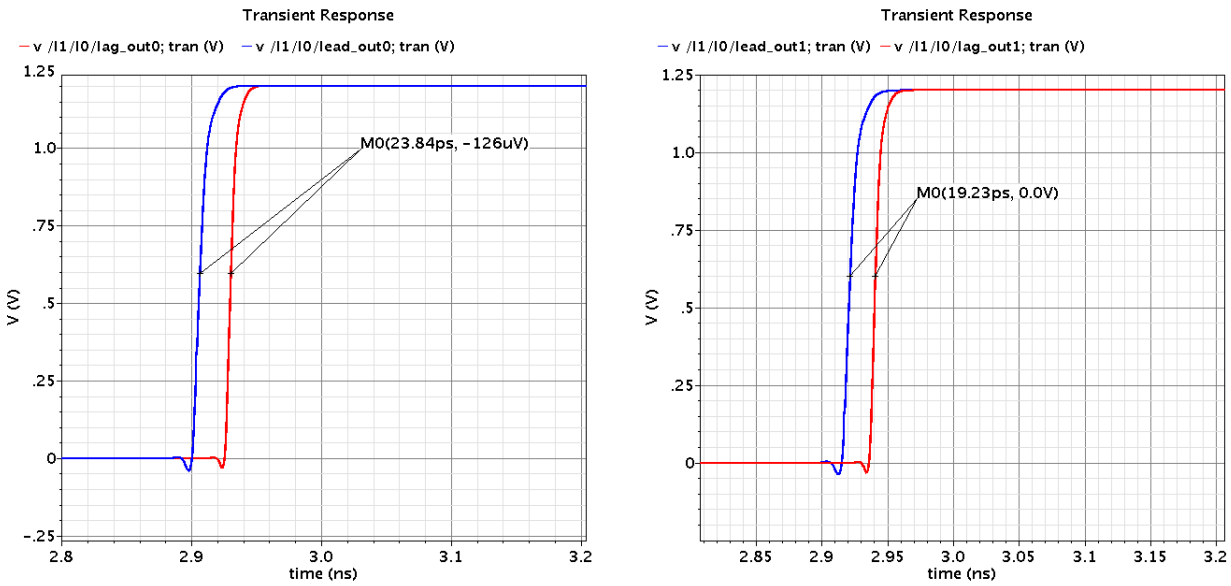

Figure 4.18: Example from a start and stop signal before and after the delay cell

4.3.5 D-FlipFlop

The flip-flop is a very important component at the VDL. It is responsible for sampling the stop signal based on the start signal. For any flip-flop it is critical to maintain a setup time between the data and the clock or the flip-flop will be in a quasi stable state. Figure 4.19 shows a modified C2MOS master slave filp-flop, the main aspect of this modified flip-flip is it's set up time. This flip-flop has an almost zero setup time as shown in figure 4.20 [5].

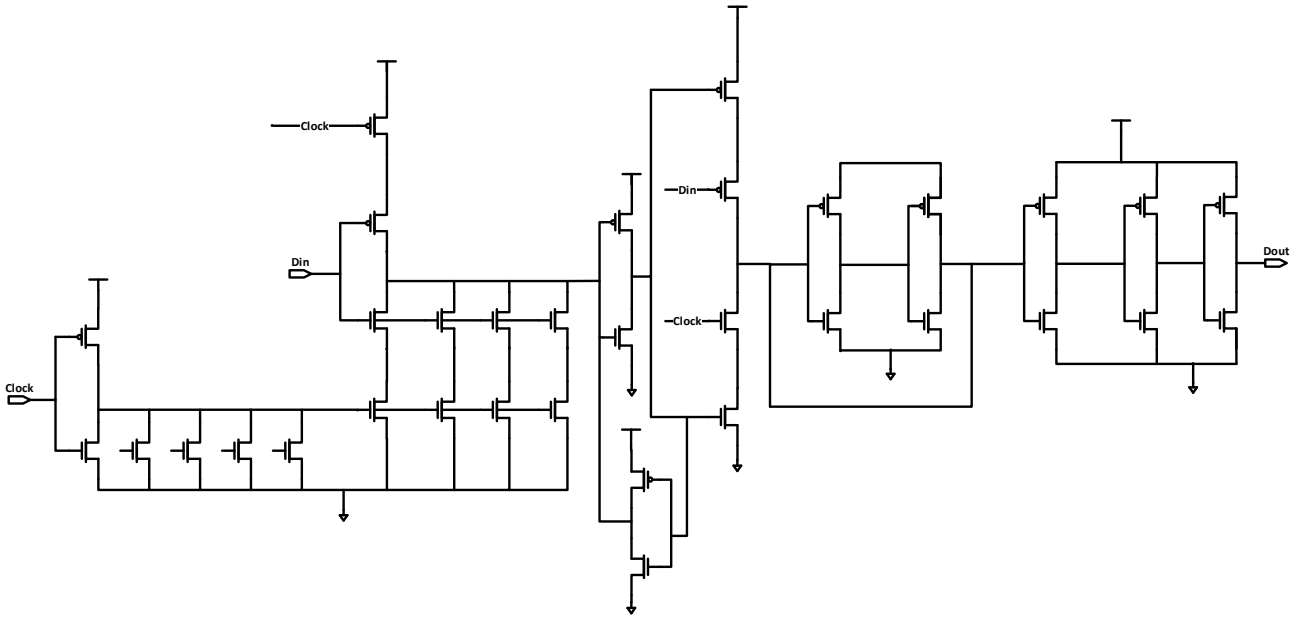

Figure 4.19: C2MOS flip-flop

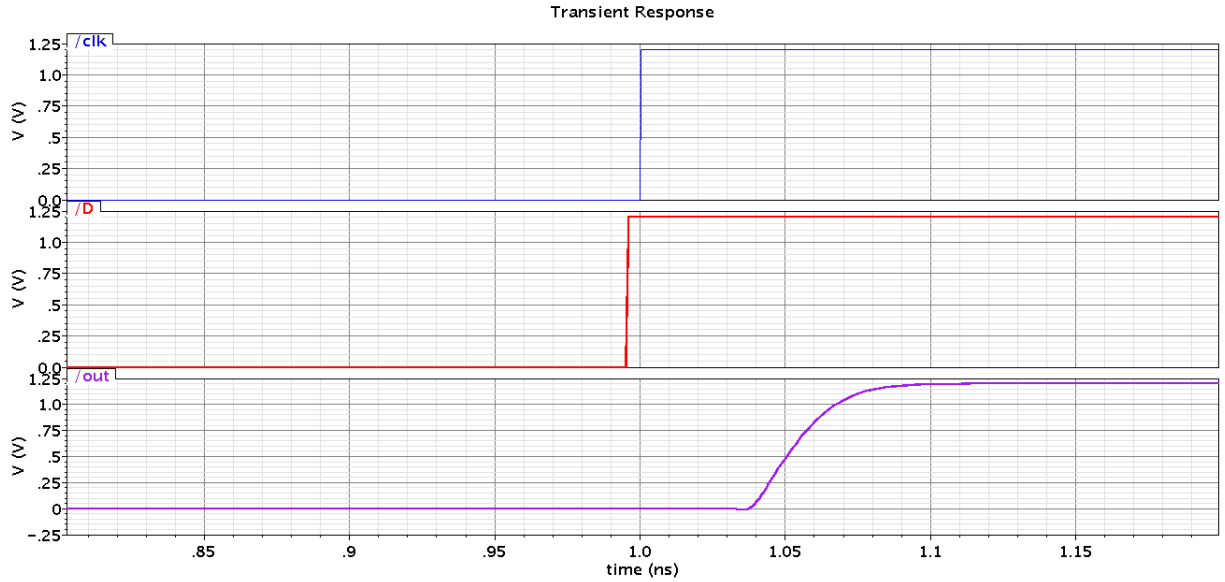

Figure 4.20: Setup time for the D-FF

However, this flip flop is a very good candidate, this flip-flop consumes large area about$2.232 \mu m^2$. Also, it consume large amoint of power. We can tolerate with the power and area requirements. But, the large area leads to lage input capacitance on the D input and the Clock input. The input capacitance seen from the D input is not equal to the amount of input capacitance seen at the clock input. The difference in the input capacitance lead to timing error between the start and stop signals. So, gradual bufferes were used at the D input and the Clock input to re-distribute the input capacitance to elliminated the delay error from the flip-flop.

4.3.6 Thermometer To Binary Conversion

As shown in figure 4.6 both the Vernier coarse and fine delay lines have a thermometer output code. As shown in figure 4.8, the $\bar{Q}_n$and the $Q_{n+1}$are used as an input to XNOR gates and the output is a One Hot (OH) code. Using a simple Fat-Tree OR gates such as shown in figure **??** the OH code is converted to binary equivalent code.

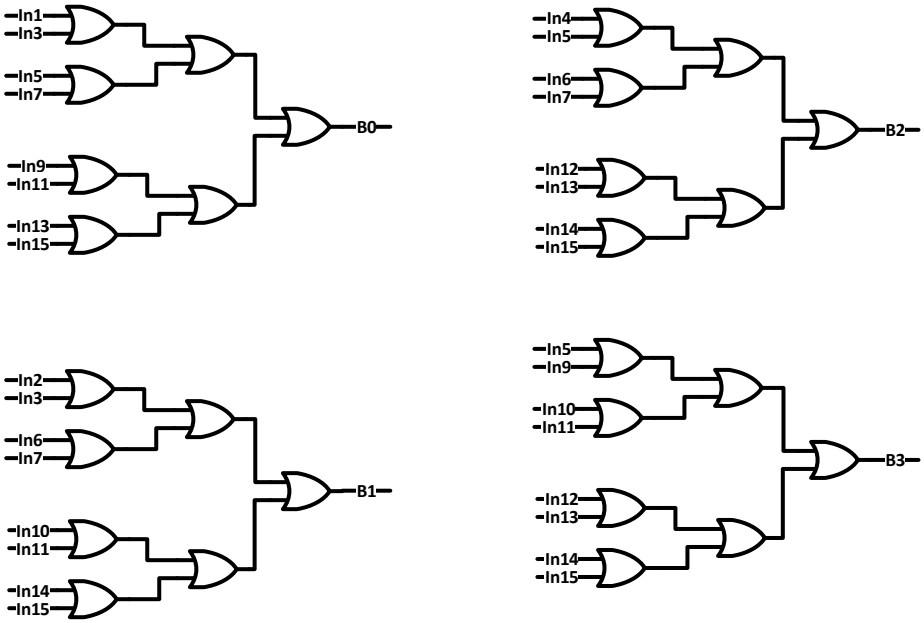

Figure 4.21: Fat-Tree OH2B converter

4.3.7 Final 8-bit subtractor

Both the CVDL and the FVDL generate 5-bits to indicate the catch up event. This binary numbers have to be subtracted using normal carry propagate adder as follow $OutCode = 16 * CVDL_{out} - FVDL_{out}$.

Chapter 5

Discussion and Conclusions

In this chapter we integrate the TB-ADC and introduce different performance metrics and parameters. Our TB-ADC consists of the VTC circuit described in chapter 3 and the TDC circuit described in chapter 4. Figure 5.1 illustrates the system block diagram. The VTC circuit inputs are a clock, rise bias, fall bias, rise input, and fall input. The input dynamic range is $460\,mV$ super imposed on a $530\,mV$ biasing.

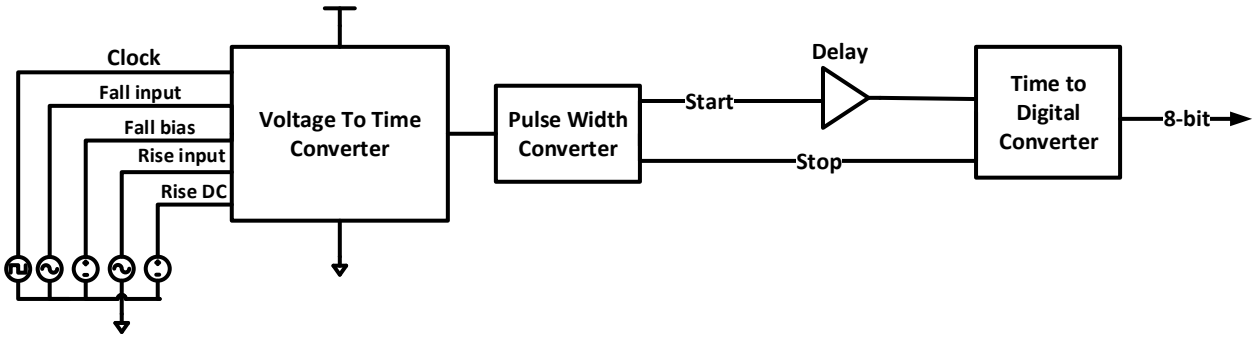

Figure 5.1: Total System block diagram

The input dynamic volt is corresponding to VTC out dynamic range of $1194\,ps$ where the smallest difference between the start and the stop signal is $768\,ps$ and the largest difference is $1962\,ps$. The delay element in figure 5.1 is used to delay the start signal by a constant delay equals to $768\,ps$. Then the TDC will calculate the time difference between the start and stop signal to convert it to a digital code. Table 5.1 illustrate the input voltages and it's output digital codes.

Volt (mV)	Code	Volt (mV)	Code
-230	0 0 0 0 0 0 0 0	4.6939	0 1 1 1 1 1 0 1
-220.6122	0 0 0 0 0 0 0 1	14.0816	1 0 0 0 0 0 1 0
-211.2245	0 0 0 0 0 1 1 0	23.4694	1 0 0 0 0 1 1 1
-201.8367	0 0 0 0 1 1 0 0	32.8571	1 0 0 0 1 1 0 0
-192.4490	0 0 0 1 0 0 0 1	42.2449	1 0 0 1 0 0 0 1
-183.0612	0 0 0 1 0 1 1 0	51.6326	1 0 0 1 0 1 1 1
-173.6735	0 0 0 1 1 0 1 1	61.0204	1 0 0 1 1 1 0 0
-164.2857	0 0 1 0 0 0 0 1	70.4082	1 0 1 0 0 0 0 1
-154.898	0 0 1 0 0 1 1 0	79.7959	1 0 1 0 0 1 1 0
-145.5102	0 0 1 0 1 1 0 0	89.1837	1 0 1 0 1 1 0 0
-136.1224	0 0 1 1 0 0 0 1	98.5714	1 0 1 1 0 0 0 1
-126.7347	0 0 1 1 0 1 1 0	107.9592	1 0 1 1 0 1 1 0
-117.3469	0 0 1 1 1 0 1 1	117.3469	1 0 1 1 1 1 0 0
-107.9592	0 1 0 0 0 0 0 0	126.7347	1 1 0 0 0 0 0 1
-98.5714	0 1 0 0 0 1 1 0	136.1224	1 1 0 0 0 1 1 1
-89.1837	0 1 0 0 1 0 1 1	145.5102	1 1 0 0 1 1 0 0
-79.7959	0 1 0 1 0 0 0 0	154.8980	1 1 0 1 0 0 1 0
-70.4082	0 1 0 1 0 1 0 1	164.2857	1 1 0 1 0 1 1 1
-61.0204	0 1 0 1 1 0 1 0	173.6735	1 1 0 1 1 1 0 1
-51.6326	0 1 0 1 1 1 1 1	183.0612	1 1 1 0 0 0 1 0
-42.2449	0 1 1 0 0 1 0 0	192.4490	1 1 1 0 0 1 1 1
-32.8571	0 1 1 0 1 0 0 1	201.8367	1 1 1 0 1 1 0 1
-23.4694	0 1 1 0 1 1 1 0	211.2245	1 1 1 1 0 0 1 0
-14.0816	0 1 1 1 0 0 1 1	220.6122	1 1 1 1 0 1 1 1
-4.6939	0 1 1 1 1 0 0 0	230	1 1 1 1 1 1 0 0

Table 5.1: Input voltages and the corresponding codes

To calculate the static ENOB figure 5.2 was drawn. In this figure the blue line represents the output code from cadence using TSMC $65-nm$, the red line represent an ideal straight line, and the red pars represent the residual error. Through calculating the SNQR for this line the static ENOB is equal to 7-bits, the calculation method documented at chapter A.

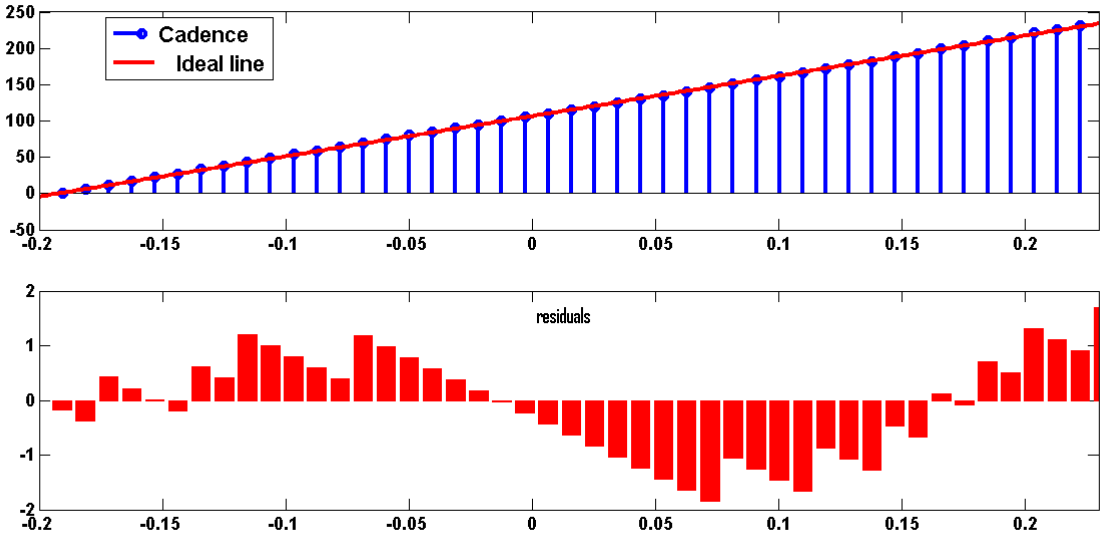

Figure 5.2: Output code linearity

5.1 Area Calculation and distribution

The total system consist of analog part represented in the VTC and digital part represented in the TDC and the PWM to start/stop converter. The VTC consumes 24.5μm^2. The TDC consists of CVDL. FVDL, Interface Circuits, Subtractor, Fat Tree or gates, and others. The CVDL consumes 170.5μm^2, the FVDL consumes 165.8μm^2, the interface Circuits consume 1μm^2, the Subtractor consumes 252μm^2, the Fat Tree consumes 340.5μm^2, and all the other components consume 109.2μm^2.

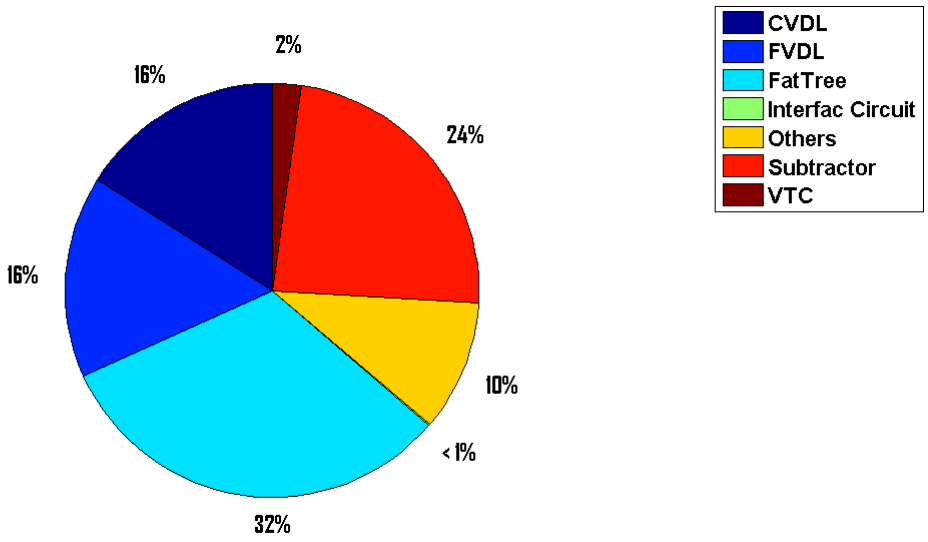

Figure 5.3: Area Distribution

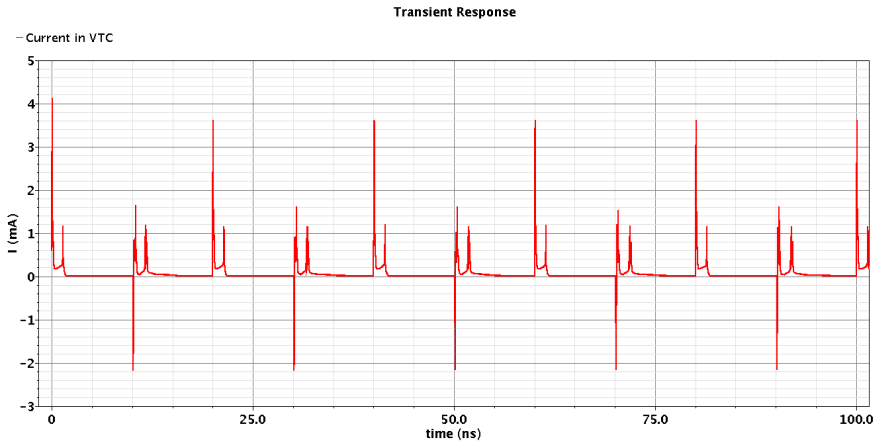

Figure 5.4: Current at the VTC circuit

Parameter	Value
Power	$2.78mW$
Sampling frequency	$170MHz$
Area	$1080\,\mu m^2$
ENOB	6.5
Maximum Input Frequency (without S&H)	$5MHz$

Table 5.2: TB-ADC parameters conclusion

5.2 Power Calculation

The power dissipation is a very important metric at any ADC. The power dissipation for the VTC is $92\,\mu w$at input frequency $1\,MHz$ and clk Frequency $200\,MHz$. Figure 5.4 illustrates the current in the VTC circuit. The whole TB-ADC dissipate 2.78 mW.

5.3 Conclusion

The TB-ADC was simulated using Cadence Tools and TSMC-65nm technology kit. This VTC can operate at maximum clock frequency of $200\,MHz$ and the TDC can operate at maximum clock frequency of $170\,MHz$. Hence, the TB-ADC operates at $170\,MHz$ maximum. The ENOB is 6.5 bits due to the non-linearity of both the VTC and the TDC. Table 5.2

The proposed methodolgy enhanced the VTC circuit for better linearity and increased the dynamic range to 3x comparable to [14]. Also, the propposed design methodology enhanced the sensitivity of the VTC up to $2.6ps/mV$. The proposed TB-ADC is a promising step to increase the integrated systems portability from technology node to technology node. This TB-ADC helps in decreasing the analog part and increasing the digital part in the circuits to save time and effort in the design cycle.

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Appendix A

First Appendix

A.1 Static ENOB calculation

The TB-ADC linearity can be calculated by making parametric analysis over the input voltage for a large number of points span the dynamic range. Choose tools as in figure A.1, choose parametric analysis as in figure A.2

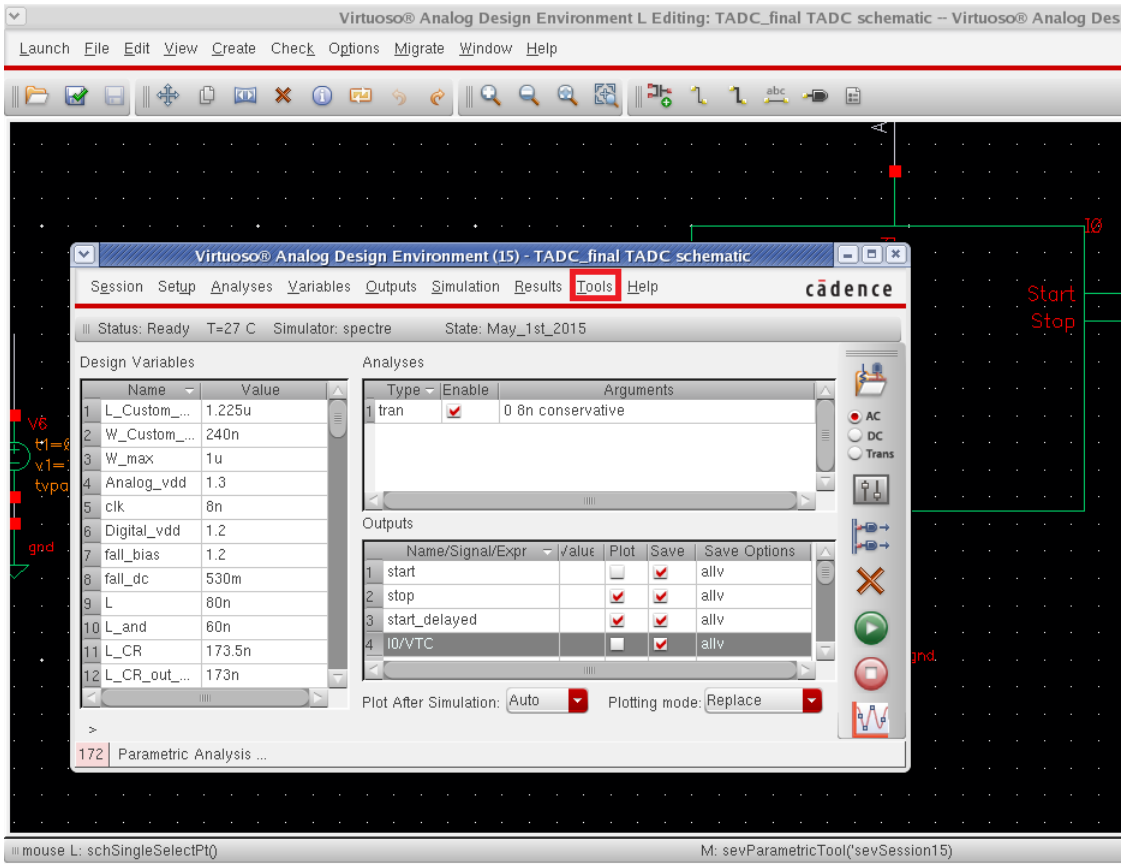


Figure A.1: Static ENOB calculation (Step 1)

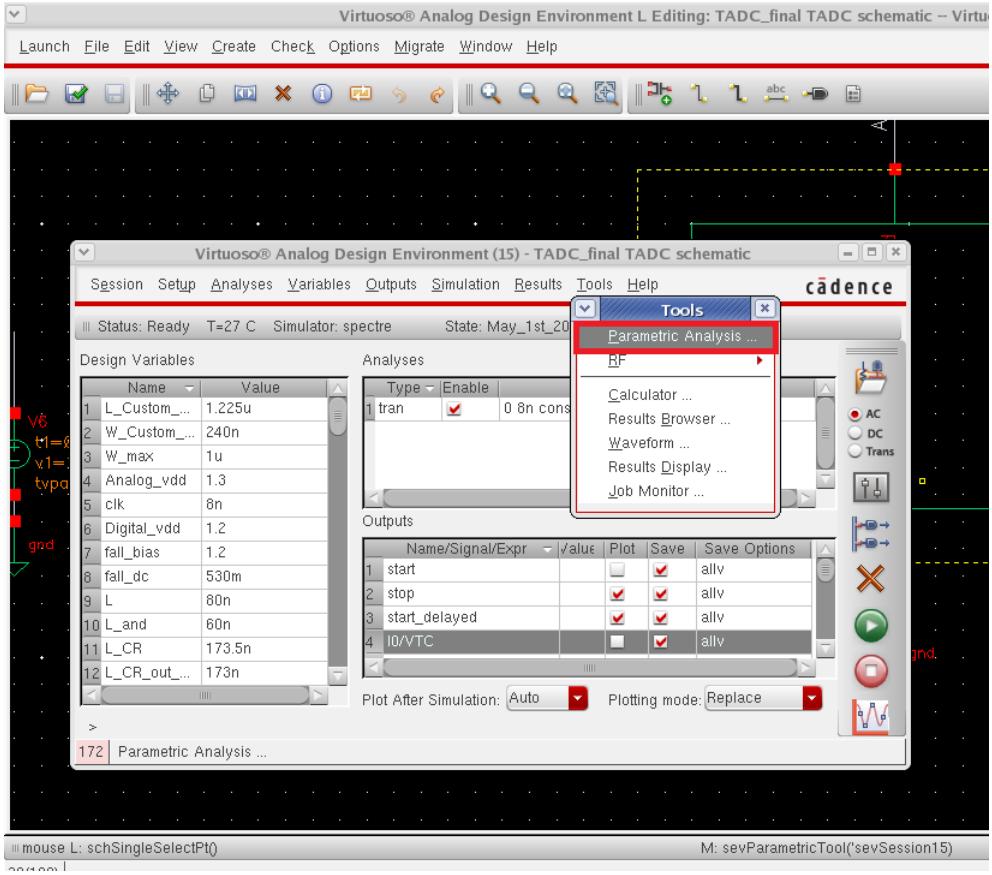


Figure A.2: Static ENOB calculation (Step 2)

Afterwards, define the input voltage, number of simulation point, and start the simulations as in figure A.3. The output bits will be produced as a plot and using the calculator the output bits can be converted to single table as in figures A.4, A.5 and A.6.

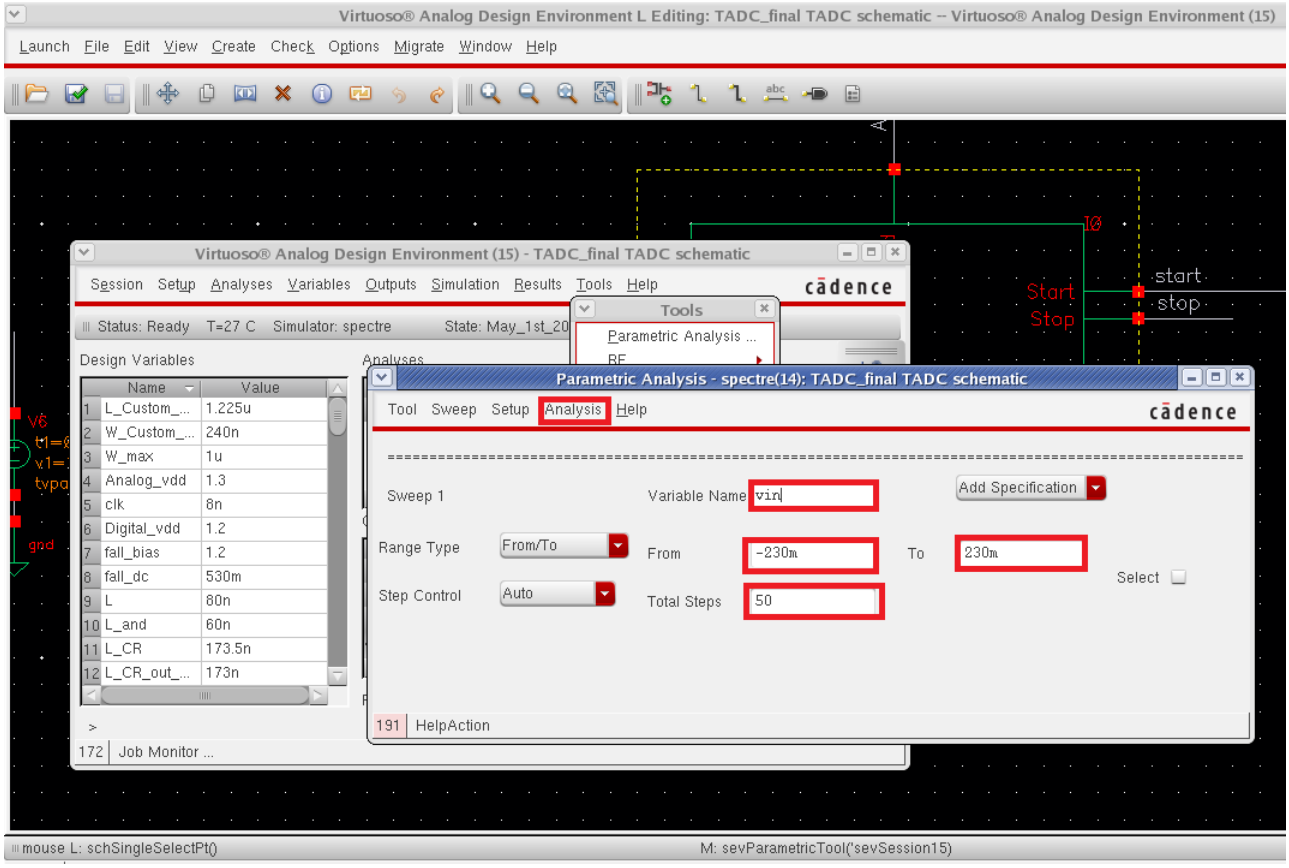


Figure A.3: Static ENOB calculation (Step 3)

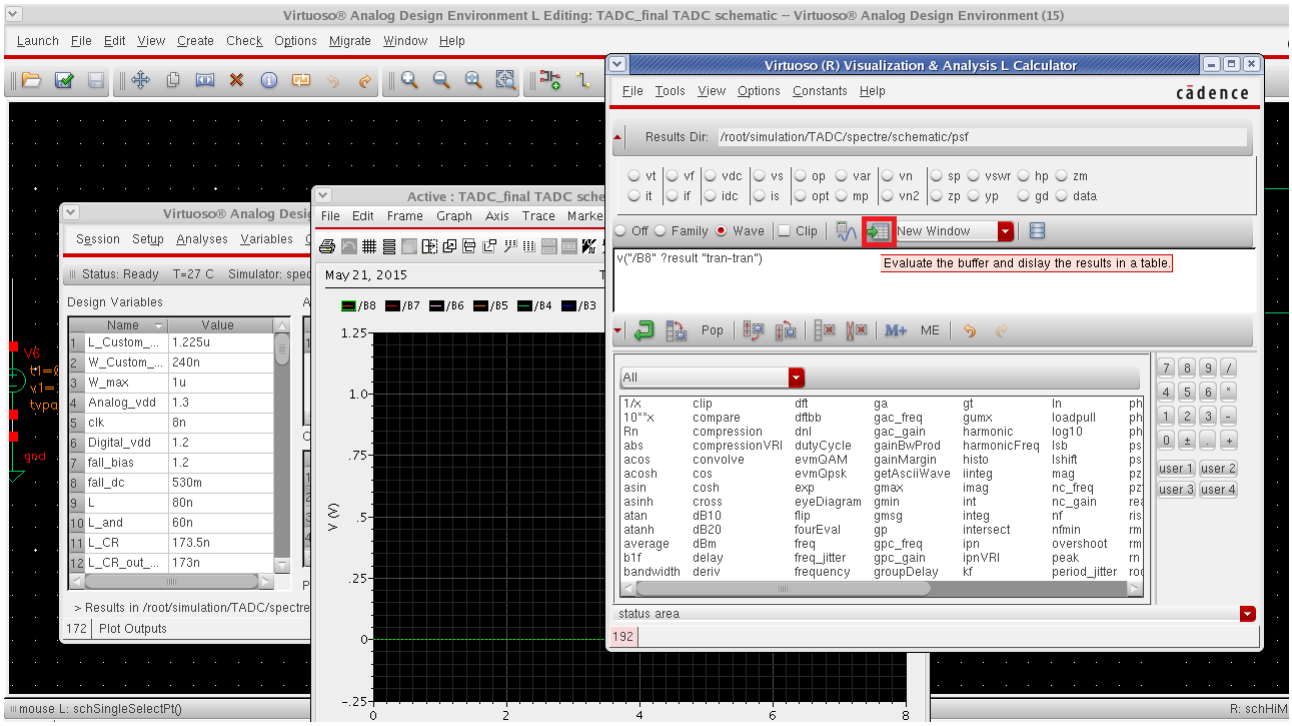


Figure A.4: Static ENOB calculation (Step 4)

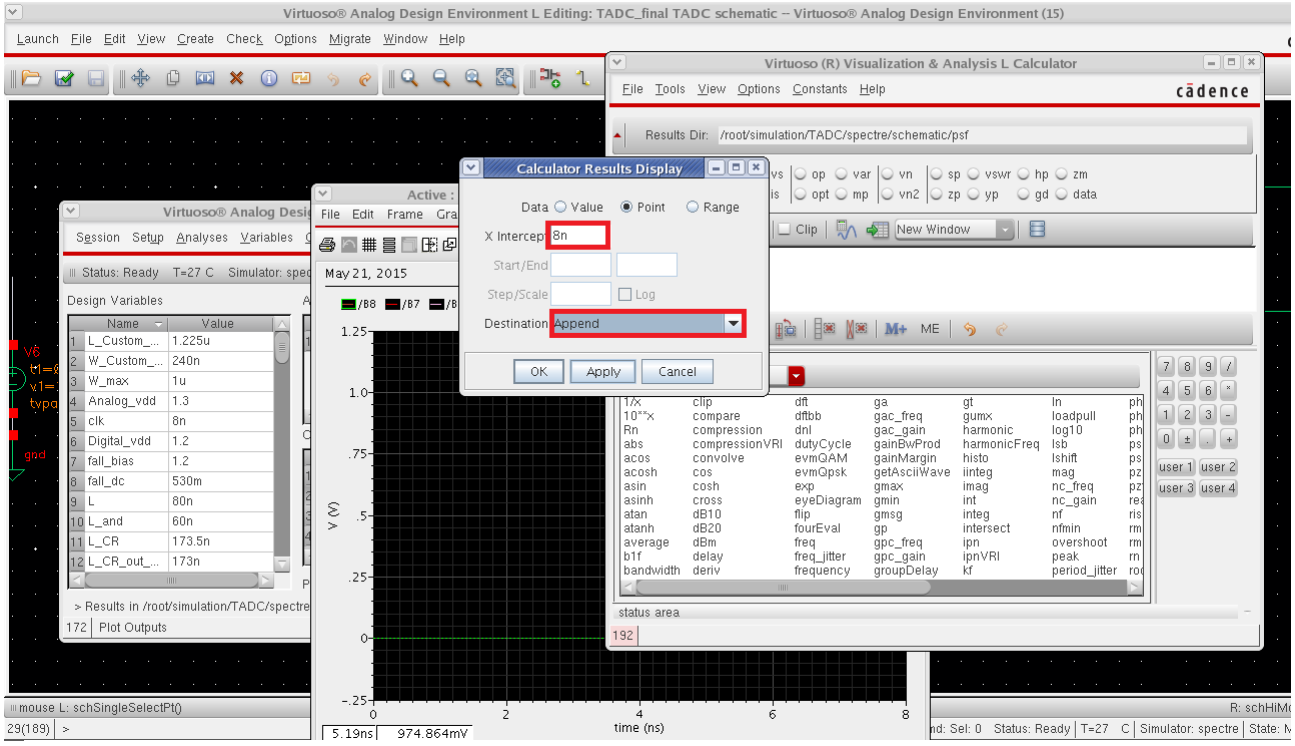


Figure A.5: Static ENOB calculation (Step 5)

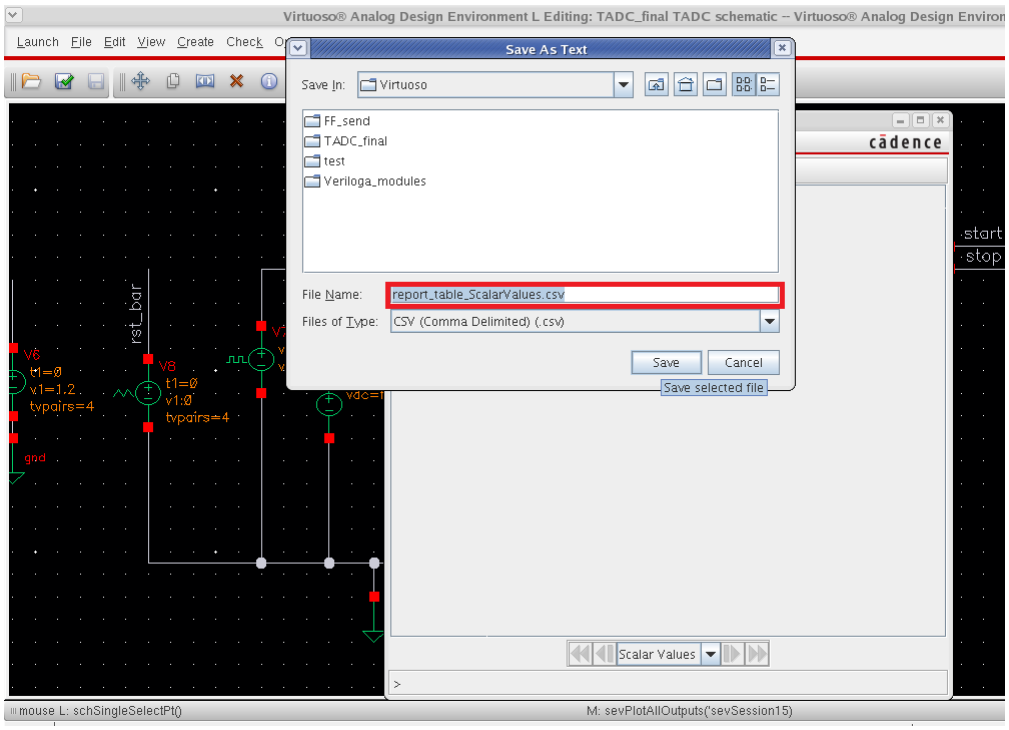


Figure A.6: Static ENOB calculation (Step 6)

Then, the comma seperated variable file is read by the matlab as in figure A.7 and A.8. Figure A.9 illustrate the work space after step 8, all the variable the represent the input voltages and the output codes are stored.

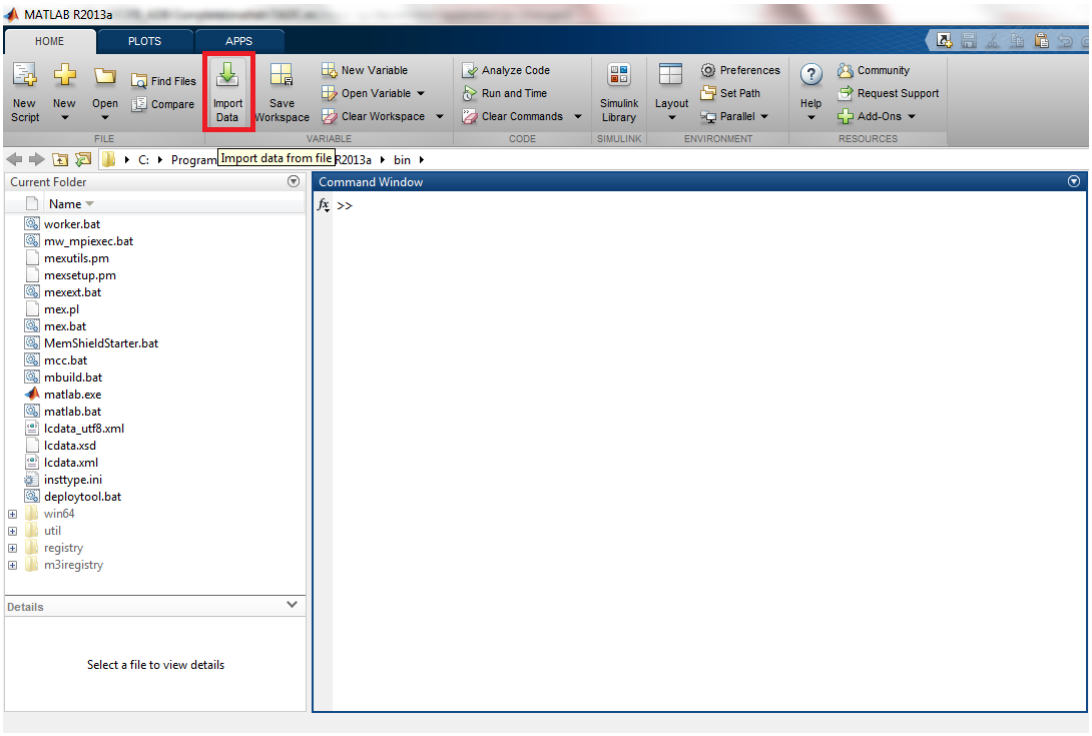
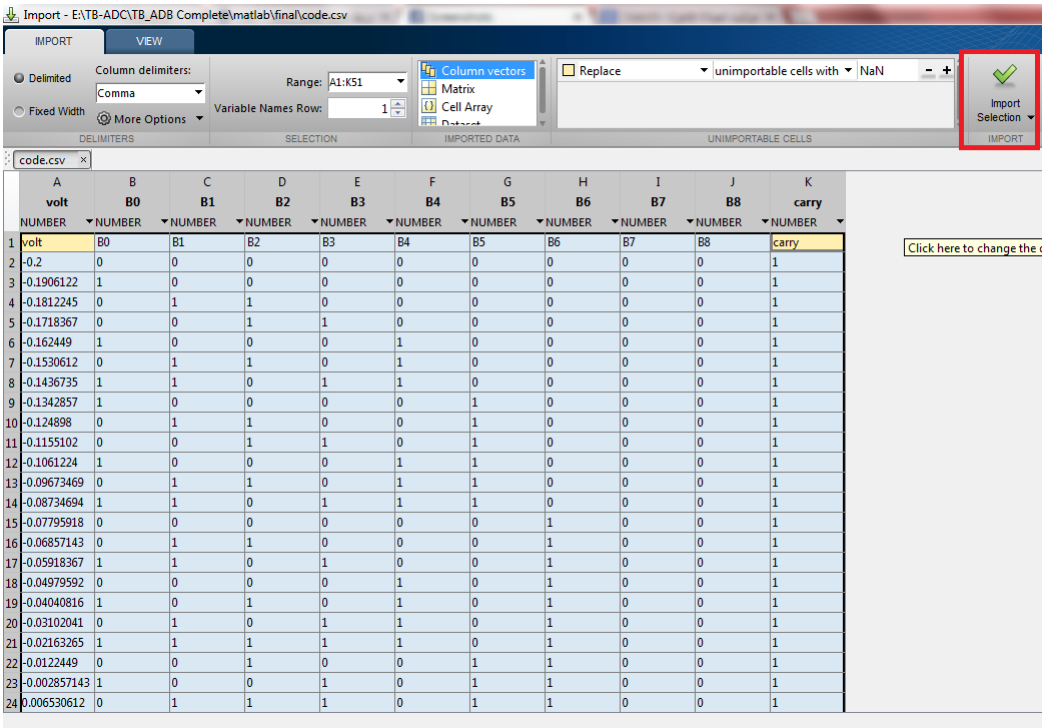


Figure A.7: Static ENOB calculation (Step 7)



	A	B	C	D	E	F	G	H	I	J	K
	volt	B0	B1	B2	B3	B4	B5	B6	B7	B8	carry
	NUMBER	NUMBER	NUMBER	NUMBER	NUMBER	NUMBER	NUMBER	NUMBER	NUMBER	NUMBER	NUMBER
1	volt	B0	B1	B2	B3	B4	B5	B6	B7	B8	carry
2	-0.2	0	0	0	0	0	0	0	0	0	1
3	-0.1906122	1	0	0	0	0	0	0	0	0	1
4	-0.1812245	0	1	1	0	0	0	0	0	0	1
5	-0.1718367	0	0	1	1	0	0	0	0	0	1
6	-0.162449	1	0	0	0	1	0	0	0	0	1
7	-0.1530612	0	1	1	0	1	0	0	0	0	1
8	-0.1436735	1	1	0	1	1	0	0	0	0	1
9	-0.1342857	1	0	0	0	0	1	0	0	0	1
10	-0.124898	0	1	1	0	0	1	0	0	0	1
11	-0.1155102	0	0	1	1	0	1	0	0	0	1
12	-0.1061224	1	0	0	0	1	1	0	0	0	1
13	-0.09673469	0	1	1	0	1	1	0	0	0	1
14	-0.08734694	1	1	0	1	1	1	0	0	0	1
15	-0.07795918	0	0	0	0	0	0	1	0	0	1
16	-0.06857143	0	1	1	0	0	0	1	0	0	1
17	-0.05918367	1	1	0	1	0	0	1	0	0	1
18	-0.04979592	0	0	0	0	1	0	1	0	0	1
19	-0.04040816	1	0	1	0	1	0	1	0	0	1
20	-0.03102041	0	1	0	1	1	0	1	0	0	1
21	-0.02163265	1	1	1	1	1	0	1	0	0	1
22	-0.0122449	0	0	1	0	0	1	1	0	0	1
23	-0.002857143	1	0	0	1	0	1	1	0	0	1
24	0.006530612	0	1	1	1	0	1	1	0	0	1

Figure A.8: Static ENOB calculation (Step 8)

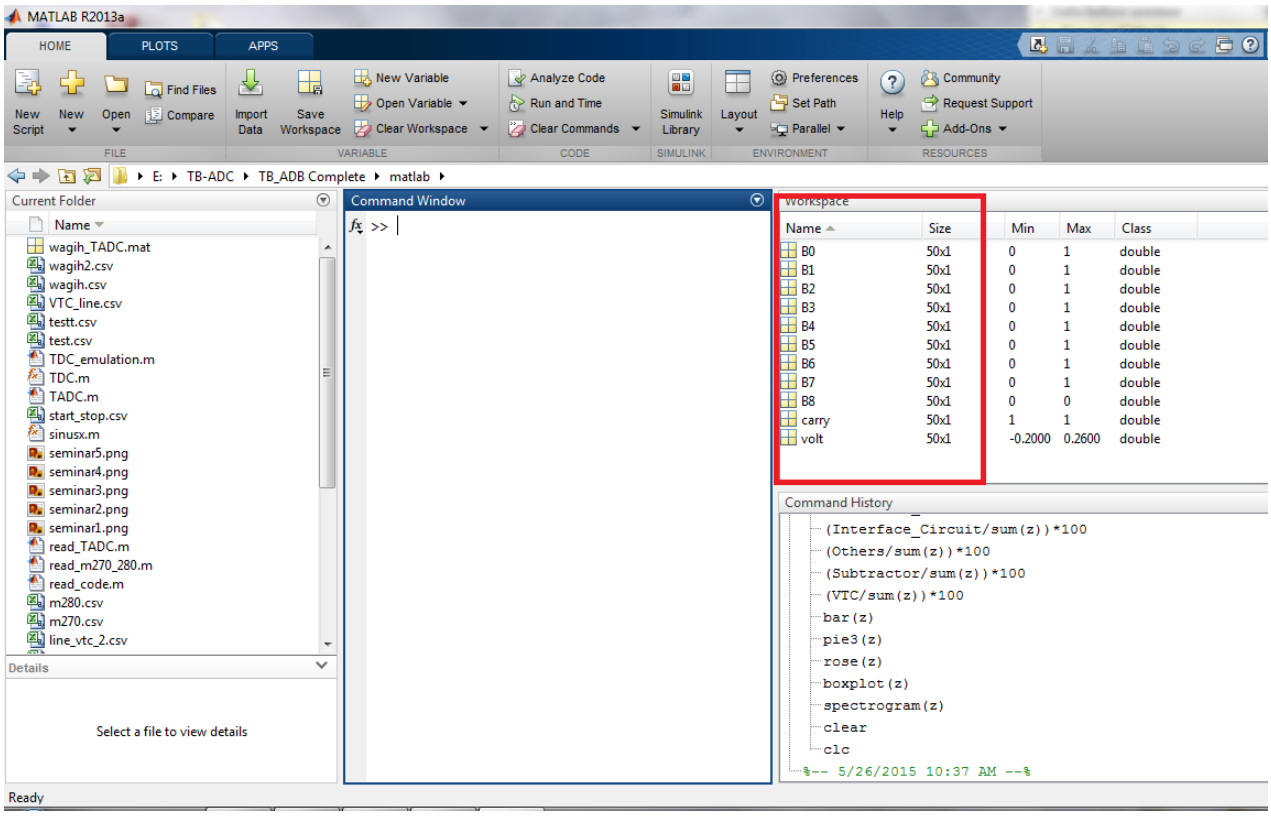


Figure A.9: Static ENOB calculation (Step 9)

Now, we have to convert the binary output codes to decimal and to draw the output vs the input as shown in the following matlab code:

```
clc;
read_code;
B0=round(B0)';
B1=round(B1)';
B2=round(B2)';
B3=round(B3)';
B4=round(B4)';
B5=round(B5)';
B6=round(B6)';
B7=round(B7)';
B8=round(B8)';
```

Volts=volt';

out_code=zeros(1,length(Volts));

for i=1:length(Volts)

out_code(i)=B0(i)*(2^0)+B1(i)*(2^1)+B2(i)*(2^2)+B3(i)*(2^3)+B4(i)*(2^4)+...

B5(i)*(2^5)+B6(i)*(2^6)+B7(i)*(2^7)+B8(i)*(2^8);

end

stem(Volts,out_code);

After runing the previous code figure A.10 will appear, select tools -> Basic Fitting. New window will appear such as figure A.11, choose the linear line that best fit to the real line and choose to plot the residue. Figure A.12 illustrates the residue error between the ideal and real line. Then, then the SQNR can be calculated as $10\log(sum(codes^2)/sum(residue^2))$. ENOB=6.02*SQNR+1.76.

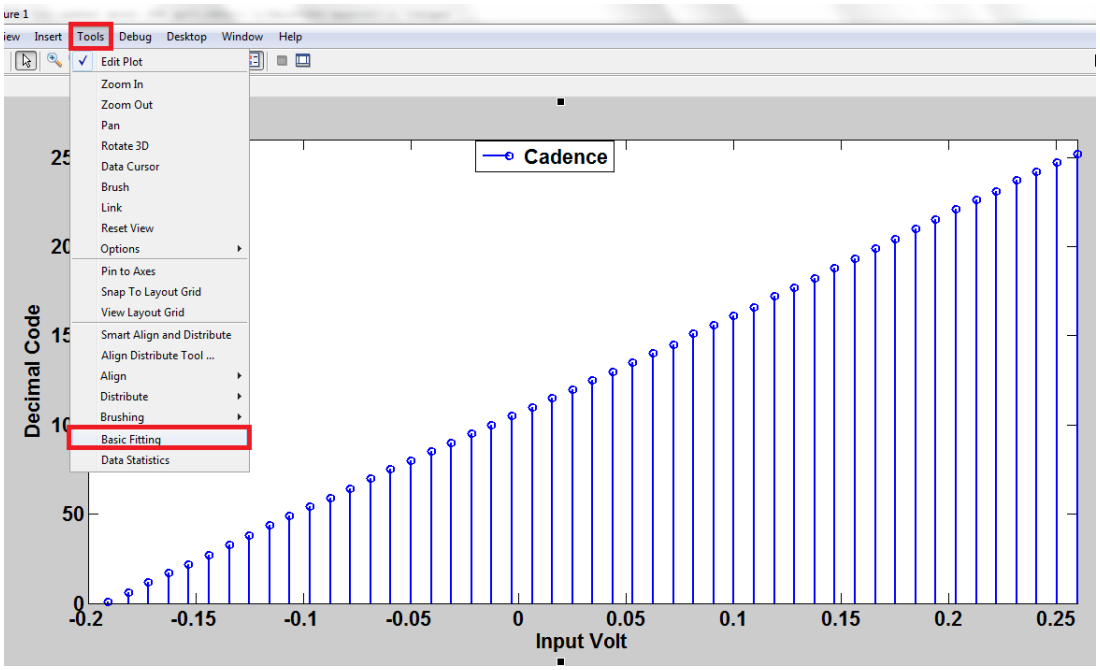


Figure A.10: Static ENOB calculation (Step 10)

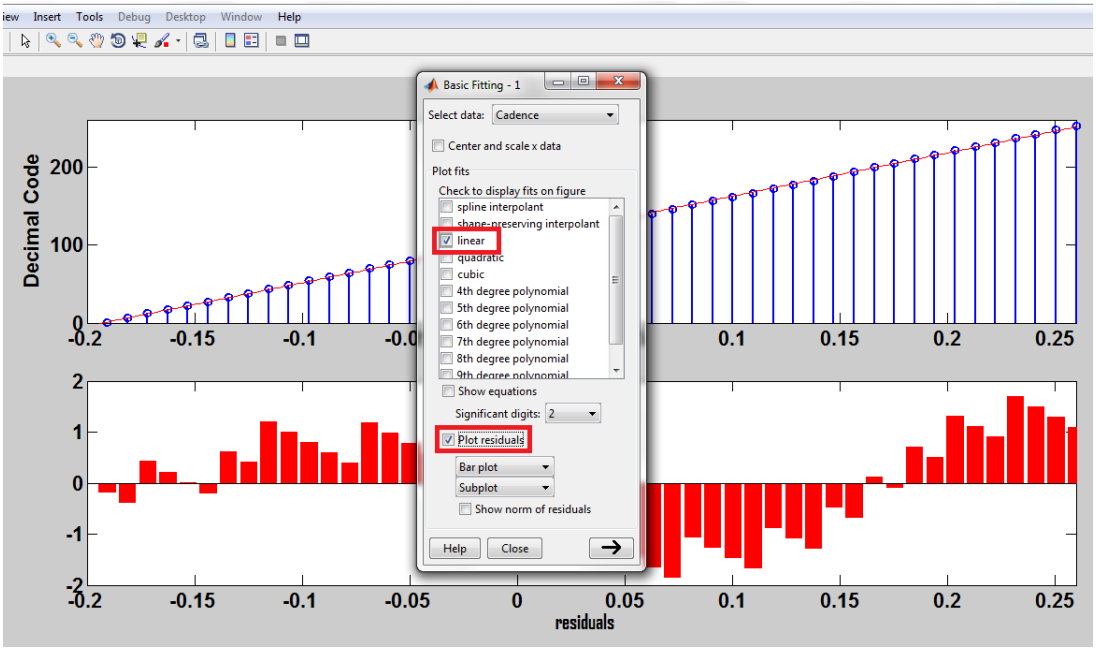


Figure A.11: Static ENOB calculation (Step 11)

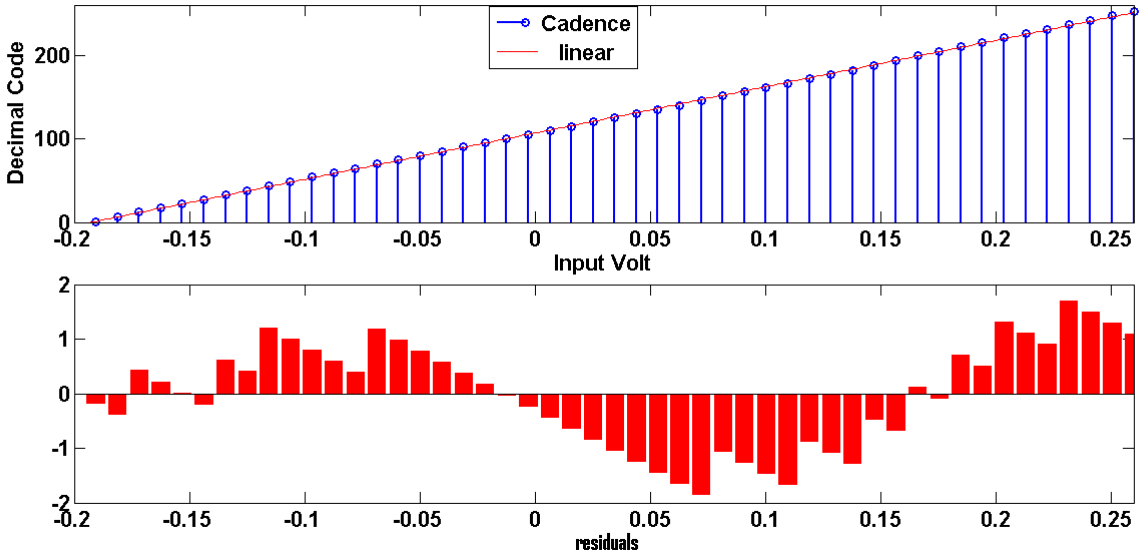


Figure A.12: Static ENOB calculation (Step 12)

A.2 Static Error Calculation For VTC

First run parametric analysis by spaning the input voltage over the dynamic range. Afterwords, using the calculator extract the comma separated value file for the output time vs input voltage curve. Then apply the following matlab code that calculate the static linearity error over tree different circuits like the fall, rise, and the new design methodology circuits as in chapter 3.

```
clear;
clc;
close all;
%% reading the data of fall circuit %%%%%%%%%%%%%%%%%%%%
fall=importdata('E:\TB-ADC\matlab\socc\tpw_f5.csv');
%% reading the data of rise circuit %%%%%%%%%%%%%%%%%%%%
rise=importdata('E:\TB-ADC\matlab\socc\tpw_r5.csv');
%% reading the data of diff circuit %%%%%%%%%%%%%%%%%%%%
diff=importdata('E:\TB-ADC\matlab\socc\final2.csv');
%% smoothing curves and getting linear relation %%%%%%%%%%%%%%%
n=1;
fall_approx=polyfit(fall(:,1),fall(:,2),n);
rise_approx=polyfit(rise(:,1),rise(:,2),n);
diff_approx=polyfit(diff(:,1),diff(:,2),n);
fall_approx_n=polyval(fall_approx,fall(:,1));
rise_approx_n=polyval(rise_approx,rise(:,1));
diff_approx_n=polyval(diff_approx,diff(:,1));
figure;
hold on;
plot(fall(:,1),fall(:,2),'+-.');
plot(rise(:,1),rise(:,2),'m+');
plot(diff(:,1),diff(:,2),'k+-');
plot(fall(:,1),fall_approx_n,'g');
plot(rise(:,1),rise_approx_n,'k');
plot(diff(:,1),diff_approx_n,'r');
hold off; grid; xlabel('Vin in volts');
ylabel('tpw in Sec');
title('pulse width Vs input Volt');
```

```
legend('fall','rise','New methodology ','fall approx','rise approx','New methodology approx');

%% Linearty error calculation %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

fall_error=((fall_approx_n-fall(:,2))./fall_approx(1))*100;

rise_error=((rise_approx_n-rise(:,2))./rise_approx(1))*100;

diff_error=((diff_approx_n-diff(:,2))./diff_approx(1))*100;

figure;

hold on;

plot(fall(:,1),smooth(fall_error));

plot(rise(:,1),smooth(rise_error),'k');

plot(diff(:,1),smooth(diff_error),'r');

plot(t,smooth(fall_error));

plot(t,smooth(rise_error),'k');

plot(t,smooth(diff_error),'r');

hold off;

grid;

xlabel('Vin in volts');

ylabel('error in %');

title('linearity Vs input Volt');

legend('fall error','rise error','New methodology error');
```

Appendix B

Second Appendix

B.1 Dynamic Effective Number Of Bits (ENOB)

The TB-ADC linearity can be calculating through calculating the ENOB. First, make the input voltage source a sine wave generator as in figure B.1. Then, make an AC analyses over a large number of input cycles, where the simulation period was $50\mu s$, the input period was $1\mu s$, and $20ns$ as a sampling clock.

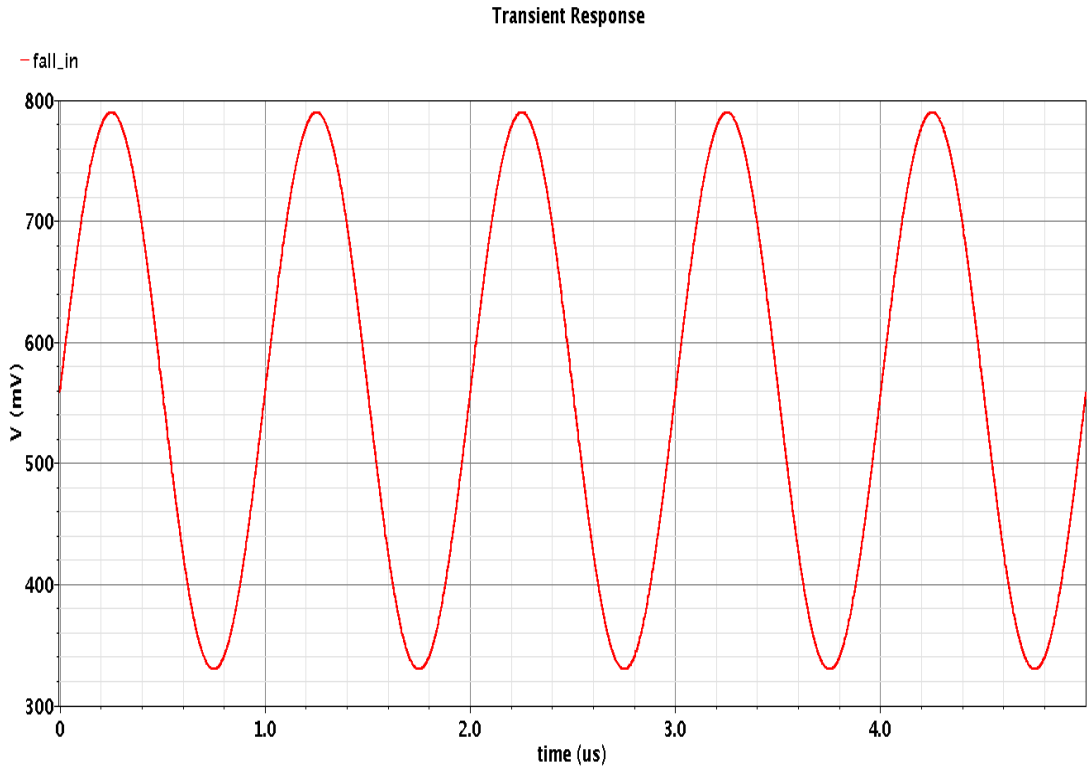


Figure B.1: Input Signal (sine wave)

Then, a group of start and stop signals will appear as shown in figure B.2. Using cadence calculator we can subtract each start signal from its corresponding stop signal as in figure B.3 . Figure B.4is the resultant of the subtraction.

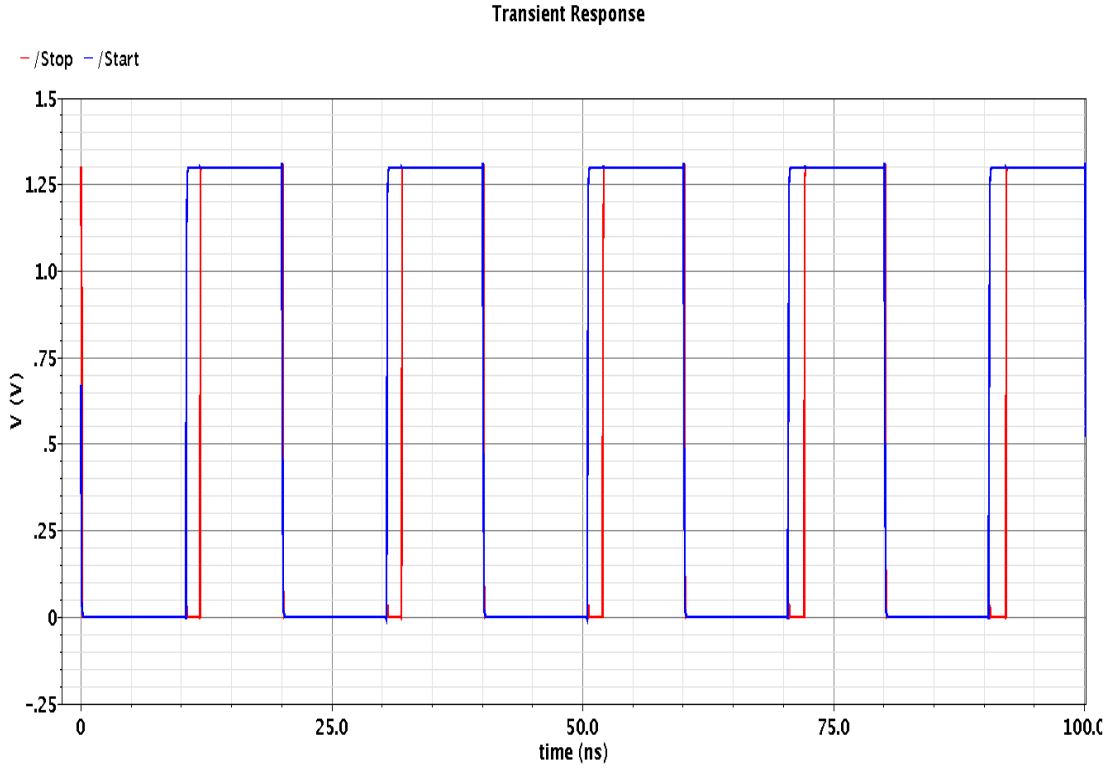


Figure B.2

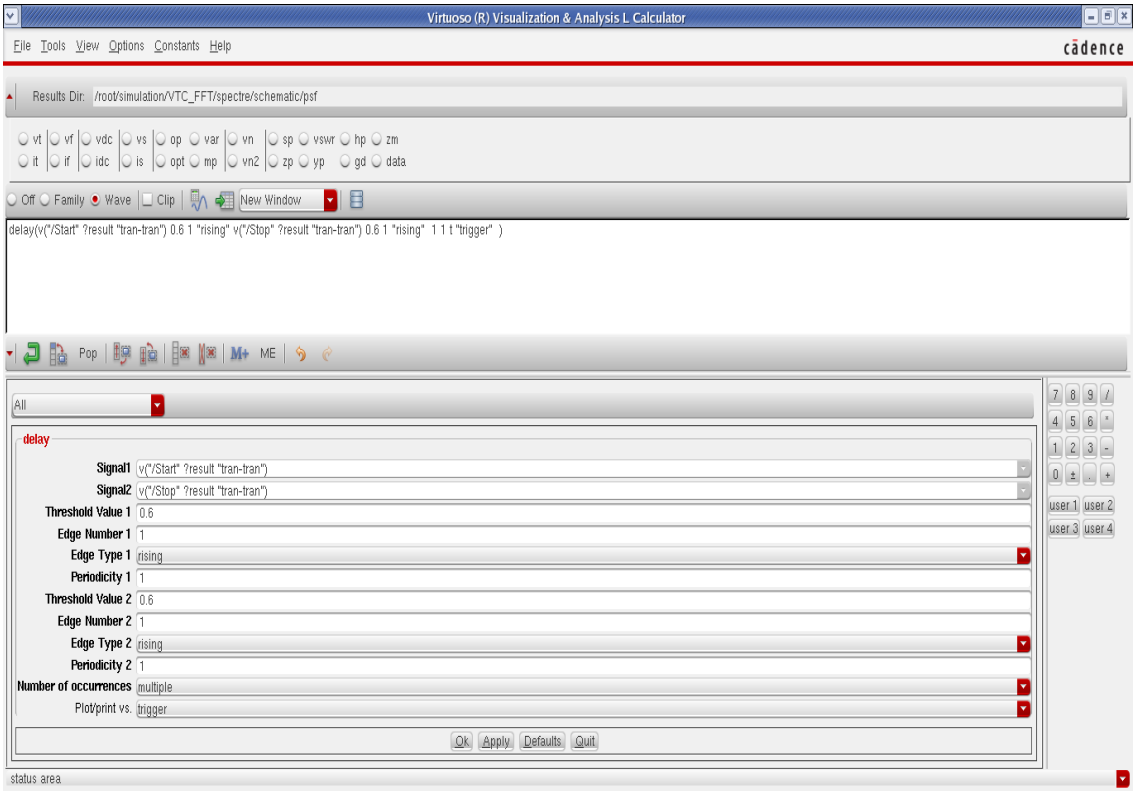


Figure B.3: Cadence calculator during evaluating the time difference between the Start and the Stop signal

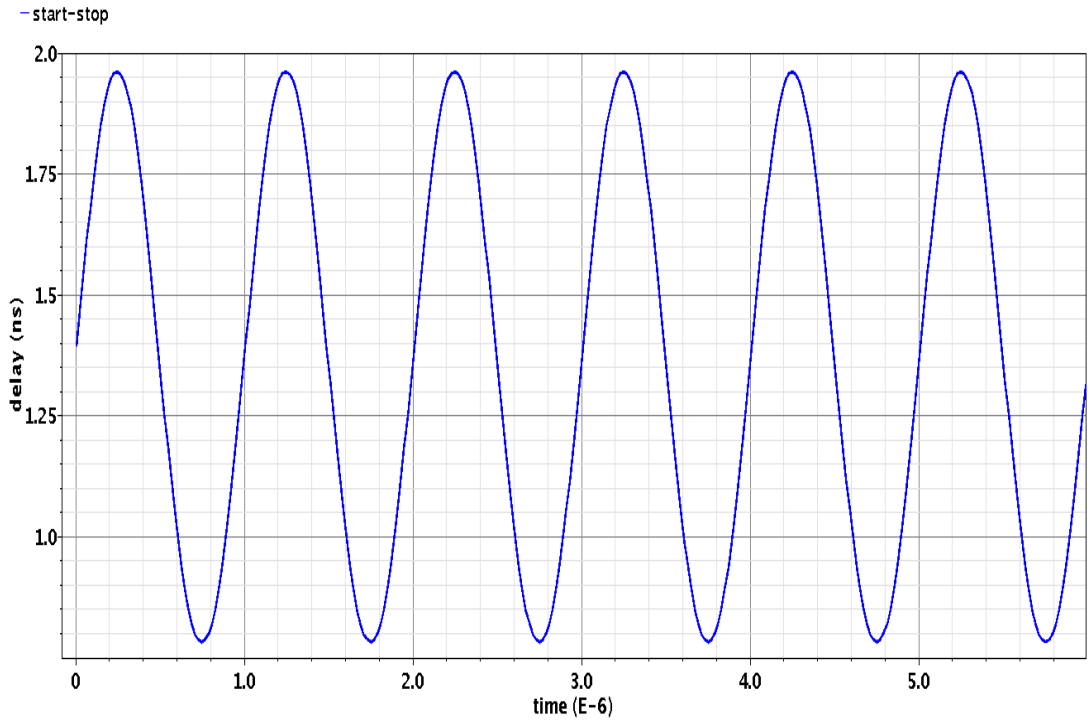


Figure B.4

Figure B.4 is the relation between the input sine wave and the output time, so it has to be as close as possible form the input sine wave. Converting this output signal from time domain to frequency domain will define the different frequency components. Using the Fast Fourier Transform (FFT) from cadence calculator as shown in figure B.5, the different frequency component can be calculated. Figure B.6 illustrate the different frequency components. However, this figure does not illustrate all the frequency because of its scale; so the scale is converted to dB scale to get all the information like in figure [].

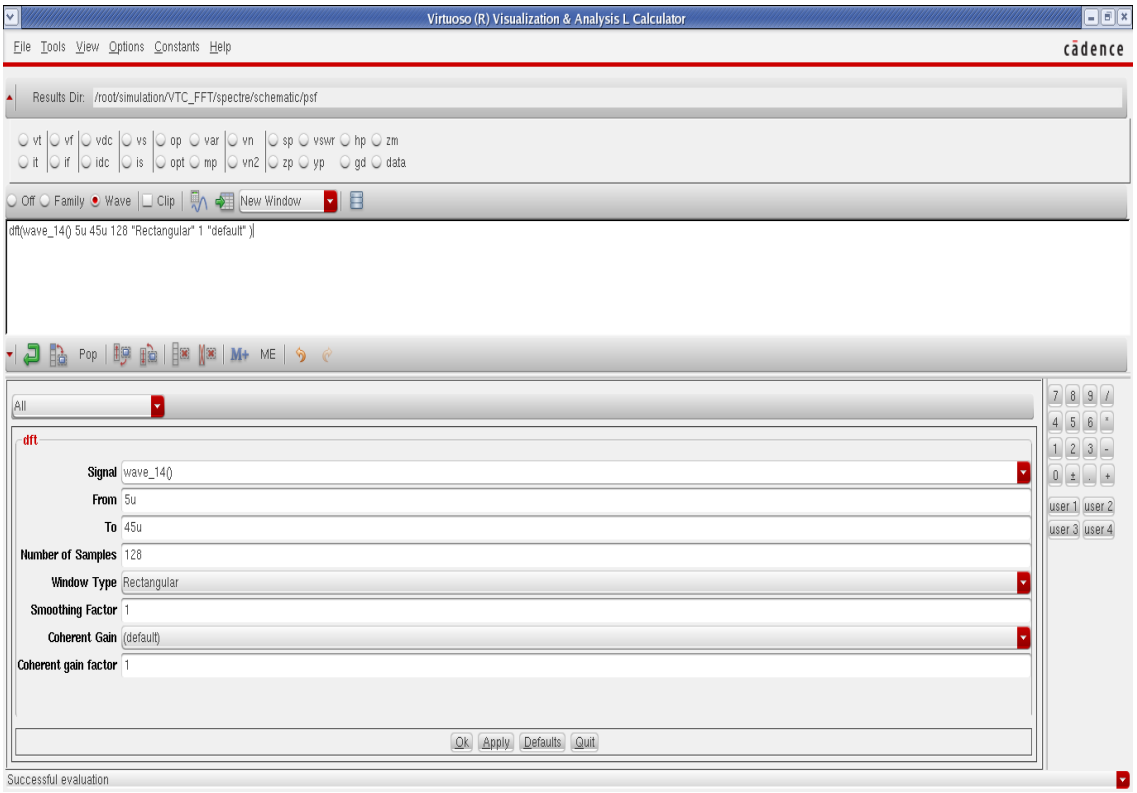


Figure B.5: How to calculate the FFT for a specific singal

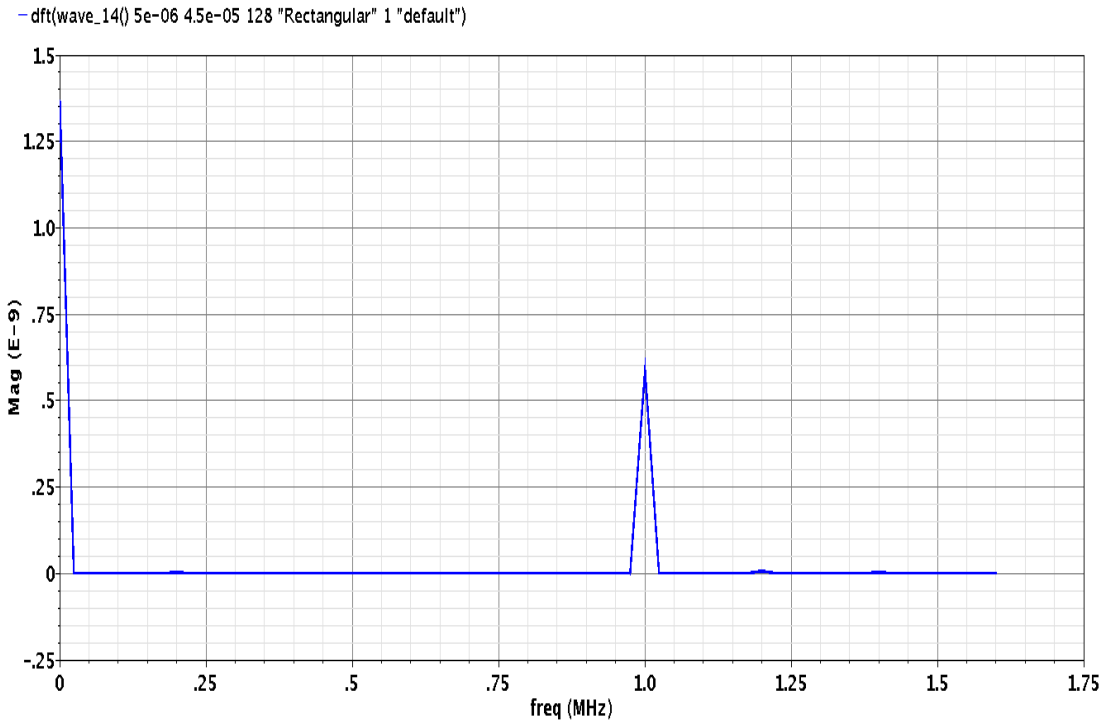


Figure B.6: The FFT result

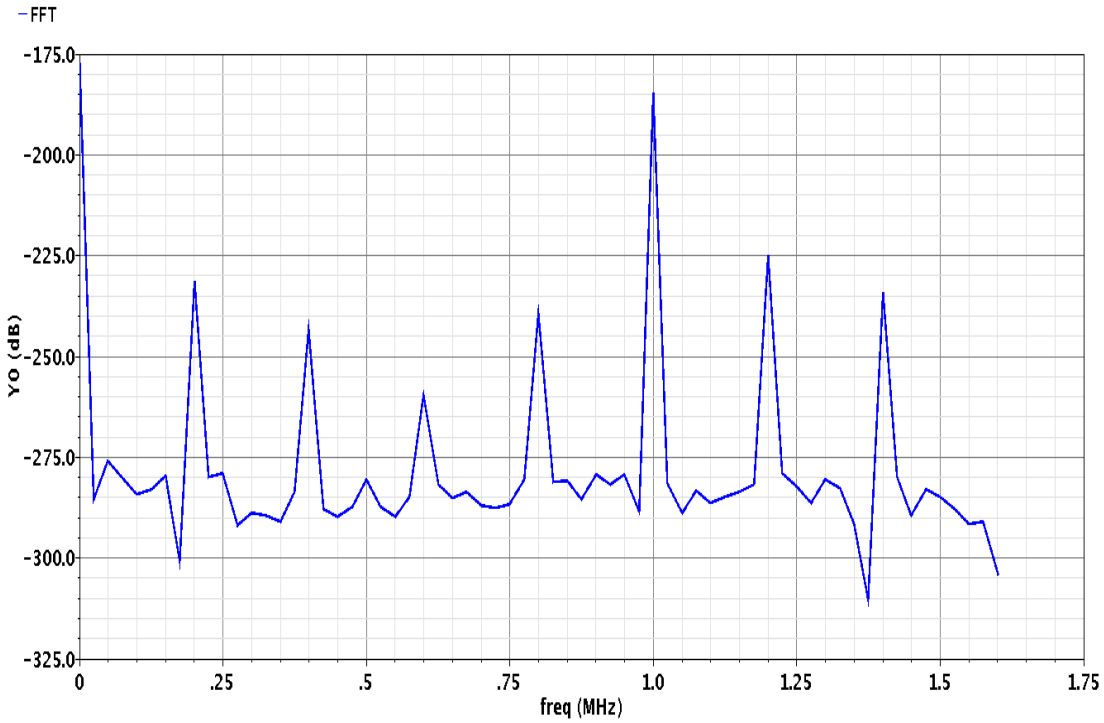


Figure B.7: FFT in dB scale

ملخص الرسالة

تعتبر محولات البيانات أحد أهم الأحجار الرئيسية فى دوائر نظم الراديو المعرفة برمجيا و المستقبلات واسعة النطاق و التطبيقات الطبية الحيوية و النظم المدمجة. الغالبية العظمى من الدوائر المتكاملة اليوم هى دوائر تجمع ما بين الإلكترونيات التناظرية و الإلكترونيات الرقمية للأستفاده من القدرات المتناميه لمعالجات الأشارات الرقمية. المعالجة الرقمية للإشارات تتفوق على المعالجات التناظرية فى الكثير من النواحى. و لذالك الهدف من هذا العمل هو تقليل نسبة الوحدات التناظرية على حساب نسبة الوحدات الرقمية فى الأنظمة آنفة الذكر.

يوجد العديد من أنواع محولات البيانات للتماشى مع المتطلبات المختلفة للأنظمة المتعددة. عوامل الأداء الأكثر تأثيرا هى السرعة , الطاقة المستنزفة, و الدقة. اعتمادا على احتياجات الأنظمة المختلفة يمكن تصميم محول البيانات الأمثل. يوجد فى البحوث العلمية السابقة أمثلة متعددة لمحولات البيانات كمحول البيانات اللحظى, المسجل التقاربى المتتالى , المنحدر الخطى, سيجما–دلتا و المحول الأنبوبى. كل المحولات الآنفة الذكر تعتمد بشكل اساسى على مكبر العمليات التناظرى.

تقليص نسبة الجزء التناظرى و زياده نسبة الجزء الرقمى فى الدوائر المتكاملة هو اتجاه عام ينصح به للحصول على أقصى أستفاده من عملية التصغير المستمرة للترانزستور. التصغير الذى لا ينتهى للترانزستور يجعل طول القناة اقصر مما يؤدى الى زياده كثافه الترانزستور على نفس المساحة مؤديا الى تقليص جهد المصدر. خفض جهد المصدر يزيد من العقبات و التحديات المفروضة على تصميم الدوائر التناظرية نظرا لأن جهد الحد الأدنى و الضوضاء لا يتقلصان بنفس معدل جهد المصدر. كلما قل مدى جهد الخارج كلما زادت صعوبة استخدام الترانزستورات المتراكمة بسبب الضوضاء و الجهد المطلوب لتعمل الترانزستورات فى نطاق التشبع. على النقيض, يتفوق أداء الدوائر المتكاملة الرقمية على الدوائر المتكاملة التناظرية فى التقنيات الحديثة ذات القنوات الصغيرة. وقت التحول يصبح أصغر و بالتالى تصبح الدوائر التى تعتمد على الوقت أكثر دقة من نظيرتها التناظرية التى تعتمد على الجهد.

فى هذه الرسالة, سوف نقوم بتقديم محول البيانات المعتمد على الوقت كبديل لمحول البيانات التقليدى فى بعض الأنظمة. الهدف الأساسى من هذا النوع من محولات البيانات هو تقليل نسبة الدوائر التناظرية لحساب الدوائر الرقمية. أيضا هذا النوع من محولات البيانات لا يحتاج إلى مكبر العمليات و يعتمد بشكل اساسى على الدقة الزمنية التى تزداد مع تطور التكنولوجيا. بالأضافة إلى عدم الحاجة إلى دائرة أخد العينات و التثبيت.

مهندس: محمد وجيه امام اسماعيل
تاريخ الميلاد: ١٩٩٠/١١/٢٣
الجنسية: مصري
تاريخ التسجيل: ٢٠١٢/١٠/٠١
تاريخ المنح: yyyy/mm/dd
الدرجة: الماجستير
القسم: هندسة الإلكترونيات والاتصالات الكهربية

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عنوان الرسالة:

تصميم محول تناظرى رقمى معتمد على صيغة الوقت: طريقة تصميم جديدة لدوائر تحويل الجهد إلى الوقت

الكلمات الدالة:
محول الجهد للوقت، محول تناظرى رقمى، نظم الراديو المعرفة برمجيا ، محول الوقت لرمز

ملخص الرسالة:
فى هذه الأطروحة نقدم طريقة تصميم جديدة لدوائر محولات الجهد الى فواصل زمنية مناسبة للمحولات التناظريه الرقمية المعتمدة على صيغة الوقت. لقد تم اختبار هذه الطريقة الجديدة على محول تناظرى رقمى ذى معدل منخفض لأستهلاك الطاقة ليكون بديلا للمحول التناظرى الرقمى التقليدى. تتكون المرحلة الاولى من هذا المحول من محول جهد إلى صيغة الوقت و المرحلة الثانية هى محول صيغة الوقت إلى رمز رقمى. يتميز هذا النوع من المحولات بأن الجزء الأكبر من الدوائر المستخدمة فيه دوائر رقمية و لا يعتمد على مكبر العمليات مطلقا.

تصميم محول تناظرى رقمى معتمد على صيغة الوقت: طريقة تصميم جديدة لدوائر تحويل الجهد إلى الوقت

إعداد

محمد وجيه امام اسماعيل

رسالة مقدمة إلي
كلية الهندسة – جامعة القاهرة
كجزء من متطلبات الحصول علي درجة
الماجستير
في
هندسة الإلكترونيات و الاتصالات الكهربية

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الجيزة – جمهورية مصر العربية
٢٠١٥

تصميم محول تناظرى رقمى معتمد على صيغة الوقت: طريقة تصميم جديدة لدوائر تحويل الجهد إلى الوقت

إعداد

محمد وجيه امام اسماعيل

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كلية الهندسة – جامعة القاهرة
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٢٠١٥

تصميم محول تناظرى رقمى معتمد على صيغة الوقت: طريقة تصميم جديدة لدوائر تحويل الجهد إلى الوقت

إعداد

محمد وجيه امام اسماعيل

رسالة مقدمة إلي
كلية الهندسة – جامعة القاهرة
كجزء من متطلبات الحصول علي درجة
الماجستير
في
هندسة الإلكترونيات و الاتصالات الكهربية

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