

The American University in Cairo

School of Science and Engineering

A Novel Versatile CMOS Operational Floating Current Conveyor Amplifier

A Thesis Submitted to

Electronics and Communication Engineering Department

In partial fulfillment of the requirements for
the degree of Master of Science

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*To my Family,
You Mean The World To Me.*

*A dream doesn't become reality through magic; it takes sweat,
determination and hard work.*

COLIN POWELL

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First of all, I would like to thank God for all what He granted me in my life in every single aspect. I believe that God has provided me with blessings, care and guidance throughout my way.

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Abstract

Nowadays, current mode devices are used as active elements at the circuits that work at high frequencies. A novel integrated CMOS based the operational floating current conveyor (OFCC) is proposed. OFCC is a five port general purpose analog building block which combines all the features of different current mode devices such as the second generation current conveyor (CCII), the current feedback operational amplifier (CFA), and the operational floating conveyor (OFC).

The OFFC is modeled and simulated using UMC 130nm technology kit in Cadence and the supply voltage of the proposed OFCC is 1.2V. Non-inverting voltage amplifier, current mode instrumentation amplifier (CMIA), universal filter and electrocardiogram read out circuit (ECG) are the applications based on OFCC that are designed to check the circuit's validity.

ECG is used in diagnosing heart diseases. It is designed as integration between current-mode instrumentation amplifiers (CMIA) and low pass filter (LPF). Normal heart behavior can be identified simply by normal ECG that consists of signal while heart disorder can be recognized by having differences in the features of their corresponding ECG waveform.

The main advantage of the proposed OFCC that it provides a wide bandwidth compared to other work. In addition, the applications based on OFCC shows good results compared to others.

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List of Symbols

- A_V : Open loop voltage amplifier gain (Volt/Volt)
- C : the effective output capacitance of the CCII+
- C_C : Compensation capacitor (Farad)
- e_n : Input noise voltage (Volt/sqrt(Hz))
- G : The closed loop gain
- G_{exact} : The closed loop gain of the actual VFA.
- G_{ideal} : The closed loop gain of ideal amplifier.
- hi_1 : The current tracking accuracy at Z_+ terminal (I_{Z_+})
- hi_2 : The current tracking accuracy at Z_- terminal (I_{Z_-})
- h_V : The voltage tracking accuracy
- I_B : Input bias current (Ampere)
- I_W : Output current at terminal W
- I_{Z_+} : Output current at terminal Z_+
- I_{Z_-} : Output current at terminal Z_-
- R_F : Feedback resistance of CFA circuit (Ohm)
- R_G : the gain setting resistor
- R_L : Load resistance (Ohm)
- R_W : Feedback resistance of OFCC circuit (Ohm)
- r_x : Open loop input resistance (Ohm)
- V_{IN} : Input voltage (Volt)
- V_{IO} : Input offset voltage (Volt)
- V_{OUT} : Output voltage (Volt)
- X_{ERROR} : Error signal (voltage or current)
- X_F : Output signal of the feedback network (voltage or current)
- X_{IN} : Error signal (voltage or current)
- X_{OUT} : Feedback signal (voltage or current)
- ϵ_{i+} : The current tracking error at Z_+ terminal
- ϵ_{i-} : The current tracking error at Z_- terminal

ϵ_v : The voltage tracking error

ω_o : The natural frequency

Q: Quality factor

$Z_T(s)$: The single pole frequency dependent open loop transimpedance.

List of Abbreviations and Nomenclature

AC: Alternating current

BJT: Bipolar junction transistor

BPF: Band pass filter

BW: Bandwidth

CCCS: Current controlled current source

CCI: First generation current conveyor

CCII: Second generation current conveyor

CCII+: Positive second generation current conveyor

CCII-: Negative second generation current conveyor

CCVS: Current controlled voltage source

CFA: Current feedback amplifier

CMOS: Complementary Metal Oxide Semiconductor

CMRR: Common mode rejection ratio

dB: Decibel

DC: Direct current

GBP: Gain bandwidth product

GND: Ground (Zero voltage)

HPF: High pass filter

Hz: Hertz

kHz: 10E3 hertz

K Ω : 10E3 ohm

LOC: Lab-On-a-Chip

LPF: Low pass filter

mA: 10E-3 ampere

MHz: 10E6 hertz

MOSFET: Metal-oxide-semiconductor field-effect transistor

Rms: Root mean square

V: Volt

VB1: DC bias voltage 1

VB2: DC bias voltage 2

VCCS: Voltage-controlled voltage source

VCVS: Voltage-controlled current source

VFA: Voltage feedback amplifier

μm : 10E-6 meter

Chapter 1: Introduction

1.1 Introduction

Analog signal processing has an important role nowadays in both Lab-On-A-Chip (LOC) and communication systems. A LOC is a device that integrates one or more circuit performing different functions on a single chip. The main part of the LOC system is the read out circuit and to build this circuit, the amplifier circuit is needed. The amplifier circuit can be implemented using either a current mode or a voltage mode.

Digital and analog applications can be built using either bipolar junction transistor (BJT) or metal oxide semiconductor field effect transistor (MOSFET). In most of the applications nowadays MOSFET is used although it is slower than the BJT but on the other side it has lower power consumption. In addition, it is smaller in size than the BJT. Moreover, it permits large number of transistors to be packed together before heat problem happens [1–4].

For the voltage mode amplifier, the voltage signal is processed by the amplifier circuit. On the other hand, for the current mode amplifier the current signal is processed by the amplifier circuit.

Originally, voltage mode was used in amplifier circuits then current mode has started to take place [5]. Both the voltage and current modes can be used in the same applications but they have different characteristics. The advantages and disadvantages of both the voltage and current mode is discussed in chapter two.

There are different current mode circuits such as the first generation current conveyor (CCI), the second generation current conveyor (CCII), the current-feedback amplifier (CFA), the operational floating conveyor (OFC), and the operational floating current conveyor (OFCC).

This research presents a novel integrated CMOS current mode circuit, titled, operational floating current conveyor (OFCC) and its applications.

1.2 Motivation

Having a constant gain-bandwidth product which affects the bandwidth of the amplifier by reducing it is the main disadvantages of the voltage mode circuit. Also, the slew rate is low in the voltage mode circuit.

OFCC is a current mode circuit which overcomes the previous problems that occurs in the voltage mode circuits [6]. OFCC can be used in many applications, which are discussed in chapter 4.

The OFCC circuit was firstly proposed by Khan. It was designed using discrete elements based on discrete BJTs and a commercial current-feedback amplifier (AD846) [7].

1.3 Thesis Outline

This thesis is organized in five chapters and one appendix as follows:

Chapter 1 presents a general introduction for the proposed amplifier circuit and describes the motivation of this work.

Chapter 2 discusses the differences between current and voltage mode devices. It presents the classification of the amplifiers in addition to the different types of current mode devices. The noise in amplifier circuits is presented as well.

In Chapter 3, the proposed design for OFCC circuit as well as a discussion comparing the advantages of the proposed OFCC with other existing circuits is presented.

Chapter 4 presents different applications based on OFCC, such as a non-inverting voltage amplifier, current mode instrumentation amplifier and universal filter. Moreover, an integrated ECG readout circuit based on OFCC as a building block is presented and discussed.

Chapter 5 contains the conclusion and the future work.

The derivations of the used equations in chapters 4 are introduced in appendix A.

Chapter 2: Current mode devices

2.1 Introduction

In this chapter, a brief literature review of the different types of current mode devices like first generation current conveyor (CCI), second generation current conveyor (CCII), the current feedback amplifier (CFA), the operational floating conveyor (OFC), and the operational floating current conveyor (OFCC) is presented. Also, the difference between current mode (represented by CFA) and voltage mode (represented by VFA) devices is discussed. In addition, at the end of this chapter there is a brief discussion of the noise and its different sources as the noise in analog circuits is an important parameter which may affect the output signal.

2.2 Amplifier Circuits

The power and/or amplitude of a signal is increased using the electronic amplifier by taking power from the DC power supply and controlling the output to match the input signal shape but with larger amplitude.

The gain of the amplifier circuit can be defined as:

1. The ratio between the output and the input voltages.
2. Or the ratio between the output and the input power.
3. Or any other combination of current, voltage and power.

There are four types of amplifiers depending on the types of the input and output signals of the amplifiers. Table 2-1 shows the ideal input/output impedance values of the four amplifier types. Figure 2-1 shows an ideal equivalent circuit for each [8].

Table 2-1: Ideal Values of Input and Output impedances for Amplifiers

Amplifier type	Dependent source	Input impedance	Output impedance
Transresistance Amplifier	CCVS	0	0
Voltage Amplifier	VCVS	∞	0
Transconductance Amplifier	VCCS	∞	∞
Current Amplifier	CCCS	0	∞

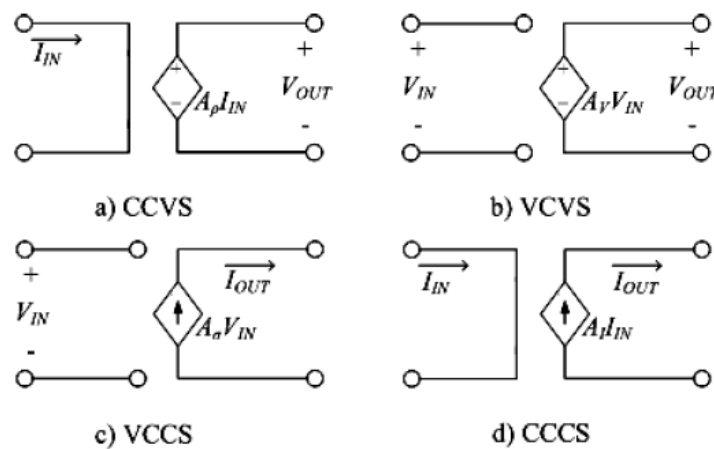


Figure 2-1: Equivalent circuits for different amplifier circuits a) Current-Controlled Voltage Source b) Voltage-Controlled Voltage Source c) Voltage-Controlled Current Source d) Current-Controlled Current Source [9]

2.3 Feedback Amplifiers and Feedback Topologies

Normally, the amplifier circuit is used in a feedback configuration. The feedback system can be either positive feedback or negative feedback. Oscillator circuits use a positive feedback configuration. On the other hand, a stable amplifier circuit or an oscillator circuit under certain conditions (named as Barkhausen condition which depends on the loop gain of the feedback system) use negative feedback [9].

The advantages of the negative feedback system are: 1) it minimizes circuit distortion, 2) increases the bandwidth of the system, 3) improves the input and output impedance of the amplifier circuit and 4) lessens sensitivity of the output to the component variations. Figure 2-2 shows a general negative feedback block diagram.

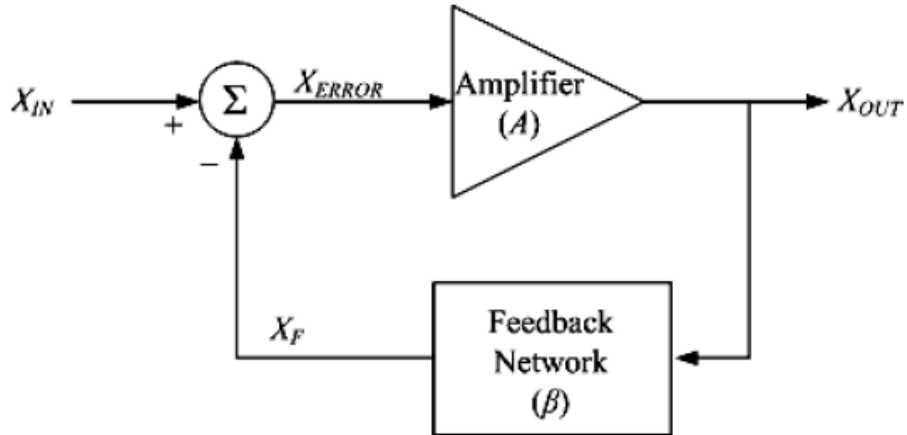


Figure 2-2: General negative feedback block diagram [9]

X_{OUT} : is the output signal of the system (voltage or current).

X_{IN} : is the input signal of the system (voltage or current).

X_{ERROR} : is the error signal (input signal of amplifier).

X_F : is the output signal of the feedback network.

A : is the open loop gain of the amplifier.

β : is the gain of the feedback network.

The overall gain of the system [8]:

$$\mathbf{G} = \frac{X_{OUT}}{X_{IN}} = \frac{A}{1+\beta A} \quad (2-1)$$

βA : is defined as the loop-gain

$(1+ \beta A)$: is the amount of feedback

G : is the closed loop gain

There are four feedback topologies according to the type of input and output signals of the system: Shunt-Shunt, Series-Series, Shunt-Series, and Series-Shunt topology. Table 2 summarizes amplifier type, amplifier gain, feedback gain, input signal type, output signal type and the closed loop gain for each type for the four feedback topologies [8].

Table 2-2: The four feedback circuit topologies [9]

Feedback Topology	Input Connection	Output Connection	Input Signal	Output Signal	Amplifier Type	Amplifier Gain	Feedback Network Gain	Closed Loop Gain
Shunt-Shunt Feedback	Shunt	Shunt	Current	Voltage	Transimpedance amplifier	$A_\rho = \frac{V_{OUT}}{I_{IN}}$	$\beta_\sigma = \frac{I_{IN}}{V_{OUT}}$	$G = \frac{V_{OUT}}{I_{IN}}$ $= \frac{A_\rho}{1 + \beta_\sigma A_\rho}$
Series-Series Feedback	Series	Series	Voltage	Current	Transconductance amplifier	$A_\sigma = \frac{I_{OUT}}{V_{IN}}$	$\beta_\rho = \frac{V_{IN}}{I_{OUT}}$	$G = \frac{I_{OUT}}{V_{IN}}$ $= \frac{A_\sigma}{1 + \beta_\rho A_\sigma}$
Shunt-Series Feedback	Shunt	Series	Current	Current	Current amplifier	$A_I = \frac{I_{OUT}}{I_{IN}}$	$\beta_I = \frac{I_{IN}}{I_{OUT}}$	$G = \frac{I_{OUT}}{I_{IN}}$ $= \frac{A_I}{1 + \beta_I A_I}$
Series-Shunt Feedback	Series	Shunt	Voltage	Voltage	Voltage amplifier	$A_V = \frac{V_{OUT}}{V_{IN}}$	$\beta_V = \frac{V_{IN}}{V_{OUT}}$	$G = \frac{V_{OUT}}{V_{IN}}$ $= \frac{A_V}{1 + \beta_V A_V}$

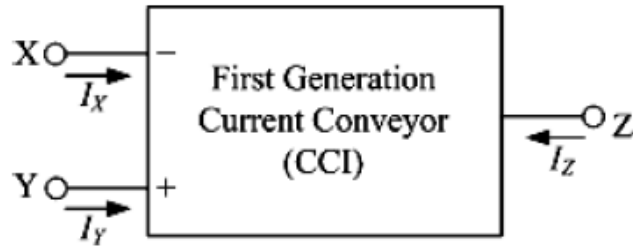


Figure 2-4: Block diagram of CCI [14]

The operation of the CCI can be described using the following operation matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2-2)$$

Wideband current measuring device and a negative impedance converter (NIC) were the first two applications using the CCI as a main block [14][15].

2.4.1.2 Second Generation Current Conveyor (CCII)

To improve the performance of the CCI, the second-generation current conveyor (CCII) was first introduced in [12][16]. It has two versions: the first one is the positive second generation current conveyor CCII+ which copies the current from a low output impedance node to a high output impedance node with the same phase and magnitude. The second one is the negative second generation current conveyor CCII- which also copies the current from low impedance to a high impedance node with the same magnitude but out of phase which is shown in Figure 2-5 [6].

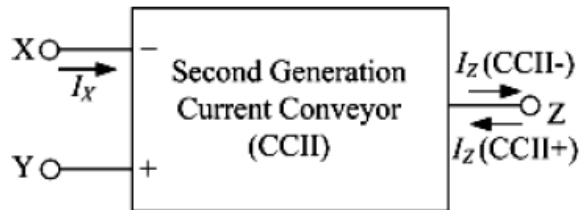


Figure 2-5: Block diagram of CCII [13]

The operation of the CCII can be described using the following operation matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2-3)$$

The input terminal Y has no input current which means that this terminal has high input impedance. The output current at terminal Z (I_Z) has the same magnitude as the input current at terminal X (I_X) but it could be either in phase (CCII+) or out of phase (CCII-) with I_X .

2.4.2 Current-Feedback Amplifier (CFA)

Based on the CCII+, the current feedback amplifier (CFA) was firstly invented by David Nelson. It was designed by using the same topology as a CCII followed by a buffer, as shown in Figure 2-6 [17]-[18].

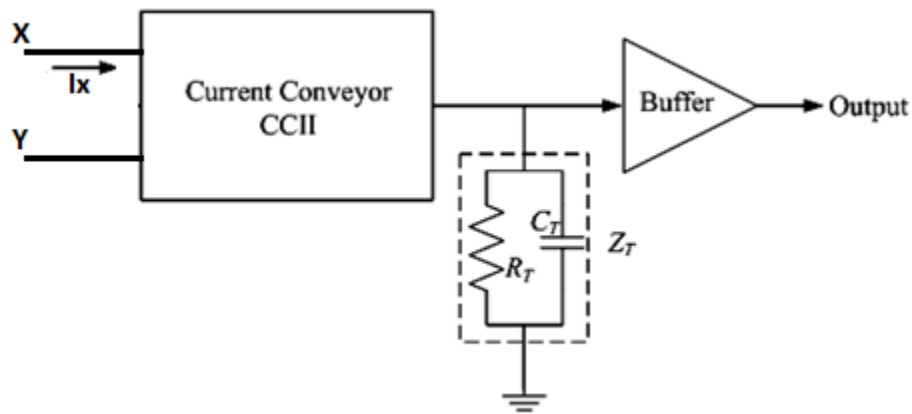


Figure 2-6: Block Diagram of CFA [17]

The CFA equivalent circuit is shown in Figure 2-7. It has two input terminals. The first input terminal is the inverting input terminal (X) with low input impedance ideally short circuit. The second input (Y) is the noninverting input terminal which has very high input impedance ideally open circuit.

The CFA circuit has a voltage-tracking action between its two input terminals X and Y. The buffer is used to model the voltage-tracking between the two input terminals of the CFA.

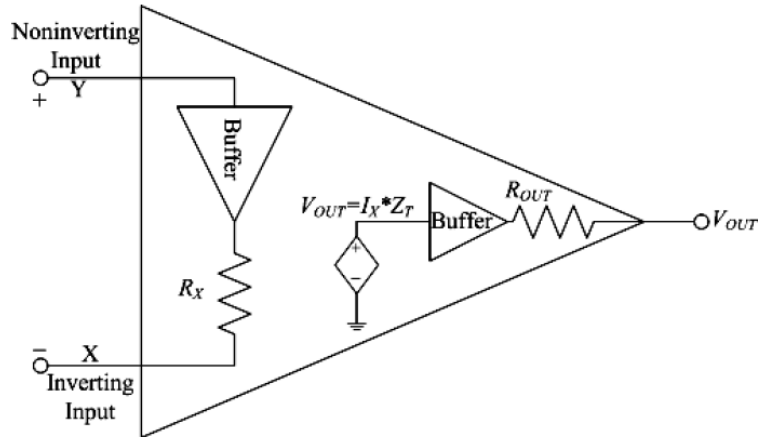


Figure 2-7: CFA equivalent circuit [19]

The output terminal V_{OUT} has very low output impedance ideally short circuit. The output voltage at this terminal is equal to the input current of the inverting terminal X times the total transimpedance of the current feedback amplifier Z_T .

The CFA circuit can only work in a closed-loop configuration. Also, the CFA circuit has an optimum feedback resistance which improves its stability and at the same time it has an effect on its bandwidth [20].

2.4.3 Operational Floating Conveyor (OFC)

As the CCII became part of the current-feedback amplifier circuit construction; the CFA became a part of the construction of other circuits as the operational floating conveyor (OFC) that was introduced by Toumazou, Payne, and Lidgey in 1991 as shown in Figure 2-8 [21].

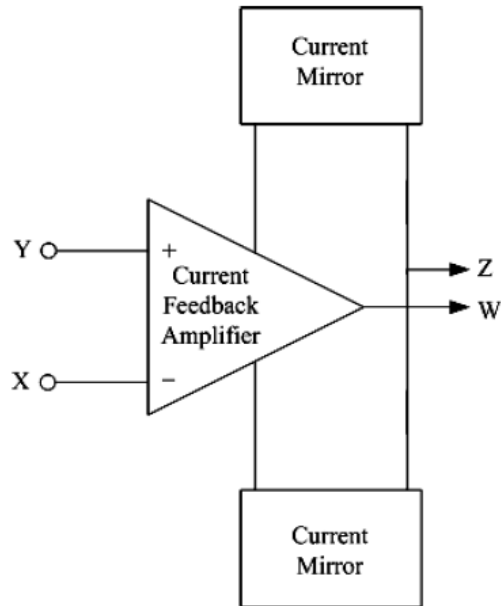


Figure 2-8: Block diagram of OFC using CFA and current mirror [22]

CFA circuit is the input stage of OFC circuit. The OFC circuit has two outputs; the first output terminal is the W terminal which is the output of the CFA. The second output terminal Z is the output of the current mirror circuit which has high output impedance. The current mirror controls the relation between the two output nodes which conveys the output current from node W to node Z. The basic difference between the OFC and CFA is the high output impedance at Z terminal which increases the OFC's versatility and enables accurate closed-loop current tracking.

To improve bandwidth and provide smaller power dissipation a new design was proposed [22]. Also, it has simpler block diagram as shown in Figure 2-9 which makes it easier to replace one block without much effect on the other blocks of the OFC realization. The first CCII+ is used to perform the voltage tracking at the input port between terminals Y and X. The second CCII+ is used to perform the required current tracking at the output port between terminals W and Z. To provide the output voltage at terminal W, the input current at terminal X is multiplied by the transimpedance amplifier gain.

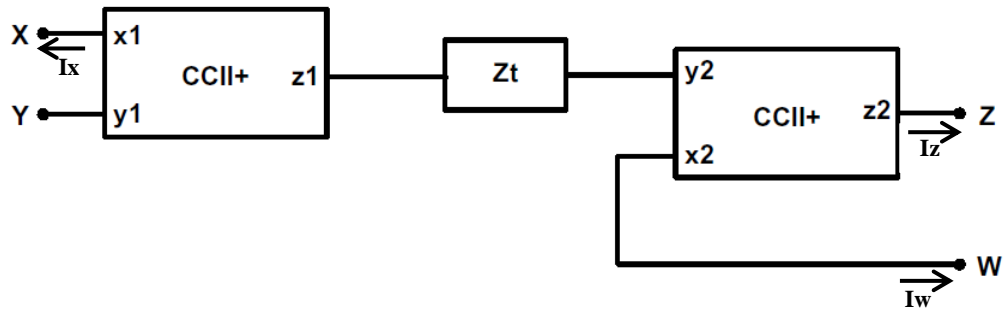


Figure 2-9: Block diagram of OFC using two CCII+ blocks and one noninverting [23]

The operation of the OFC can be described using the following operation matrix equation:

$$\begin{bmatrix} V_X \\ I_Y \\ V_W \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ Z_T & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ I_W \\ V_Z \end{bmatrix} \quad (2-4)$$

2.4.4 Operational Floating Current Conveyor (OFCC)

The Operational Floating Current Conveyor (OFCC) is a five-port general purpose analog building block. The transmission properties of OFCC are similar to OFC and CFA as they have very low input impedance compared to the current conveyor circuits, but OFCC has additional high output impedance terminal which makes the device having better flexibility than the CFA and OFC [7].

2.4.4.1 OFCC Characteristics

The OFCC has two input terminals X & Y and has three output terminals W, Z+ and Z- as shown in Figure 2-10 [23].

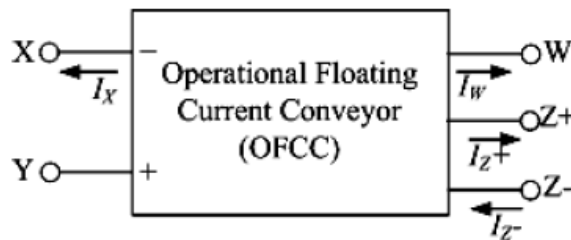


Figure 2-10: Block diagram of OFCC [23]

The first input terminal X is a low impedance current input terminal. The second input terminal Y is a high input impedance voltage input terminal, as the OFCC has a current feedback amplifier at its input stage. On the other hand, the W terminal is the output voltage terminal of the current feedback amplifier, and has low output impedance. Both Z+ and Z- are high impedance output current terminals. The Z+ terminal has an output current equal in phase and magnitude to the W terminal. The Z- terminal has an output current which has the same magnitude as the W terminal's current but is 180° out of phase.

2.4.4.2 OFCC Operation

There is an input current flowing at node X as it has very low input impedance (ideally zero). This current is multiplied by the open loop transimpedance gain (Z_T) to produce an output voltage at node W. There is a voltage tracking between the two input terminals (X and Y). The voltage at the high input impedance node Y appears at the second low input impedance node X.

The output terminal W has two kinds of output signals. The first output signal is the voltage which is equal to the input current of the input terminal X times the total transimpedance (Z_T) of the circuit. The second output signal of the W terminal is the current: it flows from this node W and depends on the load of the circuit. This current is conveyed to node Z+ with the same magnitude and phase and to Z- with the same magnitude but 180° out of phase.

To conclude, the OFCC has two types of tracking actions. The first one is the voltage tracking between the two input terminals X and Y of the OFCC. The second one is the current tracking between the output terminals W, Z+, and Z- of the OFCC.

The operation of the exact OFFC can be described using the following operation matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ V_W \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ h_v & 0 & 0 & 0 & 0 \\ 0 & -z_T & 0 & 0 & 0 \\ 0 & 0 & h_{i1} & 0 & 0 \\ 0 & 0 & -h_{i2} & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (2-5)$$

h_v is the voltage tracking and it is equal to $(1 - \epsilon_v)$, where ϵ_v is the voltage tracking error. Both h_{i1} and h_{i2} are the current tracking for both the Z+ and Z- terminals respectively. The coefficient h_{i1} is equal to $(1 - \epsilon_{i+})$ and h_{i2} is equal to $(1 - \epsilon_{i-})$, where ϵ_{i+} and ϵ_{i-} are the current tracking errors of the high output impedance terminals, Z+ and Z- respectively.

The operation of the ideal OFFC can be described using the following operation matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ V_W \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & -z_T & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (2-6)$$

2.5 Current Mode Devices vs. Voltage Mode Devices

Current mode and voltage mode devices each one of them have particular applications for which they are best matched. One of these applications is high speed application where the current mode devices are better due to the high slew rate capability of them.

An example of the current mode devices is the current feedback amplifier and an example of voltage mode devices is the voltage feedback amplifier. This section discusses the differences between them in two phases their closed loop characteristics & their open loop characteristics.

2.5.1 CFA and VFA in Closed Loop Configuration

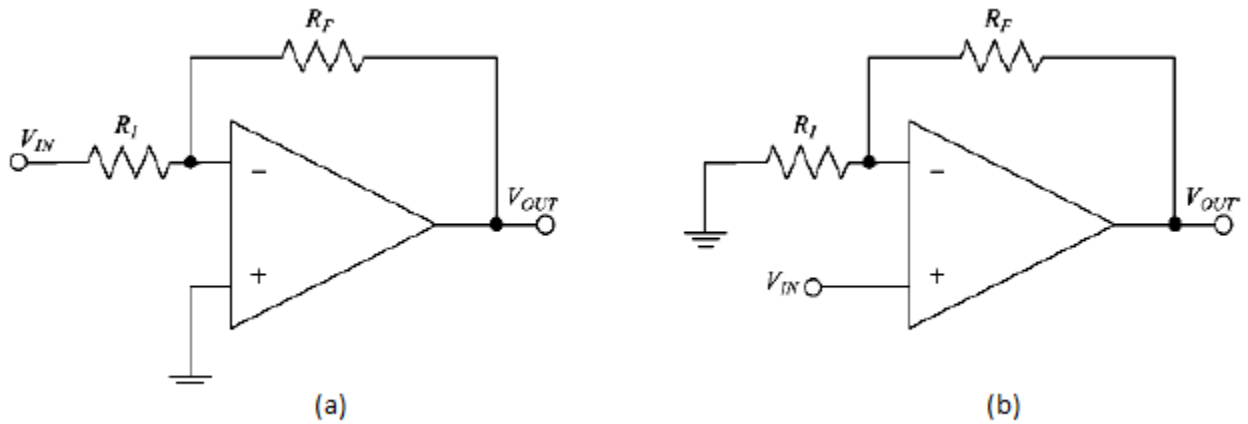


Figure 2-11: Feedback amplifier (a) Inverting configuration (b) Non-inverting configuration [24]

Table 2-3: The closed loop gain of both CFA and VFA circuits [24]

Amplifier type	Inverting closed loop	Non-inverting closed loop
VFA	$G_{ideal} = \frac{-R_F}{R_I}$	$G_{ideal} = 1 + \frac{R_F}{R_I}$
CFA	$G_{ideal} = \frac{-R_F}{R_I}$	$G_{ideal} = 1 + \frac{R_F}{R_I}$

The closed loop configuration of an amplifier can be either inverting or non-inverting as shown in Figure 2-11. The amplifiers have the same ideal closed loop gain regardless of whether CFA or VFA amplifiers are used [24].

2.5.2 CFA and VFA in Open Loop Configuration

The differences between CFA and VFA start to appear in the open loop configuration. The most important difference between the two amplifiers is the gain-bandwidth product (GBP).

2.5.2.1 Gain-bandwidth product (GBP) of CFA and VFA

I. Gain bandwidth product of VFA

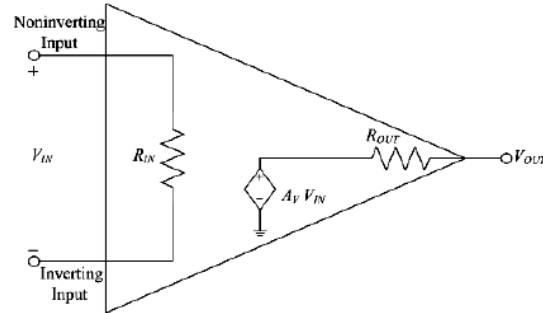


Figure 2-12: VFA equivalent circuit [24]

The equivalent circuit of the open loop voltage feedback amplifier is shown in Figure 2-12 [24]; its ideal circuit characteristics are infinite non-inverting and inverting input impedances, Zero output impedance and infinite open loop gain.

Taking into consideration the non-ideal characteristics of the VFA, the non-inverting closed loop gain for the voltage feedback amplifier shown in Figure 2-11 (b) is [24]:

$$G_{exact} = \frac{V_{OUT}}{V_{IN}} = \frac{G_{ideal}}{1 + \frac{G_{ideal}}{A_v(s)}} \quad (2-7)$$

G_{exact} : is the closed loop gain of the actual VFA.

G_{ideal} : is the closed loop gain of ideal amplifier.

$A_v(s)$: is the dominant pole open loop voltage gain of the VFA.

Due to the Miller effect the open loop gain is decreased with increasing frequency in VFA. Figure 2-13 shows the open loop gain of VFA gain versus the frequency [24]. The open loop gain is approximated by a single pole frequency dependent function. The closed loop gain is inversely proportional with the bandwidth of the amplifier circuit which means that when the closed loop gain increases the bandwidth of the amplifier decreases and vice versa. This is known as a constant gain bandwidth product in VFA circuits.

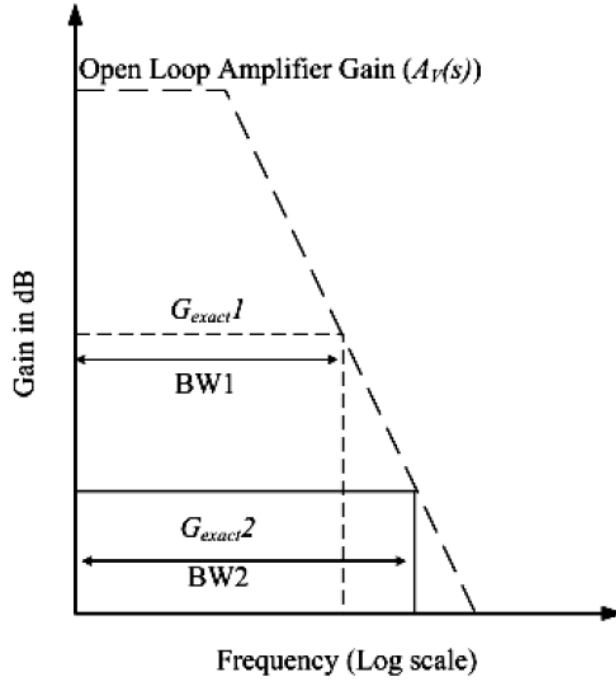


Figure 2-13: VFA gain vs. Frequency [24]

II. Gain Bandwidth Product of CFA

By referring to the open loop characteristics of the CFA in section 2.4.2 and taking into consideration the non-ideal characteristics of the CFA, the non-inverting closed loop gain for the current feedback amplifier shown in Figure 2-11 (b) is [24]:

$$G_{exact} = \frac{V_{OUT}}{V_{IN}} = \frac{G_{ideal}}{1 + \frac{R_F}{Z_T(s)}} \quad (2-8)$$

G_{exact} : is the closed loop gain of the exact CFA.

G_{ideal} : is the closed loop gain for ideal CFA.

$Z_T(s)$: is the single pole frequency dependent open loop transimpedance.

R_F : is the feedback resistor for CFA.

The Miller effect decreases the open loop gain for the voltage mode amplifier. The absence of the Miller effect in CFA circuit enables the CFA frequency response to have a dominant pole frequency higher than the dominant pole in the case of the VFA.

The open loop transimpedance gain of the amplifier $Z_T(s)$ is shown in Figure 2-14 [24]. The bandwidth in case of the open loop current amplifier circuit is wider than that of the open loop voltage amplifier circuit. The CFA circuit will have a variable gain bandwidth product as increasing or decreasing the closed loop gain won't affect the circuit bandwidth.

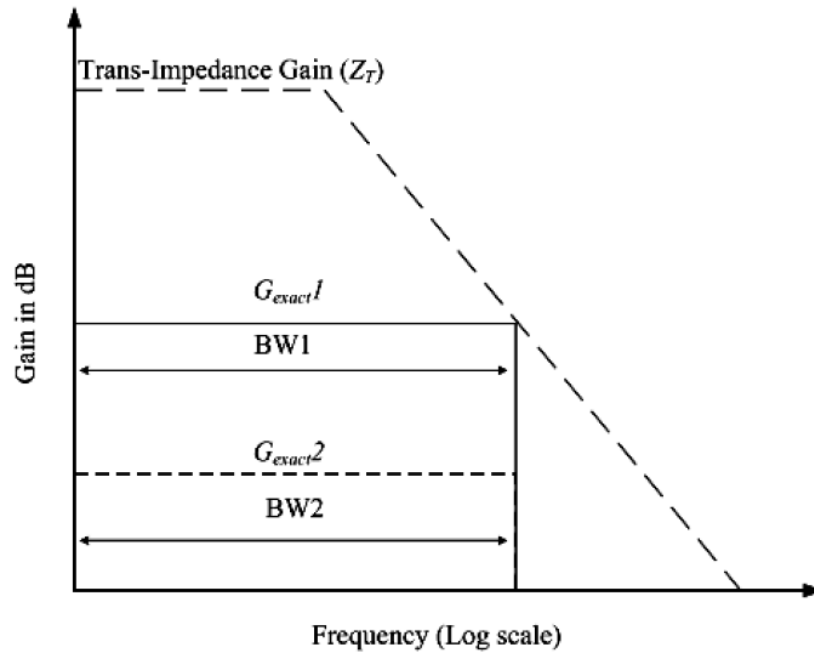


Figure 2-14: CFA gain vs. Frequency [24]

2.5.2.2 Bandwidth in VFA and CFA Circuits

The common topology of the CFA requires less gain stages than the VFA; this means less delay through the open-loop circuit which leads to higher bandwidth with the same power.

2.5.2.3 DC Characteristics of VFA and CFA Circuits

The input stage of the VFA is a differential amplifier and has four main advantages in terms of battery operation. Firstly, it has low input offset voltage (V_{IO}). Secondly, it has matched input bias currents (I_B). Thirdly, it has high power supply rejection ratio (PSRR). Finally, it has good common mode rejection ratio (CMRR).

The input stage of the most common realization circuit of the CFA is a class AB buffer as shown in Figure 2-15 which has nonzero V_{IO} and unmatched I_B [24].

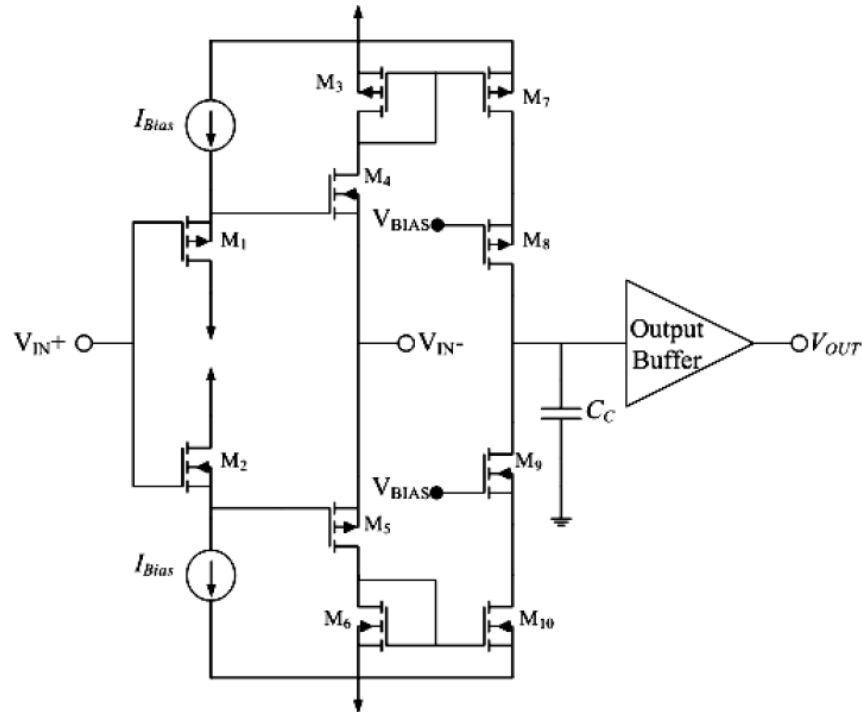


Figure 2-15: Basic CFA circuit [24]

2.5.2.4 Distortion in VFA and CFA Circuits

The overall distortion of the amplifier circuit is affected by the open loop distortion and the loop gain of the amplifier. The loop gain of the CFA circuit is much higher than that of VFA circuit, so the CFA tends to lead the VFA circuit. In the internal structure of the basic CFA circuit, as shown in Figure 2-15, each n-channel transistor has a corresponding p-channel transistor which is not the case in VFA circuits. This leads to having a low level of open loop distortion [24].

2.5.2.5 Slew Rate

For CFA that is shown in Figure 2-15, the compensation capacitor (C_C) charged and discharged by current which can be fed by both transistors M7 and M10. There is no limit (ideally) to the slew rate of the CFA as this current is a dynamic current.

For VFA that is shown in Figure 2-16 , it can be shown that the maximum current is bias current (I_{DC}) with which the C_C can be charged or discharged [24].

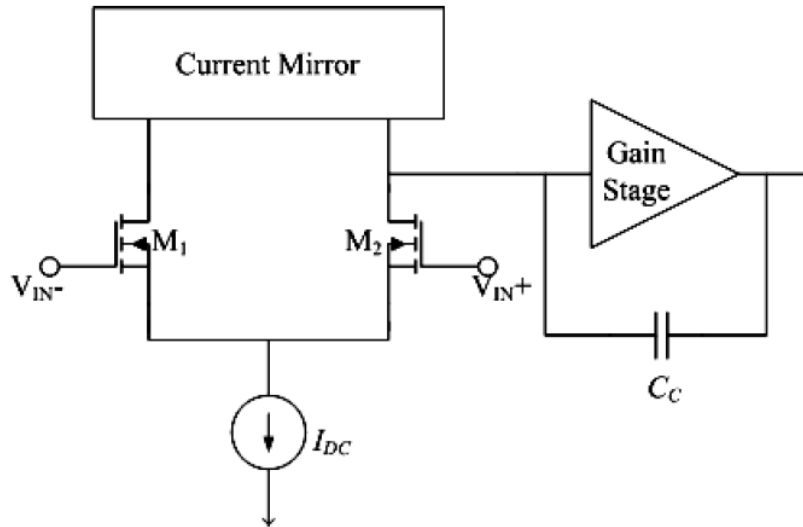


Figure 2-16: Basic VFA circuit [24]

2.6 Noise in Amplifier Circuits

Noise in electronic circuits is a random signal. Noise sources can only be described by a probability density function (the most common probability density function is Gaussian,[25]) as they have amplitudes that vary randomly with time, so it is normally specified in root mean square value (RMS).

Noise can either be superimposed on the circuit by external sources or generated internally in the amplifier, from its associated passive components.

There are different types of noise in electronic circuits such as thermal noise, flicker noise, avalanche noise, burst noise, generation-recombination noise and shot noise. Thermal noise is the most effective noise parameter in the CMOS electronic circuits as it dominates noise's value presented in the CMOS electronic circuit [26].

The input noise voltage (e_n) source for CMOS differential amplifier circuits dominates the noise effect as the input terminals have true high input impedances (gate terminal of the MOSFETs). The noise model in this case can be expressed by only one

voltage source at the noninverting input terminal of the amplifier as shown in Figure 2-17 [25].

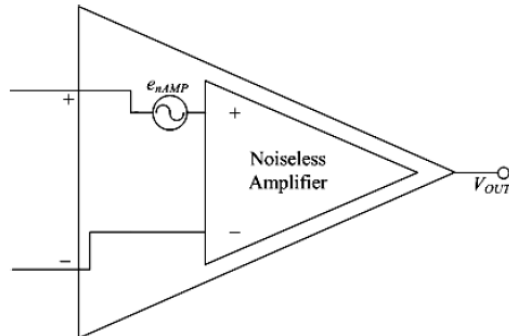


Figure 2-17: Noise model of CMOS amplifier circuit [25]

2.7 Conclusion

The OFCC circuit is a promising current mode device as it combines the entire current mode device features. Both the current mode and voltage mode devices have the same closed loop gain in the ideal case, but they have different open loop characteristics.

CFA have the following advantages compared to VFA:

- Overcome the gain dependent bandwidth limitation.
- Wider bandwidth.
- Higher gain.
- Higher slew rate.

Chapter 3: Proposed OFCC circuit

3.1 Introduction

In this chapter, a novel integrated CMOS based operational floating current conveyor (OFCC) is presented. The proposed OFCC is implemented in two stages. The first stage is an OFC and the second one is a current steering circuit.

3.2 Proposed Operational Floating Conveyor (OFC)

As described in chapter 2, there are two topologies that can be used in designing an operational floating conveyor. The first topology uses CFA circuit as a main part of the OFC circuit followed by a current mirror circuit as shown in Figure 2-8. The second one uses two CCII+ blocks, one noninverting transimpedance amplifier as shown in Figure 2-9. The second topology is the one that is used as the first stage in the proposed OFCC.

The proposed OFC circuit is shown in Figure 3-1. The first CCII+ (M1- M7) is used to perform the required voltage tracking action at the input port between terminals X and Y. In order to provide the output voltage at terminal W, the input current at terminal X is multiplied by the transimpedance amplifier gain Z_T (M8- M13). The transimpedance amplifier is working as follows; The input current at terminal X is mirrored by transistors M3, M4, M6 and M7 and the mirrored current will flow in the equivalent parasitic impedance of the gate terminal of M8, producing a voltage on it. This voltage is then amplified to produce the output voltage at terminal W. To perform the current following action at the output port between terminals W and Z, the second CCII+ (M14-M20) is used [22].

Taking into consideration the finite value of the transistor transconductance g_m and drain to source conductance g_d and replacing each transistor by its small signal equivalent circuit, the small signal voltage transfer gain from the Y terminal to the X terminal is [22]:

$$A_v = \frac{v_x}{v_y} = \frac{g_{m1}}{g_{m1} + g_{d1} + \frac{g_{d3}(g_{d1} + 2g_{d5})}{(g_{d5} + g_{m3})}} \quad (3-1)$$

The small signal input resistance seen at terminal X is [22]:

$$r_x = \frac{(g_{d1} + 2g_{d5})}{(g_{m1} + g_{d1})(g_{m3} + g_{d5}) + g_{d3}(g_{d1} + 2g_{d5})} \quad (3-2)$$

The small signal open loop transimpedance gain Z_t is [22]:

$$Z_t = \frac{g_{m12}g_{m13}g_{m14}}{(g_{d4} + g_{d7})(g_{d12} + g_{d10})(g_{m11} + g_{d13})(g_{m14} + g_{d14} + \frac{g_{d16}(g_{d14} + 2g_{d18})}{(g_{d18} + g_{m16})})} \quad (3-3)$$

The output resistance at terminal Z is [22]:

$$r_z = \frac{1}{g_{d17} + g_{d20}} \quad (3-4)$$

3.3 Proposed Design of OFCC

OFCC consists of an OFC as a first stage and a current steering circuit as a second stage. The current steering circuit (M21-M24) is used to change the phase of the mirrored current by 180°. The steered current is mirrored by transistors M25 and M26 to produce I_z as shown in Figure 3-2.

The circuit is designed and simulated using UMC 130nm CMOS technology kit in Cadence. The DC power supply used is 1.2V. The bias voltages VB1 and VB2 are equal 800mV and 380mV respectively. Design parameters of the transistors are reported in Table 3-1. The transistor aspect ratios (W/L) are in ($\mu\text{m}/\mu\text{m}$).

Table 3-1: Transistors aspect ratios

Transistor	W/ L
M1, M2	4/0.46
M3, M4, M11, M12	12.5/0.5
M14, M15	10/0.25
M16	30/0.12
M17	30/0.14
M5, M7, M10, M18	34.4/0.67
M20	10/0.12
M6, M8, M19	30/0.43
M9, M13	28/0.5
M21	30/0.14
M22, M23, M24	60/0.25
M25	160/0.35
M26	80/0.35

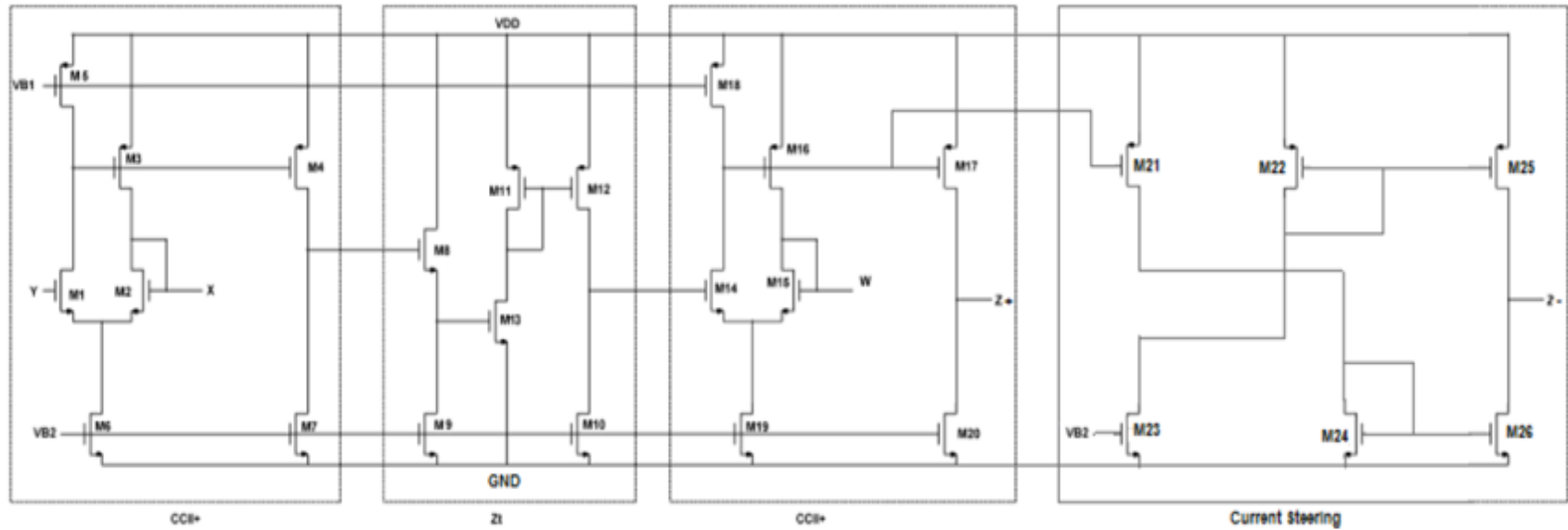


Figure 3-2: Proposed OFCC circuit schematic

3.4 Simulation Results

The proposed circuit shown in Figure 3-2 is simulated using UMC 130nm CMOS technology kit in Cadence. The supply voltage of the proposed OFCC is 1.2V. The voltage tracking between X and Y terminals is presented in Figure 3-3. There is 0.4% error.

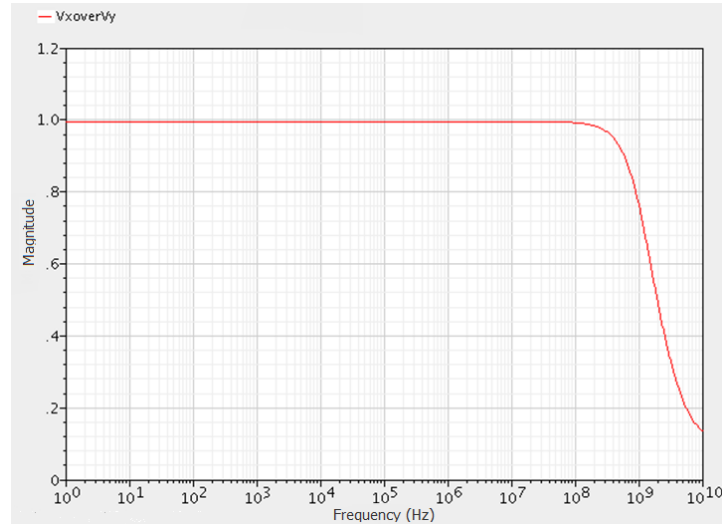


Figure 3-3: Input terminals voltage tracking V_x/V_y

The input resistance at terminal X is presented in Figure 3-4. It is equal 8.83Ω .

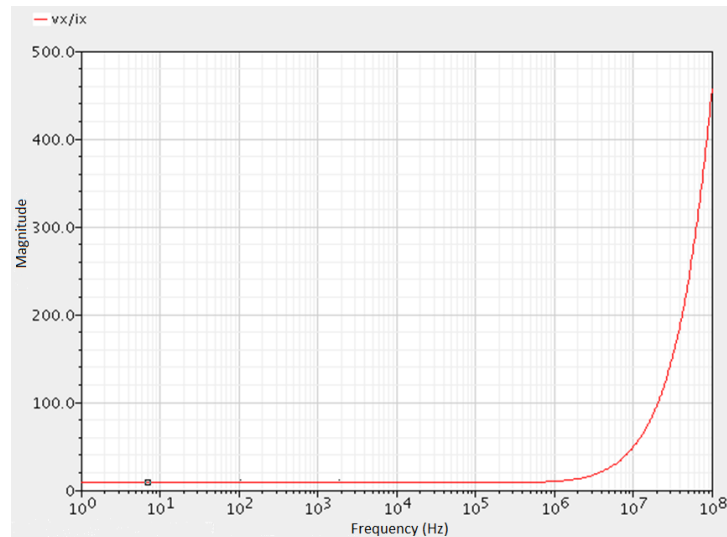


Figure 3-4: Input resistance r_x

The input resistance at terminal Y is presented in Figure 3-5. It is equal $30.8E12\Omega$.

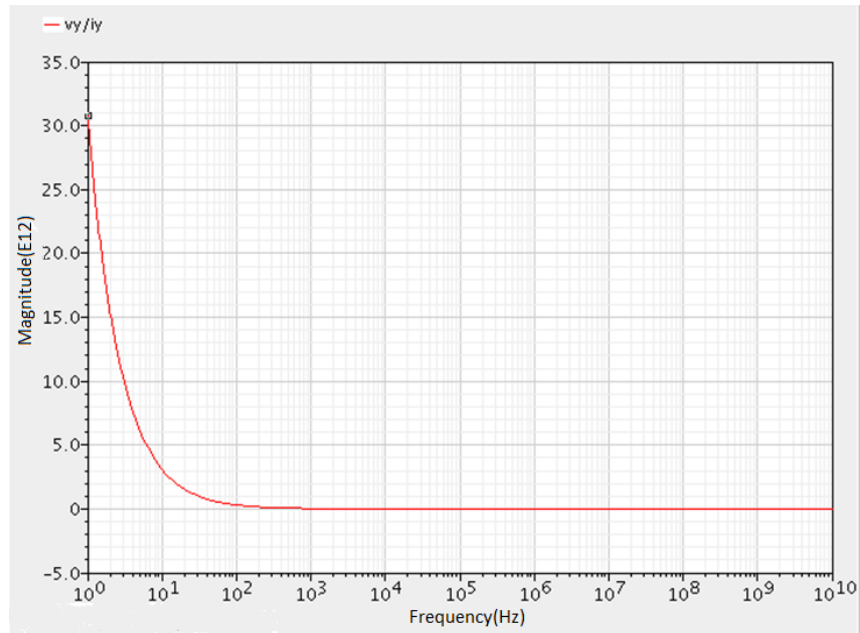


Figure 3-5: Input resistance r_Y

The frequency characteristics of the open loop transimpedance between X and W (V_w/I_x) is presented in Figure 3-6. It is equal $3.94K\Omega$.

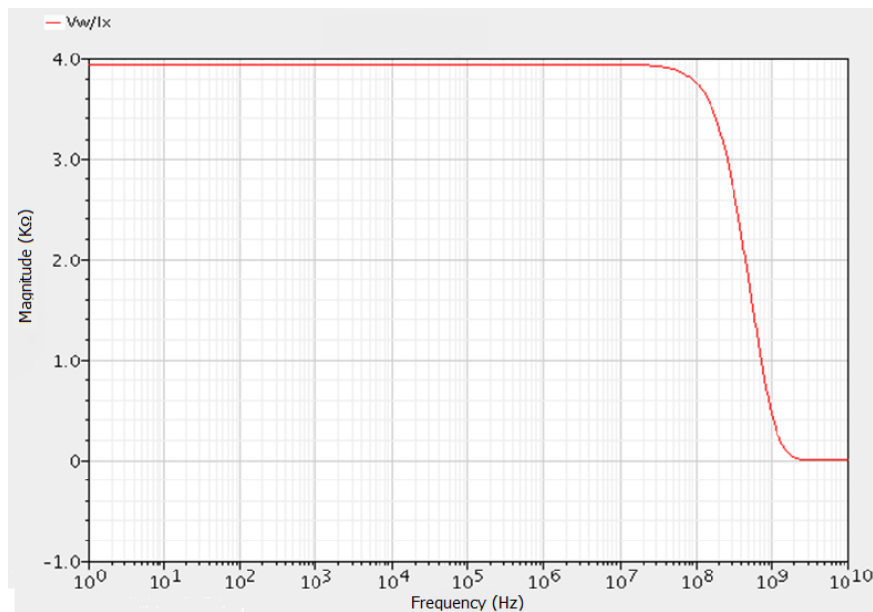


Figure 3-6: Open loop transimpedance Z_T

The output terminals current tracking I_{z+}/I_w and I_{z-}/I_w are presented in Figure 3-7 and Figure 3-8 respectively. There is 0.5% and 0.8% error respectively.

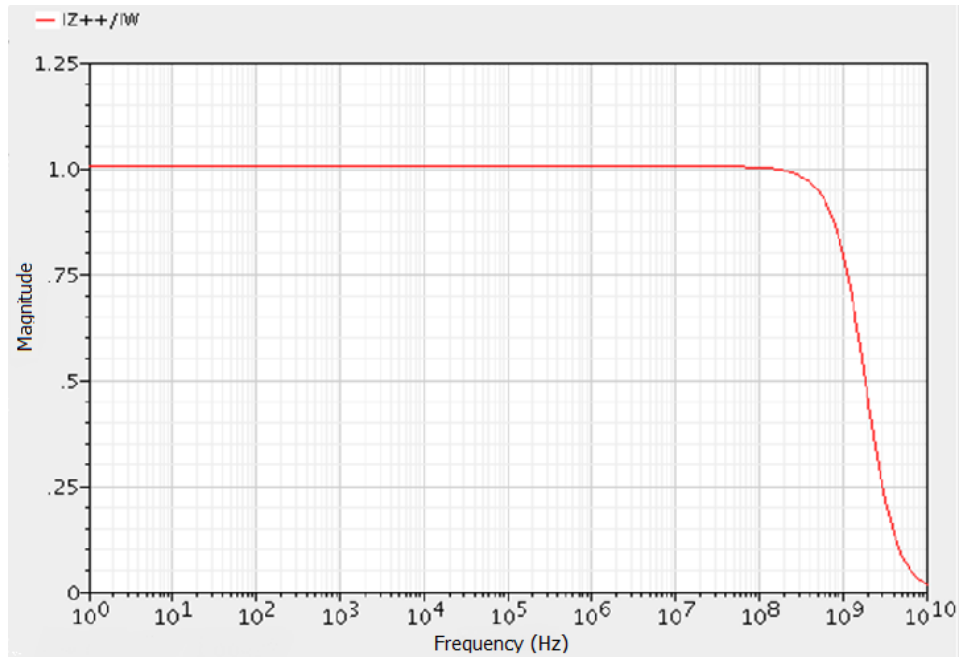


Figure 3-7: Output terminals current tracking I_{z+}/I_w

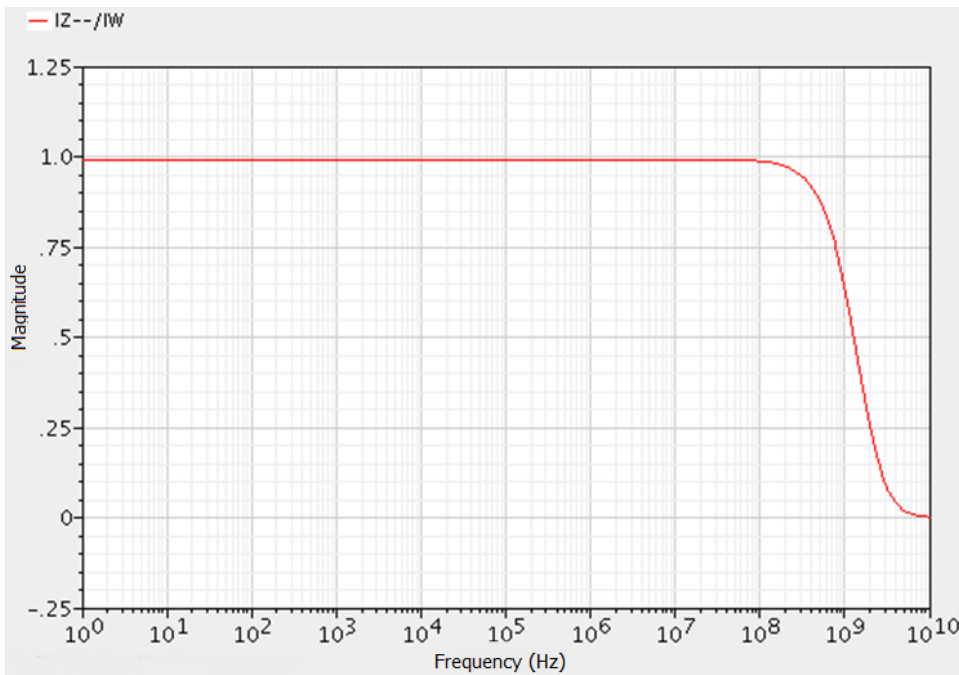


Figure 3-8: Output terminals current tracking I_{z-}/I_w

Table 3-2 shows a performance comparison between the proposed and currently used OFCC and OFC. The proposed design of the CMOS based OFCC circuit has the lowest internal resistance which is equal to 8.83Ω compared to the other two designs. Also the proposed design has the highest 3dB frequency (bandwidth) which increased by 97.5% and 30.2% compared to others [6][22] respectively. OFC circuit [22] is the highest DC open loop transimpedance gain which is equal to $29.6K\Omega$, the proposed design is higher than the OFCC circuit presented in [6] by $0.94K\Omega$. The power consumption in the proposed design is equal to $1.5mW$ which is higher than [6] by $0.4mW$. However, OFCC presented in [6] is designed based on 90nm CMOS technology. The proposed design has a lower power consumption compared to [22] by about $0.9mW$.

Table 3-2: Comparison between the proposed and other OFCC & OFC circuits

OFC & OFCC Reference	Proposed	[6]	[22]
Technology	130nm	90nm	500nm
Supply (V)	+1.2	+1.2	± 1.5
Input voltage dynamic range (V)	0.5 to 0.9	0 to 0.8	-0.4 to 1.2
Input resistance $r_x(\Omega)$	8.83	20	30.2
-3dB frequency (Bandwidth)	1.2GHz	30MHz	826MHz
DC open loop transimpedance (kΩ)	3.94	3	29.6
Power Consumption (mW)	1.5	1.1	2.4

Chapter 4: Applications based on OFCC

4.1 Introduction

OFCC is a versatile analog device as both its input and output ports are floating. It is designed to be used in a closed loop implementation with current feedback from terminal W to terminal X. There are many applications that can be designed in a closed loop such as: inverting voltage amplifier, non-inverting voltage amplifier, transresistance amplifier, transconductance amplifier, current mode instrumentation amplifier (CMIA) and universal filter. This chapter discusses only four applications based on OFCC, non-inverting voltage amplifier, CMIA, universal filter and electrocardiogram (ECG).

4.2 Non-inverting voltage amplifier

The non-inverting voltage amplifier is a voltage controlled voltage source (VCVS) and is shown in Figure 4-1 [22].

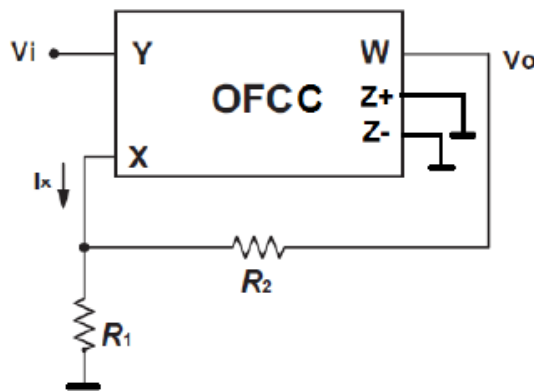


Figure 4-1: Non-inverting voltage amplifier configuration [22]

The voltage gain can be expressed as follows:

$$A_v = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1} \quad (4-1)$$

The single pole model transimpedance gain by taking the effect of the finite transimpedance gain, Z_t , and using the finite transimpedance single pole model can be expressed as:

$$\mathbf{Z}_t(\mathbf{s}) = \frac{\mathbf{Z}_{to}}{1 + \frac{\mathbf{s}}{w_o}} \quad (4-2)$$

Z_{to} : DC open loop transimpedance gain

w_o : transimpedance cutoff frequency

The transimpedance gain $Z_t(s)$ for high frequency applications:

$$\mathbf{Z}_t(\mathbf{s}) = \frac{1}{\mathbf{s}C_p} \quad (4-3)$$

$$\mathbf{C}_p = \frac{1}{\mathbf{Z}_{to}w_o} \quad (4-4)$$

Applying KCL at terminal X:

$$\mathbf{I}_x = \frac{\mathbf{V}_i - \mathbf{V}_o}{\mathbf{R}_2} + \frac{\mathbf{V}_i}{\mathbf{R}_1} \quad (4-5)$$

Substituting by $I_x = V_o/Z_t$ in eq. (4-5), the non-inverting voltage amplifier gain is given by:

$$\mathbf{A}_v = \frac{\mathbf{V}_o}{\mathbf{V}_i} = \left(\mathbf{1} + \frac{\mathbf{R}_2}{\mathbf{R}_1} \right) \frac{1}{1 + \frac{\mathbf{R}_2}{\mathbf{Z}_t(\mathbf{s})}} = \left(\mathbf{1} + \frac{\mathbf{R}_2}{\mathbf{R}_1} \right) \boldsymbol{\varepsilon}(\mathbf{s}) \quad (4-6)$$

$\varepsilon(s)$: the error function

$$\boldsymbol{\varepsilon}(\mathbf{s}) = \frac{1}{1 + \frac{\mathbf{R}_2}{\mathbf{Z}_t(\mathbf{s})}} \quad (4-7)$$

By substituting from eq. (4-3) into eq. (4-7), the error function will be reduced to:

$$\boldsymbol{\varepsilon}(\mathbf{s}) = \frac{1}{1 + \mathbf{s}R_2C_p} \quad (4-8)$$

The circuit is simulated using UMC 130nm technology kit in Cadence. $R_1=10K$ and $R_2= 5K, 90K$ and $200K$. The different gains of the differential voltage amplifier are shown in Figure 4-2. For $R_2= 5K, 90K$ and $200K$ the gain has an error equal to 0.67%, 0.3% and 0.4% respectively.

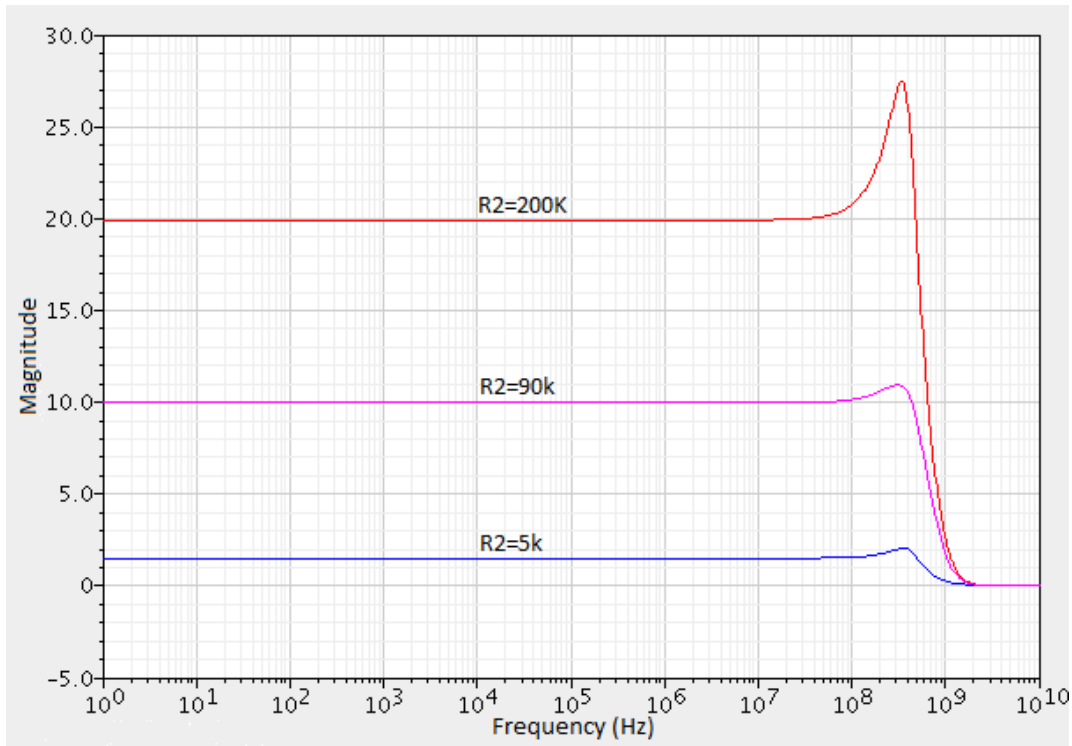


Figure 4-2: Frequency characteristics of the voltage gain of the non-inverting voltage amplifier

4.3 Current mode instrumentation amplifier

Instrumentation amplifiers are very important as they are used in many fields, such as medical instrumentation, the read-out circuit of biosensors, signal processing and data acquisition. One of the most important areas is the lab-on-a-chip, which requires the integration of the actuation and sensing parts, as well as the read-out circuit in a single chip. Lab-on-a-chip needs a wide bandwidth instrumentation amplifier to suppress any unwanted common-mode signal and amplify the differential signals [27].

There are two types of instrumentation amplifiers, they are the conventional voltage-mode instrumentation amplifiers (VMIA) based on a voltage operational amplifier and current-mode instrumentation amplifiers (CMIA) based on a current operational amplifier. As a result of the fixed gain bandwidth product of the operational amplifier, VMIA have narrow bandwidth that is highly dependent on the gain. They need precise resistor matching to attain high common-mode rejection ratio (CMRR) [28–30].

On the other hand, CMIA have better performance and wider frequency range of operation compared to VMIA. CMIA also do not require matched resistors [31]. Second-generation current conveyor (CCII) was used before in CMIA.

4.3.1 Designing using two CCII+

CMIA were designed using two CCII+ [32] as shown in Figure 4-3. This two CCII+ topology introduces a simple and symmetric circuit topology, and has a high CMRR without requiring matched resistors.

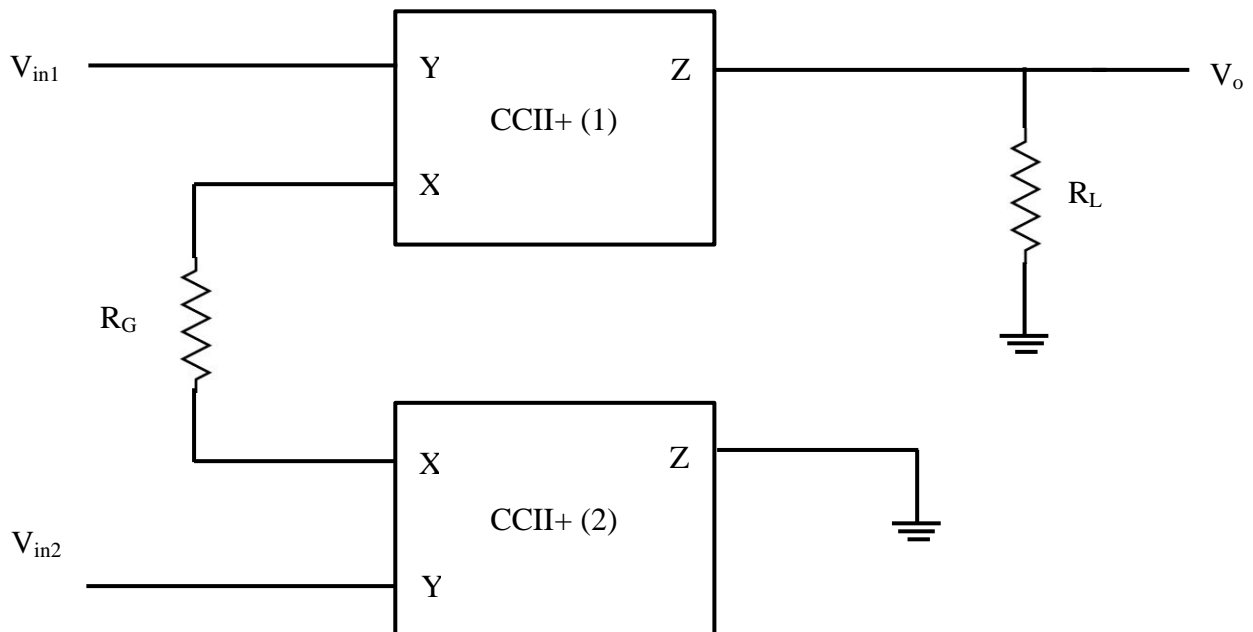


Figure 4-3: Two CCII+ CMIA [32]

The frequency dependent differential gain can be expressed as follows [32]:

$$A_d(s) = \frac{v_o}{v_{in1}-v_{in2}} = \frac{R_L}{R_G+2R_X} \cdot \frac{1}{1+sCR_L} \quad (4-9)$$

R_X : the equivalent input resistance at the X terminal

R_G : the gain setting resistor

C : the effective output capacitance of the CCII+

R_L : the load resistor

4.3.2 Designing using three CCII+

CMIA's were designed using three CCII+ [33] as shown in Figure 4-4. Comparing to the two CCII+ approach higher CMRR and higher differential gain will be reached using the three CCII+ approach.

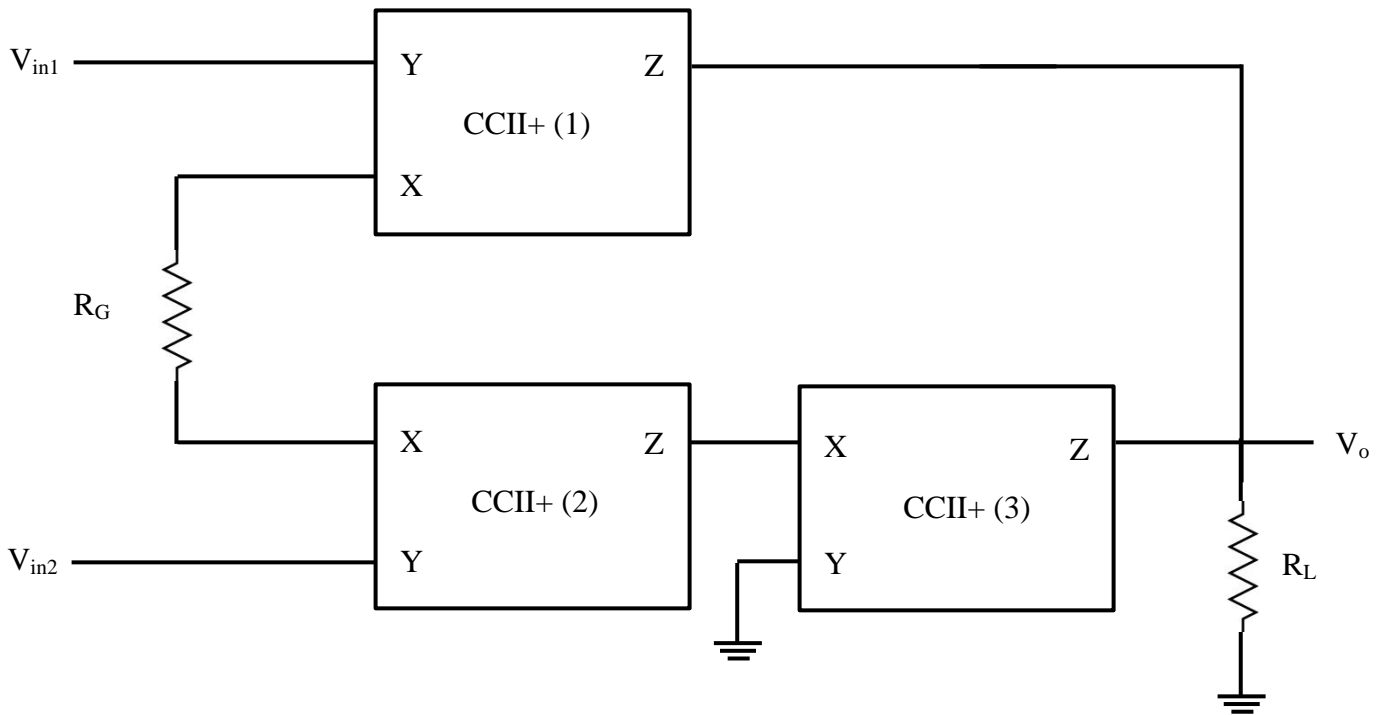


Figure 4-4: Three CCII+ CMIA [33]

The differential gain can be computed as follows [33]:

$$A_d(s) = \frac{v_o}{v_{in1}-v_{in2}} = \frac{2R_L}{R_G+2R_X} \cdot \frac{1}{1+sCR_L} \quad (4-10)$$

As shown in (4-9) and (4-10) the differential gain of both designs is inversely proportional to R_X and the accuracy is limited by the tolerance of R_X , which is low. To improve the accuracy of the CMIA, two op-amps working in conjunction with two CCII+ [34] are used.

4.3.3 Designing using two op-amps working in conjunction with two CCII+

Figure 4-5 shows CMIA that was designed using two op-amps working in conjunction with two CCII+.

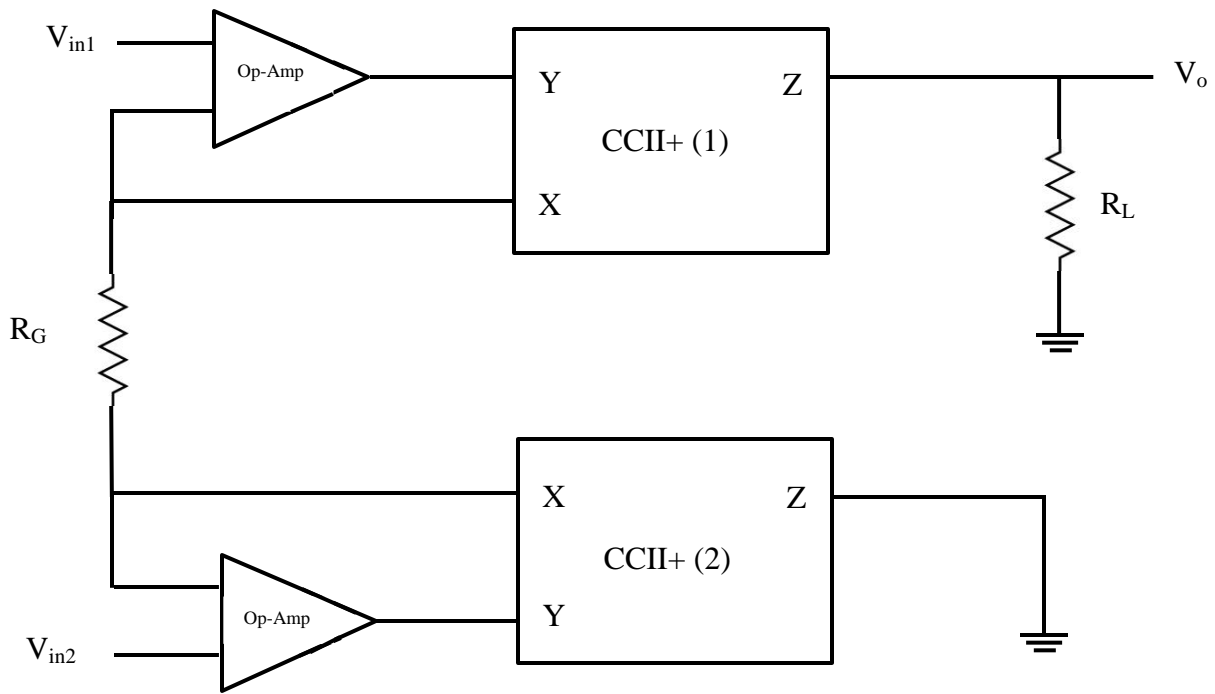


Figure 4-5: Two CCII+ used in conjunction with two Op-amp CMIA [36]

The differential gain of this CMIA is given as follows [34]:

$$A_d(s) = \frac{v_o}{v_{in1} - v_{in2}} = \frac{R_L}{R_G} \cdot \frac{1}{1 + \frac{s\tau}{1 + K\beta}} \quad (4-11)$$

$$\beta = R_G / (2R_X + R_G)$$

R_L : the load resistance

τ : the time constant of the op-amp

K : the low-frequency gain of the op-amp

As shown in (4-11), the low-frequency gain is independent of R_X , however the bandwidth is dependent on R_X . This approach suffers from higher power consumption and a more complicated circuit topology when compared with the topologies shown in Figure 4-3 and Figure 4-4. On the other hand, it has a more accurate low-frequency differential gain than the two CCII+ based CMIA.

4.3.4 Proposed integrated CMOS based CMIA

The proposed CMIA circuit is based on operational floating current conveyor (OFCC), which has flexible characteristics with respect to other current-mode or voltage mode devices [35]. It consists of two OFCCs, two feedback resistors (R_{W1} and R_{W2}), a gain-determined resistor (R_G), and a ground load (R_L), as shown in Figure 4-6.

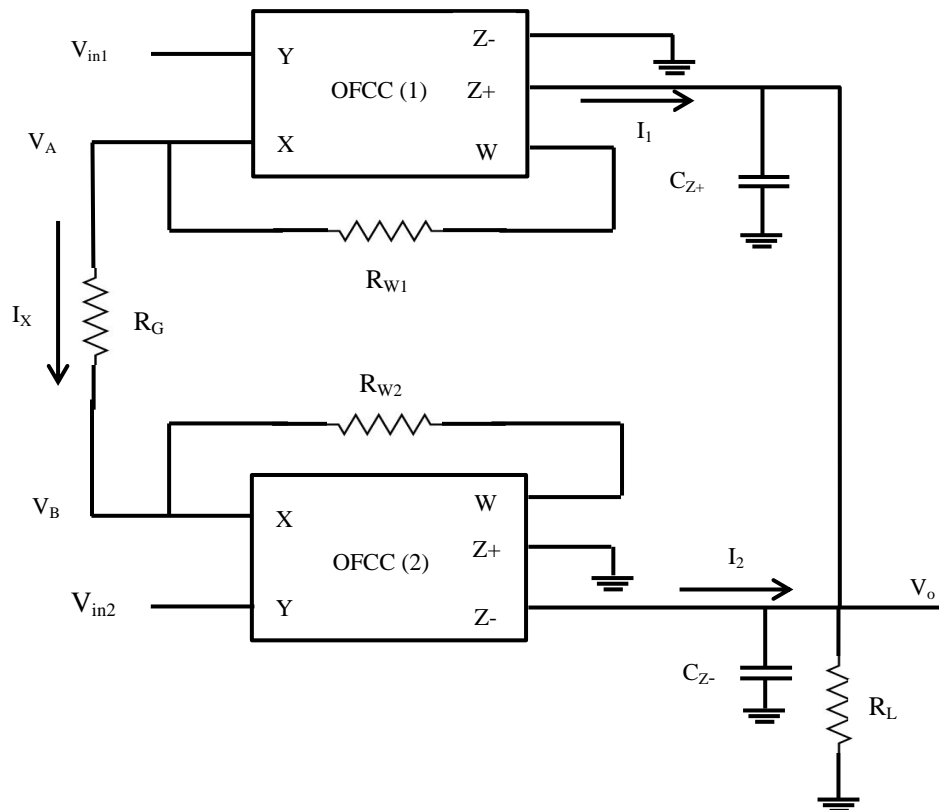


Figure 4-6: Proposed CMIA circuit [35]

The negative feedback resistor between W and X allows the OFCC to operate at a positive or negative current-conveyor while simultaneously reducing the input resistance at X port [36]. Also, the dc stability as well as the transfer function accuracy is improved due to the negative feedback [31][34].

Taking into consideration both the voltage and current tracking errors of the OFCC, the current tracking error between ports X, Z+, and Z- is [37]:

$$\alpha = 1 - \varepsilon_+ \quad (4-12)$$

$$\gamma = 1 - \varepsilon_- \quad (4-13)$$

ε_+ : the finite current tracking error at the high impedance output Z+

ε_- : the finite current tracking error at the high impedance output Z-

The port currents can be given as [37]:

$$i_{z+} = \alpha i_x \quad (4-14)$$

$$i_{z-} = \gamma i_x \quad (4-15)$$

The voltage tracking error between ports X and Y [37]:

$$\beta = 1 - \varepsilon_V \quad (4-16)$$

ε_V : the finite voltage tracking error at the low impedance X from the high input impedance node Y.

The voltage at nodes v_A and v_B can be given as [37]:

$$v_A = \beta_1 v_{in1} \quad (4-17)$$

$$v_B = \beta_2 v_{in2} \quad (4-18)$$

The resulting current i_x [37]:

$$i_x = \frac{v_A - v_B}{R_G} \quad (4-19)$$

$$i_x = \frac{(\beta_1 v_{in1} - \beta_2 v_{in2})}{R_G} \quad (4-20)$$

The output terminals currents [37]:

$$i_1 = \alpha_1 i_x = \frac{\alpha_1 (\beta_1 v_{in1} - \beta_2 v_{in2})}{R_G} \quad (4-21)$$

$$i_2 = \gamma_2 i_x = \frac{\gamma_2 (\beta_1 v_{in1} - \beta_2 v_{in2})}{R_G} \quad (4-22)$$

The output voltage [37]:

$$v_o(s) = (i_1 + i_2) \left(R_L // \frac{1}{sC_Z} \right) \quad (4-23)$$

and

$$C_Z = C_{Z+} + C_{Z-} \quad (4-24)$$

then,

$$v_o(s) = \frac{(\beta_1 v_{in1} - \beta_2 v_{in2})(\alpha_1 + \gamma_2) R_L}{R_G(1 + sC_Z R_L)} \quad (4-25)$$

When $V_{in1} = V_{in2} = V_{cm}$, the common-mode gain is equal [37]:

$$A_{CM}(S) = \frac{v_o}{v_{cm}} = \frac{(\beta_1 - \beta_2)(\alpha_1 + \gamma_2) R_L}{R_G(1 + sC_Z R_L)} \quad (4-26)$$

For ideal OFCCs,

$$\alpha_1 = \alpha_2 = \gamma_1 = \gamma_2 = \beta_1 = \beta_2 = 1$$

Then, the output voltage [37]:

$$v_o(s) = \frac{2R_L(v_{in1} - v_{in2})}{R_G(1 + sC_Z R_L)} \quad (4-27)$$

The output differential gain [37]:

$$A_d(s) = \frac{v_o}{v_{in1} - v_{in2}} = \frac{2R_L}{R_G(1 + sC_zR_L)} \quad (4-28)$$

From (4-28), it's clear that the differential gain can be adjusted and controlled by R_G without affecting the bandwidth of the CMIA.

4.3.5 Simulation Results

The circuit is designed and simulated using UMC 130nm technology kit in Cadence. The DC power supply used is 1.2 Volt.

A. Differential Gain Measurements

To measure the differential gain of the proposed CMIA, we connected the input voltage to V_{in1} and connected V_{in2} to ground. Resistors R_{W1} and R_{W2} were set to 6.5K, R_L was set to 1K and R_G was tested at different values. Figure 4-7 shows the gain for different values of R_G .

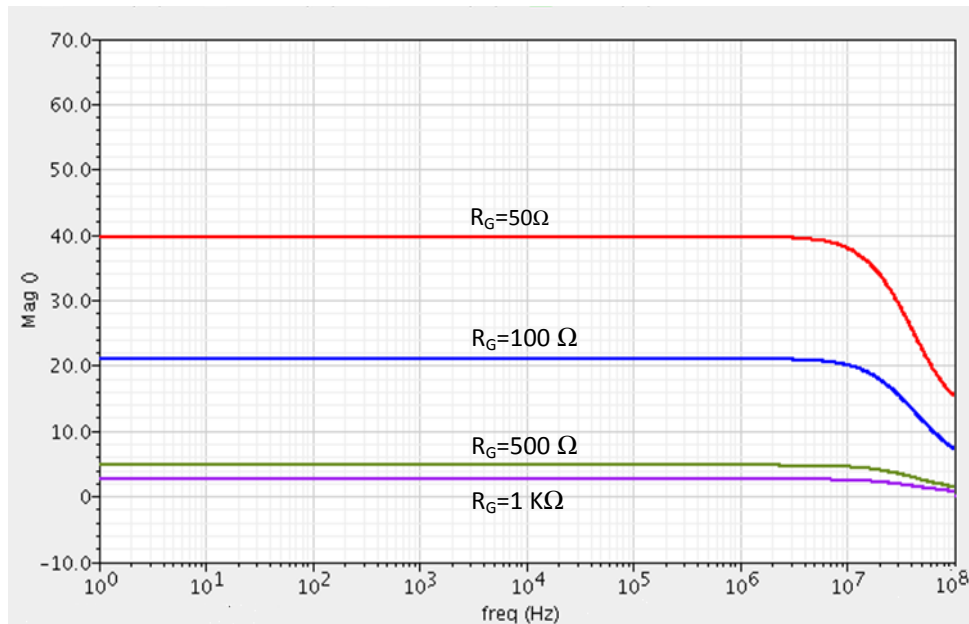


Figure 4-7: Gain for different values of R_G

The proposed topology for $R_L/R_G=10$ exhibits a differential gain equal 20 with bandwidth 32.7MHz which its gain is double the CMIA's in [32][34] and has bandwidth higher than other CMIA's by 30.7 MHz as shown in Table 4-1. However, its gain is similar to the CMIA given in [33][37]. Moreover, the proposed topology is independent of R_X and the gain is independent of the bandwidth.

B. CMRR Measurements

To measure the CMRR of the circuit, two identical ac signal source V_{cm} are connected in series with the inputs. An AC analysis is carried out for finding the CMRR [38].

$$\frac{v_o}{v_{CM}} = \frac{1}{CMRR} \quad (4-29)$$

The proposed CMIA exhibits a CMRR magnitude 61dB and bandwidth 292MHz which is independent of gain. It has the lowest CMRR as it is lower than [37] by 19.7% on the other hand the bandwidth of the CMRR is the highest as it is higher than [37] by 57.8%.

The input noise voltage for the proposed CMIA is lower than [37] by 99.98%. It has the widest dynamic range and highest signal-to-noise ratio compared to the other circuits. It is an integrated circuit compared to others which are discrete [32] [33] [34] [37].

Table 4-1: Comparison between the proposed and other CMIA circuits

CMIA Reference	Differential Gain For $R_L/R_G=10$				CMRR For $R_L/R_G=10$		Input noise voltage nV/\sqrt{Hz} for $R_L/R_G=10$	Number of building blocks used	Type of integration
	Mag (Value)	-3 dB Freq (BW)	Gain BW (MHz)	Gain varies with BW	Mag (dB)	-3 dB Freq (BW)			
[32]	9.09	2MHz	18.18	yes	65	16kHz	20.6	2 CCII+	Discrete
[34]	10	2MHz	20	yes	65	16kHz	22.4	2 CCII+ 2Op-amp	Discrete
[33]	17.8	1.4MHz	24.92	no	73	65kHz	19.8	3 CCII+	Discrete
[37]	20	1.2MHz	24	no	76	185kHz	15.2	2 OFCC	Discrete
Proposed	20	32.7MHz	654	no	61	292MHz	0.0032	2 OFCC	Integrated

4.4 Universal Filters

4.4.1 Introduction

Second-order universal filter with three inputs and a single output is selected to test the efficiency of the designed OFCC circuit [39] and is used in designing ECG as will be mentioned in section 4.5.

4.4.2 Universal Filter with three inputs and single output

Figure 4-8 shows the proposed second order universal filter with three inputs and one output. The analysis of the transfer function is shown in Appendix A.

In general the transfer function is:

$$V_o = \frac{s^2 C_1 C_2 C_3 R_1 R_2 R_3 V_1 + s C_2 R_2 R_3 V_2 + R_1 V_3}{s^2 C_1 C_2 C_3 R_1 R_2 R_3 + s C_2 R_2 R_3 + R_1} \quad (4-30)$$

This circuit can analyze three types of filters, which are low pass, band pass and high pass filters. These can be done by changing the input node connections.

For high pass filter, V_2 and V_3 are grounded and the input signal is V_1 .

For band pass filter, V_1 and V_3 are grounded and the input signal is V_2 .

For low pass filter, V_1 and V_2 are grounded and the input signal is V_3 .

The natural frequency (ω_o) and the quality factor (Q) are expressed as follows:

$$\omega_o = \sqrt{\frac{1}{C_1 C_2 R_2 R_3}} \quad (4-31)$$

$$Q = R_1 \sqrt{\frac{C_1}{C_2 R_2 R_3}} \quad (4-32)$$

Without affecting the performance of the OFCC circuit, controlling the natural frequency and the quality factor values can be done as they are independent of the feedback resistor R_w .

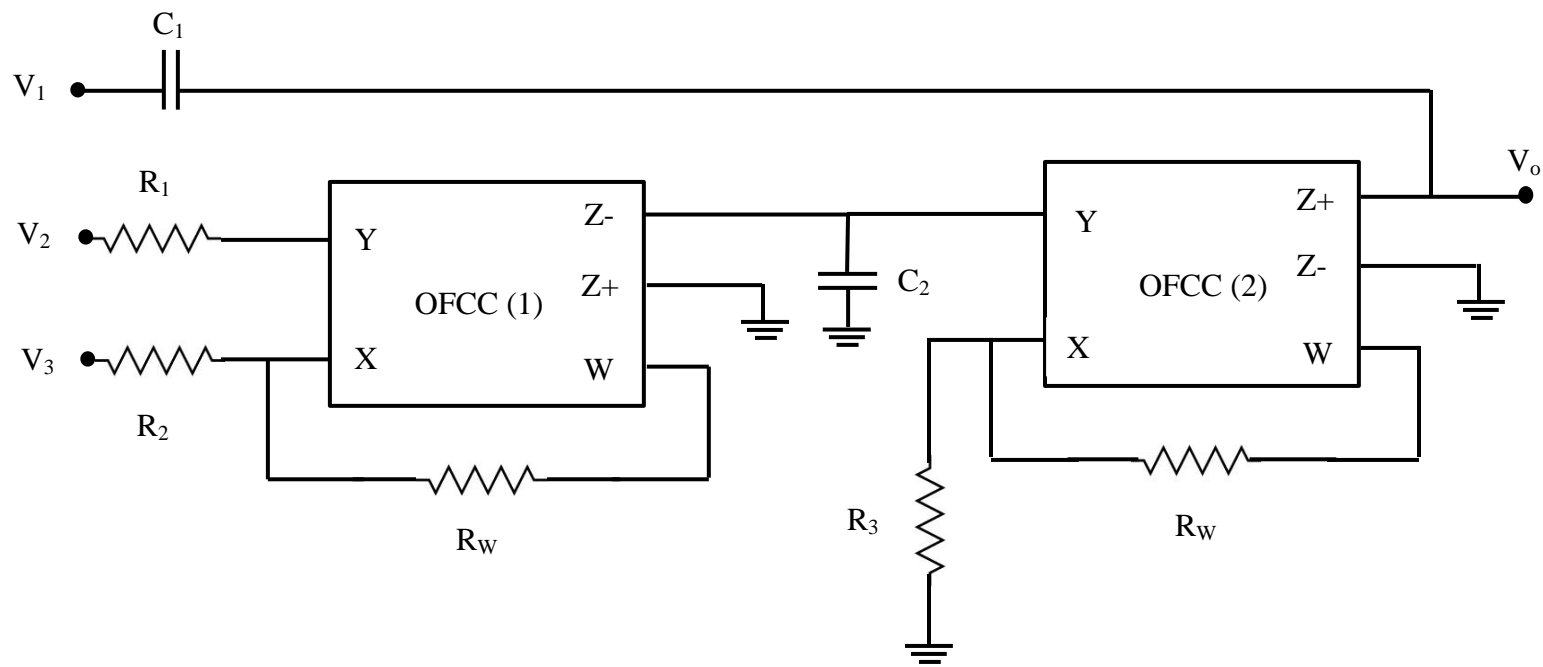


Figure 4-8: Second order universal filter [41]

4.4.3 Simulation Results

The resistance R_1 and R_3 are set to $3.6\text{K}\Omega$, R_2 was set to 300Ω and R_w was set to 1.5K . Also C_1 and C_2 are set to 19nF and 225nF respectively. The ω_o is 14.72Kr/s and the Q is equal to 1.01 .

4.4.3.1 Low pass Filter

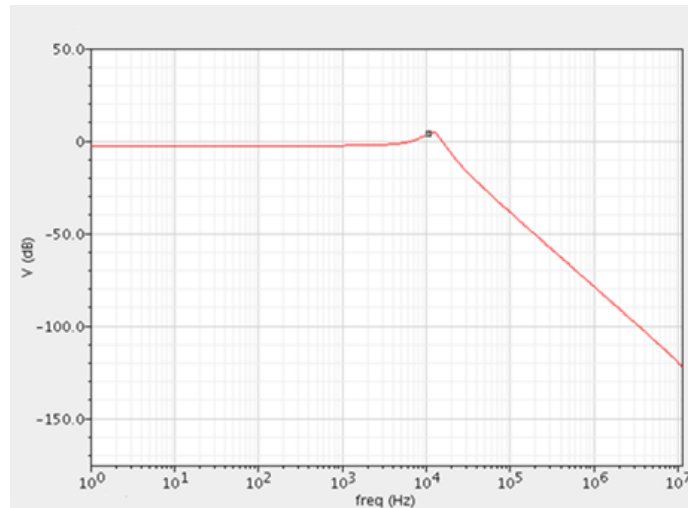


Figure 4-9: Magnitude response of the second-order universal filter in the Low-Pass Filter

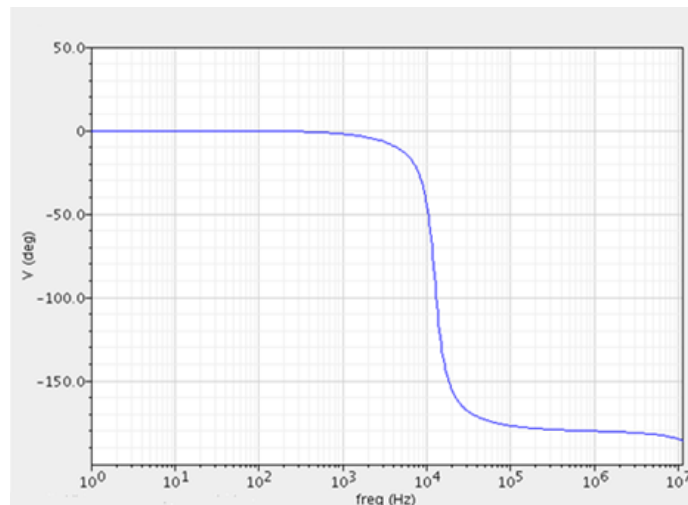


Figure 4-10: Phase response of the second-order universal filter in the Low-Pass Filter

4.4.3.2 Band pass Filter

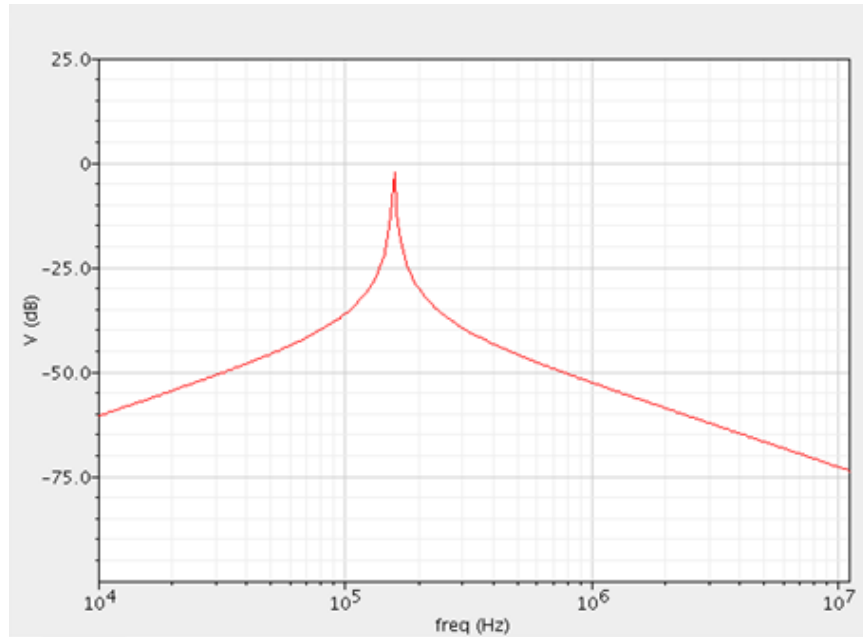


Figure 4-11: Magnitude response of the second-order universal filter in the Band-Pass Filter

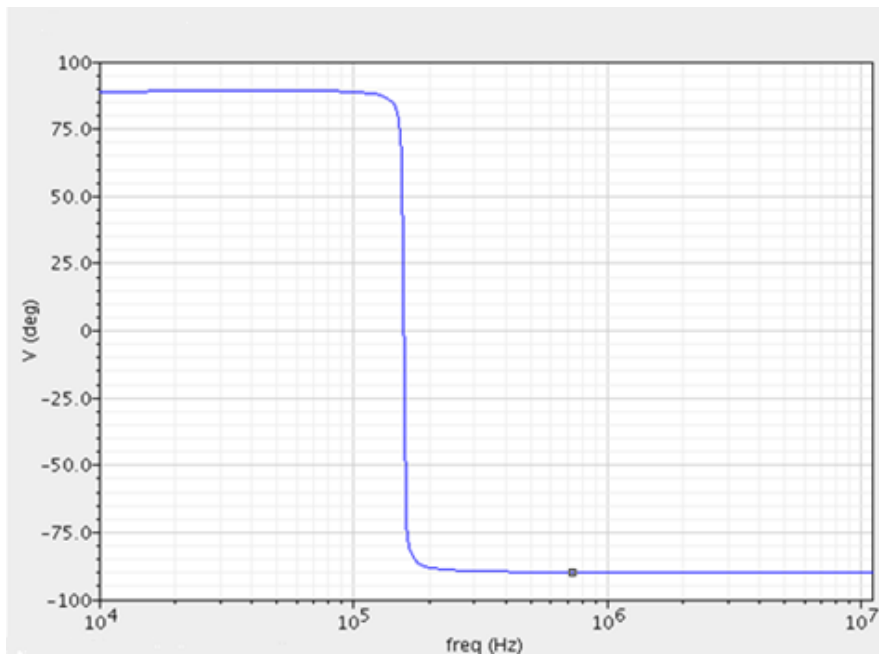


Figure 4-12: Phase response of the second-order universal filter in the Band-Pass Filter

4.4.3.3 High pass Filter

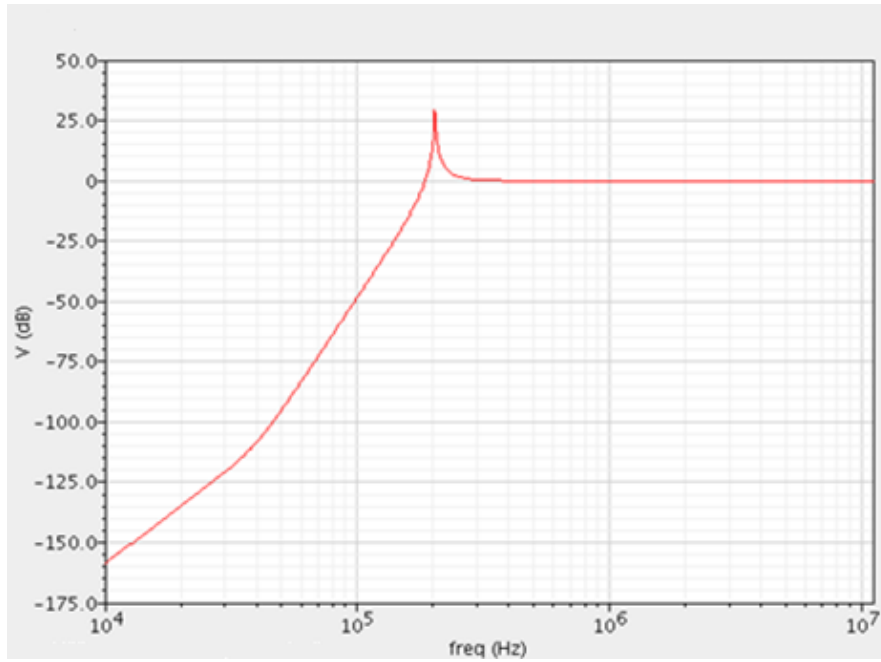


Figure 4-13: Magnitude response of the second-order universal filter in the High-Pass Filter

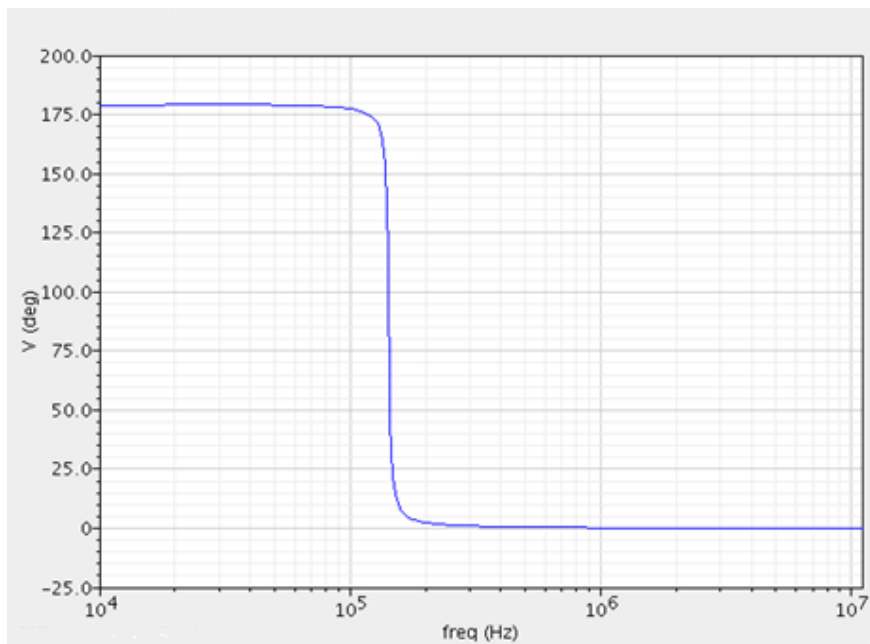


Figure 4-14: Phase response of the second-order universal filter in the High-Pass Filter

4.5 Electrocardiography

4.5.1 Introduction

Electrocardiography (ECG) is the analysis of the electrical activity of human's heart over a period of time. The human body contains cells that act like batteries. Biopotentials are small electric potentials that is created from different ions outside and inside the cells' membranes [40]. Figure 4-15 shows the depolarization and repolarization of the cell that exist when there is a disturbance in a biopotential.

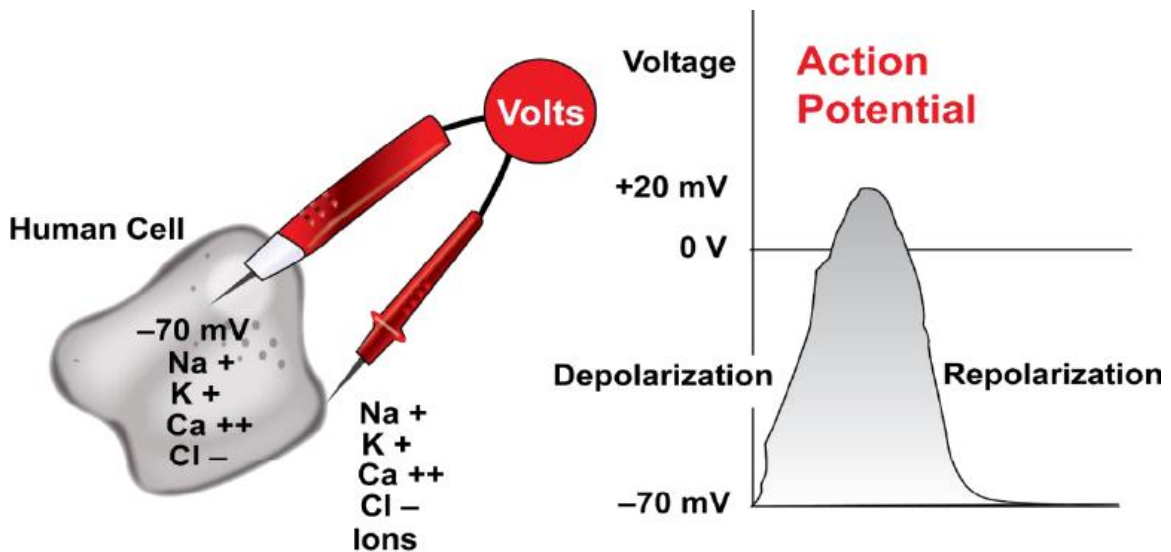


Figure 4-15: Depolarization and repolarization when there is a disturbance

Electrocardiograph (ECG) signals are made of the action potentials from different nodes in the heart as shown in Figure 4-16. Their measurement can be done by using the electrocardiogram (ECG).

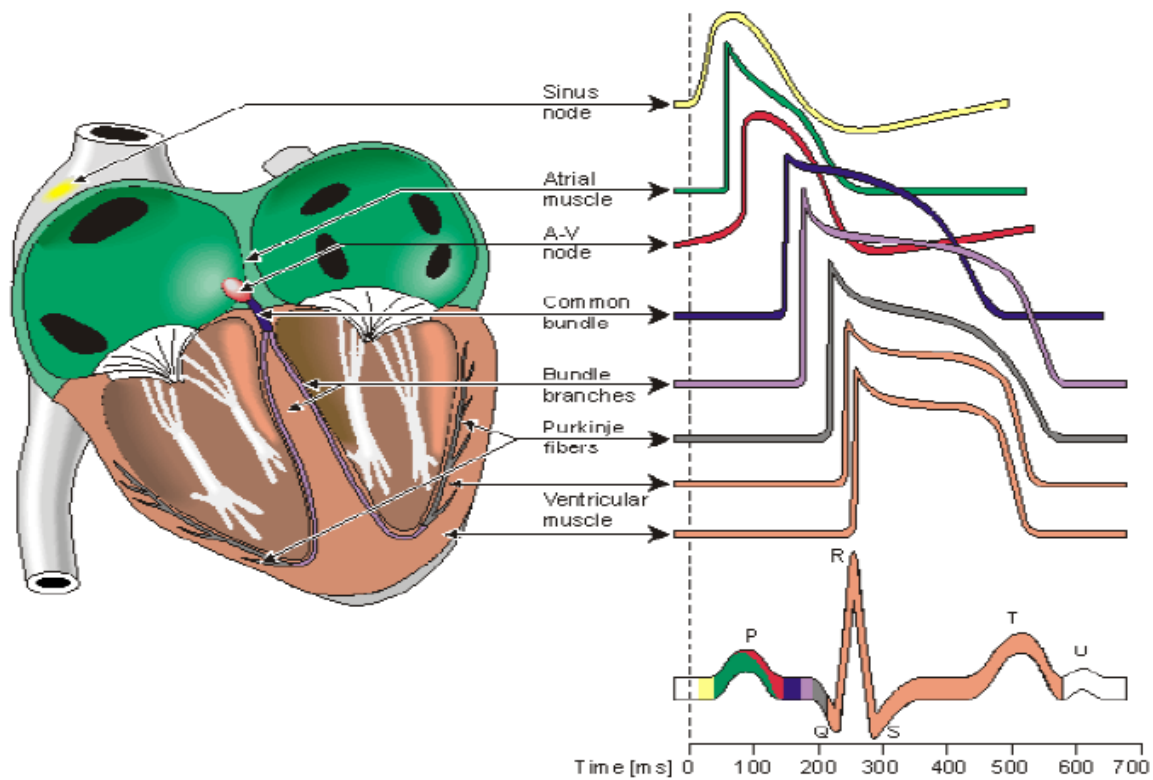


Figure 4-16: ECG signal [40]

4.5.2 Circuit Design

The main function of the ECG is to filter noise of the small signal measured from the heart then to amplify it as their range vary from the microvolt to the millivolt. So, the ECG is composed of two LPF and one CMIA as shown in Figure 4-17. Using OFCC in designing the ECG readout circuit has a great impact as it is a single block that and its layout is easy. In addition, the proposed OFCC has the lowest input voltage and its power consumption is low which makes the power of the ECG readout circuit low.

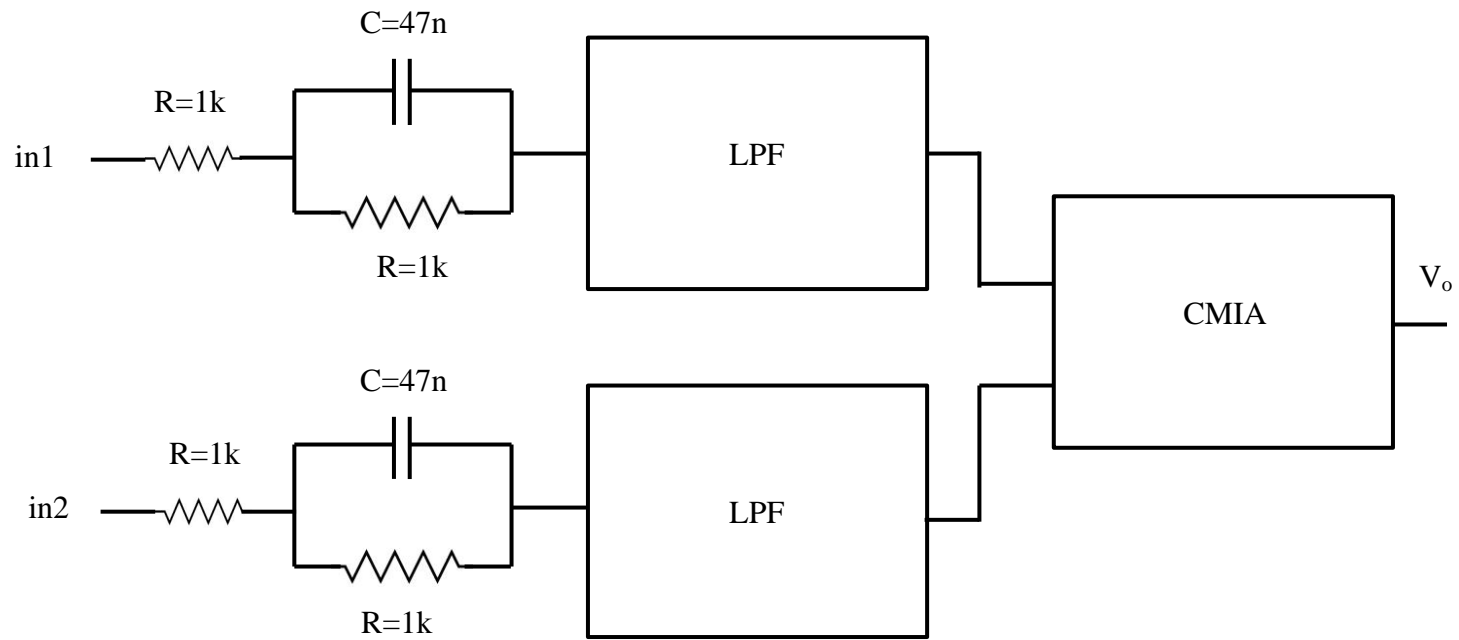


Figure 4-17: Proposed ECG circuit

4.5.2.1 Filter

The ECG signal is composed of noise that exist from the body and environment so using low pass filter helps to remove this noise. In designing the filter, we use the low pass filter as discussed in chapter 4. The resistors R_1 and R_3 are set to $4K\Omega$, R_2 is set to $2k\Omega$ and R_w is set to 500. Also C_1 and C_2 are set to $10\mu F$ and $10pF$ respectively. The frequency will be 55 Hz as shown in Figure 4-18.

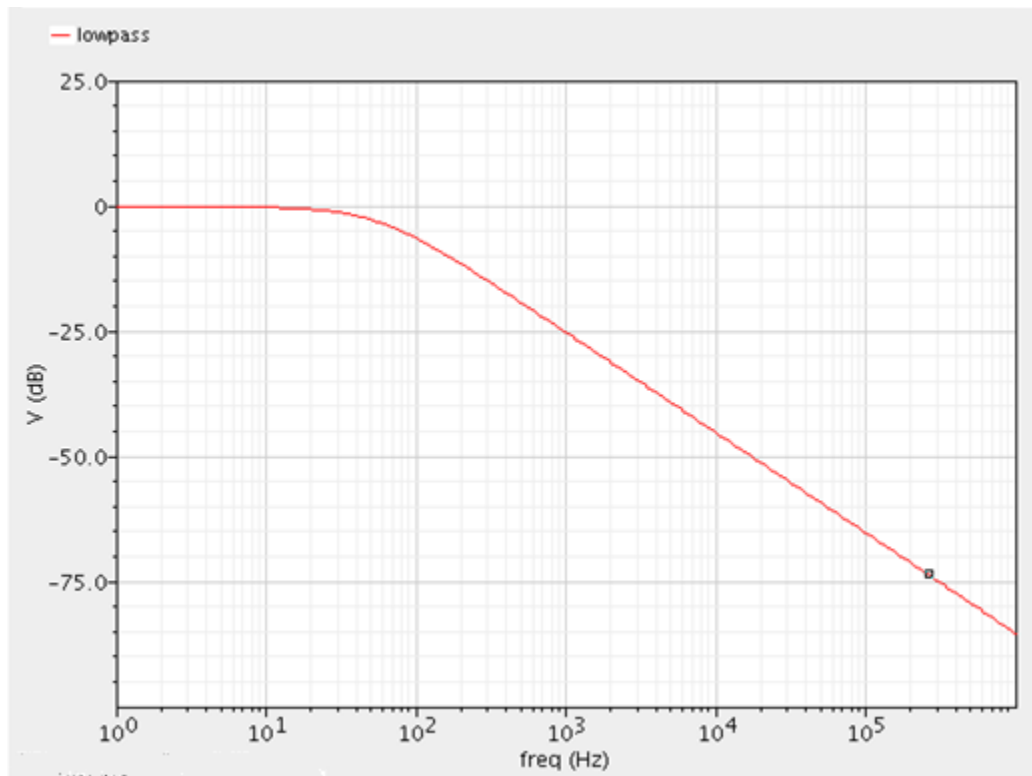


Figure 4-18: Low pass filter used in ECG

4.5.2.2 Instrumentation Amplifier

ECG signals vary from the microvolt to the millivolt range. The signal measured has to be amplified due to this small rang. In addition, to eliminate large offset signals the amplifier should have a high common mode rejection ratio. The instrumentation amplifier that is used in designing the ECG is previously discussed in chapter 4. Resistors R_{W1} and R_{W2} are set to $1K\Omega$, R_L and R_G are set to $10K\Omega$ and 50Ω respectively. Also C_1 and C_2 are set to $10pF$.

4.5.3 Simulation Results

The circuit is designed and simulated using UMC 130nm CMOS technology kit in Cadence. The DC power supply used is 1.2 Volt. The input signal is in mV so the output has to be amplified in order to appear on the ECG monitor as shown in Figure 4-19. The gain will be equal 14.4 and the power consumption is 4.65mW

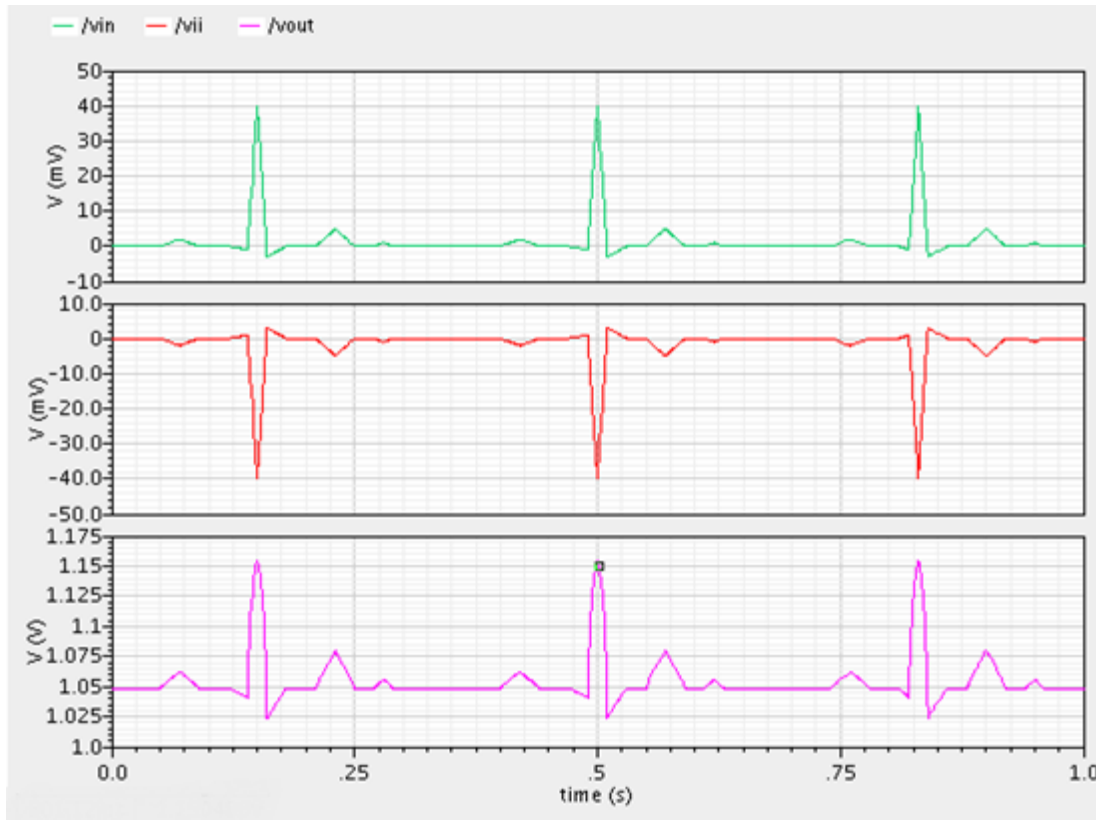


Figure 4-19: Input vs. output of ECG

Conclusion

An integrated CMOS based OFCC has been modeled and simulated. The circuit architecture uses a low-drive CCII+ as a first gain stage, a transconductance amplifier as second gain stage, and a high-drive CCII+ & a current steering circuit as output stages. The simulation results shows that the proposed OFCC has the following advantage: it offers wide bandwidth with low power consumption.

Applications based on OFCC such as non-inverting voltage amplifier, CMIA and universal filter are proposed. In addition, the first integrated OFCC based ECG read out circuit is proposed. It is designed using two LPF and CMIA and simulated using UMC 130nm CMOS technology kit in Cadence.

Future work

- OFCC will be fabricated using 130nm CMOS technology
- Compare the experimental results with the simulation results.
- An integrated readout circuit for ECG will be fabricated and its performance will be measured.
- Explore other biomedical applications that OFCC can be used.

Appendix (A)

Universal Filter

$$V_X = V_Y \quad (\text{A1})$$

$$i_{Z+} = i_W \quad (\text{A2})$$

$$i_{Z-} = -i_W \quad (\text{A3})$$

$$V_W = -Z_t i_X \quad (\text{A4})$$

Since, Z_t is very large

Then,

$$i_X \cong 0 \quad (\text{A5})$$

Low-Pass Filter:

$$V_{Y1} = V_{X1} = V_o \quad (\text{A6})$$

$$V_o \left(sC_1 + \frac{1}{R_1} \right) = \frac{V_{W2} - V_{X2}}{R_W} \quad (\text{A7})$$

$$\frac{V_{W1} - V_o}{R_W} = \frac{V_o - V_3}{R_2} \quad (\text{A8})$$

$$V_{W1} = V_o \left(1 + \frac{R_W}{R_2} \right) + \frac{R_W}{R_2} V_3 \quad (\text{A9})$$

$$V_{X2} = V_{Y2} = \frac{V_3 - V_o}{sC_2 R_2} \quad (\text{A10})$$

$$V_{X2} = V_{W2} \frac{R_3}{R_3 + R_W} \quad (\text{A11})$$

$$\frac{V_3 - V_o}{sC_2R_2} = V_{W2} \frac{R_3}{R_3 + R_W} \quad (\text{A12})$$

$$V_{W2} = R_W V_o \left(sC_1 + \frac{1}{R_1} \right) + V_{X2} \quad (\text{A13})$$

$$V_{W2} = V_{X2} \frac{R_3 + R_W}{R_3} \quad (\text{A14})$$

$$V_{X2} \frac{R_3 + R_W}{R_3} = R_W V_o \left(sC_1 + \frac{1}{R_1} \right) + V_{X2} \quad (\text{A15})$$

$$V_{X2} = R_3 V_o \left(sC_1 + \frac{1}{R_1} \right) \quad (\text{A16})$$

Substitute (A14) and (A16) in (A12)

$$V_o \left(sC_1 R_3 + \frac{R_3}{R_1} \right) = \frac{V_3 - V_o}{sC_2 R_2} \quad (\text{A17})$$

Then,

$$V_o = \frac{R_1 V_3}{s^2 C_1 C_2 R_1 R_2 R_3 + s C_2 R_2 R_3 + R_1} \quad (\text{A18})$$

Band-Pass Filter:

$$V_{Y1} = \frac{V_{W1}}{R_W + R_2} \quad (\text{A19})$$

From (A6)

Then,

$$V_{W1} = \left(\frac{R_W + R_2}{R_2} \right) V_o \quad (\text{A20})$$

$$V_{X2} = \frac{-V_{W1}}{sC_2(R_2 + R_W)} \quad (\text{A21})$$

Substitute (A20) in (A21)

$$V_{X2} = \frac{-\left(\frac{R_W+R_2}{R_2}\right)V_o}{sC_2(R_2+R_W)} \quad (A22)$$

$$V_{X2} = -\frac{V_o}{sC_2R_2} \quad (A23)$$

Substitute (A23) in (A14)

$$V_{W2} = -\left(\frac{V_o}{sC_2R_2}\right)\left(\frac{R_3+R_W}{R_3}\right) \quad (A24)$$

$$V_o\left(sC_1 + \frac{1}{R_1}\right) - \frac{V_2}{R_1} = \frac{V_{W2}-V_{X2}}{R_W} \quad (A25)$$

Substitute (A23) and (A24) in (A25)

$$V_o = \frac{sC_2R_2R_3V_2}{s^2C_1C_2R_1R_2R_3+sC_2R_2R_3+R_1} \quad (A26)$$

High- Pass Filter:

$$V_{X1} = V_{Y1} = V_o = \frac{V_{W1}}{R_2+R_W}R_2 \quad (A27)$$

$$V_{W1} = \left(\frac{R_W+R_2}{R_2}\right)V_o \quad (A28)$$

$$V_o\left(sC_1 + \frac{1}{R_1}\right) - sC_1V_1 = \frac{V_{W2}-V_{X2}}{R_W} \quad (A29)$$

Substitute (A23) and (A24) in (A29)

$$V_o\left(sC_1 + \frac{1}{R_1}\right) - sC_1V_1 = -\frac{V_o}{sC_2R_2R_3} \quad (A30)$$

$$V_o = \frac{s^2C_1C_2R_1R_2R_3V_1}{s^2C_1C_2R_1R_2R_3+sC_2R_2R_3+R_1} \quad (A31)$$

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[1] Nermine M. Edward, Yehya H. Gallab, Hassan Mostafa, and Yehea I. Ismail, “*A CMOS Based Operational Floating Current Conveyor*”, IEEE International Conference on Electronics, Circuits, and Systems, Cairo, December 2015.

[2] Nermine M. Edward, Yehya H. Gallab, Hassan Mostafa, and Yehea I. Ismail, “*A CMOS Based Operational Floating Current Conveyor And Its Applications*”, IEEE International Conference on Electronics, Circuits, and Systems, Cairo, December 2015.