



# DESIGN FOR YIELD IN MEMRISTOR- BASED MEMORY ARRAYS

By

Marwa Abdallah Mostafa Masoud

A Thesis Submitted to the  
Faculty of Engineering at Cairo University  
In Partial Fulfillment of the  
Requirements for the Degree of  
MASTER OF SCIENCE  
In  
Electronics and Communications Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY  
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**Title of Thesis:**

Design for Yield in Memristor based Memory Array

**Key Words:**

Memristor; Nonvolatile; Process Variation; Yield; Memory Array

**Summary:**

The missing fourth passive circuit element, the memristor, attracted a great attention when HP labs developed the first real memristor device in 2008. The memristor manufacturing is facing various challenges due to the difficulty to control its process variation, as it is fabricated at nano-scale geometry's size. Process variation deviate the actual electrical behavior of memristors from the desired values. This deviation reduces the yield especially in the memristor-based memory design. In this work, we analyze the impact of the process variations on the electrical properties of both TiO<sub>2</sub> thin-film and spintronic memristors. A compact model is proposed to generate a large volume of process variation-aware three-dimensional device structures for Monte-Carlo simulations. Therefore, it is very important to understand and characterize the impact of process variation on memristor performance and yield and attempt to optimize the yield.



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# **Dedication**

To God, and mother, without you none of my achievements would have been possible. Thanks you for standing by my side, giving me the required strength to overcome all my obstacles and reach my goals.

# Table of Contents

|   |             |
|---|-------------|
| <b>ACKNOWLEDGMENTS</b> .....  | <b>I</b>    |
| <b>DEDICATION</b> .....   | <b>II</b>   |
| <b>TABLE OF CONTENTS</b> .....  | <b>III</b>  |
| <b>LIST OF TABLES</b> .....   | <b>VII</b>  |
| <b>LIST OF FIGURES</b> .....  | <b>VIII</b> |
| <b>NOMENCLATURE</b> .....   | <b>XI</b>   |
| <b>ABSTRACT</b> .....   | <b>XII</b>  |
| <br>  |             |
| <b>CHAPTER 1 : INTRODUCTION</b>   | <b>1</b>    |
| 1.1 Background.....   | 1           |
| 1.2 Motivation.....   | 2           |
| 1.3 Organization of the Thesis.....                                     | 3           |
| <br>  |             |
| <b>CHAPTER 2 : OVERVIEW OF MEMORY TECHNOLOGIES</b>                      | <b>4</b>    |
| 2.1 Memory Systems.....   | 5           |
| 2.1.1 SRAM.....   | 5           |
| 2.1.2 DRAM.....   | 6           |
| 2.1.3 Disk and Flash.....   | 7           |
| 2.2 Emerging Memories.....  | 10          |
| 2.2.1 Phase-Charge RAM (PCRAM).....                                     | 10          |
| 2.2.2 Resistive RAM (RRAM).....   | 12          |
| 2.2.2.1 Memristor.....  | 12          |
| 2.2.3 Magnetoresistive RAM (MRAM).....                                  | 13          |
| 2.2.3.1 STT-RAM.....  | 14          |
| 2.3 Comparison between Memory Technologies.....                         | 15          |
| <br>  |             |
| <b>CHAPTER 3: TIO2 AND SPINTRONIC MEMRISTOR DEVICE</b> .....            | <b>16</b>   |
| 3.1 Memristor Theory.....   | 16          |
| 3.2 TiO <sub>2</sub> Memristor Working and Operation.....               | 20          |
| 3.3 TiO <sub>2</sub> Physical Model.....                                | 22          |
| 3.3 TiO <sub>2</sub> Fabrication Process.....                           | 24          |
| 3.3.1 Selection of Substrate.....                                       | 25          |
| 3.3.2 Bottom Electrode.....   | 26          |
| 3.3.3 Oxygen Incomplete Titanium Oxide Layer (TiO <sub>2-x</sub> )..... | 27          |
| 3.3.4 Oxygen Titanium Oxide Layer (TiO <sub>2</sub> ).....              | 28          |
| 3.3.5 Top Electrode.....  | 28          |
| 3.3.6 Overview of the Fabrication Process.....                          | 31          |



|   |           |
|---|-----------|
| 3.4 Spintronic Memristor Fundamentals.....                              | 33        |
| 3.5 Electrical Property of Spintronic Memristor.....                    | 34        |
| 3.5.1 Current density $J$ and effective current density $J_{eff}$ ..... | 35        |
| 3.5.2 Critical current density $J_{cr}$ .....                           | 36        |
| 3.5.3 Domain wall velocity coefficient $\Gamma v$ .....                 | 36        |
| 3.6 Compact Model of Spintronic Memristor.....                          | 36        |
| 3.6.1 Spintronic memristance.....                                       | 37        |
| 3.6.2 Spintronic resistance.....  | 37        |
| 3.6.3 Domain wall position $x$ .....                                    | 38        |
| <br>  |           |
| <b>CHAPTER 4: VARIABILITY.....</b>                                      | <b>40</b> |
| 4.1 Classification of Variations.....                                   | 42        |
| 4.1.1 Inter-die Variations.....   | 43        |
| 4.1.2 Intra-die Variations.....   | 43        |
| 4.1.2.1 Random Variations.....  | 44        |
| 4.1.2.2 Systematic Variations.....                                      | 44        |
| 4.2 Variation Sources.....  | 45        |
| 4.2.1 Process variation physical factors (Static Variation).....        | 45        |
| 4.2.1.1 Random Doping Fluctuations (RDF).....                           | 45        |
| 4.2.1.2 Line Edge Roughness (LER).....                                  | 47        |
| 4.2.1.3 Oxide Thickness Fluctuation (OTF).....                          | 48        |
| 4.2.2 Process variation environmental factors (Dynamic variation).....  | 49        |
| 4.2.2.1 Thermal Variations.....   | 49        |
| 4.2.2.2 Power Supply Variation.....                                     | 50        |
| 4.2.2.3 Soft Errors.....  | 50        |
| 4.2.3 Aging Variations.....   | 51        |

|   |            |
|---|------------|
| <b>CHAPTER 5: COMPACT MODEL OF TIO2 MEMRISTOR UNDER<br/>PROCESS VARIATIONS, AND SIMULATION RESULTS.....</b>       | <b>52</b>  |
| 6.1 TiO <sub>2</sub> Memristor Compact Model.....   | 52         |
| 6.2 TiO <sub>2</sub> Thin-Film Memristor Yield without Variation Compensation.....                                | 56         |
| 6.3 TiO <sub>2</sub> Writing Yield Optimization.....  | 59         |
| 6.4 TiO <sub>2</sub> Reading Yield Optimization.....  | 65         |
| <br>  |            |
| <b>CHAPTER 6: COMPACT MODEL OF SPINTRONIC MEMRISTOR<br/>UNDER PROCESS VARIATIONS, AND SIMULATION RESULTS.....</b> | <b>69</b>  |
| 6.1 Spintronic Memristor Compact Model.....   | 69         |
| 6.2 Spintronic Memristor Yield without Variation Compensation.....  | 74         |
| 6.3 Spintronic Memristor Writing Yield Optimization.....  | 77         |
| 6.4 Spintronic Memristor Reading Yield Optimization.....  | 81         |
| 6.5 Comparison between TiO <sub>2</sub> thin-film Memristor and Spintronic Memristor<br>Simulation Results.....   | 86         |
| <br>  |            |
| <b>CHAPTER 7: CONCLUSIONS AND FUTURE WORK.....</b>  | <b>91</b>  |
| 7.1 Conclusion.....   | 91         |
| 7.2 Published and Submitted Papers.....   | 91         |
| 7.3 Future Work.....  | 92         |
| <br>  |            |
| <b>REFERENCES .....</b>   | <b>93</b>  |
| <br>  |            |
| <b>APPENDIX A.....</b>  | <b>99</b>  |
| <br>  |            |
| <b>APPENDIX B.....</b>  | <b>105</b> |

# List of Tables

|   |    |
|---|----|
| 2.1 Detailed comparison between memristor-based memory, traditional memories,<br>And other emerging memories..... | 15 |
| 3.1 Until recent years, the three fundamental circuit elements and their physical<br>relationship.....            | 16 |
| 4.1 Constants and parameters in spintronic memristor model.....   | 39 |
| 5.2 Model parameters.....   | 55 |
| 5.2 TiO <sub>2</sub> dimensions and $\sigma_y$ values.....  | 56 |
| 5.3 Yields values before and after variation compensation.....  | 65 |
| 6.1 The model parameters.....   | 72 |
| 6.2 Spintronic memristor dimensions and $\sigma_y$ values.....  | 73 |
| 6.3 Different size of spintronic memristor and their yield values before / after variation<br>compensation.....   | 82 |

# List of Figures

|   |    |
|---|----|
| Figure 2.1: 6-T SRAM cell [1].....  | 5  |
| Figure 2.2: a) DRAM cell and b) DRAM array organization [1].....  | 6  |
| Figure 2.3: Hard disk internals overview [1].....   | 7  |
| Figure 2.4: NOR Flash array and NAND Flash array architectures [5].....   | 9  |
| Figure 2.5: Basic PCRAM cell structure [12].....  | 10 |
| Figure 2.6: Relationship between current and voltage in a memristor [16].....   | 12 |
| Figure 2.7: The memristor under the electrical behavior [16].....   | 12 |
| Figure 2.8: A conceptual view of MTJ structure. (a) Anti-parallel (high resistance), which indicates “1” state; (b) Parallel (low resistance), which indicates “0” state [17].....  | 13 |
| Figure 2.9: Basic STT-RAM cell structure [21].....  | 14 |
| Figure 3.1: The fourth Fundamental circuit elements and their physical relationship [15].....   | 17 |
| Figure 3.2: Memristor device structure presented by S. Williams and his research group at HP Laboratories [16].....   | 19 |
| Figure 3.3: a) Oxygen vacancies in the $TiO_{2-x}$ can be considered as positive charges. b) when a positive potential is applied to the $TiO_{2-x}$ side these positive charges a repelled towards the $TiO_2$ layer, c) while the opposite happens if a negative potential is applied instead. In other words, the memristor’s oxygen vacancies ion drift is possible when applying a voltage potential to its electrodes [16]..... | 21 |
| Figure 3.4: physical model HP ( $TiO_2$ thin-film memristor). (a) Structure, and (b) equivalent circuit [16].....   | 22 |
| Figure 3.5: Figure showing ideal memristor behavior. OFF and ON states shown by (b) and (c) respectively. The operation between states is illustrated in (a) [27].....  | 23 |
| Figure 3.6: $TiO_2$ memristor device architecture presented by S. Williams and his research group at HP Laboratories [16].....  | 24 |

|   |    |
|---|----|
| Figure 3.7 a) Silicon wafers with a 50mm diameter were used as substrates. b) The wafers were cleaned by deep submersion in a H <sub>2</sub> O: HF solution with 50:1 ratio [32].....   | 26 |
| Figure 3.8: A piece of silicon wafer was used to hard mask part of the tungsten bottom contact in order to avoid any other material to deposit in one section of the back contact allowing us to reach the back electrode for future electrical characterization [32].....              | 27 |
| Figure 3.9: The TiO <sub>2</sub> and TiO <sub>2-x</sub> layers can be observed as the bluish section of the wafer, while the hard masked tungsten remained accessible without any material deposited in top. Marks of the claps used to attach the hard mask are also visible [32]..... | 28 |
| Figure 3.10: Overview of the developed fabrication process for the basic TiO <sub>2</sub> memristor devices [32].....   | 32 |
| Figure 3.11: A spintronic memristor based on magnetic-domain-wall motion. (a) Structure. (b) Equivalent circuit [36].....   | 33 |
| Figure 4.1: pattern variations “Design phase & manufacturing phase” [42].....   | 40 |
| Figure 4.2: Lithography wavelength scaling for different technology nodes [44].....   | 41 |
| Figure 4.3: Wafer and die [45].....   | 42 |
| Figure 4.4: Inter-die or Die-to-Die variations (D2D). a) Variations between different dies in the same wafer, b) variations between different dies in the different wafers [45].....  | 43 |
| Figure 4.5: Intra-die or Within-Die Variations (WID) [45].....  | 44 |
| Figure 4.6: Random dopant effect [47].....  | 45 |
| Figure 4.7: Number and distribution of dopant atoms in a transistor [48].....   | 46 |
| Figure 4.8: Laser image appears details of line edge roughness (LER) [44].....  | 47 |
| Figure 4.9: Oxide thickness fluctuations [47].....  | 48 |
| Figure 4.10: Thermal profile showing within die temperature variation for a microprocessor. Hot spots with temperatures as high as 120oC are shown [46].....  | 50 |
| Figure 5.1: PDF of R <sub>ON</sub> and R <sub>OFF</sub> , the cross failure region.....   | 53 |
| Figure 5.2: TiO <sub>2</sub> thin film memristor structure.....   | 56 |
| Figure 5.3: The yield without variation compensation at case D=3nm.....   | 57 |
| Figure 5.4: The yield without variation compensation at case D=6nm.....   | 57 |

|   |    |
|---|----|
| Figure 5.5: The yield without variation compensation at case $D=10\text{nm}$ .....                                | 58 |
| Figure 5.6: The yield without variation compensation at case $D=15\text{nm}$ .....                                | 58 |
| Figure 5.7: The writing yield before/after variation compensation in case $D=3\text{nm}$ .....                    | 61 |
| Figure 5.8: The writing yield before/after variation compensation in case $D=6\text{nm}$ .....                    | 62 |
| Figure 5.9: The writing yield before/after variation compensation in case $D=10\text{nm}$ ...                     | 62 |
| Figure 5.10: The writing yield before/after variation compensation in case $D=15\text{nm}$ ..                     | 63 |
| Figure 5.11: The threshold point at $\text{TiO}_2$ Memristor.....   | 66 |
| Figure 5.12: Max reading yield in case $D=3\text{nm}$ .....   | 66 |
| Figure 5.13: Max reading yield in case $D=6\text{nm}$ .....   | 67 |
| Figure 5.14: Max reading yield in case $D=10\text{nm}$ .....  | 67 |
| Figure 5.15: Max reading yield in case $D=15\text{nm}$ .....  | 68 |
| Figure 6.1: PDF of $R_L$ and $R_H$ , the cross failure region.....  | 70 |
| Figure 6.2: Spintronic memristor structure.....   | 74 |
| Figure 6.3: Yield without variation compensation at $h=7\text{nm}$ , $z=10\text{nm}$ , and $D=100:500$<br>.....   | 74 |
| Figure 6.4: Yield without variation compensation at $h=10\text{nm}$ , $z=15\text{nm}$ , and $D=100:500$<br>.....  | 75 |
| Figure 6.5: Yield without variation compensation at $h=7\text{nm}$ , $z=10\text{nm}$ , and $D=600:1000$<br>.....  | 75 |
| Figure 6.6: Yield without variation compensation at $h=10\text{nm}$ , $z=15\text{nm}$ , and<br>$D=600:1000$ ..... | 76 |
| Figure 6.7: Writing yield at case $h=7\text{nm}$ , $z=10\text{nm}$ , and $D=100:500$ .....                        | 78 |
| Figure 6.8: Writing yield at case $h=10\text{nm}$ , $z=15\text{nm}$ , and $D=100:500$ .....                       | 78 |
| Figure 6.9: Writing yield at case $h=7\text{nm}$ , $z=10\text{nm}$ , and $D=600:1000$ .....                       | 79 |
| Figure 6.10: Writing yield at case $h=10\text{nm}$ , $z=15\text{nm}$ , and $D=600:1000$ .....                     | 79 |
| Figure 6.11: The threshold point at spintronic memristor.....   | 83 |
| Figure 6.12: Reading yield at case $h=7\text{nm}$ , $z=10\text{nm}$ and $D=100:500$ .....                         | 83 |
| Figure 6.13: Reading yield at case $h=10\text{nm}$ , $z=15\text{nm}$ and $D=100:500$ .....                        | 84 |
| Figure 6.14: Reading yield at case $h=7\text{nm}$ , $z=10\text{nm}$ and $D=600:1000$ .....                        | 84 |

|  |    |
|--|----|
| Figure 6.15: Reading yield at case $h=10\text{nm}$ , $z=15\text{nm}$ and $D=600:1000$ .....  | 85 |
| Figure.6.16: The yield of $\text{TiO}_2$ memristor and spintronic memristor in case without variation compensation.....                | 86 |
| Figure.6.17: The writing yield of $\text{TiO}_2$ memristor and spintronic memristor in case with variation compensation.....           | 87 |
| Figure 6.18: The reading yield of $\text{TiO}_2$ memristor in case of after variation compensation with threshold point technique..... | 88 |
| Figure 6.19: The reading yield of spintronic memristor in case of after variation compensation with threshold point technique.....     | 89 |

## Nomenclature

|         |   |
|---------|---|
| RAM     | Random Access Memory                      |
| SRAM    | Static Random Access Memory               |
| DRAM    | Dynamic Random Access Memory              |
| RRAM    | Resistive Random Access Memory            |
| PCRAM   | Phase Change Random Access Memory         |
| STT-RAM | Spin-Torque Transfer Random Access Memory |
| 1D1M    | one Diode one Memristor                   |
| 1T1C    | one Transistor one Capacitor              |
| 1T1M    | one Transistor one Memristor              |
| MRAM    | Magneto-resistive Random Access Memory    |
| LER     | Line Edge Roughness                       |
| RDD     | Random Discrete Doping                    |
| OTF     | Oxide Thickness Fluctuation               |



# Abstract

Forty years ago, Professor Chua predicted the existence of the memristor - the fourth fundamental circuit element, to complete the set of passive devices that previously include only resistor, capacitor, and inductor. In 2008, the first physical realization of the memristor was demonstrated by HP Labs, in which the memristive effect was achieved by moving the doping front along  $\text{TiO}_2$  thin-film device. Beside the solid-state device, magnetic technology provides other possible solutions to build a memristive system. Moreover, the memristor has the ability to retain the state for a long time after the current has been switched OFF. Due to its ability to remember past charges, an intuitive utilization for it is to be used in the memory design.

Memristor shows various promising characteristics as the next-generation data storage device, such as non-volatility, low power consumption, high performance, high density and excellent scalability. The memristor manufacturing is facing various challenges due to the difficulty to control its process variation, as it is fabricated at nano-scale geometry. Process variation deviates the actual electrical behavior of memristors from the desired values. This deviation results in reducing the yield especially in the memristor-based memory arrays. The yield is defined as the number of memristors that exhibit correct writing/reading operation. The process variations sources are line-edge roughness (LER), oxide thickness fluctuation (OTF), and random discrete doping (RDD).

In this work, we analyze the impact of the process variations on the electrical properties of both  $\text{TiO}_2$  thin-film and spintronic memristors. A compact model is proposed to generate a large volume of process variation-aware three-dimensional device structures for Monte-Carlo simulations. We introduce two techniques to optimize the memristor yield; writing yield optimization by selecting the optimal flux (optimal current density) through applying voltage to  $\text{TiO}_2$  memristor (spintronic memristor) respectively; and reading yield optimization by selecting the threshold point that achieve the maximum yield.



# Chapter 1

## Introduction

### 1.1 Background

The memristor is recognized as the missing fourth basic circuit element predicted by Leon Chua in 1971 [1]. As known, the basic circuit elements such as resistance (R), capacitance (C), and inductance (L), interpret the relationships between fundamental electrical quantities such as voltage (v), current (i), charge (q), and flux ( $\phi$ ). For instance, R relates v and i, capacitance relates q and v, and inductance relates  $\phi$  and i, respectively. L. Chua argued that there exists a missing link between  $\phi$  and q, which is called memristance [1]. Memristor also called memory resistor which has both of memory and resistor characteristics. The device has two terminals and units of resistance. By definition, a linear Memristor acts like a resistor. However, as the  $\phi$ -q relation is nonlinear, the device behavior differs from that of a resistor. The main difference between a memristor and a resistor is that memristance is a function of charge, which depends on the hysteretic behavior of current/voltage profile [4]. Moreover, the memristor has the ability to retain the state for a long time after the current has been switched OFF. Due to its ability to remember past charges, an intuitive utilization for it is to be used in memory design [2].

In 2008, the first physical realization of memristor was demonstrated by HP Lab, in which the memristive effect was achieved by moving the doping front along TiO<sub>2</sub> thin-film device [2]. Beside the solid-state device, magnetic technology provides other possible solutions to build a memristive system [3, 4]. Three spintronic memristor structures have been proposed in [3]. They are spin valve with spin-torque-induced domain-wall motion in the free layer, MTJ (magnetic tunneling junction) with spin-

torque-induced magnetization switching, and thin film element with spin-torque-induced domain-wall motion. Compared to the solid-state thin film device [2], the behavior of a spintronic memristor, e.g., the relationship between the memristance and the current through the memristor, can be controlled more flexibly. Also, the technology to integrate magnetic device on the top of CMOS device has become mature in the development of magnetic memory [5]. Memristor shows many promising characteristics as the next-generation data storage device, such as non-volatility, low power consumption, high performance, high density and excellent scalability [3] [5].

The memristor is at nano-scale geometry size, so it suffers from process variation in the fabrication process. Process variations lead to significant device parameter fluctuations which is a critical concern affecting the device performance [3] [9]. The impact of process variations on a memristive system is more severe than a conventional digital design because of the utilization of the analog states of memristors. Many models have been carried out for various memristor devices. The process variations sources are line-edge roughness (LER), and random discrete doping (RDD) [10].

## 1.2 Motivation

As the memristor is at nano-scale geometry size, the uniformity of memristor device is difficult to control due to the process variations in the fabrication process. Process variation deviate the actual electrical behavior of memristors from the desired values. This deviation results in reducing the yield especially in the memristor-based memory design. The yield is defined as the number of memristors that exhibit correct writing/reading operation. Therefore, it is very important to understand and characterize the impact of process variation on memristor performance and yield and attempt to optimize the yield of the memristor-based memory arrays. In this work, we analyze the impact of the process variations on the electrical properties of both  $\text{TiO}_2$  thin-film and spintronic memristors. A compact model is proposed to generate a large volume of process variation-aware three-dimensional device structures for Monte-Carlo simulations. We introduce two techniques to optimize the memristor yield; writing yield optimization by selecting the optimal flux (optimal current density) through

applying voltage to TiO<sub>2</sub> memristor (spintronic memristor) respectively; and reading yield optimization by selecting the threshold point that achieve the maximum yield.

## 1.3 Thesis Outline

This thesis is structured as follows. **Chapter 2** Overview of emerging nonvolatile memory technologies **Chapter 3** introduces the fundamentals of memristor theory and the physical mechanisms of TiO<sub>2</sub> thin film memristor. **Chapter 4** introduces the Spintronic memristor. **Chapter 5** introduces the process variation sources and classification. **Chapter 6** compact model of TiO<sub>2</sub> thin film memristor and spintronic memristor; analyzes the memristor models under process variations; presents and analyzes the simulation results of the TiO<sub>2</sub> thin film memristor and spintronic memristor. **Chapter 7** conclusion and future work.

# Chapter 2

## Overview of memory technologies

For almost 30 years, computer memory systems have been basically the same: volatile, high speed memory technologies like SRAM and DRAM used for cache and main memory; magnetic disks for high-end data storage; and persistent, low speed flash memory for storage with low capacity/low energy consumption requirements such as embedded/mobile devices. Today we watch the emergence of new non-volatile memory technologies, such as Phase- Change RAM (PCRAM), Magneto-resistive RAM (MRAM) and Resistive RAM (RRAM) that promise to radically change the landscape of memory systems [1].

This chapter summarizes the current state of memory system design, presents these new memory technologies and surveys the current proposals on how to apply these technologies to improve memory hierarchies. We conclude that the introduction of these new technologies will probably result in more complex memory hierarchies, but is likely to allow the construction of memory chips that are non-volatile, low-energy and have density and latency close to or better than current DRAM chips, improving performance/efficiency and allowing memory systems to continue to scale up [2].

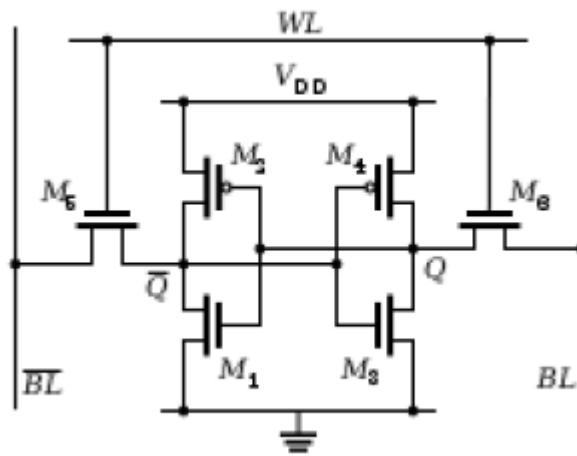
### 2.1 Memory Systems: Current technology

In order to discuss the emergent Non-Volatile Memory (NVM) technologies, we need to start by summarizing the current state of memory systems.

#### 2.1.1 SRAM

SRAM (Static Random Access Memory) is a volatile memory that retains data bits in its memory as long as power is being supplied. Unlike dynamic RAM (DRAM),

which stores bits in cells consisting of a capacitor and a transistor, SRAM does not have to be periodically refreshed [1-2].



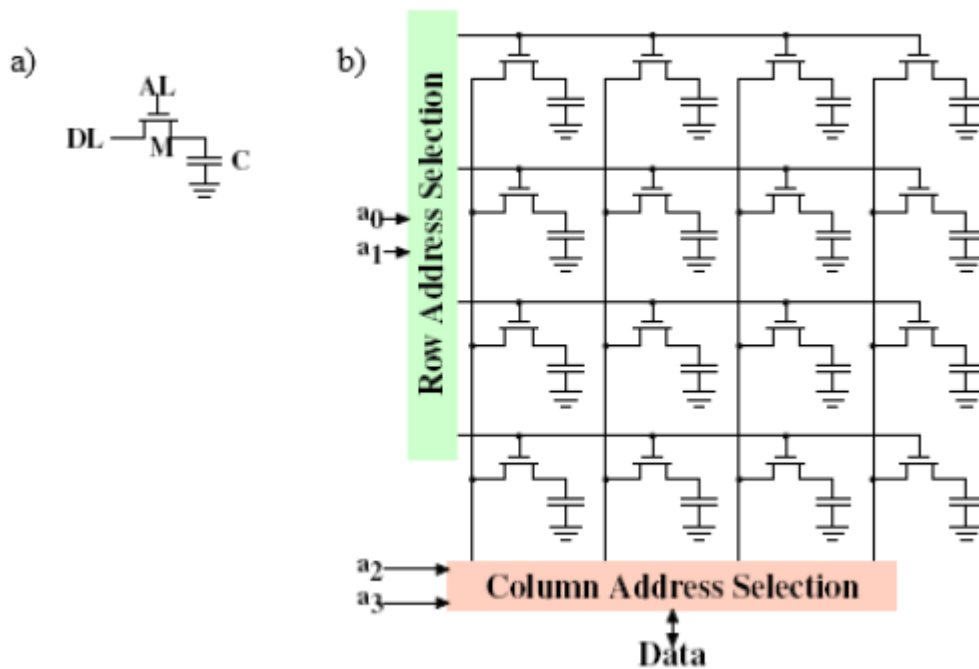
**Figure 2.1: 6-T SRAM cell [1].**

Static RAM provides faster access to data and is more expensive than DRAM. SRAM is used for a computer's cache memory and as part of the random access memory digital-to-analog converter on a video card [1-2].

A typical SRAM cell is made up of six MOSFETs as shown in Figure 2.1. Each bit in an SRAM is stored on four transistors (M1, M2, M3, and M4) that form two cross-coupled inverters. This storage cell has two stable states which are denoted by 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. In addition to such six-transistor (6T) SRAM, other kinds of SRAM chips use 4, 8, 10 (4T, 8T, 10T SRAM), or more transistors per bit. Four-transistor SRAM is quite common in stand-alone SRAM devices (as opposed to SRAM used for CPU caches).

## 2.2.2 DRAM

Dynamic random-access memory (DRAM) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated circuit. The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called 0 and 1 [1].



**Figure 2.2: a) DRAM cell and b) DRAM array organization [1].**

Since even "non-conducting" transistors always leak a small amount, the capacitors will slowly discharge, and the information eventually fades unless the capacitor charge is **refreshed** periodically. Because of this refresh requirement, it is a dynamic memory as opposed to **static random access memory** (SRAM) and other static types of memory. The main memory (the RAM) in personal computers is dynamic RAM (DRAM). It is the RAM in **desktops**, **laptops** and **workstation** computers as well as some of the RAM of **video game** consoles [2].

The advantage of DRAM is its structural simplicity: only one **transistor** and a capacitor are required per bit, compared to four or six transistors in SRAM. Figure 2.2 shows the DRAM cell and DRAM array organization. This allows DRAM to reach very high **densities**. Unlike **flash memory**, DRAM is a **volatile memory** (vs. **non-volatile memory**), since it loses its data quickly when power is removed. The transistors and capacitors used are extremely small; billions can fit on a single memory chip. Due to the nature of its **memory cells**, DRAM consumes relatively large amounts of power, with different ways for managing the power consumption [1].



### 2.1.3 Disk, Flash

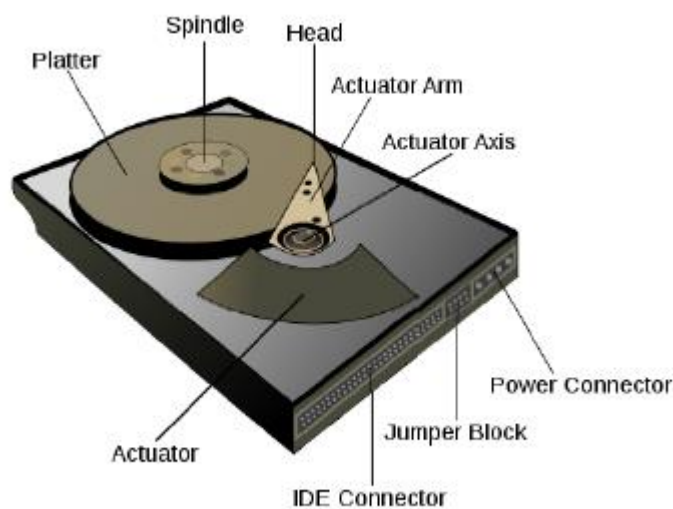
Beyond using data during computations, there are need to store data even when computers are turned off.

The requirements for persistent storage can be so described:

- It must be permanent, retaining data for several years without energy supply.
- It must be very dense, allowing the storage of huge amounts of data in a tiny space.
- Its cost/bit must be very low.
- It is acceptable for persistent storage to be slower than main memory (given that it is the last memory/storage hierarchy level).

#### Disk

The most common storage technology that matches these requirements is the Hard Disk Drive (HDD, or simply “disk”). Magnetic disks have been around since the 50s, and they have been for a long time the preponderant storage media. Most personal and enterprise computers employ disks as their persistent storage [1-4].



**Figure 2.3: Hard disk internals overview [1].**

HDDs exploit the properties of ferromagnetic materials to retain magnetic fields. A typical HDD as shown in Figure 2.3 has one or more disk platters with a magnetic coat. Data is read/write by a head device that can induce or sense magnetism in the disk. A central axis, called spindle, rotates the disk. Together with the actuator, which moves the head between the center and the border of the disk, all disk surfaces can be reached by the head. HDDs also have circuitry to convert disk data to electronic form and communicate with the computer's I/O subsystem [1].

Disks have great density (bits/square inch) and a very low cost/bit, and for this reason have been the most used persistent storage for a long time. Disks need less energy/bit than SRAM or DRAM, but their energy consumption too high for mobile and embedded devices, which require a small energy footprint. For this reason, disks are not the exclusive favored persistent storage technology today.

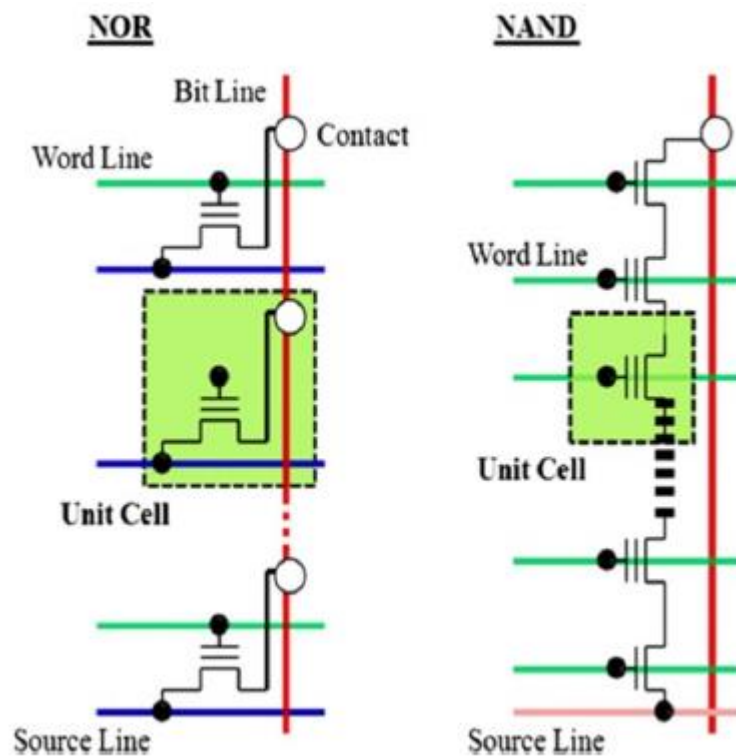
## **Flash Memory**

Flash memories, a type of non-volatile solid-state memory, have been built since the beginning of the 80s and dominate some niche markets today. Flash is more limited than disk regarding capacity and endurance, but has much lower power consumption and thus are very suitable for mobile and embedded devices [5-6]. It is primarily used in memory cards and flash drives for general storage and transfer of data between computers and other digital products. Flash cells are floating-gate devices that can be erased electrically and reprogrammed. There are two major kinds of flash memories: NOR and NAND as shown in Figure 2.4.

In NOR memory, each cell in a memory array is directly connected to the word-lines and bit-lines of the memory array. NAND memory devices are arranged in series within small blocks. Thus, while NAND flash can inherently be packed more densely than NOR flash, NOR flash offers significantly faster random access [5-9]. Due to cell density, NAND flash is the preferred type for persistent storage [10].

Depending on how the cells are organized in the matrix, it is possible to distinguish between NAND flash memories and NOR flash memories. In NOR flash, cells are connected in parallel to the bit lines, which notably allow the cells to be read and

programmed individually. The parallel connection of NOR Flash cells resemble the parallel connection of transistors in a CMOS NOR gate architecture. On the other hand, in NAND flash, the cells are connected in series, resembling a NAND gate. The series connections consume less space than the parallel ones, reducing the cost of NAND Flash. It does not, by itself, prevent NAND cells from being read and programmed individually.



**Figure 2.4: NOR flash array and NAND flash array architectures [5].**

Flash is faster than disk and consumes less energy. However, it has some drawbacks that prevent it from replacing disks except for some niche applications: less density, higher cost/bit and lowers endurance. It also cannot replace DRAM as main memory because of its low endurance and access times that are orders of magnitude slower [11].

Both disks and NAND flash are block devices. Typically they are not directly addressed by the processor, like main memory, but their contents must be moved from persistent storage to memory so the processor is able to manipulate them, and must be moved from memory to persistent storage at the end of processing. This process is not transparent to the processor, and is usually managed at operating.

## 2.2 Emerging Memory Technologies

There are several new Non-Volatile Memory (NVM) technologies under research. Most of these technologies are in different stages of maturity. Some of them are still in early research stages, others have working prototypes, and some of them are already entering into commercial manufacturing.

Here, we will introduce three of these technologies: Phase-Change RAM, Resistive RAM (including Memristors) and Magneto-resistive RAM (including Spin-Torque Transfer RAM).

### 2.2.1 Phase-Change RAM (PCRAM)

Phase-Change Random Access Memory (also called PCRAM, PRAM or PCM) is currently the most mature memory technology under research and one of the **non-volatile random-access memory** types. It can exist in two different phase states (e.g., crystalline and amorphous) [12-13]. The basic PCRAM cell structure is depicted in Figure 2.5.

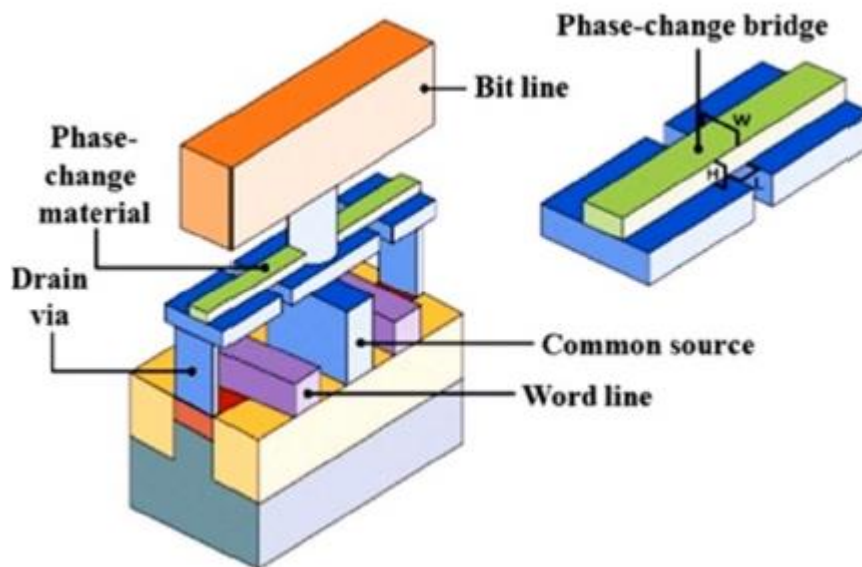


Figure 2.5: Basic PCRAM cell structure [12].

The two different phases with distinct properties:

- An amorphous phase, characterized by high electrical resistivity.
- A crystalline phase, characterized by low electrical resistivity [1].

The principle of phase-change memory is known since the 1960s, but only recent discoveries of phase-change materials with faster crystallization speeds led to the possibility of commercially feasible memory technology. The most important materials are chalcogenides such as  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  (GST), which can crystallize in less than 100 ns [12].

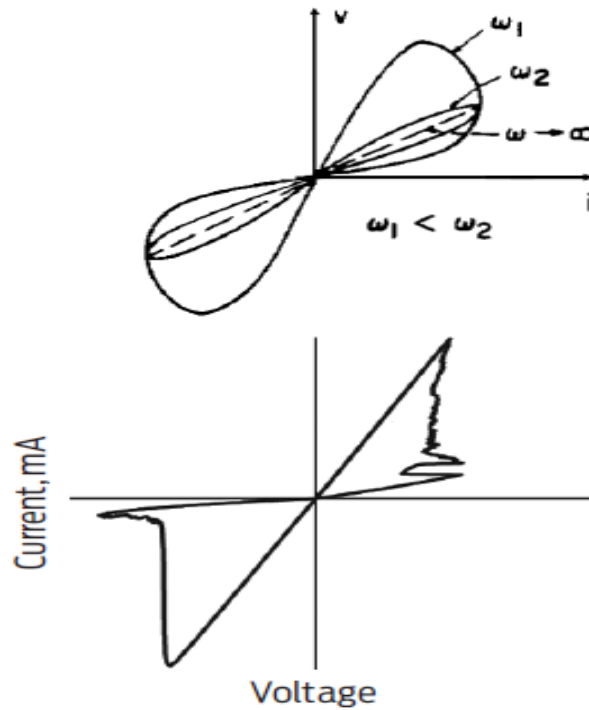
Today PCRAM is positioned as a flash replacement. It offers great advantages over Flash, but given the current limitations of access latency, energy consumption and endurance, further development is required in order to employ it as a replacement for DRAM [1].

## **2.2.2 Resistive RAM (RRAM)**

Resistive RAM (RRAM or ReRAM) has been applied to use resistance variations to store bit values. In this section we will concentrate our attention on the memristor, which is currently the most promising RRAM technology under research [14].

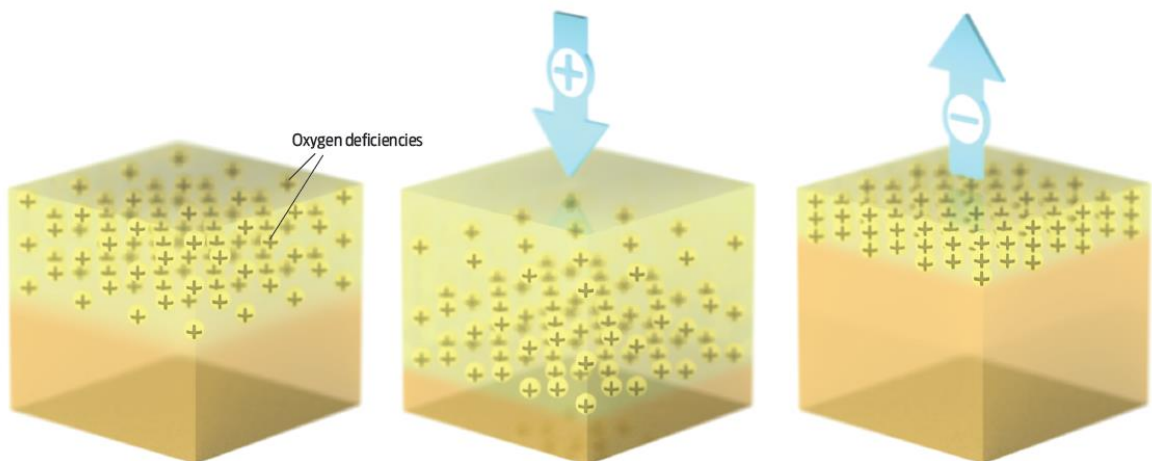
### **2.2.2.1 Memristor**

In 1971, Leon Chua theorized the existence of a fourth passive circuit element, which he called the memristor [15], as there were only three passive circuit elements, the resistor, the inductor and the capacitor. In 2008, a group of HP scientists reported the invention of a device that behaved as predicted for a memristor[16]. Later the same year, an article detailed how that device could be used to create nonvolatile memories [1]. The property of memristors particularly relevant to memory devices is the nonlinear relationship between current (I) and voltage (V), depicted on Figure 2.6.



**Figure 2.6: Relationship between current and voltage in a memristor [16].**

This memristor device consisted of a crossbar of platinum wires with titanium dioxide (TiO<sub>2</sub>) switches, as shown in Figure 2.7. Each switch consists of a lower layer of perfect titanium dioxide (TiO<sub>2</sub>), which is electrically insulating, and an upper layer of oxygen deficient titanium dioxide (TiO<sub>2-x</sub>), which is conductive. The size of each layer can be changed by applying voltage to the top electrode. If a positive voltage is applied, the TiO<sub>2-x</sub> layer thickness increases and the switch becomes conductive (ON state). A negative voltage has the opposite effect (OFF state) [16]. This behavior matches the hysteresis loop previously shown in Figure 2.6.

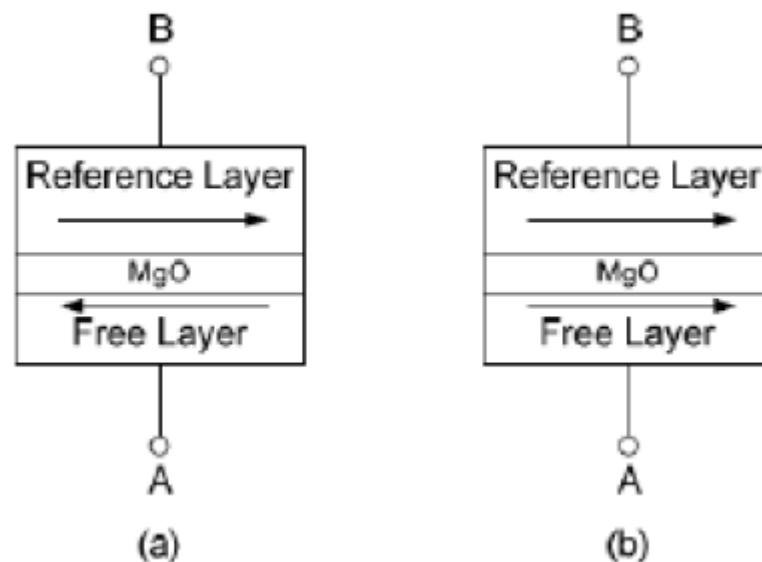


**Figure 2.7: The memristor under the electrical behavior [16].**

### 2.2.3 Magneto-resistive RAM (MRAM)

Magneto-resistive RAM (MRAM), sometimes called Magnetic RAM, is a memory technology that explores a component called Magnetic Tunnel Junction (MTJ).

An MTJ, depicted on Figure 2.8, consists of two ferromagnetic layers separated by an oxide tunnel barrier layer (e.g.,: MgO). One of the ferromagnetic layers, called the reference layer, keeps its magnetic direction fixed, while the other, called the free layer, can have its direction changed by means of either a magnetic field or a polarized current. When both the reference layer and the free layer have the same direction, the resistance of the MTJ is low. If they have different directions, the resistance is high. This phenomenon is known as Tunneling Magneto-Resistance (TMR) [17-20].



**Figure 2.8: A conceptual view of MTJ structure. (a) Anti-parallel (high resistance), which indicates “1” state; (b) Parallel (low resistance), which indicates “0” state [17].**

MRAM is a relatively mature technology, but current implementations suffer from density and energy constraints that seriously affect its capacity to compete with existing memory technologies such as DRAM or Flash. A specific type of MRAM under development called STT-RAM has a good chance to overcome these problems and position MRAM as a commercially feasible NVM alternative [17-21]. In the next section we'll explore STT-RAM in more detail.

### 2.2.3.1 STT-RAM

Spin-Torque Transfer (STT-RAM) technology tries to achieve better scalability by employing a different write mechanism based on spin polarization [21]. It is a new kind of magnetic RAM with the following features: fast read and write times, small cell sizes, potentially even smaller, and compatibility with existing DRAM and SRAM.

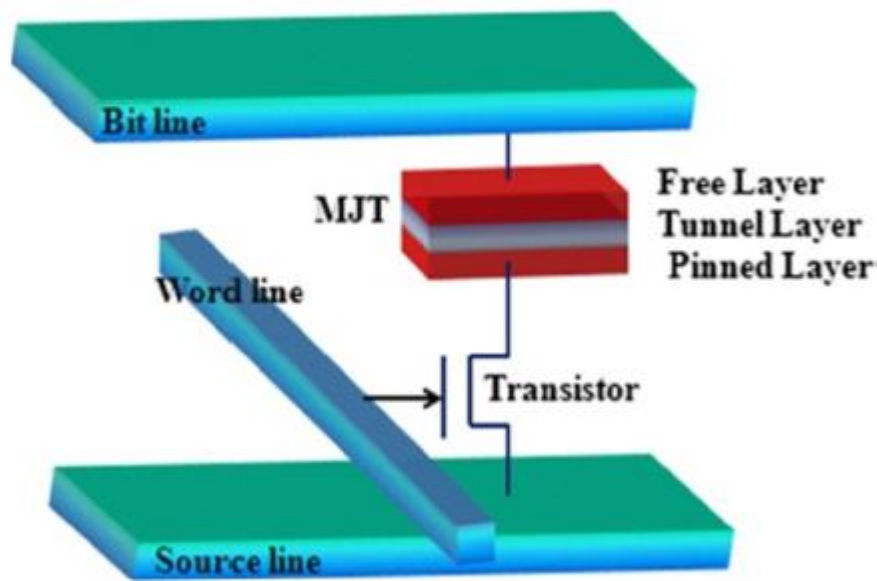


Figure 2.9: Basic STT-RAM cell structure [21].

MRAM stores data according to the magnetization direction of each bit and the nanoscopic magnetic fields set the bits in conventional MRAM. On the other hand, STT-MRAM uses spin-polarized currents, enabling smaller and less energy-consuming bits. The basic cell structure of STTRAM is depicted in Figure 2.9.

## 2.3 Comparison between Memory Technologies

We will now draw a comparison between the most promising NVM technologies as well as against the main current memory hierarchy components in table 1.



|                                 | Traditional Memories |      |                 |                 | Other Emerging Technologies |           |           | Redox      |
|---------------------------------|----------------------|------|-----------------|-----------------|-----------------------------|-----------|-----------|------------|
|                                 | DRAM                 | SRAM | NOR Flash       | NAND Flash      | FeRAM                       | MRAM      | PCRAM     | RRAM       |
| Cell Element                    | 1T1C                 | 6T   | 1T              | 1T              | 1T1C                        | 1(2)T1R   | 1T(D)1R   | (1D)(1T)1R |
| Feature Size (nm)               | 36-65                | 45   | 90              | 22              | 180                         | 65        | 45        | 9          |
| Density (Gbit/cm <sup>2</sup> ) | 0.8 - 13             | 0.4  | 1.2             | 52              | 0.14                        | 1.2       | 12        | 154-309    |
| Read Time (ns)                  | 2-10                 | 0.2  | 15              | 100             | 45                          | 35        | 12        | <50        |
| Write Time (ns)                 | 2-10                 | 0.2  | 10 <sup>7</sup> | 10 <sup>6</sup> | 65                          | 35        | 100       | 0.3        |
| Retention Time                  | 4-64 ms              | N/A  | 10 years        | 10 years        | 10 years                    | >10 years | >10 years | >10 years  |

**Table 2.1: Detailed comparison between memristor-based memory, traditional memories, and other emerging memories [1]. The abbreviations used are: T – transistor, C – capacitor, R – resistor, and D – diode [1].**

As a result, memristor-based memories are a good for replacing both the permanent and running storage. The current reading and writing speeds are slower than DRAM and SRAM, but are very fast compared to flash memories. These numbers show that memristors could easily replace flash memories, while further speed enhancement is required for replacing CMOS memories.

# Chapter 3

## The Memristor Device

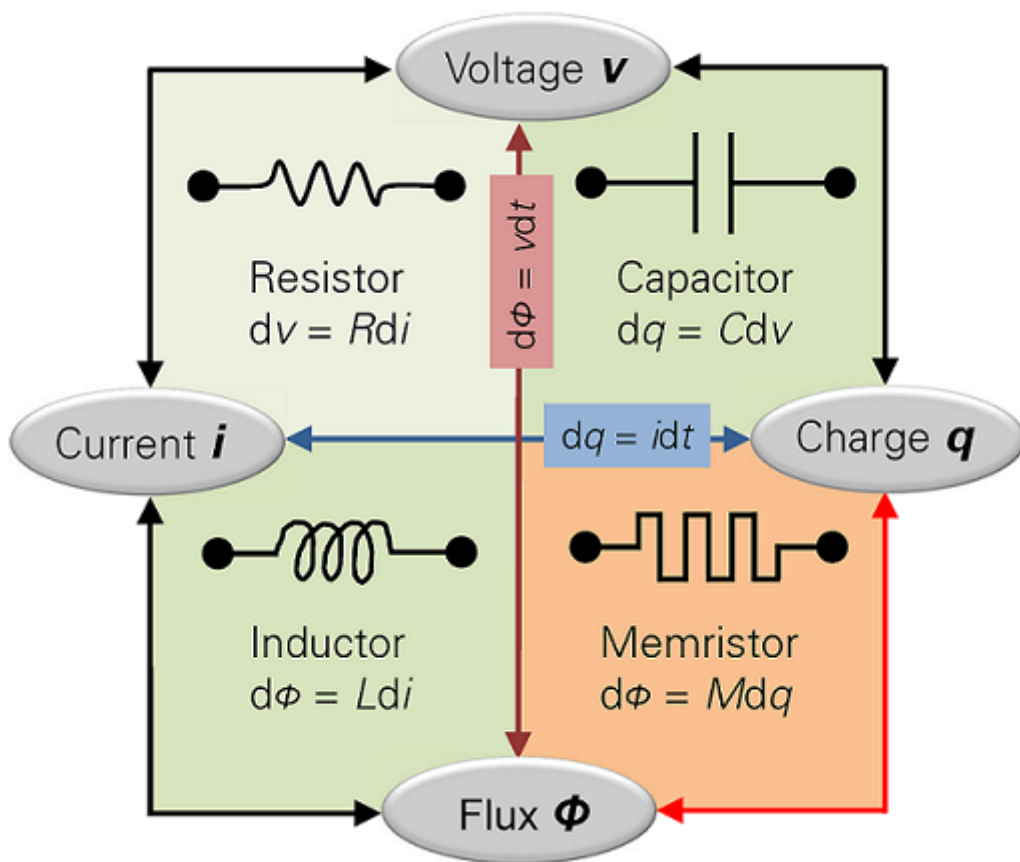
For over hundred years, three circuit elements have been considered the fundamental components of electrical circuit theory, due that every other electrical component could be expressed as the combination of these three. They refer to the capacitor (discovered in 1745), the resistor (1827) and the inductor (1831) [15] which are electrically described in Table 3.1.

| Known Fundamental Circuit Elements | Physical Descriptions  |
|------------------------------------|------------------------|
| Capacitance                        | $C = \frac{dq}{dv}$    |
| Resistance                         | $R = \frac{dv}{di}$    |
| Inductance                         | $L = \frac{d\phi}{di}$ |

**Table 3.1: Until recent years, the three fundamental circuit elements and their physical relationship [15].**

Forty years ago (in 1971), Leon Chua, a professor at the University of California Berkley, proposed the fourth fundamental circuit element, the memristor. In his findings, he demonstrated that this new device could not be described as a combination of the other fundamental electrical components suggesting that this new device should

be considered a fundamental element as well [16]. Chua based his reasoning in the relationship of the well know four circuit parameters, voltage ( $v$ ), current ( $i$ ), charge ( $q$ ) and magnetic flux ( $\phi$ ). Two physical laws relate these four components. The first one describe the current as function of charge and the second, Faraday's law, relates the voltage and the magnetic flux. Additionally, the three fundamental electric elements finalize the relationship of the four circuit parameters except for two of them, the charge and the magnetic flux. Chua predicted that, another fundamental circuit element existed and it related the magnetic flux to the charge with a simple relation. Figure 3.1 shows the four relations.



**Figure 3.1: The fourth fundamental circuit elements and their physical relationship [15].**

### 3.1 The Memristor Theory

Memristor (short for memory-resistor), relates the magnetic flux to the electric charge by changing its resistance as charges pass through it. By definition, a linear

memristor acts like a resistor. However, as the  $\phi$ - $q$  relation is nonlinear, the device behavior differs from that of a resistor. The main difference between a memristor and a resistor is that memristance is a function of charge, which depends on the hysteretic behavior of current/voltage profile [22]. By other words, memristance depends on the integral over the time of the applied stimuli on the device terminals.

Moreover, the memristor has the ability to retain the state for a long time after the current has been switched OFF. Due to its ability to remember past charges, an intuitive utilization for it is to be used in memory design [23].

Chua defined the charge-controlled memristor as follow [15]:

$$M(q) = d\phi / dq \quad (1)$$

$$v(t) = M(q(t)).i(t) \quad (2)$$

By using Faraday's Law,  $\phi = \int v(t)dt$ , and the current definition,  $i=dq/dt$ , the magnetic flux in the memristor can be re-written as:

$$\phi(q) = \int M(q(t)).i(t)dt = \int M(q(t)).dq \quad (3)$$

Now, the magnetic flux at any given time,  $t = t_0$ , can be calculated by [16]:

$$\phi(q) = \int M(q(t)).dq = \int_{q(t=-\infty)}^{q(t=t_0)} M(q(t))dt \quad (4)$$

The result, Equation 4, shows that the magnetic flux at a given time will depend on the history of the charge. In other words, the current behavior of this device is affected by the amount of charge that previously passed through it; this can be proven as a memory effect.

Memristors can be charge controlled or flux controlled depending on the biasing condition [10]. More specifically, when a memristor is connected to a current source, the current source injects charges through the memristor cell. It is convenient to treat

such a memristor as charge controlled because the state of the memristor changes according to the amount of charge injected, and the state causes memristance to change. On the other hand, when a voltage source is added across a memristor, it is natural to consider the memristor as flux controlled. In this case, the state of the memristor changes according to the amount of flux injection, and the state cause memristance to change. When the memristor state is controlled by the flux across the cell, it is described as follows [16]:

$$\phi = \frac{\phi_D}{R_{off}^2} [R_{off}^2 - R_{on}^2] \quad (5)$$

$$\phi_D = \frac{(\beta D)^2}{2\mu_v(\beta - 1)} \quad (6)$$

Where  $\beta$  denoted the  $R_{on} = \beta.R_{off}$  ratio,  $\mu_v$  is the mobility.

In 2008, Stanley Williams and his research team at the HP laboratories were able to fabricate a device that resembles Chua's description of a memristor [16, 22-25]. Williams' device consisted on two platinum electrodes separated by a stoichiometric titanium oxide un-doped layer ( $TiO_2$ ) and oxygen deficient layer of titanium oxide doped layer ( $TiO_{2-x}$ ) as shown in Figure 3.2.



**Figure 3.2: Memristor device structure presented by S. Williams and his research group at HP laboratories [16].**

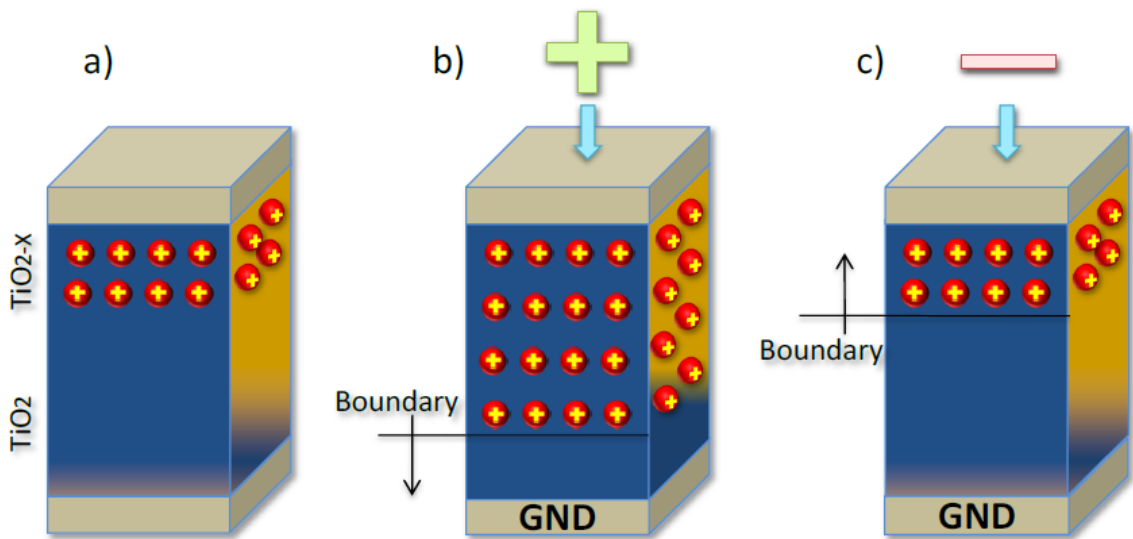
## 3.2 TiO<sub>2</sub> Memristor Working and Operation

It is well known that transition metal oxides can also act as semiconductors [22-25], this includes pure titanium oxide. Similarly than other semiconductors, it offers high resistivity in its intrinsic state. However, it can be doped to increase its electrical conductivity like other semiconductor. In this case, the titanium oxide can be doped by intentionally reducing the ratio of oxygen from its stoichiometric form.

The un-doped layer consists of stoichiometric titanium oxide with an oxygen-to-titanium ratio of 2-1,[16] thus there are hardly any chances for oxygen atoms to move randomly, which leads to relatively poor conductivity. The doped layer consists of titanium oxide with oxygen vacancies and an oxygen-to-titanium ratio from 2-x to 1. Such a ratio indicates that oxygen element is deficient compared with in the un-doped layer, so the doped layer has better conductivity, which is because there are charged oxygen vacancies that act as dopants and could move randomly inside.

The negatively charged atom of oxygen is removed from the TiO<sub>2</sub> molecule, a positive ion is formed due to the overall deficiency of electrons left in the molecule. As a result, oxygen vacancies can be assumed to be positive charged ions (Vo<sup>2+</sup>) that can act as electron donors [16, 26].

Taking the doping created by oxygen vacancy in consideration allows identifying a highly resistive layer of un-doped TiO<sub>2</sub> and a highly conductive layer of doped titanium oxide (TiO<sub>2-x</sub>) in the device fabricated by HP's team. However, differently from semiconductors such as silicon where the ionized doping atoms will remain immobile in the lattice structure of the semiconductor, oxygen vacancies in TiO<sub>2</sub> can drift in direction of the current when an electric field is applied [16, 26].



**Figure 3.3:** a) Oxygen vacancies in the  $\text{TiO}_{2-x}$  can be considered as positive charges. b) When a positive potential is applied to the  $\text{TiO}_{2-x}$  side these positive charges are repelled towards the  $\text{TiO}_2$  layer, c) while the opposite happens if a negative potential is applied instead. In other words, the memristor's oxygen vacancies ion drift is possible when applying a voltage potential to its electrodes [16].

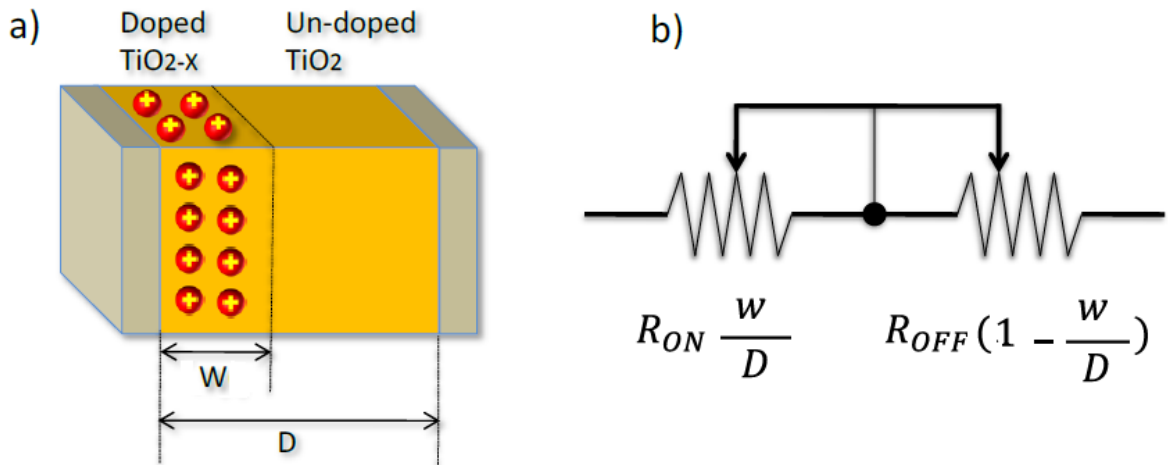
Figure 3.3 shows that if a positive potential is applied to the vacancy rich  $\text{TiO}_{2-x}$  layer respect to the un-doped  $\text{TiO}_2$ , then the positively charged oxygen-vacancy ions will be repelled and will begin to drift towards the un-doped  $\text{TiO}_2$  effectively shifting the  $\text{TiO}_{2-x}/\text{TiO}_2$  boundary reducing the thickness of the  $\text{TiO}_2$  layer.

As a result, the overall device will become more conductive. In the other hand if a negative potential is applied to the  $\text{TiO}_{2-x}$  layer, the oxygen vacancies will be attracted back to the  $\text{TiO}_{2-x}$  shifting the  $\text{TiO}_{2-x}/\text{TiO}_2$  boundary in the opposite direction increasing the thickness of the un-doped  $\text{TiO}_2$ . The result is a device with a lower overall conductivity.

### 3.3 TiO<sub>2</sub> Memristor Physical Model

HP TiO<sub>2</sub> memristor is a thin film sandwiched between two metallic contacts (Figure 3.4 a) [16]. The memristor symbol is also portrayed in Figure 3.4 b. The memristor is a very small (nano-scale) device that can be split into two main parts: I) a high doped region with low resistance ( $R_{on}$ ), and II) a low doped region with high resistance ( $R_{off}$ ). The high doped region consists of TiO<sub>2-x</sub>; however Low doped region consists mostly of TiO<sub>2</sub>. The high doped region contains more oxygen vacancies which makes its resistance less than that of the low doped region.  $R_{on}$  and  $R_{off}$  notations represent the high doped and low doped regions respectively [16, 22-26].

The memristor has the ability to retain the state for a long time after the current has been switched OFF. Due to its ability to remember past charges, an intuitive utilization for it is to be used in memory design. Memristor shows many promising characteristics as the next-generation data storage device, such as non-volatility, low power consumption, high performance, high density and excellent scalability [22-26].

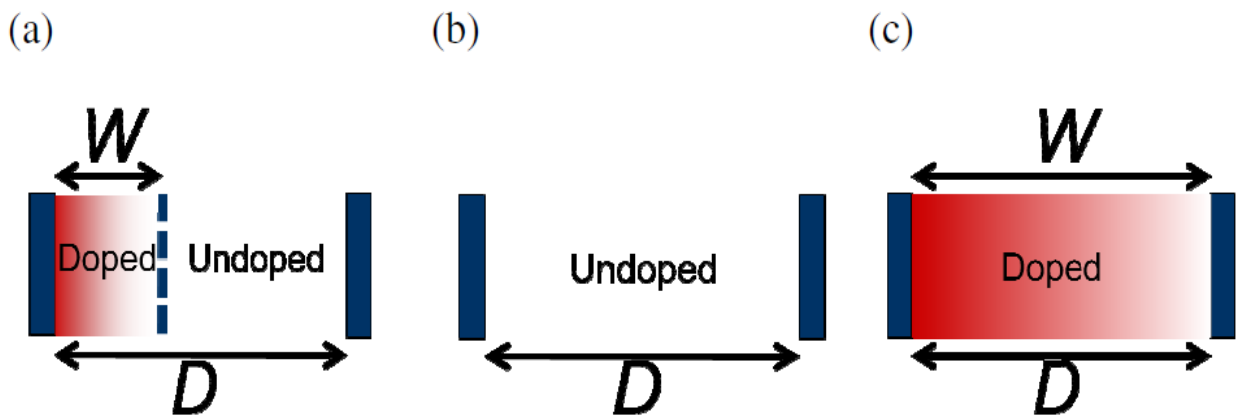


**Figure 3.4: physical model HP (TiO<sub>2</sub> thin-film memristor). (a) Structure, and (b) equivalent circuit [16].**

The semiconductor thin film has a certain length  $D$ , and the state variable  $w$  represents the width of the doped region (TiO<sub>2-x</sub> layer) the doped region which has low



resistance while that of the un-doped region is much higher [27]. As an external voltage bias is applied across the device, the electric field repels positively charged oxygen vacancies in the doped layer into the pure TiO<sub>2</sub> layer; the result is the length  $w$ . Hence, the device's total resistivity changes. If the doped region extends to the full length, that is  $w/D=1$ , the total resistivity of the device is dominated by the low resistivity region, with a value measured to be  $R_{on}$  as shown in figure 3.5.b. Likewise, when the un-doped region extends to the full length  $D$ ,  $w/D=0$ , the total resistance is denoted as  $R_{off}$  shown in figure 3.5 c.



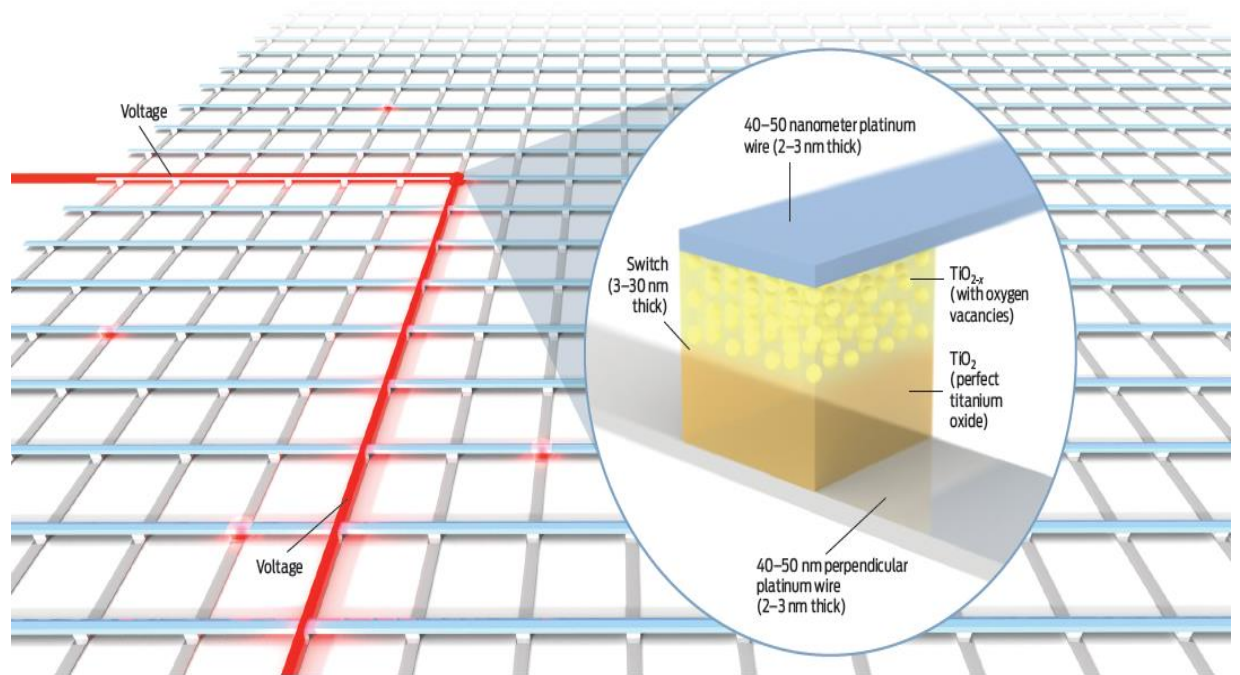
**Figure 3.5: Figure showing ideal memristor behavior. OFF and ON states shown by (b) and (c) respectively. The operation between states is illustrated in (a) [27].**

According to [15], the memristor has memory effect since the device maintains its resistivity even if the power goes off. According to the reported device characteristics [15], oxygen vacancies do not move around by themselves. They become absolutely immobile until voltage is applied again. This unique characteristic makes the memristor stand out from other devices such as diode. The mathematical model for memristive device memristance  $M$  can be described as [16]:

$$M = (R_{on} \cdot w / D + R_{off} \cdot (1 - w / D)) \quad (8)$$

### 3.4 TiO<sub>2</sub> Memristor Fabrication Process

A TiO<sub>2</sub> memristor can be made from any Metal Insulator Metal (MIM) sandwich which exhibits a bipolar switching characteristic. This suggests that TiO<sub>2</sub> is not the only material to fit the criteria for a memristor, and there has been a few papers published on the fabrication and properties of memristors fabricated using other materials. Even if the same materials are used, there are different methods of fabricating memristors. So far the most common methods are nano-imprint lithography (NIL) and atomic-layer deposition (ALD). Both of these processes require an annealing step at high temperature and a forming voltage [28-34].



**Figure 3.6: TiO<sub>2</sub> Memristor device architecture presented by S. Williams and his research group at HP Laboratories [16].**

One such paper by Stewart et al. [34] explores the possibility of using an organic monolayer as the switching medium to realize a memristor shown in figure 3.6. It had split itself up into two chemically different layers. Adjacent to the molecules, the oxide was stoichiometric TiO<sub>2</sub>, meaning the ratio of oxygen to titanium was perfect, exactly 2 to 1. But closer to the top platinum electrode, the titanium dioxide was

missing a tiny amount of its oxygen, between 2 and 3 percent. We called this oxygen-deficient titanium dioxide  $\text{TiO}_{2-x}$ , where  $x$  is about 0.05.

**THE SWITCH:** A switch is a 40-nanometer cube of titanium dioxide ( $\text{TiO}_2$ ) in two layers: The lower  $\text{TiO}_2$  layer has a perfect 2:1 oxygen-to-titanium ratio, making it an insulator. By contrast, the upper  $\text{TiO}_2$  layer is missing 0.5 percent of its oxygen ( $\text{TiO}_{2-x}$ ), so  $x$  is about 0.05. The vacancies make the  $\text{TiO}_{2-x}$  material metallic and conductive.

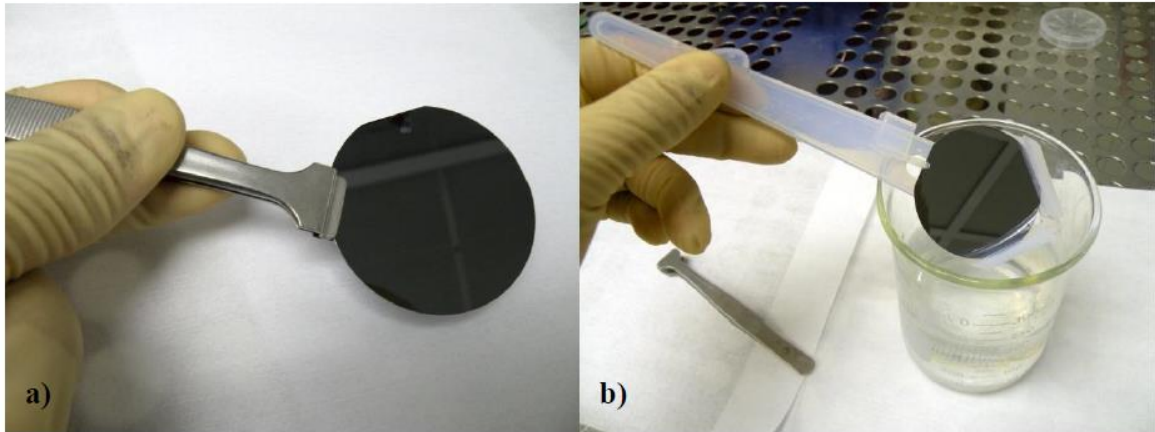
**THE CROSSBAR ARCHITECTURE:** The crossbar architecture is a fully connected mesh of perpendicular wires. Any two crossing wires are connected by a switch. To close the switch, a positive voltage is applied across the two wires to be connected. To open the switch, the voltage is reversed [16].

Also, there was another fabrication process additional to the one from HP. This fabrication process was developed by using standard fabrication techniques in order to ensure that current fabrication technology can be used to fabricate these memristor devices. However, some fabrication steps were not yet optimized for mass production but for research purposes.

### 3.4.1 Selection of the Substrate

The process begins by selecting the appropriate substrate; in this case, the substrate will serve as structural support only. Since, silicon wafer are the standard substrate used in CMOS fabrication, a blank silicon wafer was selected in this case; however other materials could also be explored. The silicon wafers used during this process had a diameter of 50mm and a thickness of 525 $\mu\text{m}$ . See Figure 3.7. These wafers were scribed and labeled for identification purposes.

These wafers were cleaned by deep submersion in a solution of Hydrofluoric acid (HF) diluted in distilled (DI) water to  $\text{H}_2\text{O}:\text{HF}$  ratio of 50:1, for 10 seconds followed by two minutes of DI water rinsing, in order to ensure that these wafers were free of any contaminant that could affect the fabrication results. See Figure 3.7.



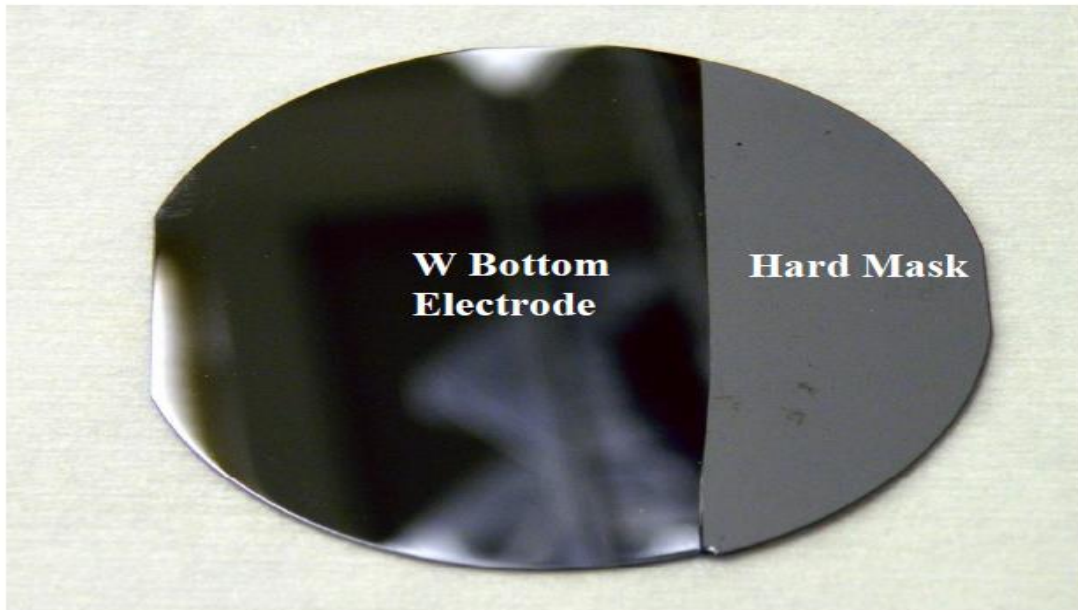
**Figure 3.7:** a) Silicon wafers with a 50mm diameter were used as substrates. b) The wafers were cleaned by deep submersion in a H<sub>2</sub>O: HF solution with 50:1 ratio [32].

### 3.4.2 Bottom Electrode

While looking for a reduction in fabrication costs, both the bottom and top electrodes of these devices were made using **Tungsten (W)** rather than **Platinum (Pt)** like the devices fabricated by HP, offering a similar interface than the one obtained with titanium while reducing the material cost.

The bottom electrode consisted in a Tungsten layer with a thickness of 1000Å. This layer was deposited over the entire silicon wafer by using RF magnetron sputtering. The thickness of this layer was controlled by calculating the deposition time with a previous characterization of the deposition rate of this material under a pressure of 5mTorr, a temperature of 19°C and a RF magnetron power of 100W.

In order to reach the bottom electrode of these sample memristor devices, it was needed to hard-mask a section of the bottom electrode with the intention that no other material could cover it in further fabrication steps allowing us to make electrical contact to this electrode. As it was mentioned before, this step was not intended for mass production but as an easy way to prototype the sample device and serve as a proof of concept. The hard masking of the device was done by covering a section of the wafer and its bottom electrode with a smaller piece of another silicon wafer, as shown in Figure 3.8. This piece of wafer was mechanically attached to the substrate before beginning the next fabrication steps.



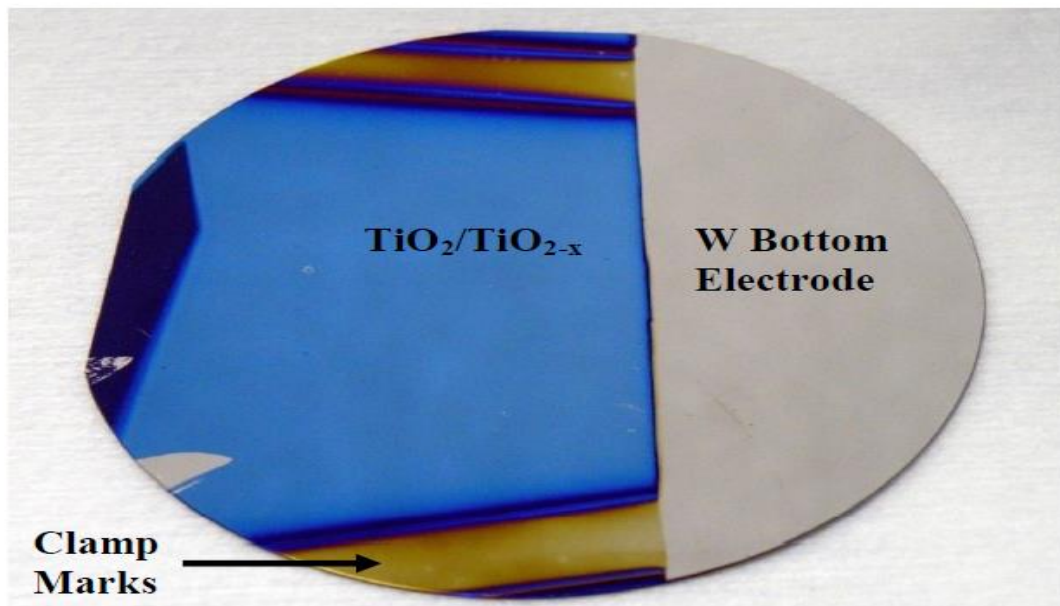
**Figure 3.8:** A piece of silicon wafer was used to hard mask part of the tungsten bottom contact in order to avoid any other material to deposit in one section of the back contact allowing us to reach the back electrode for future electrical characterization [32].

### **3.4.3 Oxygen Incomplete Titanium Oxide Layer ( $\text{TiO}_{2-x}$ )**

The Oxygen Incomplete Titanium Oxide Layer was obtained by reactive sputtering of titanium in oxygen ambient. A titanium target was used for the sputtering process which was done while infusing a gas mixture of 11% oxygen to argon ratio into the sputtering chamber. During the deposition, the temperature was maintained constant at 300°C in order to allow the titanium to react with oxygen and oxidize while being deposited over the previous tungsten bottom electrode and hard masking. Using a low oxygen flow rate (1.2sccm) allowed the formation of titanium oxide with lower oxygen concentration than titanium dioxide. As a result, oxygen deficient titanium oxide ( $\text{TiO}_{2-x}$ ) is obtained. The deposition time required for depositing the 1100Å thick  $\text{TiO}_{2-x}$  layer was calculated by using a previously characterized deposition rate of this material under a pressure of 5mTorr, a temperature of 300°C and a RF magnetron power of 200W.

### 3.4.4 Titanium Dioxide Layer (TiO<sub>2</sub>)

Similarly than the TiO<sub>2-x</sub> deposition, a 240Å thick TiO<sub>2</sub> layer was also deposited by reactive sputtering of titanium in oxygen ambient. However, a richer concentration of oxygen was used in this case. A 25% of oxygen to argon ratio was injected into the sputtering chamber while keeping a constant temperature of 300°C. The higher oxygen flow rate (2.4sccm) allowed for complete oxidation of titanium, forming TiO<sub>2</sub>. This layer was deposited in top of the previous oxygen deficient titanium oxide layer and the hard masking as shown in Figure 3.9. It is important to notice that the order of deposition, TiO<sub>2</sub> in top of TiO<sub>2-x</sub> and not in the opposite way, was decided to protect the TiO<sub>2-x</sub> layer from the further oxidation that could happen if TiO<sub>2-x</sub> is exposed to the air.



**Figure 3.9:** The TiO<sub>2</sub> and TiO<sub>2-x</sub> layers can be observed as the bluish section of the wafer, while the hard masked tungsten remained accessible without any material deposited in top. Marks of the claps used to attach the hard mask are also visible [32].

### 3.4.5 Top Electrode

The top electrode patterns are used to define the area of the device and to separate individual devices in the same wafer. The pattern was selected to be squares electrodes with side length of 200, 100, 50 and 25µm. The patterning technique selected for this device fabrication was lift-off, where a metal layer is used to cover a patterned photo-

resist layer and when the photo-resist is removed only the metal with the shape of the electrodes remain. In the other hand, the etching technique use an etching agent to react with the metal electrode in order to remove it in the areas where metal is undesired. If etching is to be used, the etching agent has to be carefully selected to etch only the metal used for the electrodes while not reacting with the  $\text{TiO}_2$  below the electrodes.

In order to design a simple fabrication process, the lift-off process was favored over the etching technique. Commonly, substrates tend to capture few molecules of water from the humidity in the air. When photo-resist is used in top of these wafers, it will bond to the water molecules instead of the substrate reducing its ability to adhere to the wafers. As a result, poor patterning definition will be obtained [35]. Furthermore, our patterning process began by performing a pre-bake of the wafer in order to remove any humidity that could affect the photo-resist development. The prebake was performed with a digital hot plate. The substrate was heated to a constant temperature of  $115^\circ\text{C}$  for a period of 5 minutes. Afterwards, the sample was allowed to cool at room temperature for another 5 minutes.

Right after the substrate cool-down, the substrate was covered with Hexamethyldisilazane (HMDS) primer. This chemical compound bounds directly to the wafer substrate sealing the surface and avoiding the capture of water molecules. HMDS was deposited by spin coating. The spin coat was performed with an initial speed of 300rpm for five seconds to spread the compound along the surface and later the speed was increased to 3000rpm for a period of 30s to eliminate the excess of HMDS in the surface.

Following the HMDS application, the deposition of photo-resist S1813 was perform also by spin coating. In this case, the initial speed was set to 500rpm for 10s to spread the photo-resist along the substrate surface and later increased to 4000rpm for 60s to eliminate the excess of photo-resist and obtain the desired photo-resist thickness.

Another factor to consider during patterning is that the solvent used in the photo-resist makes the photo-resist less sensible to the ultraviolet light used for photolithography [35]. To avoid poor patterning due to excess of solvent, the substrate covered with photo-resist was soft baked in order to dry it removing any solvent left in it. The soft



bake was performed in the digital hot plate used previously, where the substrate and photo-resist were heated to 115°C for one minute. The photolithography process was performed by applying an ultraviolet (UV) light with an intensity of 20mW/cm<sup>2</sup>. Since a negative photo-resist was used, the areas that were exposed to light will harden. While the un-exposed regions will not allowing us to remove the unexposed regions in the following developing process. The (UV) exposure was done through a mask that contained the patterns that was intended to create in the top electrodes while covering the region reserved for the back electrode contact. This mask was previously designed in order to create several devices in a 4 inches wafer. However, in this case only the portion that contains the metal-insulator-metal (MIM) capacitor electrodes are used since there is no difference between these electrodes and the ones needed for the basic sample memristor.

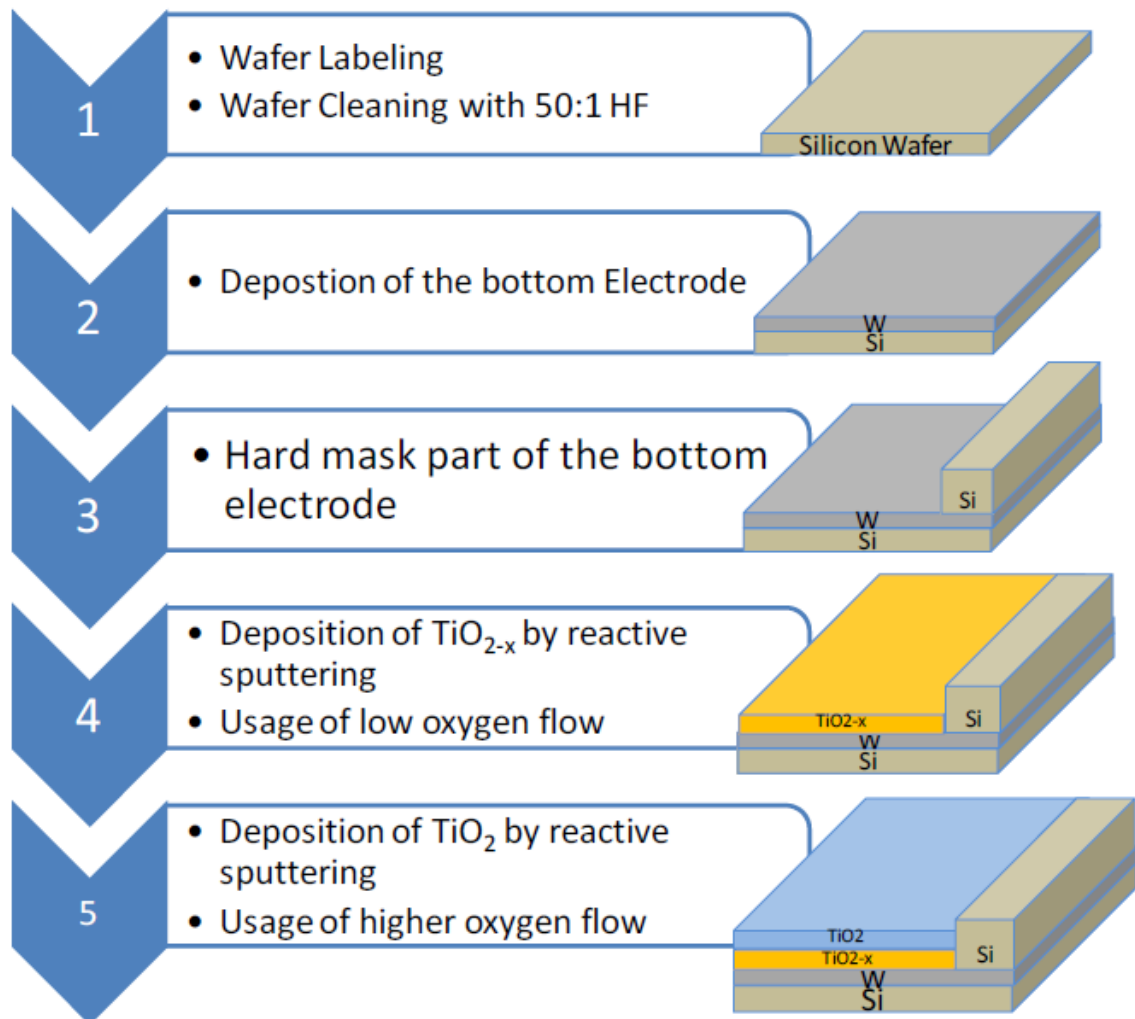
After transferring the pattern form the mask to the photo-resist by UV exposure, the undesired areas of photo-resist was removed in the photo-resist development process. This development process was performed by submerging the entire wafer in a photo-resist developer MF-319 for a period of one minute while applying gentle agitations to remove the un-exposed photo-resist.

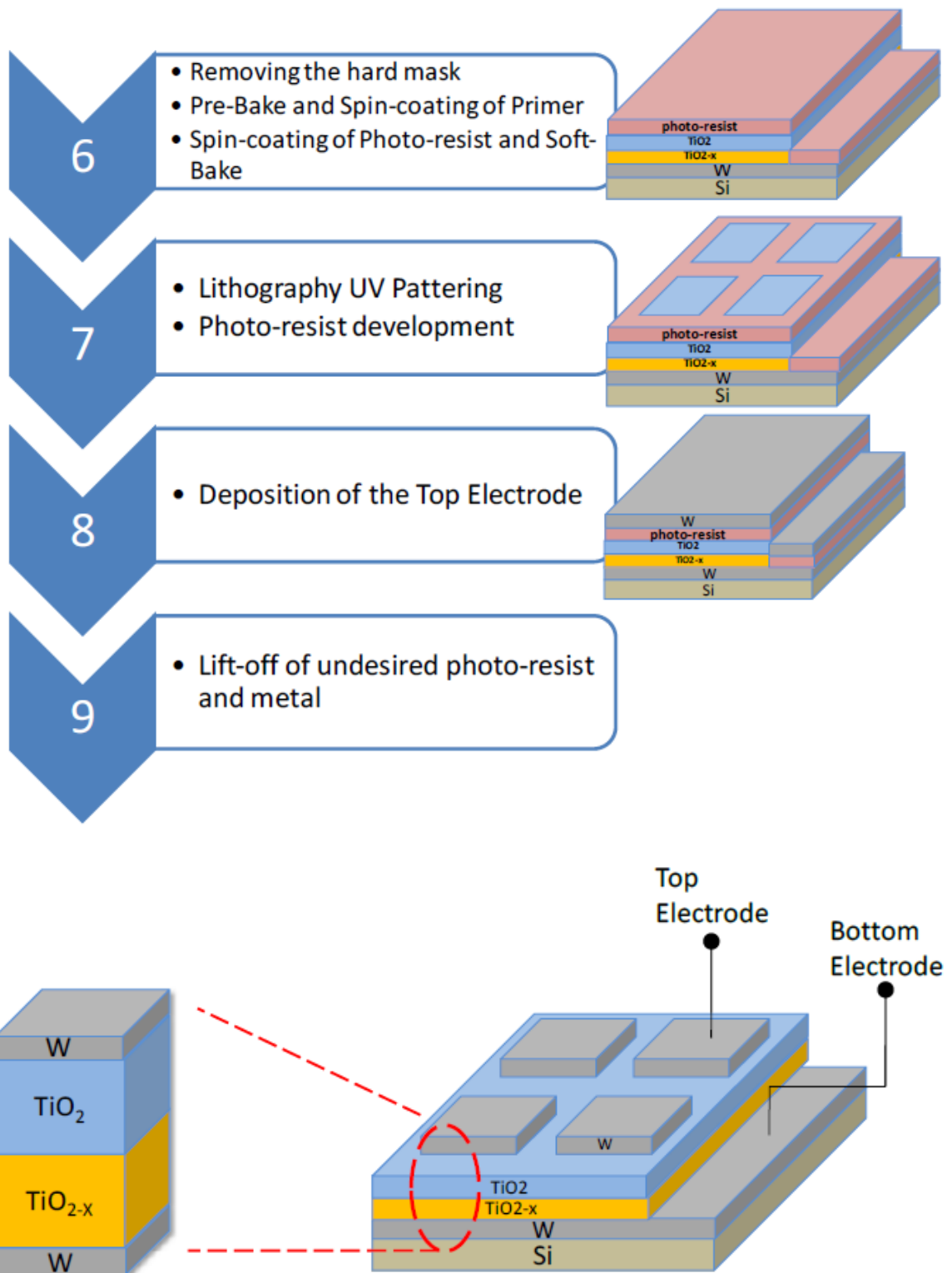
Once the surface of the substrate contained only the desired negative photo resist patterns, the top electrodes were created by depositing a tungsten layer with a thickness of 1000Å, using the same RF magnetron sputtering parameters used to deposit the bottom electrode. Subsequently, the electrode patterns were produced by the lift-off of the tungsten that was in top of the un-exposed areas of photo-resist. The lift-off process was carried by submerging the wafer in a potent solvent stripper called PG remover for a period of one minute without agitation followed by 9 minutes of ultrasonic agitation. Finally, a visual inspection was performed by using an optical microscope with a 10-x magnification in order to ensure that the memristors' top electrodes were developed correctly. The electrodes can have different square side lengths such that, 200, 100, 50 and 25µm.



### 3.4.6 Overview of the Fabrication Process

However, a brief chronological overview of the fabrication process is presented in this section with the intention of facilitate the understanding of the entire fabrication process by visual means. See Figure 3.10.



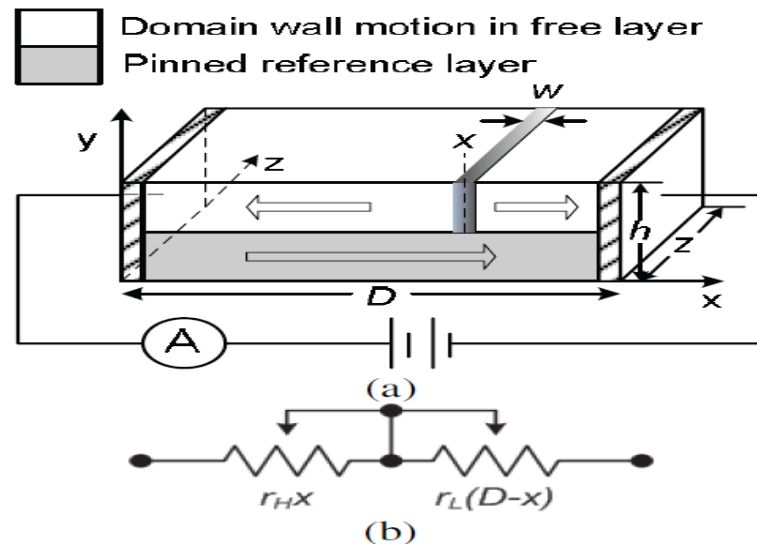


**Figure 3.10: Overview of the developed fabrication process for the basic TiO<sub>2</sub> memristor devices [32].**

### 3.4 Spintronic Memristor Fundamentals

Beside the solid-state device, magnetic technology provides other possible solutions to build a memristive system [36]. Three spintronic memristor structures have been proposed in [3]. They are spin valve with spin-torque-induced domain-wall motion in the free layer, MTJ (magnetic tunneling junction) with spin-torque-induced magnetization switching, and thin film element with spin-torque-induced domain-wall motion. Compared to the solid-state thin film device [37], the behavior of a spintronic memristor, e.g., the relationship between the memristance and the current through the memristor, can be controlled more flexibly. Also, the technology to integrate magnetic device on the top of CMOS device has become mature in the development of magnetic memory [38].

Among all spintronic memristive structures proposed in [36-38], the spin valve memristor with spin-torque-induced domain wall motion could be the most promising one for its simplest structure. In fact, the fabrication process of such spintronic memristors is similar to the mature technology that was used to manufacture the spin valve based GMR (Giant Magneto resistance) head in a hard disk drive [39]. Hence, we choose it as the objective of this research work.



**Figure 3.11: A spintronic memristor based on magnetic-domain-wall motion. (a) Structure. (b) Equivalent circuit [36].**

Figure 3.11(a) illustrates the structure of the spin-torque induced domain-wall motion based memristor [40]. Its basic structure is a long spin-valve strip, which consists of two ferromagnetic layers called reference layer and free layer, respectively. The magnetization direction of reference layer is fixed all the time by coupling to a pinned magnetic layer (called pin layer). The free layer is divided into two segments by a domain-wall: one segment has the parallel magnetization direction to the reference layer, while another segment's magnetization direction is anti-parallel to the reference layer. The domain wall in the free layer could be moved by the spin polarized current [36].

The resistance per unit length of each segment is determined by the relative magnetic directions of free layer and reference layer: when the magnetization direction of the free layer in a segment is parallel (anti-parallel) to the reference layer, the resistance per unit length of the segment is at its low (high) state [36].

We could use  $r_L$  and  $r_H$  to denote the spin-valve strip is at its low- or high-resistance states, respectively. Figure 4.1(b) shows the simplified equivalent circuit model of the spin-torque-induced domain-wall motion based memristor. The memristance of such a spintronic memristor can be expressed as [36]:

$$M(x) = [r_L \cdot \alpha + r_H \cdot (1 - \alpha)] \quad (9)$$

Which,  $\alpha = x/D$ , here  $x$  is the position of domain-wall and  $D$  is the length of the device, as shown in Figure 3.11(a). In Eq. (9), we assume the width of domain wall is negligible compared to the length of the device. Hence, the impact of the domain wall on overall memristance can be ignored.

### 3.5 Electrical Property of Spintronic Memristor

The domain wall movement in the spintronic memristor happens only when the applied current density ( $J$ ) is above the critical current density ( $J_{cr}$ ) [36-41]. But, how fast the domain-wall can move mainly relies on the strength of spin-current applied on

it. More precisely, the domain-wall velocity  $v$  is proportional to the current density  $J$  [41], as

$$v = \frac{dx}{dt} = \Gamma_v \cdot J. \quad (10)$$

$\Gamma_v$  is domain wall velocity coefficient, which is related to device structure and material property.

In other words,  $\Gamma_v = 0$  when  $J < J_{cr}$ . As we will show later,  $J_{cr}$  is determined by many factors and varies from device to device.

When reading the memristance of a spintronic memristor, a small sensing current ( $I_{rd}$ ) can be applied to the device. The value of memristance is read out by measuring the voltage drop across the memristor. As long as the read current density  $J_{rd}$  is below  $J_{cr}$ , the state of the spintronic memristor will not be disturbed.

### 3.5.1 Current density $J$ and effective current density $J_{eff}$

The current density  $J$  in a spintronic memristor can be calculated as [36]:

$$J = \frac{V}{M(X) \cdot h \cdot z}. \quad (11)$$

Where  $V$  is the voltage applied to the spintronic memristor.  $h$  and  $z$  are the thickness and the width of spin-valve strip, respectively. The effective current density  $J_{eff}$  of a spintronic memristor can be calculated as [36]:

$$J_{eff} = \begin{cases} J, & \text{when } J > J_{cr} \\ 0, & \text{when } J < J_{cr} \end{cases}. \quad (12)$$

### 3.5.2 Critical current density $J_{cr}$

Theoretically, the critical current density  $J_{cr}$  is a material related parameter, which can be calculated by [36-41]:

$$J = \frac{\alpha \cdot \gamma \cdot H_p \cdot e \cdot M_s}{P \cdot \mu_B} \cdot \sqrt{\frac{2A}{M_s \cdot H_k}} \quad (13)$$

Here,  $H_p$  is the hard anisotropy in the direction perpendicular to the thin film plane (y direction),  $H_k$  is the easy anisotropy in the strip direction (x direction),  $A$  is exchange parameter,  $\alpha$  is damping parameter, and  $\gamma$  is gyromagnetic ratio. However, the theoretical calculation of  $J_{cr}$  cannot explain all experimental measurements [41]. Therefore,  $J_{cr}$  is usually considered as an intrinsic electrical parameter that is directly obtained from the experimental calibration.

### 3.5.3 Domain wall velocity coefficient $\Gamma_v$

Domain wall velocity coefficient  $\Gamma_v$  is an electrical parameter to describe how fast the domain wall can move [36].

$$\Gamma_v = \frac{P \cdot \mu_B}{e \cdot M_s} \quad (14)$$

Instead of calculating  $\Gamma_v$ , usually people get this parameter directly from measurement.

## 3.6 Compact Model of Spintronic Memristor

The proposed a compact model of the spin valve memristor with spin-torque-induced domain-wall motion, including two main equations:

### 3.6.1 Spintronic Memristance

By considering the contribution of domain wall, the memristance of a spintronic memristor can be expressed as a function of domain wall position  $x$  as[36-38]:

$$M(x) = [r_L \cdot (x/D) + r_H \cdot (1-x/D)], \quad (15)$$

where  $w$  is the width of domain wall and  $D$  is the spintronic thickness.

for  $0 < x < D$ . Here  $M(x)$  does not depend on the width of domain wall. We note that such an assumption of the domain wall resistance is close to the physical phenomena and incurs very marginal error in the calculation of memristance [36-41].

### 3.6.2 Spintronic Resistance

Memristor is a two-terminal device that can be modeled as a time-varying resistor in a circuit. The upper- and lower bounds of resistance are two important electrical properties of spintronic memristor. The resistance of the thin film strip in the spintronic memristor is determined by the relative magnetic directions of free layer and reference layer. We denote the square sheet resistances of the spintronic memristor when the magnetic directions of the two ferromagnetic layers are antiparallel or parallel as  $r_H$  and  $r_L$ , respectively. A common parameter to represent the difference between  $r_H$  and  $r_L$  is GMR ratio, which is defined as [39]:

$$GMR = \frac{r_H - r_L}{r_L} \quad (16)$$

Low resistance  $r_L$  is determined by the resistivity ( $\rho$ ) of the thin-film strip at the low resistance state and the thickness ( $h$ ) as [36]:

$$r_L = \rho/h \quad (17)$$

$\rho$  can be considered as an intrinsic electrical parameter that is determined by the device structure and material property only. The high and low resistance per unit length of spintronic device  $r_H$  and  $r_L$  can be then calculated by [36-41]:

### 3.6.3 Domain wall position $x$

The domain wall position  $x$  can be calculated by the integral of the domain wall velocity  $v$  over time  $t$  as [36]:

$$x = \int_0^t v \cdot dt \quad (18)$$

As we explained in Section 4.2, the domain wall velocity  $v$  is proportional to the current density  $J$  and it can move only when  $J$  is bigger than  $J_{cr}$  [36-41]. Therefore,  $v$  is proportional to the effective current density  $J_{eff}$ :

$$v = \Gamma_v \cdot J_{eff} \quad (19)$$

By combining Eq. (9) and (10), the domain wall position  $x$  can be calculated as:

$$x = \Gamma_v \int_0^t J_{eff} \cdot dt \quad (20)$$

The domain wall velocity coefficient  $\Gamma_v$  is related to device structure and material property, which can be expressed as shown in equation (14).

Here  $P$  is polarization efficiency,  $\mu_B$  is Bohr magneto,  $e$  is elementary charge and  $M_s$  is magnetization saturation.



| Physical constants                   |   |                       |
|--------------------------------------|---|-----------------------|
| $e$                                  | elementary charge (C)                     | $1.602e^{-19}$        |
| $\mu_B$                              | Bohr magneto ( $J \cdot T^{-1}$ )         | $9.27e^{-24}$         |
| Materials parameters (typical value) |   |                       |
| $H_p$                                | Hard anisotropy (Oe)                      | 5000                  |
| $H_k$                                | Easy anisotropy (Oe)                      | 100                   |
| $M_s$                                | Magnetization saturation(emu/cc)          | 1010                  |
| $A$                                  | Exchange parameter (J/m)                  | $1.8e^{-11}$          |
| $\alpha$                             | Damping parameter                         | 0.002~0.1             |
| $P$                                  | Polarization efficiency                   | 0.35                  |
| $\gamma$                             | Gyromagnetic ratio                        | $1.75e7$              |
| $J_{cr}$                             | Critical current density                  | $5 \cdot 10^7 A/cm^2$ |
| Model parameters                     |   |                       |
| $D$                                  | Length (nm)                               | 200, 600, 1000        |
| $h$                                  | Thickness (nm)                            | 7                     |
| $z$                                  | Width (nm)                                | 10                    |
| $R_{el}$                             | Low sheet resistance ( $\Omega/\square$ ) | 50 (at $h=7nm$ )      |
| $GMR$                                | Giant magneto resistance ratio            | 12%                   |

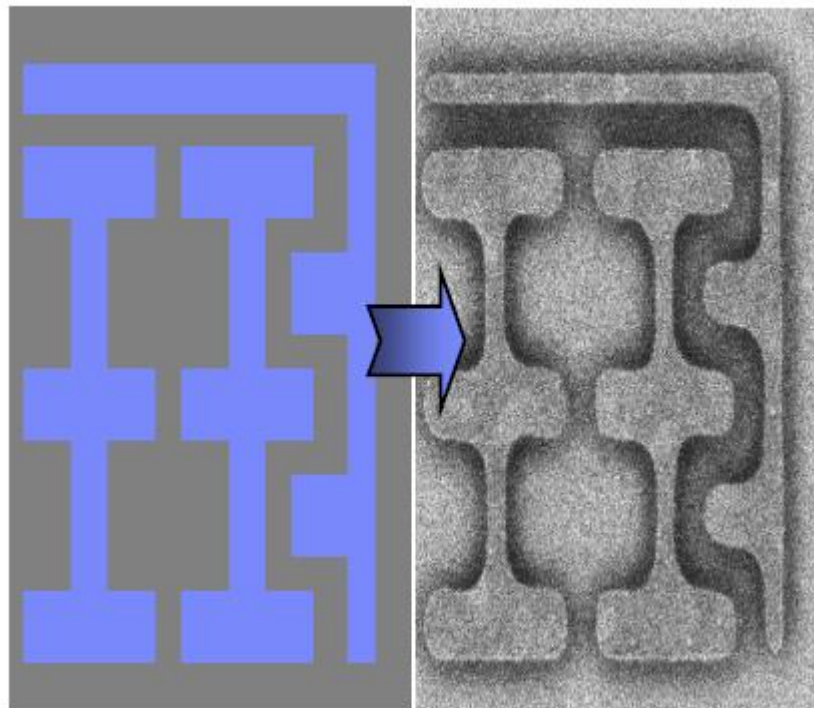
**Table 3.2: Constants and parameters in spintronic memristor model [36].**

# Chapter 4

## Variability

The variability in nanometer-scale integrated circuits is the deviations from the desired or designed values for a structure or circuit parameter to the actual or manufacturing values for a structure or circuit parameter as shown in Figure 4.1. The variations are usually caused by many different sources: physical factors, environmental factors, and aging factors.

These variations can impact key circuit performance characteristics: for digital circuits, the affected parameters include the delay, power, and lifetime of the circuit, while for analog circuits, the performance parameters to be monitored are specific to the type of circuit.



**Figure 4.1: Pattern variations “Design phase & manufacturing phase” [42].**

Physical factors cause a permanent variation in the device attributes (length, widths, oxide thickness), when integrated circuits are fabricated. It becomes particularly important at smaller process nodes (<100 nm).

As the variation becomes a larger percentage of the full length or width of the device and as feature sizes approach the fundamental dimensions such as the size of atoms and the wavelength of usable light for patterning lithography masks. The size of the device elements is smaller than the wavelength of the light, used in Optical lithography, results in distortions due to light diffraction, which is usually called Optical Proximity Effects (OPEs). These effects are expected to be worse as technology scales since the light wavelength is not scaling at the same rate as the device feature size as shown in Figure 4.2.

On the other hand, environmental factors cause variations in the operation of the circuit while the circuit is functioning, and include variations in the power supply and temperature [42-44].

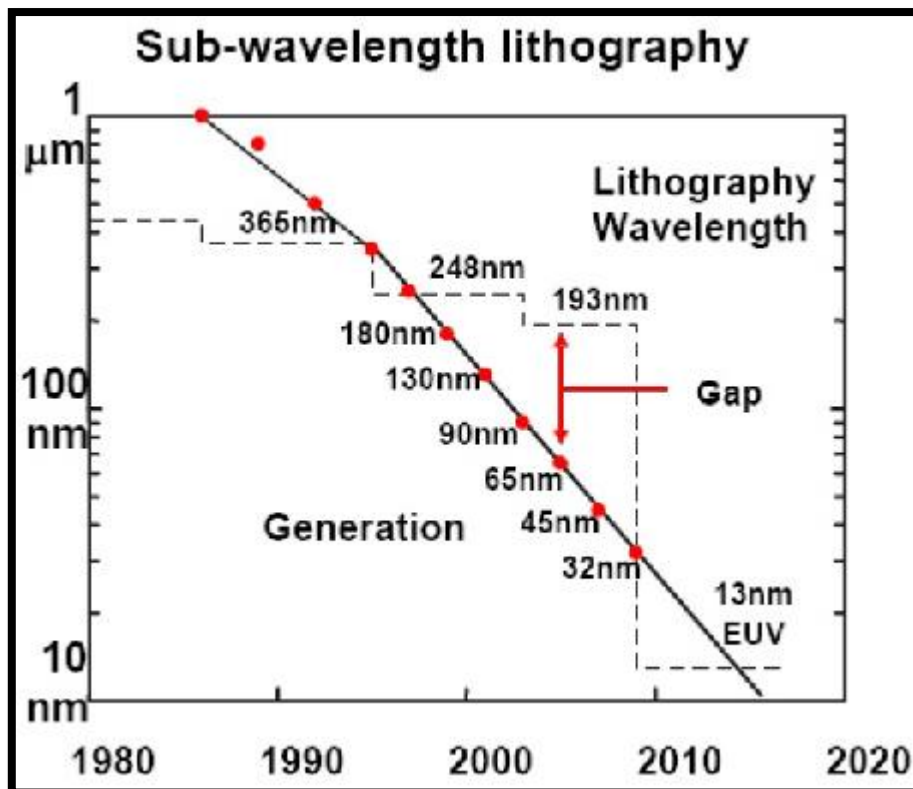


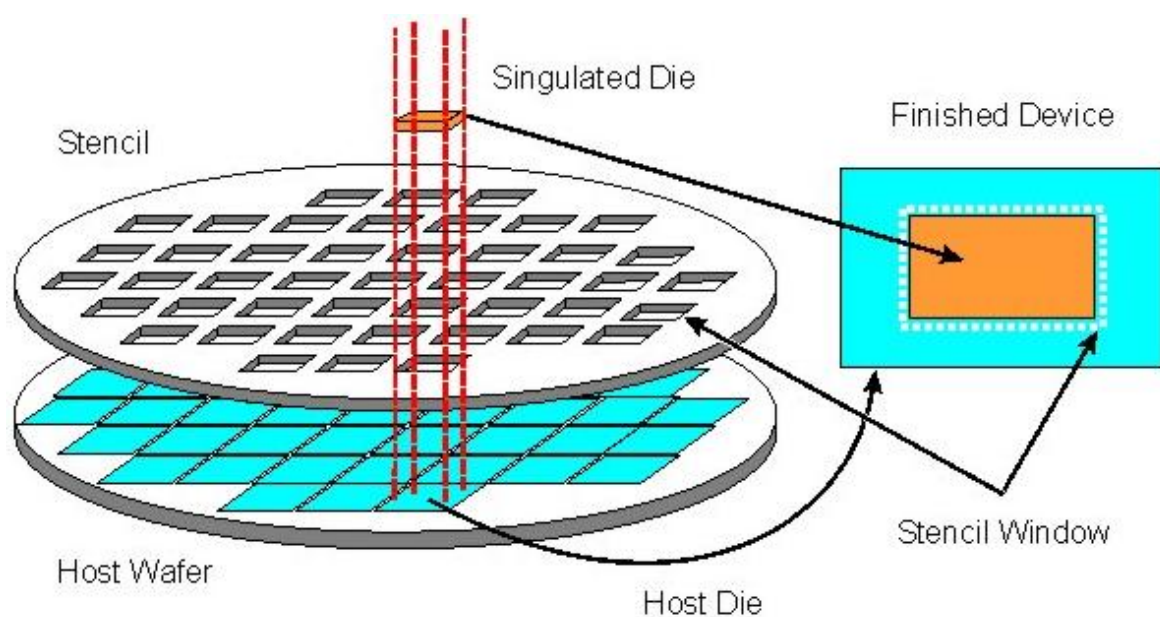
Figure 4.2: Lithography wavelength scaling for different technology nodes [44].

## 4.1 Classification of Variations

Process variations are typically divided into two classes: inter-die and intra-die. Before handling the process variation classes we must take a quick tour around some definitions.

### Wafer & Die

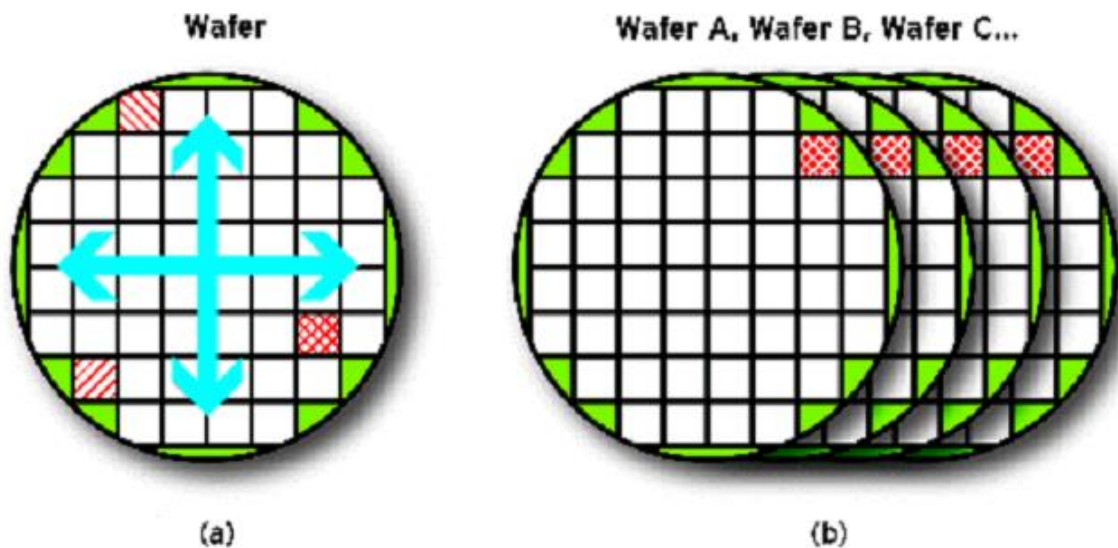
A **wafer**, also called a slice or **substrate**, is a thin slice of **semiconductor material**, such as a **crystalline silicon**, used in **electronics** for the **fabrication of integrated circuits**. The wafer serves as the **substrate** for **microelectronic devices** built in and over the wafer and under goes many micro fabrication process steps such as **doping**. Finally the individual microcircuits are separated (**dicing**) and **packaged**. A wafer with up to thousands of microcircuits (integrated circuits) is cut into rectangular pieces; each called a **die** as shown in Figure 4.3. In between those functional parts of the circuits, a thin non-functional spacing is foreseen where a saw can safely cut the wafer without damaging the circuits. This spacing is called *scribe line* or *saw street*. The width of the scribe is very small. A very thin and accurate saw is therefore needed to cut the wafer into pieces. Usually the dicing is performed with a water-cooled circular saw with diamond-tipped teeth.



**Figure 4.3: Wafer and die [45].**

### 4.1.1. Inter-die Variations

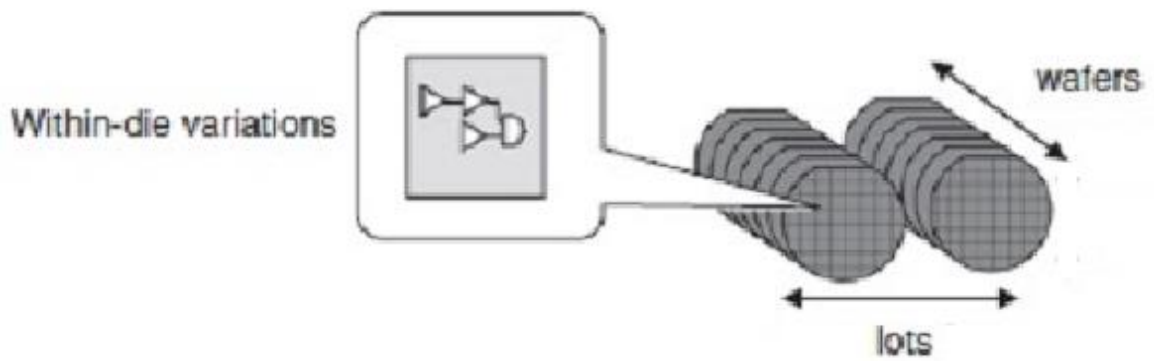
Inter-die variations are also called Die-to-Die variations (D2D). Inter-die variations account for variations that arise between different chips (dies) in the same wafer as shown in Figure 4.4 a) or in different wafers as shown in Figure 4.4 b). They capture the variations from die to die and affect all devices on the same die in the same way. These variations are independent and hence, they can be represented by a single value for each die. In addition, they represent a shift in the mean of the parameter from its nominal value. D2D variations in a single process parameter are easily captured by corner-based models, which assume that all devices on a given design sample have a value that is shifted away from the mean by a fixed amount.



**Figure 4.4: Inter-die or Die-to-Die variations (D2D). a) Variations between different dies in the same wafer, b) variations between different dies in the different wafers [45].**

### 4.1.2 Intra-Die Variations

Intra-die Variations are also called Within-die Variations (WID). Intra-die variations account for a variation that arise between different devices and interconnects that resides within the same chip (die) as shown in Figure 4.5. Thus, each device on a die requires a separate random variable to represent its WID variations. It can be classified into random variations and systematic variations.



**Figure 4.5: Intra-die or within-die variations (WID) [45].**

#### **4.1.2.1 Random Variations**

A random-WID parameter variation fluctuates randomly and independently from device to device (i.e., device-to-device correlation is zero). It is such as Random Dopant Fluctuations (RDF) and Line Edge Roughness (LER). The impact of these random variations is expected to be worse as process parameters scale. The random variations impact can be reduced by increasing the logic depth due to the averaging effect. Unfortunately, the trend to increase the clock frequency of a design using aggressive pipelining has resulted in smaller logic depth, which increases the impact of this type of variations [42-45].

#### **4.1.2.2 Systematic Variations**

A systematic-WID parameter variation results from a repeatable and governing principle, where the device-to-device correlation is empirically determined as a function of the distance between the devices. Although systematic-WID variations exhibit a correlated behavior, the profile of these variations can randomly change from die to die. From a designer's perspective, systematic-WID variations behave as continuous and smooth correlated random-WID variations [42-45].

## 4.2 Variation sources

The sources of these variations can be categorized into several classes, depending on their origin, as follows [43, 46].

### 4.2.1. Process variation physical factors (Static Variations)

Static variations are one-time variations that occur when a circuit is manufactured, and cause process parameters to drift from their designed values. The sources of process variation physical factors can be summarized as follows:

#### 4.2.1.1 Random Doping Fluctuation (RDF):

Random dopant fluctuation (RDF) is a form of process variation resulting from variation in the implanted impurity concentration, the number of doping impurities in the semiconductor decreases as shown in in Figure 4.6.

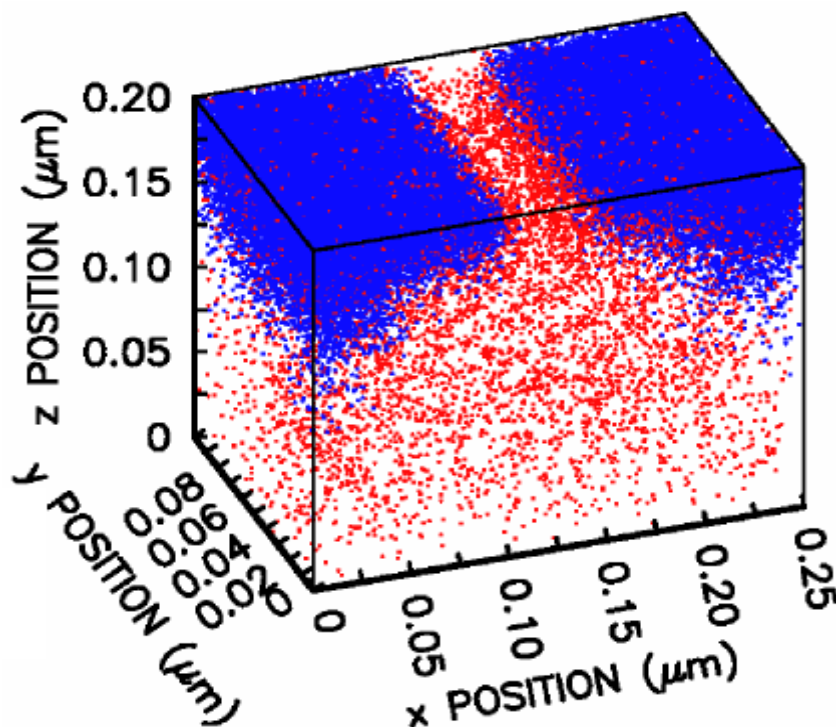


Figure 4.6: Random dopant effect [47].



In newer process technologies RDF has a larger effect because the total number of dopants is fewer, and the addition or deletion of a few impurity atoms can significantly alter transistor properties. RDF is a local form of process variation, meaning that two neighboring devices (transistors, memristors, and so on...) may have significantly different dopant concentrations. In MOSFET transistors, RDF in the channel region can alter the transistor's properties, especially threshold voltage. In Figure 4.7 shows number and the distribution of dopant atoms in a transistor. In case of memristors, the different dopant concentrations have a direct effect on the memristor resistivity, which affect the memristance value.

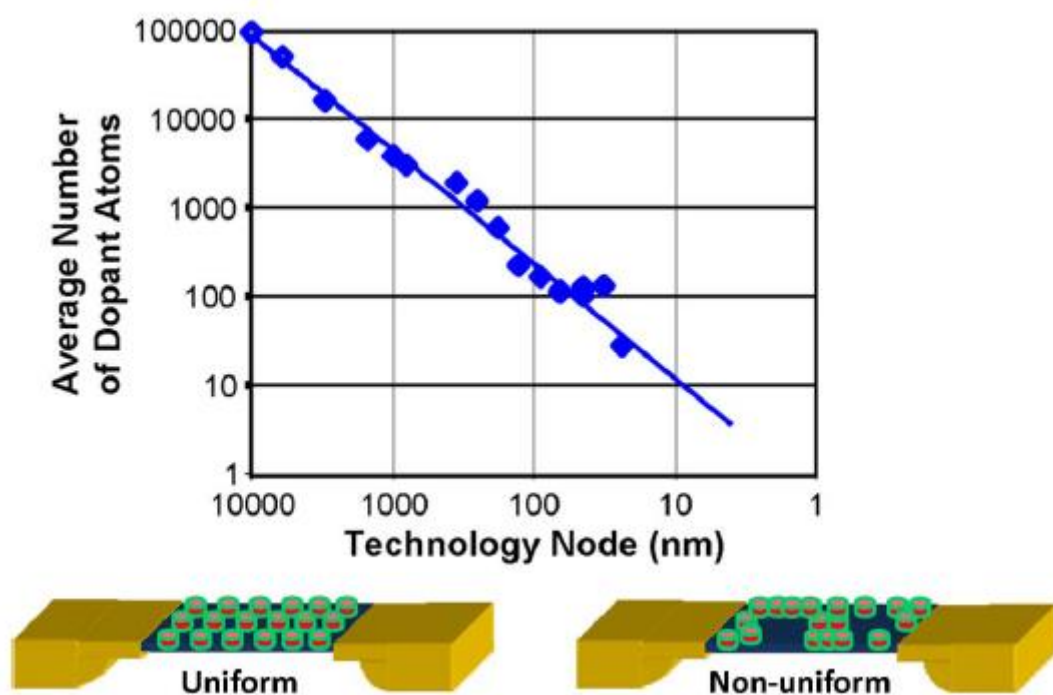
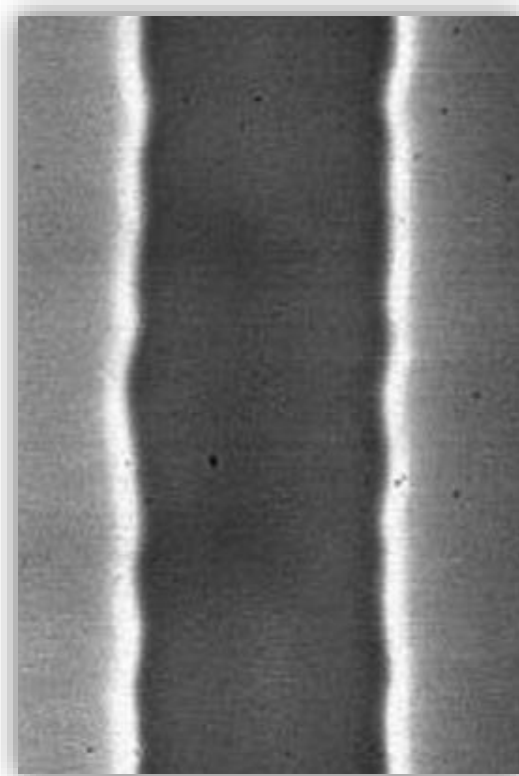


Figure 4.7: Number and distribution of dopant atoms in a transistor [48].



#### 4.2.1.2. Line Edge Roughness (LER)

Line Edge Roughness (LER) is a variation along the edge of the device surface as shown in Figure 4.8. LER becomes important for feature sizes on the order of 100 nm or less. It effects on the memristor dimensions  $w$ ,  $l$ , and  $D$ . In CMOS, LER refers to the roughness on the edge of the channel and contributes to the threshold voltage variations. Ideally, the edge of the channel should be a straight line, but as the edge of the channel is determined by a varying process, the edge will not be completely straight, as shown in Figure 4.1 [24]. Previously, the dimensions of the transistor channel were orders of magnitude larger than the roughness along the edge of the transistor channel (on the order of 5 nm), but as the transistor length is scaled down, the roughness does not scale correspondingly and can cause variations in transistor characteristics. These random effects end up causing variations in the threshold voltage.



**Figure 4.8: Laser image appears details of line edge roughness (LER) [44].**

### 4.2.1.3 Oxide Thickness Fluctuation (OTF)

A variation in the oxide thickness  $T_{ox}$  in CMOS, affect the transistor threshold voltage,  $V_t$ . Therefore, the  $T_{ox}$  variations should be considered.

In memristor, the (OTF) affect the all size  $w$ ,  $D$  and  $z$  which affect the resistivity of the memristor. The Oxide Thickness Fluctuation (OTF) is declared as shown in figure 4.9.

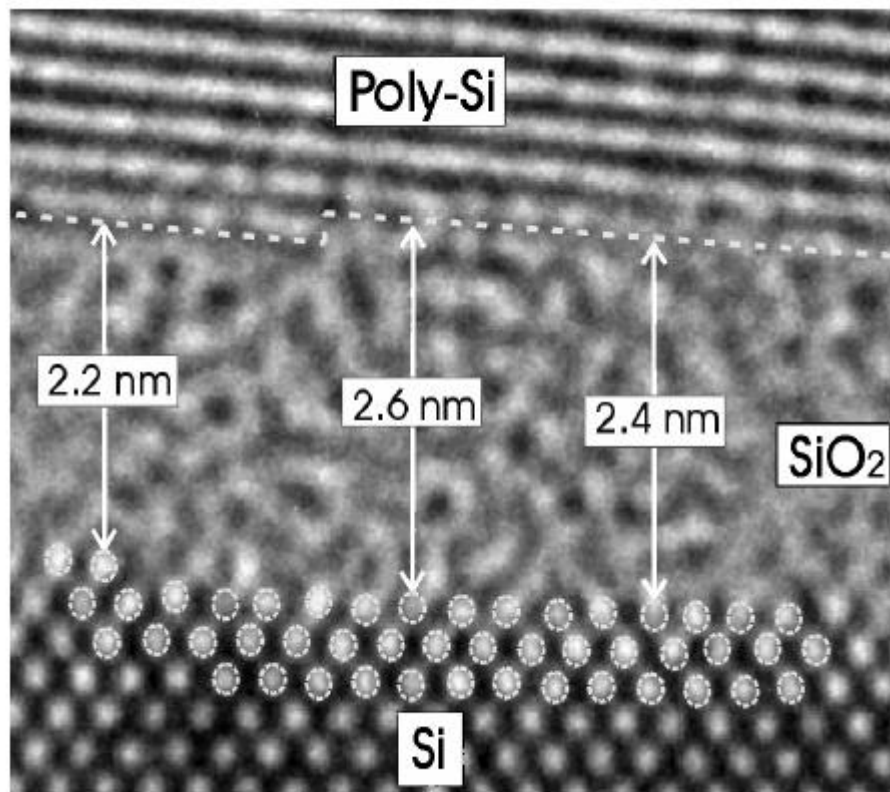


Figure 4.9: Oxide thickness fluctuations [47].

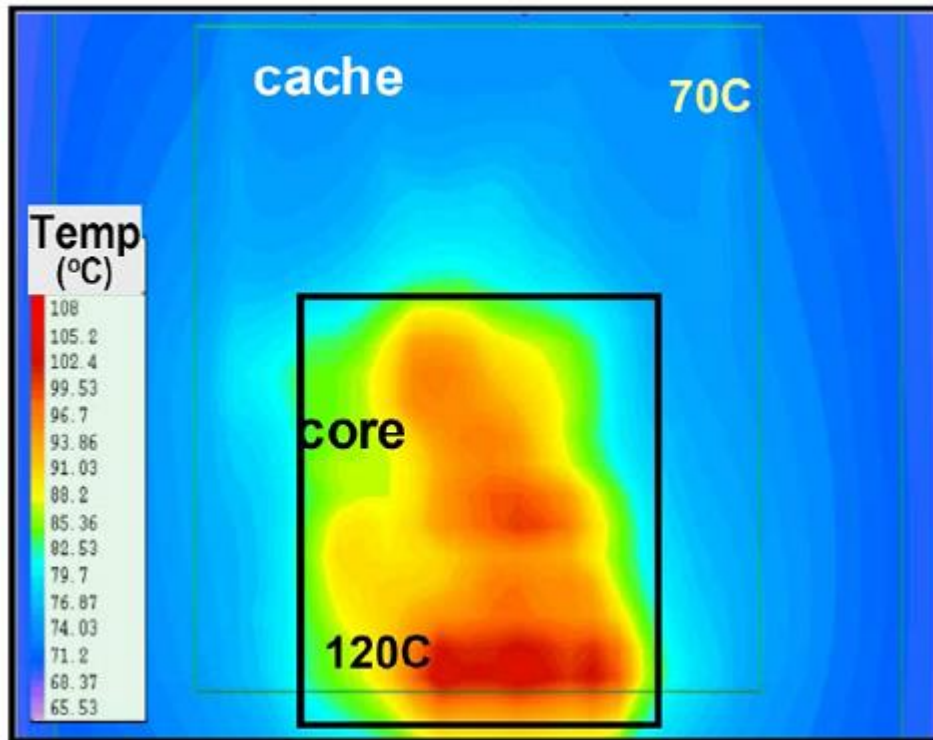
## **4.2.2. Process variation environmental factors (Dynamic variation)**

Unlike process variations, which are one-time variations that are static after a circuit is manufactured, environmental variations correspond to changes during the operation of a circuit. For process variations, it is possible to use statistical methods that optimize the manufacturing yield of the circuit, discarding (or binning) any die that fail to meet specifications. However, for any run-time environmental variations, it is essential to ensure that a circuit meets its specifications at all times. Therefore, environmental variations are subject to worst-case analysis, although approaches using statistical methods such as extreme value theory [42-43, 46] have been proposed to identify the worst case.

The dynamic variations affect the circuit operation while the circuit is functioning. Three types of environmental variations will be introduced, supply voltage fluctuations, temperature changes, and soft errors.

### **4.2.2.1 Thermal Variations**

The impact of temperature on the functioning of a chip is an important factor in inducing variation and reliability issues. Elevated on-chip temperatures can have several consequences on performance. Within die temperature fluctuations are considered one of the major performance and packaging challenges. This is because both device and interconnect have temperature dependence that causes performance to degrade at higher temperature. Moreover, the temperature variation across different communicating blocks on the same die may result in performance mismatches, which may lead to functional failures. Figure 4.10 shows WID temperature fluctuations for a microprocessor unit, with the core exhibits a hot spot of 120oC [42-43].



**Figure 4.10: Thermal profile showing within die temperature variation for a microprocessor. Hot spots with temperatures as high as 120oC are shown [46].**

#### **4.2.2.2 Power Supply Variation**

Run-time fluctuations in the supply voltage levels in a chip can cause significant variations in parameters such as gate delays, and may even result in logic failures. In nanometer-scale technologies, the current densities have increased over previous generations, and spatial imbalances between the currents in various parts of a chip are accentuated, particularly with the advent of multicore systems where some cores may switch on and off entirely [43].

#### **4.2.2.3 Soft Errors**

With the number of devices on a chip numbering in the billions, and with limited charge storage ability for each device, integrated circuits are increasingly susceptible to strikes from cosmic rays, alpha particles, and neutron-induced Boron fission [43]. These strikes can cause momentary surges in charge that can result in effects such as increased delays, logic failures, or incorrectly flipped memory bits. These impermanent

errors are referred to as soft errors, and these have been observed to be significant, not only in radiation-sensitive environments such as space, but also in normal high-performance applications on earth. Not every single-event upset may result in incorrect logic: in particular, mechanisms such as logical masking, temporal masking, and electrical masking can render such events harmless in digital logic. However, the problem is serious enough to merit significant research efforts [43].

### **4.2.3. Aging Variations**

Aging variation reflect the fact that the behavior of a circuit degrades as it ages, due to the prolonged application of stress. Such degradations may result in parametric degradations or catastrophic failures [43].

# Chapter 5

## Compact model of TiO<sub>2</sub> Thin Film Memristor under Process Variations, and Simulation Results

### 5.1 The TiO<sub>2</sub> Memristor Compact Model

The impact of process variations is affecting the device performance by deviating the actual electrical behavior of the memristor ( $R_{on}$ ,  $R_{off}$ , and  $\alpha$ ) from the desired values (failure in write/read digital logic 1/0).

This deviation results in reducing the yield. Yield= (1- failure), also the yield is defined as the number of memristor cells which have a right write/read.

We observed from our calculations that the failure percentage in the case of writing / reading '0' is much lower than that in the case of writing/reading '1', as we defined a memristor is at logic zero when  $M=R_{off}$  and a memristor is at logic one when  $M=R_{on}$ . The process variation effect is much larger on the  $R_{on}$  than  $R_{off}$ ; as  $R_{off}$  has a larger value than  $R_{on}$ ;  $R_{off} \cong 1000 * R_{on}$ . For example:

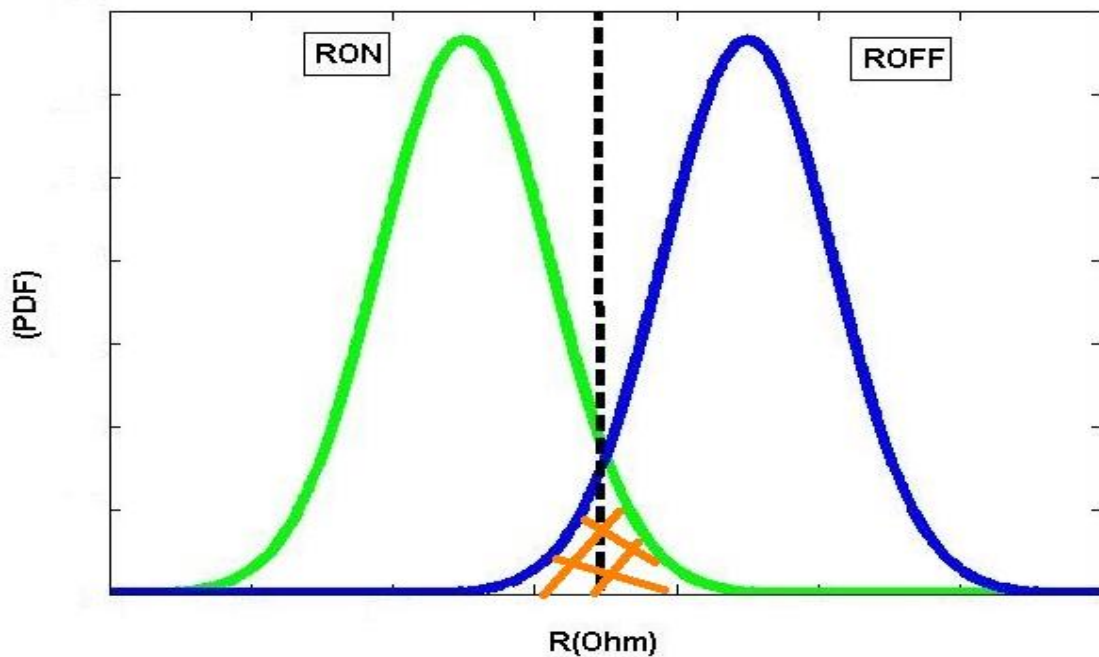
$$M(\alpha) = R_{on} \alpha + R_{off} (1-\alpha) \quad (21) .$$

When  $\alpha = 0$ ,  $M = R_{off}$ . If  $\alpha$ , due to process variation equals 0.001 (assuming  $R_{on} = 200 \Omega$  and  $R_{off} = 200 \text{ k}\Omega$ ),  $M = 0.001 * R_{off} + 0.999 * R_{off} \cong 199.8 \text{ k}\Omega$  with an error of 0.1%.

When  $\alpha = 1$ ,  $M = R_{on}$ . If  $\alpha$ , due to process variation equals 0.999,  $M = 0.001 * R_{off} + 0.999 * R_{off} \cong 400 \Omega$  with an error of 100%.

Very recently, a Monte-Carlo simulation method was proposed to analyze the impact of geometry variations on the electrical properties of the memristors [49-54]. A 3D device structure including the geometry variation information is generated by performing a sanity check of the device characterization parameters. In the Monte-Carlo simulations, the memristor device is divided into many small filaments sandwiched between two electrodes. Within a filament  $i$ , the cross-section area  $s'_i = l'_i \cdot z'_i$  and thickness  $D'_i$ , considered as constants, whose value can be modeled by taking into account the effects of LER or OTF, respectively.

A compact model was proposed to generate a large volume of process variation-aware three-dimensional device structures for Monte-Carlo simulations. We did 5000 samples to each point in our simulations. Therefore, it is very important to understand and characterize the impact of process variation on memristor performance and yield and attempt to optimize the yield. Figure 5.1 shows the PDF Monte-Carlo of  $R_{on}$  and  $R_{off}$ , and the cross failure due to variation. The cross section between the  $R_{on}$  PDF and  $R_{off}$  PDF is the failure region in which write/read operation is wrong.



**Figure 5.1: PDF of  $R_{ON}$  and  $R_{OFF}$ , the cross failure region.**

In our model, we take the memristor variations and yield analysis into account [49]. The total memristance  $M'$ , which is a time-varying parameter, can be uniquely defined by  $R'_{off}$ ,  $R'_{on}$ , and  $\alpha'(t)$ . In this section, we examine the variations of  $R'_{off}$ ,  $R'_{on}$ , and  $\alpha'(t)$ . Then, we will derive the corresponding process-variation aware memristance model. We summarize the designed values of the TiO<sub>2</sub> memristor geometry dimensions and its electrical parameters adopted in our work. For a given TiO<sub>2</sub> memristor, we use  $R'_{off}$  and  $R'_{on}$  to denote its actual highest and lowest total memristance, respectively [50-52]:

$$R'_{off} = R_{off} \cdot (\mu_{R_{off}} + \sigma_{R_{off}} \cdot E) \cdot (1 + \sigma_y \cdot D_y), \quad (22)$$

$$R'_{on} = R_{on} \cdot (\mu_{R_{on}} + \sigma_{R_{on}} \cdot E). \quad (23)$$

Here, two independent random numbers  $E \sim N(0,1)$  and  $D_y \sim N(0,1)$  are introduced.  $E$  represents the correlation between  $R'_H$  and  $R'_L$  due to the same geometry variation sources  $D_y$  and  $\sigma_y$  represents the impact of RDD.

By running extensive numerical simulations under various conditions, we found the actual  $\alpha'$  can be modeled as the product of the designed value  $\alpha$  and a coefficient  $\eta$  that represents the influence of process variations as [50-52]:

$$\alpha' = \eta \cdot \alpha. \quad (24)$$

Here  $\eta$  can be expressed by [50-52]:

$$\eta = \frac{1}{(1 + \varphi \cdot \varepsilon_1 + \varphi \cdot \varepsilon_2 (\omega_1 \cdot E + \omega_2 \cdot G)) \cdot (1 + \sigma_y \cdot D_y)}. \quad (25)$$

To avoid overestimating the impact of geometry variations on  $\alpha'$ , a new random number  $G \sim N(0, 1)$  is introduced to offset the impact of LER.  $\varepsilon_1$  and  $\varepsilon_2$  are two scalars



extracted from the actual simulations performed by the device simulator. The coefficients  $\omega_1$  and  $\omega_2$  represent the weights of  $E$  and  $G$ , where  $\omega_1^2 + \omega_2^2 = 1$ . By modeling  $R'_{on}$ ,  $R'_{off}$  and  $\alpha'$ , the total memristance  $M'$  of a  $\text{TiO}_2$  memristor can be simply calculated by [50-52]:

$$M'(\alpha) = R'_{on} \cdot \alpha' + R'_{off} \cdot (1 - \alpha'). \quad (26)$$

Table 6.1 shows the model variation parameters and table 6.2 shows another variation parameter ( $\sigma_y$ ) which determined in Toronto by COMSOL help.

| Variation Parameters |       | Coefficients |        |
|----------------------|-------|--------------|--------|
| $\mu_{Roff}$         | 0.994 | $\epsilon_1$ | -0.028 |
| $\mu_{Ron}$          | 0.994 | $\epsilon_2$ | 0.072  |
| $\sigma_{Roff}$      | 2.16% | $\omega_1$   | 0.98   |
| $\sigma_{Ron}$       | 2.16% | $\omega_2$   | 0.2    |

**Table 5.1: Model parameters [52].**

| D   | L=z   | $\sigma_y$ | D   | L=z   | $\sigma_y$ |
|-----|-------|------------|-----|-------|------------|
| 3nm | 10nm  | 1.1879     | 6nm | 10nm  | 1.115      |
|     | 30nm  | 1.1185     |     | 30nm  | 1.06       |
|     | 50nm  | 1.04       |     | 50nm  | 0.9812     |
|     | 70nm  | 0.9947     |     | 70nm  | 0.9366     |
|     | 100nm | 0.9515     |     | 100nm | 0.8921     |

| D    | L=z   | $\sigma_y$ | D    | L=z   | $\sigma_y$ |
|------|-------|------------|------|-------|------------|
| 10nm | 10nm  | 1.03       | 15nm | 10nm  | 0.9986     |
|      | 30nm  | 0.9785     |      | 30nm  | 0.9486     |
|      | 50nm  | 0.9064     |      | 50nm  | 0.8787     |
|      | 70nm  | 0.8652     |      | 70nm  | 0.8388     |
|      | 100nm | 0.8199     |      | 100nm | 0.7989     |

Table 5.2: TiO2 Dimensions and  $\sigma_y$  Values.

## 5.2 TiO<sub>2</sub> Thin-Film Memristor yield without variation compensation

We take many example of TiO<sub>2</sub> memristor in different dimensions and did a Monte-Carlo simulation to each case and calculate the yield before variation compensation.

From our observation that the failure in the case of writing and reading '0' is much lower than that in the case of writing and reading '1'. We will consider only the case when  $\alpha = 1$  which dominated the overall memory failure probability.

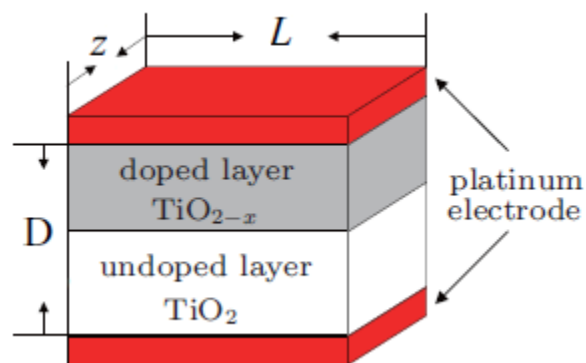


Figure 5.2: TiO2 Thin-film memristor structure.

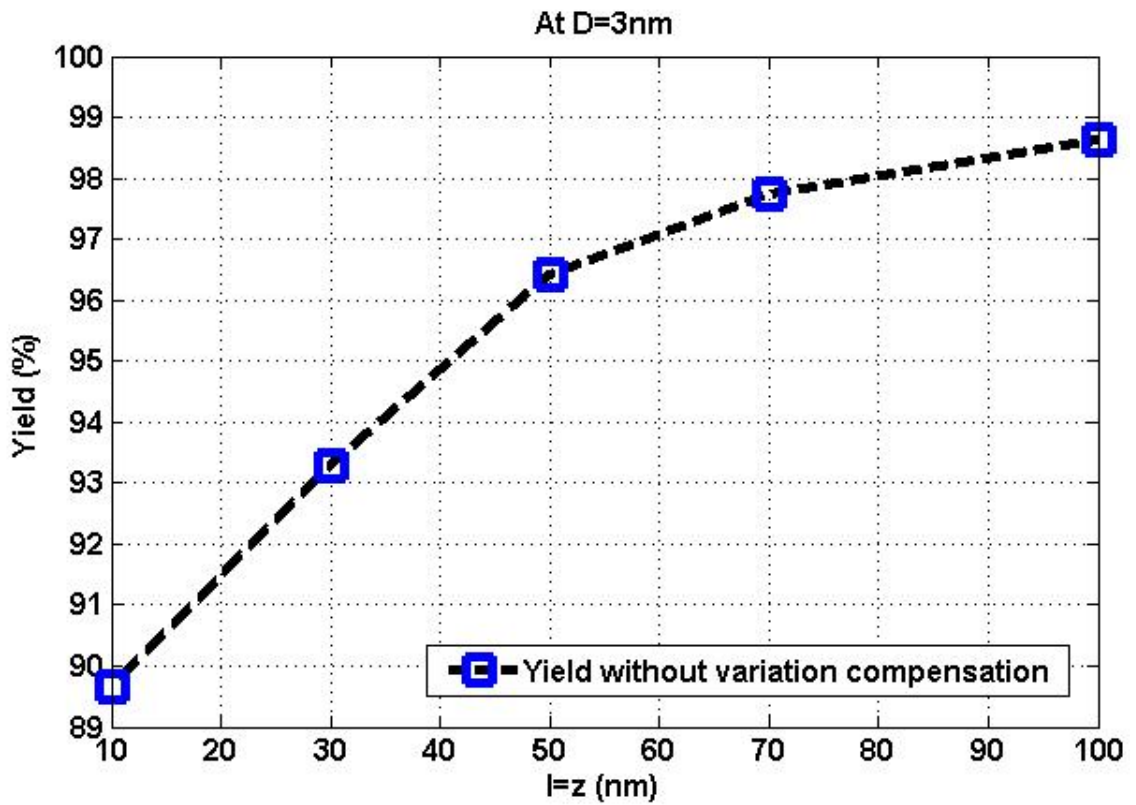


Figure 5.3: The yield without variation compensation at case D=3nm.

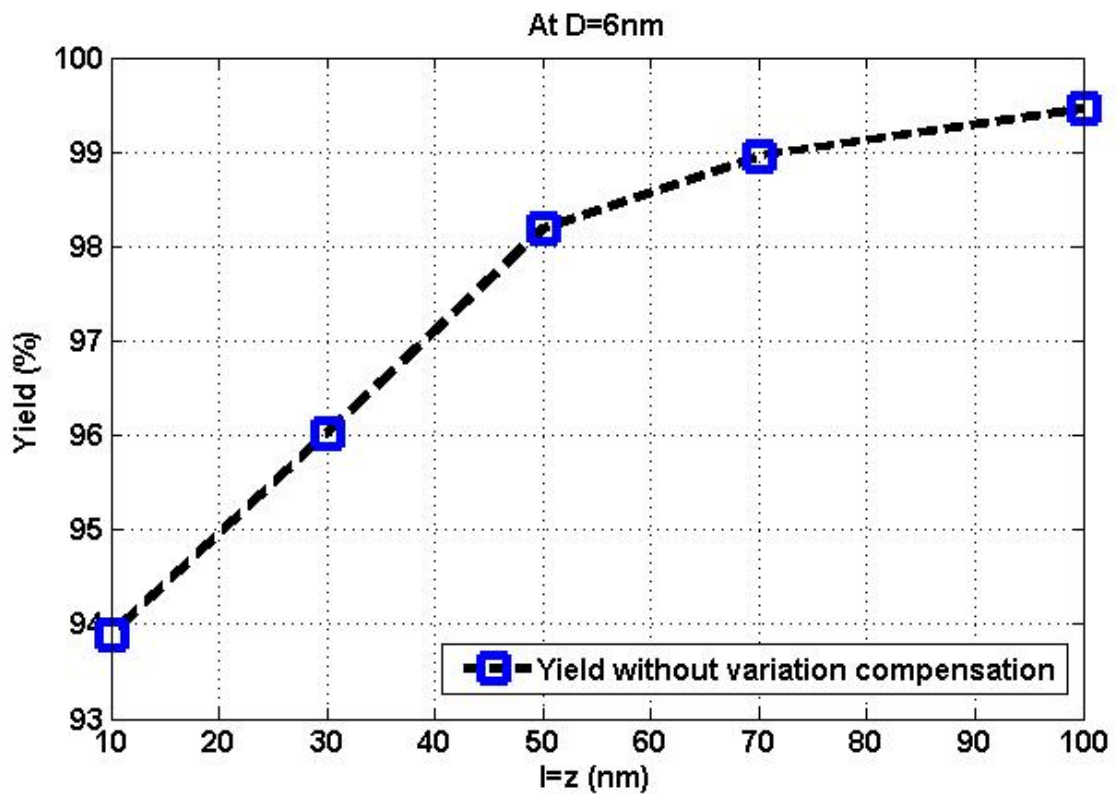


Figure 5.4: The yield without variation compensation at case D=6nm.

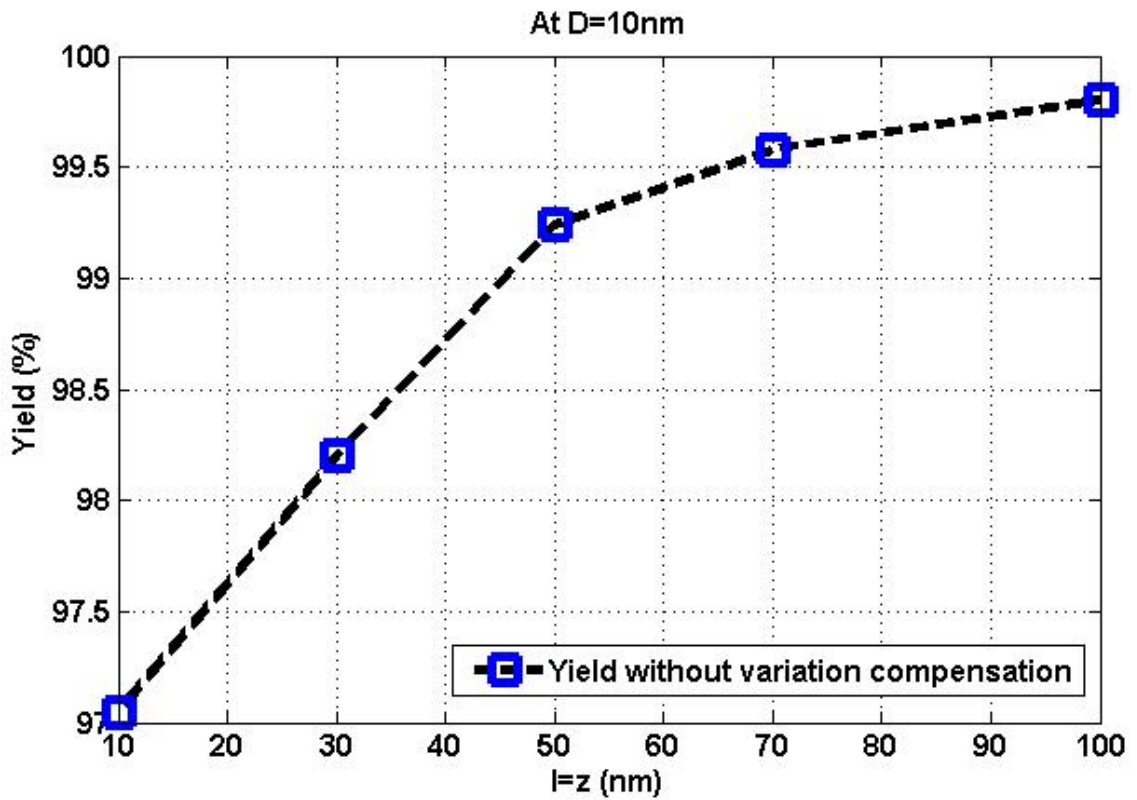


Figure 5.5: The yield without variation compensation at case D=10nm.

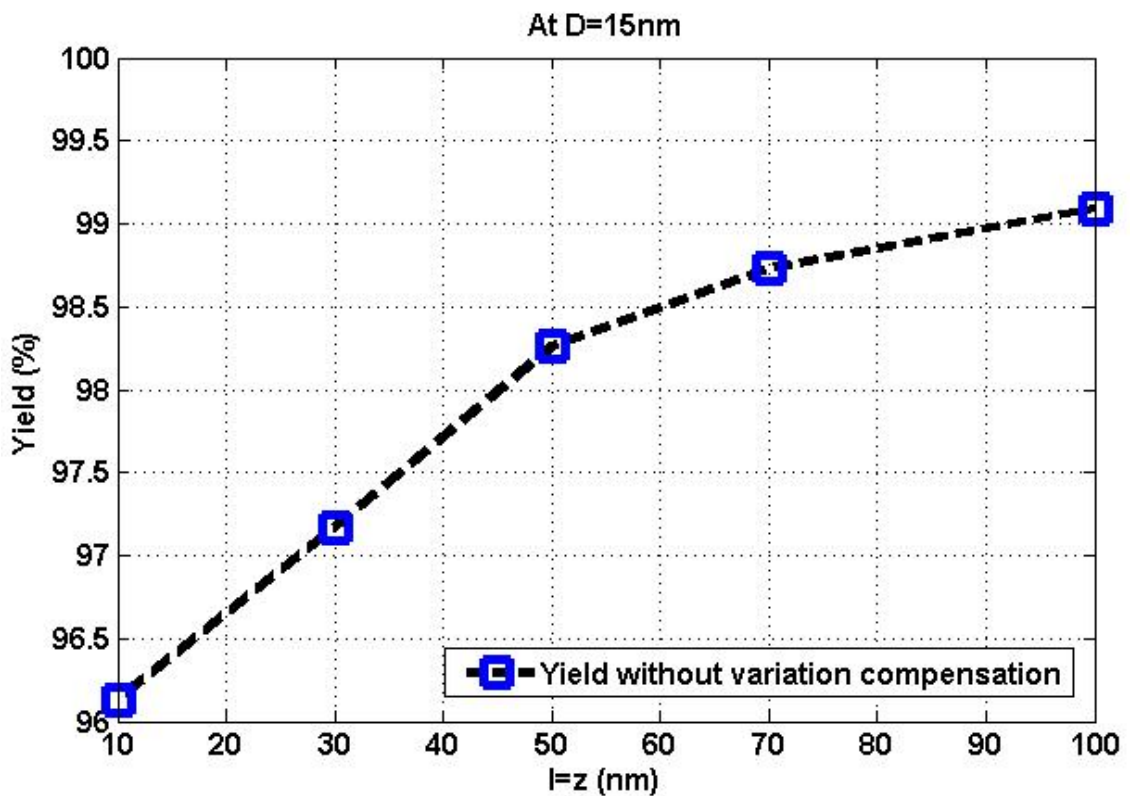


Figure 5.6: The yield without variation compensation at case D=15nm.

Figure.5.2 shows the  $\text{TiO}_2$  memristor dimensions; memristor thickness  $D$ , memristor length  $l$ , and memristor width  $z$ .

Figure.5.3 shows the yield in case without variation compensation in case of  $\text{TiO}_2$  memristor thickness  $D=3\text{nm}$  and its length  $l$  and the width  $z$  are equally and vary from 10nm to 100nm. At  $l=z=10\text{nm}$  the yield equal 89.67%, at  $l=z=30\text{nm}$  the yield equal 93.29%, at  $l=z=50\text{nm}$  the yield equal 96.43%, at  $l=z=70\text{nm}$  the yield equal 97.73%, and at  $l=z=100\text{nm}$  the yield equal 98.63%.

Figure.5.4 shows the yield in case without variation compensation in case of  $\text{TiO}_2$  memristor thickness  $D=6\text{nm}$  and its length  $l$  and the width  $z$  are equally and vary from 10nm to 100nm. At  $l=z=10\text{nm}$  the yield equal 93.89%, at  $l=z=30\text{nm}$  the yield equal 96.03%, at  $l=z=50\text{nm}$  the yield equal 98.19%, at  $l=z=70\text{nm}$  the yield equal 98.96%, and at  $l=z=100\text{nm}$  the yield equal 99.46%.

Figure.5.5 shows the yield in case without variation compensation in case of  $\text{TiO}_2$  memristor thickness  $D=10\text{nm}$  and its length  $l$  and the width  $z$  are equally and vary from 10nm to 100nm. At  $l=z=10\text{nm}$  the yield equal 97.05%, at  $l=z=30\text{nm}$  the yield equal 98.20%, at  $l=z=50\text{nm}$  the yield equal 99.24%, at  $l=z=70\text{nm}$  the yield equal 99.58%, and at  $l=z=100\text{nm}$  the yield equal 99.80%.

Figure.5.6 shows the yield in case without variation compensation in case of  $\text{TiO}_2$  memristor thickness  $D=15\text{nm}$  and its length  $l$  and the width  $z$  are equally and from 10nm to 100nm. At  $l=z=10\text{nm}$  the yield equal 96.13%, at  $l=z=30\text{nm}$  the yield equal 97.17%, at  $l=z=50\text{nm}$  the yield equal 98.26%, at  $l=z=70\text{nm}$  the yield equal 98.73%, and at  $l=z=100\text{nm}$  the yield equal 99.09%.

### **5.3 $\text{TiO}_2$ Writing Yield Optimization**

Memristors can be charge controlled or flux controlled depending on the biasing condition [50]–[52]. More specifically, when a memristor is connected to a current source, the current source will inject charges through the memristor cell. It is convenient to treat such a memristor as charge controlled because the state of the memristor changes according to the amount of charge injection, and the state cause

memristance to change. On the other hand, when a voltage source is added across a memristor, it is natural to consider the memristor as flux controlled. In this case, the state of the memristor changes according to the amount of flux injection, and the state cause memristance to change. To write a logic value to a memristor cell, there is a one simple way “applying voltage source”.

In the case of the writing '1' operation, the input writing flux should be adjusted to change the memristor device's memristance from  $R_{off}$  to  $R_{on}$ , the flux can be described as follow [50, 52]:

$$\phi = \frac{\phi_D}{R_H} [R_{off}^2 - R_{on}^2] \quad (27)$$

$$\phi_D = \frac{(\beta D)^2}{2\mu_v(\beta - 1)} \quad (28)$$

Where  $\beta$  denoted the  $R_H = \beta.R_L$  ratio,  $\mu_v$  is the mobility.

In this case, all the memristor devices should have their Memristance  $M'$  less than a given threshold (normally selected to be midway between  $R_{on}$  and  $R_{off}$ , typically,  $[(R_{on} + R_{off})/2]$ ). Since in the case of  $\alpha = 1$ , the ideal memristance without variations should equal  $R_{on}$ , variations result in making the memristance of some memristor devices deviates from  $R_{on}$  and becomes larger than the threshold.

The writing yield is defined as the number of memristors samples (out of 5000 samples in our simulations) that exhibit correct writing operation (i.e., their memristance is less than the mid-way threshold when variations is taken into account).

In order to optimize the writing yield, the input flux is changed by changing the input voltage amplitude as well as reading duration time to achieve the maximum possible writing yield.

The following simulation results provide an important design insight to the memristor-based memory array designers as follows. If the designer ignores the variations and find only the input writing flux that changes the memristance value from

$R_{off}$  to  $R_{on}$ . This flux will not achieve the maximum writing yield. However, if the designer considers the variations, a new flux value should be used that results in optimizing the yield. Here, the writing yield is defined as the percentage of memory cells that are written correctly (i.e., the cells that are written as '1' when they are desired to store '1' with no failure).

We did a (for loop) by using Matlab in Monte-Carlo technique to determine the optimum yield when using a certain flux value. The yield defined as PDF to the memristance values.

Once again, the case of writing '0' provide very small failure probability compared to the writing '1' case. Therefore, only the writing '1' case (i.e.,  $\alpha = 1$ ) is considered in this paper. Figures 5.7, 5.8 5.9 and 5.10 portray a comparison of the writing yield for different memristor sizes when the normal input writing flux given in equation (27) is used (i.e., no writing yield optimization and the variations are not compensated) and when the optimal input writing flux is used (i.e., the writing yield is optimized and the variations are taken into account).

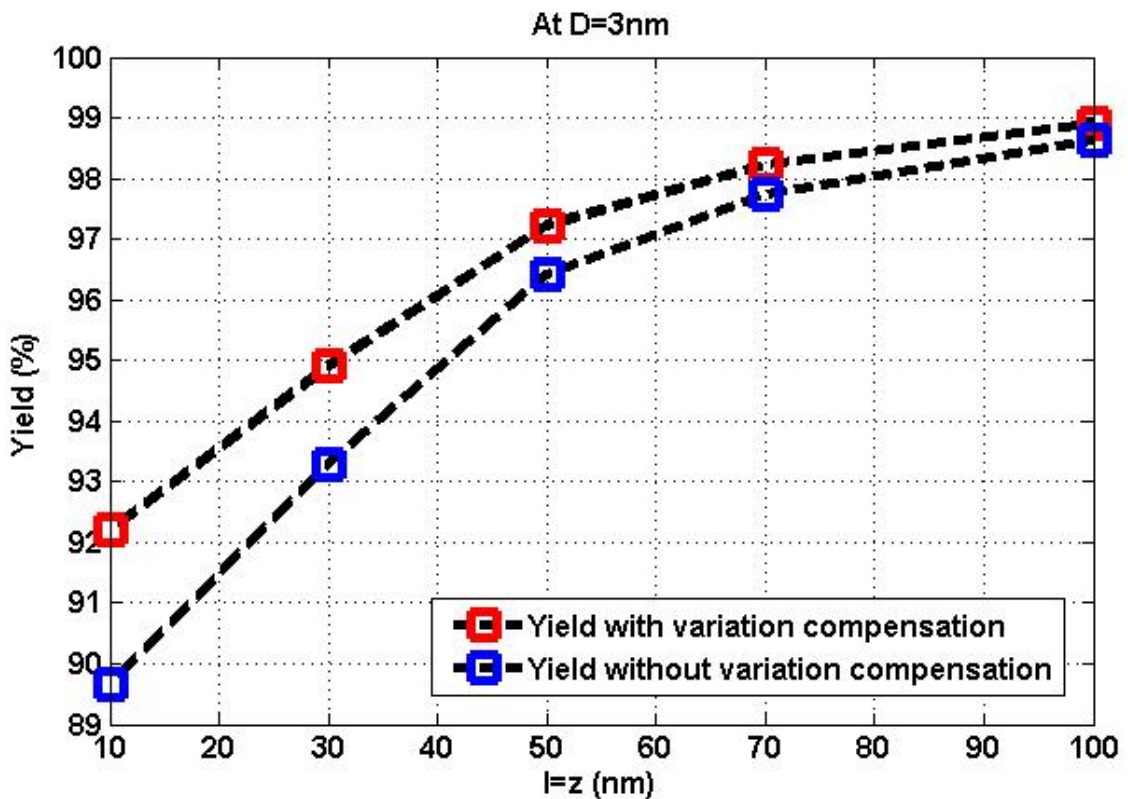


Figure 5.7: The writing yield before/after variation compensation in case  $D=3$ nm.

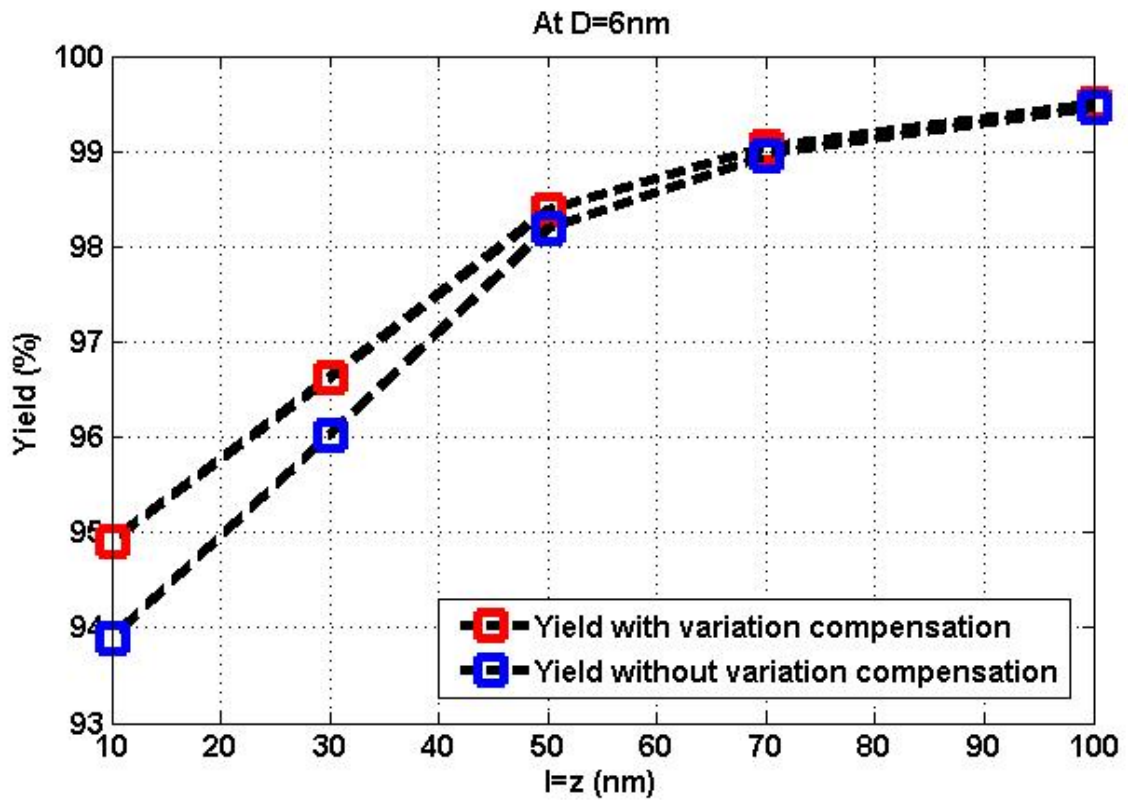


Figure 5.8: The writing yield before/after variation compensation in case D=6nm.

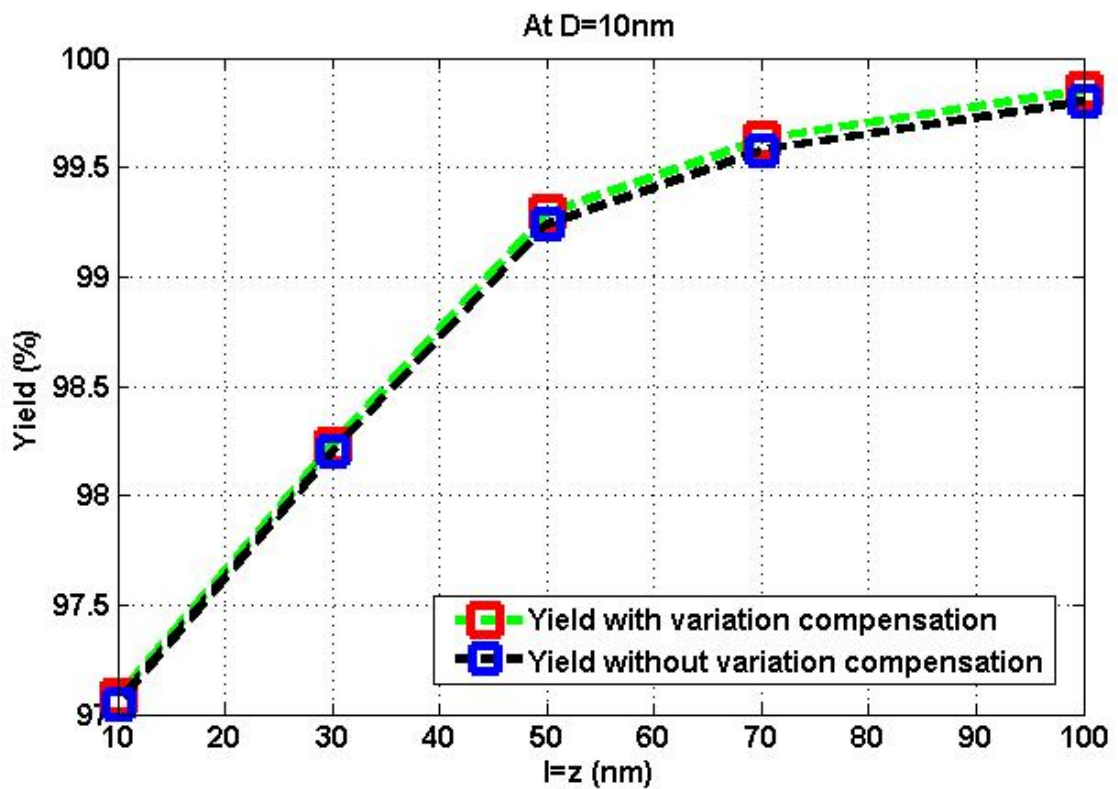
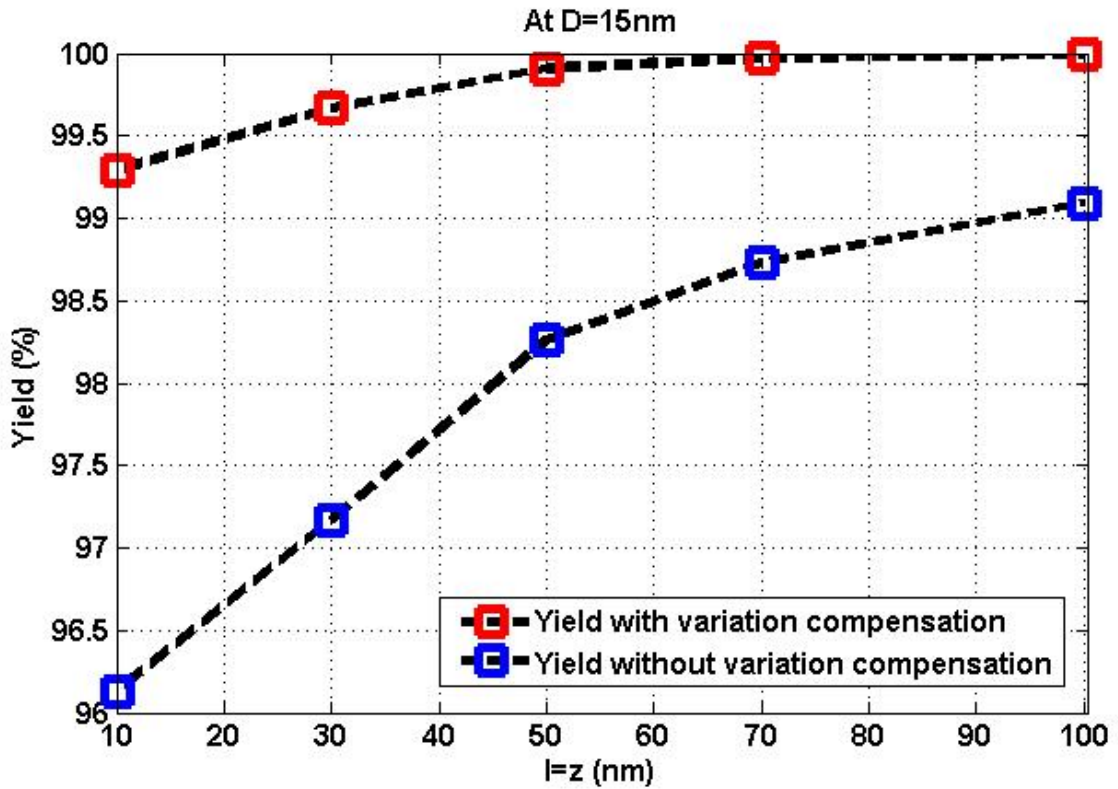


Figure 5.9: The writing yield before/after variation compensation in case D=10nm.





**Figure 5.10: The writing yield before/after variation compensation in case D=15nm.**

Figure.5.7 show the case of TiO<sub>2</sub> at D=3nm, before the variation compensation, after variation compensation by changing the flux and cleared the improvement in yield values. For example: the case (l=z=10nm) the yield improve from 89.67% to 92.2%, the case (l=z=30nm) from 93.29% to 94.9%, the case (l=z=50nm) from 96.43% to 97.23%, the case (l=z=70nm) from 97.73% to 98.22%, and the case (l=z=100nm) from 98.63% to 98.91%.

Figure.5.8 show the case of TiO<sub>2</sub> at D=6nm, before the variation compensation, after variation compensation by changing the flux and cleared the improvement in yield values. For example: the case (l=z=10nm) the yield improve from 93.89% to 94.91%, the case (l=z=30nm) from 96.03% to 96.62%, the case (l=z=50nm) from 98.19% to 98.38%, the case (l=z=70nm) from 98.96% to 99.05%, and the case (l=z=100nm) from 99.46% to 99.50%.

Figure.5.9 show the case of TiO<sub>2</sub> at D=10nm, before the variation compensation, after variation compensation by changing the flux and cleared the improvement in yield values. For example: the case (l=z=10nm) the yield improve from 97.05% to 97.08%,

the case ( $l=z=30\text{nm}$ ) from 98.20% to 98.23%, the case ( $l=z=50\text{nm}$ ) from 99.24% to 99.29%, the case ( $l=z=70\text{nm}$ ) from 99.58% to 99.63%, and the case ( $l=z=100\text{nm}$ ) from 99.80% to 99.85%.

Figures.5.10 show the case of  $\text{TiO}_2$  at  $D=15\text{nm}$ , before/ after variation compensation and cleared the improvement in yield values. For example: the case ( $l=z=10\text{nm}$ ) the yield improve from 96.13% to 97.55%, the case ( $l=z=30\text{nm}$ ) from 97.17% to 98.63%, the case ( $l=z=50\text{nm}$ ) from 98.26% to 99.51%, the case ( $l=z=70\text{nm}$ ) from 98.73% to 99.97%, and the case ( $l=z=100\text{nm}$ ) from 99.09% to 99.99%.

It is obvious from Figures. 5.7, 5.8, 5.9 and 5.10 that as the device dimensions increase, the variations decrease and the corresponding writing yield increases, and in small memristor dimensions the yield improvement ratio is larger than the yield improvement ratio in big size. For example in case ( $D=3$ , and  $l=z=10\text{nm}$ ) the yield improve ratio equal 2.53% and in case ( $D=15$ , and  $l=z=10\text{nm}$ ) the yield improve ratio equal 1.42% but in case ( $D=15$ , and  $l=z=100\text{nm}$ ) the yield improve ratio equal 0.9%.

Table 5.3 shows the yield's values before and after the variation compensation with clearing  $\sigma_y$  (variation parameter) and  $\text{TiO}_2$  dimensions value.

| D  | L=z  | $\sigma_y$ | Writing Yield before variation compensation | Optimized Writing Yield after variation compensation |
|----|------|------------|---|--|
| 3n | 10n  | 1.1879     | 89.67%                                      | 92.2%  |
|    | 30n  | 1.1185     | 93.29%                                      | 94.9%  |
|    | 50n  | 1.04       | 96.43%                                      | 97.23%   |
|    | 70n  | 0.9947     | 97.73%                                      | 98.22%   |
|    | 100n | 0.9515     | 98.63%                                      | 98.91%   |
|    | 10n  | 1.115      | 93.89%                                      | 94.91%   |
|    | 30n  | 1.06       | 96.03%                                      | 96.62%   |

|     |       |        |        |        |
|-----|-------|--------|--------|--------|
| 6n  | 50n   | .9812  | 98.19% | 98.38% |
|     | 70nm  | 0.9366 | 98.96% | 99.05% |
|     | 100nm | 0.8921 | 99.46% | 99.50% |
| 10n | 10nm  | 1.03   | 97.05% | 97.08% |
|     | 30nm  | 0.9785 | 98.20% | 98.23% |
|     | 50nm  | 0.9064 | 99.24% | 99.29% |
|     | 70nm  | 0.8652 | 99.58% | 99.63% |
|     | 100nm | 0.8199 | 99.80% | 99.85% |
| 15n | 10n   | 0.9986 | 96.13% | 97.55% |
|     | 30n   | 0.9486 | 97.17% | 98.63% |
|     | 50n   | 0.8787 | 98.26% | 99.51% |
|     | 70n   | 0.8388 | 98.73% | 99.97% |
|     | 100n  | 0.7989 | 99.09% | 99.9%  |

**Table 5.3: Yields values before and after variation compensation.**

## 5.4 TiO<sub>2</sub> Reading Yield Optimization

In the case of reading '1' which dominates the failure probability as explained earlier, the device's memristance,  $M'$ , is compared to a certain threshold which is selected to be 50% (mid-way) between  $R_{on}$  and  $R_{off}$ , typically,  $[(R_{on} + R_{off})/2]$ . As shown in Figure 5.11.

$R_{ON}$

50%

$R_{off}$

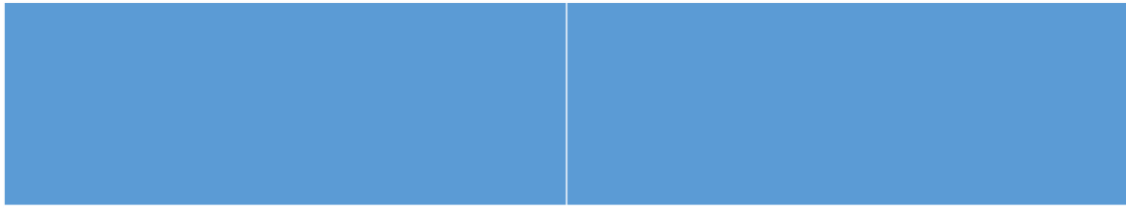


Figure 5.11: The threshold point at  $TiO_2$  memristor.

To optimize the reading yield, this threshold has been varied to find the optimal threshold those results in maximum reading yield. The reading yield is defined in a similar way as the writing yield. In order to maximize the reading yield, the threshold is changed to achieve the maximum possible reading yield.

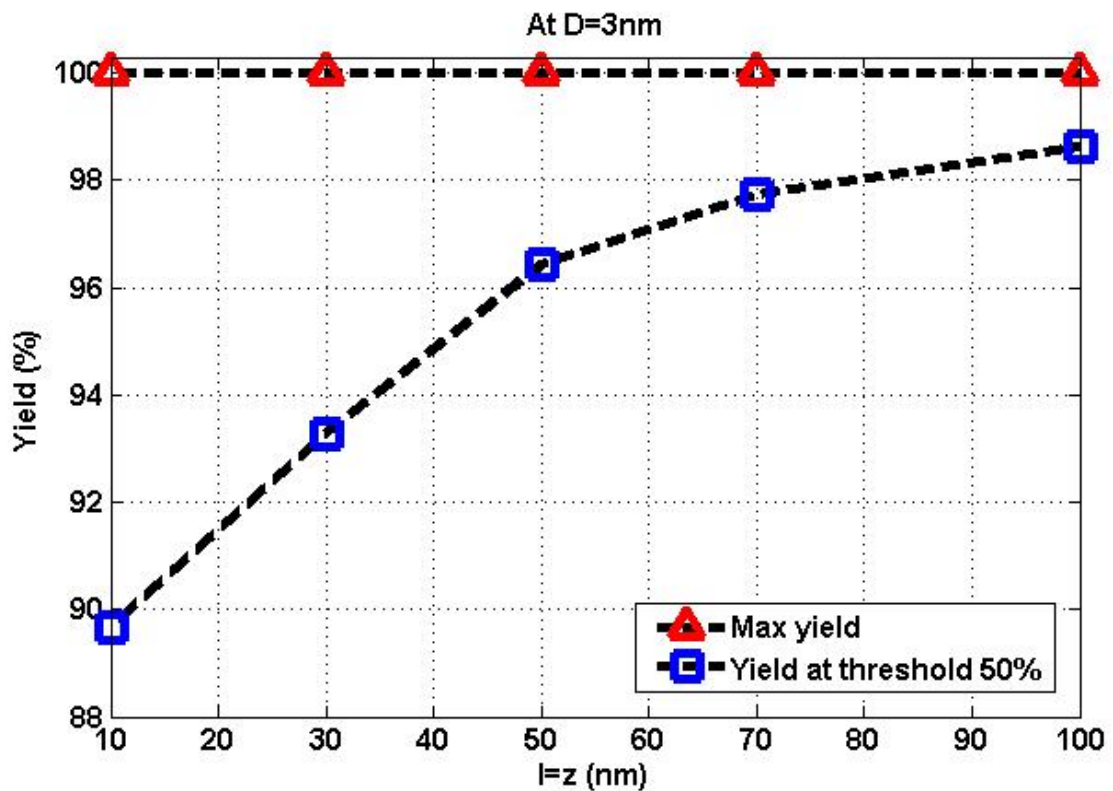


Figure 5.12: Max reading yield in case  $D=3nm$ .

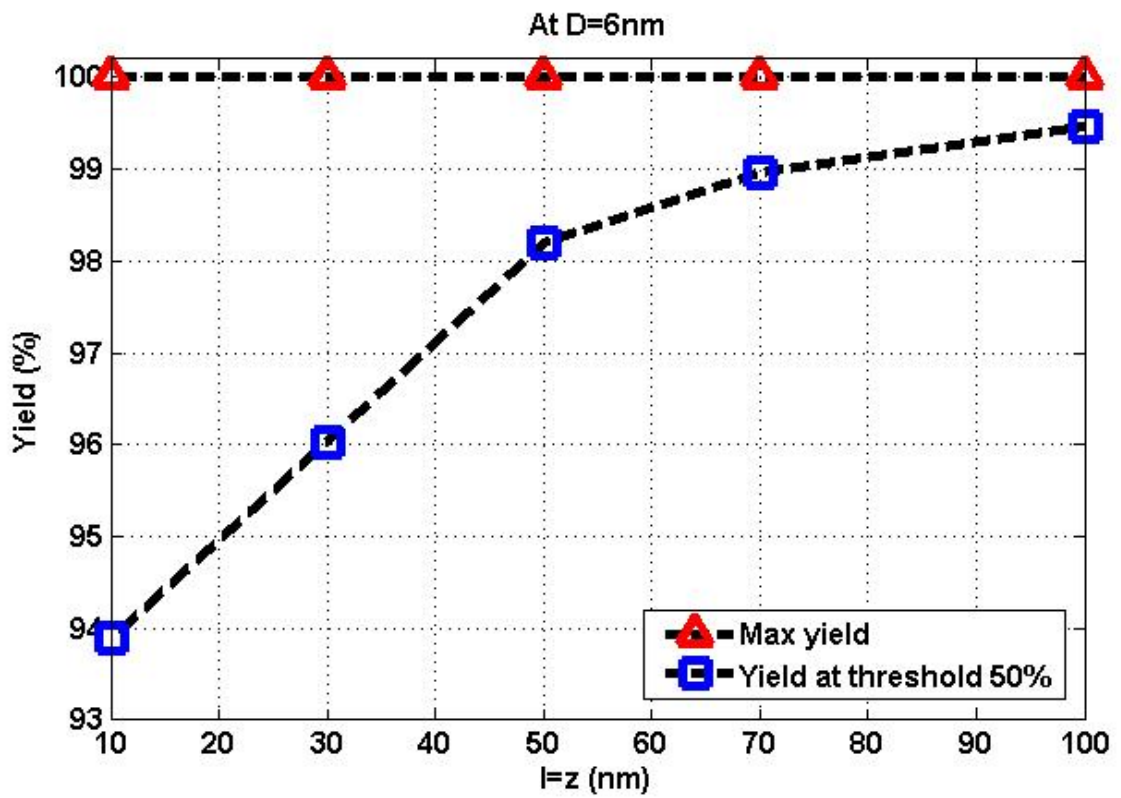


Figure 5.13: Max reading yield in case D=6nm.

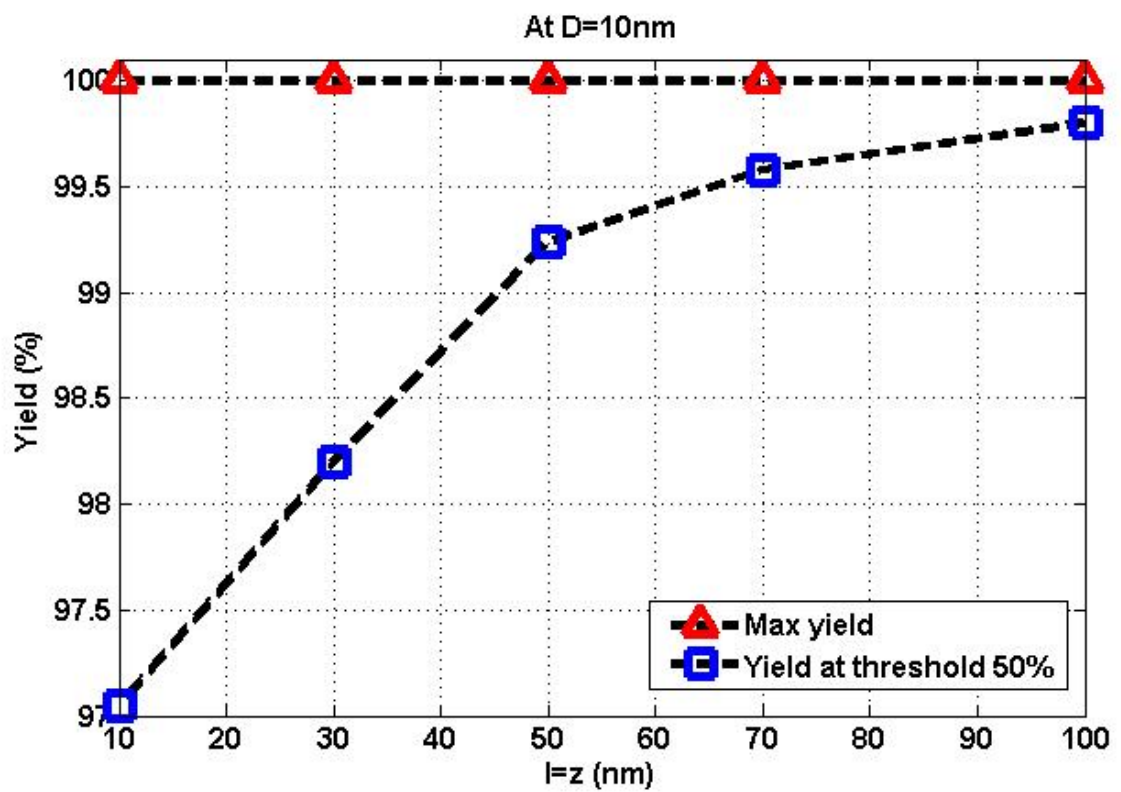
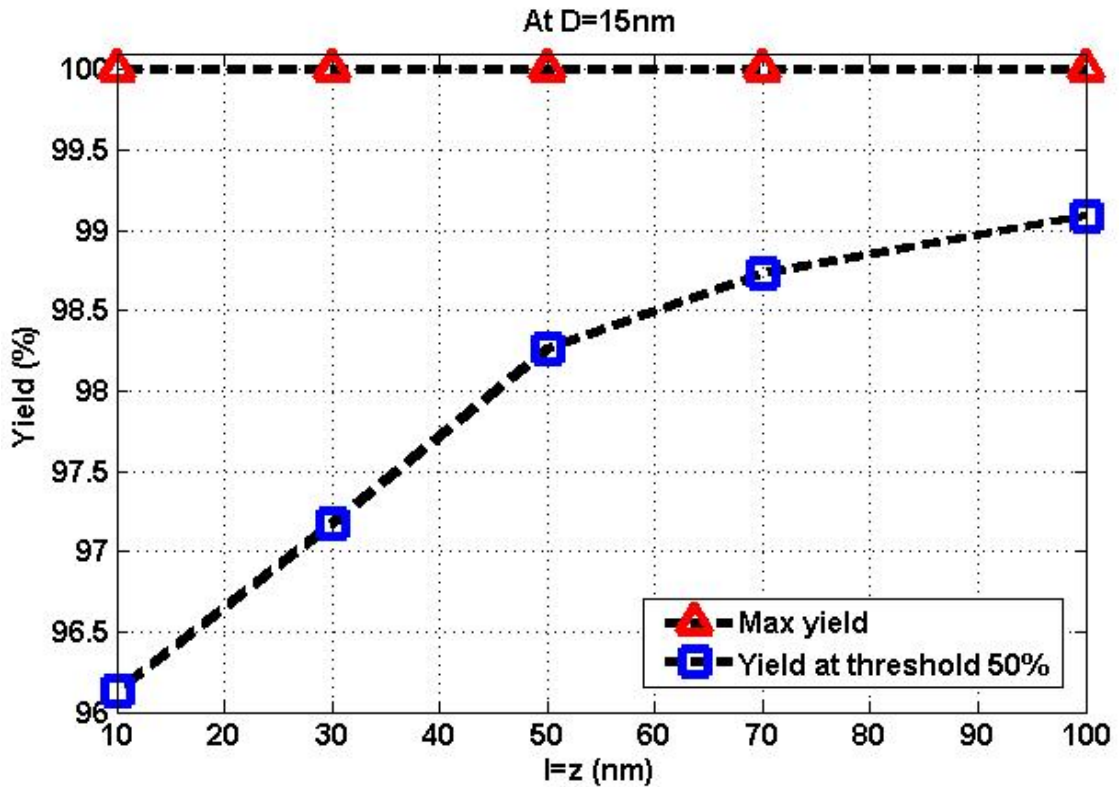


Figure 5.14: Max reading yield in case D=10nm.



**Figure 5.15: Max reading yield in case D=15nm.**

In Figures 5.12, 5.13, 5.14, and 5.15, the reading yield achieved when the threshold is selected at 50% is plotted versus the maximum reading yield achieved when the optimal threshold values are used for different memristor device' dimensions, we take four samples which the thickness  $D=3\text{nm}$ ,  $D=6\text{nm}$ ,  $D=10\text{nm}$ , and  $D=15\text{nm}$  with the length  $l$  equal to the width  $z$  and varied from  $10\text{nm}$  to  $100\text{nm}$ .

In Figure 5.12,  $D=3\text{nm}$  and  $l, z$  vary from  $10\text{nm}$  to  $100\text{nm}$ , for example: when the 50% threshold is used, the reading yield equals  $89.67\%$  at  $l=z=10\text{nm}$  and equals  $98.63\%$  at  $l=z=100\text{nm}$ . However, when the optimal threshold is adopted, the reading yield equals  $100\%$  in all cases of  $l, z$ .

In Figures 5.13, 5.14, and 5.15; for  $D = 6\text{nm}$ ,  $D=10\text{nm}$  and  $D=15\text{nm}$  also when the optimal threshold is adopted, the reading yield equals  $100\%$  in all cases of  $l, z$ .

# Chapter 6

## Compact model of Spintronic Memristor under Process Variations, and Simulation Results

### 6.1 The Spintronic Memristor Compact Model

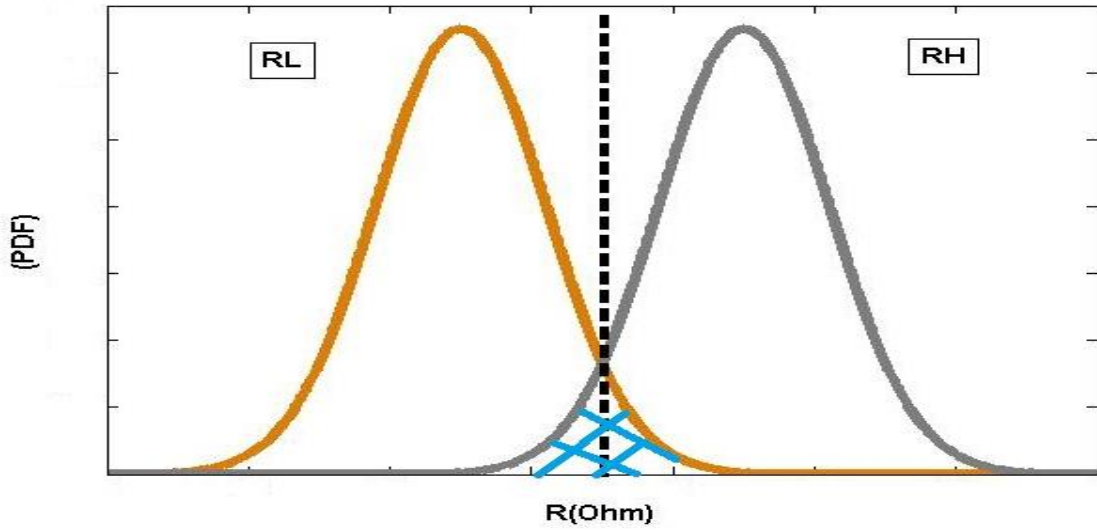
The impact of process variations is affecting the device performance by deviating the actual electrical behavior of the memristor ( $r_L$ ,  $r_H$ , and  $\alpha$ ) from the desired values (failure in write/read digital logic 1/0).

This deviation results in reducing the yield. Yield= (1- failure), also the yield is defined as the number of memristor cells which have a right write/read.

We observed from our calculations that the failure percentage in the case of writing / reading '0' is much lower than that in the case of writing/reading '1', as we defined a memristor is at logic zero when  $M=r_H$  and a memristor is at logic one when  $M=r_L$ . The process variation effect is larger on the  $r_L$  than  $r_H$ ; as  $r_H$  has a larger value than  $r_L$ ;  $r_H \cong 10 * r_L$ .

Very recently, a Monte-Carlo simulation method was proposed to analyze the impact of geometry variations on the electrical properties of the memristors [49-54]. A 3D device structure including the geometry variation information is generated by performing a sanity check of the device characterization parameters. In the Monte-Carlo simulations, the memristor device is divided into many small filaments sandwiched between two electrodes. Within a filament  $i$ , the cross-section area  $s_i' = l_i' \cdot z_i'$  and thickness  $D_i'$ , considered as constants, whose value can be modeled by taking into account the effects of LER or OTF, respectively.

A compact model was proposed to generate a large volume of process variation-aware three-dimensional device structures for Monte-Carlo simulations. We did 5000 samples to each point in our simulations. Therefore, it is very important to understand and characterize the impact of process variation on memristor performance and yield and attempt to optimize the yield. Figure 6.1 shows the PDF Monte-Carlo of  $R_{on}$  and  $R_{off}$ , and the cross failure due to variation. The cross section between the  $R_{on}$  PDF and  $R_{off}$  PDF is the failure region in which write/read operation is wrong.



**Figure 6.1: PDF of  $R_{ON}$  and  $R_{OFF}$ , the cross failure region.**

### 1) Memristance at domain wall position $x$

If considering the width of domain wall  $w$  and assuming that the resistance per unit length of the thin film strip changes linearly from  $r_L$  to  $r_H$  within the domain wall, the overall memristance of such a spintronic memristor can be calculated as:

$$M(\alpha) = [r_L \cdot \alpha + r_H \cdot (1 - \alpha)], \quad (29)$$

for  $0 < x < D$  and  $\alpha = x/D$ . Here  $M(\alpha)$  does not depend on the width of domain wall [3, 6-7].



## 2) Current density $J$ and effective current density $J_{\text{eff}}$

The current density  $J$  in a spintronic memristor can be calculated as [7]:

$$J = \frac{V}{M(\alpha).h.z}. \quad (30)$$

Where,  $V$  is the voltage applied to the spintronic memristor.  $h$  and  $z$  are the thickness and the width of spin-valve strip, respectively. The effective current density  $J_{\text{eff}}$  of a spintronic memristor can be calculated as [3]:

$$J_{\text{eff}} = \begin{cases} J, & \text{when } J > J_{cr} \\ 0, & \text{when } J < J_{cr} \end{cases}. \quad (31)$$

The critical current density  $J_{cr}$  can be defined and different from model to another.

## 3) Analysis the spintronic memristor model under the process variation

In our model, the memristor variations and yield analysis are taken into account. The yield is defined as the number of memristors that exhibit correct writing/read operation. Here, we will derive the corresponding process-variation aware memristance model, and summarize the designed values of the spintronic memristor geometry dimensions and its electrical parameters adopted in our work. For a given spintronic memristor, we use  $r_H'$  and  $r_L'$  to denote its actual highest and lowest total memristance, respectively [6-7].

$$r_H' = r_H \cdot (\mu_{r_H} + \sigma_{r_H} \cdot E) \cdot (1 + \sigma_y \cdot D_y) \quad (32)$$

$$r_L' = r_L \cdot (\mu_{r_L} + \sigma_{r_L} \cdot E) \quad (33)$$

Here, two independent random numbers  $E \sim N(0,1)$  and  $D_y \sim N(0,1)$  are introduced.  $E$  represents the correlation between  $r_H'$  and  $r_L'$  due to the same geometry variation sources  $D_y$  and  $\sigma_y$  represents the impact of RDD.  $\mu_{r_H}$ ,  $\mu_{r_L}$ ,  $\sigma_{r_H}$ , and  $\sigma_{r_L}$  are the variation

parameters. By running extensive numerical simulations under various conditions, we found the actual  $\alpha'$  can be modeled as the product of the designed value  $\alpha$  and a coefficient  $\eta$  that represents the influence of process variations as [6-7]:

$$\alpha' = \eta \cdot \alpha \quad (34)$$

Here  $\eta$  can be expressed by [6, 7]:

$$\eta = \frac{1}{(1 + J \cdot \varepsilon_1 + J \cdot \varepsilon_2 (\omega_1 \cdot E + \omega_2 \cdot G)) \cdot (1 + \sigma_y \cdot D_y)} \quad (35)$$

To avoid overestimating the impact of geometry variations on  $\alpha'$ , a new random number  $G \sim N(0, 1)$  is introduced to offset the impact of LER.  $\varepsilon_1$  and  $\varepsilon_2$  are two scalars extracted from the actual simulations performed by the device simulator. The coefficients  $\omega_1$  and  $\omega_2$  represent the weights of  $E$  and  $G$ , where  $\omega_1^2 + \omega_2^2 = 1$ . By modeling  $r'_L$ ,  $r'_H$  and  $\alpha'$ , the total memristance  $M'$  of a Spintronic memristor can be simply calculated by:

$$M'(\alpha) = r'_L \cdot \alpha' + r'_H \cdot (1 - \alpha') \quad (36)$$

Table 6.1 shows the model variation parameters. Table 6.2 shows another variation parameter  $\sigma_y$  values which determined in Toronto – Canada by “COMSOL” help vary with the spintronic memristor dimensions  $h$ ,  $z$ , and  $D$  is as shown in Figure 6.2.

| Variation Parameters |       | Coefficients    |        |
|----------------------|-------|-----------------|--------|
| $\mu_{rH}$           | 0.994 | $\varepsilon_1$ | -0.028 |
| $\mu_{rL}$           | 0.994 | $\varepsilon_2$ | 0.072  |
| $\sigma_{rH}$        | 2.16% | $\omega_1$      | 0.98   |
| $\sigma_{rL}$        | 2.16% | $\omega_2$      | 0.2    |

**Table 6.1: The model parameters [52].**

| h, z    | D     | $\sigma_y$ | h, z     | D     | $\sigma_y$ |
|---------|-------|------------|----------|-------|------------|
| 7, 10nm | 100nm | 1.99       | 10, 15nm | 100nm | 1.543      |
|         | 200nm | 1.579      |          | 200nm | 1.225      |
|         | 300nm | 1.379      |          | 300nm | 1.07       |
|         | 400nm | 1.253      |          | 400nm | 0.9723     |
|         | 500nm | 1.163      |          | 500nm | 0.9026     |

| h, z    | D      | $\sigma_y$ | h, z     | D      | $\sigma_y$ |
|---------|--------|------------|----------|--------|------------|
| 7, 10nm | 600nm  | 1.095      | 10, 15nm | 600nm  | 0.8494     |
|         | 700nm  | 1.04       |          | 700nm  | 0.8069     |
|         | 800nm  | 0.995      |          | 800nm  | 0.771      |
|         | 900nm  | 0.9566     |          | 900nm  | 0.742      |
|         | 1000nm | 0.9236     |          | 1000nm | 0.716      |

**Table 6.2: Spintronic memristor dimensions and  $\sigma_y$  Values.**

## 6.2 Spintronic Memristor Yield without Variation Compensation

We take many example of spintronic memristor in different dimensions and did a mote-Carlo simulation to each case and calculate the yield before variation compensation. Figure 6.2 shows the spintronic memristor and its dimensions.

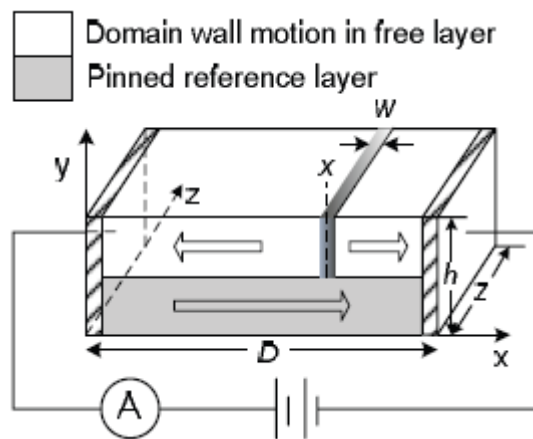


Figure 6.2: Spintronic memristor structure.

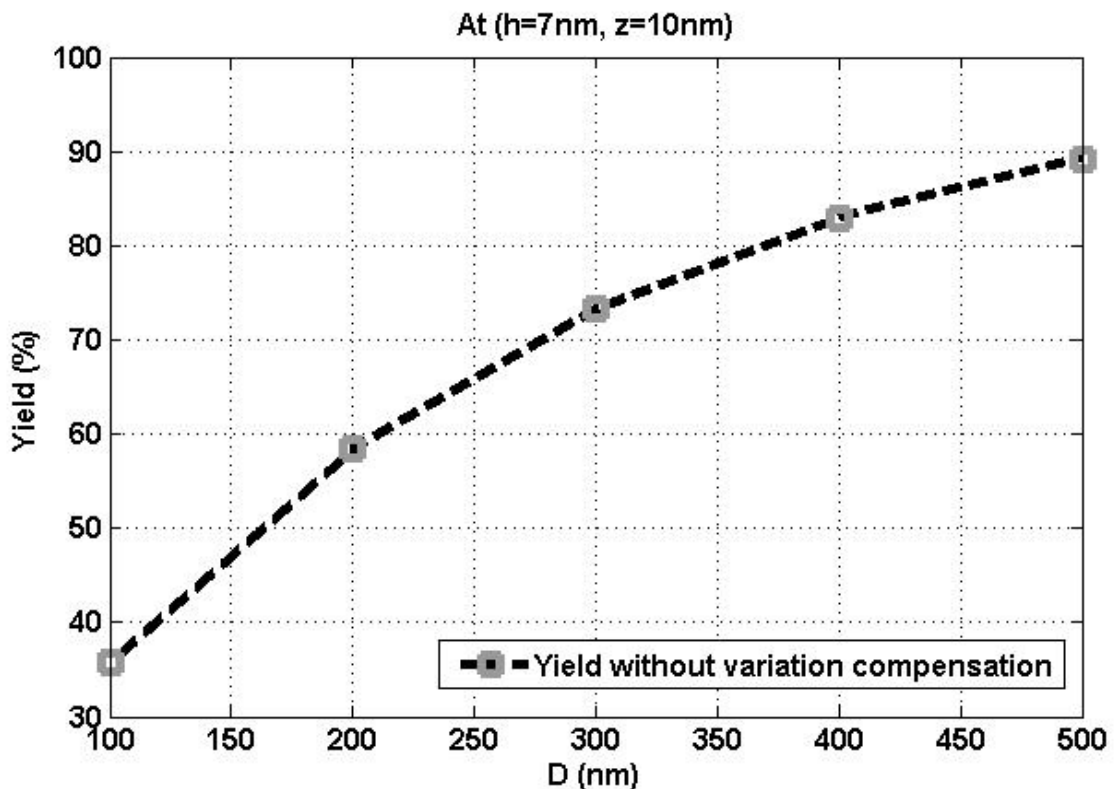


Figure 6.3: Yield without variation compensation at  $h=7\text{nm}$ ,  $z=10\text{nm}$  and  $D=100:500$ .

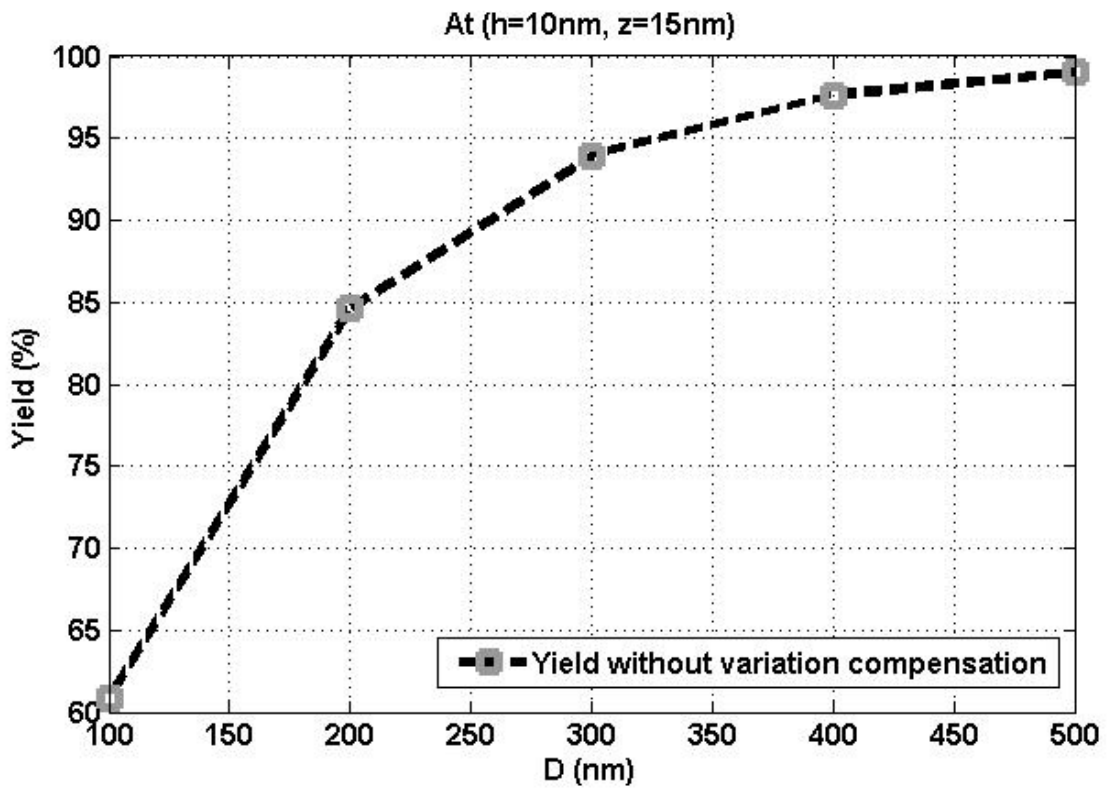


Figure 6.4: Yield without variation compensation at  $h=10\text{nm}$ ,  $z=15\text{nm}$  and  $D=100:500$ .

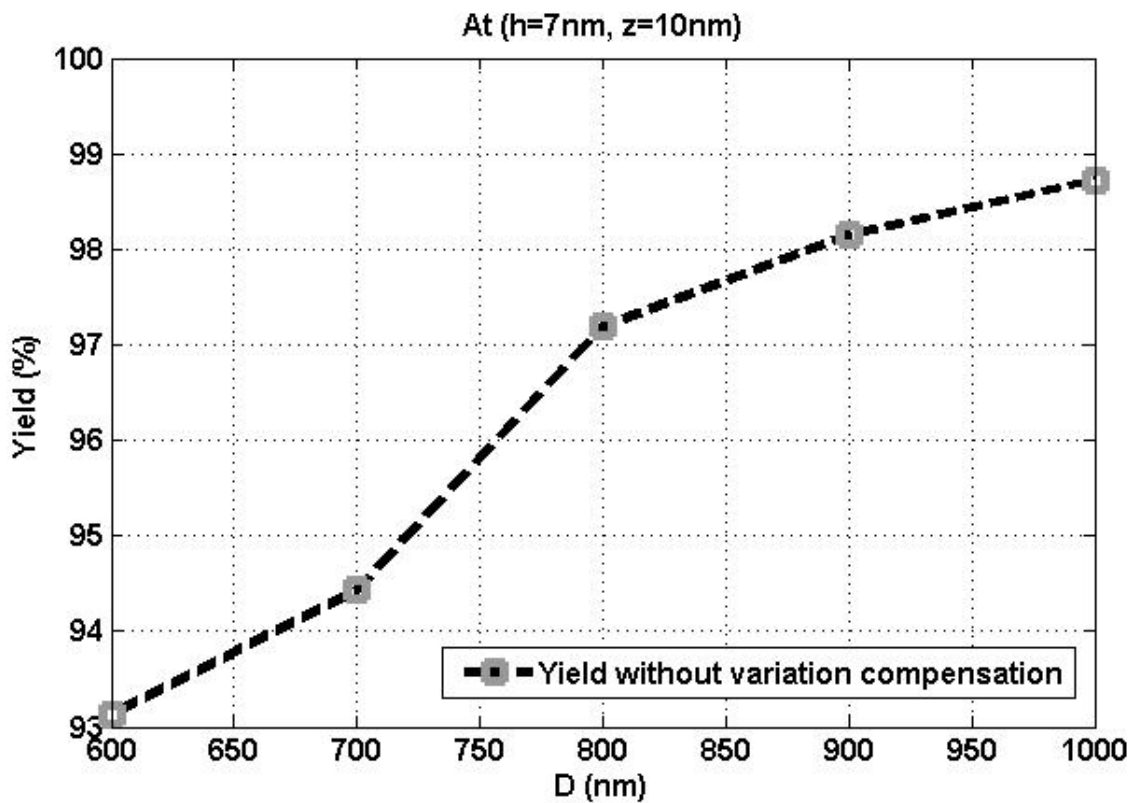
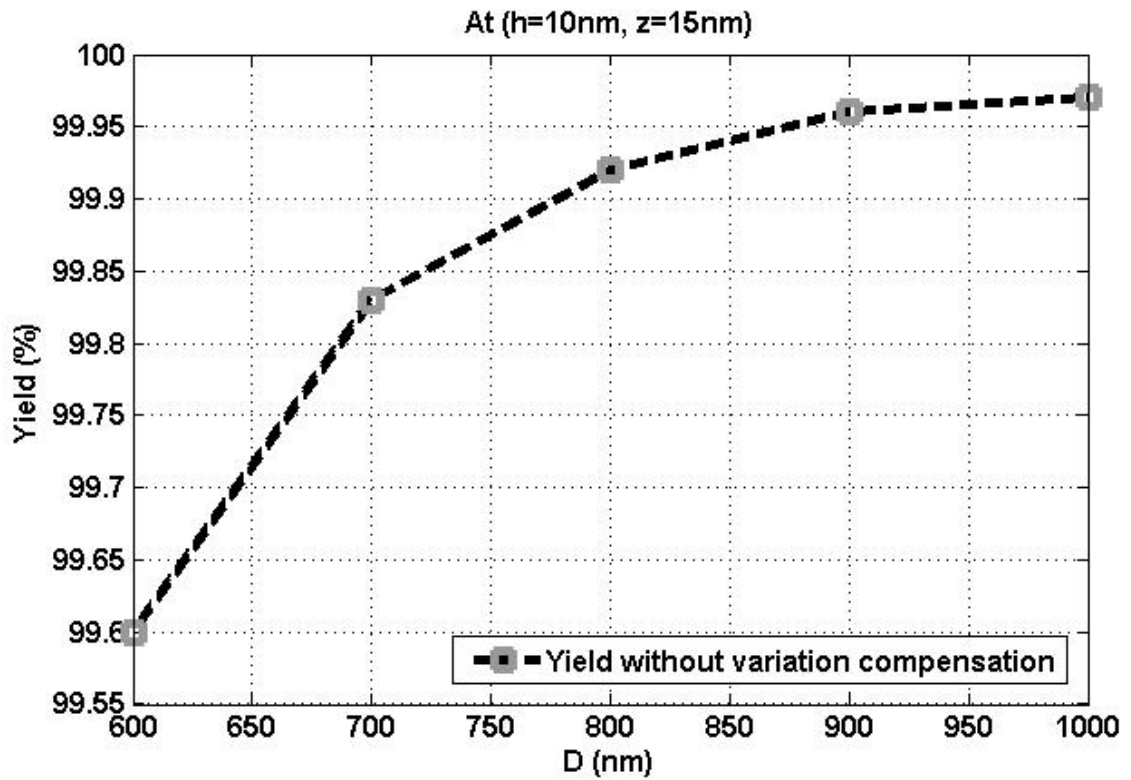


Figure 6.5: Yield without variation compensation at  $h=7\text{nm}$ ,  $z=10\text{nm}$  and  $D=600:1000$ .



**Figure 6.6: Yield without variation compensation at h=10nm, z=15nm and D=600:1000.**

Figure.6.3 shows the yield in case without variation compensation in case of Spintronic memristor (length  $h=7\text{nm}$ , width  $z=10\text{nm}$ ) vary with thickness  $D$  from 100nm to 500nm. At  $D=100\text{nm}$  the yield equal 35.71%, at  $D=200\text{nm}$  the yield equal 58.36%, %, at  $D=300\text{nm}$  the yield equal 73.25%, at  $D=400\text{nm}$  the yield equal 82.93%, and at  $D=500\text{nm}$  the yield equal 89.17%.

Figure.6.4 shows the yield in case without variation compensation in case of Spintronic memristor (length  $h=10\text{nm}$ , width  $z=15\text{nm}$ ) vary with thickness  $D$  from 100nm to 500nm. At  $D=100\text{nm}$  the yield equal 60.80%, at  $D=200\text{nm}$  the yield equal 84.59%, %, at  $D=300\text{nm}$  the yield equal 93.92%, at  $D=400\text{nm}$  the yield equal 97.60%, and at  $D=500\text{nm}$  the yield equal 99.03%.

Figure.6.5 shows the yield in case without variation compensation in case of Spintronic memristor (length  $h=7\text{nm}$ , width  $z=10\text{nm}$ ) vary with larger thickness  $D$  from 600nm to 1000nm. At  $D=600\text{nm}$  the yield equal 93.12%, at  $D=700\text{nm}$  the yield equal 94.34%, %, at  $D=800\text{nm}$  the yield equal 97.19%, at  $D=900\text{nm}$  the yield equal 98.15%, and at  $D=1000\text{nm}$  the yield equal 98.72%.

Figure.6.6 shows the yield in case without variation compensation in case of Spintronic memristor (length  $h=10\text{nm}$ , width  $z=15\text{nm}$ ) vary with larger thickness  $D$  from  $600\text{nm}$  to  $1000\text{nm}$ . At  $D=600\text{nm}$  the yield equal  $99.60\%$ , at  $D=700\text{nm}$  the yield equal  $99.83\%$ , %, at  $D=800\text{nm}$  the yield equal  $99.92\%$ , at  $D=900\text{nm}$  the yield equal  $99.96\%$ , and at  $D=1000\text{nm}$  the yield equal  $99.97\%$ .

### 6.3 Spintronic Memristor Writing Yield Optimization

In the case of the writing '1' operation, the input writing current density should be adjusted to change the memristor device's memristance from  $r_H$  to  $r_L$ , which is given by equation (9). In this case, all the memristor devices should have their Memristance  $M'$  less than a given threshold (normally selected to be midway between  $r_L$  and  $r_H$ , typically,  $[(r_L + r_H)/2]$ ) normally as  $\text{TiO}_2$  memristor. Since in the case of  $\alpha=1$ , the ideal memristance without variations should equal  $r_L$ , variations result in making the memristance of some memristor devices deviates from  $r_L$  and becomes larger than the threshold. The writing yield is defined as the number of memristors samples (out of 5000 samples in our simulations) that exhibit correct writing operation (i.e., their memristance is less than the mid-way threshold when variations is taken into account) typically as used in  $\text{TiO}_2$  thin film memristor.

In order to maximize the writing yield, the input current density is changed by changing the input current amplitude to achieve the maximum possible writing yield. The following simulation results provide an important design insight to the memristor-based memory array designers as follows. If the designer ignores the variations and find only the input writing current density that changes the memristance value from  $r_H$  to  $r_L$ , this current will not achieve the optimize writing yield as shown in figures. 6.7 to 6.10. However, if the designer considers the variations, a new current density value should be used that results in optimize the yield. Here, the writing yield is defined as the percentage of memory cells that are written correctly (i.e., the cells that are written as '1' when they are desired to store '1' with no failure). Once again, the case of writing '0' provide very small failure probability compared to the writing '1' case.

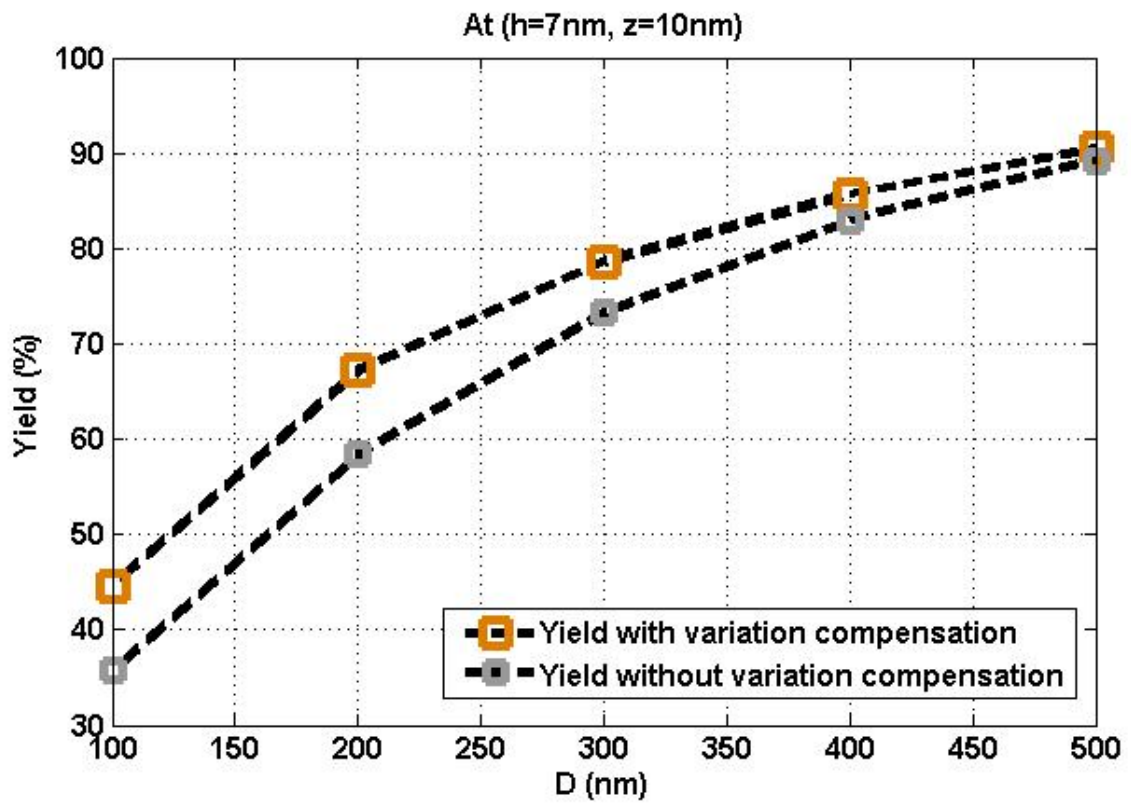


Figure 6.7: Writing yield at case  $h=7\text{nm}$  and  $z=10\text{nm}$  and  $D=100:500$ .

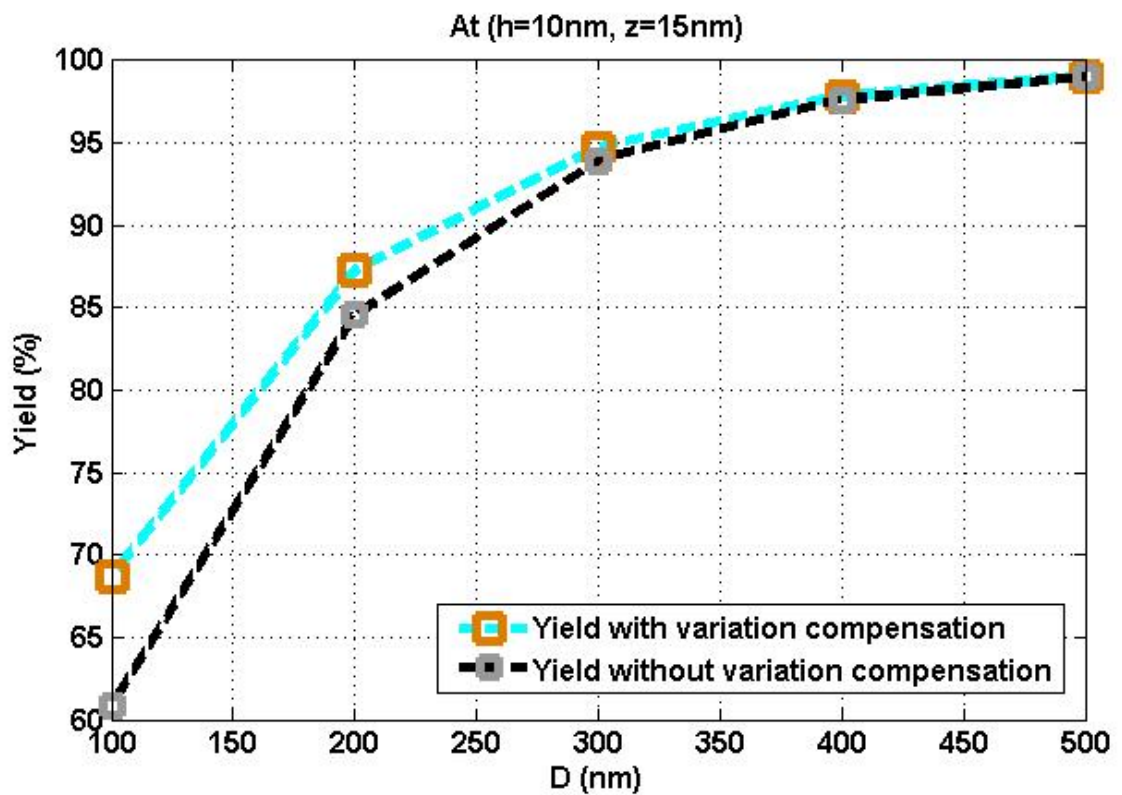


Figure 6.8: Writing yield at case  $h=10\text{nm}$  and  $z=15\text{nm}$  and  $D=100:500$ .



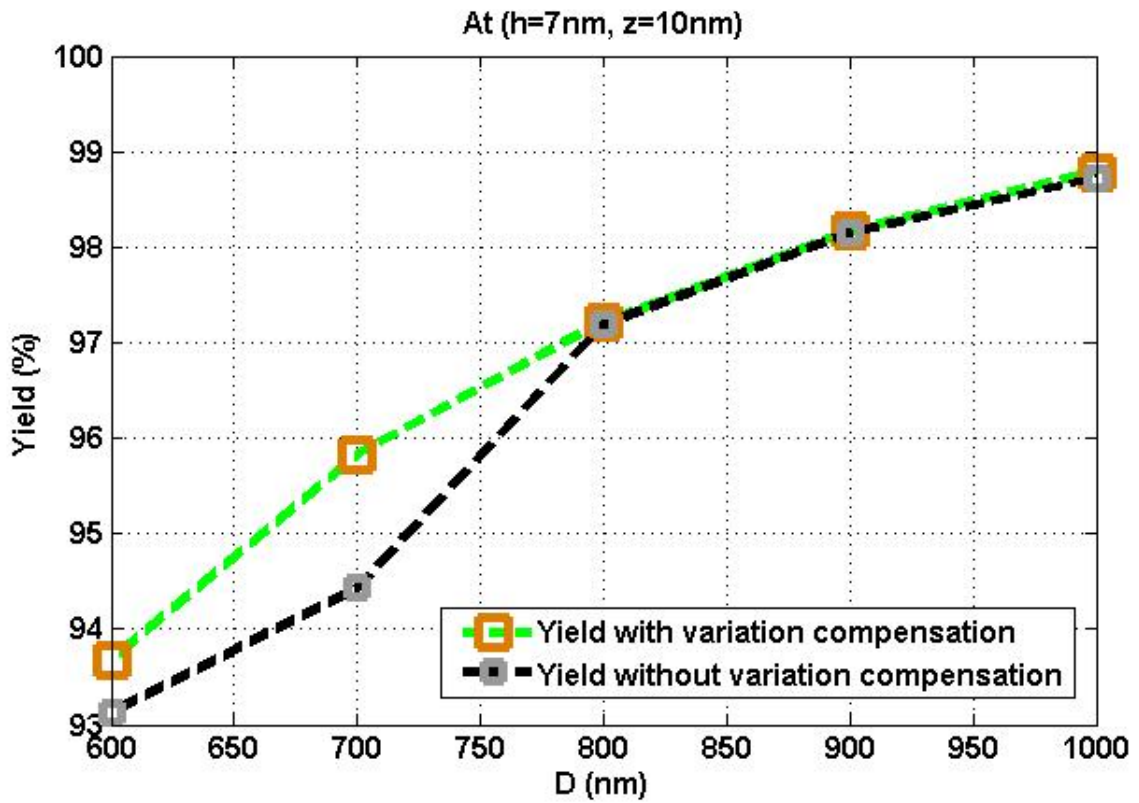


Figure 6.9: Writing yield at case h=7nm and z=10nm and D=600:1000.

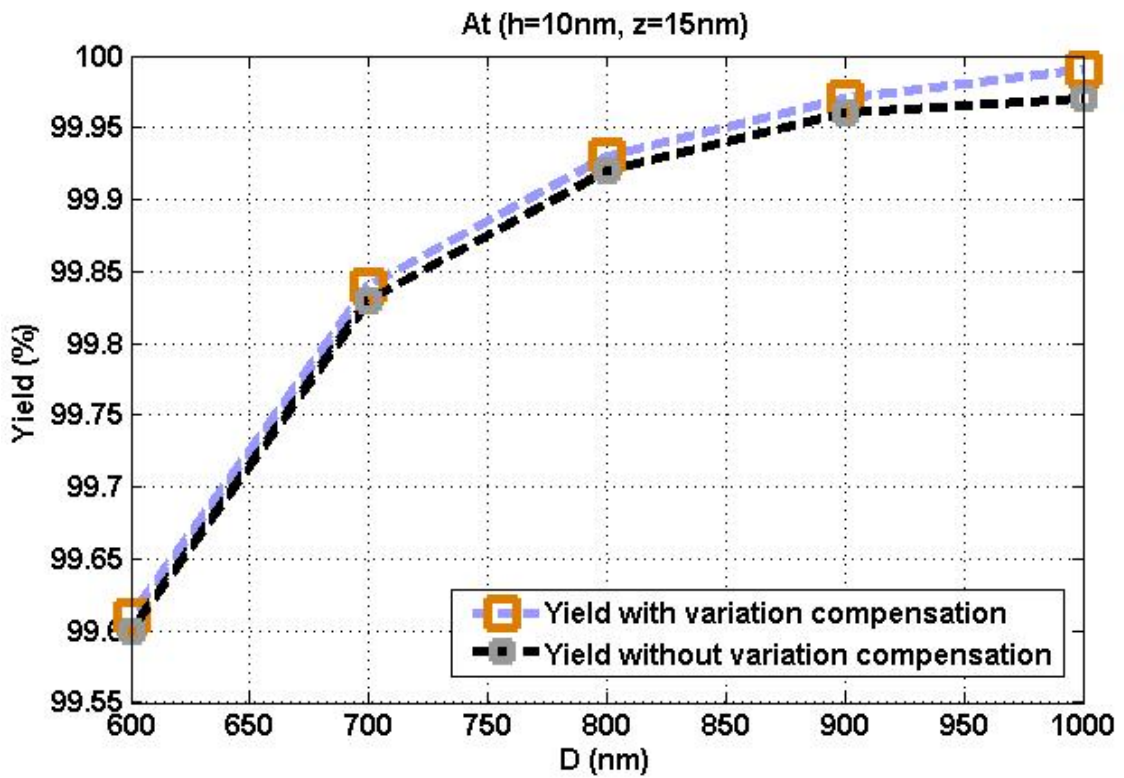


Figure 6.10: Writing yield at case h=7nm and z=10nm and D=600:1000.

Figures 6.7, 6.8, 6.9, and 6.10 portray of the writing yield for different memristor sizes when the normal input writing current density given in equation (11) is used (i.e., no writing yield optimization and the variations are not compensated) and when the optimal input writing current density is used (i.e., the writing yield is optimized and the variations are taken into account).

In figure 6.7, the case that the length  $h=7\text{nm}$  and the width  $z=10\text{nm}$  with thickness  $D$  vary from  $100\text{nm}$  to  $500\text{nm}$ . When  $D=100\text{nm}$ , the device yield equals  $35.71\%$  without variation compensation whereas, the device yield equals  $44.65\%$ , after the variation compensation (selected optimal current). When  $D=200\text{nm}$ , the device yield equals  $58.36\%$  and after selected the optimal current it is improved to  $67.18\%$ . When  $D=300\text{nm}$ , the device yield improved from  $73.25\%$  to  $78.61\%$  after the variation compensation. When  $D=400\text{nm}$ , the device yield improved from  $82.17\%$  to  $85.68\%$  after the variation compensation. Also when  $D=500\text{nm}$ , the device yield improved from  $89.17\%$  to  $90.47\%$  after the variation compensation.

In figure 6.8, the case that the length  $h=10\text{nm}$  and the width  $z=15\text{nm}$  with thickness  $D$  vary from  $100\text{nm}$  to  $500\text{nm}$ . When  $D=100\text{nm}$ , the device yield equals  $60.80\%$  without variation compensation whereas, the device yield equals  $86.73\%$ , after the variation compensation (selected optimal current). When  $D=200\text{nm}$ , the device yield equals  $84.59\%$  and after selected the optimal current it is improved to  $87.22\%$ . When  $D=300\text{nm}$ , the device yield improved from  $93.92\%$  to  $94.70\%$  after the variation compensation. When  $D=400\text{nm}$ , the device yield improved from  $97.60\%$  to  $97.81\%$  after the variation compensation. Also when  $D=500\text{nm}$ , the device yield improved from  $99.03\%$  to  $99.08\%$  after the variation compensation.

In figure 6.9, the case that the length  $h=7\text{nm}$  and the width  $z=10\text{nm}$  with thickness  $D$  vary from  $600\text{nm}$  to  $1000\text{nm}$ . When  $D=600\text{nm}$ , the device yield equals  $93.12\%$  without variation compensation whereas, the device yield equals  $93.68\%$ , after the variation compensation (selected optimal current). When  $D=700\text{nm}$ , the device yield equals  $94.43\%$  and after selected the optimal current it is improved to  $95.83\%$ . When  $D=800\text{nm}$ , the device yield improved from  $97.19\%$  to  $97.22\%$  after the variation compensation. When  $D=900\text{nm}$ , the device yield improved from  $98.15\%$  to  $98.17\%$  after the variation compensation. Also when  $D=1000\text{nm}$ , the device yield improved from  $98.72\%$  to  $98.78\%$  after the variation compensation.

In figure 6.10, the case that the length  $h=10\text{nm}$  and the width  $z=15\text{nm}$  with thickness  $D$  vary from  $600\text{nm}$  to  $1000\text{nm}$ . When  $D=600\text{nm}$ , the device yield equals  $99.60\%$  without variation compensation whereas, the device yield equals  $99.61\%$ , after the variation compensation (selected optimal current). When  $D=700\text{nm}$ , the device yield equals  $99.83\%$  and after selected the optimal current it is improved to  $99.84\%$ . When  $D=800\text{nm}$ , the device yield improved from  $99.92\%$  to  $99.93\%$  after the variation compensation. When  $D=900\text{nm}$ , the device yield improved from  $99.96\%$  to  $99.97\%$  after the variation compensation. Also when  $D=1000\text{nm}$ , the device yield improved from  $99.97\%$  to  $99.99\%$  after the variation compensation.

It is observed from figures 6.7, 6.8, 6.9, and 6.10 that a new optimal current density value improved the yield. In addition, when the device dimensions increase, the variations decrease and the corresponding writing yield increases. Also, in small memristor dimensions the yield improvement ratio is larger than the yield improvement ratio in big size. Table 6.3 shows the all spintronic memristor cases values.

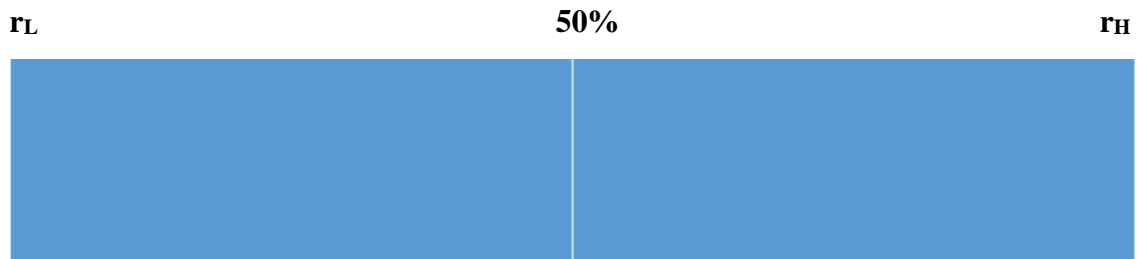
| h, z    | D      | $\sigma_y$ | Writing Yield before variation compensation | Writing Yield after variation compensation |
|---------|--------|------------|---|--|
| 7, 10nm | 100nm  | 1.99       | 35.71%                                      | 44.65%                                     |
|         | 200nm  | 1.579      | 58.36%                                      | 67.18%                                     |
|         | 300nm  | 1.379      | 73.25%                                      | 78.71%                                     |
|         | 400nm  | 1.253      | 82.93%                                      | 85.68%                                     |
|         | 500nm  | 1.163      | 89.17%                                      | 90.47%                                     |
|         | 600nm  | 1.095      | 93.12%                                      | 93.68%                                     |
|         | 700nm  | 1.04       | 94.43%                                      | 95.83%                                     |
|         | 800nm  | 0.995      | 97.19%                                      | 97.22%                                     |
|         | 900nm  | 0.9566     | 98.15%                                      | 98.17%                                     |
|         | 1000nm | 0.9236     | 98.72%                                      | 98.78%                                     |

| h, z     | D      | $\sigma_y$ | Writing Yield before variation compensation | Writing Yield after variation compensation |
|----------|--------|------------|---|--|
| 10, 15nm | 100nm  | 1.543      | 60.80%                                      | 68.73%                                     |
|          | 200nm  | 1.225      | 84.59%                                      | 87.22%                                     |
|          | 300nm  | 1.07       | 93.92%                                      | 94.70%                                     |
|          | 400nm  | 0.9723     | 97.60%                                      | 97.81%                                     |
|          | 500nm  | 0.9026     | 99.03%                                      | 99.08%                                     |
|          | 600nm  | 0.8494     | 99.60%                                      | 99.61%                                     |
|          | 700nm  | 0.8069     | 99.83%                                      | 99.84%                                     |
|          | 800nm  | 0.771      | 99.92%                                      | 99.93%                                     |
|          | 900nm  | 0.742      | 99.96%                                      | 99.97%                                     |
|          | 1000nm | 0.716      | 99.97%                                      | 99.99%                                     |

**Table 6.3: Different size of spintronic memristor and their yield values before / after variation compensation.**

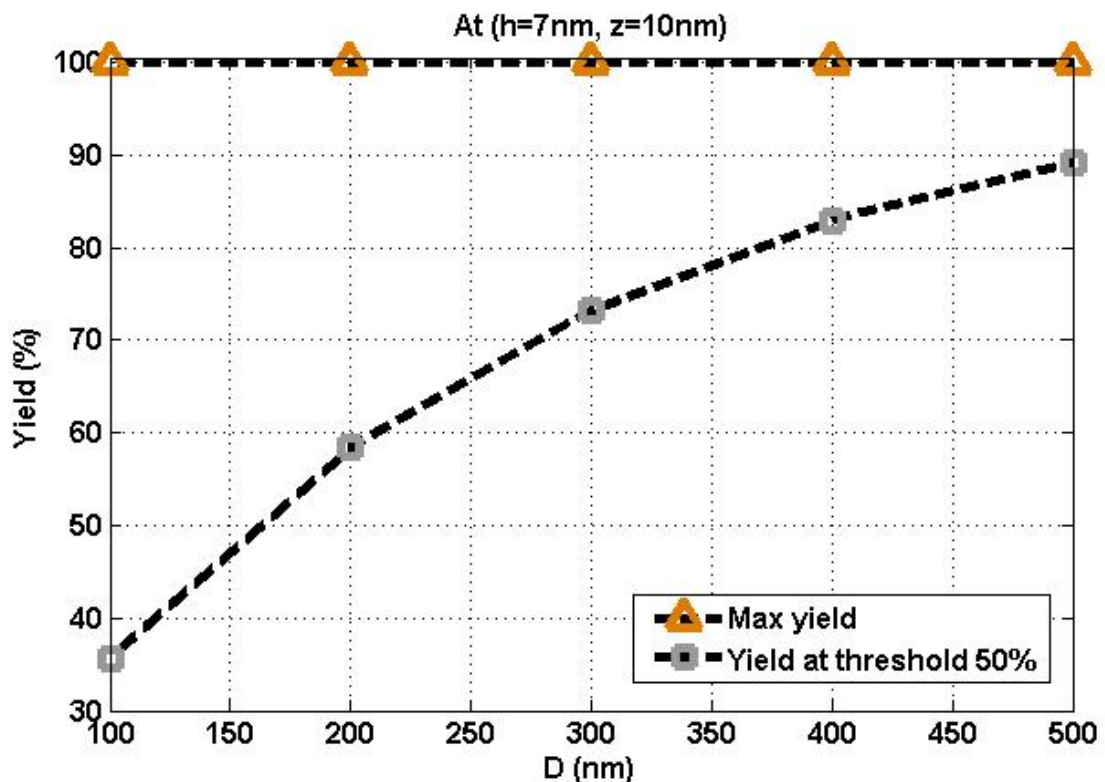
## 6.4 Spintronic Memristor Reading Yield Optimization

In the case of reading '1' which dominates the failure probability as explained earlier, the device's memristance,  $M'$ , is compared to a certain threshold which is selected to be 50% (mid-way) between  $r_L$  and  $r_H$ , typically,  $[(r_L + r_H)/2]$ . as shown in figure 6.11.



**Figure 6.11: The threshold point at spintronic memristor.**

To optimize the reading yield, this threshold has been varied to find the optimal threshold that results in optimize reading yield. The reading yield is defined in a similar way as the writing yield. In order to optimize the reading yield, the threshold is changed to achieve the possible optimization reading yield.



**Figure 6.12: Reading yield at case h=7nm, z=10nm and D=100:500.**

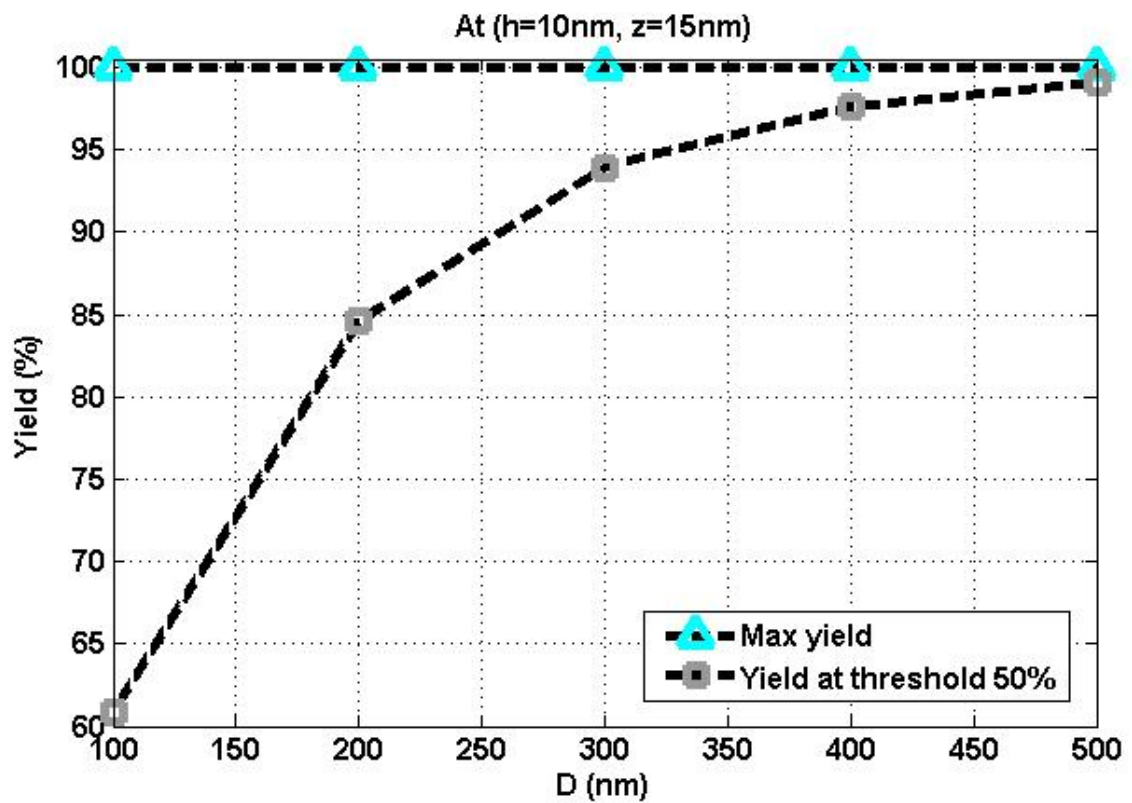


Figure 6.13: Reading yield at case h=10nm, z=15nm and D=100:500.

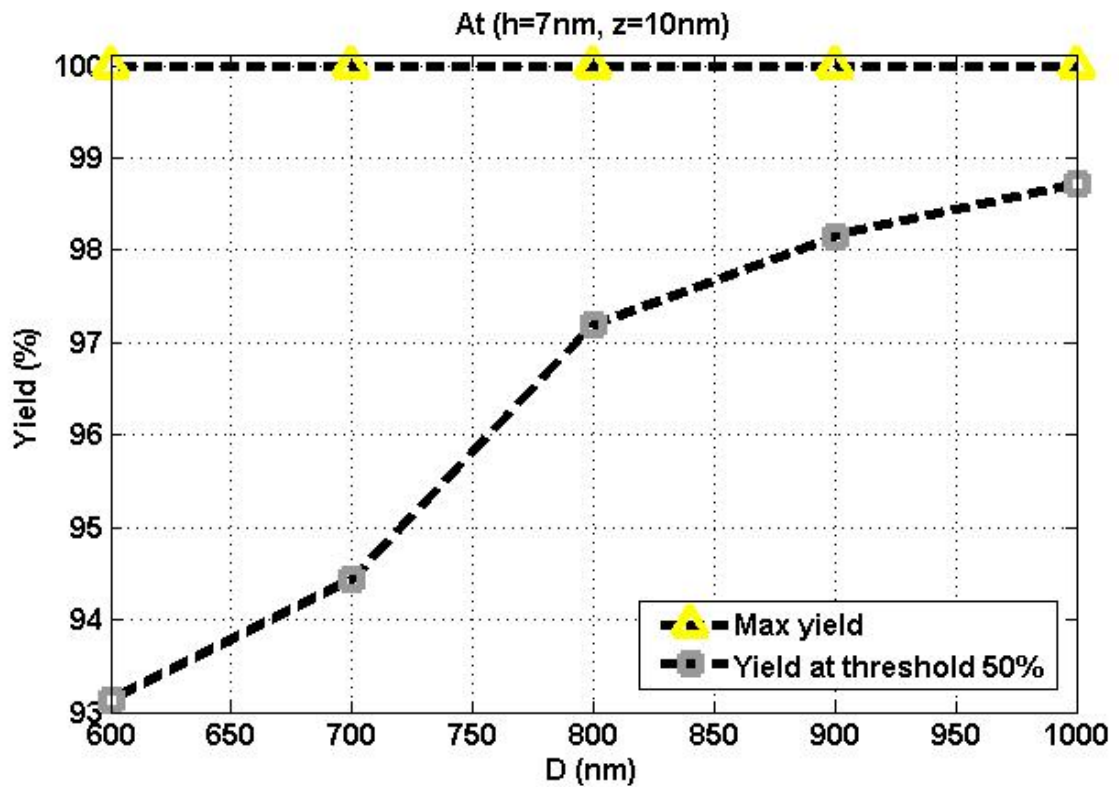


Figure 6.14: Reading yield at case h=7nm and z=10nm and D=600:1000.

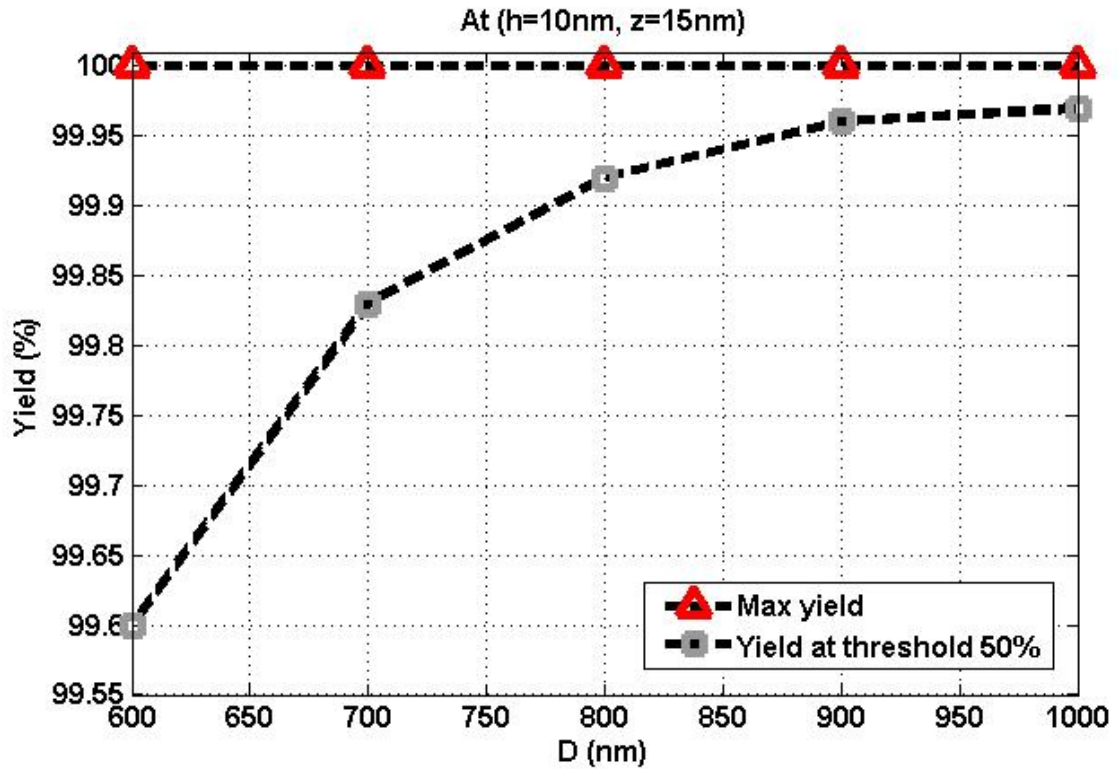


Figure 6.15: Reading yield at case  $h=10\text{nm}$  and  $z=15\text{nm}$  and  $D=600:1000$ .

In Figures 6.12, 6.13, 6.14, and 6.15, the reading yield achieved when the threshold is selected at 50% is plotted versus the maximum reading yield achieved when the optimal threshold values are used for different memristor device' dimensions, we take four samples which the thickness vary from  $D=100\text{nm}$  to  $500$  with the length  $l$  equal  $7\text{nm}$  and  $10\text{nm}$ ; the width  $z$  equal  $10\text{nm}$  and  $15\text{nm}$ , and the thickness vary from  $D=600\text{nm}$  to  $1000\text{nm}$ , with the length  $l$  equal  $7\text{nm}$  and  $10\text{nm}$ ; the width  $z$  equal  $10\text{nm}$  and  $15\text{nm}$ .

In figure 6.12, when the 50% threshold is used, the reading yield equals  $35.71\%$  at  $D=100\text{nm}$ , equals  $73.25\%$  at  $D=300\text{nm}$  and equals  $89.17\%$  at  $D=500\text{nm}$ . However, when the optimal threshold is adopted, the reading yield equals  $100\%$  in all cases.

It is observed from figures 6.13, 6.14, and 6.15 that a new technique of selecting the threshold point achieve great improvement in yield, the reading yield equals  $100\%$  in all cases when the optimal threshold is adopted.



## 6.4 Comparison between TiO<sub>2</sub> thin-film memristor and spintronic memristor simulation results

We tried to find a common point between the two types of memristors to make the comparison more clear. Figure 6.16 has shown the comparison between two memristor types yield values in a semi volume before variation compensation, and figure 6.17 has shown the comparison between two memristor types yield values in a semi volume after variation compensation in cases of selected flux and selected current to TiO<sub>2</sub> and spintronic memristor, respectively. For more spot, we handled two cases to the volume of two types of memristors is the same volume, case 30000nm and 150000nm.

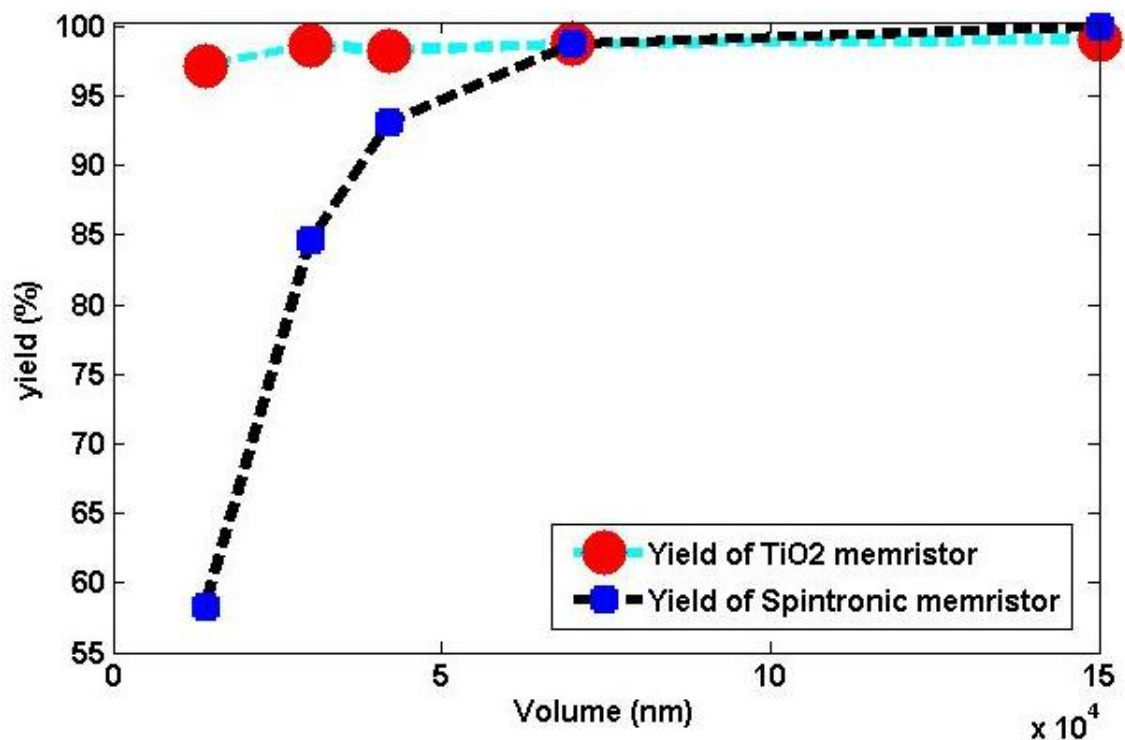
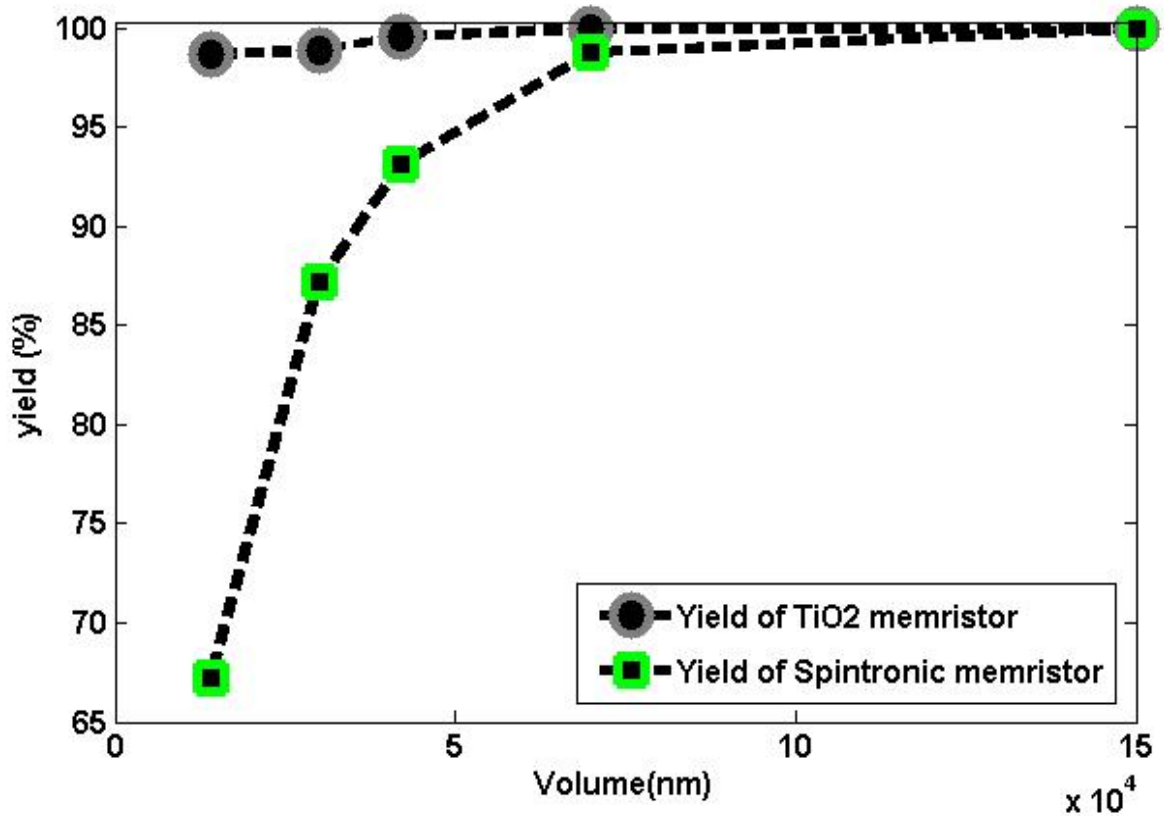


Figure 6.16: The yield of TiO<sub>2</sub> memristor and spintronic memristor in case without variation compensation.





**Figure 6.17: The writing yield of TiO<sub>2</sub> memristor and spintronic memristor in case with variation compensation.**

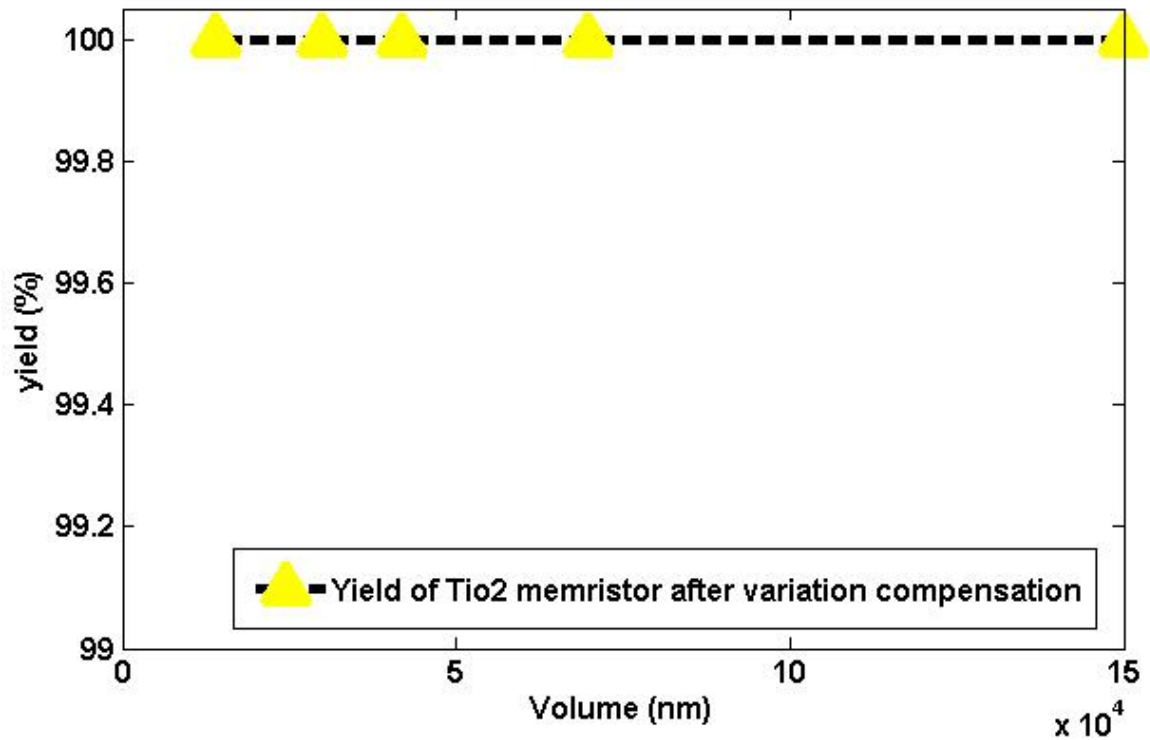
The case of memristors' volume equal to 30000nm<sup>3</sup>, TiO<sub>2</sub> memristor yield equal 98.63%, spintronic memristor yield equal 84.59% before variation compensation for two cases. TiO<sub>2</sub> memristor yield equal 98.91% after variation compensation by selected optimal flux, spintronic memristor yield equal 87.22% after variation compensation by selected optimal current density.

The case of memristors' volume equal to 150000nm<sup>3</sup>, TiO<sub>2</sub> memristor yield equal 99.09%, spintronic memristor yield equal to 9.97% before variation compensation for the two cases. TiO<sub>2</sub> memristor yield equal 99.99% after variation compensation by selected optimal flux, spintronic memristor yield equal 99.99% after variation compensation by selected optimal current density.

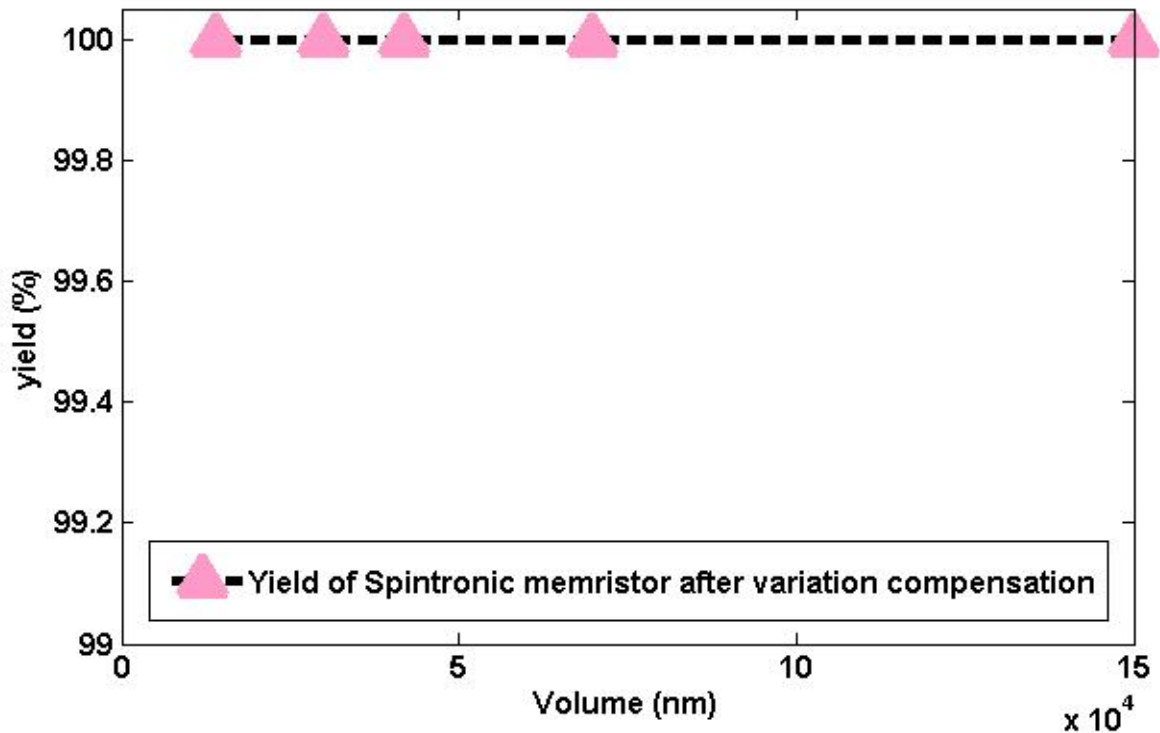
We notice that, the TiO<sub>2</sub> memristor has almost better result than the spintronic memristor after/before variation compensation as shown in figures 6.16, 6.17 respectively except the case of 150000nm volume, the spintronic memristor yield is

better than TiO<sub>2</sub> yield before the variation compensation but after the variation compensation the two yields is equally.

The second technique of variation compensation, selecting optimal threshold point achieve reading yield equal 100% to both type TiO<sub>2</sub> and spintronic memristor as shown in figures 6.18 and 6.19.



**Figure 6.18: The reading yield of TiO<sub>2</sub> memristor in case of after variation compensation with threshold point technique.**



**Figure 6.19: The reading yield of spintronic memristor in case of after variation compensation with threshold point technique.**

In general we have some notices:

- ♣ *The variations have an inverse proportional with the dimensions of the memristor.*
- ♣ *The yield has a direct proportional with the memristor dimensions.*
- ♣ *When the dimensions of the memristor increase the yield increase.*
- ♣ *In TiO<sub>2</sub> memristor, at small dimensions, the yield improves with a big ratio than large dimensions in cases of selected flux to variation compensation.*
- ♣ *In spintronic memristor, at small dimensions, the yield improves with a big ratio than large dimensions in cases of selected current density to variation compensation.*

- ♣ *In a semi small volume of TiO<sub>2</sub> and spintronic memristor, TiO<sub>2</sub> memristor gives better results for the yield value than the Spintronic memristor.*
- ♣ *In a big memristor volume the yield of TiO<sub>2</sub> and spintronic memristor is almost equal.*
- ♣ *In the threshold point selected technique to variation compensation, both TiO<sub>2</sub> and spintronic memristor achieve reading yield of 100%.*

# Chapter 7

## Conclusions and Future Work

### 7.1 Contributions

In this thesis, an overview of memory technologies usable memories and emerging memories are discussed. The physics behind different memristors types is discussed in light of the current state of the art and provided a comparative review between two of the most promising memristor physical realization (i.e., TiO<sub>2</sub> thin film memristor and spintronic memristor). We evaluate the impact of process variations to the electrical properties of TiO<sub>2</sub> thin-film memristors and spintronic memristor, by conducting the analytic modeling analysis and Monte-Carlo simulations. This thesis has attempted to improve the device writing and reading yields by finding the optimal writing input flux for TiO<sub>2</sub> memristor and the optimal current density for spintronic memristor, also by selecting the optimal threshold for TiO<sub>2</sub> memristor and spintronic memristor, respectively.

### 7.2 Published and Submitted Papers

M. Abdallah, H. Mostafa, and M. Fathy, “Yield Maximization of Memristor-Based Memory Arrays”. *IEEE International Conference on Microelectronics (ICM 2014)*, Doha, Qatar, IEEE, PP. 5-8, 2014.

M. Abdallah, H. Mostafa, and M. Fathy, “Yield Optimization of Spintronic Memristor-Based Memory Arrays”. *In Press*.

M. Abdallah, H. Mostafa, and M. Fathy, "Yield Optimization of TiO<sub>2</sub> and Spintronic Memristor-Based Memory Arrays". *Journal, In Press*.

## 7.3 Future Work

This thesis provides a foundation for much future work in the areas of titanium dioxide and spintronic memristor modeling and design of memristor-based memory cells.

The extension of this work is to find a closed form solution for the writing yield and the reading yield in terms of the memristor device's dimensions, threshold, input flux, input current..etc. When these closed form solutions exist, an optimization problem can be solved to achieve the optimal parameters that optimize the writing and the reading yields.

Other models can be proposed to generate a large volume of process variation-aware three-dimensional device structures for Monte-Carlo simulations to impact of process variation on memristor. We may take a multi threshold point in to achieve better performance yield results.

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# Appendix A: TiO<sub>2</sub> Memristor Monte-Carlo Using Matlab

```
%%%%%%%%%%  
%TiO2 Yield without Variation Compensation  
%%%%%%%%%%  
%rh = roff ; rl = ron ; alpha = w/D (0-->1); phi = input flux;  
%h =D= thickness; uv = mobility;  
clear;  
  
w= 10e-9;    l=10e-9;    h= 20e-9;  
  
rl = ceil(0.1667e-3*h/(w*1)); rh = ceil(0.1667*h/(w*1));  
  
urh = 0.994; sigmarh=.0216*urh;  
url = 0.994; sigmarl=0.0216*url;  
  
%sigmay0=10e-9./sqrt(w.*1);    sigmay=sigmay0.*urh;  
  
sigmay = 0.9015; % determined by device simulator and changed with every different  
size  
  
alpha=1;  
  
epsilon1= -.028; epsilon2=0.072;omiga1=0.98;omiga2=0.2;  
  
uv = 1e-14;  
  
x = randn(1000);  
y= randn(1000);  
z=randn(1000);  
e= normpdf(x,0,1);  
d = normpdf(y,0,1);  
g = normpdf(z,0,1);  
  
rldash = rl .* (url+sigmarl.*e);  
rhdash = rh .* (rldash/rl) .*(urh+sigmarh.*e) .*(1+sigmay.*d);
```

```

beta1 =rh/rl;
phid =((beta1.*h).^2)/(2*uv*(beta1-1));
phi =phid*((rh.^2)-(rl.^2))/(rh.^2)
phieff = h.*h.*(rh+rl)/(2.*uv.*rl);

etadenominator = (1+ phi.*
epsilon1+phi.*epsilon2.*(omega1.*e+omega2.*g)).*(1+sigmay.*d);
etadenomatoreff = (1+ phieff.*
epsilon1+phieff.*epsilon2.*(omega1.*e+omega2.*g)).*(1+sigmay.*d);

eta = 1./etadenominator ;
etaeff = 1./etadenomatoreff ;

alphadash1 = eta.*alpha;
alphadasheff = etaeff.*alpha;

alphadash = alphadash1.*(alphadash1<1)+alphadasheff.*(alphadash1>=1);

mdash = rldash.*alphadash + rhdash.*(1-alphadash);

umdash = mean(mean(mdash));
sigmamdash= mean((var(mdash)).^0.5);

M = [rl:1:rh];

fM=normpdf(M,umdash,sigmamdash);
yield=normcdf(M,umdash,sigmamdash);

%figure; plot(M, fM);

threshold = ceil((rl+rh)/2)

RL=ceil(rl)
RH=ceil(rh)

Y=yield(find(M==threshold))

%plot(phi, fM);

%plot(M,yield);
plot(M,fM);
umdash;
sigmamdash;
(umdash+sigmamdash.*6)<threshold;

```

```
%%%%%%%%%%
```

```
%%%%%%%%%%
```

## % TiO<sub>2</sub> Memristor Writing Yield Optimization

```
%%%%%%%%%%
```

```
%rh = roff ; rl = ron ; alpha = w/D (0-->1); phi = input flux;
```

```
%h = thickness; uv = mobility;
```

```
clear;
```

```
w= 10e-9;    l= 10e-9;    h= 20e-9;  phi_low= 8;
```

```
rl = ceil(0.1667e-3*h/(w*l)); rh = ceil(0.1667*h/(w*l));
```

```
urh = 0.994; sigmarh=.0216*urh;
```

```
url = 0.994; sigmarl=0.0216*url;
```

```
sigmay= 0.9015;
```

```
% assuming Na*h = constant, therefore sigmay is only proportional to square root of WL
```

```
alpha=1;
```

```
epsilon1= -.028; epsilon2=0.072;omiga1=0.98;omiga2=0.2;
```

```
uv = 1e-14;
```

```
x = randn(1000);
```

```
y= randn(1000);
```

```
z=randn(1000);
```

```
e= normpdf(x,0,1);
```

```
d = normpdf(y,0,1);
```

```
g = normpdf(z,0,1);
```

```
rhdash = rh .* (urh+sigmarh.*e) .*(1+sigmay.*d);
```

```
rldash = rl .* (url+sigmarl.*e);
```

```
f= 20;
```

```
for R = 1:f
```

```
    %phi(R) = (R-f/2); % change phi from -f/2 to f/2 to find phi that maximize yield
```

```
    phi(R) = phi_low + R/10;
```

```
    phieff = h.*h.*(rh+rl)/(2.*uv.*rl);
```

```

etadenominator = (1+ phi(R).*
epsilon1+phi(R).*epsilon2.*(omega1.*e+omega2.*g)).*(1+sigmay.*d);
etadenominatoreff = (1+ phieff.*
epsilon1+phieff.*epsilon2.*(omega1.*e+omega2.*g)).*(1+sigmay.*d);

eta = 1./etadenominator ;
etaeff = 1./etadenominatoreff ;

alphadash1 = eta.*alpha;
alphadasheff = etaeff.*alpha;

alphadash = alphadash1.*(alphadash1<1)+alphadasheff.*(alphadash1>=1);

mdash = rldash.*alphadash + rhdash.*(1-alphadash);

umdash = mean(mean(mdash));
sigmamdash= mean((var(mdash)).^0.5);

M = [rl:1:rh];

fM=normpdf(M,umdash,sigmamdash);
yield=normcdf(M,umdash,sigmamdash);

%figure; plot(M, fM);

threshold = ceil((rl+rh)/2);

x=yield(find(M==threshold));

cond(R)=(umdash+sigmamdash*6)<threshold;

YIELD(R)= x.*100;

end

plot(phi, YIELD);

%plot(M,fM);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```



```

%%%%%%%%%%
% Reading Yield Optimization code
%%%%%%%%%%
%rh = roff ; rl = ron ; alpha = w/D (0-->1); phi = input flux;
%h = thickness; uv = mobility;
clear;

w=100e-9;    l=100e-9;    h= 20e-9;

rl = ceil(0.1667e-3*h/(w*1)); rh = ceil(0.1667*h/(w*1));

urh = 0.994; sigmarh=.0216*urh;
url = 0.994; sigmarl=0.0216*url;

%sigmay0=10e-9./sqrt(w.*1);    sigmay=sigmay0.*urh;

sigmay = 0.7212; % will be determined by device simulator

% assuming Na*h = constant, therefore sigmay is only proportional to square root of
WL

alpha=1;

epsilon1= -.028; epsilon2=0.072;omiga1=0.98;omiga2=0.2;

uv = 1e-14;

x = randn(1000);
y= randn(1000);
z=randn(1000);
e= normpdf(x,0,1);
d = normpdf(y,0,1);
g = normpdf(z,0,1);

rldash = rl .* (url+sigmarl.*e);
rhdash = rh .* (rldash/rl) .* (urh+sigmarh.*e) .* (1+sigmay.*d);

beta1 =rh/rl;
phid =((beta1.*h).^2)/(2*uv*(beta1-1));
phi =phid*((rh.^2)-(rl.^2))/(rh.^2)

phieff = h.*h.*(rh+rl)/(2.*uv.*rl);

```

```

etadenominator = (1+ phi.*
epsilon1+phi.*epsilon2.*(omega1.*e+omega2.*g)).*(1+sigmay.*d);
etadenominatoreff = (1+ phieff.*
epsilon1+phieff.*epsilon2.*(omega1.*e+omega2.*g)).*(1+sigmay.*d);

eta = 1./etadenominator ;
etaeff = 1./etadenominatoreff ;

alphadash1 = eta.*alpha;
alphadasheff = etaeff.*alpha;

alphadash = alphadash1.*(alphadash1<1)+alphadasheff.*(alphadash1>=1);

mdash = rldash.*alphadash + rhdash.*(1-alphadash);

umdash = mean(mean(mdash));
sigmamdash= mean((var(mdash)).^0.5);

for x = 1:100

    threshold(x)=x*3334;

M = [rl:1:rh];
fM=normpdf(M,umdash,sigmamdash);
yield=normcdf(M,umdash,sigmamdash);

%figure; plot(M, fM);

%%%%%%%%%%%%

%threshold = ceil((rl+rh)/2);

Y(x)=yield(find(M==threshold(x)))

%plot(phi, fM);
%plot(M,yield);
end
plot(threshold,Y);

%%%%%%%%%%%%
%%%%%%%%

```

# Appendix B: Spintronic Memristor Monte-Carlo Using Matlab

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% spintronic memristor Yield without variation compensation
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear;

w= 10e-9;    l=15e-9;    h= 900e-9;

%rl=50; rh=500;
%rl = ceil(3.5e-9*h/(w*1)); rh = ceil(3.5e-8*h/(w*1));
rl = 3.5e-7*h/(w*1); rh = 3.5e-6*h/(w*1);

urh = 0.994; sigmarh=.0216*urh;
url = 0.994; sigmarl=0.0216*url;
epsilon1= -.028; epsilon2=0.072;omiga1=0.98;omiga2=0.2;

sigmay = 0.742 % will be determined by device simulator
%%%%
beta=rh/rl;
j1=((beta*h).^2)./(beta-1);
j2=((rh^2)-(rl^2))./(rh^2);
jeff=4e11*j1*j2

alphawindow = 1;

x = randn(1000);
y= randn(1000);
z=randn(1000);
e= normpdf(x,0,1);
d = normpdf(y,0,1);
```

```

g = normpdf(z,0,1);

rldash = rl .* (url+sigmarl.*e);
rhdash = rh .* (rldash/rl) .*(urh+sigmarh.*e) .*(1+sigmay.*d);

etadenominatoreff = (1+ jeff.*
epsilon1+jeff.*epsilon2.*(omiga1.*e+omiga2.*g)).*(1+sigmay.*d);

etaeff = 1./etadenominatoreff ;

alphadash = etaeff.*alphawindow;

mdash = rldash.*alphadash + rhdash.*(1-alphadash);

umdash = mean(mean(mdash));
sigmamdash= mean((var(mdash)).^0.5);

r1l=ceil(rl); rh1=ceil(rh);
M = [r1l-50:1:rh1+50];

fM=normpdf(M,umdash,sigmamdash);

%plot(M,fM)

yield=normcdf(M,umdash,sigmamdash);

%figure;

threshold = ceil((r1+rh)/2)

Y=yield(find(M==threshold))

plot(M,yield);
%plot(M,fM);

%%%%%%%%%%%%%%
%%%%%%%%%%%%%%

```

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Spintronic Memristor Writing Yield Optimization
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```

```
clear;
```

```
w= 10e-9;    l=15e-9;    h= 900e-9;
```

```
%rl=50; rh=500;
%rl = ceil(3.5e-9*h/(w*1)); rh = ceil(3.5e-8*h/(w*1));
rl = 3.5e-7*h/(w*1); rh = 3.5e-6*h/(w*1);
```

```
urh = 0.994; sigmarh=.0216*urh;
url = 0.994; sigmarl=0.0216*url;
epsilon1= -.028; epsilon2=0.072;omiga1=0.98;omiga2=0.2;
```

```
sigmay = 0.742 % will be determined by device simulator
```

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%beta=rh/rl;
%j1=((beta*h).^2)./(beta-1);
%j2=((rh^2)-(rl^2))./(rh^2);
%jeff=4e11*j1*j2

```

```

j_low=0;
f=100;
for R=1:f
j(R)=j_low+R/10;

```

```
alphawindow = 1;
```

```

x = randn(1000);
y= randn(1000);
z=randn(1000);
e= normpdf(x,0,1);
d = normpdf(y,0,1);
g = normpdf(z,0,1);

```

```

rldash = rl .* (url+sigmarl.*e);
rhdash = rh .* (rldash/rl) .*(urh+sigmarh.*e) .*(1+sigmay.*d);

```

```

etadenominatoreff = (1 + j(R).*
epsilon1+j(R).*epsilon2.*(omega1.*e+omega2.*g)).*(1+sigmay.*d);

etaeff = 1./etadenominatoreff ;

alphadash = etaeff.*alphawindow;

mdash = rldash.*alphadash + rhdash.*(1-alphadash);

umdash = mean(mean(mdash));
sigmamdash= mean((var(mdash)).^0.5);

r11=ceil(rl); rh1=ceil(rh);
M = [r11-50:1:rh1+50];

fM=normpdf(M,umdash,sigmamdash);

%plot(M,fM)

yield=normcdf(M,umdash,sigmamdash);

%figure;

threshold = ceil((rl+rh)/2);

Y=yield(find(M==threshold));

cond(R)=(umdash+sigmamdash*6)<threshold;

YIELD(R)= Y.*100;

end

%plot(M,yield);

plot(j,YIELD)
%plot(M,fM);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% spintronic memristor Reading Yield Optimization
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```

```
clear;
```

```
w= 7e-9;    l=10e-9;    h= 1000e-9;
```

```
%rl=50; rh=500;
%rl = ceil(3.5e-9*h/(w*1)); rh = ceil(3.5e-8*h/(w*1));
rl = 3.5e-7*h/(w*1); rh = 3.5e-6*h/(w*1);
```

```
urh = 0.994; sigmarh=.0216*urh;
url = 0.994; sigmarl=0.0216*url;
epsilon1= -.028; epsilon2=0.072;omega1=0.98;omega2=0.2;
```

```
sigmay = 0.9236 % will be determined by device simulator
%%%
```

```
beta=rh/rl;
j1=((beta*h).^2)/(beta-1);
j2=((rh^2)-(rl^2))/(rh^2);
jeff=4e11*j1*j2
```

```
alphawindow = 1;
```

```
x = randn(1000);
y= randn(1000);
z=randn(1000);
e= normpdf(x,0,1);
d = normpdf(y,0,1);
g = normpdf(z,0,1);
```

```
rldash = rl .* (url+sigmarl.*e);
rhdash = rh .* (rldash/rl) .*(urh+sigmarh.*e) .*(1+sigmay.*d);
```

```
etadenominatoreff = (1+ jeff.*
epsilon1+jeff.*epsilon2.*(omega1.*e+omega2.*g)).*(1+sigmay.*d);
```

```

etaeff = 1./etadenominatoreff ;

alphadash = etaeff.*alphawindow;

mdash = rldash.*alphadash + rhdash.*(1-alphadash);

umdash = mean(mean(mdash));
sigmamdash= mean((var(mdash)).^0.5);

for x = 1:10

    threshold(x)=x*5000;
    rl1=ceil(rl); rh1=ceil(rh);
    M = [rl1-50:1:rh1+50];

    fM=normpdf(M,umdash,sigmamdash);

    yield=normcdf(M,umdash,sigmamdash);

    %figure;

    Y(x)=yield(find(M==threshold(x)))

end

plot(threshold,Y);
%plot(M,yield);
%plot(M,fM);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```





## الملخص

منذ أربعين عاما، توقع البروفيسور شوا وجود المقاومة ذات الذاكرة (ممرستور) و هي تعتبر العنصر الرابع المفقود للعناصر الاساسية للدائرة ، الثلاث عناصر الاساسية المقاومة ، المكثف، والملف. في عام 2008، وقد تحقق أول تحقيق مادي لل(ممرستور) من قبل معامل شركة HP. بجانب تكنولوجيا الحالة الصلبة، توفر التكنولوجيا المغناطيسية حلول أخرى ممكنة لبناء نظام يعتمد على الممرستور. الممرستور لديها القدرة على الإبقاء على قيمتها لفترة طويلة بعد انقطاع التيار الكهربى عنها. نظرا لقدرتها على تذكر القيم الماضية، لذلك هي يتم استخدامها في تصميم الذاكرة. يظهر ايضا للممرستور خصائص واعدة للجيل المقبل من اجهزة تخزين البيانات، مثل عدم التقلب، وانخفاض استهلاك الطاقة، والأداء الرفيع، وصغر الحجم وارتفاع الكثافة والقابلية ممتازة.

تواجه صناعة الممرستور مختلف التحديات بسبب صعوبة السيطرة على التغيرات التي تحدث اثناء عملية التصنيع ، نظرا لانها تصنع فى احجام تقاس بالنانو. عملية التغيير هي انحراف السلوك الكهربائي الفعلي للممرستور من القيم المطلوبة. نتائج هذا الانحراف هو خفض العائد خاصة في صفائف الذاكرة القائمة على ممرستور. يتم تعريف العائد على انة عدد خلايا الممرستور التي تؤدي دورها بشكل سليم (عملية الكتابة / القراءة سليمة). مصادر التغيرات تسمى , تكنولوجيا تقليل عدد العناصر المستخدمة فى التطعيم (الشوائب) مما يؤدي الى حركة عشوائية)سطح الجهاز يكون غير مستوي, واخيرا تغيرات فى سمك الاكسيد.

في هذا العمل، نحن نقوم بتحليل تأثير التغيرات العملية على الخصائص الكهربائية لكلا ( $TiO_2$ ) الأغشية الرقيقة الممرستور وايضا نوع اخر من الممرستور يدعى الإلكتروني الدوراني(Spintronic). اقترحنا نموذج بسيط لتوليد كمية كبيرة من الهياكل والتغيرات جهاز ثلاثي الأبعاد- باستخدام علم عملية محاكاة طريقة مونت كارلو (Monte-Carlo). ونحن نقدم اثنين من التقنيات لتحسين نسبة العائد من الممرستور(اكبر عدد من الممرستور تقوم بالكتابة والقراءة بشكل سليم).

التقنية الاولى هي كتابة العائد الأمثل من خلال تحديد التدفق الأمثل (للتيار الكهربى) من خلال تطبيق الجهد لممرستور لكلا النوعين  $TiO_2$  والنوع الإلكتروني الدوراني.

التقنية الثانية هي قراءة العائد الأمثل من خلال تحديد نقطة عندها يتحقق اعلى كفاءة لاداء جهاز الممرستور.

ضع صورتك هنا

مروة عبدالله مصطفى مسعود

1987\10\1

مصرية

2010\10\1

.....\.....\.....

الإلكترونيات والاتصالات الكهربائية

ماجستير

إ.د. محمد فتحى

د. حسن مصطفى

مهندسة:

تاريخ الميلاد:

الجنسية:

تاريخ التسجيل:

تاريخ المنح:

القسم:

الدرجة:

المشرفون:

المتحنون:

أ.د. .... (المتحن الخارجي)

أ.د. .... (المتحن الداخلي)

أ.د. .... (المشرف الرئيسي)

أ.د. .... (عضو)

عنوان الرسالة:

التصميم لقراءة وكتابة سليمة لمصفوفات الذاكرة المعتمدة على المقاومة ذات الذاكرة (ممرستور)

الكلمات الدالة:

الذاكرة النانو، ممرستور، مشاكل التصنيع فى تكنولوجيا النانو، دائرة، قراءة/كتابة

ملخص الرسالة:

المقاومة ذات الذاكرة (ممرستور)، والمعروفة بالعنصر الرابع المفقود والمكمل للثلاث عناصر الأساسية (المقاومة، المكثف، الملف) تعتبر من المرشحين المحتملين للجيل القادم من الذاكرة والتي لفتت انتباه كبير من المجتمع البحثى منذ ان قامت شركة اتش بي بتصنيع اول واحدة عام 2008. تصنيع الممرستور بىواجة تحديات صعبة فى التغلب و السيطرة على مشاكل التصنيع حيث انه حجمة يقاس بالنانو. نتائج مشاكل التصنيع هى اختلاف القيم المتمثلة فى حجم الجهاز عن قيمها الحقيقية اثناء التصميم. وهذه المشاكل تودى الى تقليل كفاءة الممرستور وبلتالى اعداد كبيرة من الممرستور تقوم بكتابة وقراءة خاطئة. فى هذه الرسالة نقوم بمحاولة زيادة اعداد الممرستور التى تستطيع ان تودى قراءة وكتابة سليمة باستخدام طريقة منتو-كارلو للتحليل العدى. ونقدم تقنيتين احدهما لتحقيق اكبر عدد من الممرستور تقوم بكتابة بشكل سليم والاخرى لتحقيق اكبر عدد من الممرستور تقوم بالقراءة بشكل سليم.

التصميم لقراءة وكتابة سليمة لمصفوفات الذاكرة المعتمدة على المقاومة ذات  
الذاكرة (ممرستور)

اعداد

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رسالة مقدمة إلى كلية الهندسة - جامعة القاهرة  
كجزء من متطلبات الحصول على درجة الماجستير  
في  
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الجيزة - جمهورية مصر العربية

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تحت اشراف

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