DESIGN OF HIGH-PERFORMANCE VARIATION-TOLERANT DIFFERENTIAL VOLTAGE-TO-TIME CONVERTER (VTC) CIRCUITS

By

Abdullah Mohamed Ahmed El-Bayoumi

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2016

DESIGN OF HIGH-PERFORMANCE VARIATION-TOLERANT DIFFERENTIAL VOLTAGE-TO-TIME CONVERTER (VTC) CIRCUITS

By

Abdullah Mohamed Ahmed El-Bayoumi

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

Under the Supervision of

Prof. Dr. Ahmed M. Soliman

Emeritus Professor

Electronics and Communications
Engineering Department
Faculty of Engineering, Cairo University

Dr. Hassan Mostafa

Assistant Professor

Electronics and Communications
Engineering Department
Faculty of Engineering, Cairo University

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2016

DESIGN OF HIGH-PERFORMANCE VARIATION-TOLERANT DIFFERENTIAL VOLTAGE-TO-TIME CONVERTER (VTC) CIRCUITS

By

Abdullah Mohamed Ahmed El-Bayoumi

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

Approved by the
Examining Committee

_____
Prof. Dr. Ahmed M. Soliman, Thesis Main Advisor

_____
Prof. Mohamed Riad, Internal Examiner

_____
Prof. Hassanein H. Amer, External Examiner
(Electronics and Communications Engineering, The American University in Cairo)

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2016

Engineer's Name: Abdullah Mohamed Ahmed El-Bayoumi
Date of Birth: 05/11/1990
Nationality: Egyptian
E-mail: abdullah.elbayoumi@pg.cu.edu.eg
Phone: +20 100 380 7047
Address: Electronics and Communications Engineering Department, Cairo University, Giza 12613, Egypt

Registration Date: 01/10/2012
Awarding Date: --/--/2016
Degree: Master of Science
Department: Electronics and Communications Engineering

Supervisors:

Prof. Dr. Ahmed M. Soliman
Dr. Hassan Mostafa

Examiners:

Prof. Dr. Ahmed M. Soliman (Thesis main advisor)
Prof. Mohamed Riad (Internal examiner)
Prof. Hassanein H. Amer (External examiner)
(Electronics and Communications Engineering, The American University in Cairo)

Title of Thesis:

Design of Time-based Analog-to-Digital Converter (T-ADC): High-Performance Variation-Tolerant Differential Voltage-to-Time Converter (VTC) Circuits

Key Words:
Nanometer CMOS technology; voltage-to-time converter; time-based analog-to-digital converter; software-defined radio; biomedical applications; metal-insulator-metal capacitor; dynamic range.

Summary:

In this thesis, various metal-insulator-metal (MIM) capacitor-based differential Voltage-to-Time Converters (VTCs) including 2 novel proposed designs, which achieve a high performance at higher sampling frequency for a Software-Defined Radio (SDR) receiver at 65-nm CMOS technology, are presented and compared to their single-ended design. A study on tolerating the process-voltage-temperature (PVT) variations for the 1st proposed design with proposing a dynamic calibration technique based on a set of large-sized capacitor-based voltage dividers circuits is presented. Post-layout simulation results are provided for both designs at 130-nm CMOS technology for low-frequency low-power implantable biomedical systems.

Acknowledgments

To begin with, I would like to take this opportunity by expressing my deepest gratitude and appreciation towards my supervisors Prof. Dr. Ahmed M. Soliman and Dr. Hassan Mostafa. Their continuous support, guidance and enthusiasm have made my research instrumental, intellectually stimulating, enjoyable and very rewarding in successfully performing and completing my thesis. It is a great honor to be accepted as a masters' degree student under the supervision of Prof. Dr. Soliman. It is really remarkable to attend the IEEE International Conference on Electronics, Circuits and Systems (ICECS 2015) as an author and watch the honorary ceremony of Prof. Dr. Soliman for his amazing research contribution record in the cutting-edge technologies for academia and industry. His inspiration stories and his excellence dedication have guided me to finalize this work.

Also, I would like to specialize my thanks to Dr. Mostafa who has shaped my research direction with his ideas. His vision, mentorship, professional advices of technical and non-technical issues and friendship have advanced me through the thesis, although his lots of postgraduate and undergraduate students. These also encourage me to take the lead and participate in various international conferences. That helps me to get accepted of some of them. As we know the main aspect of any journey is to understand your failures, I have learnt from Dr. Mostafa to study well the review comments of my rejected papers and analyze them to start again. I really appreciate Dr. Mostafa's patience towards me regarding the work load of my industrial career. I am also thankful to Dr. Mohamed Refky for using his experience and knowledge to help me whenever I needed it. I would like to thank my fellow graduate students in the EECE department who have provided me with the tools and support needed to complete this dissertation.

Research is something when you change your way of thinking. This process of change may be slow. Thus, it could leave you completely unaware of the change you have made, and the progress that you are currently making. An instance of recollection, such as writing a summary of the progress you have been doing for the last years brings these things to your attention. This process of change is something that your environment is aware of, as one is thrown between despair and hope. Being a software engineer in a multinational company is stressful and at times it is emotionally challenging to struggle to manage your time between your industrial work background and your academic research. Although, they could fulfill a perfection background of how we innovate ideas till we can provide products to the market. Finally, I am also grateful to all my friends who have encouraged me to keep going on and brought social balance into my life.

Dedication

I have devoted this dissertation with a special thank you to my family for helping me to come this far and for being a continuous source of love, care, warmth and stability throughout my life. Collectively, they are an enormous pool of support for which I would not have succeeded without. I owe them every single achievement in my life.

Table of Contents

List of Tables

List of Figures

Nomenclature

DR	Dynamic Range
F_S	Sampling Frequency
$F_{S,MAX}$	Maximum Sampling Frequency
ΔT_0	Time Difference variable of the 2nd proposed VTC circuit
ΔT_1	Time Difference variable of the 2nd core of the 2nd proposed VTC
ΔT_2	Time Difference variable of the 1st core of the 2nd proposed VTC
Φ_{CLK}	Reference Clock
Φ_{O0}	Output of the single-core of the 2nd proposed VTC circuit
I_{IN}	Input Current
I_{REF}	Reference Constant Current
V_{IN}	Applied Input Voltage
V_{REF}	Reference Voltage
V_{TH}	Threshold Voltage
V_A	Capacitor Voltage
V_{DS}	Drain-Source Voltage
$V_{N,RMS}$	Overall Output Referred Noise RMS Value Per Frequency
$V_{N,TH}$	Thermal Noise Voltage RMS Value
$V_{I,RMS}$	Input Signal Harmonics RMS Value
$V_{D,RMS}$	Overall Circuit Distortion RMS Value
$V_{F,RMS}$	Harmonically-Related Distortion Component RMS Value
V_{FS}	Full Scale Voltage
N	Number-of-Bits
F_{IN}	Fundamental Input Frequency
$F_{I,MAX}$	Maximum Allowed Input Frequency
ΔF	Signal Bandwidth
R	Internal MOSFET Resistance
C_L	Load Capacitor
F_B	Nyquist Frequency
P_D	Power Dissipation
Δ	Buffer Delay
$\Sigma\Delta$	Sigma-Delta
T_R	Rise Delay of the rising VTC circuit
T_F	Fall Delay of the falling VTC circuit
TT	Typical Speed nMOS – Typical Speed pMOS
SS	Slow Speed nMOS – Slow Speed pMOS
FF	Fast Speed nMOS – Fast Speed pMOS
SF	Slow Speed nMOS – Fast Speed pMOS
FS	Fast Speed nMOS – Slow Speed pMOS
S-H	Sample-and-Hold
DIBL	Drain-Induced Barrier Lowering
OSR	Oversampling Ratio
LNA	Low-Noise Amplifier
VCO	Voltage-Controlled Oscillator
VTC	Voltage-to-Time Converter
TDC	Time-to-Digital Converter
ADC	Analog-to-Digital Converter

T-ADC	Time-based Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
SQNR	Signal-to-Quantization-and-Noise Ratio
LSB	Least Significant Byte
MSB	Most Significant Byte
INL	Integral Non-Linearity
DNL	Differential Non-Linearity
FFT	Fast Fourier Transform
ENOB	Effective Number of Bits
THD	Total Harmonic Distortion
UWB	Ultra-Wide Band
SDR	Software-Defined radio
PWM	Pulse Width Modulator
PPM	Pulse Position Modulator
IC	Integrated Circuit
DSP	Digital Signal Processing
MIMCAP	Metal-Insulator-Metal Capacitor
PVT	Process-Voltage-Temperature
FOM_1	1^{st} Approach of Walden Figure-of-Merit
FOM_2	2^{nd} Approach of Walden Figure-of-Merit
TSMC	Taiwan Semiconductor Manufacturing Corporation
CMOS	Complementary Metal-Oxide Semiconductor
RMS	Root-Mean-Square
DFT	Discrete Fourier Transform
PEX	Parasitic Extraction
DRC	Design Rule Check
LVS	Layout Versus Schematic
SAR	Successive-Approximation Register
ADE	Analog Design Environment

List of Publications

Published:

[1] A. El-Bayoumi, H. Mostafa, and A.M. Soliman, "A New 65nm-CMOS 1V 8GS/s 9-bit Differential Voltage-Controlled Delay Unit Utilized for a Time-Based Analog-to-Digital Converter Circuit," The 27th IEEE International Conference on Microelectronics (ICM 2015), Casablanca, Morocco, pp. 158-161, 2015.

[2] A. El-Bayoumi, H. Mostafa, and A.M. Soliman, "A New 16-Bit Low-Power PVT-Calibrated Time-Based Differential Analog-to-Digital Converter (ADC) Circuit in CMOS 65nm Technology," The 22nd IEEE International Conference on Electronics, Circuits and Systems (ICECS 2015), Cairo, Egypt, pp. 492-493, 2015.

[3] A. El-Bayoumi, H. Mostafa, and A.M. Soliman, "A New Highly-Linear Highly-Sensitive Differential Voltage-to-Time Converter Circuit in CMOS 65nm Technology," The 19th IEEE International Symposium on Circuits and Systems (ISCAS'2015), Lisbon, Portugal, pp. 1262-1265, 2015.

Submitted:

[4] A. El-Bayoumi, H. Mostafa, and A.M. Soliman, "A Novel MIM-Capacitor Based 1-GS/s 14-bit Variation-Tolerant Fully-Differential Voltage-to-Time Converter (VTC) Circuit," Journal of Circuits, Systems, and Computers, accepted, pp. 1-32, 2016.

Abstract

At scaled CMOS technologies, the time resolution of digital circuits is much better than the voltage resolution of analog circuits. Therefore, increasing the digital design percentage becomes more crucial especially at high frequencies. As a result, utilizing the Time-based Analog-to-Digital Converter (TADC) becomes one of the essential blocks in designing high-speed applications such as: Software-Defined Radio (SDR) and Ultra-Wide Band (UWB) receivers; and in designing high-accurate systems such as: biomedical, automotive and military application. It manifests lower power and area than conventional ADCs. TADC includes 2 main blocks: a Voltage-to-Time Converter (VTC) which converts the input voltage into a pulse delay, and a Time-to-Digital Converter (TDC) which converts the pulse delay into a digital word.

In this thesis, various fully-differential VTCs including 2 novel proposed designs for SDR receiver, at 65-nm CMOS technology are presented and compared to their single-ended design. The proposed designs are based on Metal-Insulator-Metal (MIM) capacitor to minimize the process-voltage-temperature (PVT) variations. The first proposed design is based on an enhanced methodology which achieves 12.8 bits effective-number-of-bits (ENOB), a 229 μm^2 area and a 0.25 mW power. It operates at a 1 GS/s sampling frequency (F_S) with a 1.2 V supply voltage. A study of the PVT variations which are tolerated by a calibration circuit is proposed. The second proposed design operates on a high sampling frequency of 8 GS/s with a 1 V supply voltage. It achieves 8.9 bits ENOB, a 742 μm^2 area and a 1.6 mW power. These calculations are based on pre-layout simulation results on Cadence Spectre and MATLAB.

Post-layout simulation results are also provided for both designs at 130-nm CMOS technology in biomedical applications such as implantable neural systems. The main target of these systems is to exhibit low power dissipation, operate on low sampling frequency and have a high resolution. The layout design using Calibre is maintained to achieve the minimum-distance approach in order to have a low-area design. The operating sampling frequency at this case is 10 MS/s. The dynamic calibration technique, which is based on a set of large-sized capacitor-based voltage dividers circuits, utilized as DC offset voltages to compensate the effect of the PVT variations on the circuit characteristics, is validated after the post-layout design of the 1st proposed design.

Chapter 1 : Introduction

We live in a continuous analog prospective world. Our main aim is to fully understand the analog signals processing around us. Nowadays, the electronics industry evolution seeks to monitor, sense and control every single details around us. Starting from the mid of the 20th century till these moments, the exceptional advance of the digital signal processing domain directed the academia and the industry communities to shorten the gap between the continuous analog signals information and the discrete digital signals information. With utilizing cutting-edge technologies, we are about to make the digital signal become closer to reach the analog signals' information with a few number of noise, quantization and distortion errors. Consequently, designing various types of Analog-to-Digital Converters (ADCs) is one of the major objectives to satisfy the consumer market needs.

Due to the electronics revolution, a periodic demand, to provide more detailed digital representations of the analog signals, has been for designing and implementing faster ADCs. In 1987, the first ADC was designed with a sampling speed of 1 GS/s [1]. Then, this design has been followed by high-speed ADCs to be used in oscilloscopes. The technology used was bipolar transistor and it typically has consumed a power of more than 3 watts [2]. In large-scale operations, this power is much high regarding the Integrated Circuit (IC) heat management and the battery life. By the time of the end of 20th century, new applications was emerged which required low-power and faster ADCs. This made us to think about new alternatives to evolve gradually the bipolar transistor technology.

At the beginning of the 21st century, the Complementary Metal-Oxide Semiconductor (CMOS) high-speed ADCs revealed to the industry [3]. This was an indifferent shift in the industrial technology due to the much low power introduced by the MOSFETs than the bipolar transistors and its integration ease with the digital circuitry. The ADC based on CMOS technology has faced some challenges at the beginning (latch-up) [4], in which its appearance was delayed for a decade with the dependency of the bipolar technology based ADC. Then, the CMOS technology has dominated the ADC market once it was able to reach the aimed sampling rate. The industrial race has advanced to produce a wide variety of either low-power low-area high-speed ADCs architecture on the count of ADC accuracy and vice versa. Thus, a new classification should be introduced to shorten this gap in order to present high-performance ADCs with the lowest area and power.

The major parameters in the ADC specifications [5] are resolution, sampling frequency, area and power. As each system has its own requirements with different critical parameters, various types of ADCs exist to satisfy these requirements. These systems; that need ADCs which have specific constraints on the major ADC parameters;

could be used in such applications as: Automotive, Software-defined Radio (SDR), biomedical systems, wireless communications, internet of things and sensors. For example, sensors sense, amplify and measure various physical quantities like speed, pressure, viscosity and flexibility. These quantities are analog signals and they need to be processed by Digital Signal Processing (DSP) circuits. Hence, sensors should impose restrictions on the dissipate power. This emphasizes the need of new low-power ADC category.

The ADC is classified based on either the conversion type or the sampling rate [6]. At first, the conversion type classification consists of 2 kinds of conversions. The first conversion type is the traditional one which is called direct conversion. Whereas the analog applied voltage is converted to the digital code directly by an ADC. The second conversion type is the indirect conversion. Whereas the analog applied voltage is converted to an intermediate domain such as frequency or time, then this domain is converted to the digital code by VCO-based ADC or Time-based ADC (TADC), respectively. At second, the sampling rate classification consists of 2 main categories. The first category is oversampling ADCs such as: Sigma-Delta modulator; while the second category is Nyquist-rate ADCs such as: Flash ADC, pipelined ADC and Successive-Approximation Register ADC.

1.1. Motivation

Nowadays, the flow of scaling CMOS technology invades all industrial and scientific communities. This drift overcomes the main problems that face conventional Analog-to-Digital Converters (ADCs) [5]–[9] to satisfy the Software-Defined Radio (SDR) applications requirements. In fact, due to the capacity of demands, a single chip is intended to have several chains of transmitting and receiving blocks needed for different wireless standards that require from the ADC: a high sampling frequency and a wide dynamic range. This results in large power consumption that is not affordable by a wireless device.

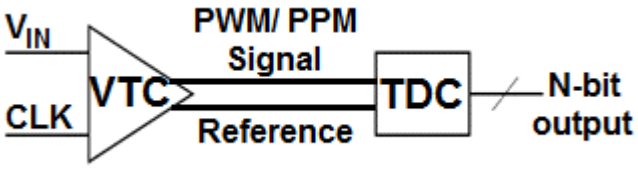


Figure 1.1: TADC architecture

This induces applications such as SDR receivers to appear [10], and [11]. The SDR IC configures and controls the chain which is currently used, otherwise all chains are switched on. In SDR receiver, the received analog signal is applied to a wide-band ADC, followed by a real-time Digital Signal Processor (DSP). New ADCs are reconfigured

according to the SDR standard. This leads to think about new techniques of ADCs design that exhibit small area and low power dissipation.

In deep sub-micron CMOS technology, technology scaling makes the ADC design more complex, as it reduces the supply voltage which degrades the signal swing (headroom level) and the signal-to-noise ratio (SNR). Besides, it has a few effects on the threshold voltage resulting in a complexity in the analog design prospective [6].

In high frequencies, the time resolution of digital signals is often greater than the voltage resolution of the analog signals. Consequently, the percentage of the digital part of the ADC system is increased using digital CMOS technology in order to: solve analog design problems, get the full use of the digital signal processing, reduce power and area consumption, have faster ADCs with higher performance and make the ADC move closer to the receiver signal input [5].

In TADC, the analog signal amplitude is sampled and converted into a pulse in time-domain by modulating edges of the reference signal, then the time-domain pulse is quantized into a digital output. The operation is performed using a Voltage-to-Time Converter (VTC) and a Time-to-Digital Converter (TDC) as shown in Figure 1.1. The VTC is referred to as either a Pulse Width Modulator (PWM) or Pulse Position Modulator (PPM), depending on whether the delay is applied to one or both input clock pulses edges [12]. The TDC circuit includes digital logic and counter circuits [9], [13].

Several VTC circuits have been introduced in the literature [6], [8]–[9], [12] and [14]–[15]. The basic core in the literature circuits is the current inverter, in which the applied input voltage (V_{IN}) controls the fall time and makes the pulse width of the output inversely proportional to it. All previously published circuits are facing various limitations and design trade-offs between dynamic range, linearity and the ADC resolution. Also, they suffer from a limited sensitivity.

Currently, the neuroscience research and electronic industry incredible growth has led to implementing remarkable applications in biomedical systems. One of these applications is the microsystems which can stimulate, record and enhance the activities of the neural brain. Consequently, it is applicable to eliminate and treat various neurological disorders such as: Parkinson diseases and Epilepsy. The implantable neural system is connected to the brain by some electrodes under the skull. It is fed by supply either wirelessly or by energy harvesting ways. One of the main metrics of designing an implantable neural systems is to produce a low power consumption in order to extend the battery life of these systems. As a result, the number of surgical operations (i.e. therapy operation) that aimed to replace only the battery could be minimized [16].

There are superior advantages in the differential design than that in the single-ended design. First, the common-mode noise is rejected. Second, the differential input offers doubling of the signal amplitude resulting in a 6-dB improvement in the SNR. Finally, the components of the even-order harmonic distortion caused by a single-ended VTC circuit non-linearity are suppressed.

Finally, by gathering all the advantages of the usage of scaled technology nodes, promising results in linearity, dynamic range (DR) and resolution are achieved at a reasonable expense of extra power/ area overheads.

1.2. Thesis scope

By using the CMOS technology node, this thesis focuses on proposing 2 novel VTC designs:

1. The 1st proposed design is designing a fully-differential VTC architecture based on a modified VTC methodology to produce a higher dynamic range. This design is optimized with several techniques including proposing a calibration circuit to tolerate the process-voltage-temperature (PVT) variations. Moreover, a study on the PVT simulation results is introduced before and after adding the calibration circuit.

2. The 2nd proposed design is a differential high-speed VTC which could be sampled at a frequency of 8 GS/s. This design is also optimized to minimize the PVT variations.

Simulation results of both designs have been illustrated for both 65-nm CMOS and 130-nm CMOS technologies. The aim of proposing both designs in 65-nm CMOS is to show the maximum frequency that could be used in high-frequency applications such as SDR transceiver. On the other hand, the aim of proposing both designs in 130-nm CMOS is to show the minimum frequency that could be produced in low-frequency applications such as biomedical applications. The effective-number-of-bits (ENOB) is discussed to show the strength of each proposed design. Moreover, layout and post-layout simulations results have been introduced at the 130-nm CMOS technology.

1.3. Thesis overview

The rest of the thesis is organized as follows. In Chapter 2, the ADC functionality is introduced with defining the ADC sampling and quantization error. Moreover, a literature review of the state-of-the-art ADCs is presented from the prospective of both the conversion and the sampling types.

In Chapter 3, several differential VTC circuits using TSMC 65 nm CMOS technology for SDR applications have been discussed and analyzed. Furthermore, these designs include 2 novel proposed design where they could operate on 2.5 GS/s an 8 GS/s, respectively, with higher ENOB and dynamic range. Furthermore, a study of the PVT variations with proposing a calibration circuit to tolerate them has been introduced for the 1st proposed design.

Chapter 4 discusses the behavior of both produced designs in UMC 130 nm CMOS technology at lower sampling frequency in order to be used in biomedical applications. In additions, post-layout simulation results are introduced for both propose designs

including a check of the calibrated corner variation for the 1st proposed design with the calibration circuit. Chapter 5 reveals the thesis conclusion and shows the future work.

Finally, Appendix A shows the transistors dimensions of all designs proposed by this thesis. While, Appendix B shows all steps needed using Virtuoso Analog Design Environment and MATLAB to simulate and validate the linearity check, circuit sensitivity, total harmonic distortion, power consumption, noise figure, effective number of bits and the PVT variations.

Chapter 2 : Literature Review

2.1. Analog-to-Digital Converter

Analog-to-Digital Converter (ADC) converts the continuous amplitude and time signal to a discrete time and amplitude digital code word. Each digital code word represents a combination of a specific sampled instance with its corresponding quantized amplitude known as a quantization error. The quantization error is reduced by increasing the ADC number of bits and the ADC resolution as well as decreasing the ADC circuit thermal noise and the ADC non-linearity and distortion. Figure 2.1 illustrates a 3-bit ADC sampling instance. A Digital-to-Analog Converter (DAC) carries out the opposite operation of the ADC, where it converts the applied digital code words into the corresponding analog level voltages [6].

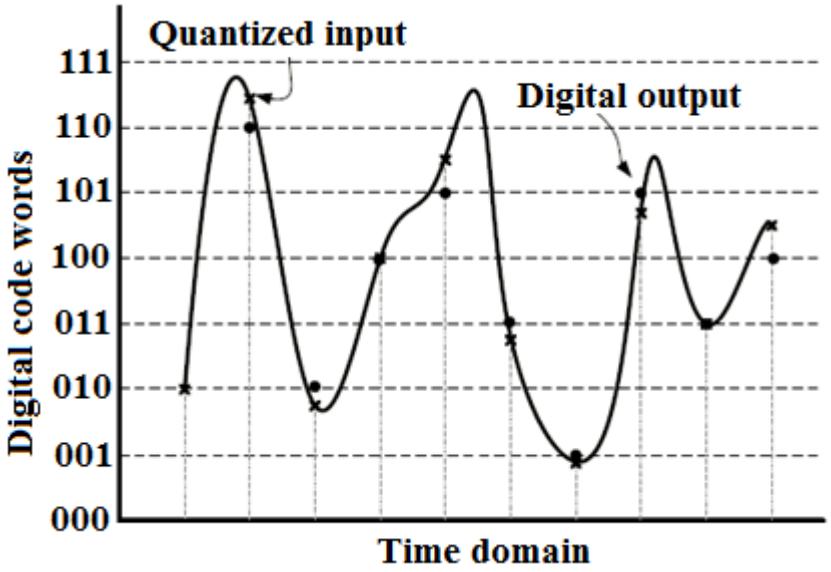


Figure 2.1: A functionality of a 3-bit ADC

2.1.1. Sampling

ADC samples the analog input signal with a sampling frequency (F_S) which should achieve the Nyquist-rate with a frequency larger than the double of the maximum frequency of an input signal spectrum. Figure 2.2 shows the spectrum of an input signal achieving the Nyquist-rate criterion, while Figure 2.3 shows the spectrum of an input signal which does not achieve the Nyquist-rate criterion.

To be able to reconstruct an original analog input signal, a reconstruction low-pass filter is requested. So, it is easier to get back the original signal as long as it satisfies the Nyquist criterion. Hence, this filter design can be simply implemented in time and frequency domains. On the other hand, if the input signal spectrum does not achieve the Nyquist-rate criterion, the signal is not reconstructed correctly due to an aliasing occurring as in Figure 2.3. The aliasing represents frequency interference, where the

original signal needs another filter design than the low pass filter in order to be extracted [17].

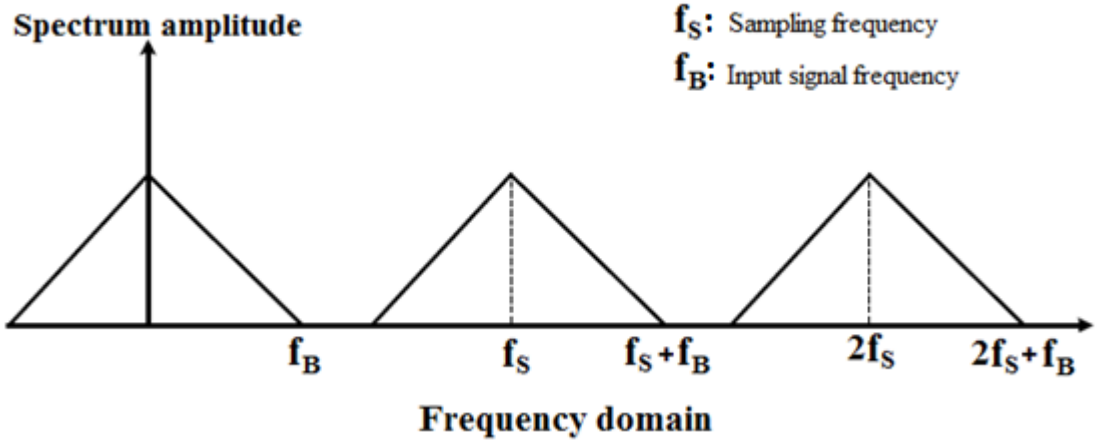


Figure 2.2: An input signal spectrum achieving the Nyquist-rate criterion

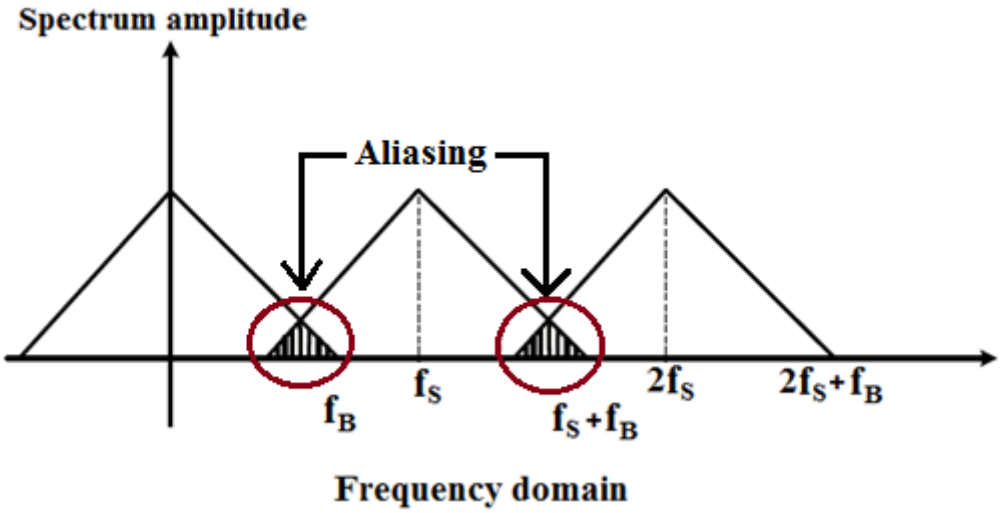


Figure 2.3: An input signal spectrum not achieving the Nyquist-rate criterion

2.1.2. **Quantization**

Quantization process happens after sampling a continuous analog input range so as to translate the sampled signal into a stream of digital output code words as revealed in Figure 2.4. This process leads to a logical undesired main property which is the

quantization error [17]. The quantization error is defined as the difference between the quantized version of an original signal and this original signal itself. It always ranges from –0.5×LSB: +0.5×LSB as shown in Figure 2.5, where LSB is the Least Significant Bit. Using a high resolution ADC with a higher number of bits (N) could reduce this error as in equation (2.1). Where, V_{FS} is the ADC full scale voltage.

$$LSB = \left(\frac{V_{FS}}{2^N}\right) \tag{2.1}$$

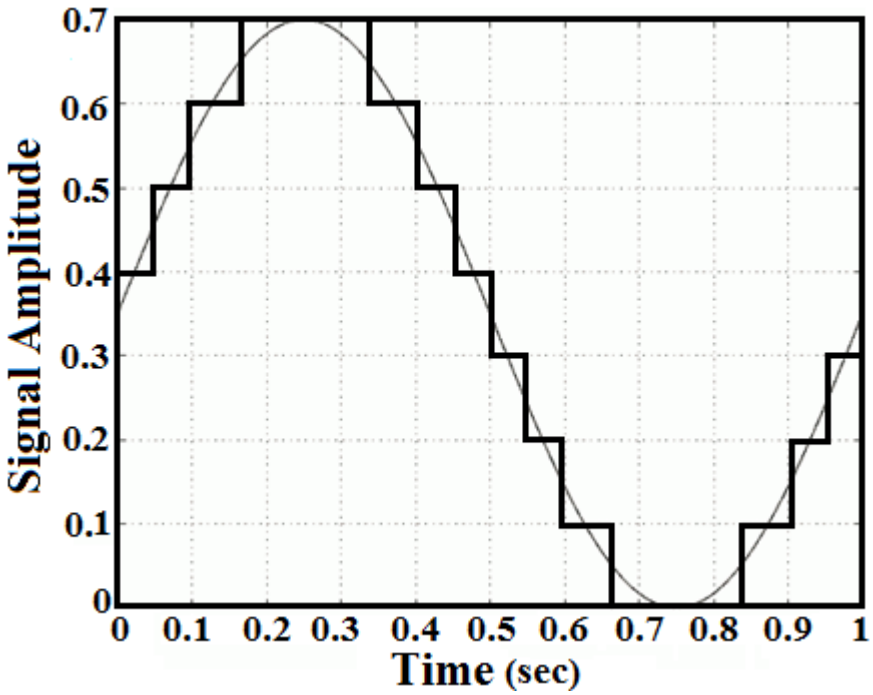


Figure 2.4: Original signal versus quantized signal

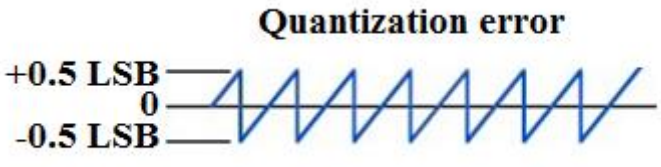


Figure 2.5: Quantization error representation

2.2. ADC types

A various number of ADC architectures have been presented to achieve either higher sampling rates than 1GS/s or higher accuracy level than 8 bits or even both of them. These ADCs can be categorized as direct conversion ADCs or indirect conversion ones. Both could be implemented based on Nyquist formula where the ADCs input bandwidth

should be close to the Nyquist-rate which is a half of the sampling rate or based on the principle of oversampling where ADCs input signals with fundamental frequencies should be far below the sampling rate [4].

2.2.1. Direct conversion ADCs

2.2.1.1. Nyquist-rate ADC

2.2.1.1.1. Successive-Approximation ADC

Successive-Approximation Register (SAR) ADCs have been one of the best energy efficient and accurate ADC architecture on the account of the sampling rate. Recent reduced-power SAR ADCs use switched-capacitor-based charge redistribution DACs [4]. The basic idea of the SAR ADC is based on the iterative method. Whereas the input signal (V_{IN}) is modulated and provided to a comparator in the duration of the conversion process as shown in Figure 2.6. Then, the comparator output decides if the Digital-to-Analog Converter (DAC) output is lower or higher than the sampled V_{IN} in order to complete the first conversion step. As a result, the control digital logic uses the comparison result to set the register's value to a midpoint representing a half of the full-scale value. The register's value is converted to an analog signal by the DAC.

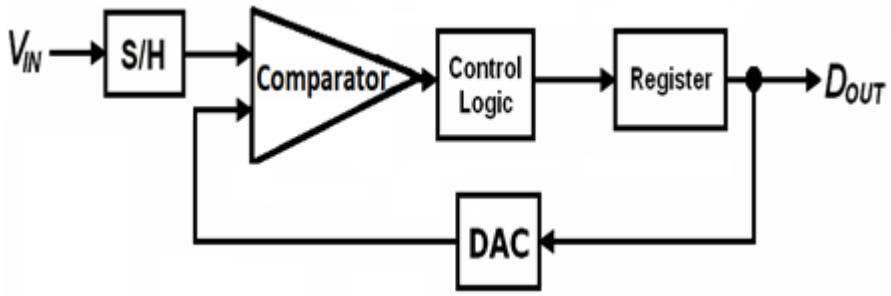


Figure 2.6: SAR architecture

So, if the first conversion step result indicated by the comparator reveals that V_{IN} is greater than the DAC output, the signal must lie after a 50% of the full scale value. In the second conversion step, the control digital logic sets the register to 75% of the full scale value (two '1's followed by '0's which represent the remaining bits). In this way the ADC produces a closer approximation to the sampled V_{IN}. After number of bits (N), the conversion is completed and the value stored in the digital register is the ADC output for the current sample. This process then repeats over and over for each new sample as shown in Figure 2.7.

As each conversion process requires several steps, and a new conversion must not be started until the current one is completed, SAR ADCs literally operate at low clock frequencies. Such modifications done to the basic SAR ADC designs have allowed them to operate at higher sampling rates as 1.25GS/s [18]. These innovations include the use of comparators in parallel and asynchronous rather than clocked operation.

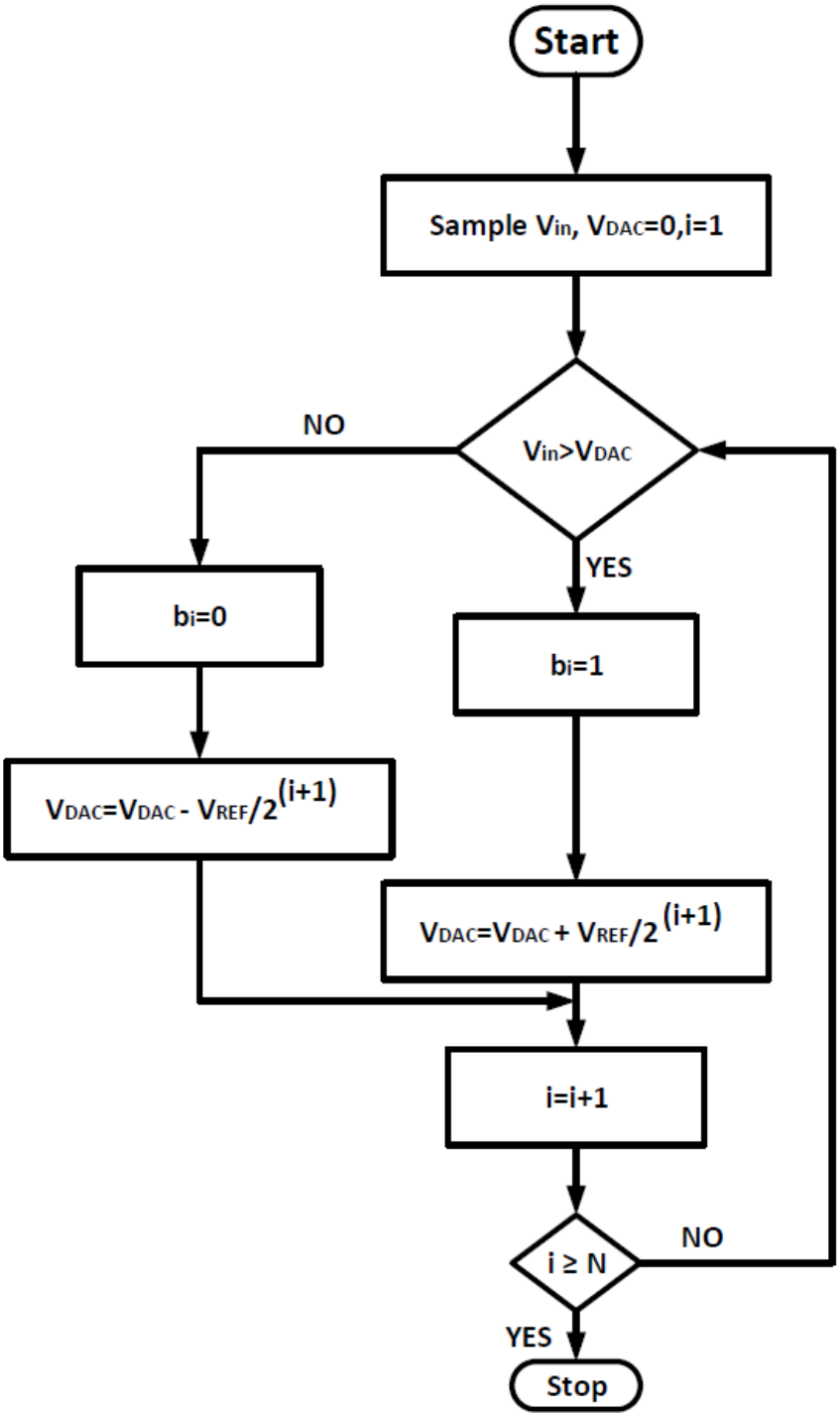


Figure 2.7: SAR algorithm

2.2.1.1.2. Flash ADC

Flash ADC can work at Giga-sample rate as it uses parallel processing in order to push the speed limits for a specific fabrication technology. Figure 2.8 shows a 3-bit flash ADC architecture, in which a resistive reference ladder provides 8 equally spaced reference voltages over the input span of the ADC. Each reference voltage is provided to its own comparator, along with V_{IN}. The comparators decide to output a '0' or '1' signal

depending on whether V_{IN} is lower or higher than the reference voltage. The result is a 7-bit thermometer code where the bottom the code includes '1's up to the V_{IN}, followed by '0's up to the top. A digital decoder block converts the 7-bit thermometer code into a 3-bit digital code [5].

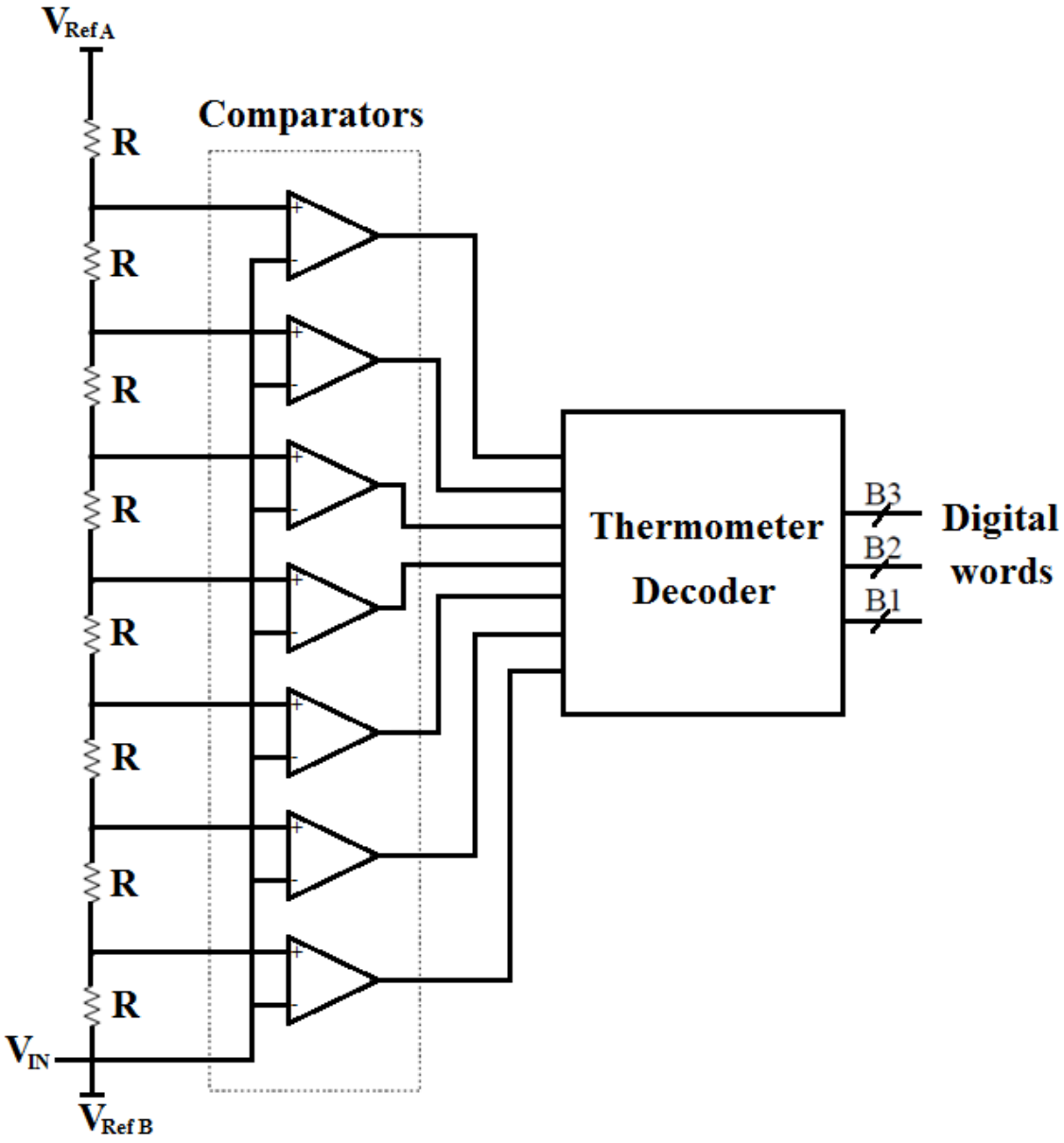


Figure 2.8: Flash ADC architecture

The main disadvantage of the flash ADC is that it becomes larger twice in area and power for every additional conversion bit [12]. In additions, the resistive ladder consumes a static power. Various modifications have been introduced to reduce the extra heads of area and power using dynamic comparators connected with banks of capacitors as built-in offsets. On the other hand, these offsets should be calibrated from process-voltage-temperature (PVT) variations. Also, folding architecture [12] could be used for flash ADCs to reduce the area and power requirements. Figure 2.9 shows a folded flash ADC with a folding factor of 2. Hence, there is an additional comparator added to the standard area and power of the flash ADC for an additional conversion bit plus some analog

circuitry to perform the voltage addition. If V_{IN} is greater than zero, the input is passed to the flash ADC as it is. In contrast, if V_{IN} is less than zero, an additional value (Vamp) is added t o V_{IN}. The final digital output includes the most significant bit (MSB) of the folding stage and the remaining bits of the flash ADC.

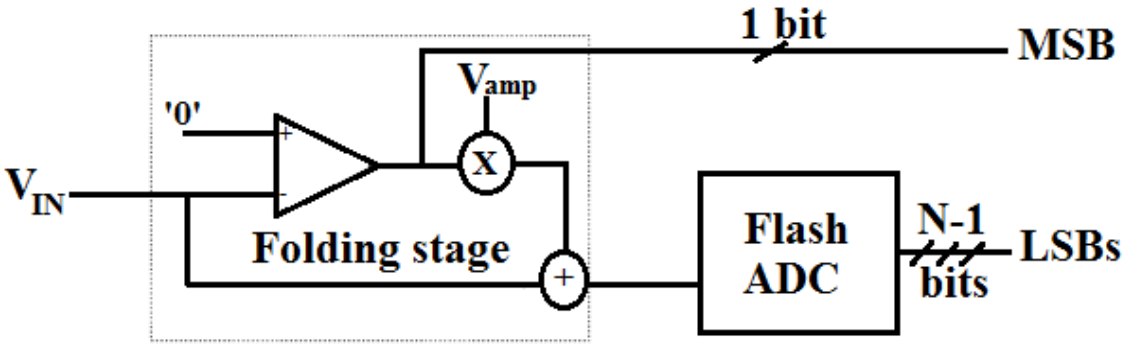


Figure 2.9: Folded flash ADC architecture

2.2.1.1.3. Pipelined ADC

The pipeline ADC is based on the folding idea where it consists of several cascaded stages followed by a flash ADC as illustrated in Figure 2.10 and Figure 2.11. As a result, the pipeline ADCs is considered a midlevel between the SAR ADC and the flash ADC with respect to the ADC specifications. It neither quietly reaches the flash ADCs sampling speed nor reaches the SAR ADC number of bits. For each clock cycle, a new input signal enters the ADC first stage while the existing inputs move forward to the following stage in the chain. Unlike the SAR ADC, there are various inputs being processed inside the ADC. Hence, each clock cycle a new sample could be outputted from the final stage of the ADC. This means that pipeline ADCs achieves high throughputs. However, this means that there is latency between the time of an input signal entering the pipeline ADC and the time of presenting the corresponding digital output word [5].

Each stage consists of a flash ADC (a comparator could be used for a simple representation of a 1-bit stage), a DAC block, a sample and hold block, an amplifier and a subtractor. The digital value presented from the flash ADC is converted back to an analog signal with the help of the DAC and subtracted from the original sampled input. This represents the quantization error of a pipeline ADC stage. The error is amplified and sent to the next stage. Recently, some modifications have been introduced to the CMOS pipeline ADC by combining the DAC, sample and hold, subtractor and amplifier to form a switched-capacitor circuit. This is known as a multiplying DAC.

A time alignment block should be taken in our account to store the output of each digital stage and assemble it perfectly once the conversion is completed. Most pipeline ADCs are implemented with extra bits in each stage [19], in order to reduce the comparators accuracy requirements. In additions, in order to provide some overlaps among stages, 1.5 bit stages are utilized by using 2 comparators inside the flash ADC. Hence, the amplified quantization error is within the input range of the following stage

for any error of a sampled input signal close to its threshold occurs at the current stage. However, the linearity and gain errors in the DACs and amplifiers cannot be fixed by this correction strategy. Digital control logic is applied to correct the overall quantization error, once all stages outputs are presented.

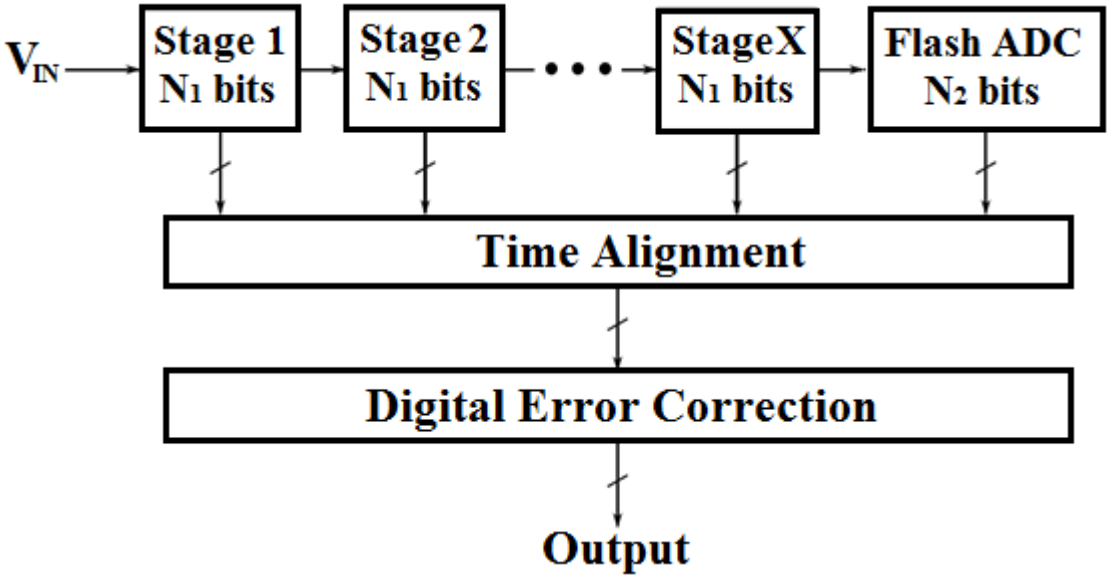


Figure 2.10: Pipeline ADC architecture

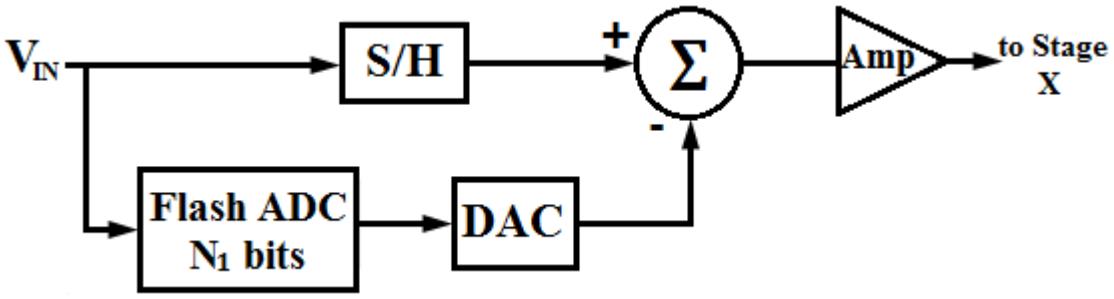


Figure 2.11: Block diagram of a single stage of a pipeline ADC

The pipeline ADC might be converted into an algorithmic or cyclic architecture, as shown in Figure 2.12, in order to decrease area and power consumption. This implementation uses a pipeline stage and a quantization voltage feedback through a switch to be processed by the same stage. The main drawback of the cyclic ADC is that it no longer takes the advantage of the pipelining speed. On the other hand, there is no issue in the data latency as a sample is processed per clock period. Moreover, it occupies a much smaller silicon area and consumes significantly less power. Furthermore, DAC, ADC and amplifier are only needed to be calibrated instead of calibration each stage components [17].

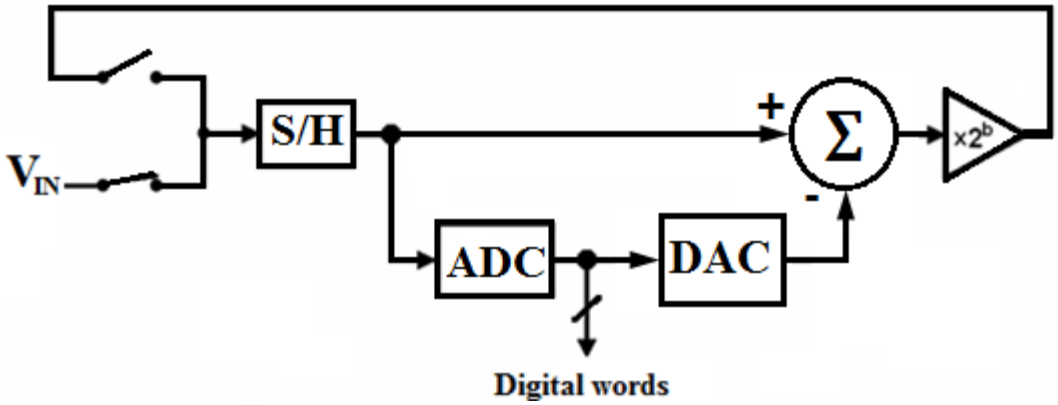


Figure 2.12: Cyclic ADC architecture

2.2.1.1.4. Time-interleaved ADC

Time-interleaved ADC is the fastest ADC that works on higher sampling rates. It consists of a number of M moderate-speed ADCs with a sampling rate of F_S/M as shown in Figure 2.13. These sub-ADCs can utilize any architectural ADC including SAR, flash or pipeline [20]. The input is sampled at the full sampling rate F_S and distributed to the sub-ADCs by the front-end sample and hold block. The M clock signals are generated with one phase-shifted frequency by the timing generation circuit. So, each sub-ADC converts an input sample every M periods of the full speed clock. In additions, these sub-ADCs have their own sample and hold circuits running at M. The sub-ADCs outputs are combined into a single digital word running at the full sampling rate by a multiplexer.

Consequently, the time-interleaving mechanism relaxes the speed requirements on the actual ADCs. However, time-interleaved ADCs suffer from offset and gain mismatches between the ADCs. As a result, calibration is highly recommended to tolerate these mismatches. In contrast, this could increase the system design complexity. Also, there is an additional power and area than single ADCs due to the additional overheads used as output multiplexing, calibration circuit and the clock generation circuit.

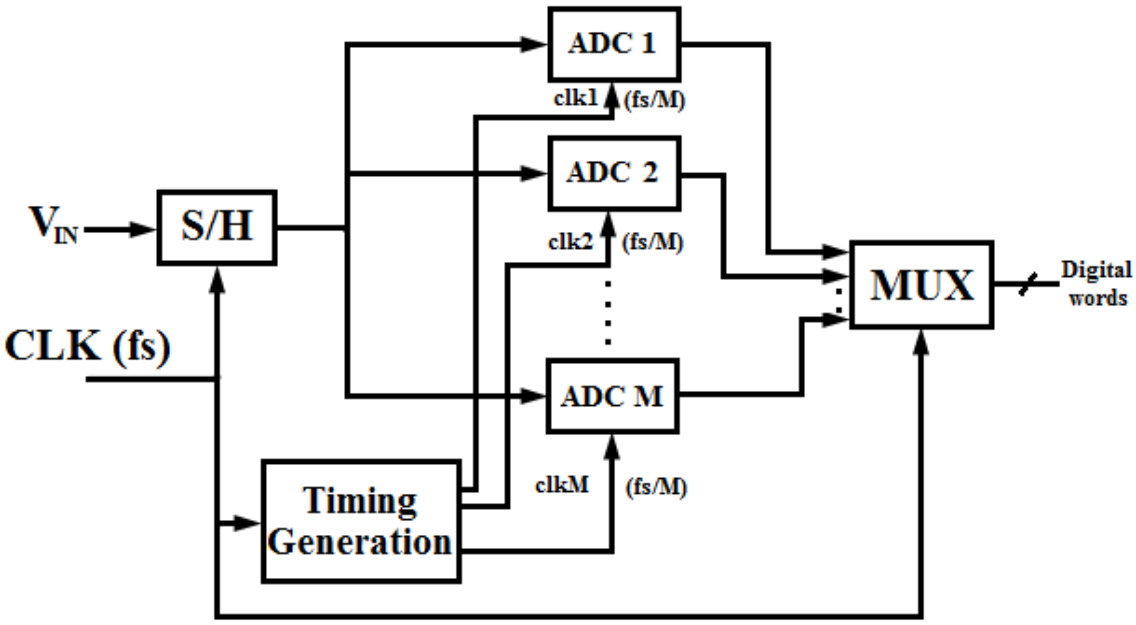


Figure 2.13: Time-interleaved ADC architecture

2.2.1.2. Oversampling ADC

2.2.1.2.1. Sigma-Delta Modulator

Sigma-Delta (ΣΔ) ADC depends on the error feedback loop to achieve high resolutions as shown in time-domain representation in Figure 2.14 (a) and Figure 2.14 (b). Equation (2.2) represents the final output form. Whereas V_{IN} is converted to a digital output word D_{OUT} with the help of a quantizer ADC block. The digital output is converter back into an analog signal V_{OUT} using a DAC block. V_{OUT} is subtracted from V_{IN} to introduce the ADC quantization error signal E_q. This quantization error is subtracted again from the new input signal value to be converted and so on. If the input signal is oversampled than the rate of the sampling frequency, there will be a relatively difference between each consecutive input samples. Hence, the quantization error could be minimized as the current and the previous errors are so close in the magnitude. On the other hand, there should be a calibration technique to the noise-shaping scheme as the quantization noise low-frequency spectral components are transformed into higher frequency ones [7].

$$D_{OUT}(n-1) = V_{IN}(n-1) + Eq(n) - Eq(n-1) \tag{2.2}$$

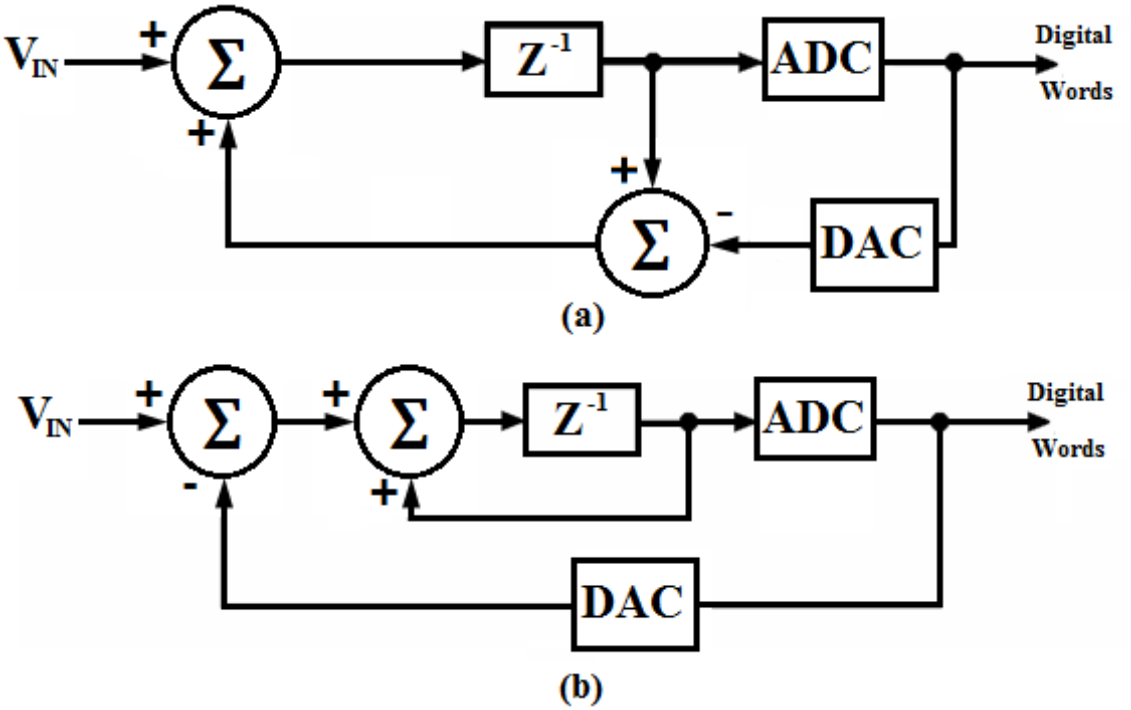


Figure 2.14: First-order ΣΔ ADC architecture. (a) error feedback model. (b) output feedback model.

The feedback loop itself could reform the implementation of the ΣΔ ADC either from the error or from the output. The internal positive feedback loop of Figure 2.14 (b) formed with the delay element could be considered an analog integrator. The external negative feedback loop needs a summation block. For linearity, ΣΔ ADC configurations use a single-bit quantizer (a comparator) which needs a 1-bit feedback DAC. To reduce the feedback quantization error, Multi-bit quantizers are recently used to reduce.

The oversampling ratio (OSR) represents how much the sampling rate is greater than the input frequency as in Equation (2.3). In additions, it reveals the signal-to-quantization-and-noise ratio (SQNR) performance as in Equation (2. 4). As a result, the ΣΔ ADC resolution enhances if the OSR of a first-order ADC increases. Due to the first-order ΣΔ ADC linearity limitations based on the DAC and the integrator blocks and the ADC resolution as in Equation (2.3), higher-order ΣΔ with a larger number of integrators ADCs are commonly used. They have an improved SQNR value as in Equation (2.5). For the second-order ΣΔ ADC as shown in Figure 2.15, the ADC resolution is improved by 2.5 bits. Also, Third and higher-order ΣΔ ADCs provides even better SQNR performance. In contrast, increasing the number of integrator could lead to an unstable system.

$$OSR = \left(\frac{F_S}{2 \times F_{IN}}\right) \tag{2.3}$$

$$SQNR = 6.02 \times N + 10 \times log(OSR) + 1.76 \tag{2.4}$$

$$SQNR = 6.02 \times N + 50 \times log(OSR) + 11.14 \quad (2.5)$$

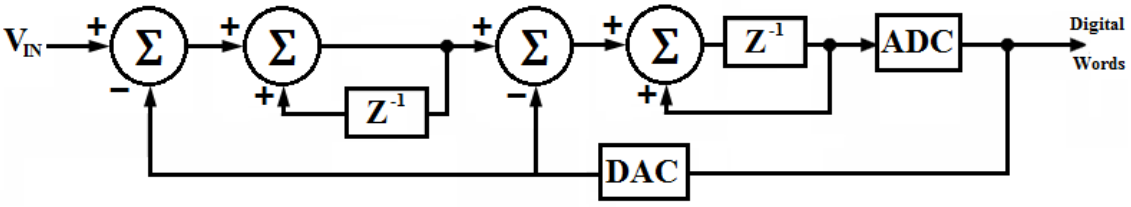


Figure 2.15: Second-order ΣΔ ADC architecture

2.2.2. Indirect conversion ADCs

2.2.2.1. Nyquist-rate ADC

2.2.2.1.1. Integrating-based ADC

Integrating (single-slope) ADCs provides a ramping voltage with a slope proportional to the input signal, as shown in Figure 2.16. The single-slope ADC samples and holds the analog input signal with the help of the sample and hold block. Then, it discharges the output using the constant current (I_{REF}) source. The comparator determines whether the ramping output reaches a fixed reference voltage (V_{REF}) between the start and stop signals, once discharging the sample and hold output value is completed after a T discharging time. An output voltage-controlled delay is represented, once the start signal reaches the stop signal edge. The counter counts the number of clock cycles needed for reaching the stop signal edge [6].

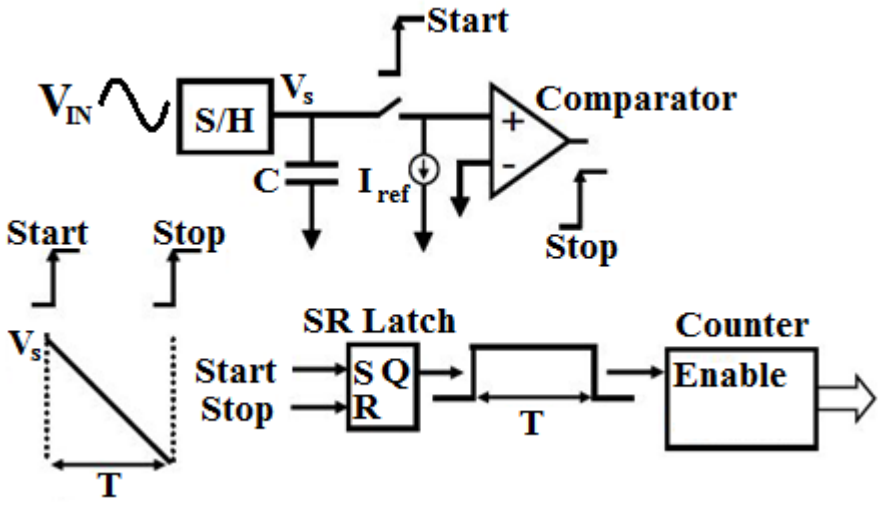


Figure 2.16: Single-slope ADC architecture

Although single-slope ADC consumes a small area and power and produces a high resolution, it modulates the input signal in a very low sampling rate as the ramping slope is so sensitive to the capacitor and resistor values. In additions, the counter timing clock

should be much faster than the sampling rate with a factor of 2^N to be able to count the delay perfectly. So the dual-slope is not promising for Giga-sampling applications.

The ADC accuracy and sampling rate could be enhanced further by decreasing the dependency on the resistor and the capacitor values. At first, the circuit ramp should be, for a fixed time, proportionally upwards to V_{IN}. Then, this ramp should be proportionally downwards to V_{REF} in order to make the ramp output reach the zero volts. In other words, the circuit ramp proportionally ends up to the ratio of V_{IN}/V_{REF}, so it is independent of the analog component (capacitor and resistor) values. This is known as a dual-slope ADC as shown in Figure 2.17.

The dual-slope ADC consists of an integrator, a comparator, control logic, and a counter. At half of the clock cycle, V_{IN} is integrated to provide the output voltage. Then, the switch converts from - V_{IN} to V_{REF} to start discharging the output voltage to reach the zero volts as illustrated in equation (2.6). Hence, the pulse width depends on V_{IN}. Finally, the counter converts the time to digital code word. Instead of using the slow power-hungry op-amp based of an integrating ADC, zero-crossing-based comparators are used to provide the output ramps in matters of power efficiency [21].

$$V_{OUT} = \left(\frac{V_{IN} \times \mathrm{T}}{\mathrm{RC}}\right) - \left(\frac{V_{REF} \times (\mathrm{T}-\mathrm{t})}{\mathrm{RC}}\right) \tag{2.6}$$

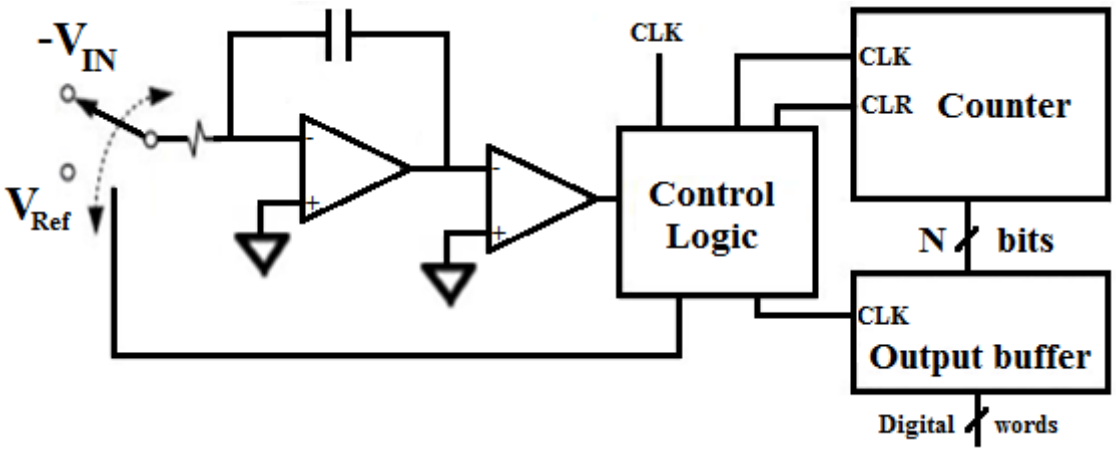


Figure 2.17: Dual-slope ADC architecture

2.2.2.2. Oversampling ADC

2.2.2.2.1. PWM-based ADC

Pulse Width Modulation (PWM)-based ADC is one of the oldest time-based ADC. PWM-based ADC shown in Figure 2.18 modulates an analog input and produces a PWM output. This output is converted to a delay using a digital counter. This technique depend on converting the amplitude to pulse width. To enhance the linearity distorted by the produced PWM signal, it is preferable to sample the input signal with a factor of 8 times the Nyquist-rate [22].

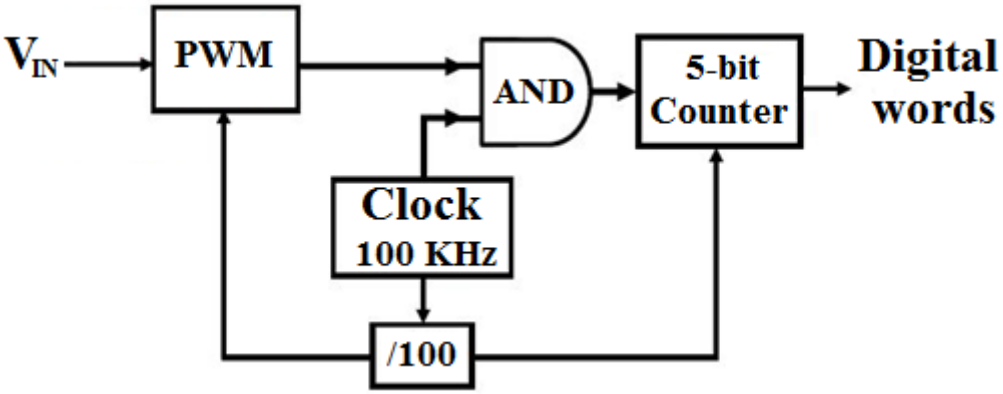


Figure 2.18: PWM based ADC architecture

2.2.2.2.2. VTC-based ADC

A Voltage-to-Time converter (VTC) circuit modulates the analog input voltage with respect to the sampling frequency and produces a series of delay pulses where each pulse is proportional to the sampled input. The produced signal including the stream of delayed pulses is expressed as pulse-position modulation (PPM) or pulse-width modulation (PWM) depending on either a pulse edge or both pulses edges are delayed, respectively. The resulting PWM pulse has a delayed edge so that the pulse gets narrower or wider depending on the input signal value. The PPM pulses have a constant width as both edges are delayed, although the entire PPM pulse is proportionally shifted to the input value. In other words, the VTC gets information from the voltage domain, where the signal value is proportional to the signal amplitude, and converts it to the time domain, where the resulting signal is proportional to the time period [12].

To complete the functionality of the ADC, the output of the VTC is fed with a time-to-digital converter (TDC), which converts the periods among pulse edges and converts them to digital code words [13]. Due to the digital circuitry, the TDC leverages the switching-speed of deep-submicron CMOS technology [8]. The VTC-based ADC architecture is shown in Figure 1.1. VTCs tend to exhibit 2 challenges: non-linearity and susceptibility to process-voltage-temperature (PVT) variations. A novel linearization technique a calibration model for several proposed designs are introduced in this thesis with to overcome the VTC issues.

2.2.2.2.3. VCO-based ADC

Voltage-controlled oscillator (VCO) based ADC modulates an analog input voltage to a frequency of a VCO. Then, it measures this frequency using various methods including sampling the output of a VCO with a fixed-frequency clock, counting the VCO clock cycles number in a set period or using a time-to-digital converter (TDC) [23].Post-conversion look-up-tables or VCO linearization techniques should be maintained to adjust the VCO non-linearity. As the oscillator frequency should be much higher than the sampling rate, VCO-based ADCs are suited for low-sampling-rate applications so as to integrating ADC architectures.

2.3. Performance metrics

2.3.1. ADC characteristics

2.3.1.1. Gain Error

An ideal ADC has a typical unity gain, so the full scale analog input voltage range maps to 2^N digital code output organized in a uniform way [17]. Practically, the ADC gain slope is shifted from the unity slope as shown in Figure 2.19. Hence, the full scale input voltage range decreases if the ADC gain is greater than the unity one. As a result, most digital code output could not be obtained or exercised. In additions, the Least Significant Byte (LSB) length deviates than the ideal one as in equation (2.7). Where V_{FS}, N and G are the full scale voltage, number of bits and the gain factor, respectively.

$$LSB = G \times \frac{V_{FS}}{2^N - 1} \tag{2.7}$$

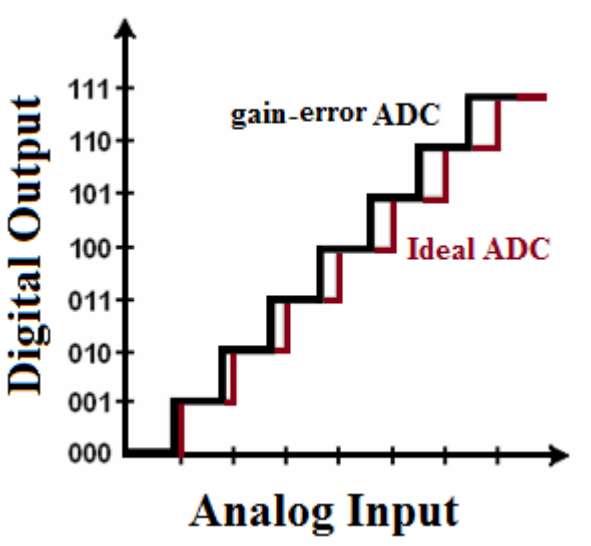


Figure 2.19: ADC gain error

2.3.1.2. Offset Error

The ADC offset error is the deviation between the ideal ADC characteristic line and the actual ADC characteristic line, as illustrated in Figure 2.20. The main reason of the ADC offset error is the mismatch between the operational amplifier terminals due to the component itself variations or the technology fabrication [4]. The ADC offset error results in transitions in the digital code words that occur at the analog input voltages.

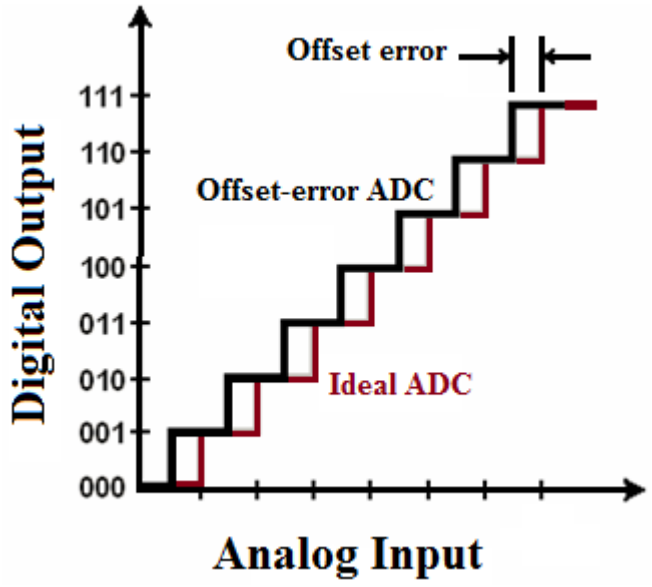


Figure 2.20: ADC offset error

2.3.1.3. Integral Non-Linearity

The ADC integral non-linearity (INL) [5] is the deviation between the actual output of an ADC transfer function and the ideal straight line output of an ideal ADC transfer function as shown in Figure 2.21. Hence, INL typically measures the transitions of the ADC straight line. INL should be within the range ±0.5 LSBs, to have a linear ADC. INL could be measured as in equations (2.8) and (2.9). Where C(n) and DNL are the actual digital code width of the word n and the differential non-linearity of an ADC transfer function.

$$\mathrm{INL(m)} = \sum_{i=0}^{m}(DNL) \tag{2.7}$$

$$\mathrm{DNL(n)} = \frac{C(n)-1\ LSB}{1\ LSB} \tag{2.8}$$

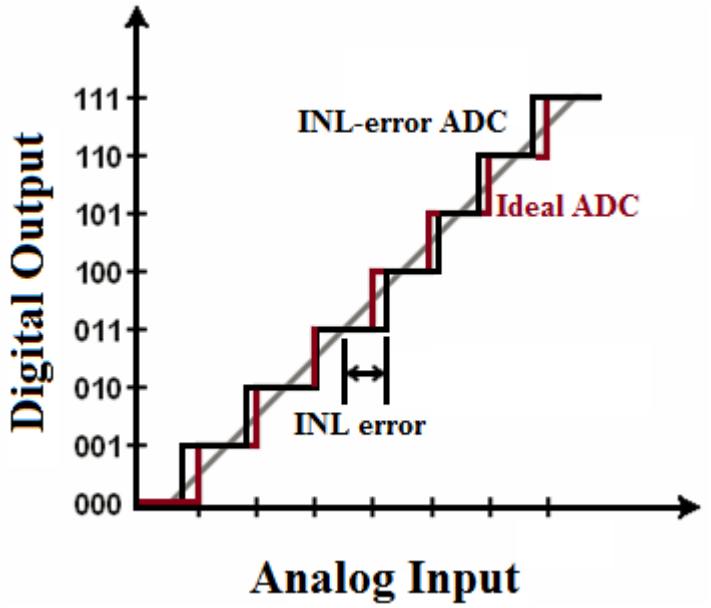


Figure 2.21: ADC integral non-linearity

2.3.1.4. Differential Non-Linearity

The ADC DNL [22] is the deviation between an ideal code width and an actual width of a LSB as shown in Figure 2.22. It can be measured as in equations (2.7) and (2.8). If it exceeds the width of a LSB, the ADC output probably has some missing codes.

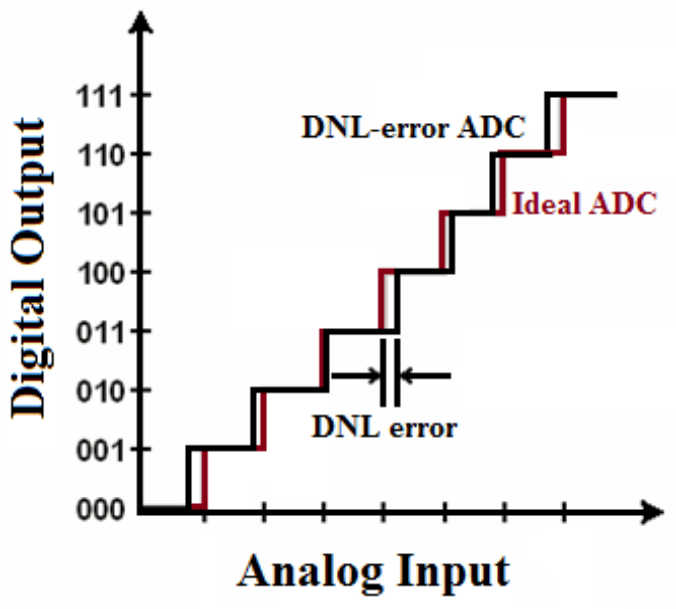


Figure 2.22: ADC differential non-linearity

2.3.1.5. Missing Codes

Missing codes is a result of the ADC design defects which result undesired skips of one or more of the ADC digital output codes as in Figure 2.23. They could affect the ADC linearity badly. The main reasons of having some missing codes are having the maximum INL of an ADC becoming less than 0.5 LSB or having the maximum DNL of an ADC becoming less than 1 LSB [17].

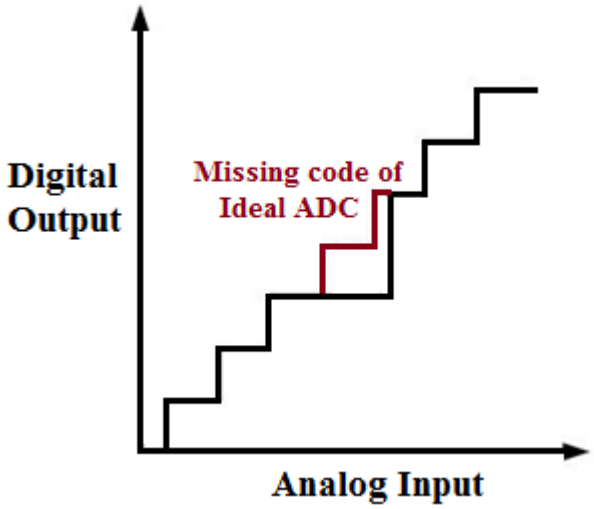


Figure 2.23: ADC missing code output

2.3.2. VTC characteristics

2.3.2.1. Linearity and Dynamic Range

Due to the scaling down of emerging CMOS technology, the gate oxide thickness of a transistor decreases as well the supply voltage. As a result, the transistor region that has a linear operation reduces. Consequently, the utilized ADC input voltage signal swing is reduced. This means that the ADC dynamic range is loosely defined as the input amplitude range which is larger than the distortion and noise of the circuit itself. Therefore, this dynamic range suffers whether the noise and/ distortion are increased or the output signal swing is decreased [5].

To be able to get a perfect dynamic range that suits the VTC/ ADC circuit, an iteration technique is used to scan for this linear range. To have an acceptable linearity error (i.e. the maximum acceptable error value is 3% [6]), the input voltage, V_{IN}, is swept in matters of delay to scan for the linear dynamic that achieves this acceptable error value in the delay-versus-V_{IN} waveform. After estimating a linear line from the waveform, the linearity is checked on MATLAB for this range. After a number of iterations, the 3% acceptable error is reached. The linearity error check is based on curve fitting method, in which the difference should be measured between the ideal first-order fundamental coefficients that fit actual points that are produced from the Cadence schematic design and the fundamental coefficients of the actual linear equation [15].

2.3.2.2. Voltage sensitivity

After getting the circuit dynamic range, the VTC voltage sensitivity could be calculated. Within the dynamic linear range, the first and last points are used to evaluate the slope between the delay on y-axis and V_{IN} on x-axis [15]. A higher sensitivity means that the delay of the circuit is enhanced. Although the high sensitivity is preferred for a TDC block to be able to sense the delay changes over the linear range, the higher resulting delay affects the ADC conversion speed and stability.

2.3.2.3. Maximum Sampling Frequency

The VTC bandwidth is typically defined by the frequency range over which the VTC maintains its quoted resolution. The input signal bandwidth and sampling frequency are expressed by the Nyquist criterion. Hence, the sampling rate should be equals to at least the double of the input signal bandwidth. There are many applications require specific sampling rate ranges and resolution from the ADC circuit as a whole as illustrated in Table (2.1) [5].

Table 2.1: ADC resolution and sampling rate for various applications

Application	Resolution (bits)	Sampling rate (Hz)
Sensors, Energy monitoring, Motor-control	16 – 24	1 – 100
Audio market	12 – 16	48k – 192k
Data acquisition systems	12 – 18	500k – 5M
Medical Imaging	10 – 16	5M– 200M
Communication	10 – 14	30M– 100M
Instrumentation	10 – 14	5M – 100M
Consumer electronics	10 – 12	5M– 75M
Digital Video	12 – 14	29M– 100M
Software Defined Radio	12 – 14	125M – 500M
Test & Measurement Direct RF Down conversion High-Speed Data Acquisition	6 – 8	0.5G – 4G

In fact, as increasing Fs than the operating one distorts the signal linearity, the dynamic range is reduced to keep the acceptable error below 3%. This procedure is permitted, as long as the effective number of bits (ENOB) is high. On the other hand, high-frequency applications have larger power dissipation (P_D). This power is minimized by decreasing transistors' size.

2.3.2.4. Total Harmonic Distortion

The Total Harmonic Distortion (THD) is one of the main metrics for quantifying the circuit linearity. THD is a measure of the ratio of the square root between all input signal harmonics root-mean-square (RMS) value ($V_{i,RMS}$) and the harmonically-related distortion component (the fundamental frequency $V_{F,RMS}$). The THD is expressed in decibels as in equation (2.9). THD is calculated by replacing the DC Input Voltage with a sinusoidal waveform.

$$THD = 20 \times \log\left(\sqrt{\frac{\sum_{i!=1}^{n} V_{i,RMS}}{V_{F,RMS}}}\right) \quad (2.9)$$

2.3.2.5. Signal-to-noise-and-distortion ratio

The signal-to-noise-and-distortion ratio (SNDR) is the ratio of the input signal RMS value ($V_{I,RMS}$) to the sum of the RMS value all harmonics components ($V_{D,RMS}$), except for the fundamental one, over a defined bandwidth adding to the overall RMS value of the circuit referred noise ($V_{N,NRMS}$), but excluding the DC component. SNDR is usually expressed in decibels as in equation (2.10). The total SNDR value represents the harmonics and the noise of both the VTC and TDC circuits. To calculate the SNDR value, the output of the TDC circuit should be converted again into analog voltages using a digital-to-analog converter (DAC) in order to compare the resulting error value with the corresponding analog input of the VTC circuit [22].

$$SNDR = 20 \times \log\left(\frac{V_{i,RMS}}{V_{D,RMS} + V_{N,RMS}}\right) \quad (2.10)$$

2.3.2.6. Effective Number of Bits

ENOB is considered the main metric that tests all different types of errors (including noise and distortion errors) that a VTC practically faces. The signal-to-noise-and-distortion (SNDR) ratio should be measured at first in order to get the ENOB using equation (2.10) and (2.11).

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (2.11)$$

2.3.2.7. Resolution

The ADC Resolution [22]is a measure of how the digital code word output represents the analog signal input accurately. It might be denoted as the smallest analog signal input change which results in a LSB change in the digital code word output. The ADC Resolution is expressed as the number of bits (N) of the digital output. Table 2.1 presents the resolution of various applications. As the sampling frequency of a specific ADC increases, the ADC resolution decreases. In additions, the circuit non-linearity and noise affects the ADC resolution inversely.

2.3.2.8. Noise

Noise represents a random environmental fluctuation in any electrical signal [24]. Noise sources include thermal noise, cross talk, power supply noise, electromagnetic interference, flicker noise and clock jitter. Thermal noise is the main dominant noise parameter of a MOSFET transistor represented in equation (2.12). Whereas $V_{N,TH}$ is the RMS voltage due to thermal noise generated in a resistance (R) over a bandwidth (ΔF) in a room temperature (T). The thermal noise can be reduced by innovative circuit design techniques. In additions, cross talk can also be eliminated with some layout techniques.

Clock jitter and power supply noise are ADC external influences and significantly affect the ADC performance [24]. In fact, noise falls off steadily at low frequencies, due to the flicker noise effect. Then, a wide noise which appears over the frequencies represents the thermal noise. In fact, the total RMS noise should be less than a single step conversion of the ADC as in equation (2.1).

$$V_{N,TH} = \sqrt{4 \times K \times T \times R \times \Delta F} \tag{2.12}$$

2.3.2.9. Area

The area of a design inevitably occupies an area, when the design is laid out in a silicon-based technology. As area increases, the cost of the silicon grows proportionally. Moreover, within the technology, CMOS processes subject to defects. The density of these defects statistically affects larger circuits. As a result, decreasing area reduces cost and the probability of a failed circuit design due to defects.

2.3.2.10. Power

Minimizing circuit power dissipation is one of the main majors to any circuit design. In large VLSI systems where analog, mixed-signal and digital components are integrated together, the maximum power consumption is governed and stipulated by power supply restrictions (e.g. battery powered devices) and circuit reliability issues. As such, a power budget is allocated to a VTC. The power dissipation control is achieved with circuit design techniques and architectural selection [8].

2.3.2.11. Figure-of-Merit

R.H. Walden in [25] has discussed 2 approaches to calculate the Figure-of-Merit (FOM) to be able to compare among all VTC designs regarding their different technology node, circuit topology, resolution, operating sampling frequency, area and power consumption. These approaches are illustrated in equations (2.13) and (2.14), respectively. Where P_D and F_B are the dissipated power and the lower of either the Nyquist frequency or the effective resolution bandwidth. FOM_1 describes how much the VTC has an efficient performance in terms of its higher dynamic range, higher sampling rate and lower power dissipation. While, FOM_2 describes how much the VTC lacks in performance and its design is deficient in terms of its high power dissipation, lower ENOB and bandwidth. As a result, a better performance shows in a high FOM_1 and a low FOM_2. In general, the FOM represents the efficiency of using the power to increase the maximum frequency and/or the DR.

$$FOM_1 = \frac{F_S \times DR^2}{P_D} \tag{2.13}$$

$$FOM_2 = \frac{P_D}{(2F_B) \times 2^{ENOB}} \tag{2.14}$$

Chapter 3 : Novel Differential VTC circuits for High-Speed SDR applications

In this chapter, an introduction to the current starving VTC circuits is discussed. Then, the concept of basic differential VTC circuits will be discussed for a falling VTC circuit and a rising VTC circuit. Moreover, a differential architecture will be proposed for a high-resolution high-sensitive new design methodology and an enhanced one, respectively. Finally, a differential architecture for a high-speed VTC circuit is discussed. The proposed designs are eligible for the use in SDR applications due to their higher sampling rate and their higher accuracy.

3.1. Introduction

Currently, smartphones are considered multi-standard receivers. They include receiver chains to deal with their corresponding frequency once the signal availability is placed in the surroundings. These receivers' chains, as shown in Figure 3.1, include: GSM, WIFI, Bluetooth, CDMA, etc. The main challenging aspect for the smartphones is that once they are turned on, all receivers' chains work automatically to search on the signal availability. This consumes much power [5].

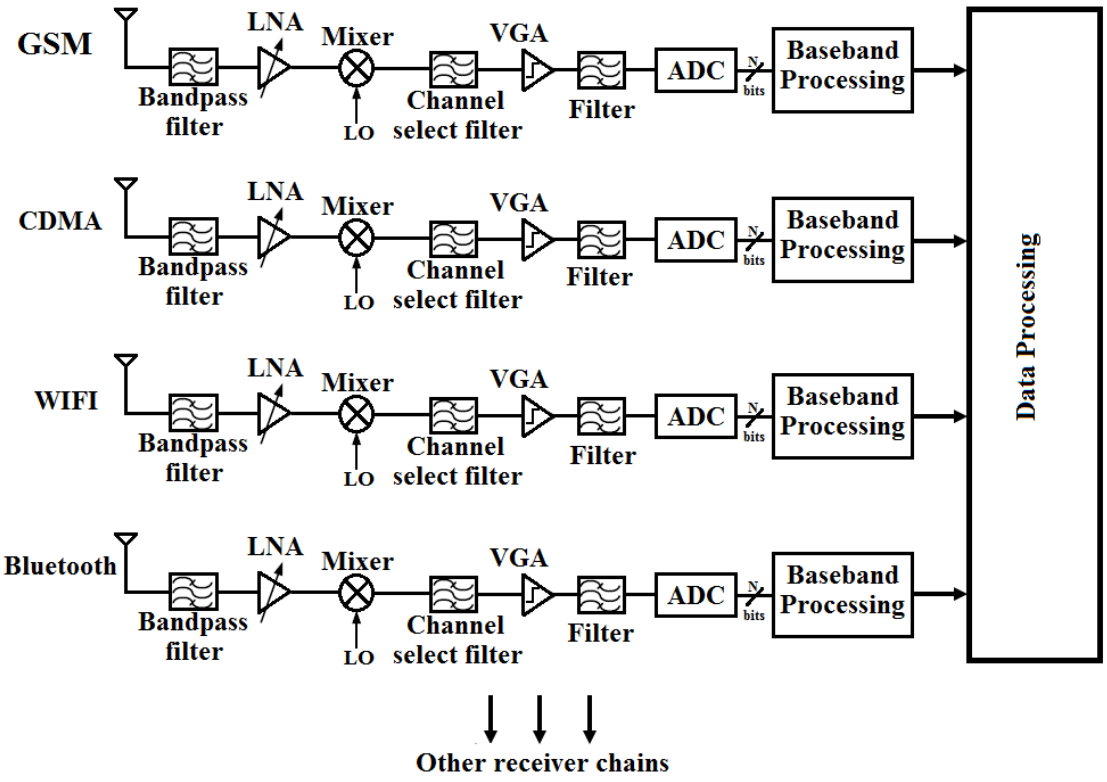


Figure 3.1: Smartphone receiver chains.

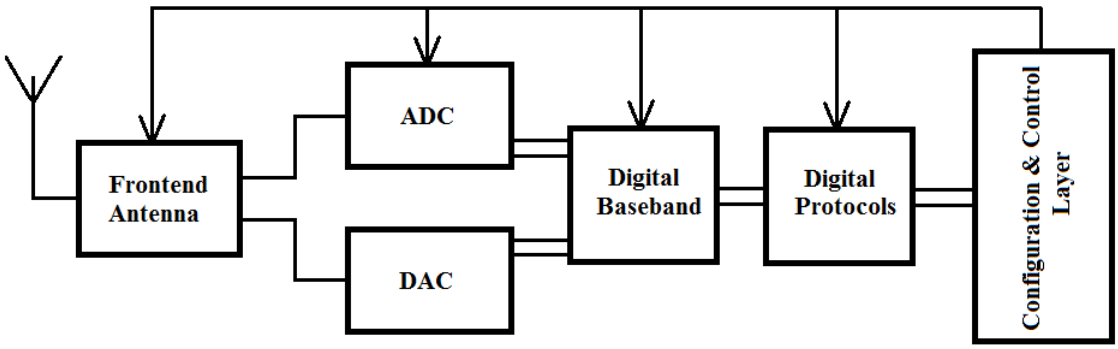


Figure 3.2: Software defined radio receiver block diagram.

The main advantage of the SDR receiver is that it can reconfigure and control the hardware to be suitable for dealing with the aimed technology (GSM, WIFI, CDMA, etc). Hence, there is a single used chain at a time instead of turning all other chains as in smartphones. Consequently, the SDR receiver integrated circuit consumes a much lower power and area. On the other hand, it should have a higher performance and resolution based on the toughest communication protocol requirements that can be built-in.

Figure 3.2 shows the block diagram of an SDR receiver in which it consists of only one chain. The analog blocks in this receiver are considered the frontend antenna and the ADC/DAC [5]. While others are digital blocks. All blocks are controlled by the configuration and control layer. The main objective of the frontend antenna is to (1) receive any allowable frequency signals, (2) condition the desired signal for further DSP, and (3) do amplification to the required ADC level with lowering down the noise level to achieve a compatible dynamic range with ADC (which is limited by noise and interference).

The digital baseband block does the job of the most analog blocks of Figure 3.1. It (1) rejects as many undesired signals as possible, (2) mixes the signal frequency translation digitally to comply with ADC sample rate limitations, (3) selects the aimed channel bandwidth, (4) amplifying variably the signals amplitudes, and finally (5) processes the received signals digitally. This means that all analog challenging problems are analyzed and become more feasible after processing them digitally with the help of the software tunable analog frontend. The digital baseband block has an impedance synthesizer subsystem to optimize the performance of the software tunable analog radio systems

Actually, SDR requirements of an ADC (small area and low power dissipation) are relaxed at deep sub-micron CMOS technology, as well as, with the use of a TADC technique. Operating on low CMOS technology nodes could produce smaller area and higher SNR. While, designing a TADC produces: (1) a higher time resolution, (2) more DSP flexibility, and (3) a reduced power and area consumption.

By using the CMOS technology of the 65 nm node, this chapter focuses on proposing a new VTC design methodology and designing a fully-differential architecture with an on-chip calibration method to tolerate the process-voltage-temperature (PVT) variations node, this chapter focuses on proposing a new VTC design methodology and

designing a fully-differential architecture with an on-chip calibration method to tolerate the process-voltage-temperature (PVT) variations.

In fact, the differential architecture enhances the VTC specifications. It enlarges the SNDR, ENOB, FOM_1, sensitivity, dynamic range with some overheads in the consumed power, area and noise. Despite of these overheads, they could not be compared with respect to the much low area and power of the TADC technique.

This chapter provides several novel VTC circuits based on the differential mechanism as shown in Figure 3.3 where the core of this mechanism is changed from proposed design to others. The applied input voltage of each VTC core equals to $+V_{IN}/2$ and $-V_{IN}/2$, respectively. In additions, a square-pulse clock is provided for each core to sample the analog input signal as well as a DC input voltage.

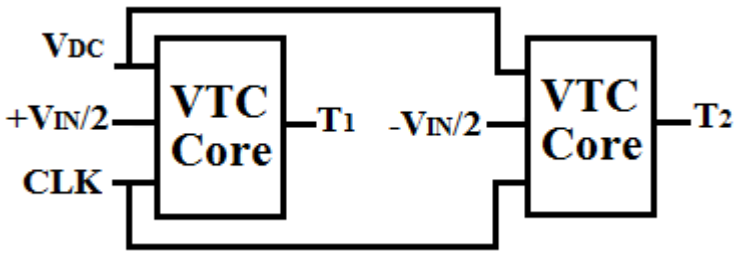


Figure 3.3: The differential VTC architecture

The rest of Chapter 3 discusses some basic differential circuits as a starter where they are compared to their single-ended designs. These circuits are implemented using Taiwan Semiconductor Manufacturing Corporation (TSMC) 65-nm CMOS technology and their results have been tested using MATLAB. These designs are as following:

1. A differential falling VTC circuit: It is a modified VTC circuit from the basic VTC circuit to have an enhanced linearity. In additions, it controls the falling delay time of the applied analog input voltage.

2. A differential rising VTC circuit: It is a modified VTC circuit from the basic VTC circuit to have an enhanced linearity. In additions, it controls the rising delay time of the applied analog input voltage.

3. A differential VTC methodology circuit: It is a novel VTC design that controls the falling and the rising delay times of the applied analog input voltage. It provides an ENOB of 10.7 bits. Besides, it has a higher dynamic range, SNDR and FOM at 2.5 GS/s operating sampling frequency.

4. A modified differential VTC methodology circuit: It is the first proposed novel VTC design where a high-sized inverter is added to one of the previously mentioned design's core in order to produce a higher ENOB. The ENOB of this circuit is 12.8 bits at 1 GS/s operating sampling frequency. A study of the PVT variations is done for this design. A Metal-Insulator-Metal

(MIM) capacitor is used to minimize the PVT variations. Moreover, a calibration circuit is proposed to compensate these variations.

5. A differential high-speed VTC circuit: It is the second proposed novel VTC design where it achieves an ENOB of 8.9 bits at 8 GS/s operating sampling frequency.

3.2. Differential falling VTC circuit

3.2.1. The differential falling VTC design

The core of this differential design is a falling VTC circuit which controls the output falling edges. This results in a Pulse Position Modulation (PPM) VTC design. Figure 3.3 shows the whole block diagram of the differential design, while Figure 3.4 shows the single core design. T_F is the fall delay of the falling VTC circuit in which the *Na2* transistor width is increased for a high discharging rate of the load capacitor (C_L). The falling circuit delay equation of each core is the difference in time between the falling edge of the design output and the rising edge of the clock. After measuring the delay of each core, the difference between them is the overall delay of the differential falling VTC circuit.

This circuit is as same as the basic current-starved VTC circuit (i.e. it consists of *Na2*, *Na3* and *Pa1* transistors) with a simple modification as revealed in the *Na1* transistor of Figure 3.4. This transistor is used to add another path to flowing current to make the circuit be in the on-mode instead of the off-mode, in case of lower values of $V_{IN}/2$. Furthermore, *Na1* width should be much smaller than *Na2* transistor. As a result, it has a higher resistance enough to make the current flow easier through *Na2* which has a higher size. Consequently, the dynamic linear range increases.

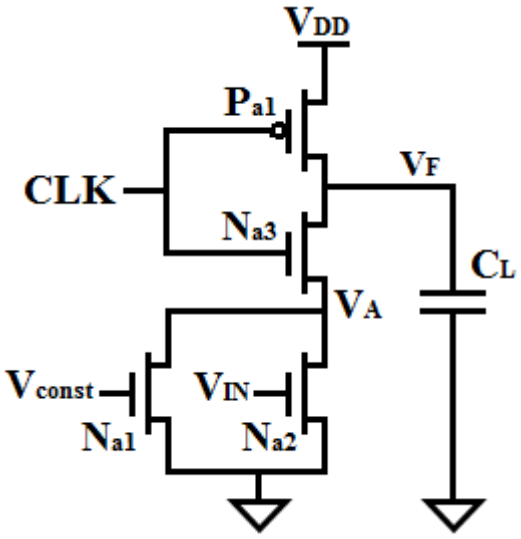


Figure 3.4: Circuit schematic of the core of a differential falling VTC circuit.

The clock controls *Pa1* and *Na3* transistors, while the analog input voltage controls *Na2* transistor. At the steady state, the clock signal and the drain voltage of *Na1* and *Na2* (V_A) are at logic '0' (low signals), while transistors *Pa1*, *Na1* and *Na2* are in deep triode region and *Na3* is in cut-off region. V_A begins with 0 volts when the V_{CONST} is not applied.

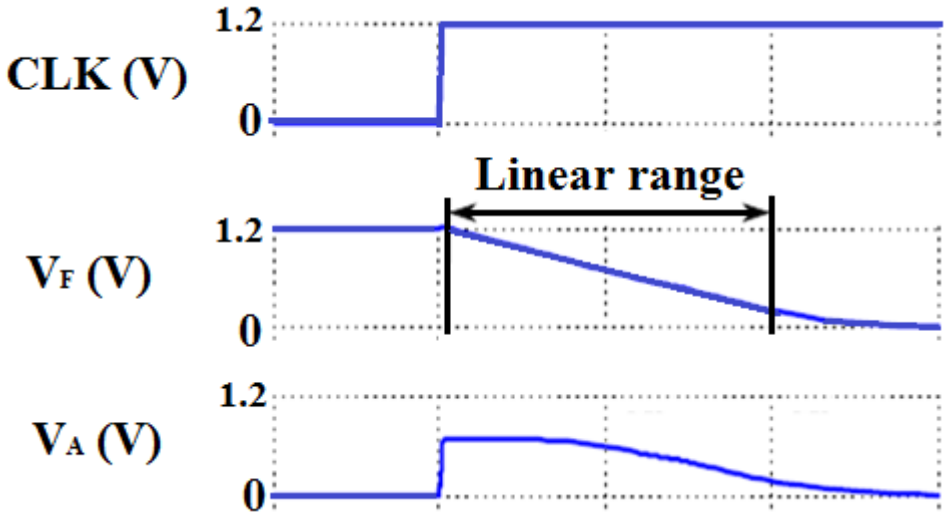


Figure 3.5: VTC operation mode timing diagram.

Once the clock signal rises up, *Pa1* enters the cut-off region, while *Na3* goes to the saturation mode. At this moment, the stored charge of C_L passes through Na3 and makes V_A increase rapidly. Afterwards, during the V_A increase, *Na1* and *Na2* transistors leave the deep triode region and enter the saturation mode. As a result, the current flowing through *Na3* is limited and equals to the current flowing through *Na1* and *Na2*. This fixed current sets the gate-source voltage of *Na3* to a constant value. Furthermore, the VTC output (V_F) decreases linearly in a ramp-down shape at a constant rate equals to the total capacitance divided by the total current. V_F is the inverted falling edge version from the clock rising edge.

Due to the continuous decrease of V_F, Na3 enters the triode mode if its drain-source voltage becomes less than its gate-source voltage subtracted from its threshold voltage. Hence, the Na3 gate-source voltage is no longer a constant value causing a voltage decrease to V_A node. On the other hand, the current flowing through Na3 is still at its maximum value making the V_F in the same linear ramp-down shape.

Once the V_A reaches the maximum value of either V_{IN} - V_{TH2} or V_{CONST} - V_{TH1}, *Na1* and *Na2* enter the triode mode. Where V_{TH1} and V_{TH2} are the threshold voltage of *Na1* and *Na2*, respectively. Hence the Na3 current decreases and the V_F ramp is changed into a non-linear slope. Finally, V_F and V_A return to their steady state. The whole timing operation mode is shown in Figure 3.5.

3.2.2. **Simulation results**

As mentioned in Section 2.3.2.1, iteration method has been done to achieve the highest linear range that could be provided from a VTC circuit with a linearity error of 3 percent. The input voltage linear range of the differential VTC circuit is from 264 mV to 264 mV (i.e. the dynamic range is 528 mV). The circuit sensitivity is 1 ps/mV. Area and the consumed power are: 0.83 μm^2 and 19 µW. The applied input DC voltage is about 600 mV, while the supply voltage is 1.2 V.

Simulations have been carried out using an operating clock frequency of 250 MS/s, while the maximum sampling frequency ($F_{S,MAX}$) that the circuit can achieve with keeping the linearity range high (i.e. higher than the linearity range of a VTC single-ended design) is 4 GS/s. At operating on the 4 GS/s $F_{S,MAX}$, the differential design has a dynamic range of 364 mV and a sensitivity of 0.5 ps/mV.

The maximum power consumed at this high frequency is 259 µW. This consumed power could be considered a dynamic power of a CMOS circuit during the high frequency switching. FOM_1 is the Figure-of-Merit stated in Section 2.3.2.11 which is defined by the maximum sampling frequency that a circuit can operate on, the input linear range and the dissipated power. It equals to 3.59×10^{12} and 2.05×10^{12} in case of a sampling frequency of 250 MS/s and 4 GS/s, respectively. Operating on a higher sampling frequency produces a higher power consumption. This decreases the FOM_1 than that value produced at a 250 MS/s sampling frequency.

The Total Harmonic Distortion (THD), as discussed in Section 2.3.2.4, equals to -17.3 dB where the input frequency (F_I) is chosen to satisfy the Nyquist criterion to be 100 MS/s while the sampling frequency equals to 250 MS/s. The maximum THD which equals to -23.3 dB, is achieved at a 1.8 GS/s maximum allowed input frequency ($F_{I,MAX}$) and a 4 GS/s sampling frequency.

Figure 3.6(a), Figure 3.6(b) show the differential falling VTC design curve fitting of the input dynamic range and the check of the linearity error of at a 250 MS/s sampling frequency. Moreover, Figure 3.6(c), Figure 3.6(d) show also both of them at a 4 GS/s sampling frequency.

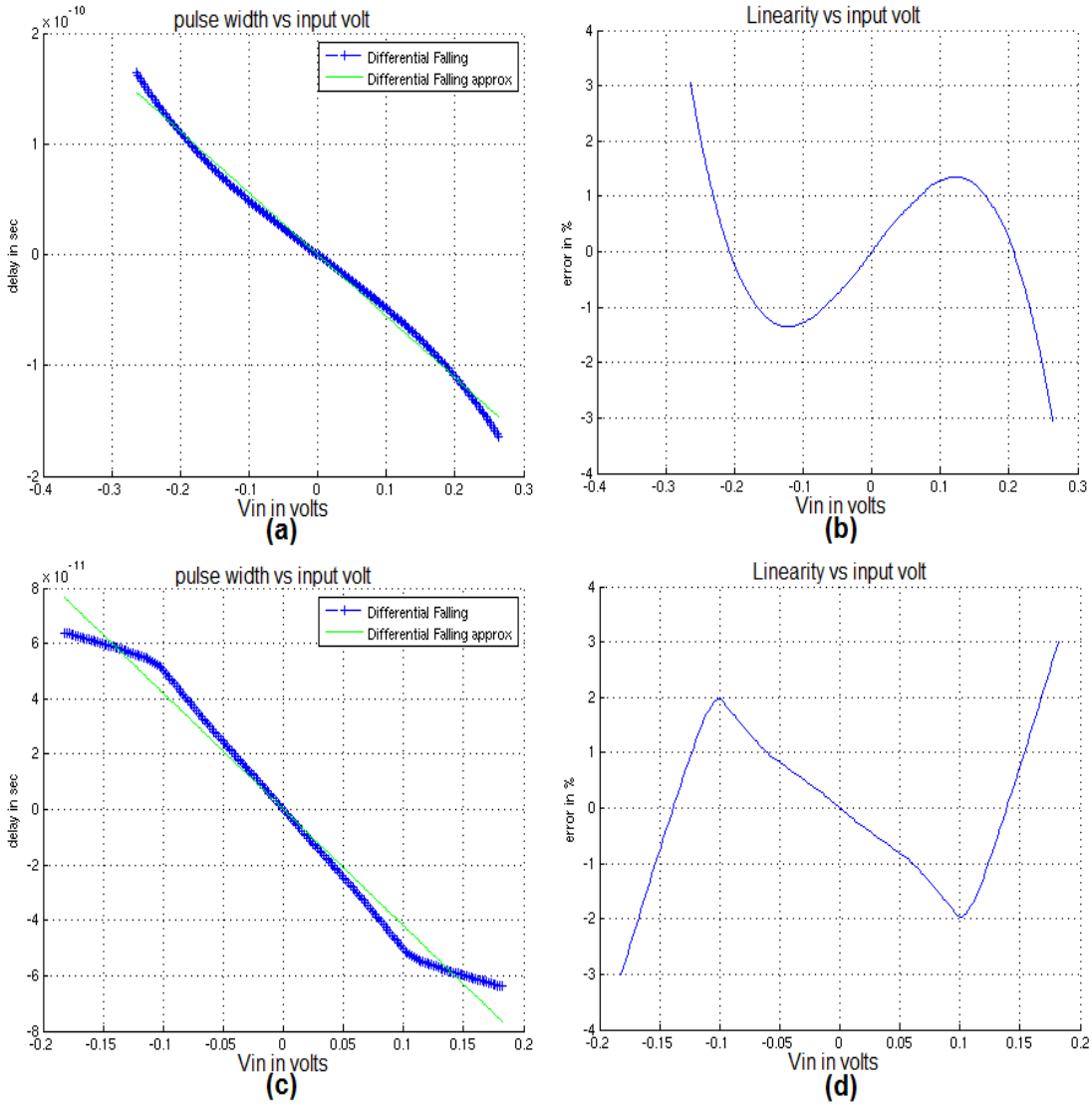


Figure 3.6: Differential falling VTC. (a) Linear range at F_S = 250 MS/s. (b) Linearity error check at F_S = 250 MS/s. (c) Linear range at $F_{S,MAX}$ = 4 GS/s. (d) Linearity error check at $F_{S,MAX}$ = 4 GS/s.

Table 3.1: Performance comparison between the differential falling VTC circuit and its single-ended design @ 3% linearity error

Parameter	Differential Falling VTC	Falling VTC of [26]
$F_{S,MAX}$ (GS/s)	4	1.6
VTC Area (μm^2)	0.83	0.41
DR @F_S/$F_{S,MAX}$ (mV)	528/364	240/80
Sensitivity (ps/mV)	1	0.6
P_D @F_S/$F_{S,MAX}$ (μW)	19/259	10/-
THD (dB) @F_I/$F_{I,MAX}$	-17.3/-23.3	-9.9/-
FOM_1 @F_S/$F_{S,MAX}$ ($\times 10^{12}$)	3.6/2	1/-

Table 3.1 compares at a 3% acceptable linearity error the specifications of the differential VTC design with the corresponding single-stage falling VTC design of [26]. The differential design has a higher dynamic range (DR), FOM_1 and sensitivity. The higher sensitivity is provided due to the high delay produced by the differential design regarding the higher number of the used MOSFETS. On the other hand, the single-ended design has lower area and power consumption. Furthermore, the differential design can operate on a higher sampling frequency than the single-ended design due to the larger dynamic linearity range.

Table 3.2 reveals, at a 3% acceptable linearity error, the design specifications of the differential falling VTC circuit corresponding to various sampling frequencies with their configured clock rise and fall times. The clock rise and fall times should be identical in order to have a symmetric design output. Moreover, they should in range of 1 % : 10 % from the overall clock sampling frequency in order to achieve the maximum dynamic range. The design has a higher dynamic linear range and FOM_1, in additions to a lower consumed power at low frequencies. On the other hand, the higher sampling frequencies has a lower FOM_1 due to the high consumed power. Operating on a clock frequency of 5 GS/s is not recommended due to the few dynamic range that is provided by the circuit (i.e. less than the dynamic range that the single-ended design provides).

Table 3.2: Performance comparison of the differential falling while sweeping the sampling frequency with a 3% linearity error.

Clock Sampling Frequency (GS/s)	Clock rise and fall times (pS)	Dynamic Range (mV)	Input Linear Range (mV)	Power (µW)	FOM_1 ($\times 10^{12}$)
0.25	40	528	-264 : 263	19	3.6
1	10	526	-263 : 263	96	2.9
4	2	364	-128 : 128	259	2
5	2	170	-85 : 85	280	0.5

3.3. Differential rising VTC circuit

3.3.1. The differential rising VTC design

This design is based on the complementary functionality of the falling VTC circuit. The core of this differential design is the rising VTC circuit which controls the output rising edges. Figure 3.7 shows the single core design with inverted clock pulses to ensure modulating the output rising edges. T_R is the rise delay of the rising VTC circuit in which the width of *Pb2* is greater than *Pb3* for a high charging rate of the load capacitor. The PPM rising circuit delay equation of each core is the difference in time between the rising edge of the design output and the falling edge of the clock. After measuring the delay of each core, the difference between them is the overall delay of the differential rising VTC circuit shown in Figure 3.4.

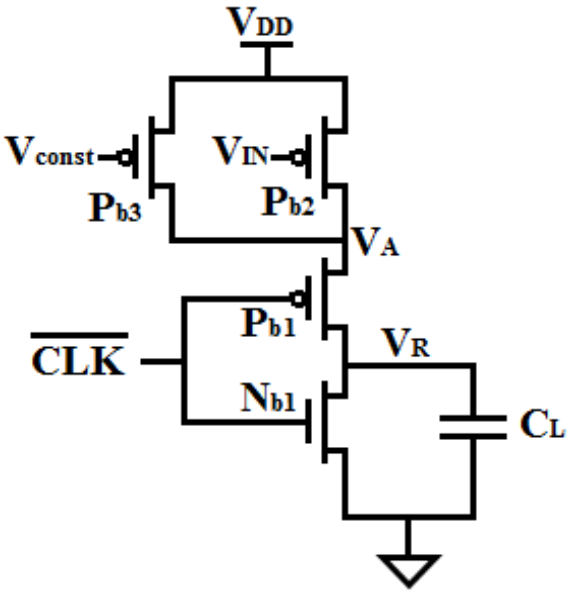


Figure 3.7: Circuit schematic of the core of a differential rising VTC circuit.

3.3.2. Simulation results

The input voltage linear range of the differential rising VTC circuit is from -568 mV to 568 mV (i.e. the dynamic range is 1136 mV). As the node V_F parasitic capacitances are so small compared to that of the differential falling design, this design has a higher dynamic range. Consequently, the circuit speed is so limited (i.e. $F_{S,MAX}$ is only 700 MS/s). The circuit sensitivity is 2.7 ps/mV. Area and the consumed power are: 0.63 μm^2 and 15.7 µW. The DC voltage is 600 mV, while the supply voltage is 1.2 V.

Simulations have been carried out using an operating clock frequency of 250 MS/s, while the maximum sampling frequency ($F_{S,MAX}$) that the circuit can achieve with keeping the linearity range high is 0.7 GS/s. At operating on the 0.7 GS/s $F_{S,MAX}$, the differential design has a dynamic range of 620 mV and a sensitivity of 1.7 ps/mV. The maximum power consumed at this high frequency is 37 µW. FOM_1 equals to 20.5×10^{12} and 7.2×10^{12} in case of a sampling frequency of 250 MS/s and 0.7 GS/s, respectively. THD equals to -18 dB at a 50 MS/s F_I and a 250 MS/s F_S, while it equals to -15.4 dB, is achieved at a 1.8 $F_{I,MAX}$ and a 400 MS/s F_S.

Table 3.3: Performance comparison between the differential rising VTC circuit and its single-ended design @ 3% linearity error

Parameter	Differential Rising VTC	Rising VTC of [26]
$F_{S,MAX}$ (GS/s)	0.7	0.3
VTC Area (μm^2)	0.63	0.32
DR @F_S/$F_{S,MAX}$ (mV)	1136/620	400/140
Sensitivity (ps/mV)	2.7	2.5
P_D @F_S/$F_{S,MAX}$ (µW)	16/37	9/-
THD (dB) @F_I/$F_{I,MAX}$	-15.4/-18	-12.5/-
FOM_1 @F_S/$F_{S,MAX}$ ($\times10^{12}$)	20.5/7.2	0.14/-

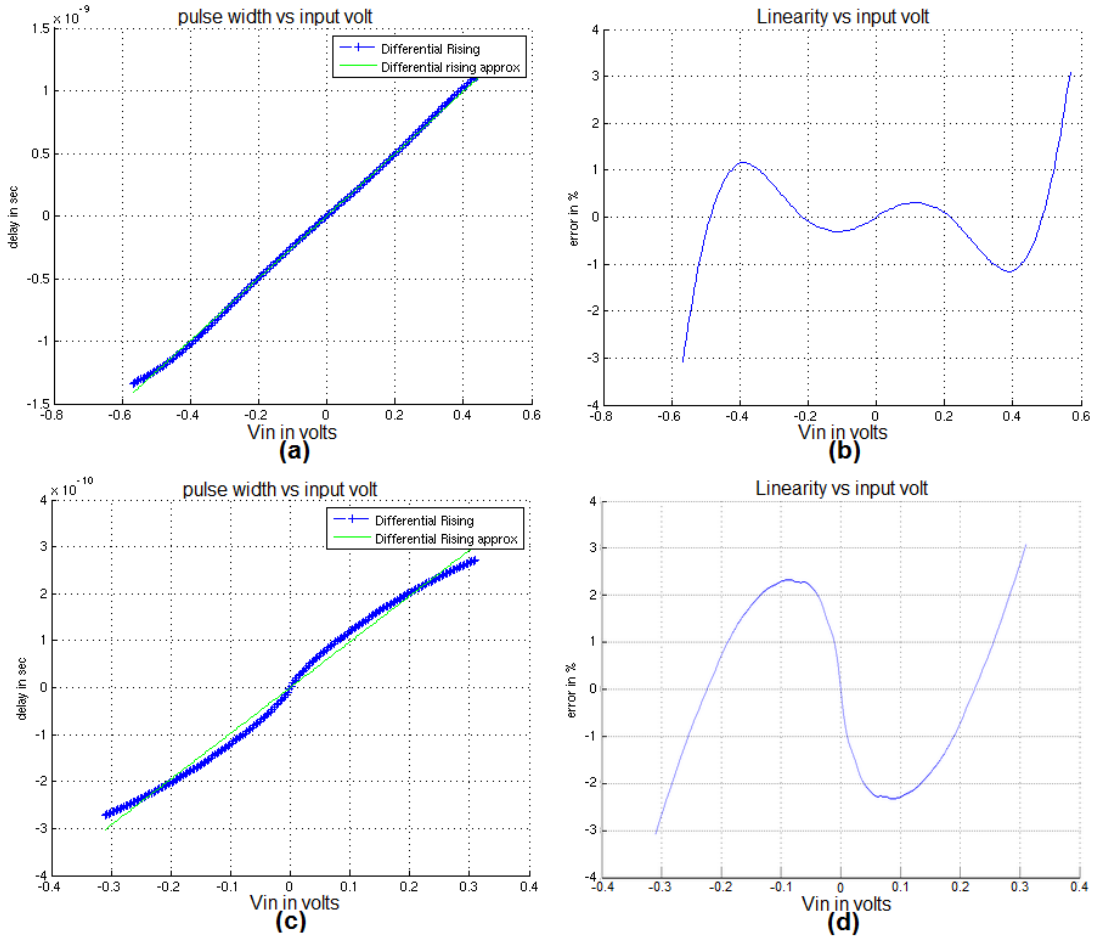


Figure 3.8: Differential rising VTC. (a) Linear range at F_S = 250 MS/s. (b) Linearity error check at F_S = 250 MS/s. (c) Linear range at $F_{S,MAX}$ = 0.7 GS/s. (d) Linearity error check at $F_{S,MAX}$ = 0.7 GS/s.

Figure 3.8(a), Figure 3.8(b) show the differential rising VTC design curve fitting of the input dynamic range and the check of the linearity error of at a 250 MS/s sampling frequency. Moreover, Figure 3.8(c), Figure 3.8(d) show also both of them at a 0.7 GS/s sampling frequency.

Table 3.3 compares at a 3% acceptable linearity error the specifications of the differential VTC design with the corresponding single-stage rising VTC design of [26]. The differential design has a higher dynamic range (DR), FOM_1, sampling frequency and sensitivity, while the single-ended design has lower area and power consumption.

3.4. Differential VTC methodology circuit

3.4.1. The differential VTC methodology design

The proposed differential architecture is modified as in Figure 3.9 where the clock of the second VTC core is inverted by a delay line. The single core of this differential design is a new design methodology which makes use of the falling circuit and the rising

circuit functionalities based on their complementary behavior in order to control both falling and rising output edges. This produces a higher dynamic input range than

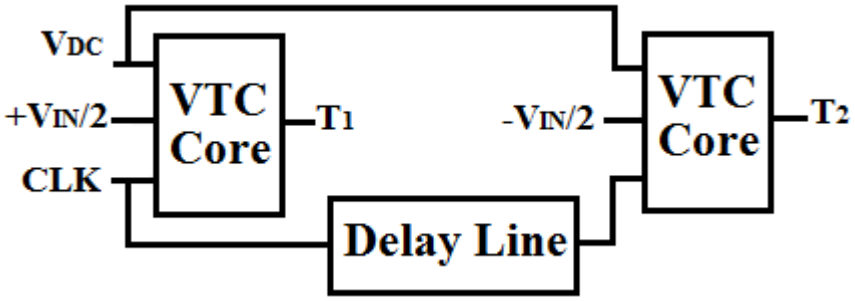


Figure 3.9: The differential methodology architecture.

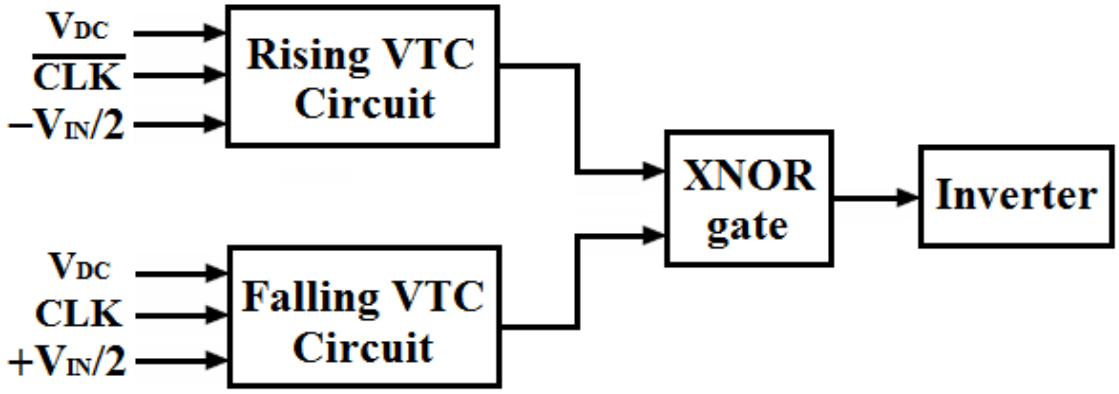


Figure 3.10: The VTC core of the differential methodology architecture.

designing each VTC circuit (the falling VTC circuit or the rising VTC circuit) separately. Hence, this design is considered a Pulse Width Modulation (PWM) VTC where the single VTC circuit core is shown in. Figure 3.10.

The pull-up block (the rising VTC circuit) has an inverted delayed clock using a delay line buffer based inverter as shown in Figure 3.9. An 11-cell inverter are used to define the buffer delay. This results in a high linear output as the output pulse equals to $\Delta + T_R - T_F$. Where Δ is the buffer delay which should be high to have a positive delay after subtracting the value of T_F so as to have a higher dynamic linear range; T_F is the fall delay of the pull-down block (falling VTC circuit) which equals to $\frac{V_{DD} \times C_L}{2 \times I_F}$; and T_R is the rise delay of the pull-up block which equals to $\frac{V_{DD} \times C_L}{2 \times I_R}$. Where V_{DD}, I_F and I_R are the supply voltage, the falling VTC output current and the rising VTC output current, respectively.

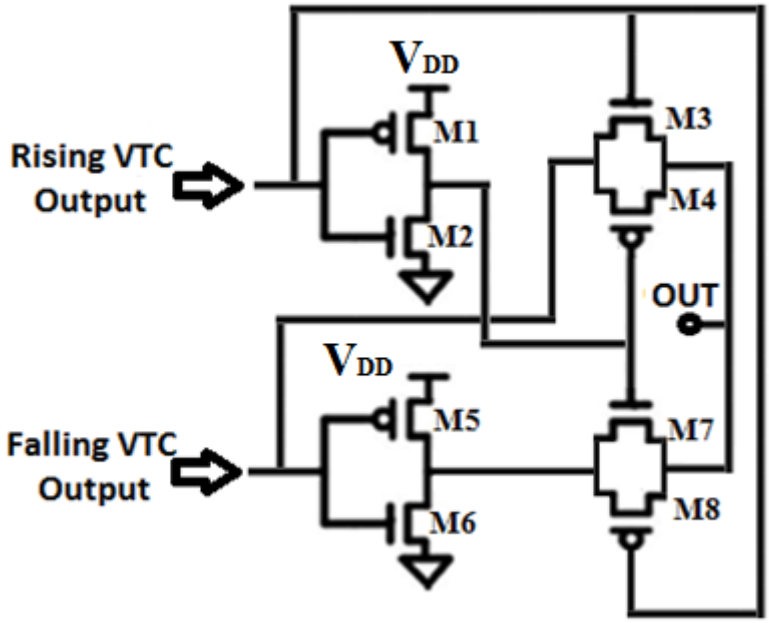


Figure 3.11: The XNOR circuit schematic.

The XNOR gate, as illustrated in Figure 3.11, is used to get the difference between the rise delay and the fall delay and to produce the PWM VTC output which is the input to the TDC block. Actually, the XNOR gate is the bottleneck of this design to operate on higher frequencies. It is designed to work on very narrow pulses such as pulses with 100 ps widths. This is implemented by enlarging transistors' sizes which results in overheads in area and power [23]. On the other hand, transmission gate transistors are used in the design of the XNOR gate so as to reduce the resulting overheads of the power and area. Consequently, the proposed design delay equation is expressed as the difference between the pulse-width delay of the 1st core output and the 2nd core output. An output inverter is used to sharpen and linearize the output.

3.4.2. **Simulation results**

The input voltage linear range of the differential VTC methodology circuit is from -500 mV to 500 mV (i.e. the dynamic range is 1000 mV). The circuit sensitivity is 3.4 ps/mV which is higher than the individual circuits (falling and rising VTC) due to the extra delay provided by this design. Area and the consumed power are: 310 µm^2 and 159 µW. The DC voltage is 600 mV, while the supply voltage is 1.2 V.

Simulations have been carried out using an operating clock frequency of 250 MS/s, while the maximum sampling frequency ($F_{S,MAX}$) that the circuit can achieve with keeping the linearity range high is 2.5 GS/s. At operating on the 2.5 GS/s $F_{S,MAX}$, the differential design has a dynamic range of 462 mV and a sensitivity of 3.2 ps/mV. The maximum power consumed at this high frequency is 358 µW.

The total output RMS noise voltage ($V_{N,RMS}$) of the differential design and the single-ended design at mid-frequencies is 3.5 nV/$\sqrt{Hz}$ and 2.4 nV/$\sqrt{Hz}$, respectively. The proposed design shows a higher RMS noise due to the differential mechanism which

has a larger number of the circuit transistors. In fact, the total RMS noise should be less than a single step conversion of the ADC as in equation (2.1). Consequently, $V_{N,RMS}$, at

Table 3.4: Performance comparison between the differential VTC methodology circuit and its single-ended design @ 3% linearity error.

Parameter	Differential VTC Methodology	Proposed design of [26]
$F_{S,MAX}$ (GS/s)	2.5	0.7
VTC Area (μm^2)	310	140
DR @$F_S/F_{S,MAX}$ (mV)	1000/462	550/550
Sensitivity (ps/mV)	3.4	2.1
P_D @$F_S/F_{S,MAX}$ (μW)	159/358	62/-
THD (dB) @$F_I/F_{I,MAX}$	-30/-33	-20/-
SNDR (dB) @F_I	66.3	48.9
ENOB (bits) @F_I	10.7	7.8
FOM_1 @$F_S/F_{S,MAX}$ ($\times 10^{12}$)	1.6/1.5	3.4/-
FOM_2 (fj/conversion)	0.04	-

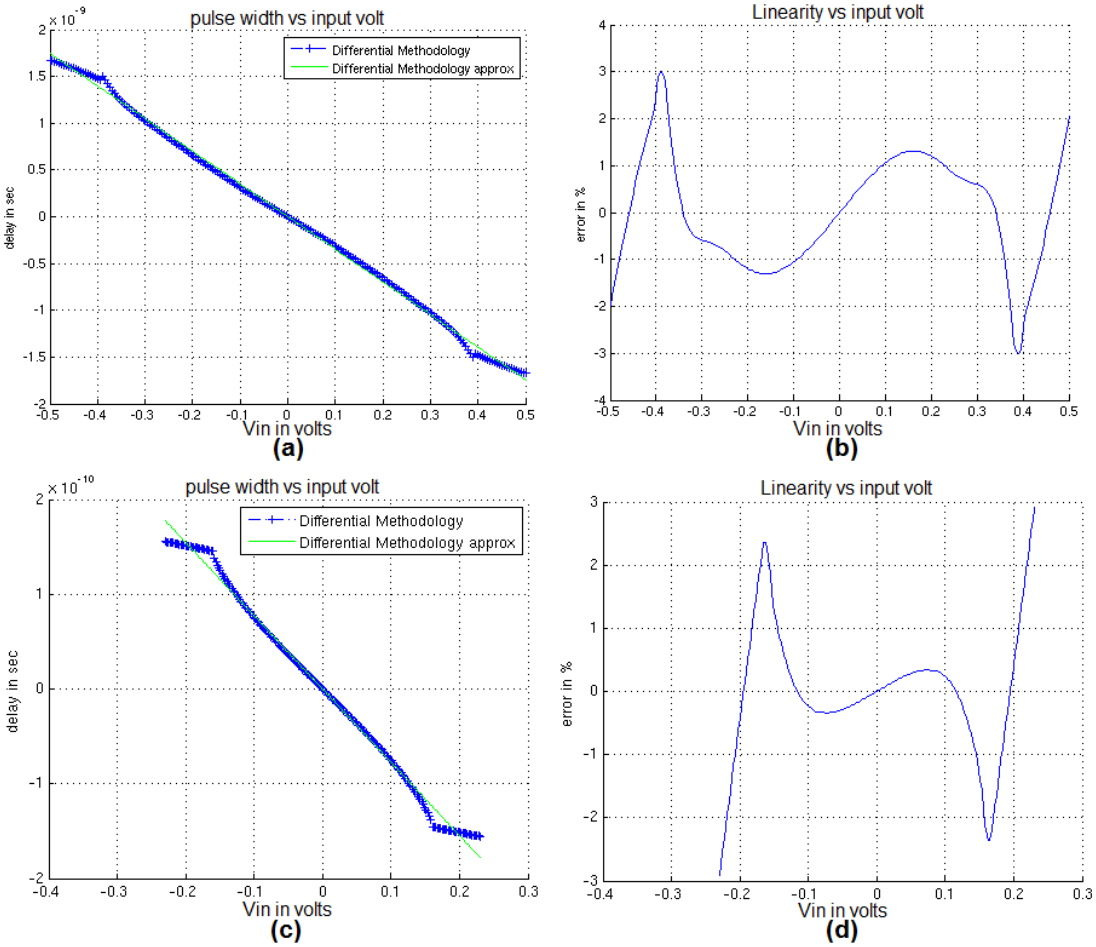


Figure 3.12: Differential VTC methodology. (a) Linear range at F_S = 250 MS/s. (b) Linearity error check at F_S = 250 MS/s. (c) Linear range at $F_{S,MAX}$ = 2.5 GS/s. (d) Linearity error check at $F_{S,MAX}$ = 2.5 GS/s.

a high sampling frequency such as 2.5 GS/s, equals to 0.17 mV. This implies the differential VTC methodology design to be capable of providing a 11-bit TADC (i.e. the ADC single step conversion equals to 0.29 mV) with a high value of the ENOB.

THD equals to -30 dB at a 100 MS/s F_I and a 250 MS/s F_S. The maximum THD which equals to -33 dB, is achieved at a 1 GS/s $F_{I,MAX}$ and a 2.5 GS/s F_S. FOM_1 equals to 1.6×10^{12} and 1.5×10^{12} in case of a sampling frequency of 250 MS/s and 2.5 GS/s, respectively. The effective-number-of-bits (ENOB), the signal-to-noise-and-distortion ratio (SNDR) and the second formula of the figure-of-merit (FOM_2) are measured for the differential methodology design at a 100 MS/s F_I and they equal to 66.3 dB, 10.7 bits and 0.04 *fj*/conversion.

Figure 3.12(a), Figure 3.12(b) show the differential VTC methodology design curve fitting of the input dynamic range and the check of the linearity error of at a 250 MS/s sampling frequency. Moreover, Figure 3.12(c), Figure 3.12(d) show also both of them at a 2.5 GS/s sampling frequency.

Table 3.4 compares at a 3% acceptable linearity error the specifications of the differential VTC design with the corresponding single-stage VTC design of [26]. The differential design has a higher dynamic range (DR), FOM_1, sampling frequency and sensitivity, while the single-ended design has lower area and power consumption.

Table 3.5 reveals, at a 3% acceptable linearity error, the design specifications of the differential VTC methodology circuit corresponding to various sampling frequencies with their configured clock rise and fall times. The design has a higher dynamic linear range and FOM_1, in additions to a lower consumed power at 60 MS/s F_S. On the other hand, the higher sampling frequencies has a lower FOM_1 due to the high consumed power.

Table 3.5: Performance comparison of the differential methodology while sweeping the sampling frequency with a 3% linearity error.

Clock Sampling Frequency (MS/s)	Clock rise and fall times (pS)	Dynamic Range (mV)	Input Linear Range (mV)	Power (µW)	FOM_1 ($\times10^{12}$)
60	167	1056	-528 : 528	30	2.2
100	100	1054	-527 : 527	80	1.4
250	40	1000	-500 : 500	159	1.6
1000	10	666	-333 : 333	258	1.7
2500	2	462	-231 : 231	358	1.5

3.5. Modified differential VTC methodology circuit

3.5.1. The 1st differential VTC proposed design

This design is a modified version from the previously mentioned design. It is considered the 1st proposed design by this thesis. The differential VTC methodology design is modified for the following reasons:

1. To make a good use from the methodology complementary behavior and have a further higher SNDR, ENOB and FOM_2.

2. To reduce the dependency on the process-voltage-temperature (PVT) variations that face all electronic circuits.

A design enhancement in the delay line block of Figure 3.9 could overcome the 1st issue so as to provide an extra dynamic range and ENOB. The reason is the delay line buffer is one of the main parameters that affects the methodology output equation ($\Delta + T_R - T_F$). The proposed design architecture, as portrayed in Figure 3.13, depends on a large-sized inverter to provide more linearized output.

A single buffer based-inverter is better than a delay line based-inverter due to several reasons: the series inverter branch produces weaker and less current capable channel; the delay line produces a highly output resistance and capacitance due to the wiring and fan-out effect; and a larger power consumption due to the dynamic power which comes from charging/discharging capacitances, the short circuit power due to delay-line transistors switching and the leakage power due to current flow when transistors are off. This could produces a not fully-amplitude inverted clock to the rising VTC circuit (pull-up block of Figure 3.10).

To overcome the 2nd main issue, 2 more enhancements are presented. The 1st enhancement is to embed a metal-insulator-metal (MIM) capacitor instead of a MOSFET capacitor to the output nodes V_F and V_R of Figure 3.4 and Figure 3.7, respectively. The MIM capacitor includes 2 higher metal layers (i.e Metal 7 and Metal 8) to provide higher

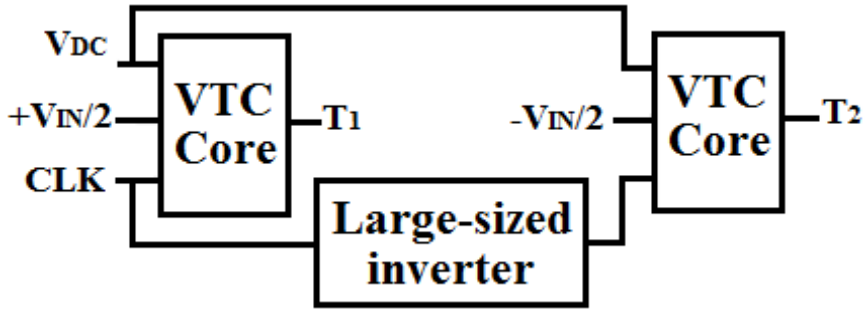


Figure 3.13: The proposed modified differential methodology architecture.

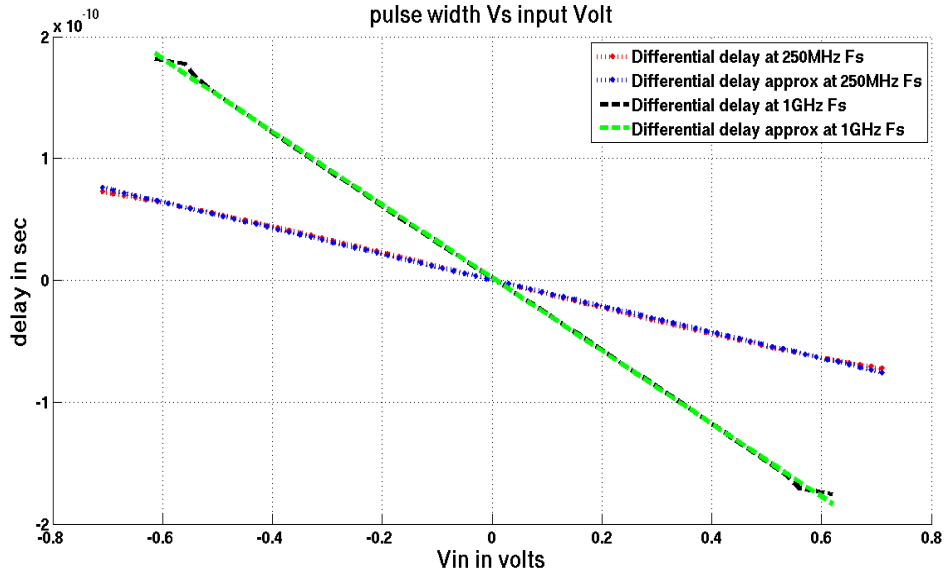
density and linearity and smaller parasitic capacitances. Generally, it mostly minimizes the PVT variations that happen in the drain-source voltage (V_{DS}) of a basic MOSFET capacitor especially at high frequencies. The main disadvantage of the MIMCAP is that it consumes a larger area as the field-oxide insulator is thicker than the gate-oxide of the MOSFET capacitor [27], [28].

The 2nd enhancement is to design a calibration circuit which compensates all effect of the PVT variations towards the VTC design specifications. The PVT variations effect reveal at the design dynamic range, where they produce some imperfections at the dynamic linear range illustrated with 3 % linearity error at typical conditions ((typical speed nMOS corner - typical speed pMOS corner, 27 ^{O}C temperature and a 1.2 V nominal

supply voltage). Moreover, the design DC bias offset is shifted and makes the proposed design produce not the best design specifications [29]. As a result, the ENOB is a variable for each corner, temperature and supply voltage changes. The calibration circuit is discussed in-detail at Section 3.5.3.

3.5.2. **Simulation results**

The proposed design is optimized, in order to achieve a high linearity design. Also, A MATLAB algorithm has been developed to automatically tune all possible TDC delays



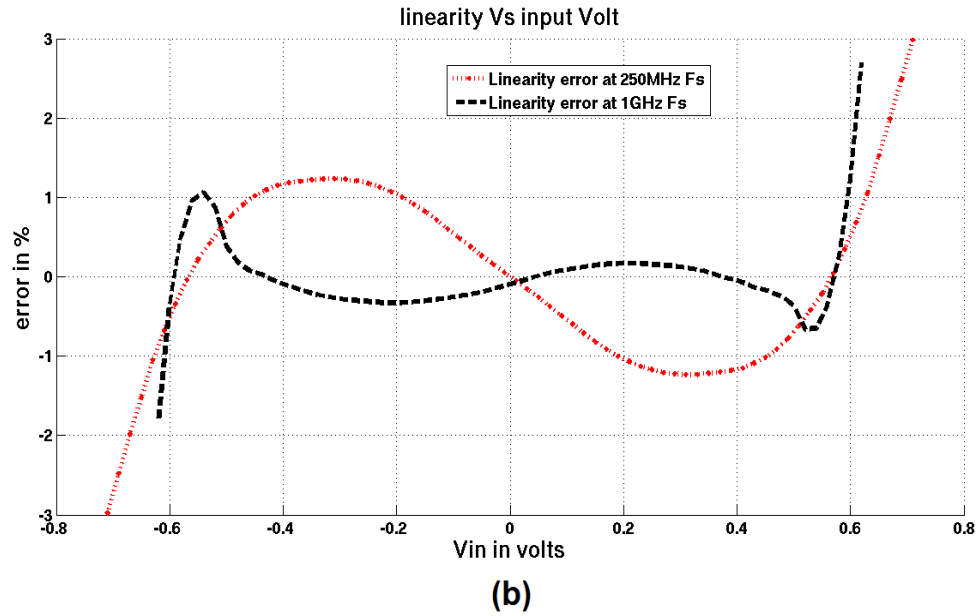


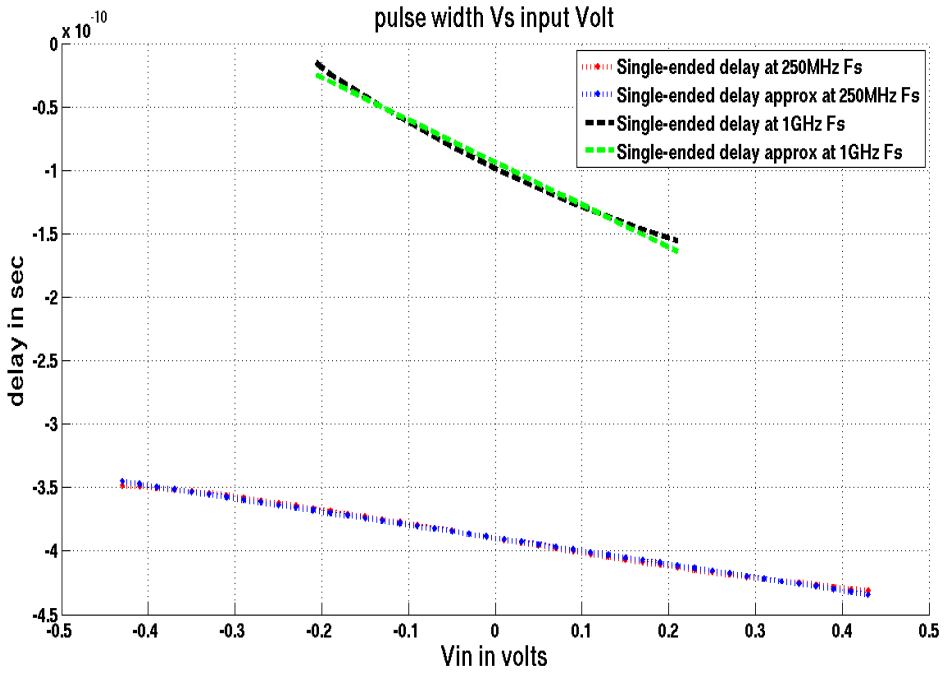
Figure 3.14: The modified differential VTC methodology design. (a) Dynamic linear range (b) Linearity error check.

for optimum dynamic range and ENOB results. The supply voltage and the operating clock frequency with a 50% duty cycle are 1.2 V and 250 MS/s, respectively. Optimal bias conditions have been selected using a design optimization technique by which the largest linear range is achieved. The applied DC input voltage is 750 mV.

Figure 3.14(a) and Figure 3.15(b) show the dynamic linear range of the proposed VTC design and the single-ended VTC core, respectively, at a sampling frequency (F_S) of 250 MS/s and 1 GS/s. The proposed design linear range which has a range of -0.71 V: 0.71 V is nearly a double of the linear range of the single ended design which has a range of -0.43 V: 0.43 V. Moreover, Figure 3.14(b) and Figure 3.15(b) reveal the linearity error check of both designs at 250 MS/s and 1 GS/s, respectively, to make sure that the nonlinearity error is within an acceptable error. The decreased linear range due to a 1 GS/s F_S is illustrated in Figure 14(a) and Figure 15(a). At low sampling frequencies (such as 10 MS/s), the consumed power of the proposed design reaches 9.2 µW, while the consumed power of the single ended design is 5.7 µW.

The linearity slope represents the circuit sensitivity which equals to 0.1 ps/mV and 0.09 ps/mV for the proposed design and the single-ended design, respectively. Although higher sensitivity is preferred for a TDC block to be able to sense the delay changes over the linear range, the higher resulting delay affects the ADC conversion speed and stability. The proposed design is able to tolerate this sensitivity with the help of its high linear range in order to make the TDC block sense the voltage changes perfectly.

In case of F_S of 250 MS/s and 1 GS/s, the input fundamental frequency (F_{IN}) is chosen to equal to 100 MS/s and 400 MS/s, respectively, in order to achieve the Nyquist conditions criteria for the ADC [5]. The proposed design presents an improved linearity due to the differential mechanism with a THD of -31.1 dB and -37 dB, respectively, while the single-ended design presents a THD of -25.3 and -31.1 dB, respectively.



(a)

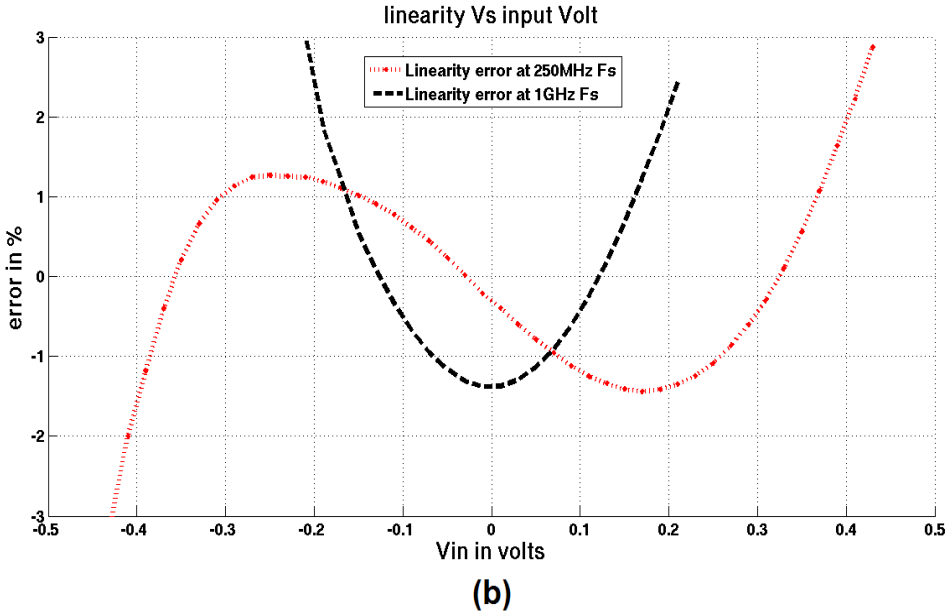


Figure 3.15: The single-ended VTC core. (a) Dynamic linear range (b) Linearity error check.

The $V_{N,RMS}$ of the differential design and the single-ended design at mid-frequencies is the same as in Section 3.4.2 as the delay line design is not the main noise contribution of the whole circuit. $V_{N,RMS}$ equals to 5.5×10^{-5} V which could make the proposed design to be integrated with a 14-bit TADC.

The proposed design presents a higher ENOB of 12.8 bits and 11.3 bits at 250 MS/s and 1 GS/s F_S, respectively, while the single-ended design presents an ENOB of 9.8 bits and 5.7 bits for a F_S of 250 MS/s and 1 GS/s, respectively. This is due to the higher linearity provided by the proposed design.

Table 3.6: Performance comparison between the modified differential VTC methodology circuit and its single-ended design @ 3% linearity error.

Parameter	The 1st proposed VTC design	Single-ended VTC design
F_S/ $F_{S,MAX}$ (GS/s)	0.25/ 1	0.25/ 1
F_{IN} @ F_S/ $F_{S,MAX}$ (GS/s)	0.1/ 0.4	0.1/ 0.4
DR @ F_S/ $F_{S,MAX}$ (V)	1.42/ 1.25	0.86/ 0.42
Sensitivity (*p*s/mV)	0.1	0.09
P_D @ F_S/ $F_{S,MAX}$ (*m*W)	0.25/ 0.48	0.12/ 0.24
FOM_1 @ F_S/ $F_{S,MAX}$ ($\times 10^{12}$)	2.1/ 3.3	1.5/ 0.74
FOM_2 @ F_S/ $F_{S,MAX}$ (*f*J/conv.)	0.07/ 0.4	0.27/ 9.2
THD @ F_S/ $F_{S,MAX}$ (dB)	-31.1/ -37	-25.3/ -31.1
$V_{N,RMS}$ (nV/$\sqrt{Hz}$)	3.5	2.4
ENOB @ F_S/ $F_{S,MAX}$ (bits)	12.8/ 11.3	9.8/ 5.7
SNDR @ F_S/ $F_{S,MAX}$ (dB)	78.8/ 69.8	60.8/ 36.1
Area (μm^2) without MIMCAP	3	1.6

Table 3.6 compares all specifications, at a 3 % acceptable error, of the proposed VTC design and the corresponding single-ended VTC design. The proposed design shows a better dynamic range, sensitivity, FOM, ENOB and SNDR values than the single-ended design due to differential mechanism. In contrast, it consumes a higher area and power and exhibits a larger noise as well.

3.5.3. PVT variations calibration

The proposed calibration circuits of [29]–[34] illustrate various implementations to cancel the DC offset variations. These implementations consume much larger power and area. In this section, the PVT variations are tolerated by varying the input DC bias voltage (it is the V_{CONST} of Na1 and Pb3 shown in Figure 3.4 and Figure 3.7, respectively) which has been produced by a simple architecture of low-power large-sized capacitor-based voltage divider circuits.

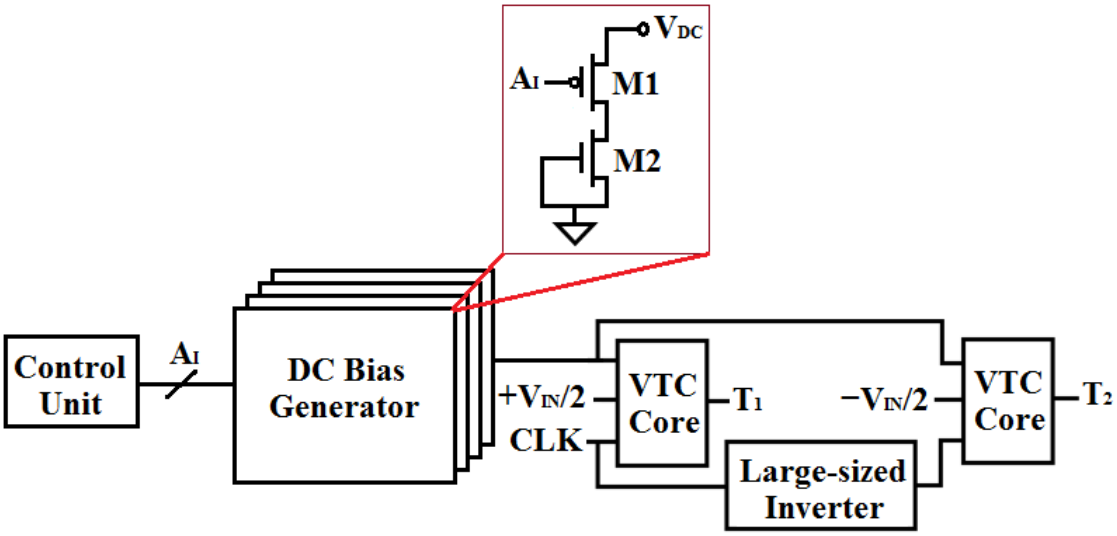


Figure 3.16: The calibration circuit integrated with the proposed design.

Figure 3.16 shows the basic architecture of the calibration circuit. A set of these calibration circuits is maintained to calibrate various combinations of each process, voltage and temperature change. To calibrate a specific variation, selection lines should be fed with the supply voltage to M1 transistor. These selection lines (A_I) are provided from a control unit. M2 acts as a capacitor (MOSFET capacitor). Once a specific circuit is selected by A_I, the current flowing through M2 is set due to charging the capacitor. The overall area of the set of these calibration circuits equals to 3.4457 μm^2, while the maximum power consumed equals to 0.3 nW. This is considered smaller area and power compared to calibration circuits designs in [29]-[34]. The transistors sizes of each circuit of the set is optimized for each variation to be cancelled in order to increase the dynamic range and the ENOB to reach relatively their values in the TT state. As the circuit could also be affected by the PVT variation, the transistors sizes are maintained at the same conditions of variations that the circuit operates on.

3.5.3.1. Process variations

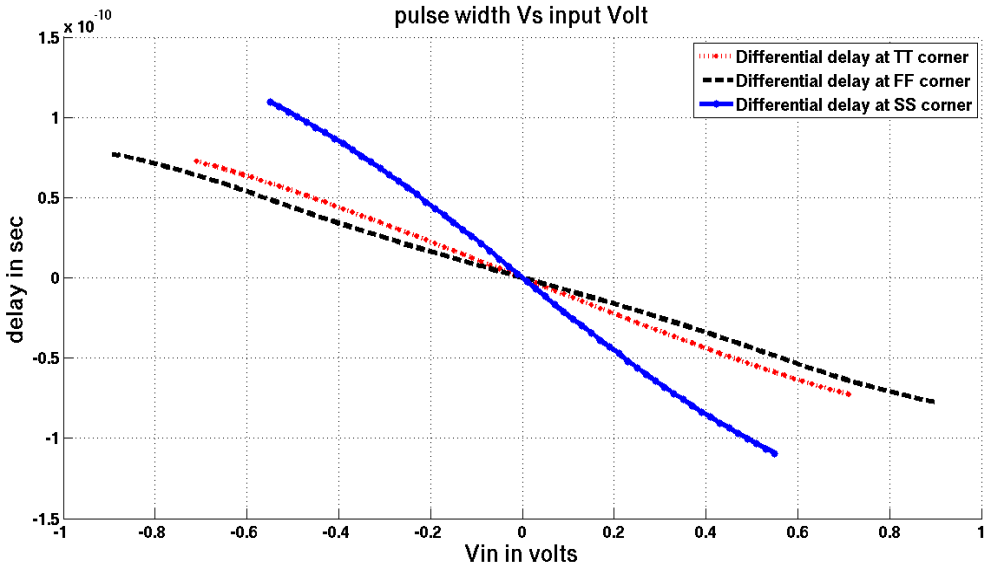
Due to CMOS technology scaling, process variations are expected to worsen in future technologies. They are classified as die-to-die (global) and within-die (local) variations. They affect device parameters, resulting in fluctuations which change the dynamic range. The impact of the global variations is typically evaluated by corner simulations [35].

The process variations main sources [36], [37] at the 65nm CMOS technology, that affect the device parameters, are: (1) random dopants which are decreased in the MOSFET depletion region and results in variations of device threshold voltage (V_{TH}) which is proportional inversely to the square root of the transistor active area; and (2) channel length which impacts exponentially the V_{TH} due to the drain-induced barrier lowering (DIBL) effect in short channel devices. These lead to variations on V_{TH} or gate capacitance from the analog prospective and on gate delays or leakage currents from digital prospective.

3.5.3.1.1. Before calibration

Process corners (SS corner which represents slow-speed nMOS and pMOS and FF corner which represents fast-speed nMOS and pMOS) have been simulated and compared to the typical-speed nMOS and pMOS (TT) corner. They represent the worst case process variations than the other process corners (FS and SF corners) [38]. Figure 3.17(a) and Figure 3.18(a) show the effect of process variations on the dynamic range with 3% error of the proposed design and the single-ended design, respectively. While, Figure 3.17(b) and Figure 3.18(b) show the linearity error check for both designs, respectively.

The proposed design shows that the FF corner achieves a 1.8 V dynamic range with an error of 2.3%. On the other hand, due to the high linearity errors that face the single-



(a)

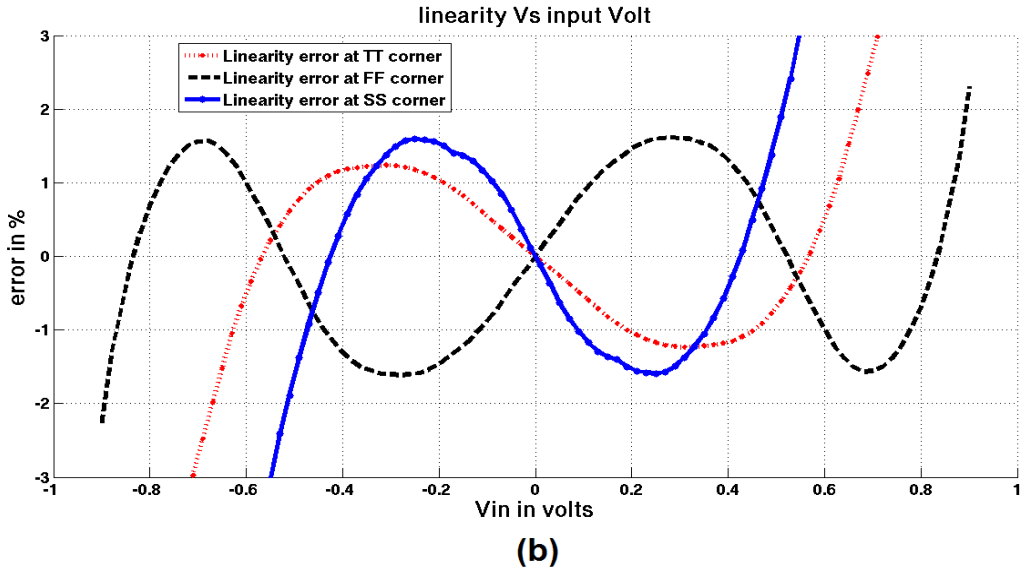
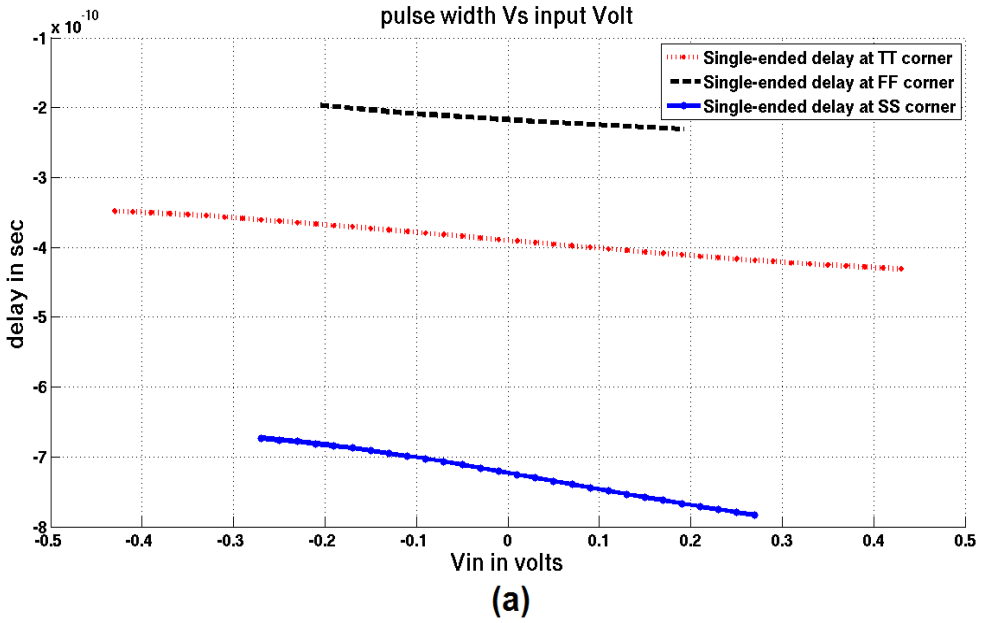


Figure 3.17: The proposed differential VTC before calibration at worst-case corners variations. (a) Dynamic linear range (b) Linearity error check.

ended design, operating on FF corner has a less dynamic range than the SS corner. Table 3.7 shows all specifications at different corners for both designs, where the worst case ENOB before calibration of the proposed design is 9.9 bits at the SS corner.

Table 3.7: Performance comparison before calibration between the proposed design and the single-ended design at different corners.

Parameter	This work			The single-ended design		
	TT	SS	FF	TT	SS	FF
Dynamic Range (V)	1.42	1.1	1.8	0.86	0.54	0.42
DC Voltage (V)	0.75	0.75	0.75	0.77	0.77	0.77
Sensitivity (ps/mV)	0.1	0.2	0.09	0.09	0.2	0.08
Linearity Error (%)	3	3	2.3	3	3	3
P_D (mW)	0.25	0.22	0.27	0.12	0.11	0.13
$V_{N,RMS}$ (nV/$\sqrt{Hz}$)	3.5	3.6	3.3	2.4	2.6	2.3
SNDR (dB)	78.8	61.4	84.2	60.8	46.3	60.4
ENOB (bits)	12.8	9.9	13.7	9.8	7.4	5.7
FOM_1 ($\times 10^{12}$)	2.1	1.4	3	1.5	0.7	0.3
FOM_2 (fJ/conv.)	0.07	0.46	0.04	0.27	1.3	5



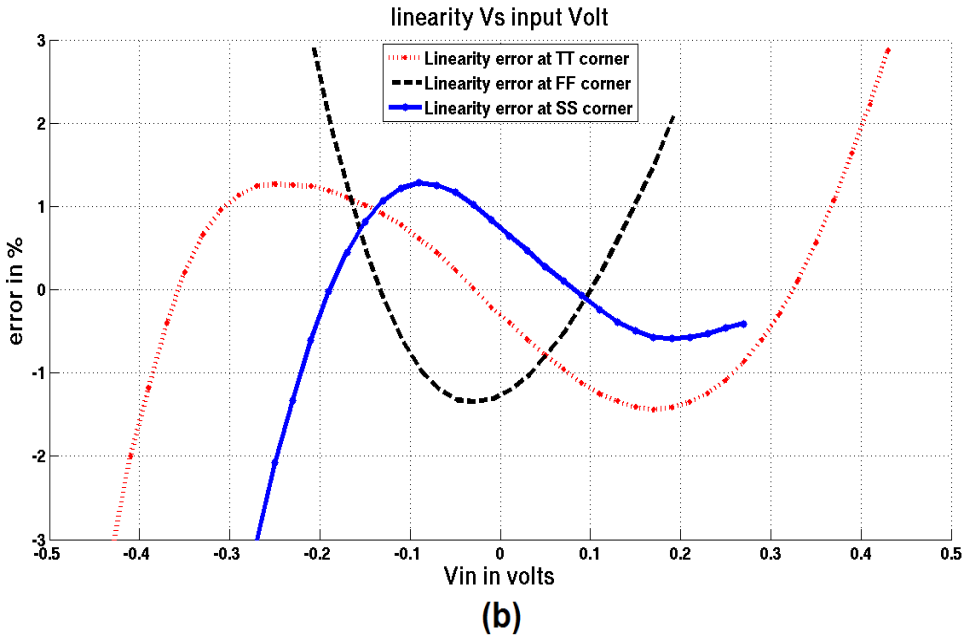


Figure 3.18: The single-ended VTC core before calibration at worst-case corners variations. (a) Dynamic linear range (b) Linearity error check.

3.5.3.1.2. After calibration

By adjusting the DC voltage of each corner case with keeping the linearity error being at 3 %, the proposed design performance of different corners is enhanced. Figure 3.19(a), Figure 3.19(b), Figure 3.20(a) and Figure 3.20(b) illustrate these enhancements on the dynamic range and the corresponding linearity error check for both designs, respectively. Consequently, the proposed design SS corner by more than

60 %, the single-ended design operated on the worst case FF corner is improved by only 15 %. This emphasizes that the single-ended design needs other calibration techniques as discussed in [6]. Table 3.8 shows the calibration effect on all designs specifications. The calibration circuit consumes a 0.125 nW, 0.31 nW and 0.13 nW at TT, SS and FF corners, respectively. While the proposed design itself consumes 0.25 nW, 0.22 nW and 0.27 nW at TT, SS and FF corners, respectively.

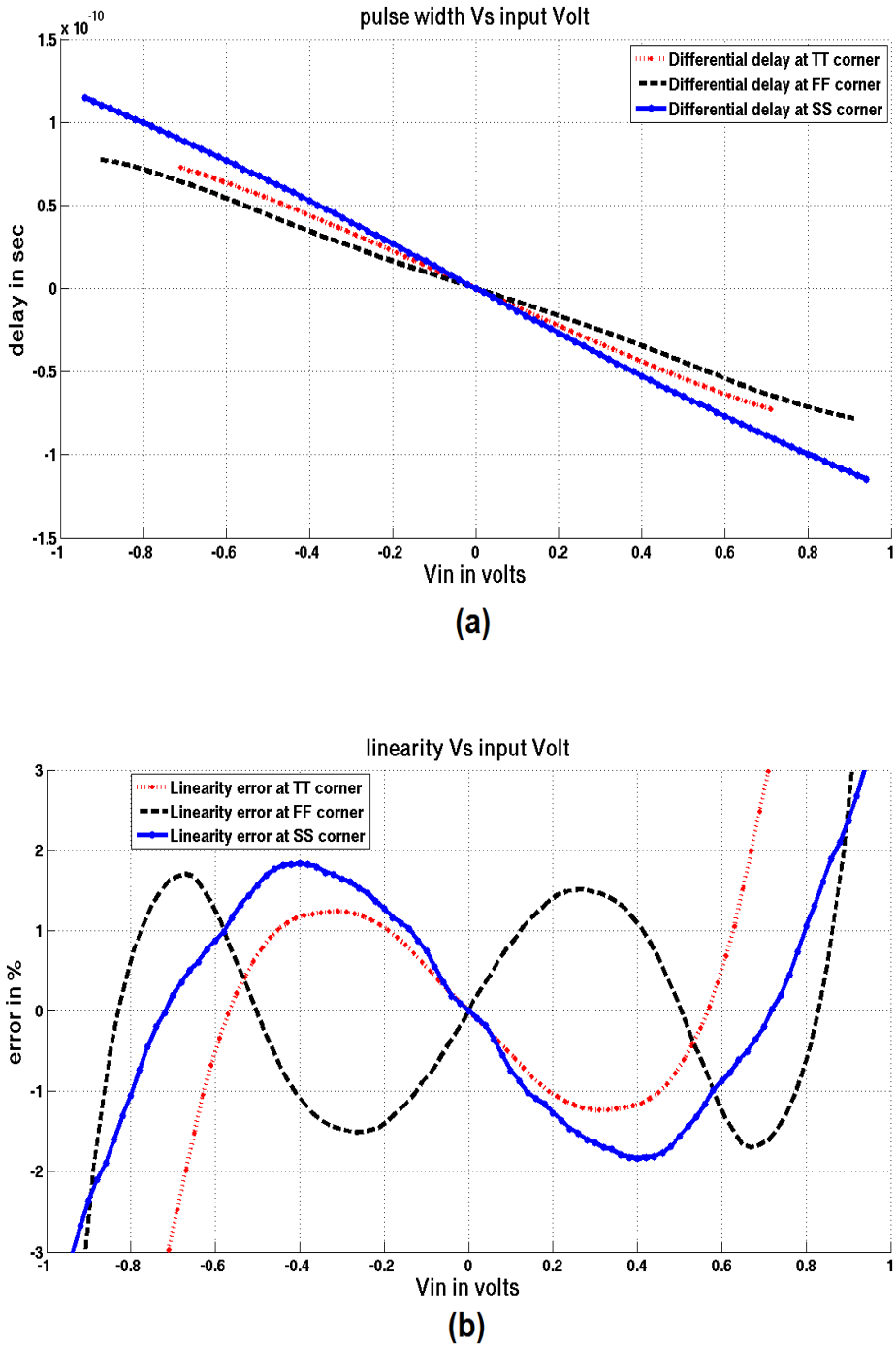
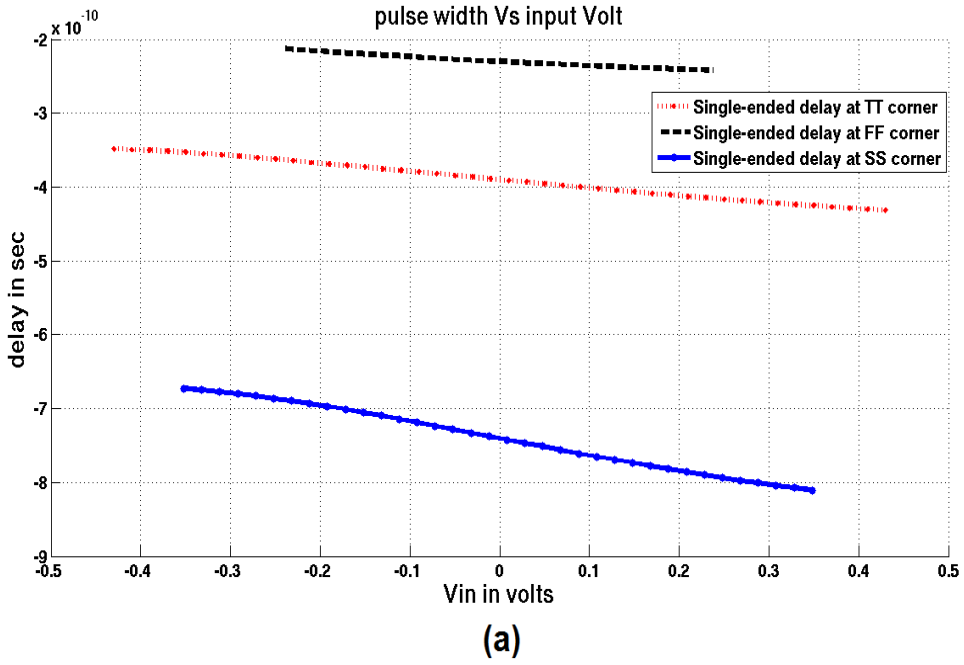


Figure 3.19: The proposed differential VTC after calibration at worst-case corners variations. (a) Dynamic linear range (b) Linearity error check.

Table 3.8: Performance comparison after calibration between the proposed design and the single-ended design at different corners.

Parameter	This work with the calibration circuit			The single-ended design		
	TT	**SS**	**FF**	**TT**	**SS**	**FF**
Dynamic Range (V)	1.42	1.88	1.82	0.86	0.7	0.48
DC Voltage (V)	0.75	0.55	0.74	0.77	0.85	0.95
Sensitivity (ps/mV)	0.1	0.12	0.09	0.09	0.2	0.06
Linearity Error (%)	3	3	3	3	3	3
P_D (mW)	0.375	0.53	0.4	0.12	0.11	0.13
$V_{N,RMS}$ ($n\text{V}/\sqrt{Hz}$)	3.5	3.6	3.3	2.4	2.6	2.3
SNDR (dB)	78.8	84.2	84.2	60.8	56	41.5
ENOB (bits)	12.8	13.7	13.7	9.8	9	6.6
FOM_1 ($\times 10^{12}$)	2.1	4	3.1	1.5	1.1	0.4
FOM_2 (fJ/conv.)	0.07	0.46	0.04	0.27	0.43	2.7



(a)

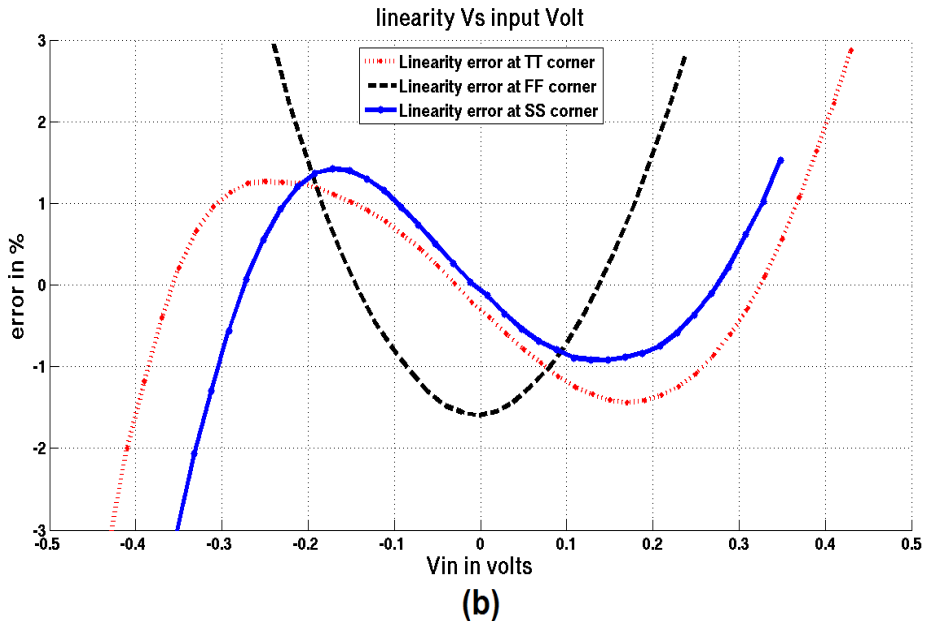


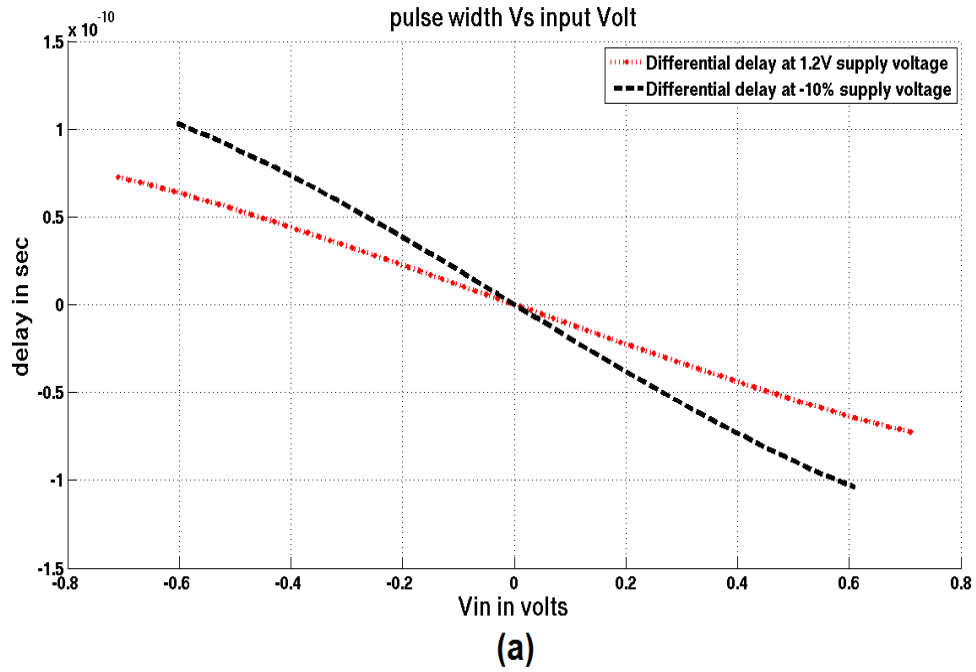
Figure 3.20: The single-ended VTC core after calibration at worst-case corners variations. (a) Dynamic linear range (b) Linearity error check.

3.5.3.2. Voltage variations

Supply voltage fluctuations are mainly caused by the current flow over the parasitic capacitance and resistance of the power grid. These variations change the current flowing through the circuit transistors resulting in a change of the transistors operation mode. Consequently, dynamic range is deviated from the nominal one. Voltage variations are minimized by using a voltage regulator or a band-gap circuit which also face a deviation in the original nominal supply voltage [35].

3.5.3.2.1. Before calibration

The proposed design and the single-ended design performances are simulated at a supply voltage of 1.2 V, 1.1 V and 1.3 V, respectively. Figure 3.21(a), Figure 3.21(b), Figure 3.22(a) and Figure 3.22(b) demonstrate the dynamic range and the corresponding linearity error check for both designs, respectively. At 1.3 V supply voltage, the overdrive voltage of Na2 and Pb2 are increased due to the limitation of the parallel MOSFETs Na1 and Pb3. This means that the V_{TH} is increased enough to make the device operate on the off-mode. Consequently, dynamic range with a 3 % error is not obtained at this supply voltage for both designs [39]. On the other hand, at 1.1 V supply voltage, the impacted device has a lower V_{TH} that makes the device not to operate on the off-mode based on V_{IN}. Table 3.9 represents the supply voltage variations effect on all designs specifications.



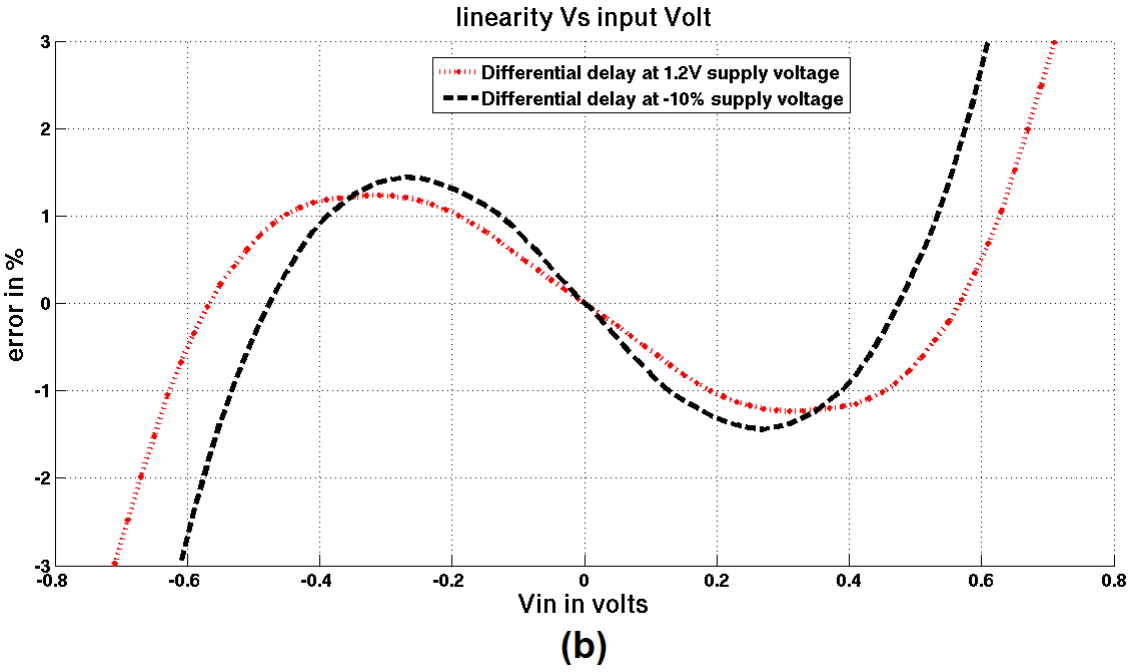
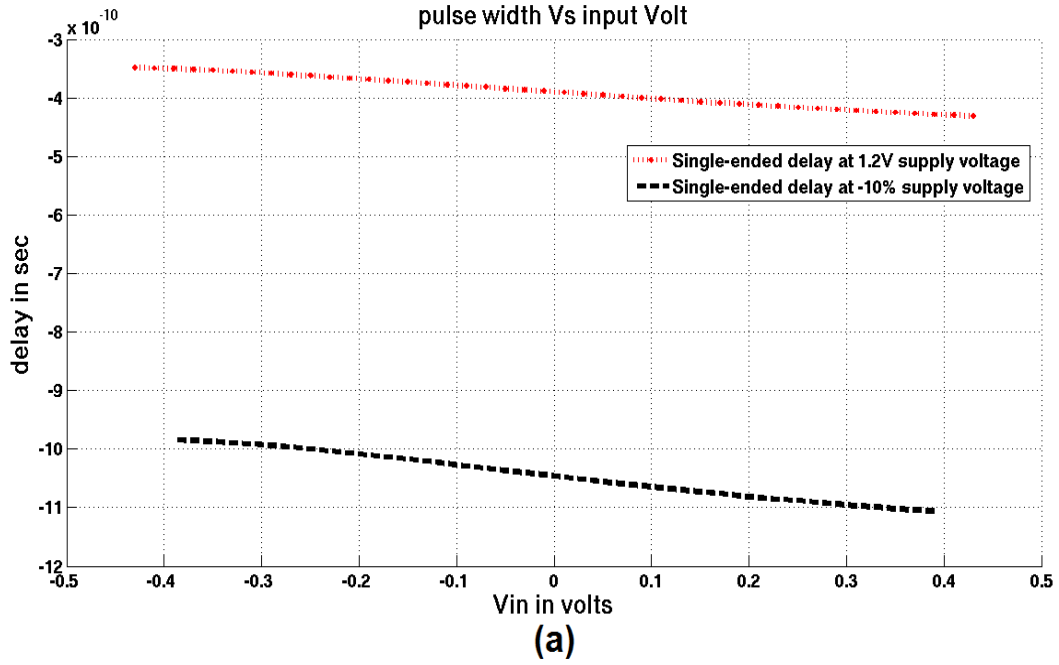


Figure 3.21: The proposed differential VTC before calibration at voltage variations. (a) Dynamic linear range (b) Linearity error check.

Table 3.9: Performance comparison before calibration between the proposed design and the single-ended design at supply voltage variations.

Parameter	This work			The single-ended design		
	-10%	**1.2V**	**+10%**	**-10%**	**1.2V**	**+10%**
Dynamic Range (V)	1.22	1.42	-	0.78	0.86	-
DC Voltage (V)	0.75	0.75	0.75	0.77	0.77	0.77
Sensitivity (ps/mV)	0.2	0.1	-	0.16	0.09	-
Linearity Error (%)	3	3	-	3	3	-
P_D (mW)	0.21	0.25	0.28	0.1	0.12	0.14
$V_{N,RMS}$ ($nV/\sqrt{Hz}$)	4.4	3.5	3.3	3.2	2.4	2.39
SNDR (dB)	71	78.8	-	56.5	60.8	
ENOB (bits)	11.5	12.8	-	9.1	9.8	-
FOM_1 ($\times 10^{12}$)	1.8	2.1	-	1.4	1.5	-
FOM_2 (fJ/conv.)	0.15	0.07	-	0.36	0.27	-



(a)

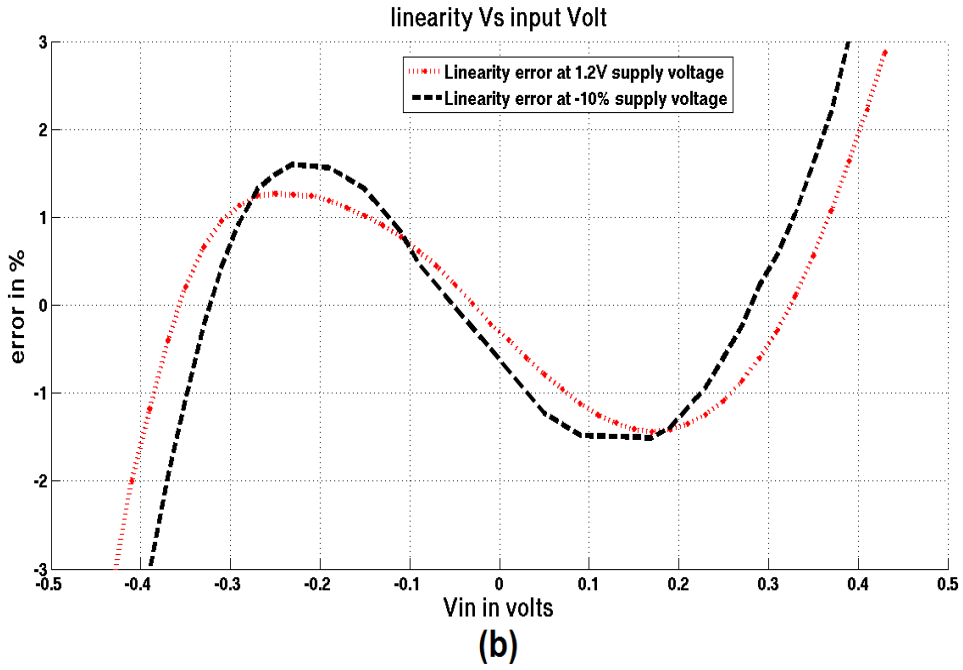
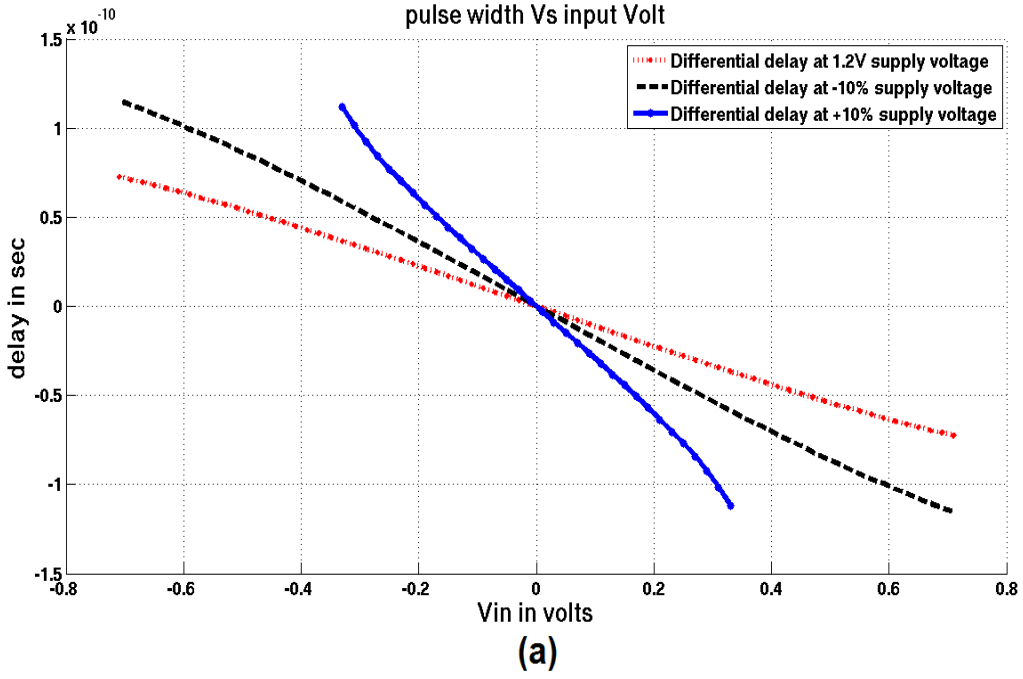


Figure 3.22: The single-ended VTC core before calibration at voltage variations. (a) Dynamic linear range (b) Linearity error check

3.5.3.2.2. After calibration

Adjusting the DC voltage of Na2 and Pb2 or Na1 and Pb3 is the practical solution instead of changing the circuit transistors size. Enhancements of the dynamic range and the linearity error for both designs are shown in Figure 3.23(a), Figure 3.23(b), Figure 3.24(a) and Figure 3.24(b), respectively. Although the dynamic range at 1.3 V supply



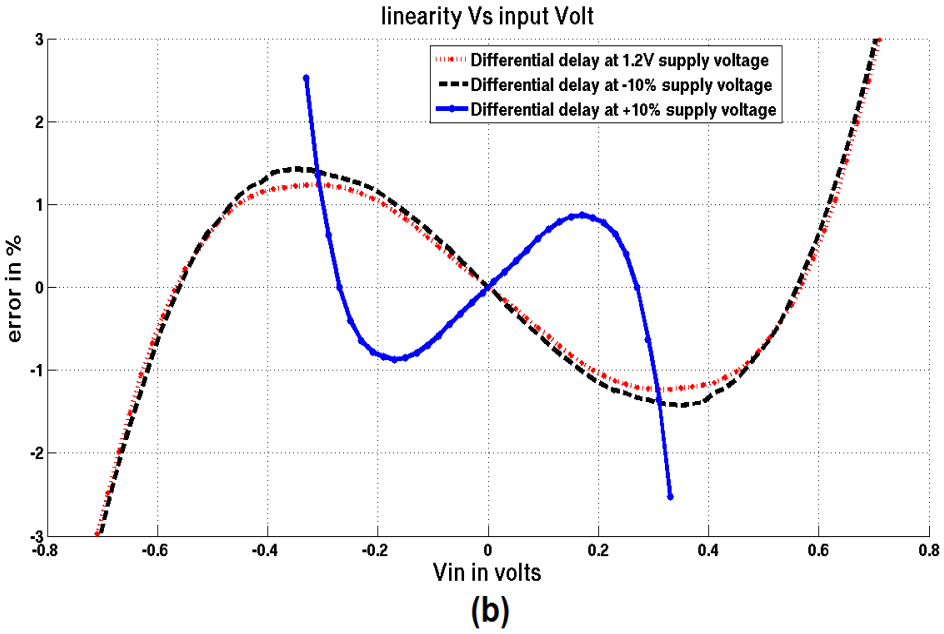
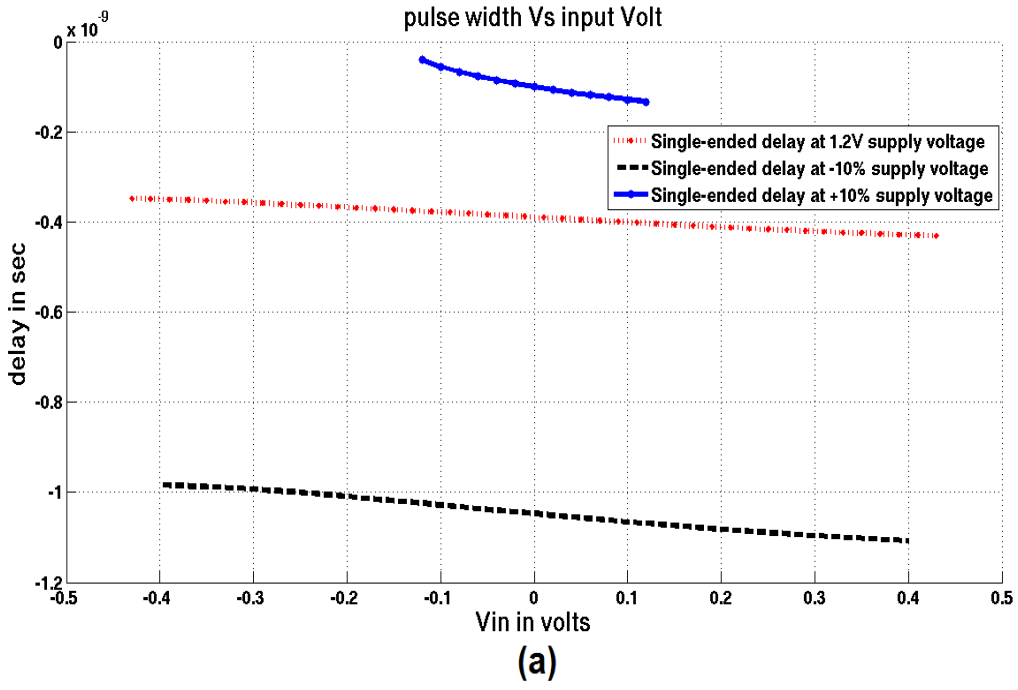


Figure 3.23: The proposed differential VTC after calibration at voltage variations. (a) Dynamic linear range (b) Linearity error check.

voltage is achieved after calibration with an enhancement of 100 %, it only gives an ENOB of 8.5 bits. As a result, other calibration techniques are needed to raise it up. Table 3.10 represents all designs specifications under calibrated supply voltage variations. The calibration circuit consumes a 0.125 nW, 0.17 nW and 0.18 nW at 1.2 V, 1.1 V and 1.3 V, respectively. While the proposed design consumes 0.25 nW, 0.21 nW and 0.3 nW at 1.2 V, 1.1 V and 1.3 V, respectively.



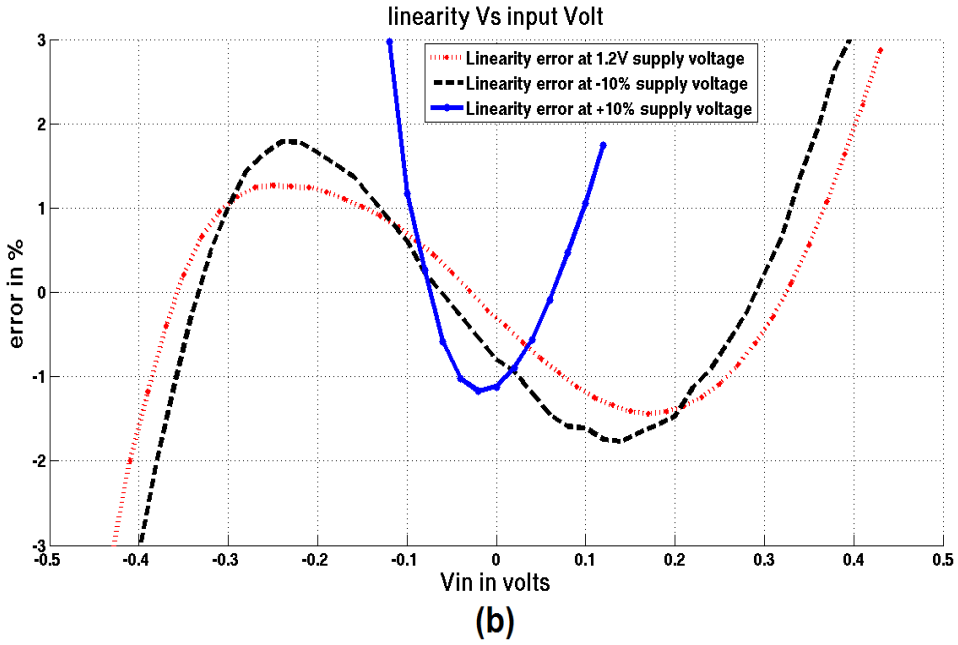


Figure 3.24: The single-ended VTC core after calibration at voltage variations. (a) Dynamic linear range (b) Linearity error check.

Table 3.10: Performance comparison after calibration between the proposed design and the single-ended design at supply voltage variations.

Parameter	This work with the calibration circuit			The single-ended design		
	-10%	1.2V	+10%	-10%	1.2V	+10%
Dynamic Range (V)	1.4	1.42	0.66	0.8	0.86	0.24
DC Voltage (V)	0.85	0.75	1.03	0.78	0.77	1
Sensitivity (ps/mV)	0.16	0.1	0.3	0.16	0.09	0.38
Linearity Error (%)	2.9	3	3	3	3	3
P_D (mW)	0.38	0.375	0.48	0.1	0.12	0.15
$V_{N,RMS}$ ($nV/\sqrt{Hz}$)	4.5	3.5	3.3	3.2	2.4	2.39
SNDR (dB)	71	78.8	53	59	60.8	31.6
ENOB (bits)	12.7	12.8	8.5	9.5	9.8	4.9
FOM_1 ($\times 10^{12}$)	2.3	2.1	0.4	1.6	1.5	0.1
FOM_2 (fJ/conv.)	0.06	0.07	1.66	0.26	0.27	10

3.5.3.3. Temperature variations

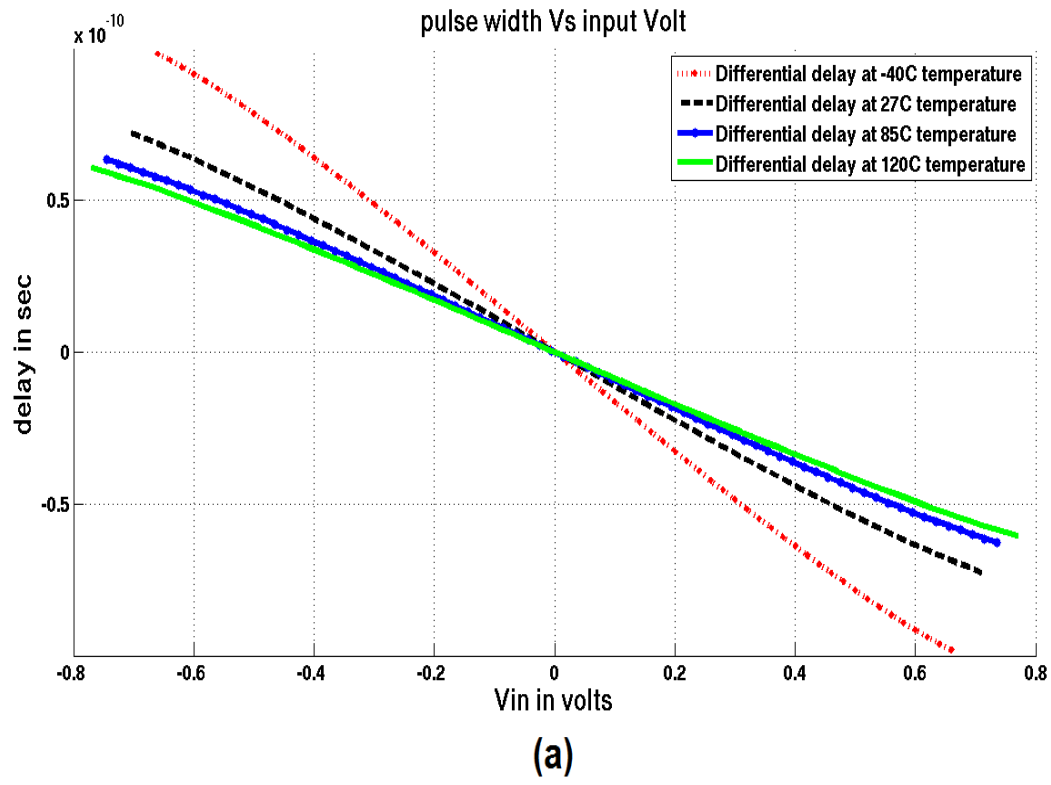
Environmental temperature fluctuations is responsible of major variations in die temperature. They have a direct effect to the flowing drain current that changes each MOSFET characteristics (i.e. V_{TH}, carrier mobility and saturation velocity) and the nominal supply voltage as well. In fact, mobility variations are the dominant factor than the nominal supply voltage variations due to the temperature fluctuations. As a result, the circuit characteristics including linearity are changed [40].

3.5.3.3.1. Before calibration

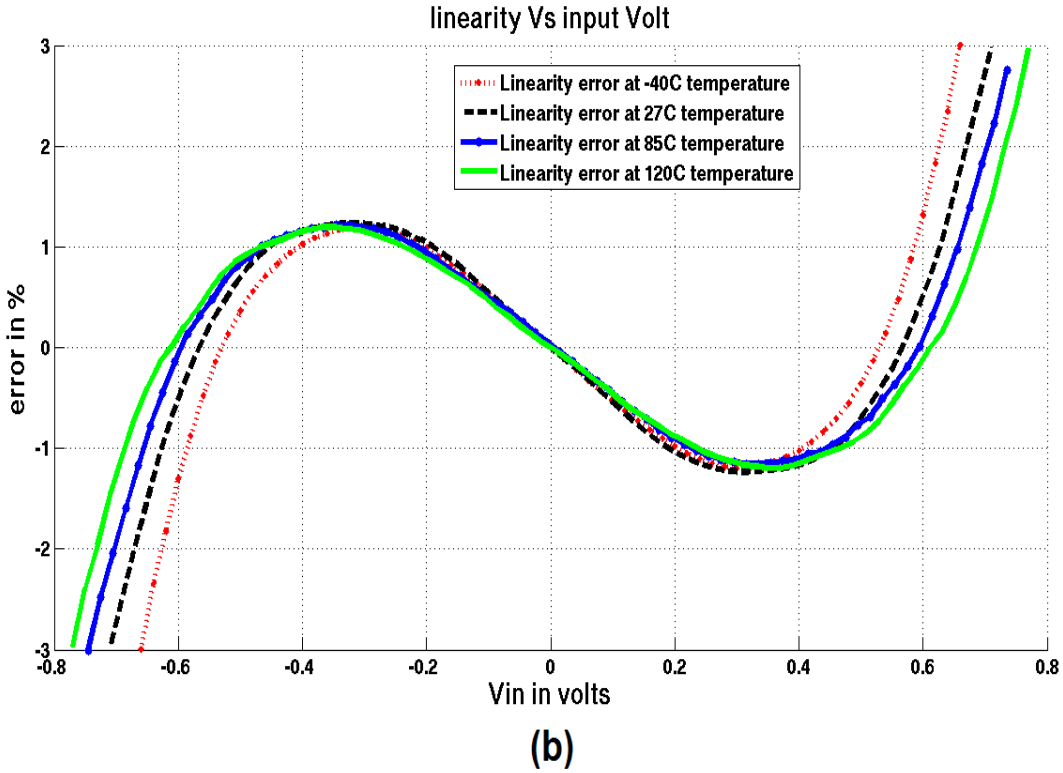
Figure 3.25(a), Figure 3.25(b), Figure 3.26(a) and Figure 3.26(b) show the dynamic range and the corresponding linearity error check for both designs at temperatures of -40 ^{O}C, 27 ^{O}C (the typical operating temperature), 85 ^{O}C and 120 ^{O}C, respectively. An increase in temperature typically causes a circuit to slow down due to reduced carrier mobility and increased MOSFET current, interconnect resistance and gate overdrive variations. As a result, the dynamic range, SNDR, SNDR, FOM_1 and FOM_2 are enhanced, unlike SS corner, than that of the 27 ^{O}C at the expense of more power dissipation due to the increased flowing current. In contrast, a decrease in temperature causes a circuit to speed up. Unlike the FF corner, this decreases the dynamic range, SNDR, ENOB, FOM_1 and FOM_2 than that of the 27 ^{O}C with a decrease in the dissipated power. Table 3.11 represents all designs specifications under temperature variations.

Table 3.11: Performance comparison before calibration between the proposed design and the single-ended design at temperature variations.

Parameter	This work				The single-ended design			
	-40^{O}	**27^{O}**	**85^{O}**	**120^{O}**	**-40^{O}**	**27^{O}**	**85^{O}**	**120^{O}**
Dynamic Range (V)	1.32	1.42	1.49	1.54	0.81	0.86	0.78	0.71
DC Voltage (V)	0.75	0.75	0.75	0.75	0.77	0.77	0.77	0.77
Sensitivity (*ps*/*m*V)	0.15	0.1	0.09	0.08	0.14	0.09	0.08	0.08
Linearity Error (%)	3	3	3	3	3	3	2.9	3
P_D (*m*W)	0.23	0.25	0.26	0.27	0.11	0.12	0.13	0.14
$V_{N,RMS}$ (nV/$\sqrt{Hz}$)	2.9	3.5	3.9	4.2	2.1	2.4	2.8	3
SNDR (dB)	72.2	78.8	80	81.2	57.1	60.8	56.5	56
-ENOB (bits)	11.7	12.8	13	13.2	9.2	9.8	9.1	9
FOM_1 ($\times 10^{12}$)	1.9	2.1	2.1	2.2	1.49	1.5	1.2	0.9
FOM_2 (*f*J/conv.)	0.14	0.07	0.06	0.05	0.37	0.27	0.47	0.5

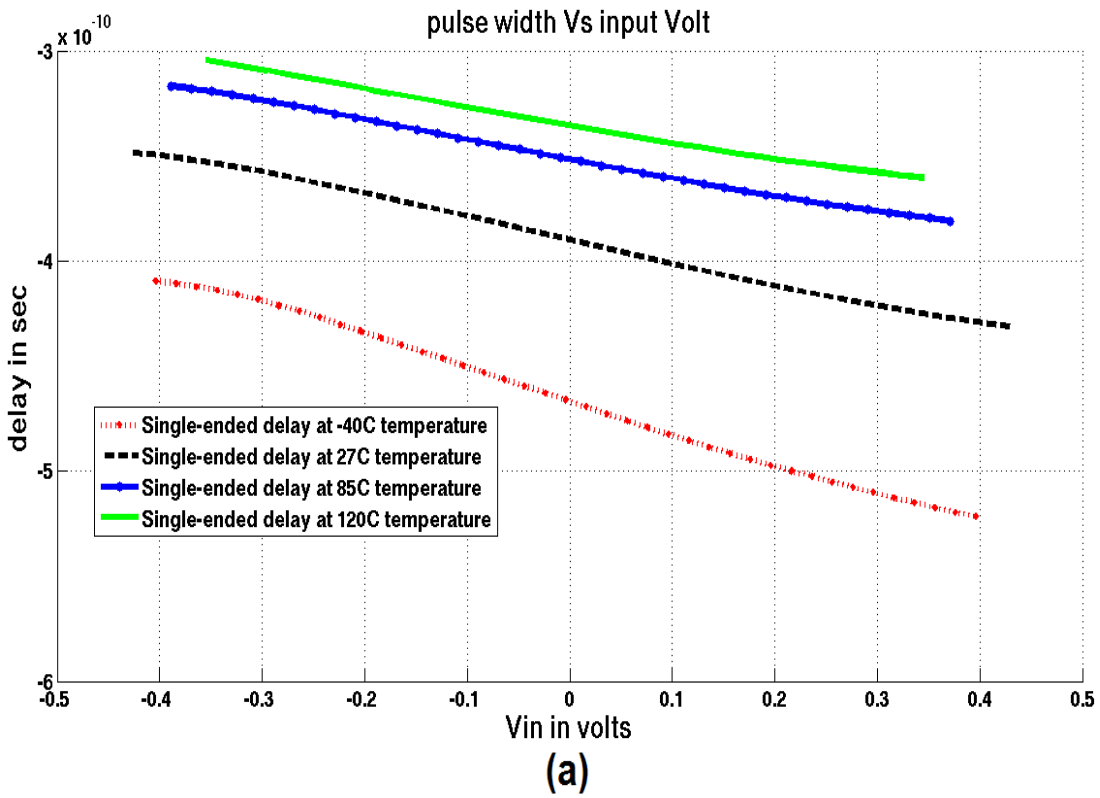


(a)



(b)

Figure 3.25: The proposed differential VTC before calibration at temperature variations. (a) Dynamic linear range (b) Linearity error check.



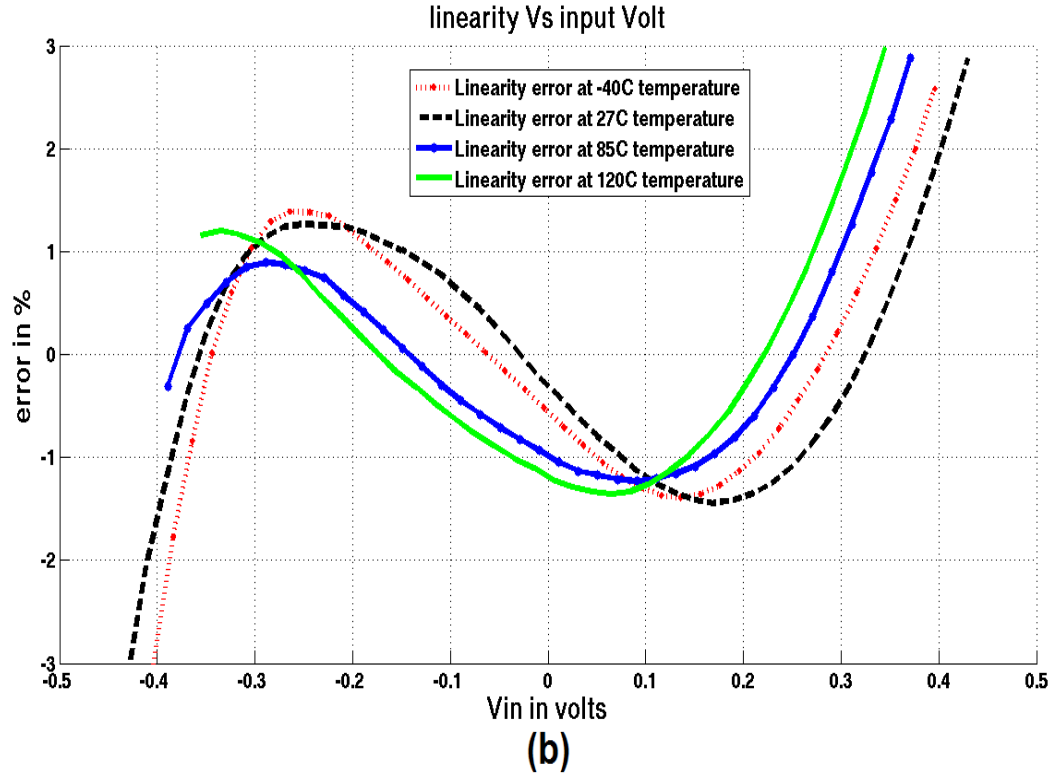


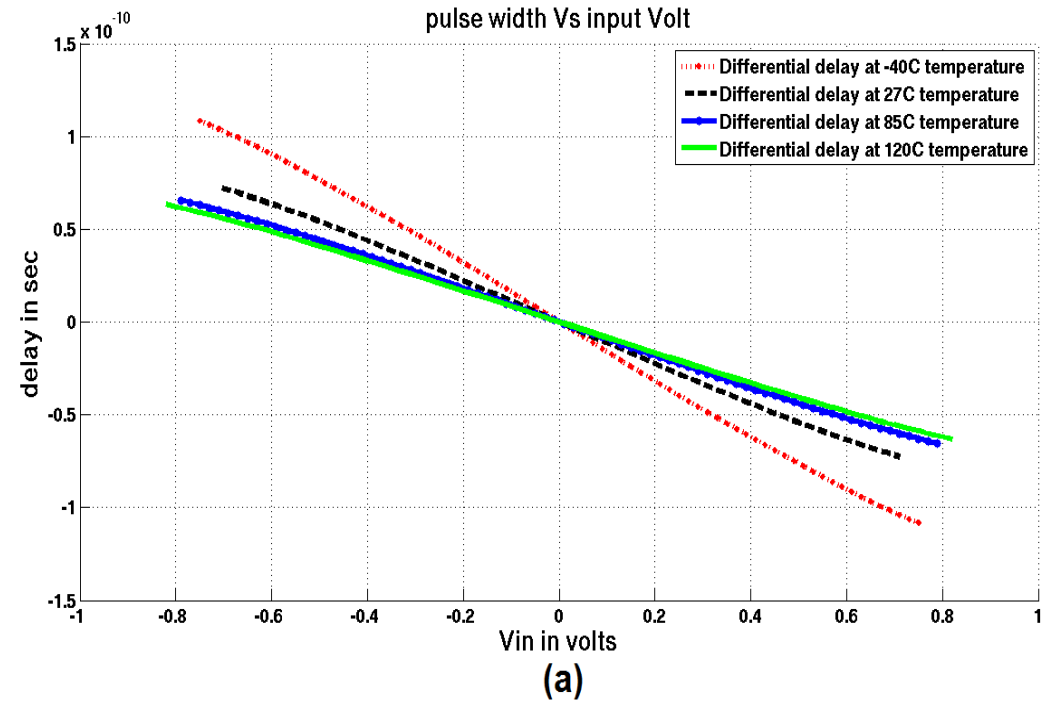
Figure 3.26: The single-ended VTC core before calibration at temperature variations. (a) Dynamic linear range (b) Linearity error check.

3.5.3.3.2. After calibration

Figure 3.27(a), Figure 3.27(b), Figure 3.28(a) and Figure 3.28(b) show the dynamic range and the corresponding linearity error check for both designs at various temperatures after calibration, respectively. The calibrated DC voltage improves the proposed design operated on the worst case temperature -40 ^{O}C by more than 13 %. Due to this enhancement, the proposed design achieves an ENOB at -40 ^{O}C of 13.2 bits which is higher than that of the typical conditions. Table 3.12 represents all designs specifications after calibration under temperature variations. The calibration circuit consumes a 0.19 nW, 0.18 nW, 0.17 nW and 0.16 nW at -40 ^{O}C, 27 ^{O}C, 85 ^{O}C and 120 ^{O}C, respectively. While the design itself consumes 0.23 nW, 0.25 nW, 0.26 nW and 0.27 nW at -40 ^{O}C, 27 ^{O}C, 85 ^{O}C and 120 ^{O}C respectively.

Table 3.12: Performance comparison after calibration between the proposed design and the single-ended design at temperature variations.

Parameter	**This work with the calibration circuit**				**The single-ended design**			
	-40^{O}	**27^{O}**	**85^{O}**	**120^{O}**	**-40^{O}**	**27^{O}**	**85^{O}**	**120^{O}**
Dynamic Range (V)	1.5	1.42	1.58	1.64	0.84	0.86	0.86	0.85
DC Voltage (V)	0.82	0.75	0.8	0.79	0.78	0.77	0.74	0.71
Sensitivity (*ps*/*m*V)	0.15	0.1	0.08	0.08	0.14	0.09	0.08	0.08
Linearity Error (%)	3	3	3	3	3	3	3	3
P_D (*m*W)	0.42	0.43	0.43	0.43	0.11	0.12	0.13	0.14
$V_{N,RMS}$ (nV/$\sqrt{Hz}$)	2.9	3.5	3.9	4.2	2.1	2.4	2.8	3
SNDR (dB)	81.2	78.8	83	82.4	59.6	60.8	60.8	60.2
ENOB (bits)	13.2	12.8	13.5	13.4	9.6	9.8	9.8	9.7
FOM_1 ($\times 10^{12}$)	2.5	2.1	2.4	2.49	1.6	1.5	1.4	1.3
FOM_2 (*f*J/conv.)	0.05	0.07	0.04	0.05	0.28	0.27	0.29	0.34



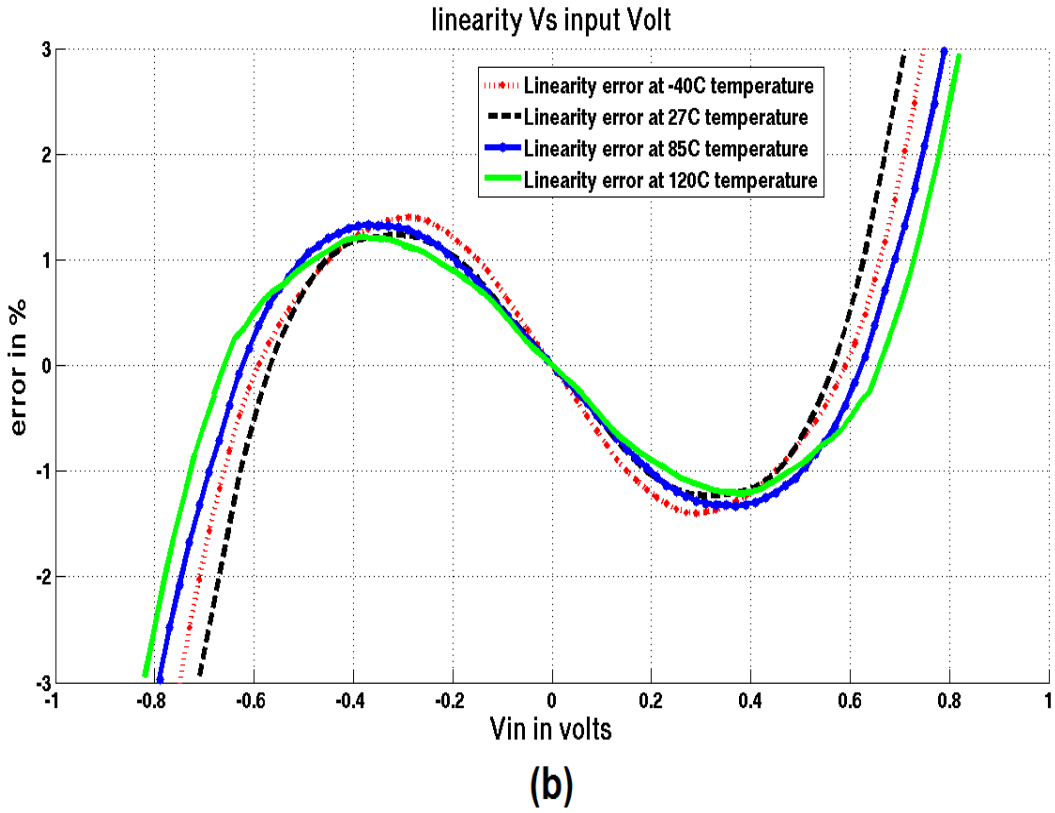
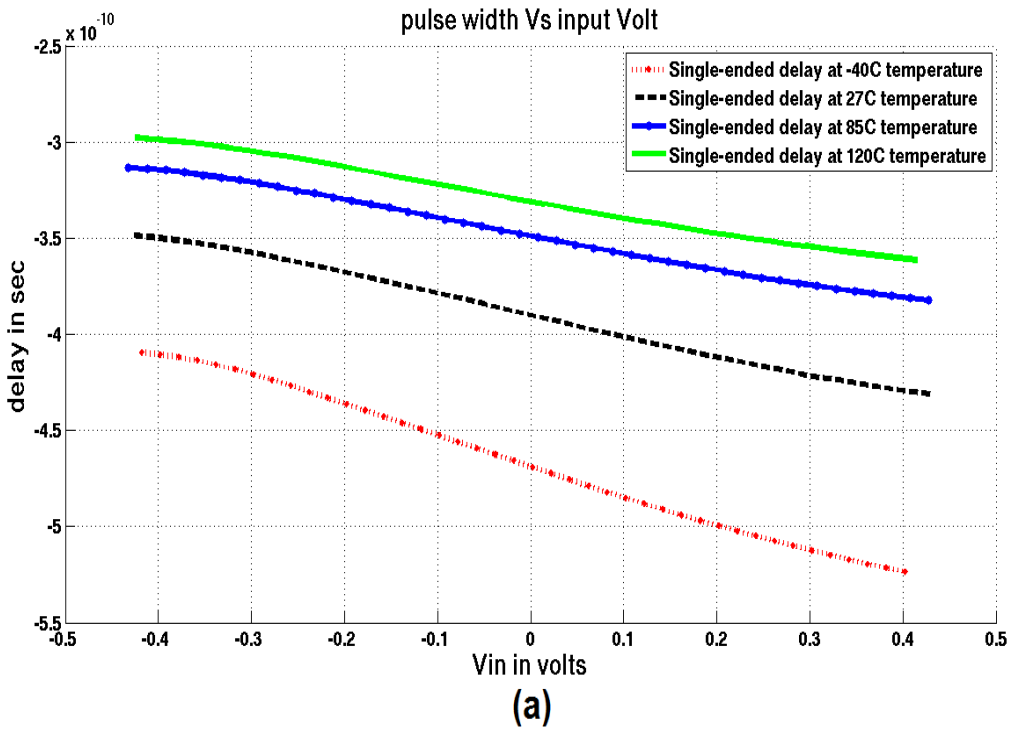


Figure 3.27: The proposed differential VTC after calibration at temperature variations. (a) Dynamic linear range (b) Linearity error check.



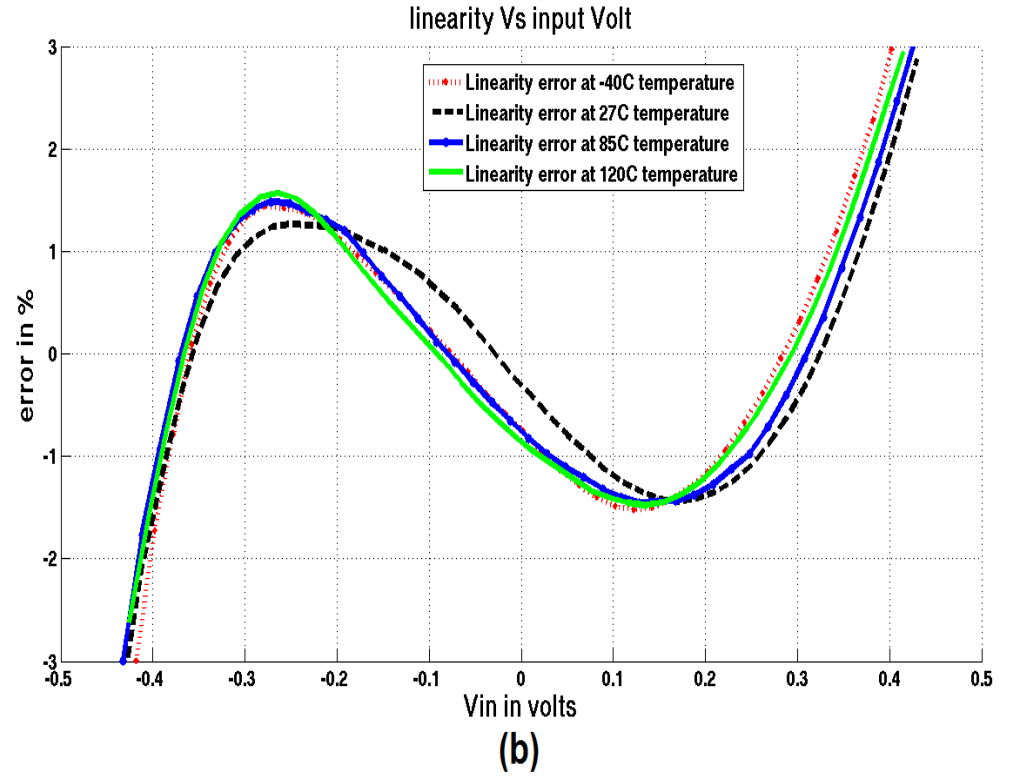


Figure 3.28: The single-ended VTC core after calibration at temperature variations. (a) Dynamic linear range (b) Linearity error check.

3.5.4. MIMCAP-based design Versus MOSCAP-based design

Simulation results have also been done to MIM-capacitor and MOSFET-capacitor based designs. The MIM-capacitor based design shows better results with 10% enhancements than the MOSFET-capacitor (MOSCAP) based design for tolerating PVT variations as shown in Table 3.13. This table illustrates the variations effect on the proposed design linearity error and power at a 1.42 mV dynamic range and a 0.75 mV DC bias voltage (V_{CONST}). Both capacitors equal to 155.4 *F*F. Although using a MIMCAP decreases the PVT variations it also gives more linearization to the design at the expense of the consumed power and area. Hence, it is considered in the proposed design even if the calibration circuits eliminate all the PVT variations.

Table 3.13: Performance comparison between the proposed design with a MIMCAP and a MOSCAP at a fixed dynamic range and DC bias voltage.

Variations	MIMCAP based		MOSCAP based	
	Error (%)	**Power (*m*W)**	**Error (%)**	**Power (*m*W)**
TT state	2.7	0.25	3	0.245
SS corner	4	0.22	5.5	0.216
FF corner	1.2	0.27	1.4	0.266
1.1 V	3.5	0.21	6.3	0.124
1.3 V	7	0.284	10.2	0.23
-40 ^{O}C	3.3	0.23	3.8	0.226
85 ^{O}C	2.8	0.261	4	0.21
120 ^{O}C	2.5	0.272	4.3	0.2

3.6. Differential high-speed VTC circuit

3.6.1. The 2nd differential VTC proposed design

This design is considered the 2nd proposed design by this thesis, where its main objective is to achieve the VTC functionality at higher sampling frequencies. The proposed architecture is as the same as Figure 3.15 in which, the 1st core converts the $+V_{IN}/2$ value into a delay-difference variable (ΔT_2), while the 2nd core converts the $-V_{IN}/2$ value into a delay-difference variable (ΔT_1). These delays are measured between the rising edge of a reference clock (Φ_{CLK}) which samples the input voltage and the rising edge of the core output. The delay equation of the 2nd proposed design (ΔT_0) is the difference between both delay variables (ΔT_2 and ΔT_1). Figure 3.29 shows the single VTC core circuit schematic of the 2nd proposed design.

When Φ_{CLK} changes to logic '0', M6 transistor resets the capacitor stored voltage. The capacitor is a MIMCAP-type to produce smaller parasitic capacitances, linearize the output signal and minimize the high frequencies PVT variations. M1-M3 transistors are a Wilson current mirror [41], where they feed the capacitor with the proper current

generated by M20 through the transmission gate switch, formed by transistors M4 and M5, when Φ_{CLK} changes to logic '1'. At this state, the VTC core output remains at logic '0'. To minimize the gate-source voltage variations due to the current sensitivity, M2

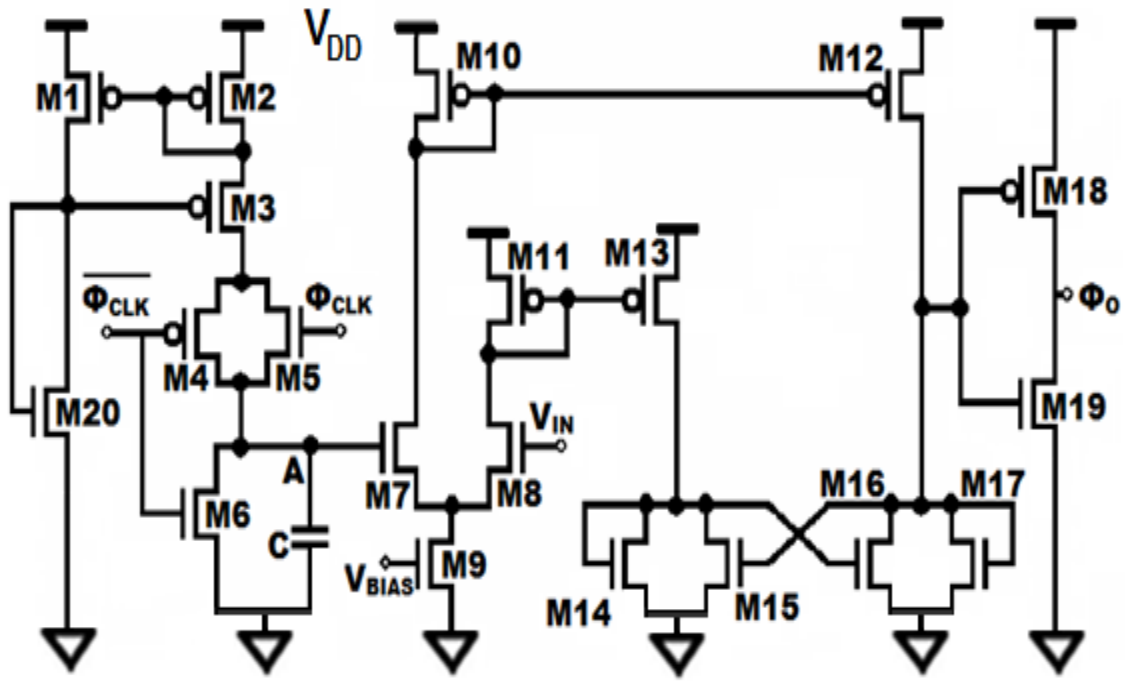


Figure 3.29: Circuit schematic of the core of the differential high-speed VTC design.

transistor should have a higher gate voltage. M7-M13 transistors construct a current-steering amplifier to sense the voltage difference between the capacitor voltage (V_A) and the (V_{IN}). If V_A voltage reaches the aimed V_{IN} voltage, the VTC core output turns into logic '1' with the help of M14-M17 transistors, the latching circuit, to make the correct logic decision and the linear range is maintained. To highly sharpen and linearize the dynamic range, M18-M19 transistors are used which act as an output inverter.

3.6.2. **Simulation results**

The supply voltage of this design is 1 V. The applied DC voltage for the proposed differential design is 0.5 V. The operating clock frequency which has a 50 % duty cycle, is 8 GS/s. A 167 fF MIMCAP is utilized. Figure 3.30(a) and Figure 3.30(b) show the linear range of the 2nd proposed differential VTC design and its single-ended design, respectively, where the linear range is clearly enhanced at the proposed design. Figure 3.31(a) and Figure 3.31(b) show the linearity error of both designs which is not exceed 3 %, respectively.

Table 3.16 shows all specifications of both designs at an 8 GS/s F_S. It illustrates that the proposed design has a better dynamic range, sensitivity and FOM at the expense of the area, power dissipation and the RMS noise than the single-ended design.

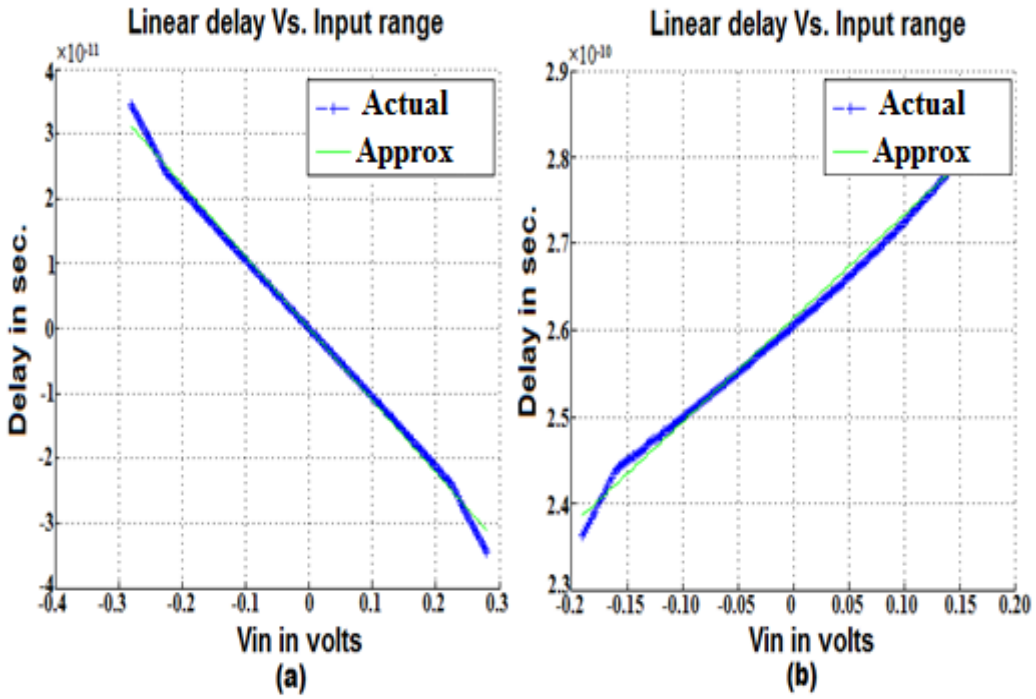


Figure 3.30: Curve fitting of the linear range using MATLAB. (a) The 2nd proposed differential VTC design. (b) The single-ended design.

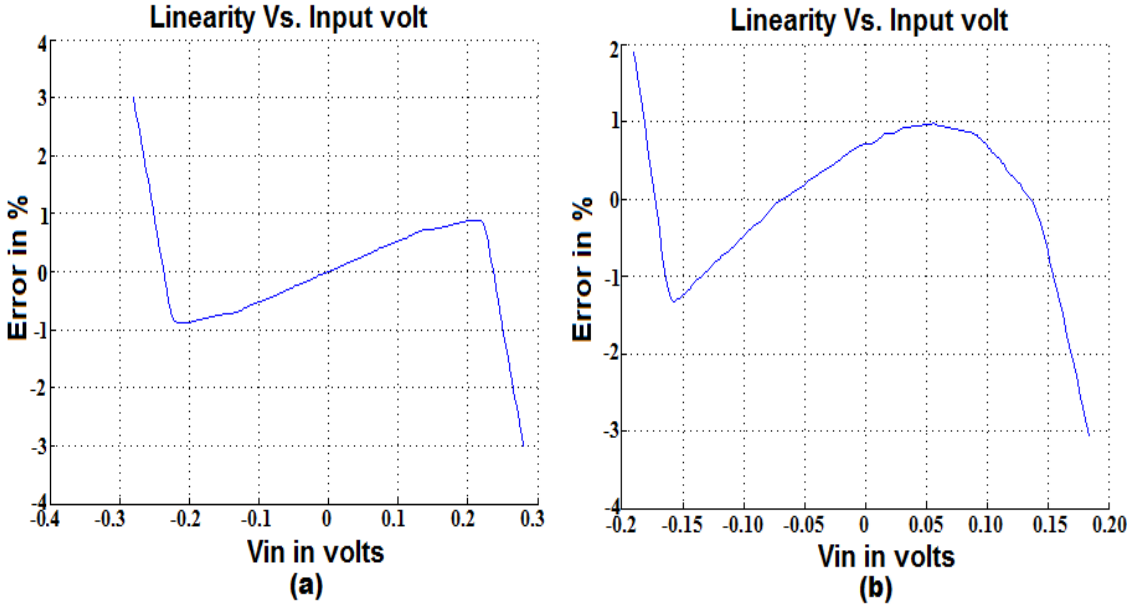


Figure 3.31: Linearity error check of the linear range using MATLAB. (a) The 2nd proposed differential VTC design. (b) The single-ended VTC design.

Table 3.14: Performance comparison between the differential high-speed VTC circuit and its single-ended design @ 3% linearity error

Parameter	The 2nd proposed design	The single-ended VTC design
Input range (V)	-0.28: +0.28	-0.19: +0.19
DR (mV)	560	380
Sensitivity (*p*s/mV)	0.9	0.3
P_D (*m*W)	1.6	0.8
FOM_1 ($\times 10^{12}$)	1.6	1.3
FOM_2 (*f*J/conv.)	0.2	1
$V_{N,RMS}$ ($nV/\sqrt{Hz}$)	14.5	10.2
ENOB (bits)	8.9	5.7
SNDR (dB)	55.4	36.1
Area (μm^2)	742	360

The major contributing noise parameters of the 2nd proposed design are the current flow of the latching circuit, output inverter and the steering amplifier of each VTC core circuit with a percentage of 26 %, 32 % and 41 %, respectively. $V_{N,RMS}$ equals to 1.3 mV at a 8 GS/s F_S, which makes this design be integrated with a 9-bit TDC. The area of this design is 742 μm^2 which includes on top of it the MIMCAP area which equals to 156 μm^2. The ENOB equals to 8.9 bits for a 3.5 GS/s F_{IN}.

Table 3.15 and 3.16 show the VTC specification of both the single-ended high-speed VTC and the 2nd proposed design, respectively, at various sampling frequencies. In each sampling frequency, the DC bias input voltage is optimized to achieve higher FOM_1 and higher dynamic range.

Table 3.15: Performance comparison of the single-ended high-speed VTC while sweeping the sampling frequency.

F_S (GS/s)	Clock T_R and T_F (pS)	Linearity Error (%)	DR (mV)	V_{DC} (mV)	V_{IN} (mV)	Power (mW)	FOM_1 ($\times 10^{12}$)
0.1	1000	2	330	549	-165 : 528	0.9	0.01
1	100	3	342	600	-171 : 171	0.7	0.2
5	10	2.8	312	665	-156 : 156	0.9	0.5
8	2.5	3	372	546	-186 : 186	0.9	1.3

Table 3.16: Performance comparison of the differential high-speed VTC while sweeping the sampling frequency.

F_S (GS/s)	Clock T_R and T_F (pS)	Linearity Error (%)	DR (mV)	V_{DC} (mV)	V_{IN} (mV)	Power (mW)	FOM_1 ($\times 10^{12}$)
0.1	1000	3	944	562	-472 : 472	1.8	0.1
1	100	3	1070	500	-535 : 535	1.4	0.8
5	10	3	702	711	-351 : 351	1.8	1.4
8	2.5	3	560	500	-280 : 280	1.6	1.6

Chapter 4 : Differential VTC Circuits for High-Accuracy Biomedical Applications.

4.1. Introduction

There are a lot of challenges that face the design of a recording neural system such as: designing a way for recording any neurological signal (i.e. an implantable electrode) [16], outputting the recorded signals in order to analyze them and inject other signals as a feedback to cure the disordered signals, and producing a much low power consumption.

The 1st block needed in designing an implantable neural system is a low-noise amplifier (LNA) to magnify microvolt bio-potential signals to a higher level as well as eliminating the noise signal that is spread on a wide-band of frequencies. The LNA block should eliminate the electrode interface DC offset without affecting the real signal.

A low-power low-frequency less-area ADC is needed to simplify analyzing the neurological signals. The ADC should have a high ENOB as several neurological signals operate on near low-band frequencies with near amplitudes. Hence, the ADC should be precise in generating the corresponding digital neurological signal for early and accurate seizure detection. Consequently, the TADC could fulfil all the biomedical applications requirements as it provides a low-power less-area design with high performance.

In this chapter, both proposed designs at chapter 3 (modified differential VTC methodology circuit and the differential high-speed VTC circuit) have been introduced at 130-nm CMOS with a 10 MS/s sampling frequency. A general scaling technique is used to migrate the transistors' size from the 65-nm CMOS platform to the 130-nm CMOS platform. The main advantages of the general scaling is that it does not lead to extreme fields and heat such as constant voltage scaling technique and it does not produce a high loss of noise margin such as full scaling technique.

The rest of Chapter 4 discusses the migration of both proposed designs at UMC 130-nm CMOS technology. Moreover, layout and post-layout simulation results have been illustrated and tested using Calibre and MATLAB. Post-layout simulation results are the steps after: (1) implementing the design layout, (2) applying the Design-Rule Check (DRC), (3) applying the Layout-Versus-Schematic (LVS) check, and (4) applying the Parasitic-Extractions (PEX) [42].

4.2. Modified differential VTC methodology circuit at 130-nm CMOS

4.2.1. Post-layout results without the calibration circuit

The 1st proposed design is optimized to have the maximum allowed linear range with a DC bias voltage of 0.6 V, while the single-ended core is implemented to show the strength of the proposed design which is biased with a DC bias voltage of 0.69 V. This section illustrates the post-layout simulation results at typical conditions before adding the calibration circuit. Figure 4.1 shows the layout of the 1st proposed VTC circuit using Calibre. The proposed layout ensures the minimum-space among all used transistors and wires connections. The area of this design equals to 30.28 × 15.125 µm^2, while it equals

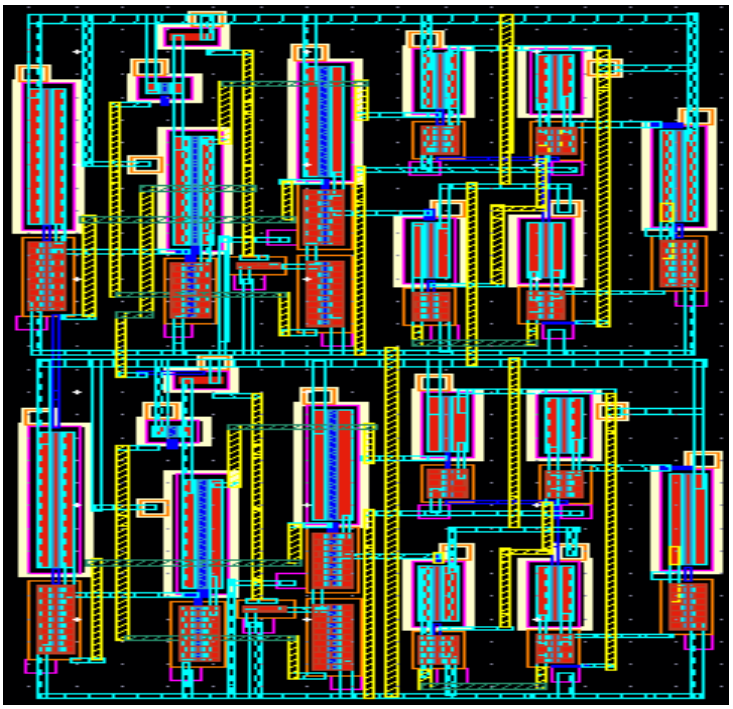


Figure 4.1: Layout of the 1st proposed VTC design.

Table 4.1: Post-layout performance comparison between the 1st proposed design and its single-ended VTC circuit at 3 % linearity error.

Parameter	The 1st proposed VTC design	Single-ended VTC Methodology
Linear range (mV)	-460 : 460	-232 : 232
DC bias (mV)	600	690
VTC Area (µm^2)	458	228.8
DR (mV)	920	470
Sensitivity (ps/mV)	2.31	2.29
$V_{N,RMS}$ $(nV/\sqrt{Hz})$	692	1.7
P_D (µW)	11.3	6.3
FOM_1 ($\times 10^{12}$)	0.75	0.35

to 15.13 × 15.125 μm^2 for the single-ended VTC methodology design.

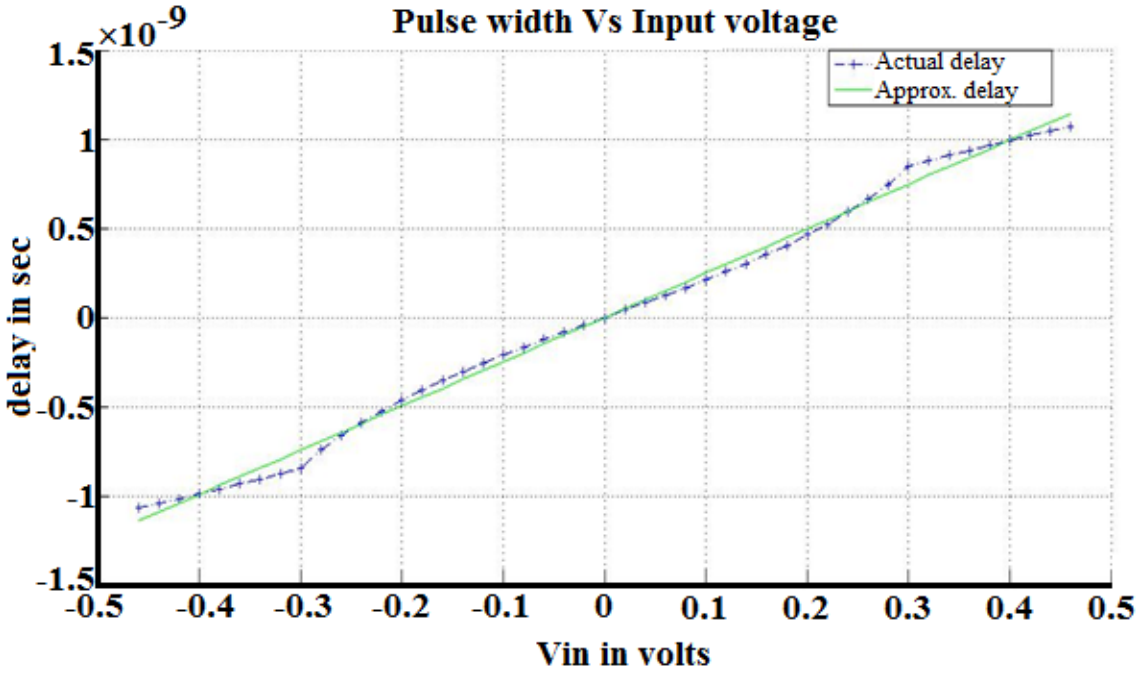


Figure 4.2: The post-layout linear range of the 1st proposed VTC design at 3 % linearity error.

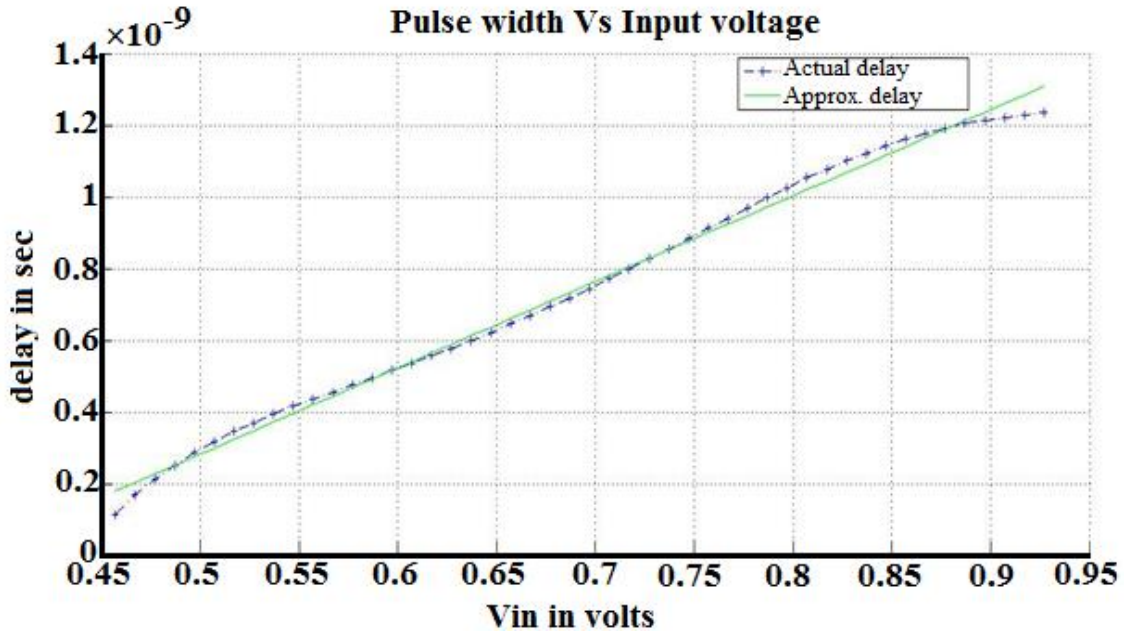


Figure 4.3: The post-layout linear range with the DC bias of the single-core of the 1st proposed VTC design at 3 % linearity error.

Table 4.1 illustrates the post-layout simulation results of both the 1st proposed VTC design and its single-ended design. Although transistors sizes are migrated to 130-nm CMOS which maximizes the dissipated power due to the larger flowing current through transistors, operating on a low frequency (10 MS/s F_S) is the prior to minimize the overall

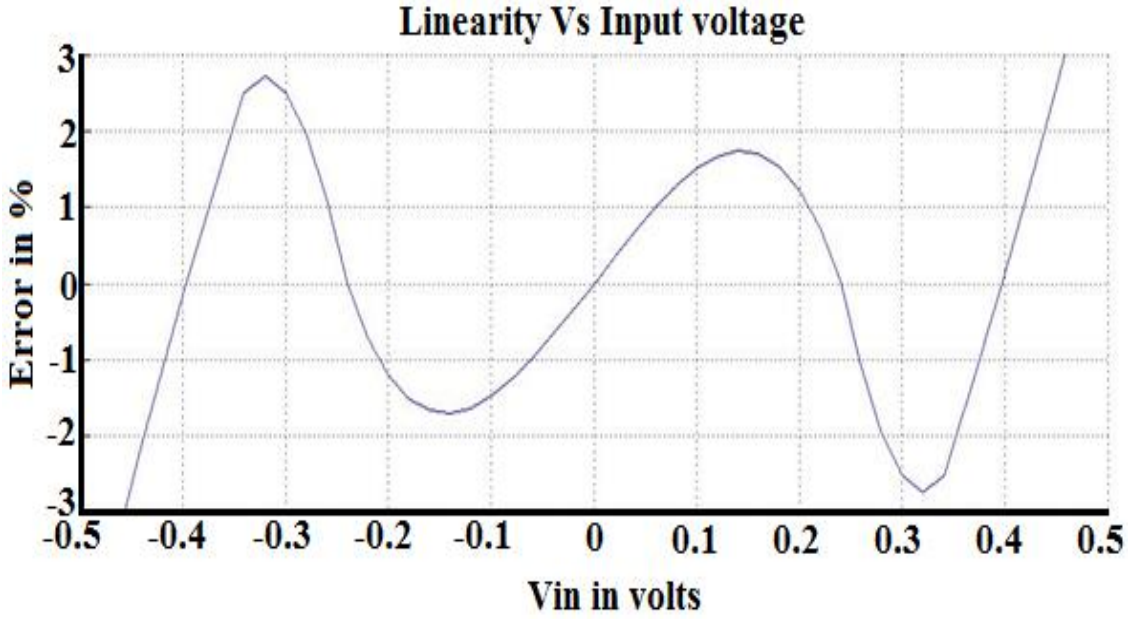


Figure 4.4: The post-layout linearity error check of the 1st proposed VTC design.

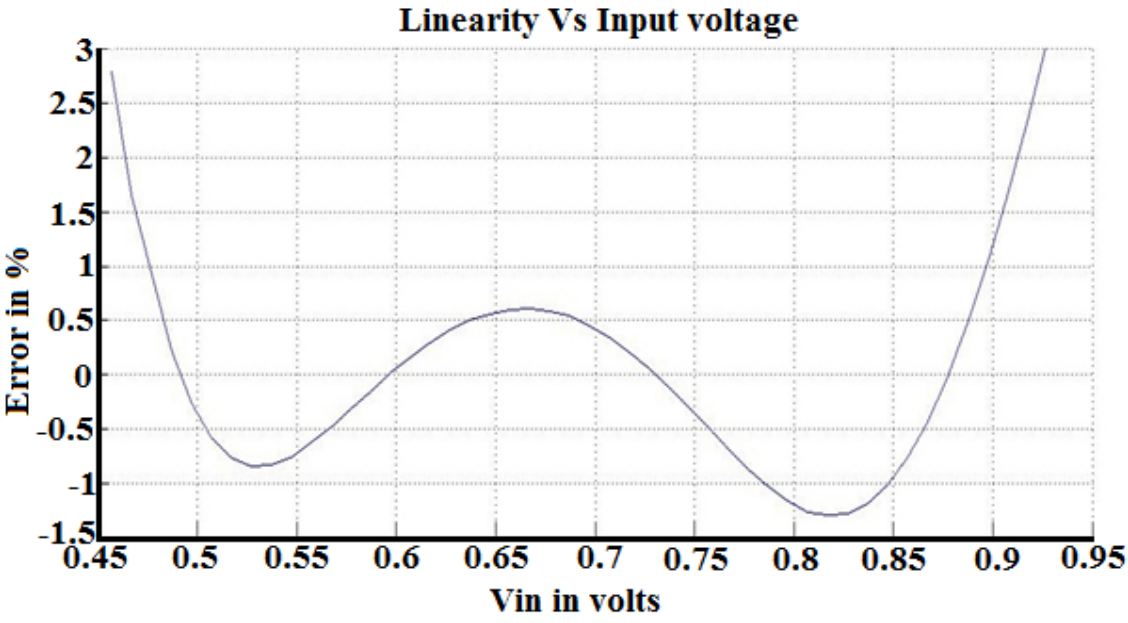


Figure 4.5: The post-layout linearity error check of the single-core of the 1st proposed VTC design.

power consumption. The added parasitic resistances and capacitances, as a result from running the PEX to the proposed layout, imply a larger circuit sensitivity value where the proposed design output delay gets increased. Moreover, the $V_{N,RMS}$ value of the proposed design is maximized due to the PEX effect.

Figure 4.2 and Figure 4.3 show the linear range at 3 % linearity error for both the 1st proposed VTC design and its single-ended design, respectively. Whereas, Figure 4.4 and Figure 4.5 show the linearity error check for both designs, respectively. The proposed design has a higher DR of 920 mV due to the differential architecture. FOM_1 of the 1st proposed design equals to 0.75×10^{12}. This value is less than the FOM_1 derived from Table 3.6 for the same design implemented at 65-nm CMOS technology node due to the design's low sampling frequency. Noise simulations have been simulated at post-layout over the frequencies for both the 1st proposed design and the single-ended design at TT corner. At very low frequencies (mille hertz), the noise falls down due to the flicker noise effect. Then, it becomes flat due to the thermal noise.

Figure 4.6 and Figure 4.7 show the linear range and the linearity error check, respectively, of the 1st proposed VTC design at SS corner before adding the calibration circuit. The SS corner affects the dynamic range badly. Hence, the dynamic range should be decreased to keep the linearity error as lower as we can. This input range at 3% linearity error is from -0.34 V: 0.34 V (i.e. the dynamic range equals to 0.68 V). Actually, it needs to be tolerated to enhance the VTC specifications.

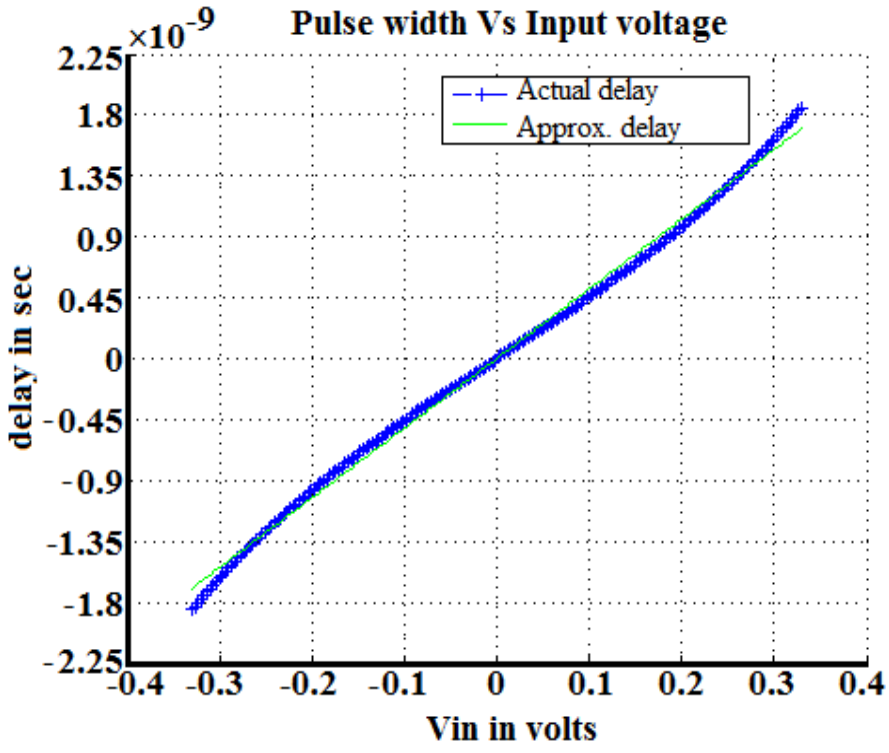


Figure 4.6: Dynamic range of the 1st proposed differential VTC at SS corner before calibration at 3% linearity error.

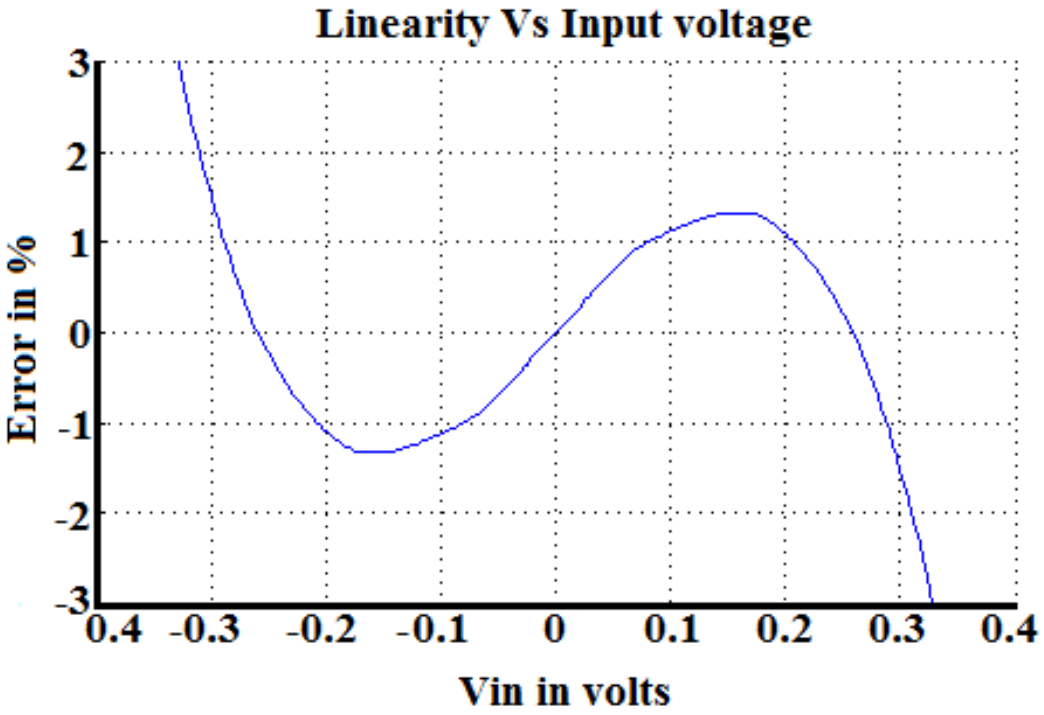


Figure 4.7: Linearity error check of the 1st proposed differential VTC at SS corner before calibration.

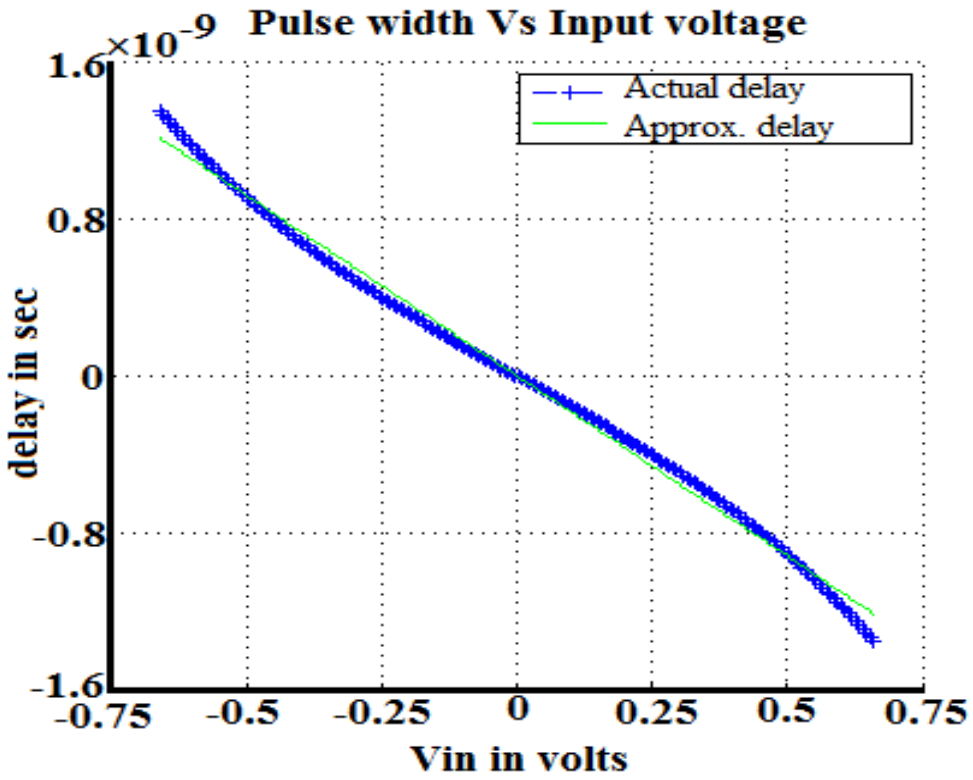


Figure 4.8: Linearity error check of the 1st proposed differential VTC at FF corner.

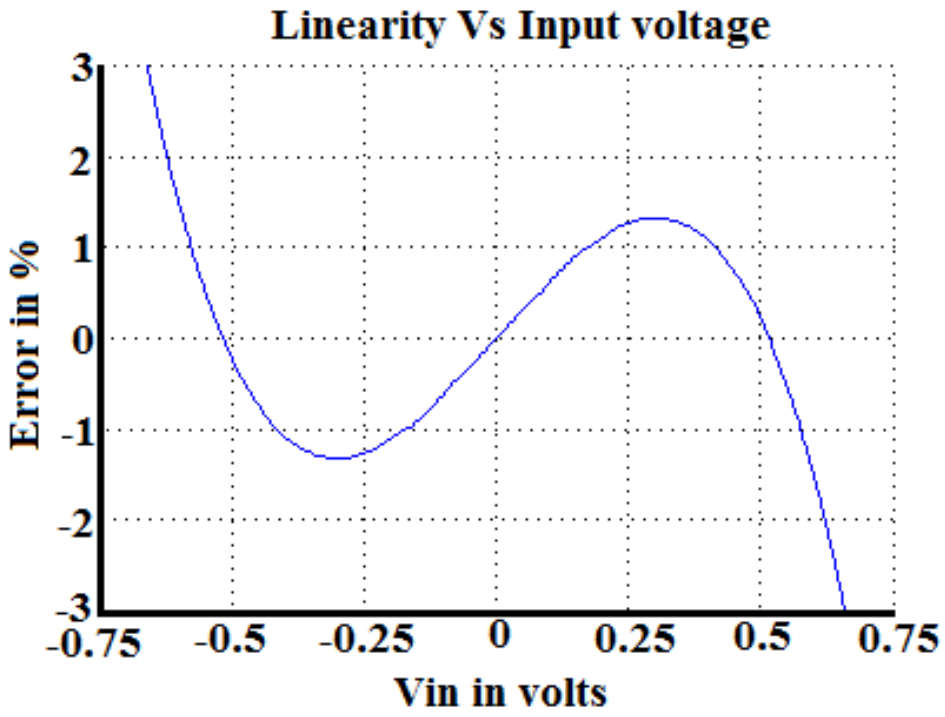


Figure 4.9: Linearity error check of the 1st proposed differential VTC at FF corner.

On the other hand, Figure 4.8 and Figure 4.9 show the linear range and the linearity error check, respectively, of the 1st proposed VTC design at FF. Due to increasing the electrons' speed of pMOS and nMOS devices, The FF corner enhances the VTC specifications with the expense of extra heads on the power consumption and with less circuit sensitivity. The consumed power increased due to the high electrons' mobility which produces high flowing current. While, the sensitivity is decreased due to the produced lower delay in the circuit design due to the electrons' speed. The input range at 3% linearity error is from -0.675 V: 0.675 V (i.e. the dynamic range equals to 1.35 V). This dynamic range is higher than the TT corner dynamic range. Consequently, there is no need to add a calibration circuit for this design.

Table 4.2 shows the post-layout specifications of the 1st proposed design at various corners before adding a calibration circuit. This is to check the design performance of the proposed design after designing the layout against the corners changes. The SS corner shows a higher RMS noise due to the higher produced thermal noise. In additions, it provides the highest sensitivity due to the decreased electrons' mobility among the whole circuit devices. Finally, the overall FOM_1 is enhanced at the FF corner.

Table 4.2: Post-layout performance comparison of the 1st proposed design corner variations at 3 % linearity error before calibration.

Parameter	TT corner	SS corner	FF corner
Dynamic Range (V)	0.92	0.68	1.35
DC Voltage (V)	0.6	0.6	0.6
Sensitivity (ps/mV)	2.31	2.8	1
Linearity Error (%)	3	3	3
P_D (µW)	11.3	9.9	12.2
$V_{N,RMS}$ (nV/$\sqrt{Hz}$)	692	711	652
FOM_1 ($\times 10^{12}$)	0.75	0.47	1.5

4.2.2. **Post-layout results with the calibration circuit**

This section illustrates the post-layout simulation results at corners variations (SS and FF) after adding the calibration circuit. As the maximum allowed dynamic range is achieved at TT corner and FF corner. The calibration circuit is maintained to maximize the dynamic range at the SS corner, in additions to, design a real DC bias voltage for the FF and TT corners instead of feeding them to the circuit externally. This adds some extra heads on the consumed power and area. The calibration circuit that is discussed in Section 3.5.3 is modified to achieve the highest DR that could be provided by this technology node (130nm CMOS).

Figure 4.10 and Figure 4.11 show the linear range and the linearity error check, respectively, of the 1st proposed VTC design at SS corner after adding the calibration circuit. The dynamic range is enhanced at 3% linearity error to be in a range of -0.6 V: 0.6 V (i.e. the dynamic range equals to 1.2 V). Also, the FOM_1 is increased due to higher dynamic range at almost same power consumption (only 0.01 µW overheads in the consumed power due to the calibration circuit).

Table 4.3 shows the post-layout specifications of the 1st proposed design at various corners after adding a calibration circuit. It shows the enhancements of the proposed design at the SS corner regarding the calibration circuit which is revealed at the FOM_1 value (it is higher than the FOM_1 of the proposed design at TT corner).

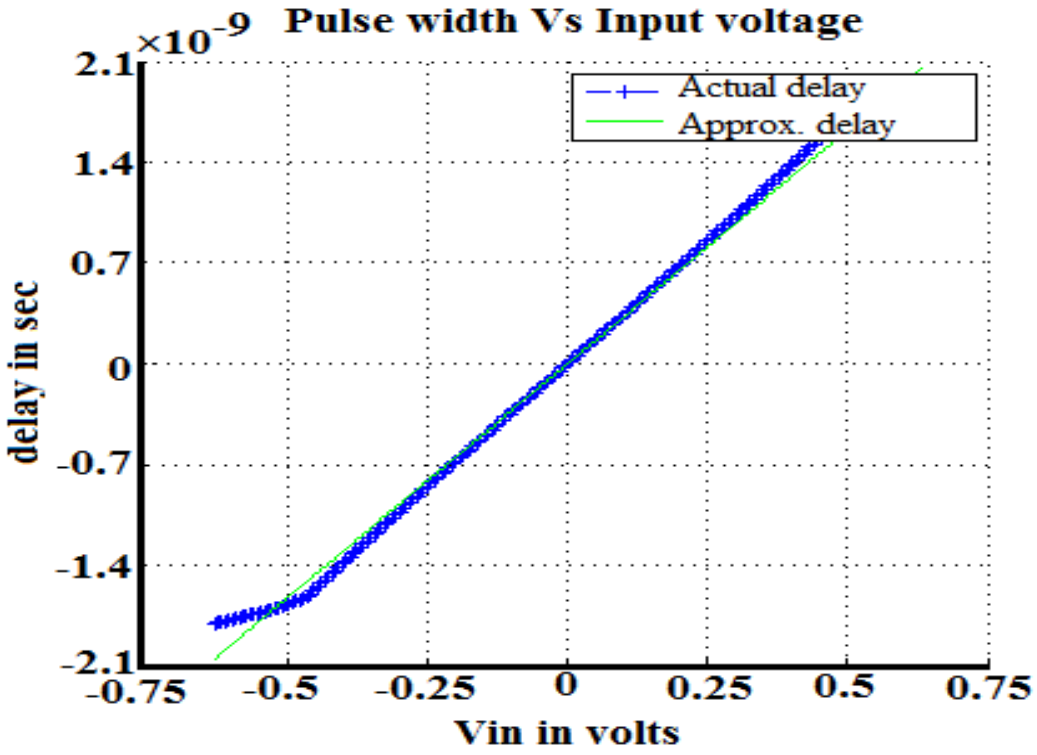


Figure 4.10: Dynamic range of the 1st proposed differential VTC at SS corner after calibration at 3% linearity error.

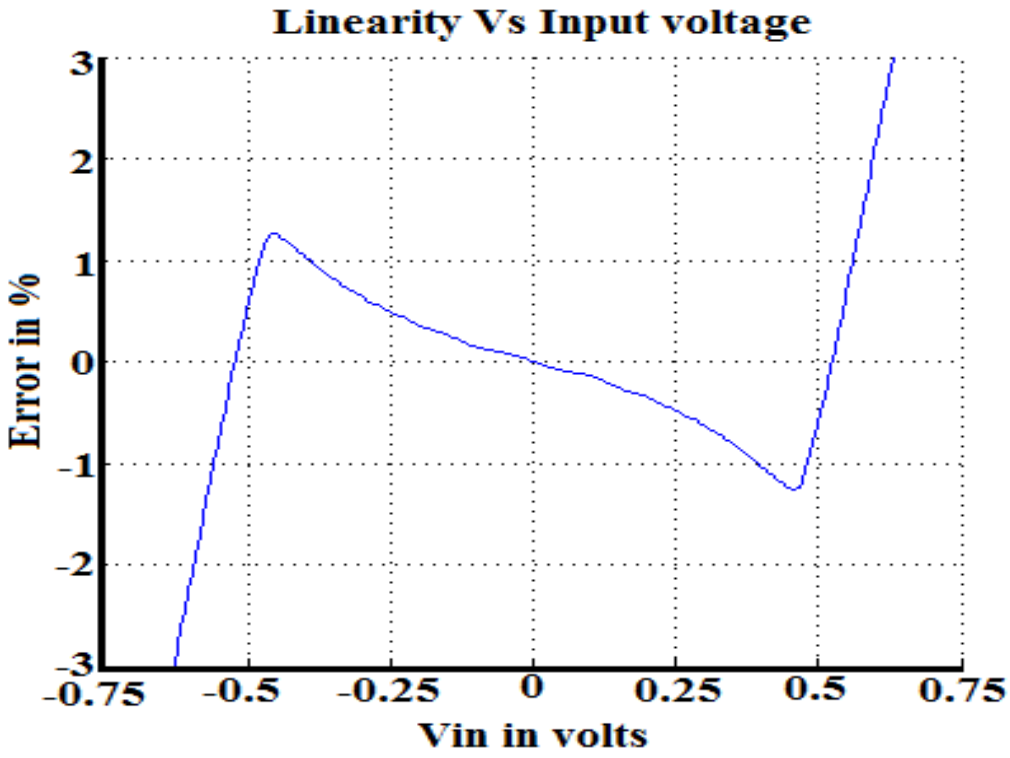


Figure 4.11: Linearity error check of the 1st proposed differential VTC at SS corner after calibration.

Table 4.3: Post-layout performance comparison of the 1st proposed design corner variations at 3 % linearity error after calibration.

Parameter	TT corner	SS corner	FF corner
Dynamic Range (V)	0.92	1.2	1.35
DC Voltage (V)	0.6	0.44	0.6
Sensitivity (ps/mV)	2.31	1.6	1
Linearity Error (%)	3	3	3
P_D (µW)	11.31	9.93	12.21
$V_{N,RMS}$ ($n\text{V}/\sqrt{Hz}$)	692	711	652
FOM_1 ($\times 10^{12}$)	0.7	1.45	1.49

4.3. Differential high-speed VTC circuit at 130-nm CMOS

The 2nd proposed design is optimized to have the maximum allowed linear range with a DC bias voltage of 645 mV. Figure 4.12 shows the layout of the 2nd proposed VTC circuit using Calibre. The area of this design equals to 43.32 × 34.27 µm^2, while it equals to 43.32 × 16.63 µm^2 for the single-ended VTC design.

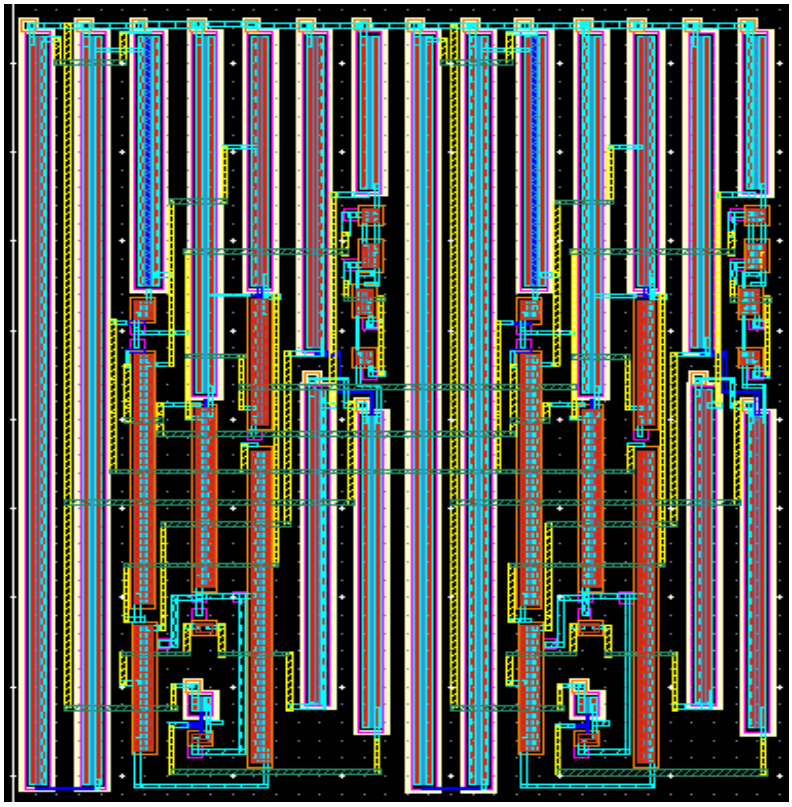


Figure 4.12: Layout of the 2nd proposed VTC design.

Table 4.4: Post-layout performance comparison between the 2nd proposed design and its single-ended VTC circuit.

Parameter	The 2nd proposed VTC design	Single-ended VTC design
Linear range (mV)	-462 : 462	-185 : 185
DC bias (mV)	645	645
Linearity Error (%)	2.2	2.9
VTC Area (µm^2)	1484.6	720.4
DR (mV)	924	370
Sensitivity (ps/mV)	8	6.3
$V_{N,RMS}$ $(nV/\sqrt{Hz})$	5.7	4
P_D (mW)	0.2	0.07
FOM_1 ($\times 10^{12}$)	0.04	0.02

Table 4.4 illustrates the post-layout simulation results of both the 2nd proposed VTC design and its single-ended design. The added parasitic resistances and capacitances, maximizes circuit sensitivity with extra overheads in the dissipated power and noise.

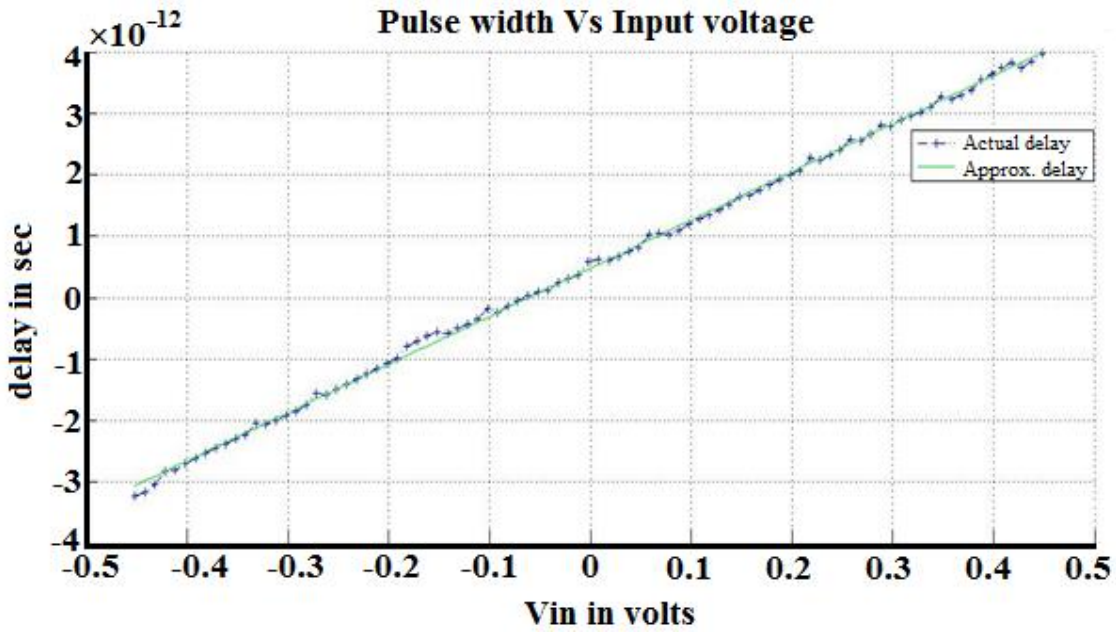


Figure 4.13: The post-layout linear range of the 2nd proposed VTC design at allowed linearity error.

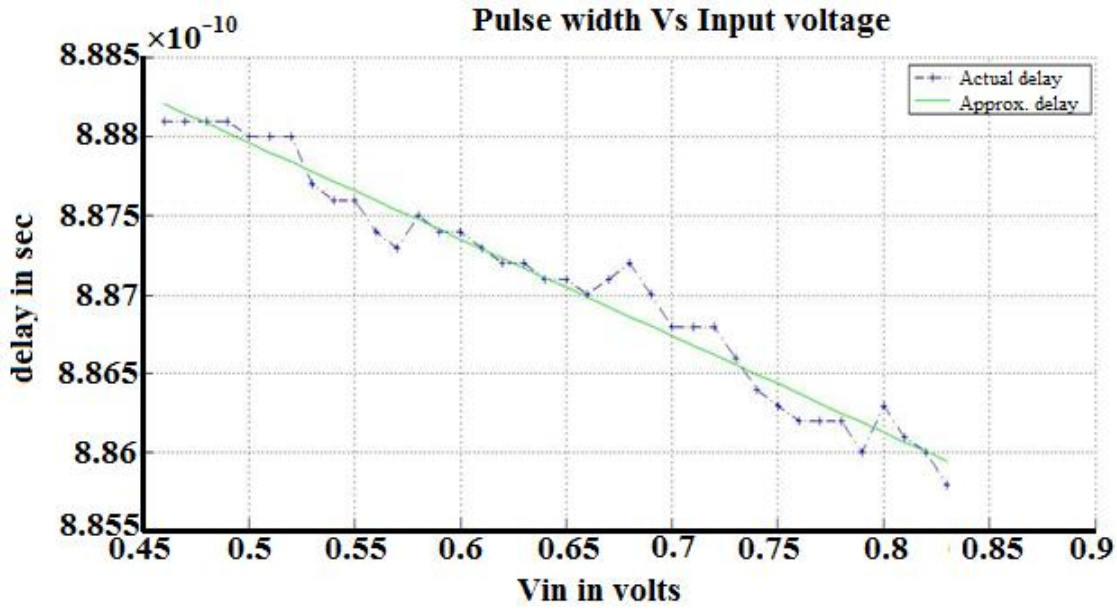


Figure 4.14: The post-layout linear range of the single-core of the 2nd proposed VTC design at allowed linearity error.

Figure 4.13 and Figure 4.14 show the linear range at allowed linearity error for both the 2nd proposed VTC design and its single-ended design, respectively. Whereas, Figure 4.15 and Figure 4.16 show the linearity error check for both designs, respectively. The

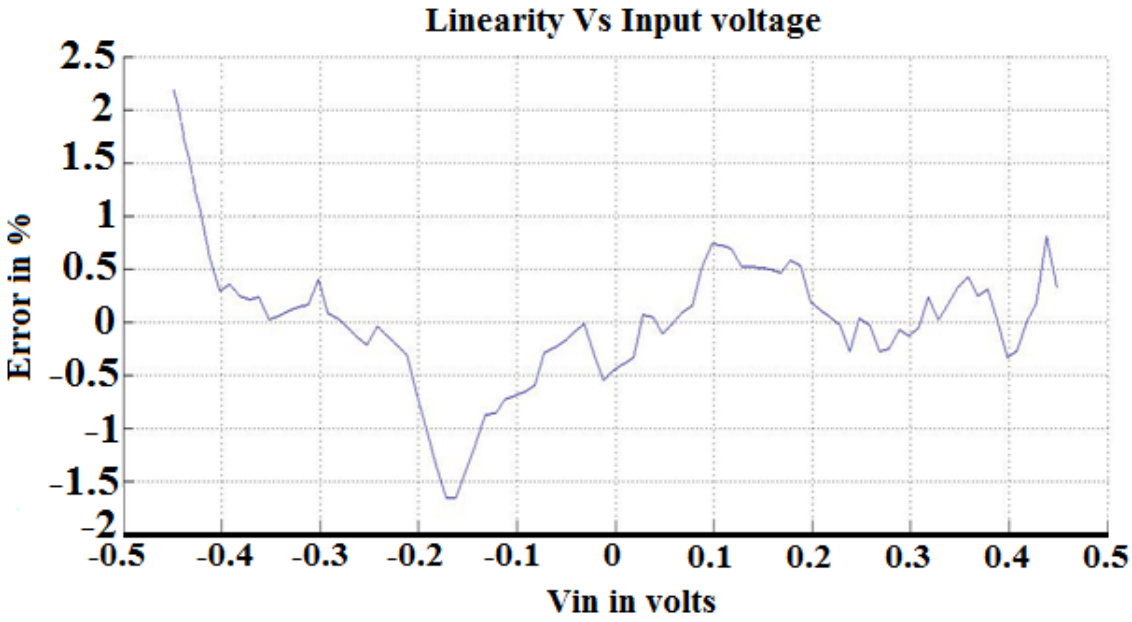


Figure 4.15: The post-layout linearity error check of the 2nd proposed VTC design.

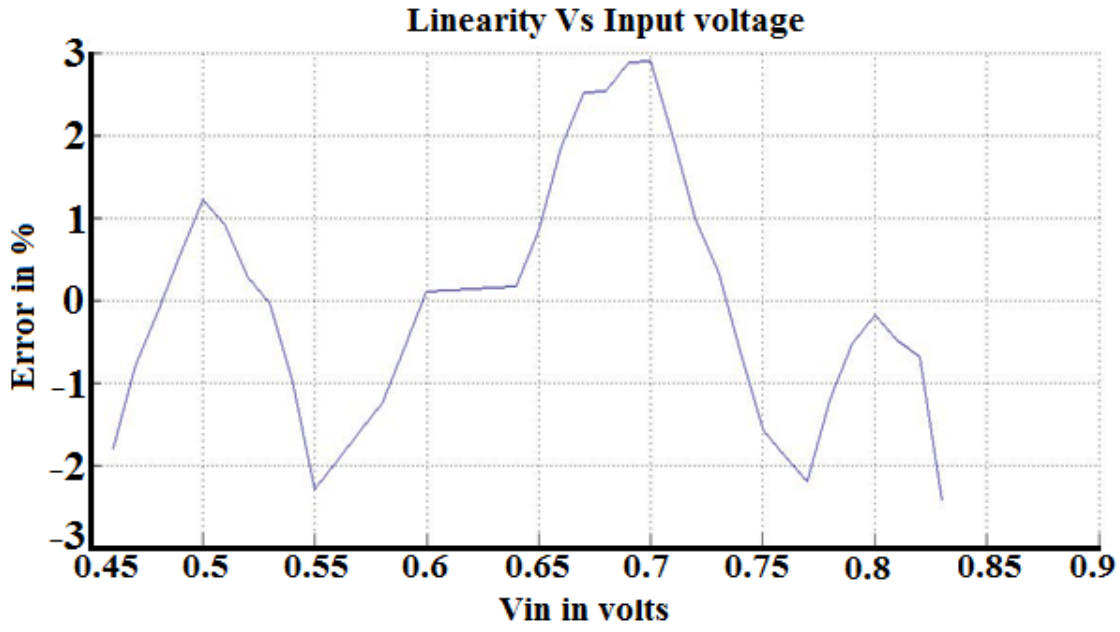


Figure 4.16: The post-layout linearity error check of the single-core of the 2nd proposed VTC design.

proposed design has a higher DR of 924 mV due to the differential architecture. FOM_1 of the 1st proposed design equals to 0.04×10^{12}. This value is less than the FOM_1 derived from Table 3.13 for the same design implemented at 65-nm CMOS technology node due to the design's low sampling frequency as well as the high dissipated power due to parasitic capacitances. Noise simulations have been simulated at post-layout over the frequencies for both the 2nd proposed design and the single-ended design. $V_{N,RMS}$ of the 2nd proposed design equals to 5.4 nV/$\sqrt{Hz}$.

Discussion and Conclusions

1. Proposed designs performance

This thesis introduces novel differential VTC circuits designed using TSMC of 65nm CMOS technology and UMC of 130nm CMOS technology. It has made several important contributions up to the author's knowledge, such as:

- Novel fully-differential VTC circuits based on MIM capacitors.
- The first published VTC circuit that reports a higher ENOB of 10.7 bits at 2.5 GS/s [43].
- The highest reported ENOB of 12.8 bits at 1GS/s (the 1st proposed design).
- The highest FOM reported (0.07 *f*J/conversion of the 1st proposed design).
- The fastest currently published VTC (8 GS/s of the 2nd proposed design) [44].
- A detailed study of the PVT variations tolerated with a low-power and low-area calibration circuit.
- Different kinds of linearity analysis (dynamic range, linearity error, SNDR, ENOB and THD) of VTC circuits.
- The lowest reported layout area of differential VTC circuits of 458 μm^2 and 1484 μm^2 of the 1st proposed design and the 2nd proposed one, respectively, at 130nm CMOS technology.
- The lowest reported power consumption of a differential VTC circuit (0.16 mW) [43].

2. Future work

The concept of time-based ADC is almost new and the possibilities seem endless at this stage of its development as designers aim to exploit all possibly advantages of the deep submicron CMOS technology. The work presented in this thesis proposes various implementations of differential scheme of the 1st block in designing the TADC which is the VTC with a basic calibration circuit to enlarge and enhance the design linearity affected by the PVT variations. There are other ideas to provide more enhancements in designing the TADC and to extend this work such as:

- The proposed VTC designs could be modified to operate on higher sampling frequencies with consuming a low power by minimizing the transistors' sizes and modifying the large-sized inverter that acts as a buffer delay. This could also increase the applied signal bandwidth and reduce the circuit linearity distortion.

- Due to the differential architecture used in the proposed designs, mismatches could be possibly generated in each single core design. This results in a DC offset in the core output. Hence, a basic filter might be utilized to extract the output offset to be provided to next stage TDC block.

- Proposing a TDC which could deal simultaneously with the pulses produced by the block that has an applied input signal with a positive half amplitude and the block that has an applied input signal with a negative half amplitude.

- Proposing a differential TDC, in which each single-core takes the output delay of a single-core of the differential VTC. Then, each core converts the produced delay into digital words. After that, an assembly block gets the output of each core in order to be organized digitally by a DSP approach. A differential TADC is fairly used in the research work.

- Proposing a 10-bit digital-to-analog converter to produce a number of 1024 level to fully eliminate the DC offset that is produced by the PVT variations.

- Proposing a complete background calibration technique which could be applied to the full TADC block. This technique has a feedback connection from the TADC design to estimate the needed voltage/current that could be provided to neglect all possible PVT variations as well as the high jitter produced by the TDC block.

- Implementing a TADC IC chip and providing the experimental (measurement) results by a testing environment. This could also be integrated with a complete transceiver chain that could be used in various applications.

- Providing a time-interleaved architecture for the complete TADC block in order to maximizing the used operating sampling frequency and the allowed input frequency that is used to calculate the THD, SNDR and the ENOB. The TADC block is considered the sub-ADC block shown in Figure 2.14. The time-interleaved mechanism needs a timing generation to generate the needed clock frequency for each TADC block. With an 8 GS/s TADC, the time-interleaved design could reach to the fastest reported ADC design in the mixed-signal research work. A calibration circuit is highly recommended in this case to overcome the offset and gain errors which are differently produced in each TADC block that is connected with a output multiplexing block.

- Spreading the time-based approach in several research areas such as: the DC-DC converter where the first DC signal will be converted to time, then to another DC signal. This could enhance the overall converter specifications.

- A high resolution TADC could be implemented if each time delay produced by each core of the differential VTC is possibly added with the help of designing cascading TADCs.

- Providing a sample-and-hold (S/H) circuit could enlarge the applied input signal frequency which is restricted by the circuit linearity distortion, the Nyquist criterion and the sampling frequency. This also enhances a lot of linearity error problems at higher signal speed.

- A final proposal is to study the layout effect of much lower CMOS technology nodes for the TADC design. In additions, it is preferable to validate the TADC approach with the use of the tri-state transistors (i.e. FINFET transistor).

3. Conclusion

The main objective of this thesis is to introduce 2 proposed differential VTC circuits based on MIM capacitors applicable for SDR system and biomedical applications in 65nm CMOS technology and 130nm CMOS technology, respectively. The layout of both designs is introduced at 130nm CMOS using Calibre tool. Linearity analysis including dynamic range and ENOB is ensured for both designs using Cadence Virtuoso and MATLAB. A study of the PVT variations is introduced for the 1st proposed design with proposing a simple calibration circuit. The calibration circuit adapts the DC bias voltage that is fed to the proposed design in order to overcome the PVT variations that cause imperfections on the design linearity. It's designed based on a set of the capacitor-based voltage dividers to ensure a low-power and a low-area circuit.

First, at 65nm CMOS simulation results, the 1st proposed design achieves a 12.8 bits ENOB, a 1.42 V dynamic range, a 2.1×10^{12} FOM_1, a 0.07 *f*J/conversion FOM_2, a 3.5 $nV/\sqrt{Hz}$ $V_{N,RMS,}$ a 229 μm^2 area and a 0.25 mW power. It operates on a 1 GS/s F_S with a 1.2 V supply voltage. The total area of the calibration circuits equals to 3.4457 μm^2, while the consumed power equals to 0.3 nW. The 2nd proposed design operates on a 8 GS/s F_S with a 1 V supply voltage. It achieves 8.9 bits ENOB, a 0.56 V dynamic range, a 1.6×10^{12} FOM_1, a 0.2 *f*J/conversion FOM_2, a 742 μm^2 area and a 1.6 mW power.

Second, at 130nm CMOS post-layout simulation results, the 1st proposed design achieves a 0.92 V dynamic range, a 0.75×10^{12} FOM_1, a 692 $nV/\sqrt{Hz}$ $V_{N,RMS,}$ a 458 μm^2 area and a 0.01 mW power. It operates on a 10 MS/s F_S with a 1-V supply voltage. The 2nd proposed design operates on a 10 MS/s F_S with a 1 V supply voltage. It achieves a 0.924 V dynamic range, a 0.04×10^{12} FOM_1, a 1484 μm^2 area and a 0.2 mW power.

References

[1] K. Poulton, and T. Hornak, "A 1-GS/s 6-bit ADC System," IEEE Journal of Solid-State Circuits (JSSC) , vol. 22, no. 6, pp. 962–970, 1987.

[2] K. Poulton, J. Kerley, J. Kang, J. Tani, E. Cornish, and et al., "an 8-GS/s 8-bit ADC system," IEEE Symposium on Very Large Scale Integration (VLSI) Circuits, pp. 23–24, 1997.

[3] K. Uyttenhove, and M. Steyaert, "A 6-bit 1 GS/s Acquisition Speed CMOS Flash ADC with Digital Error Correction," IEEE Custom Integrated Circuits Conference (CICC), pp. 249–252, 2000.

[4] B. Razavi, Design of Integrated Circuits for Optical Communications. John Wiley and Sons, 2012.

[5] E.M.I. Gustafsson, "reconfigurable analog to digital converters for low power wireless applications," Doctoral Dissertation KTH – Royal Institute of Technology Stockholm, 2008.

[6] A.R. Macpherson, "a time-based 5GS/s CMOS analog-to-digital converter," A Thesis Submitted to the Faculty of Graduate Studies in the University of Calgary in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy, 2013.

[7] R. Saad, D.L. A.-Ramirez, and S. Hoyos, "Sensitivity Analysis of Continuous-Time ΔΣ ADCs to Out-of-Band Blockers in Future SAW-Less Multi-Standard Wireless Receivers," IEEE Transactions on Circuits and Systems (TCAS) I: Regular Papers, vol. 59, no. 9, pp. 1894–1905, 2012.

[8] P.K. Yenduri, A.Z. Rocca, A.S. Rao, S. Naraghi, M.P. Flynn, and et al., "A low-power compressive sampling time-based analog-to-digital converter," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 2, no. 3, pp. 502-515, 2012.

[9] T. Oh, H. Venkatram, and U.-K. Moon, "A Time-Based Pipelined ADC Using Both Voltage and Time Domain Information," IEEE JSSC, vol. 49, no. 4, pp. 961–971, 2014.

[10] C.R. Anderson, J.E. Ibrahim, R.M. Buehrer, and J.H. Reed, "Analysis and Implementation of a Time-Interleaved ADC Array for a Software-Defined UWB Receiver," IEEE Transactions on Vehicular Technology, vol. 58, no. 8, pp. 4046–4063, 2009.

[11] M. Palkovic, P. Raghavan, M. Li, A. Dejonghe, L. Van Der Perre, and et al., "Future Software-Defined Radio Platforms and Mapping Flows," IEEE Signal Processing Magazine, vol. 27, no. 2, pp. 22–33, 2010.

[12] A.R. Macpherson, K. Townsend, and J.W. Haslett, “A 5GS/s Voltage-to-Time Converter in 90nm CMOS,” Proceedings of the 4th European Microwave Integrated Circuits Conference (EuMIC’09), pp. 254–257, 2009.

[13] G. Li, Y. Tousi, A. Hassibi, and E. Afshari, “Delay-Line-Based Analog-to-Digital Converters,” IEEE TCAS II: Express Briefs, vol. 56, no. 6, pp. 464–468, 2009.

[14] H. Pekau, A. Yousif, and J.W. Haslett, “A CMOS Integrated Linear Voltage-to-Pulse-Delay-Time Converter for time-based Analog-to-Digital Converters,” IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2373–2376, 2006.

[15] A.R. Macpherson, J.W. Haslett, and L. Belostotski, “A 5GS/s 4-bit Time-Based Single-Channel CMOS ADC for Radio Astronomy,” IEEE CICC, pp. 1–4, 2013.

[16] K. Abdelhalim, “Wireless Neural Recording and Stimulation SOCS for Monitoring and Treatment of Intractable Epilepsy” A thesis submitted in conformity with the requirements for the degree of degree of Doctor of Philosophy Graduate Department of Electrical and Computer Engineering University of Toronto, 2013.

[17] B. Razavi, Design of Analog CMOS Integrated Circuits. McGraw-Hill, 1999.

[18] T. Jiang, W. Liu, and P. Chiang, “a single-channel, 1.25-GS/s, 6bit, 6.08-mW asynchronous successive-approximation ADC with improved feedback delay in 40-nm CMOS,” IEEE JSSC, vol. 47, no. 10, pp. 2444– 2453, 2012.

[19] T. Sundstrom, C. SVENSSON, and A. Alvandpour, “a 2.4 GS/s, single-channel, 31.3 dB SNDR at Nyquist, Pipeline ADC in 65 nm CMOS,” IEEE JSSC, vol. 46, no. 7, pp. 1575–1584, 2011.

[20] C. Huang, C. Wang, and J. Wu, “A CMOS 6-Bit 16-GS/s Time-Interleaved ADC with Digital Background Calibration,” IEEE Symposium on VLSI Circuits, pp. 159–160, 2010.

[21] L. Brooks, and H. Lee, “a zero-crossing-based 8b 200MS/s pipelined ADC,” IEEE International Solid-State Circuits Conference (ISSCC), pp. 460–615, 2007.

[22] S. Naraghi, “Time-Based Analog to Digital Converters,” PhD thesis, The University of Michigan, 2009.

[23] T. Watanabe, T. Mizuno, and Y. Makino, “An All-Digital Analog-to-Digital Converter with 12-μV/LSB Using Moving-Average Filtering,” IEEE JSSC, vol. 38, no. 1, pp. 120–125, 2003.

[24] J. Cheon, and G. Han, “Noise Analysis and Simulation Method for a Single-Slope ADC with CDS in a CMOS Image Sensor,” IEEE TCAS I: Regular Papers, vol. 55, no. 10, pp. 2980–2987, 2008.

[25] R. Walden, “Analog to Digital Converter Survey and Analysis,” IEEE Journal on Selected Areas in Communications, vol. 17, no. 4, pp. 539–550, 1999.

[26] M. Ismail, and H. Mostafa, “a new design methodology for voltage-to-time converters (VTCs) circuits suitable for time-based analog-to-digital converters (T-ADC),” 27th IEEE International System-on-Chip Conference (SOCC), pp. 103–108, 2014.

[27] C. Ng, S. Chu, and S. Sun, “MIM Capacitor Integration for Mixed-Signal/RF Applications,” IEEE Transactions on Electron Devices, vol. 52, no. 7, pp. 1399–1409, 2005.

[28] P. Chiu, and M. Ker, “Metal-layer Capacitors in the 65 nm CMOS Process and the Application for Low-Leakage Power-Rail ESD Clamp Circuit,” Elsevier Microelectronics Reliability, vol. 54, no. 1, pp. 64–70, 2014.

[29] S.Q. Liang, Y.S. Yin, H.H. Deng, and X.L. Wang, “A mixed-signal calibration technology for the pipeline A/D converter,” 8th IEEE International Conference on ASIC, pp. 242–245, 2009.

[30] A. Mesgarani, I.T. Abougindia, and S.U. Ay, “A 6-bit 1.5GS/s pipelined binary search ADC with simplified clocking scheme,” 56th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 896–899, 2013.

[31] J. Yang, Y. Chen, H. Qian, Y. Wang, and R. Yue, “A 3.65 mW 5 bit 2GS/s flash ADC with built-in reference voltage in 65nm CMOS process,” IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), pp. 1–3, 2012.

[32] S. Rao, K. Reddy, B. Young, and P. Hanumolu “A Deterministic Digital Background Calibration Technique for VCO-Based ADCs,” IEEE JSSC, vol. 49, no. 4, pp. 950–960, 2014.

[33] S.K. Shin, J.C. Rudell, D.C. Daly, C.E. Munez, D.-Y. Chang, and et al., “A 12 bit 200 MS/s Zero-Crossing-Based Pipelined ADC With Early Sub-ADC Decision and Output Residue Background Calibration,” IEEE JSSC, vol. 49, no. 6, pp. 1366–1382, 2014.

[34] C.-C. Huang, C.-Y. Wang, and J.-T. Wu, “A CMOS 6-Bit 16-GS/s Time-Interleaved ADC Using Digital Background Calibration Techniques,” IEEE JSSC, vol. 46, no. 4, pp. 848–858, 2011.

[35] M. Wirnshofer, “Variation-Aware Adaptive Voltage Scaling for Digital CMOS Circuits,” Springer Series in Advanced Microelectronics, 1st ed., Springer Netherlands: Springer Science and Business Media, vol. 41, 2013.

[36] H. Mostafa, and Y. Ismail, “A Design-Oriented Timing Jitter/Skew Model in Voltage-to-Time Converter Circuits,” Analog Integrated Circuits and Signal Processing, Springer, vol. 82, issue 1, pp. 309-321, 2015.

[37] M.S. Gupta, J.A. Rivers, P. Bose, W. Gu-Yeon, and D. Brooks, “Tribeca: Design for PVT variations with local recovery and fine-grained adaptation,” Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), pp. 435-446, 2009.

[38] S. Pasricha, Y. Park, N. Dutt, and F. J. Kurdahi, “System-level PVT variation-aware power exploration of on-chip communication architectures,” ACM Transactions on Design Automation of Electronic Systems (TODAES), vol. 14, no. 2, pp. 1–25, 2009.

[39] J. Kil, G. Jie, and C.H. Kim, “A high-speed variation-tolerant interconnect technique for sub-threshold circuits using capacitive boosting,” IEEE International Symposium on Low Power Electronics and Design, pp. 67-72, 2006.

[40] R. Kumar, and V. Kursun, “Impact of temperature fluctuations on circuit characteristics in 180nm and 65nm CMOS technologies,” IEEE ISCAS, pp. 1-4, 2006.

[41] B. Minch, “Low-Voltage Wilson Current Mirrors in CMOS,” IEEE ISCAS, pp. 2220–2223, 2007.

[42] R. Baker, CMOS: Circuit Design, Layout, and Simulation. John Wiley & Sons, 2nd ed., 2005.

[43] A. El-Bayoumi, H. Mostafa, and A.M. Soliman, “A New Highly-Linear Highly-Sensitive Differential Voltage-to-Time Converter Circuit in CMOS 65nm Technology,” IEEE ISCAS'2015, pp. 1262-1265, 2015.

[44] A. El-Bayoumi, H. Mostafa, and A.M. Soliman, “A New 65nm-CMOS 1V 8GS/s 9-bit Differential Voltage-Controlled Delay Unit Utilized for a Time-Based Analog-to-Digital Converter Circuit,” IEEE ICM, pp. 1-4, 2015.

Appendix A: Design Parameters

A.1 Differential falling VTC design parameters at 65-nm CMOS

Table A.1 shows the design parameters of a single core of the differential falling VTC circuit which is discussed in Section 3.2. These parameters are used for TSMC-type transistors at a 65-nm CMOS technology platform.

Table A.1: Design parameters of the core of the differential falling VTC circuit.

Parameter	Value
Pa1 width	2.4 µm
Pa1 length	80 nm
Na3 width	1.2 µm
Na3 length	80 nm
Na2 width	1.44 µm
Na2 length	80 nm
Na1 width	120 nm
Na1 length	80 nm
C_L	30 ff
V_{CONST}	600 mv

A.2 Differential rising VTC design parameters at 65-nm CMOS

Table A.2 shows the design parameters of a single core of the differential rising VTC circuit which is discussed in Section 3.3. These parameters are used for TSMC-type transistors at a 65-nm CMOS technology platform.

Table A.2: Design parameters of the core of the differential rising VTC circuit.

Parameter	Value
Pb3 width	120 nm
Pb3 length	80 nm
Pb2 width	240 nm
Pb2 length	80 nm
Pb1 width	2.4 µm
Pb1 length	80 nm
Nb1 width	1.2 µm
Nb1 length	80 nm
C_L	30 ff
V_{CONST}	600 mv

A.3 Differential VTC methodology design parameters at 65-nm CMOS

Table A.3 shows the design parameters of the XNOR gate of the differential VTC methodology circuit which is discussed in Section 3.4. The pull-down block and the pull-up block parameters are represented in Table A.1 and Table A.2, respectively. Table A.4 shows the output inverter parameters of the single core of the differential VTC methodology circuit. The delay line consists of 11 inverters of length 60 nm. In each inverter, the pMOS width equals to 240 nm, while the nMOS width equals to 120 nm. These parameters are used for TSMC-type transistors at a 65-nm CMOS technology platform.

Table A.3: Design parameters of the XNOR gate of the single core of the differential VTC methodology circuit.

Parameter	Transistor Width	Transistor Length
M1	1.2 µm	60 nm
M2	0.6 µm	60 nm
M3	0.6 µm	60 nm
M4	1.2 µm	60 nm
M5	1.2 µm	60 nm
M6	0.6 µm	60 nm
M7	0.6 µm	60 nm
M8	1.2 µm	60 nm

Table A.4: Design parameters of the output inverter of the single core of the differential VTC methodology circuit.

Parameter	Transistor Width	Transistor Length
pMOS	2 µm	60 nm
nMOS	1 µm	60 nm

A.4 Modified Differential VTC methodology design parameters at 65-nm CMOS

Table A.5 shows the design parameters of the XNOR gate as well as the pull-up and pull-down blocks capacitor load of the differential VTC methodology circuit which is discussed in Section 3.5. Other design blocks parameters have been discussed in Section A1, A2 and A3. These parameters are used for TSMC-type transistors at a 65-nm CMOS technology platform. Table A.6 shows the design parameters of the calibration circuit on the different PVT variations.

Table A.5: Design parameters of the modified differential VTC methodology circuit.

Parameter	Value
Large-sized inverter pMOS width	3 µm
Large-sized inverter pMOS length	60 nm
Large-sized inverter nMOS width	1.5 µm
Large-sized inverter nMOS width	60 nm
C_L	155.4 ff

Table A.6: Design parameters of the set of the calibration circuits on PVT variations.

Tolerated variation	Output DC Bias Voltage	Parameter	Transistor Width	Transistor Length
TT state	0.75 V	M1	0.215 µm	0.14 µm
		M2	0.12 µm	0.395 µm
SS corner	0.55 V	M1	0.12 µm	0.12 µm
		M2	0.545 µm	0.12 µm
FF corner	0.74 V	M1	0.21 µm	0.17 µm
		M2	0.14 µm	0.4 µm
1.1 V	0.85 V	M1	1 µm	1.3 µm
		M2	0.12 µm	0.62 µm
1.3 V	1.03 V	M1	0.7 µm	1 µm
		M2	0.12 µm	0.34 µm
-40 ^{O}C	0.82 V	M1	0.315 µm	0.14 µm
		M2	0.12 µm	0.11 µm
85 ^{O}C	0.8 V	M1	0.7 µm	0.6 µm
		M2	0.12 µm	0.27 µm
120 ^{O}C	0.79 V	M1	0.5 µm	1.02 µm
		M2	0.12 µm	0.515 µm

A.5 Differential high-speed VTC design parameters at 65-nm CMOS

Table A.7 shows the design parameters of the single core of the differential high-speed VTC circuit which is discussed in Section 3.6. These parameters are used for TSMC-type transistors at a 65-nm CMOS technology platform.

Table A.7: Design parameters of the single core of the differential high-speed VTC circuit.

Parameter	Transistor Width	Transistor Length
M1	20 µm	60 nm
M2	20 µm	60 nm
M3	6.67 µm	0.12 µm
M4	6.67 µm	60 nm
M5	6.67 µm	60 nm
M6	3.33 µm	60 nm
M7	3.33 µm	60 nm
M8	3.33 µm	60 nm
M9	8.33 µm	60 nm
M10	8.33 µm	60 nm
M11	8.33 µm	60 nm
M12	8.33 µm	60 nm
M13	4.3 µm	60 nm
M14	0.335 µm	60 nm
M15	0.67 µm	60 nm
M16	0.67 µm	60 nm
M17	0.335 µm	60 nm
M18	3.33 µm	60 nm
M19	3.33 µm	60 nm
M20	0.5 µm	60 nm

Table A.8: Design parameters of the single core of the 1st proposed differential VTC circuit.

Parameter	Transistor Width	Transistor Length
Pa1	4.8 µm	0.12 µm
Na3	2.4 µm	0.12 µm
Na2	2.88 µm	0.12 µm
Na1	0.24 µm	0.12 µm
Pb3	0.24 µm	0.12 µm
Pb2	0.48 µm	0.12 µm
Pb1	4.8 µm	0.12 µm
Nb1	2.4 µm	0.12 µm
Inverter pMOS	6 µm	0.12 µm
Inverter nMOS	3 µm	0.12 µm
Output inverter pMOS	4 µm	0.13 µm
Output inverter nMOS	2 µm	0.13 µm
M1	2.4 µm	0.13 µm
M2	1.2 µm	0.13 µm
M3	1.2 µm	0.13 µm
M4	2.4 µm	0.13 µm
M5	2.4 µm	0.13 µm
M6	1.2 µm	0.13 µm
M7	1.2 µm	0.13 µm
M8	2.4 µm	0.13 µm

Table A.9: Design parameters of the set of the calibration circuits on PVT variations.

Tolerated variation	Output DC Bias Voltage	Parameter	Transistor Width	Transistor Length
TT state	0.6 V	M1	0.2 µm	0.13 µm
		M2	0.12 µm	0.4 µm
SS corner	0.44 V	M1	0.13 µm	0.13 µm
		M2	0.59 µm	0.13 µm
FF corner	0.6 V	M1	0.17 µm	0.13 µm
		M2	0.11 µm	0.32 µm
		M2	0.2 µm	0.13 µm

A.6 Differential VTC methodology design parameters at 130-nm CMOS

Table A.8 shows the design parameters of the migrated single core of the 1st proposed VTC circuit which is discussed in Section 4.2. It includes the parameters of the falling VTC circuit, the rising VTC circuit, the delay inverter, the output inverter and the XNOR gate. These parameters are used for UMC-type transistors at a 130-nm CMOS technology platform. Table A.9 shows the parameters of the modified calibration circuit that tolerates corners variations for the 1st proposed design implemented at 130nm CMOS.

A.7 Differential high-speed VTC design parameters at 130-nm CMOS

Table A.10 shows the design parameters of the migrated single core of the 2nd proposed VTC circuit which is discussed in Section 4.3. These parameters are used for UMC-type transistors at a 130-nm CMOS technology platform.

Parameter	Transistor Width	Transistor Length
M1	42 µm	0.13 µm
M2	42 µm	0.13 µm
M3	14 µm	0.26 µm
M4	14 µm	0.13 µm
M5	14 µm	0.13 µm
M6	7 µm	0.13 µm
M7	7 µm	0.13 µm
M8	7 µm	0.13 µm
M9	19.5 µm	0.13 µm
M10	19.5 µm	0.13 µm
M11	19.5 µm	0.13 µm
M12	19.5 µm	0.13 µm
M13	8.6 µm	0.13 µm
M14	0.7 µm	0.13 µm
M15	1.4 µm	0.13 µm
M16	1.4 µm	0.13 µm
M17	0.7 µm	0.13 µm
M18	7 µm	0.13 µm
M19	7 µm	0.13 µm
M20	1 µm	0.13 µm

Table A.10: Design parameters of the single core of the 2nd proposed VTC circuit.

Appendix B: Simulations Methods

B.1 Linearity check

The linearity graph is simulated by Cadence Virtuoso and MATLAB tools. You should sweep the input voltage over a range of frequencies. This produces the corresponding delay for each swept input voltage points. These values are the inputs of the MATLAB which calculates the linearity error. To have the delay points, the Cadence should be configured as in the following steps.

First, after designing the VTC circuit, the amplitude of the input voltage should be set as a variable such as: the input amplitude of the 1st single-core is set to DC offset + $V_{IN}/2$, while the amplitude of the 2nd single-core is set to DC offset - $V_{IN}/2$. The linear range shall be varied on the DC offset with the range $-V_{IN}/2 : V_{IN}/2$.

Second, From "Launch" icon, choose Analog Design Environment (ADE) L. On the appeared new window, choose the analysis type to add DC analysis and transient analysis. The DC analysis makes sure that all DC operating points of each device is based on your assumptions as shown in Figure B.1. In the transient analysis shown in Figure B.2, the stop time should at least covers a sample of the highest period designed circuit (it is better to be larger than the sampling period multiplied by an integer number).

Third, to add the design variables on the Virtuoso ADE, choose "Variables". From

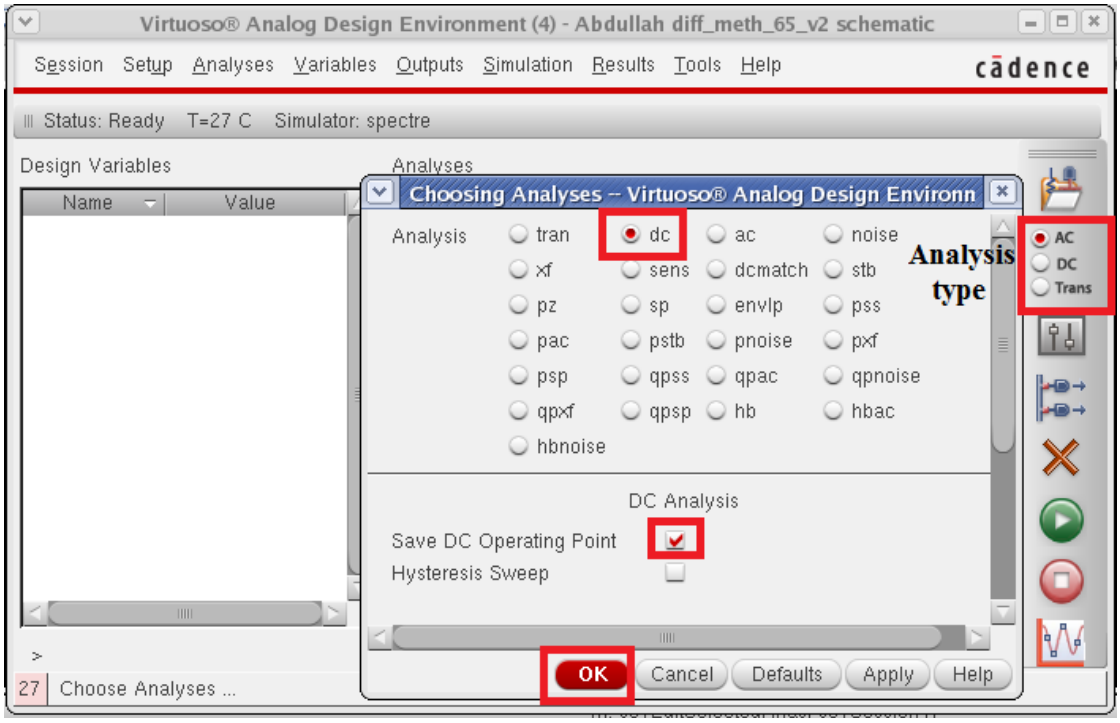


Figure B.1: Choosing the DC analysis on Virtuoso Analog Design Environment.

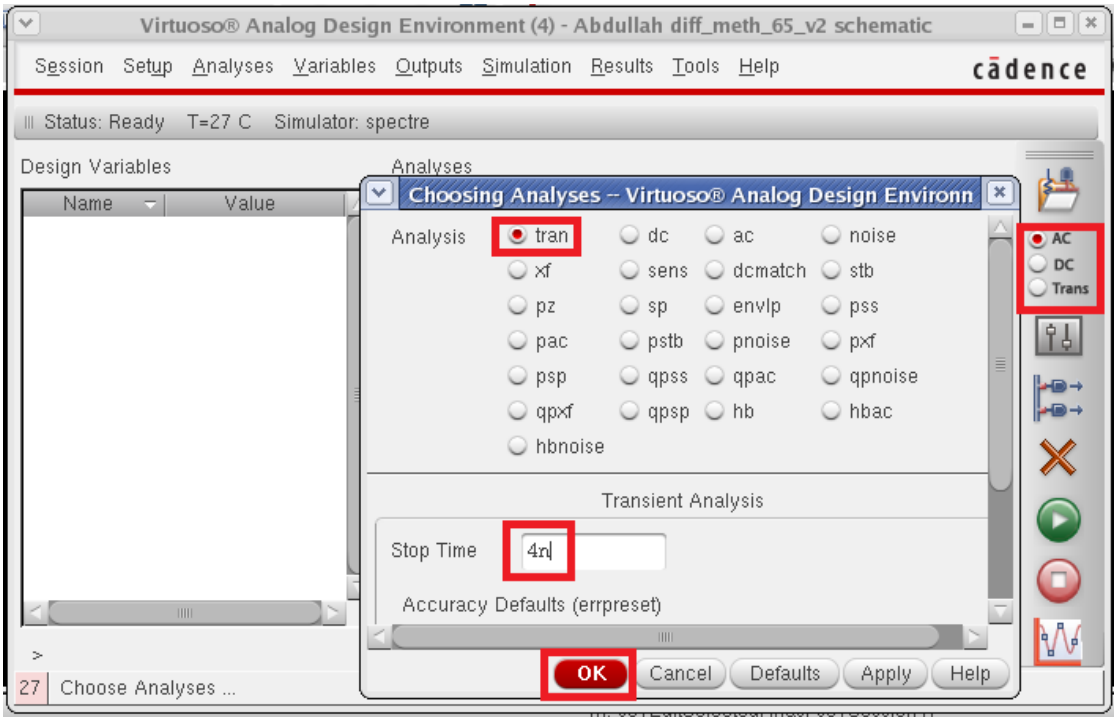


Figure B.2: Choosing the transient analysis on Virtuoso ADE.

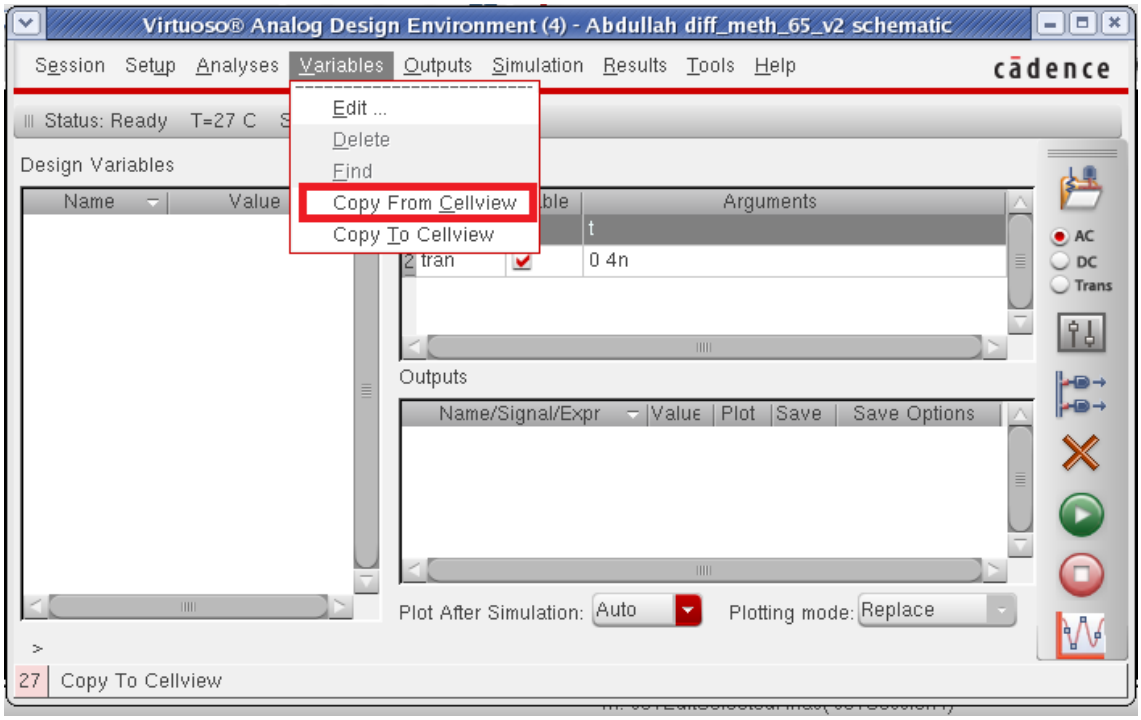


Figure B.3: Adding the design variables on Virtuoso ADE.

the drop down menu, choose "Copy Form Cellview" as shown in Figure B.3. Then, you

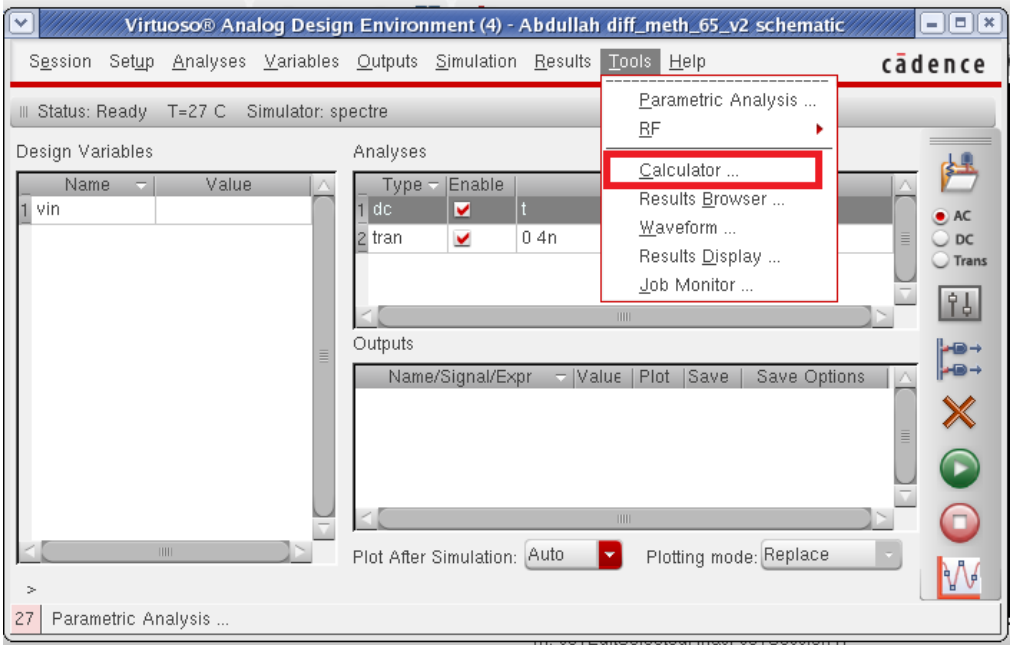


Figure B.4: Opening the Virtuoso Calculator.

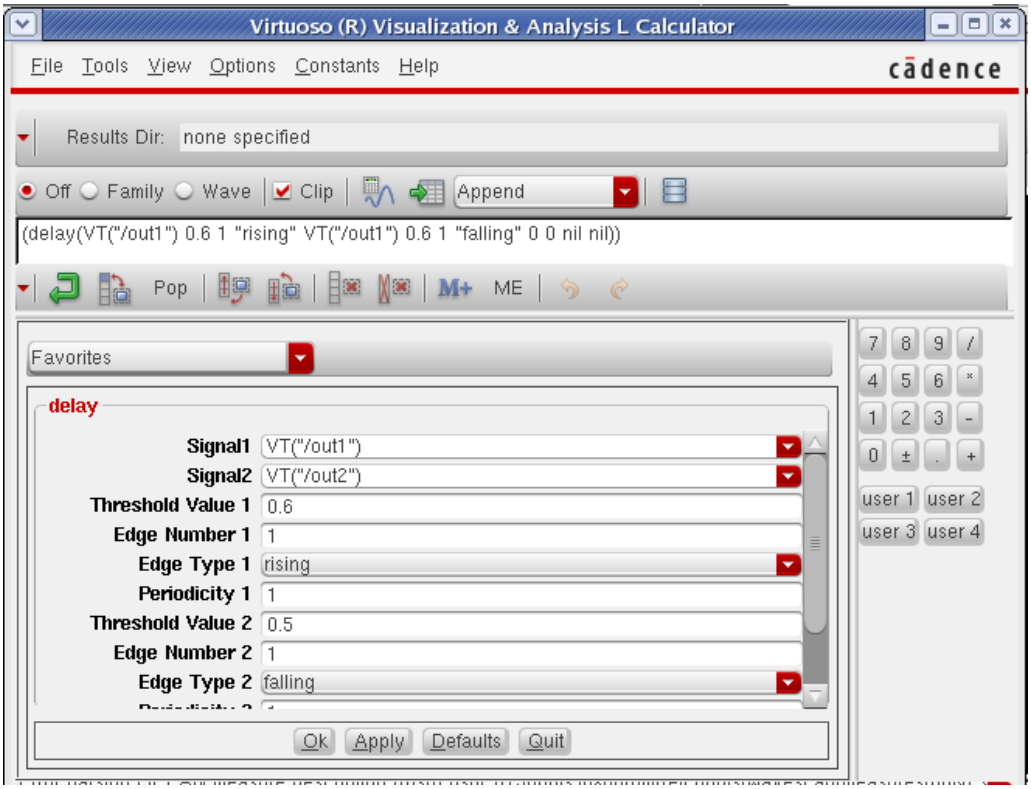


Figure B.5: Delay equation on Virtuoso Calculator.

should calculate the needed delay equation by opening the Virtuoso Calculator as shown in Figure B.4. Figure B.5 calculates the delay equation by typing its main parameters. For a PWM VTC circuit "Signal1" is the rising edge of the VTC output voltage, while "Signal2" is the falling edge the VTC output voltage. For a PPM VTC circuit "Signal2" should be calculated from the input clock voltage.

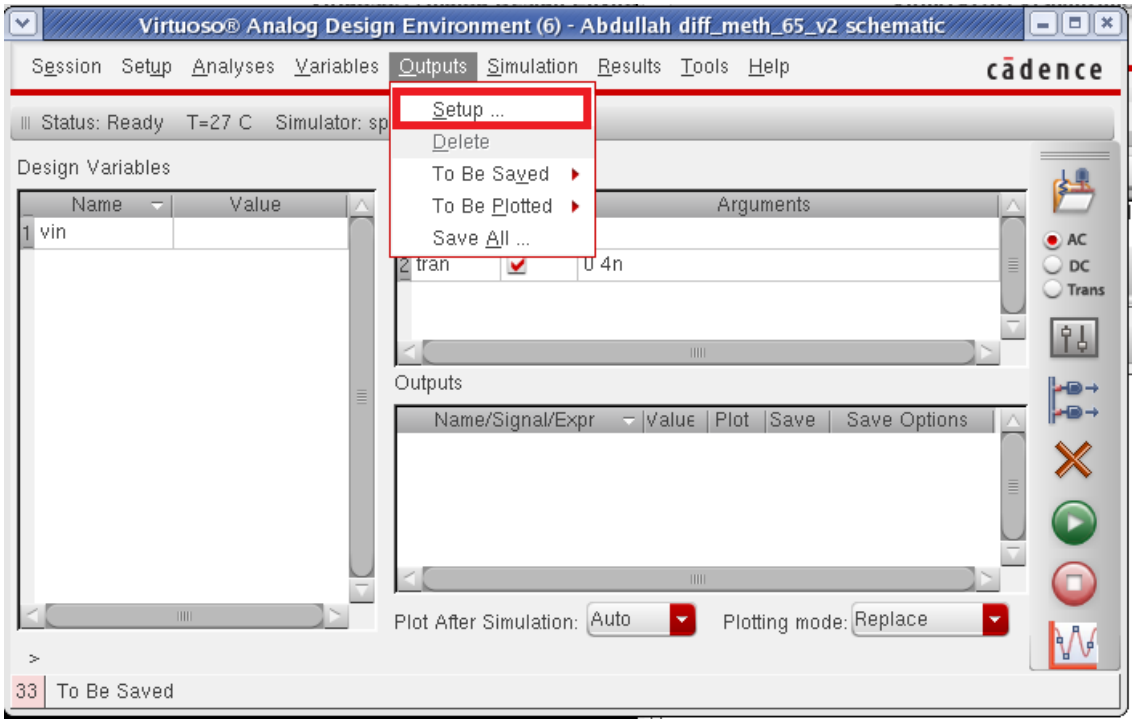


Figure B.6: Outputs on Virtuoso ADE.

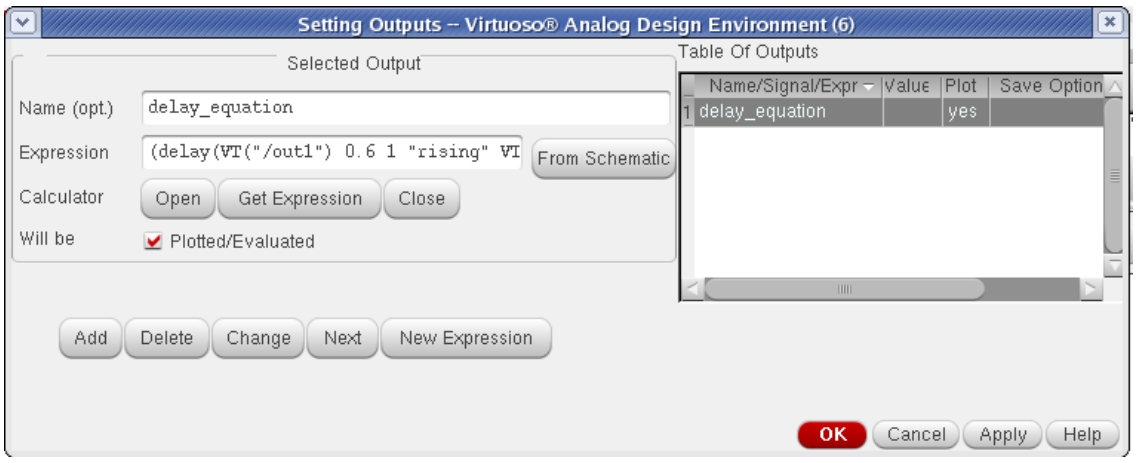


Figure B.7: Outputting the Delay equation on Virtuoso ADE.

The calculated delay equation is for a single-core, so you should do the same for the 2nd core to calculate the overall delay equation. Then, to add the delay equation to output, you should press on "Outputs" from Virtuoso ADE and "Setup" from the appeared drop down menu as shown in Figure B.6. Figure B.7 shows the new window where we should press on "Get expression" to get the needed equation to be outputted from the Calculator. Then, press on "ADD" and "OK".

The next step is to sweep the input voltage by pressing on "Tools" and "Parametric Analysis from the appeared drop down menu as shown in Figure B.8. Figure B.9 shows

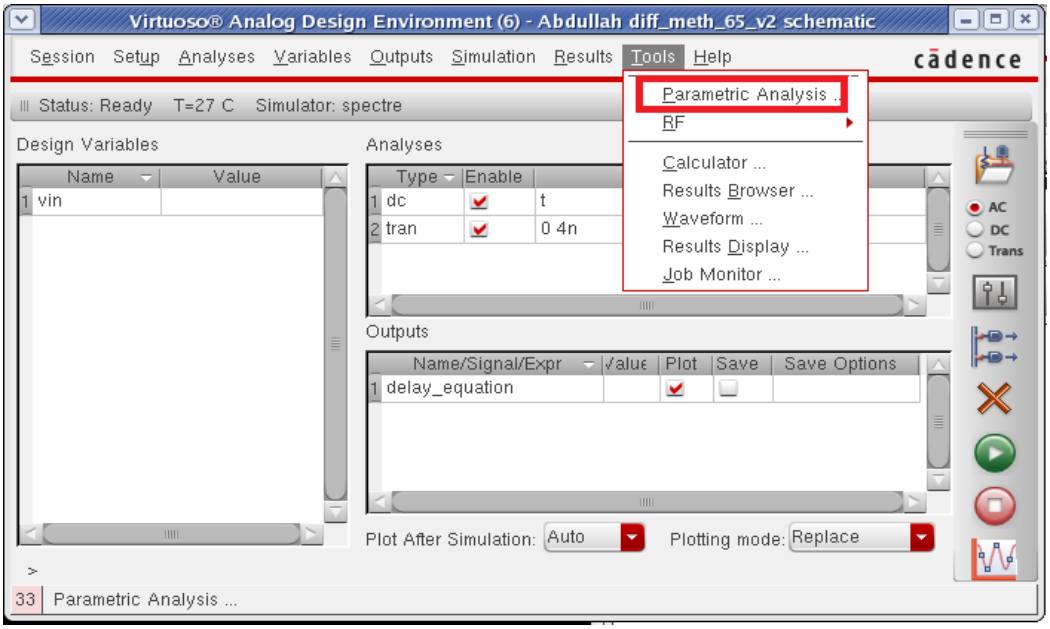


Figure B.8: Parametric Analysis on Virtuoso ADE.

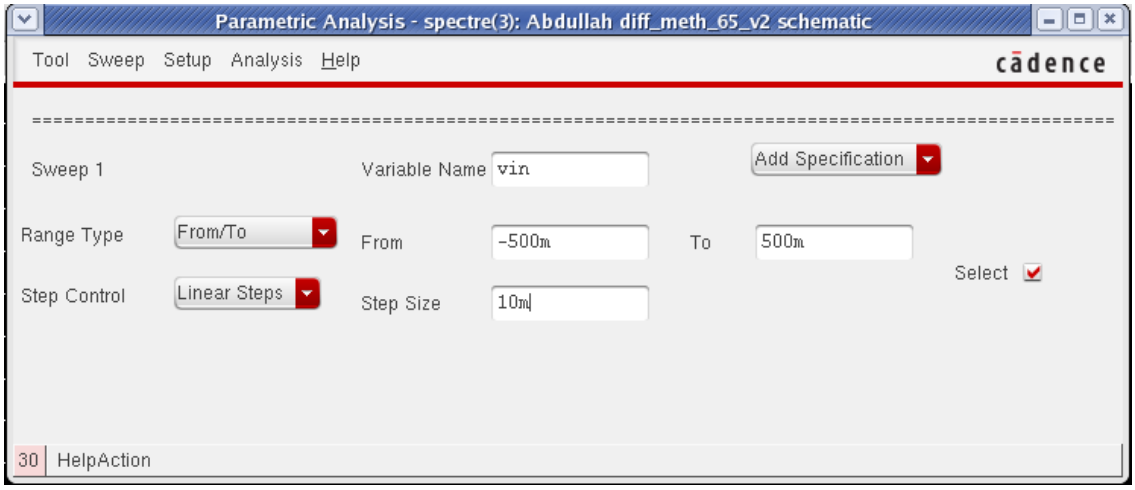


Figure B.9: Sweeping the input voltage.

the range of sweeping the variable where the step-type should be linear with possibly minimum step size. Finally, press on "Analyze" and "Start" from the drop down menu, as shown in Figure B.10. The delay versus voltage graph appears and iteration method should be applied to get the exact linear range as shown in Figure B.11.

Now, we need to calculate the linearity error check. The 1st step is to save all graphed points by pressing on the Calculator icon as marked on Figure B.11. Figure B.12 shows the new appeared Calculator window with the needed equation to save its all simulated

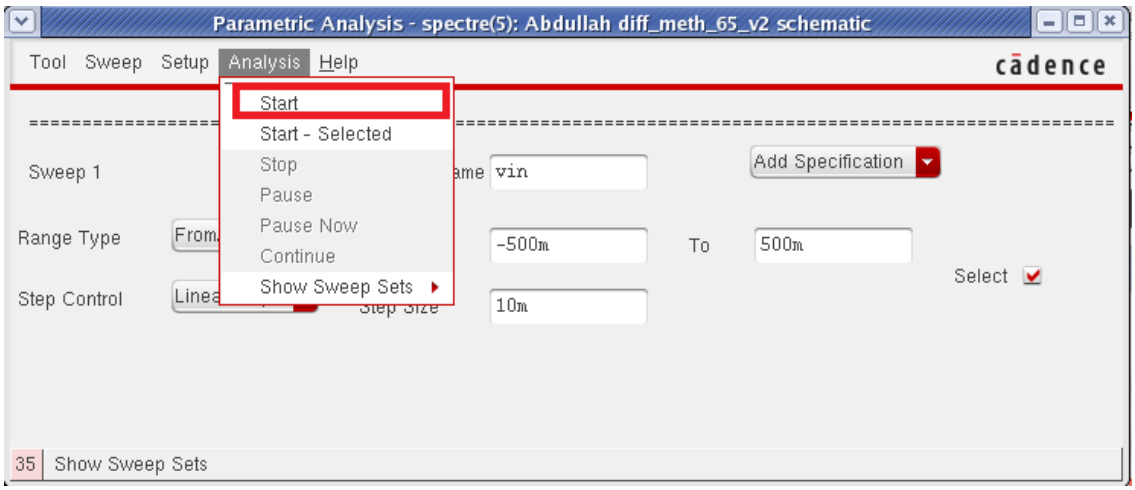


Figure B.10: Starting drawing the delay equation.

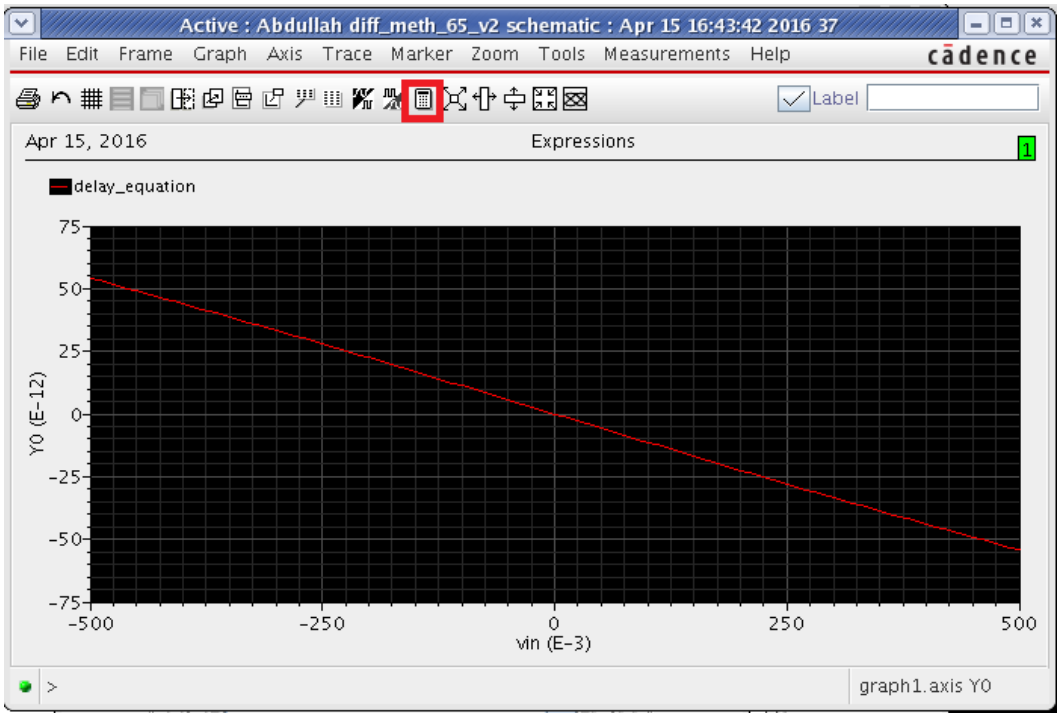


Figure B.11: The VTC dynamic linear range.

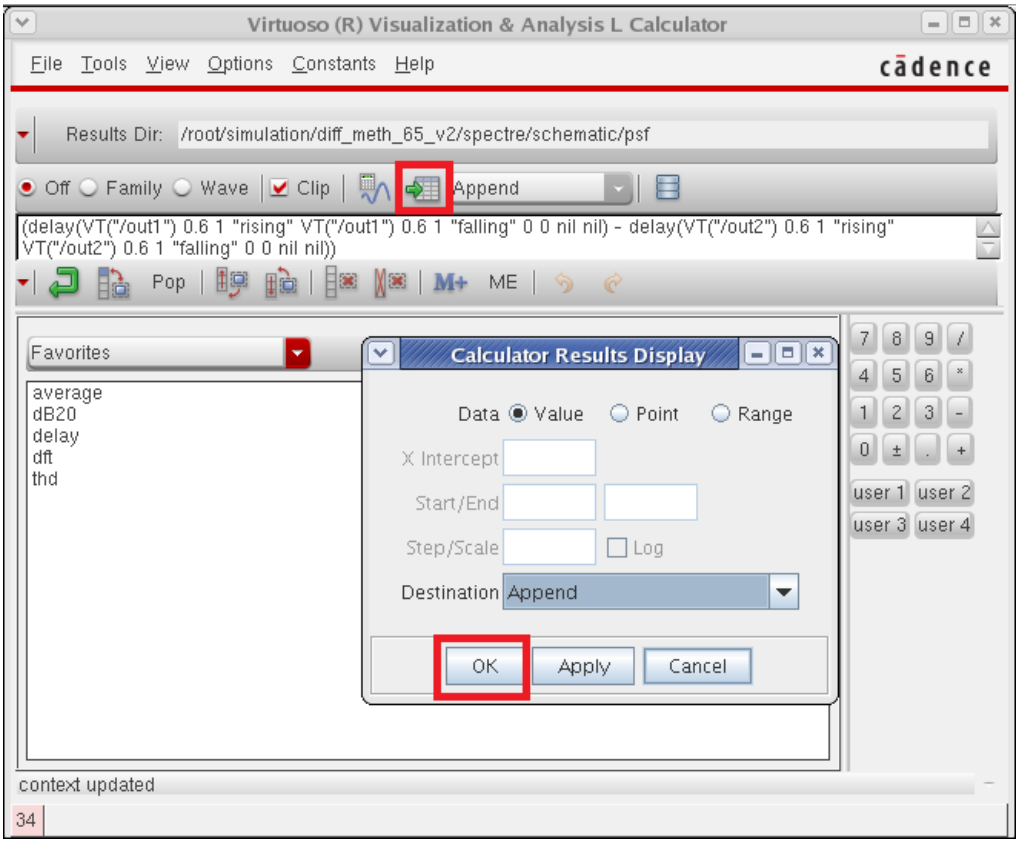


Figure B.12: Delay buffer calculation.

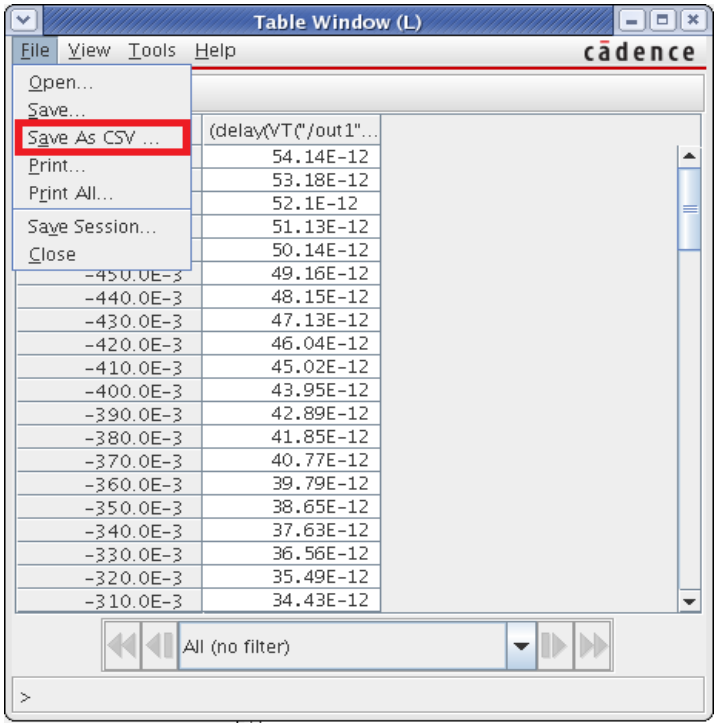


Figure B.13: CSV saved file.

points. You should press on the icon "Evaluate the buffer and display the results in a table" and press on "OK" at the new appeared window. Figure B.13 shows the saved file on extension CSV. You should save this file on your workstation as these points will be an input to a MATLAB code to calculate the linearity error.

The MATLAB code which figures the linear line curve fitting and the linearity error is as following:

```
% imported Delay Vs Input Voltage .csv file from cadence
%n: order for curve fitting
clc;
clear all;
n=1; % to be linear
axis=csvread('CadenceDelayOutput',1.0)
x=axis(:,1);
y=axis(:,2);
axis_approx=polyfit(x,y,n);
axis_approx_n=polyval(axis_approx,x);
figure;
hold on;
plot(x,y,'+-');
plot(x,axis_approx_n,'g');
hold off
grid;
xlabel('Vin in volts');
ylabel('delay in ps');
title('pulse width Vs input voltage');
SetLocation=legend('Differenial delay', 'Differenial delay approx');
set(SetLocation, 'Location', 'NorthEast')
set(SetLocation, 'Interpreter', 'None')
linearity_error=((axis_approx_n-y)./axis_approx(1))*100;
figure;
hold on;
plot(x,smooth(linearity_error));
hold off;
grid;
xlabel('Vin in volts');
ylabel('error in %');
title('linearity Vs input voltage');
```

After running this code, it asks for the destination of the saved CSV file. It outputs graphs such as in Figure 4.2 and Figure 4.4.

B.2 Circuit sensitivity

As mentioned before that the circuit sensitivity is the delay versus input voltage slope, after generating the delay graph as in Figure B.11, the slope could be calculated from the graph itself. You should press on "Trace" icon and "Delta Cursor" from the drop down menu as shown in Figure B.14. Now, you can move the 1st cursor at the 1st point, while the 2nd cursor at the last one. The slope will be calculated automatically as shown in Figure B.14.

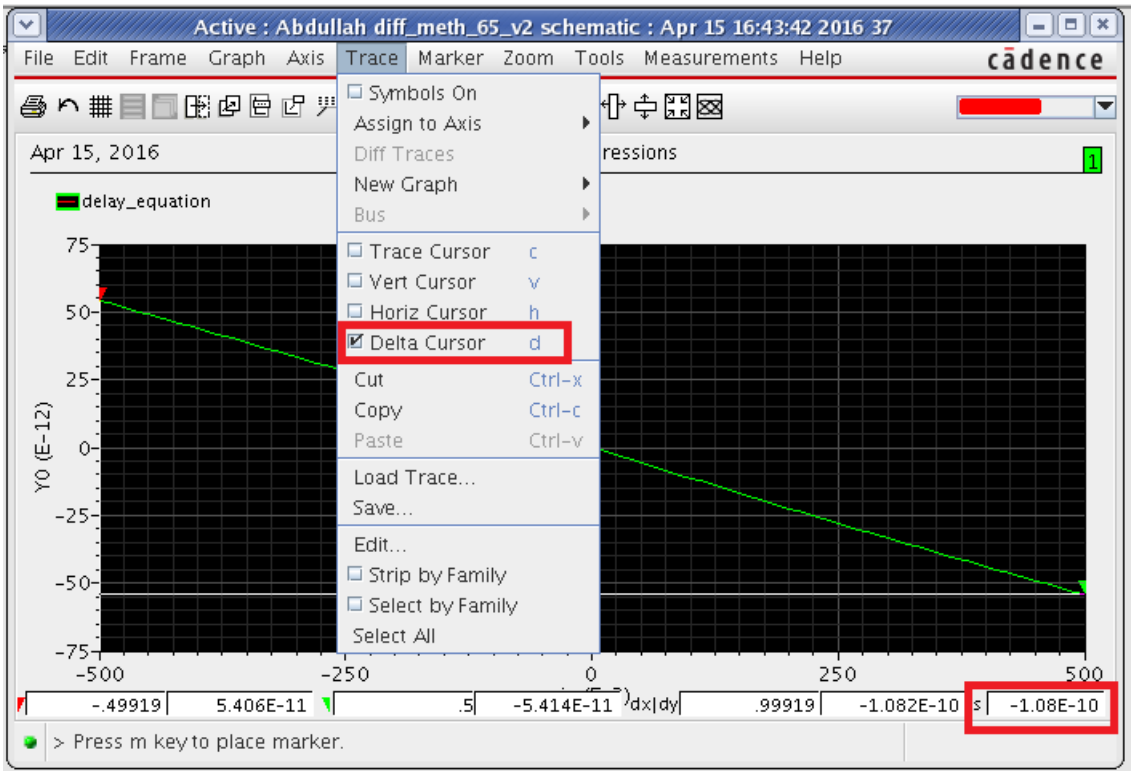


Figure B.14: Circuit sensitivity.

B.3 Total Harmonic Distortion

With the same procedure followed in calculating the linearity, we can calculate the THD but with some changes. The 1st change is to change the DC voltage source with a sinusoidal voltage source. Whereas its frequency is the input frequency which should equal to a factor from the sampling frequency. In additions, the source amplitude should be half of the dynamic range DC bias ± V_{IN}/2. You should consider a larger stop time of the transient analysis (i.e. to consider 1024 × the sampling period). The 2nd change is to add a new equation to the Calculator as the THD is based on the Discrete Fourier Transform (DFT) which figures all related signal harmonics over frequencies. Figure B.15 shows the Discrete Fourier Transform (DFT) equation on the Virtuoso Calculator. Then, this equation should be saved in the Output Setup and the input voltage should be swept to output a graph of the DFT equation. The drawn points should be saved as CSV

to be used as inputs to a MATLAB code. This code calculates the overall THD as following:

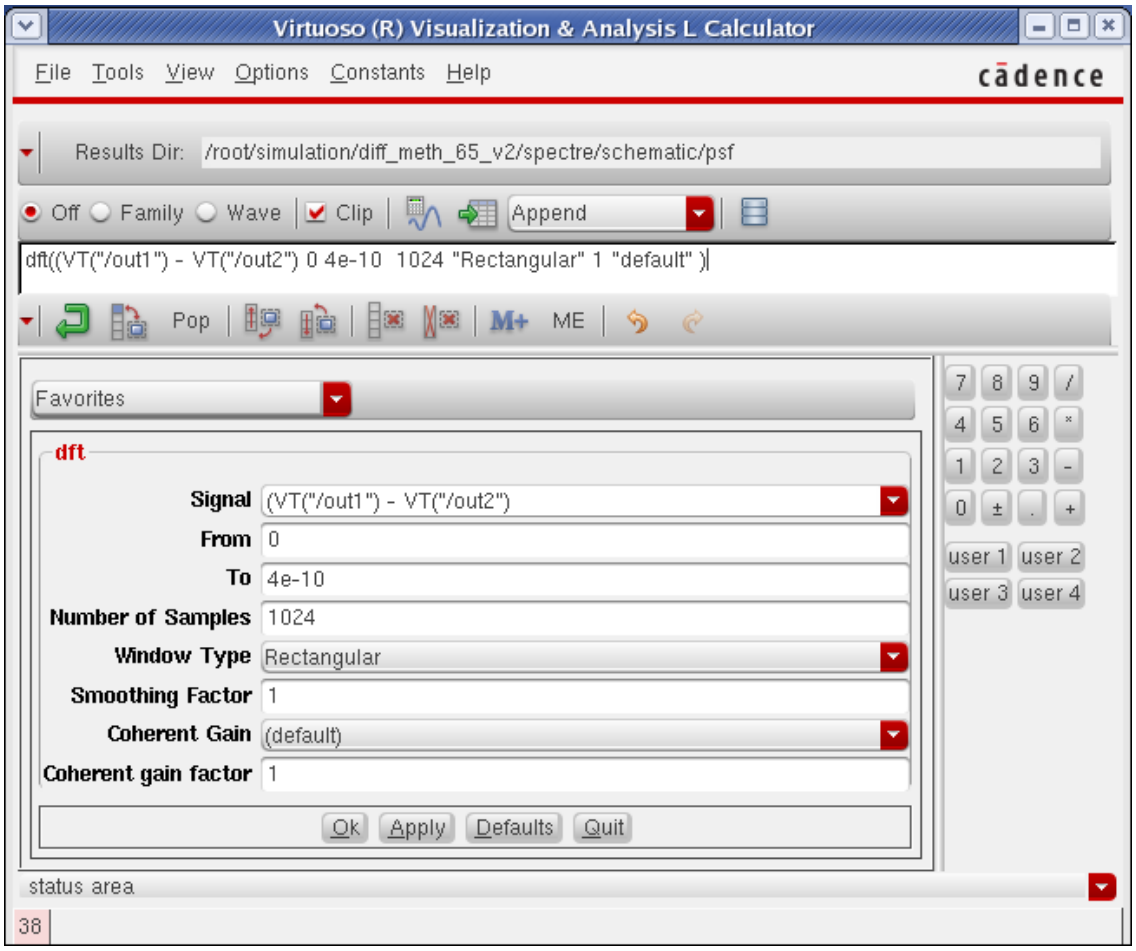


Figure B.15: DFT on Virtuoso Calculator.

```
% imported DFT .csv file from cadence
clc;
clear all;
dft=csvread('CadenceTHDOutput',1.0)
freq=dft(:,1);
amplitude=dft(:,2);
amplitude_total=0;
for iteration=3:1:length(amplitude)
        amplitude_total=amplitude_total+amplitude(iteration)^2;
end
harmonics=sqrt(amplitude_total);
THD=20*log(harmonics/amplitude(2))
```

B.4 Power consumption

To calculate the power consumption, you should save the components DC operating point in the DC analysis as in Figure B.1. Moreover, the transient analysis, as shown in Figure B.2, should be operated with a stop time much larger than the sampling frequency (i.e. the stop time is preferred to equal to at least 1000 × the sampling period, so as to

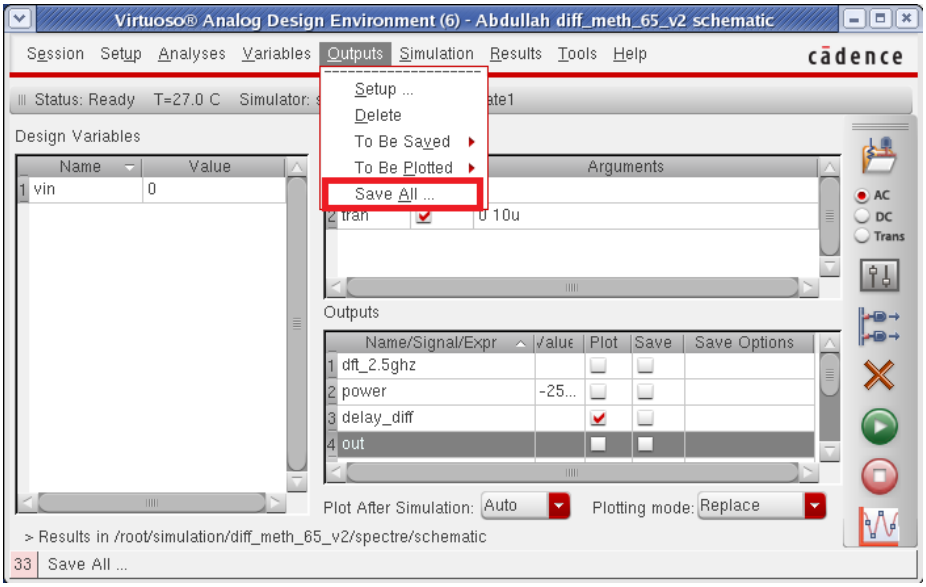


Figure B.16: Power configuration on Virtuoso ADE.

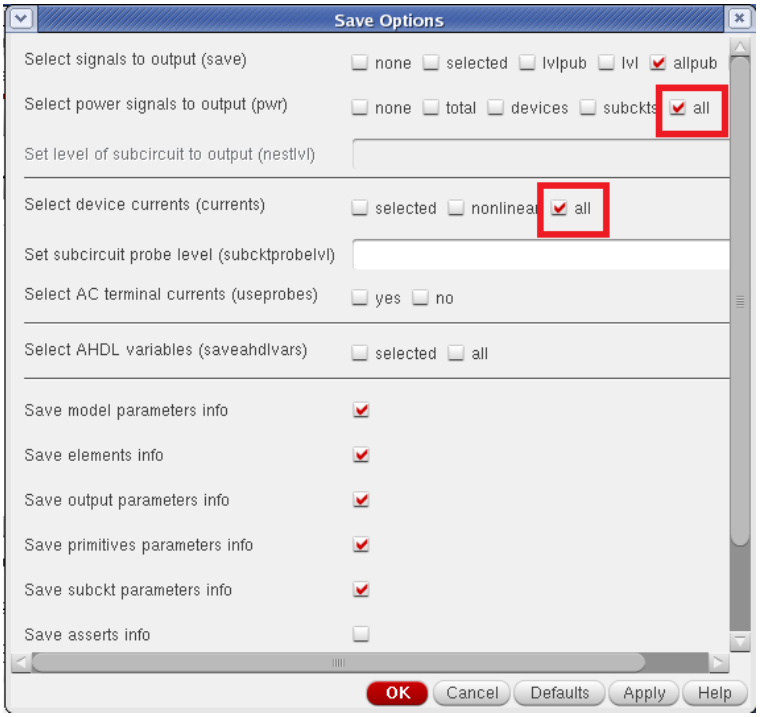


Figure B.17: Current configuration on Virtuoso ADE.

have an accurate consumed power value). To set the power configuration on Virtuoso ADE, press on "Outputs" and "Save All" from the appeared drop down menu as shown in Figure B.16. A new window appears, as shown in Figure B.17, where you should mark on the highlighted power and current to be able to measure them. Now you should calculate the power equation on the Virtuoso Calculator which equals to the average value of the supply voltage value multiplied by the supply current value as shown in Figure B.18.

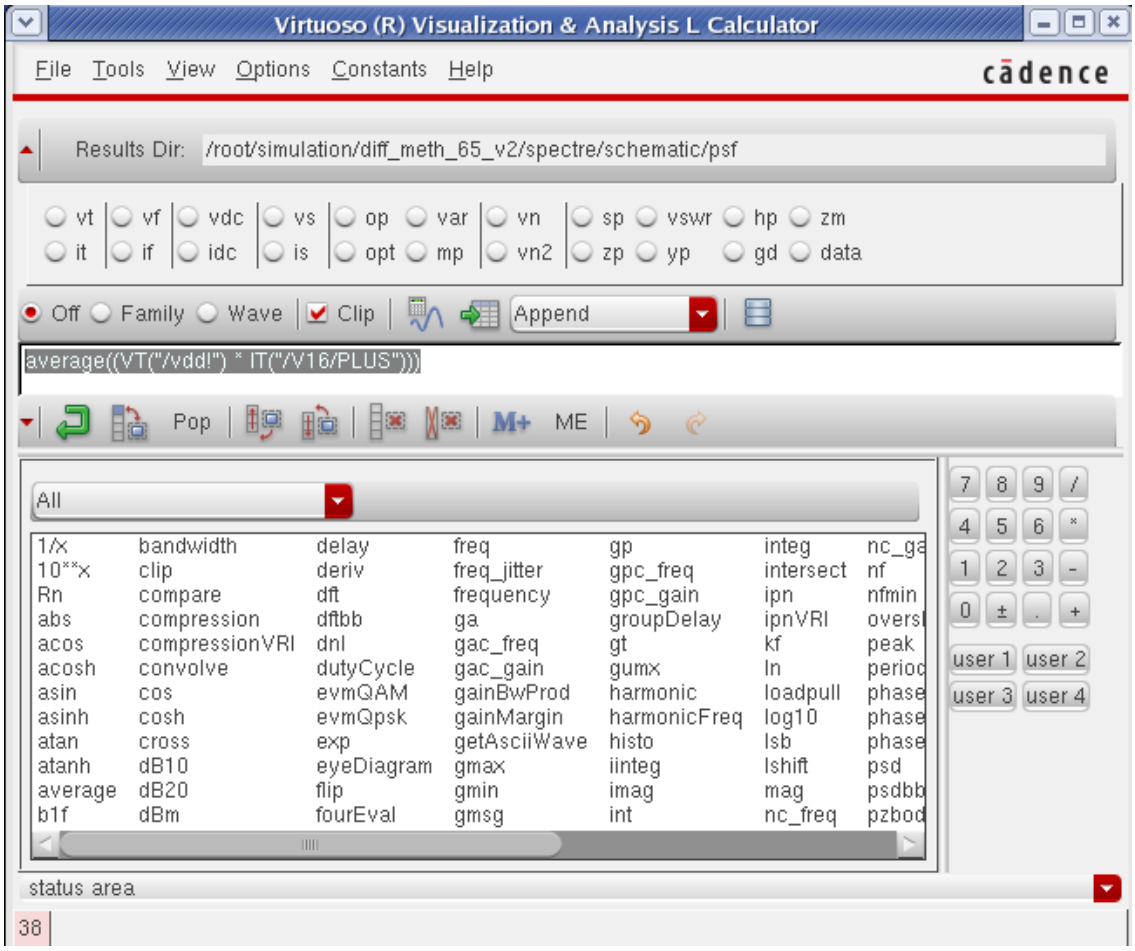


Figure B.18: Power equation on Virtuoso Calculator.

B.5 Noise Figure

To output the overall circuit noise versus the frequency, noise analysis should be chosen from the Analysis icon on Virtuoso ADE. Then, its configuration should be implemented for a single core design as shown in Figure B.19 where the noise is calculated from a single-core output voltage and the ground. Then, the noise equation should be outputted on Virtuoso ADE as shown in Figure B.20. Whereas, the overall output referred noise is doubled to measure the overall differential output referred noise. Then, sweeping the input voltage generates the noise figure as in Figure 4.6.

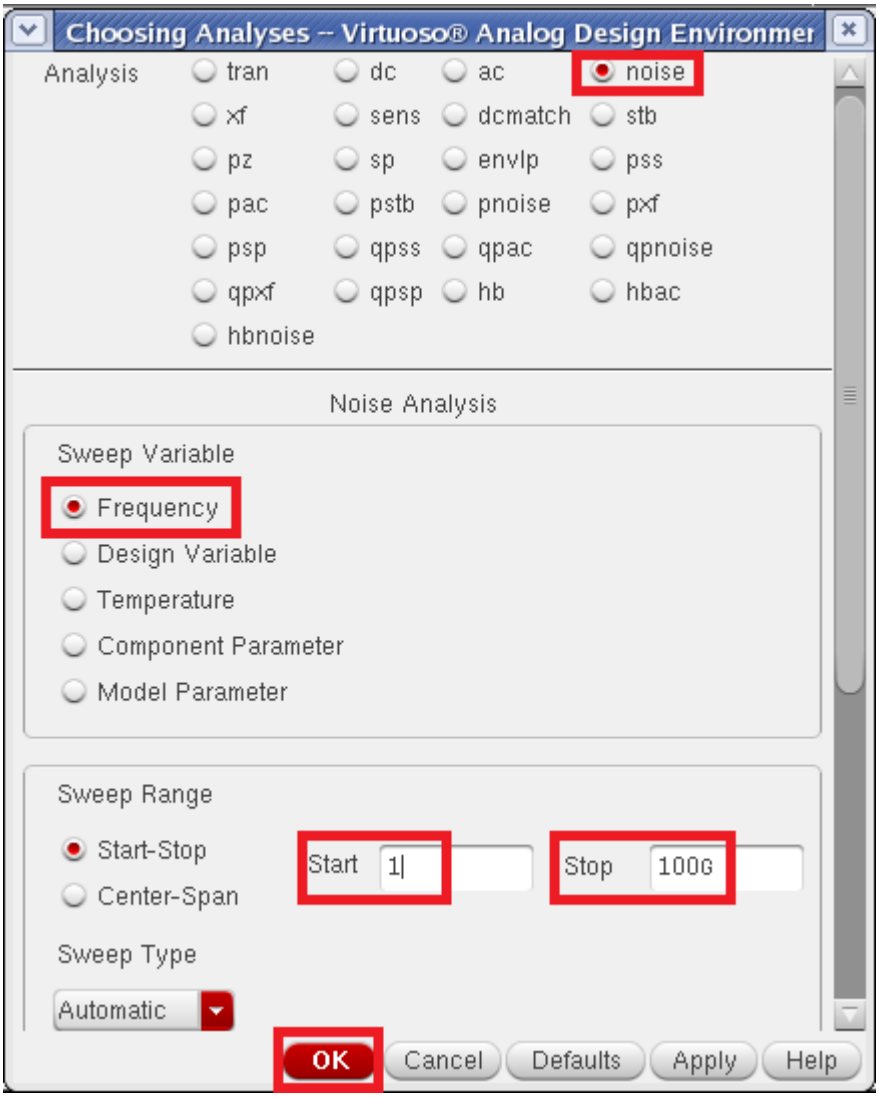


Figure B.19: Noise analysis configuration on Virtuoso ADE.

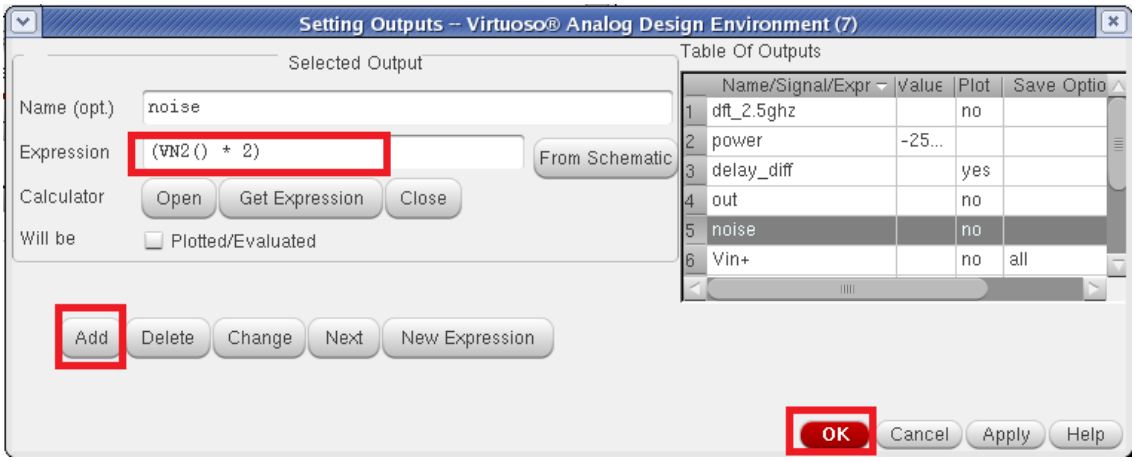


Figure B.20: Noise expression on Virtuoso ADE.

B.6 Effective Number of Bits

The ENOB is measured with the same procedure followed by calculating the THD. First, we should configure the transient analysis to have about 1024 samples by typing the value of 1024 × the sampling period on the stop time. Second, on Virtuoso Calculator we should generate the output voltage of the proposed design and add it to the "Outputs" setup on Virtuoso ADE as illustrated before. Furthermore, the input voltage source should be a sinusoidal one.

By sweeping the input voltage with the proper dynamic range, the output graph appears where you should save it as CSV. This file will be the input of a MATLAB code which calculate at first the TADC output code words. It needs the average value of the PPM/PWM VTC pulse to determine the decision of whether the pulse acts as '0' or '1'. This could be calculated by inputting the lowest and highest applicable input voltages based on the dynamic range and we shall measure the transient output pulse.

After generating the digital words of a TADC block, another code used as DAC to get the originals analog amplitudes. This is maintained to calculate the difference between the original applied signal and the analog signal after passing by a TADC and DAC, respectively. In the MATLAB code, you shall type the F_I, F_B and F_S with their aimed values. The MATLAB code with the used functions are as following:

%%%%%%%%%%%%%%%main code%%%%%%%%%%%%%%%%%%

```
clc;
clear all;
matrix=csvread('VTC_output.csv',1,0); %getting the VTC output data from Cadence
time =matrix(:,1)؛
out =matrix(:,2)؛
TADC=width2dig(time,out); %to convert the PWM analog to digital code words
% TADC=ppm2dig(time,out); %to convert the PPM analog to digital code words
DAC_out=dac(TADC); %to get back the analog signals using a DAC code
dc_offset = sum(DAC_out)./length(DAC_out)؛
data_stream = DAC_out-dc_offset؛
N = length(data_stream); % timedomain data length (for settling)
w=hann(N)/(N/4); %Hann window %to adjust fft results
bw=0.5e9; %BW of your system %if ADC is nyquist BW=.5FS
Fs=1e9; %sampling freq
Fin=0.4e9; %frequency of the input test sin wave
f=Fin/Fs; % Normalized signal frequency
fB=N*(bw/Fs); % Base-band frequency bins (the BW you are looking at)
[sndr,ptot,psig,pnoise,output_W]=calcSNDR(data_stream,f,1,fB,w,N)؛
ENOB=(sndr-1.76)/6.02 % Equivalent resolution in bits
L=length(data_stream)؛
figure;
sig_db= abs(20*log(fftshift(output_W)));
```

```
len=length(sig_db);
index=1;
min_val=20000;
for      i=1:len
         if       sig_db(i)<min_val
                  min_val=sig_db(i);
                  index=i;
         end
end
ENOB= (sndr-1.76)/6.02
fx=linspace(0,Fs,len-index+1); %frequency axis
plot(fx,sig_db(index:len))
title(['FFT 1024, ', 'ENOB= ', num2str(ENOB)]);
xlabel('frequency (Hz)');
ylabel('Signal in frequency domain (db)');
grid;

%%%%%%%%%%%%%%%used functions%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%width2dig%%%%%%%%%%%%%%%%%%

function  [Digital]  =  width2dig(period,Vin)
pulse_width =zeros(200000,1);
digital_output =zeros(200000,1);
Pos_edge=0;
pos_counter=0;
neg_counter=0;
i=1;
 calibration=1;
 Samp_id =1;
 flag=0;
 period_avg = .85*(10^-9);
     while (i <= length(period))
        %neglecting the 1st sample for calibration
         while (Vin(i,1) >= 0.6 && calibration ==1)
                i=i+1;
         end
          calibration= calibration+1;

            if (Vin(i,1) > 0.6 && flag ==0 )
            Pos_edge = period(i,1);
            flag = 1;
            pos_counter=pos_counter+1;% just indicator of # +ve edges
            end

            if (Vin(i,1) < 0.6 && Pos_edge ~=0 )
            Neg_edge = period(i,1);
            neg_counter=neg_counter+1;% just indicator of # -ve edges
            pulse_width(i,1) = Neg_edge - Pos_edge;

                  if (pulse_width(i,1) > period_avg)
```

```
                digital_output(Samp_id,1)=1;
              else
                digital_output(Samp_id,1)=0;
              end

            Samp_id = Samp_id+1;
            flag =0;
            Pos_edge =0;
            Neg_edge =0;
           end

      i=i+1;
    end

    pulse_width = pulse_width(1:Samp_id,1);
    digital_output = digital_output(1:Samp_id,1);

    figure;
    subplot(2,1,1);
    stem(digital_output);
        hold on;
    title( 'ADC OUTPUT');
    Digital= digital_output;
end

%%%%%%%%%%%%%%%used functions%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%ppm2dig%%%%%%%%%%%%%%%%%%%%

function  [Digital]  = ppm2dig(period,Vin)
slope =zeros(200000,1);
digital_output =zeros(200000,1);
x1=0;
x2=0;
y1=0;
y2=0;
i=1;
 calibration=1;
 Samp_id =1;
 flag=0;
 slope_avg=1.8*10^9;
    while (i < length(period))
       %neglecting the 1st sample for calibration
        while (Vin(i,1) > 0.625 && calibration ==1)
              i=i+1;
        end
         calibration= calibration+1;

           if (Vin(i,1) >= 0.625 && flag ==0 )
           x1 = period(i,1);
           x2 = period(i+10,1);
```

```
            y1= Vin(i,1);
            y2= Vin(i+10,1);
            slope(Samp_id,1)= (y2-y1)/(x2-x1);
            flag = 1;
               if (slope(Samp_id,1) > slope_avg)
                     digital_output(Samp_id,1)=1;
                  else
                     digital_output(Samp_id,1)=0;
                  end
               Samp_id=Samp_id+1;% just indicator of # +ve edges



               elseif (Vin(i,1) < 0.625)
                  if (Vin(i+1,1) >= 0.625 && flag ==1 )
                  flag=0;
                  end
               end
                     i=i+1;

    end

    slope = slope(1:Samp_id-1,1)
    digital_output = digital_output(1:Samp_id-1,1);
       figure;
    subplot(2,1,1);
    stem(digital_output);
        hold on;
    title( 'ADC OUTPUT');
Digital= digital_output;
 end

%%%%%%%%%%%%%%%used functions%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%DAC%%%%%%%%%%%%%%%%%%

function  [Vout]  =  dac(Digital)
% Applying output to DAC
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 % FOR 12-bit DAC meth.
 % output(11) = 1.2v/2^1 = 0.6
 % output(10) = 1.2v/2^2 = 0.3
 % output(9) = 1.2v/2^3 = 0.15
 % output(8) = 1.2v/2^4 = 0.075
 % output(7) = 1.2v/2^5 = 0.0375
 % output(6) = 1.2v/2^6 = 0.01875
 % output(5) = 1.2v/2^7 = 0.009375
 % output(4) = 1.2v/2^8 = 0.0046875
 % output(3) = 1.2v/2^9 = 0.00234375
 % output(2) = 1.2v/2^10 = 0.001171875
 % output(1) = 1.2v/2^11 = 0.0005859375
```

```
 % output(0) = 1.2v/2^12 = 0.00029296875
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  % FOR 12-bit DAC VTC.
 % output(11) = 1v/2^1 = 0.5
 % output(10) = 1v/2^2 = 0.25
 % output(9) = 1v/2^3 = 0.125
 % output(8) = 1v/2^4 = 0.0625
 % output(7) = 1v/2^5 = 0.03125
 % output(6) = 1v/2^6 = 0.015625
 % output(5) = 1v/2^7 = 0.0078125
  % output(4) = 1v/2^8 = 0.00390625
 % output(3) = 1v/2^9 = 0.001953125
 % output(2) = 1v/2^10 = 0.0009765625
 % output(1) = 1v/2^11 = 0.00048828125
 % output(0) = 1v/2^12 = 0.000244140625
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 DAC_OP = zeros(200000,1);
while (rem(length(Digital),9)~=0)
   Digital = Digital(1:end-1,1);
end
 xx = length(Digital);
m=1;
%%%%%%%%%%%%%%%%
% % for 6bits DAC for the VTC
%   for j=1 :6: (xx)
%      DAC_OP(m,1) = 0.360+ (373/1000)*(Digital(j,1)*0.015625...
% + Digital(j+1,1)*0.03125+ Digital(j+2,1)*0.0625...
% + Digital(j+3,1)*0.125+ Digital(j+4,1)*0.25+Digital(j+5,1)*0.5);
%  m=m+1;
%   end
%%%%%%%%%%%%%%%%%%%%%
% % for 10bits DAC for the diff vcd
% for j=1 :9: (xx)
%      DAC_OP(m,1) = 0.22+ (560/1000)*(Digital(j,1)*0.001953125...
% + Digital(j+1,1)*0.00390625+Digital(j+2,1)*0.0078125+ Digital(j+3,1)*0.015625...
% + Digital(j+4,1)*0.03125+ Digital(j+5,1)*0.0625...
% + Digital(j+6,1)*0.125+ Digital(j+7,1)*0.25+Digital(j+8,1)*0.5);
%  m=m+1;
%   end
% % for 10bits DAC for the diff VTC
%   for j=1 :10: (xx)
%      DAC_OP(m,1) = 0.22+ (560/1000)*(Digital(j,1)*0.0009765625+
Digital(j+1,1)*0.001953125...
% + Digital(j+2,1)*0.00390625+Digital(j+3,1)*0.0078125+ Digital(j+4,1)*0.015625...
% + Digital(j+5,1)*0.03125+ Digital(j+6,1)*0.0625...
% + Digital(j+7,1)*0.125+ Digital(j+8,1)*0.25+Digital(j+9,1)*0.5);
%  m=m+1;
%   end
%%%%%%%%%%%%%%%%%%
% 12 bits
```

```
%  for j=1 :12: (xx)
%      DAC_OP(m,1) = 0.369 +(462/1200)*( Digital(j,1)* 0.00029296875
+Digital(j+1,1) *0.0005859375 ...
% + Digital(j+2,1)* 0.001171875+ Digital(j+3,1)*0.00234375+
Digital(j+4,1)*0.0046875...
% + Digital(j+5,1)*0.009375+ Digital(j+6,1)*0.01875+ Digital(j+7,1)*0.0375...
% + Digital(j+8,1)*0.075+ Digital(j+9,1)*0.15+
Digital(j+10,1)*0.3+Digital(j+11,1)*0.6);
% % %  if the 8bits of one sample output =1 , dac_op=715.5m (end of max DR +DC)
% % %  if the 8bits of one sample output =0 , dac_op=484.5m (end of min DR +DC)
%  m=m+1;
%  end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
%  for j=1 :11: (xx)
%      DAC_OP(m,1) = 0.369 +(462/1200)*(Digital(j,1) *0.0005859375 ...
% + Digital(j+1,1)* 0.001171875+ Digital(j+2,1)*0.00234375+
Digital(j+3,1)*0.0046875...
% + Digital(j+4,1)*0.009375+ Digital(j+5,1)*0.01875+ Digital(j+6,1)*0.0375...
% + Digital(j+7,1)*0.075+ Digital(j+8,1)*0.15+
Digital(j+9,1)*0.3+Digital(j+10,1)*0.6);
%   m=m+1;
%  end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% %for 4 bits DAC
%   for j=1 :4: (xx)
%      DAC_OP(m,1) = 0.369 + (231/1200)*(Digital(j,1)*0.075...
%      + Digital(j+1,1)*0.15 + Digital(j+2,1)*0.3+ Digital(j+3,1)*0.6);
%  m=m+1;
%  end


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% %for 10 bits dac
%  for j=1 :10: (xx)
%      DAC_OP(m,1) = 0.369 +(462/1200)*(Digital(j,1)* 0.001171875 +
Digital(j+1,1)*0.00234375...
% + Digital(j+2,1)*0.0046875 + Digital(j+3,1)*0.009375+ Digital(j+4,1)*0.01875+
Digital(j+5,1)*0.0375...
% + Digital(j+6,1)*0.075+ Digital(j+7,1)*0.15+
Digital(j+8,1)*0.3+Digital(j+9,1)*0.6);
%  m=m+1;
%  end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% for 8bits DAC for single meth
 for j=1 :9: (xx)
```

```
    DAC_OP(m,1) = 0.4+ (550/1200)*(Digital(j,1)*0.00234375...
       + Digital(j+1,1)*0.0046875+ Digital(j+2,1)*0.009375...
+ Digital(j+3,1)*0.01875+ Digital(j+4,1)*0.0375+ Digital(j+5,1)*0.075...
+ Digital(j+6,1)*0.15+ Digital(j+7,1)*0.3+Digital(j+8,1)*0.6);
 m=m+1;
  end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
DAC_OP = DAC_OP(1:m-1,1);
     subplot(2,1,2);
     stem(DAC_OP);
     hold on;
     title( 'Equivalent amplitudes AFTER DAC');
Vout= DAC_OP;
end

%%%%%%%%%%%%%%%used functions%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%calcsndr%%%%%%%%%%%%%%%%%%

function [sndrdB,ptotdB,psigdB,pnoisedB,output_W] =
calcSNDR(vout,f,fBL,fBH,w,N)
% vout: Sigma-Delta bitstream taken at the modulator output
% f: Normalized signal frequency (fs = 1)
% fBL: Base-band lower limit frequency bins
% fBH: Base-band upper limit frequency bins
% w: Windowing vector
% N: Number of samples
% sndrdB: SNDR in dB
% ptotdB: Sigma-Delta modulator output power spectral density (vector) in dB
% psigdB: Extracted signal power spectral density (vector) in dB
% pnoisedB: Noise power spectral density (vector) in dB
fBL=ceil(fBL);
fBH=ceil(fBH);
signal=(N/sum(w)).*sinusx(vout(1:N).*w,f,N); % Extracts sinusoidal signal
noise=vout(1:N)-signal; % Extracts noise components
stot=(abs(fft((vout(1:N).*w)'))).^2;% Bitstream PSD
ssignal=(abs(fft((signal(1:N).*w)'))).^2*(10^5); % Signal PSD
snoise=(abs(fft((noise(1:N).*w)'))).^2; % Noise PSD
pwsignal=sum(ssignal(fBL:fBH)); % Signal power
pwnoise=sum(snoise(fBL:fBH)); % Noise power

output_W=stot;
sndr=(pwsignal/pwnoise);

sndrdB=dbp(sndr)
norm=sum(stot(1:N/2));%/sum(vout(1:N).^2)*N; % PSD normalization

        if      nargout > 1
                ptot=stot/norm;
                ptotdB=dbp(ptot);
        end
```

```
        if      nargout > 2
                psig=ssignal/norm;
                psigdB=dbp(psig);
        end
        if      nargout > 3
                pnoise=snoise/norm;
                pnoisedB=dbp(pnoise);
        end

%%%%%%%%%%%%%%%%used functions%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%sinusx%%%%%%%%%%%%%%%%%%
function outx = sinusx(in,f,n)
% in: Input data vector
% f: Normalized input signal frequency
% n: Number of simulation points
% outx: Sinusoidal signal
sinx=sin(2*pi*f*[1:n])';
cosx=cos(2*pi*f*[1:n])';
in=in(1:n);
a1=2*sinx.*in;
a=sum(a1)/n;
b1=2*cosx.*in;
b=sum(b1)/n;
outx=a.*sinx + b.*cosx;

%%%%%%%%%%%%%%%%used functions%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%dby%%%%%%%%%%%%%%%%%%%

function y = dbv(x)
% x: Input
% y: Output in dB
y = -Inf*ones(size(x));
nonzero = x~=0;
y(nonzero) = 20*log10(abs(x(nonzero)));

%%%%%%%%%%%%%%%%used functions%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%dbp%%%%%%%%%%%%%%%%%%%

function y = dbp(x)
% x: Input
% y: Output in dB
y = -Inf*ones(size(x));
nonzero = x~=0;
y(nonzero) = 10*log10(abs(x(nonzero)));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

B.7 PVT Variations

In order to make all components operate on the same corner, you should identify the used components type and you shall modify their model file to the aimed process. To operate on a specific corner, first, you shall press on "Setup" icon and "Model libraries"

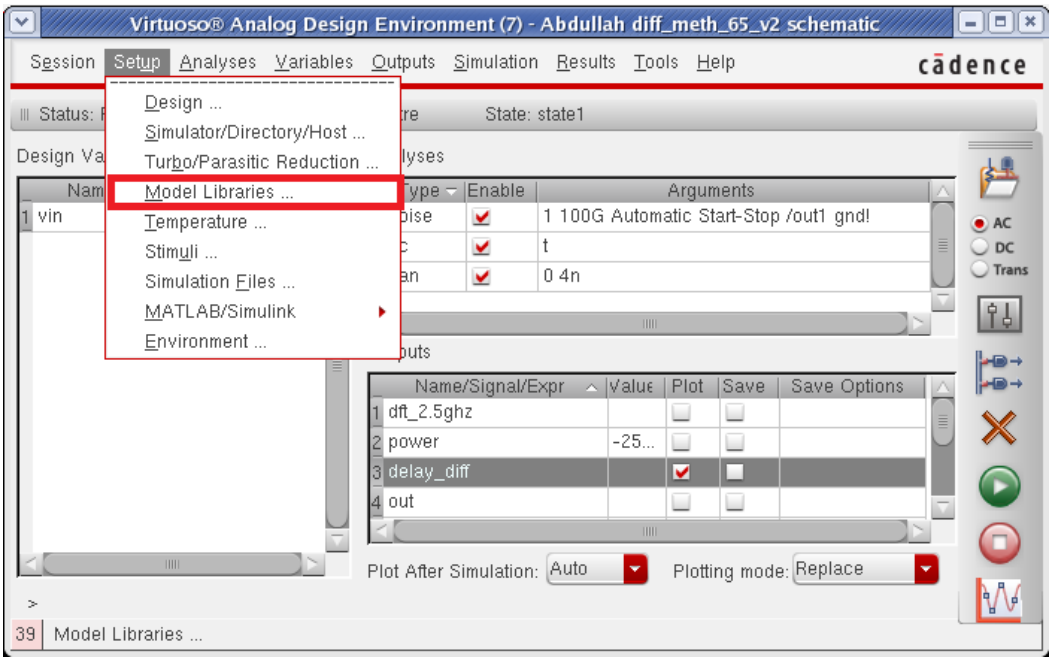


Figure B.21: Model libraries setup on Virtuoso ADE.

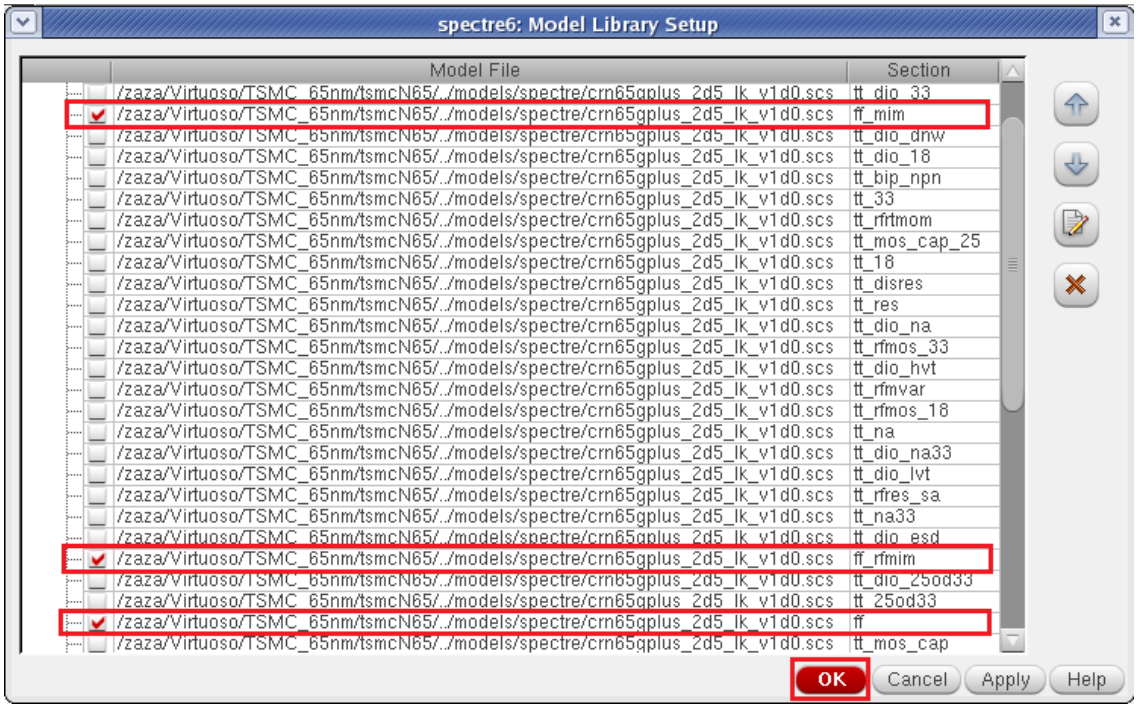


Figure B.22: Modifying the device model process.

from the appeared drop down menu on the Virtuoso ADE as shown in Figure B.21. In the proposed design the main circuit components are transistors and the MIMCAP. Hence, it is preferred to modify their model to a specific corner. For example, if we study the FF corner, we modify the transistors model file to "ff" and the MIMCAP model files to "ff_mim" and "ff_rfmim" as illustrated on Figure B.22. This is applicable for all corners (TT, FS, SF, SS and FF). Then, you can check the effect of operating on this corner by simulating the needed output as: VTC output, delay equation, power consumption, etc.

To check the simulation results regarding a supply variations, all you need to do is to modify the voltage value of the supply source. For example, if the supply voltage originally equals to 1.2 V, you shall check the design behavior if you add a variation value of ± 10 % from the default supply voltage.

To modify the operating temperature, you shall press on "Setup" icon and "Temperature" from the appeared drop down menu on the Virtuoso ADE as shown in Figure B.23. Then, you shall type the new temperature value as shown in Figure B.24 and study the design specifications based on this new value.

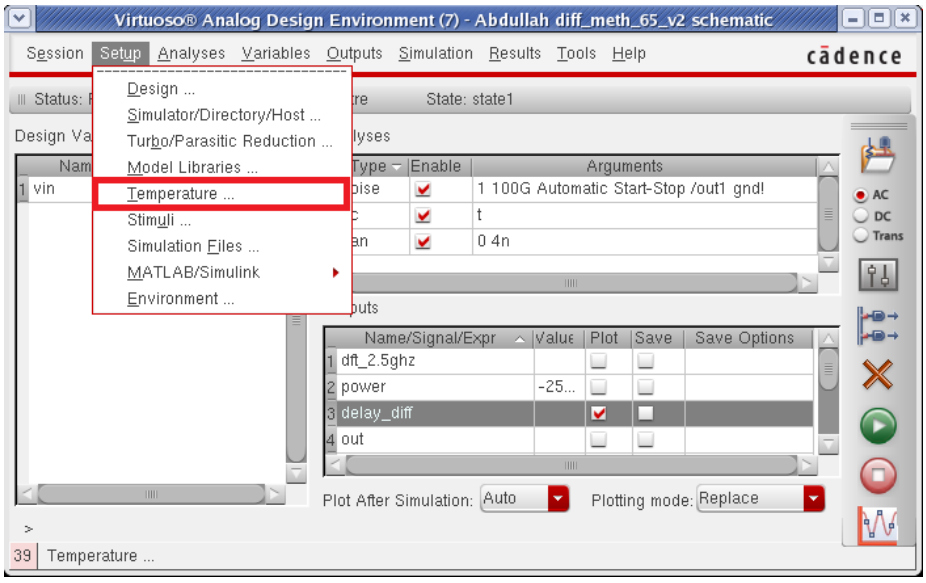


Figure B.23: Temperature libraries setup on Virtuoso ADE.

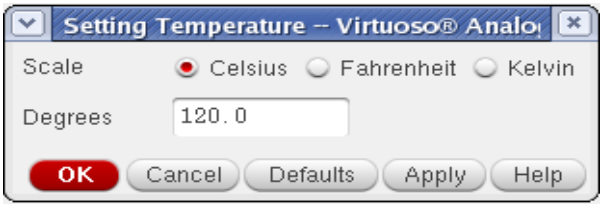


Figure B.24: The operating temperature setup on Virtuoso ADE.

ملخص الرسالة

عند التدرج للمستويات الأدنى لتكنولوجيا السيموس تكون دقة الوقت للدوائر الرقمية أعلى بكثير من دقة الجهد للدوائر التناظرية، لذلك أصبح زيادة نسبة الجزء الرقمى عن الجزء التناظرى أمر حيوى لا شك فيه خصوصا عند الترددات العالية. بناء على ذلك يعد استخدام المحول التناظرى الرقمى المعتمد على الوقت من الأركان الأساسية لتصميم التطبيقات عالية التردد كمستقبلات الراديو المعرفة برمجيا والمستقبلات واسعة النطاق، وأيضا لتصميم أنظمة الدقة العالية كتطبيقات الطبية الحيوية والتطبيقات العسكرية. الجدير بالذكر أن تلك المحولات تستهلك طاقة مستنفذة ومساحة أقل من المحولات الرقمية التقليدية. يتكون المحول التناظرى الرقمى المعتمد على الوقت من عنصرين أساسيين هما: محول الجهد الوقتى ومحول الوقت الرقمى

فى تلك الرسالة يتم عرض عدة تصميمات مختلفة من الدوائر التفاضلية المتكاملة للمحولات الجهدية الوقتية متضمنة تصميم روايتان قابلة الإدماج فى مستقبلات الراديو المعرفة برمجيا باستخدام تكنولوجيا ٦٥ نانومتر، كما يتم مقارنة تلك المحولات بالتصميمات أحادية النهاية. تعتمد تلك المحولات التفاضلية على المكثفات عازلة المعادن للحد من التغيرات العملية الجهدية الحرارية المصاحبة لأساليب الصناعة. يستند التصميم الروائى الأول على منهجية محسنة تحقق ١٢,٨ بت من عدد البتات الفعالة، ويستهلك مساحة حوالى ٢٢٩ ميكرومتر^{٢}، ويستنفذ طاقة مقدارها ٠,٢٥ ميللى وات. يعمل هذا التصميم على تردد ١,٢ جيجا هرتز وجهد موفر يساوى ١ فولت. كما تعرض دراسة لتلك التغيرات الصناعية المؤثرة على خصائص هذا التصميم مع تقديم دائرة تقويم لتحسيين تلك الخصائص المشوهة. بينما من الممكن أن يستخدم فى التصميم الروائى الثانى فى الترددات شديدة العلو التى تصل إلى ٨ جيجا هرتز تحت جهد موفر يساوى ١ فولت. يحقق ذلك التصميم حوالى ٨,٩ بت، ويستهلك مساحة قدرها ٧٤٢ ميكرومتر^{٢}، وطاقة قدرها ١,٦ ميللى وات. تم اختبار تلك الحسابات عن طريق نتائج المحاكاة من برنامج الماتلاب وبرنامج كيدانس.

أيضا يتم عرض فى تلك الرسالة نتائج المحاكاة لما بعد التخطيط الشكلى للتصميمن الروائيين عند تكنولوجيا ١٣٠ نانومتر القابلة للإدماج بالتطبيقات الطبية الحيوية كما فى الأنظمة المزرعة العصبية. يعتبر الهدف الرئيسى من تصميم تلك الأنظمة هو توليد طاقة مستنفذة ومساحة

مستهلكة متفانية فى الصغر عن طريق التشغييل عند ترددات صغيرة وحتى تكون قادرة على إنتاج دقة عالية. يصمم هذا التخطيط الشكلى بناء على معيار أقل مسافة ممكنة للحصول على أقل مساحة ممكنة. ١٠ ميجا هرتز هى التردد المستخدم للتصميمين فى تلك التكنولوجيا. بعد تصميم المخطط الشكلى للتصميم الأول تم اختبار دائرة التقويم المكونة من مجموعة من الدوائر مقسمة الجهد المعتدمة على المكثفات عالية الحجم التى توفر مجموعة من الجهد الثابت لإزالة تغيرات الصناعة.

مهندس: عبدالله محمد أحمد البيومى

تاريخ الميلاد: ١٩٩٠\١١\٠٥

الجنسية: مصرى

تاريخ التسجيل: ٢٠١٢\١٠\٠١

تاريخ المنح: --/--/٢٠١٦

القسم: هندسة الإلكترونيات والاتصالات الكهربية

الدرجة: ماجستير العلوم

المشرفون:

أ.د. أحمد محمد سليمان

د. حسن مصطفى حسن مصطفى

الممتحنون:

أ.د أحمد محمد سليمان (المشرف الرئيسي)

أ. محمد رياض (الممتحن الداخلي)

أ. حسانين عامر (الممتحن الخارجي) (هندسة الالكترونيات والاتصالات بالجامعة الأمريكية بالقاهرة)

عنوان الرسالة:

تصميم دوائر تفاضلية عالية الأداء معادلة التغيرات لتحويل الجهد إلى وقت

الكلمات الدالة:

تكنولوجيا النانومتر، محول الجهد للوقت، المحول الرقمى التناظرى المؤسس على الوقت، نظم الراديو المعرفة برمجيا، تطبيقات الطب الحيوية، المكثف عازل المعادن، النطاق الديناميكى.

ملخص الرسالة:

تقدم هذه الأطروحة عدة تصميمات مختلفة من الدوائر التفاضلية للمحولات الجهدية الوقتية المعتمدة على المكثفات عازلة المعادن متضمنة تصميمين روائيين مقترحين يحققا أداء عالى عند الترددات العالية قابلة للإدماج بمستقبلات الراديو المعرفة برمجيا باستخدام تكنولوجيا ٦٥ نانومتر ومقارنة بالتصميمات أحادية النهاية. أيضا يتم عرض دراسة مفصلة عن التغيرات الناتجة عن الصناعة مع طرح طريقة لمعادلة تلك التغيرات للتصميم المقترح الأول عن طريق مجموعة من الدوائر مقسمة الجهد المؤسسة على مكثفات عالية الحجم. كما يتم توفير نتائج المحاكاة لما بعد التخطيط الشكلى للروايتين المقترحين باستخدام تكنولوجيا ١٣٠ نانومتر للإدماج بالأنظمة الطبية الحيوية القابلة للزرع ذات الترددات المنخفضة.

تصميم دوائر تفاضلية عالية الأداء معادلة التغيرات لتحويل الجهد إلى وقت

اعداد
عبدالله محمد أحمد البيومى

رسالة مقدمة إلى
كلية الهندسة - جامعة القاهرة
كجزء من متطلبات الحصول على درجة
ماجستير العلوم
في
هندسة الإلكترونيات و الاتصالات الكهربية

يعتمد من لجنة الممتحنين:

الاستاذ الدكتور: أحمد محمد سليمان	المشرف الرئيسى
الاستاذ: محمد رياض	الممتحن الداخلي
الاستاذ: حسانين عامر	الممتحن الخارجي (استاذ بهندسة الإلكترونيات والاتصالات بالجامعة الأمريكية بالقاهرة)

كليــة الهندســة - جامعــة القاهـرة
الجيـزة - جمهوريـة مصـر العربيــة
٢٠١٦

تصميم دوائر تفاضلية عالية الأداء معادلة التغيرات لتحويل الجهد إلى وقت

اعداد

عبدالله محمد أحمد البيومى

رسالة مقدمة إلى

كلية الهندسة - جامعة القاهرة

كجزء من متطلبات الحصول على درجة

ماجستير العلوم

في

هندسة الإلكترونيات و الاتصالات الكهربية

تحت اشراف

أ.د. أحمد محمد سليمان

أستاذ متفرغ

قسم هندسة الإلكترونيات و الاتصالات الكهربية

كلية الهندسة - جامعة القاهرة

د. حسن مصطفى حسن مصطفى

مدرس

قسم هندسة الإلكترونيات و الاتصالات الكهربية

كلية الهندسة - جامعة القاهرة

كليــة الهندســة - جامعــة القاهـرة

الجيـزة - جمهوريـة مصـر العربيــة

٢٠١٦

تصميم دوائر تفاضلية عالية الأداء معادلة التغيرات لتحويل الجهد إلى وقت

اعداد

عبدالله محمد أحمد البيومى

رسالة مقدمة إلى

كلية الهندسة - جامعة القاهرة

كجزء من متطلبات الحصول على درجة

ماجستير العلوم

في

هندسة الإلكترونيات و الاتصالات الكهربية

كليــة الهندســة - جامعــة القاهـرة

الجيـزة - جمهوريـة مصـر العربيــة

٢٠١٦