The American University in Cairo

School of Science and Engineering

Circuit Design Techniques for Power Efficient Microscale Energy Harvesting Systems

A thesis submitted in partial fulfillment of the requirements
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Dedicated to My Parents and My Brother. For Their Endless Love, Support and Encouragement ...

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"Your time is limited, don't waste it living someone else's life. Don't be trapped by dogma, which is living the result of other people's thinking. Don't let the noise of other's opinion drowned your own inner voice. And most important, have the courage to follow your heart and intuition, they somehow already know what you truly want to become. Everything else is secondary".

Steve Jobs

The American University in Cairo

Abstract

School of Science and Engineering
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Circuit Design Techniques for Power Efficient Microscale Energy Harvesting Systems

by Ayman Eltaliawy

Power Management is considered one of the hot topics nowadays, as it is already known that all integrated circuits need a stable supply with low noise, a constant voltage level across time, and the ability to supply large range of loads. Normal batteries do not provide those specifications. A new concept of energy management called energy harvesting is introduced here. Energy harvesting means collecting power from ambient resources like solar power, Radio Frequency (RF) power, energy from motion...etc. The Energy is collected by means of a transducer that directly converts this energy into electrical energy that can be managed by design to supply different loads. Harvested energy management is critical because normal batteries have to be replaced with energy harvesting modules with power management, in order to make integrated circuits fully autonomous; this leads to a decrease in maintenance costs and increases the life time.

This work covers the design of an energy harvesting system focusing on microscale solar energy harvesting with power management. The target application of this study is a Wireless Sensor Node/Network (WSN) because its applications are very wide and power management in it is a big issue, as it is very hard to

replace the battery of a WSN after deployment. The contribution of this work is mainly shown on two different scopes. The first scope is to propose a new tracking technique and to verify on the system level. The second scope is to propose a new optimized architecture for switched capacitor based power converters. At last, some future recommendations are proposed for this work to be more robust and reliable so that it can be transfered to the production phase.

The proposed system design is based on the sub-threshold operation. This design approach decreases the amount of power consumed in the control circuit. It can efficiently harvest the maximum power possible from the photo-voltaic cell and transfer this power to the super-capacitor side with high efficiency. It shows a better performance compared to the literature work. The proposed architecture of the charge pump is more efficient in terms of power capability and knee frequency over the basic linear charge pump topology. Comparison with recent topologies are discussed and shows the robustness of the proposed technique.

Contents

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Abbreviations

WSN	**W**ireless **S**ensor **N**etwork
PV Cell	**P**hoto-**V**oltaic Cell
MPPT	**M**aximum **P**ower **P**oint **T**racking
SC	**S**hort **C**ircuit
OC	**O**pen **C**ircuit
SCCP	**S**witched **C**apacitor **C**harge **P**ump
OTA	**O**perational **T**ransconductance **A**mplifier
TSPC	**T**rue **S**ingle **P**hase **C**lock
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
ABB	**A**daptive **B**ody **B**ias
AC	**A**lternating **C**urrent
DC	**D**irect **C**urrent
MIMO	**M**ulti-**I**nput **M**ulti-**O**utput
RF	**R**adio **F**requency
TEG	**T**hermo-**E**lectric **G**enerator
EMI	**E**lectro-**M**agnetic **I**nterference
DTCM	**D**esign **T**ime **C**omponent **M**atching
VCO	**V**oltage **C**ontrolled **O**scillator

Symbols

P	Power	Watts (Js^{-1})
V	Voltage	Volt
I	Current	Ampere
J	Current/unit area	Ampere/unit area (A/cm^2)
η	Efficiency	dimensionless
C	Capacitance	Farad
R	Resistance	Ohm (Ω)
T	Temperature	Kelvin/Celsius ($^\circ K/^\circ C$)
ϕ_F	Technology Constant	Volt
γ	Technology Constant	dimensionless
G	Irradiance	Watt/unit area
E_v	Illuminance	Lux(lx)

Chapter 1

Introduction

1.1 Motivation

Since the integrated circuit technology is pushing the fabrication scale to the nanometer region, a new category of small ultra low power applications has taken a challenging place in the electronics market. Examples of these tiny systems are smart dusts [1], biomedical implants [2] and wireless sensor nodes [3]. The most important characteristics of these devices are small size, low cost integration, ideally infinite life time and maintenance-free operation. The available power sources (act as storage elements) used for powering the portable consumer electronics are batteries (so called super-capacitors). They have limited energy storage. Since the micro-scale systems dictate limited amount of energy, the available storage reservoirs will run out of energy after a limited time. Accordingly, these systems stops working, thus an alternative power management solution should hand over to maintain sustainability to these devices.

Because of the tight constraints dictated by those tiny systems especially in size, the available solution is either to replace the powering battery, or to implant a rechargeable storage from the beginning, so that when it goes out of charge,

it can be recharged. Nevertheless, both solutions are infeasible in terms of area and maintainence costs. The batteries itself are very bulky and limited in energy density. The effort and cost done for replacing the normal batteries (i.e., battery replacement of implanted pacemakers [4]) or recharging the rechargeable batteries are huge. Moreover, the time lost in re-installing the application at their sites specially in wireless sensor networks; it consists of thousands of nodes connected through a wireless network. So there should be a more engineered solution for this problem. The new solution should verify the sizing constraints and the lowest maintainence cost/effort possible through providing unlimited energy capacity.

The most matched solution for the problems stated above is powering the small scale systems through an integrated micro-scale energy harvesting circuits. Energy harvesting is a concept of collecting energy from ambient sources. This process is done by means of transducers to transform the ambient power into electrical power, accordingly this power is managed through power conditioning circuits to be suitable for supplying different loads. This process is also called "Energy Scavenging". Actually, the concept is old and covers a lot of common applications. It can be used in solar panels to supply electricity for houses; it is also used in wind turbines, other examples like solar farms [5], windmills [6] and hydro-generators [7], however these are considered as large scale systems. In this work, design issues for powering small scale systems, so called stand-alone electronic systems, will be discussed. Examples of these systems are traffic, medical and environmental applications, navigation and system controls of buildings. By using the energy harvesting techniques, the micro-scale systems can deliver unlimited amount of energy. They can be independent of the storage element size and capacity, so they can be self-powered modules [8],[9].

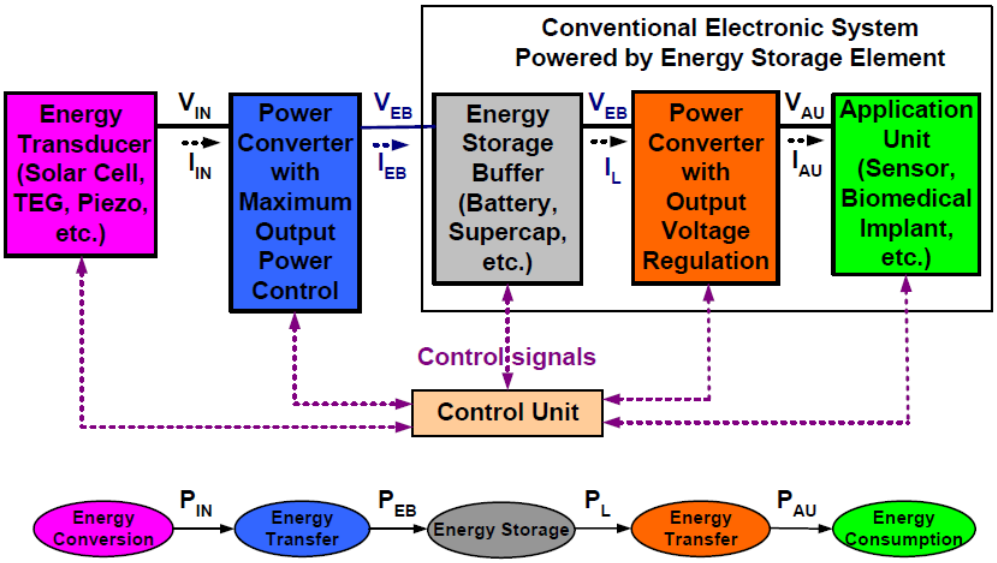


FIGURE 1.1: A typical block diagram of an energy harvesting system.[10]

1.2 System Blocks Overview

Figure 1.1 shows a generic block diagram for the micro-scale energy harvesting system. The system shown in figure is consisting of six main blocks: an energy transducer, a power converter with maximum output power control, an energy storage buffer (usually a super-capacitor or a rechargeable battery), another power converter for output energy regulation and the application unit like sensors, biomedical implants,...etc. Finally, the control unit that manages the energy flow through different stages.

It can be shown also that the input energy passes through different states starting with energy conversion, energy transfer, energy storage, energy transfer, energy consumption. The main design goal is to minimize the energy losses between these blocks so that a maximum power delivery to the load can be realized.

The micro-scale energy transducer converts the ambient energy available in the environment into electrical energy. This energy is used to power the application unit or used to recharge a rechargeable battery. Energy conversion has two main mechanisms, either single input energy conversion technique [11],[12] or multiple

input energy conversion [13],[14]. The system is explained in Chapter 2 block by block, in order to understand the system performance and discuss different limitations and design space for efficient energy harvesters. Since the energy harvesting system is dealing with the outer world which is the ambient energy, the available energy is varying across time. Accordingly, the input power to the system is also varying across time. The nature of the time variant input power dictates a very careful design and understanding of system blocks. This is to provide two main specifications, first, the design should guarantee the power needed by the load across any instant of time, second, the system should sustain itself under any conditions regarding process variations, source availability. Those external changes adopt critical design solutions in the absence of external source while delivering the needed power to the load. Usually, the voltage level appeared on the transducer side is low such that it can not supply the application directly, so a power converter is used in order to boost the voltage to a feasible level that has the ability to supply different ranges of loads. The second role of the power converter also is to do power matching for the available power at the transducer side. This could be done by means of a control mechanism. So the second most important block in the system is the control unit. It has the ability to maintain the power converter at its maximum power capability, and here comes the concept of the maximum power tracking, it is a way or an algorithm that the control unit follows to maintain the whole system at its best performance. Different implementation techniques for the control unit are discussed in Chapter 2. Different topologies of power converters are also discussed showing the pros and cons of each topology. Selection criteria are also highlighted.

1.3 Design Challenges

Since the energy harvesting systems are a little bit complex, the system should be carefully analyzed. External and internal variations should be addressed well.

Sustainability is the most important metric for those systems for correct functionality. Design challenges are categorized into two levels, level 1 is the energy harvester system level, level 2 is the block design of each part of the system.

The first design challenge of such systems is that the energy transducers used are in the range of cm^2. These transducers are supposed to produce ultra low terminal voltage levels (in the range of 0.3 V $\rightarrow$ 0.6 V). The low voltage operation dictates a careful power converter design to boost the voltage level to a new level that can be able to supply the application unit. The power converter should also be matched for maximum power transfer as well as occupying minimum possible area.

The second design challenge is the limited power available at the energy transducer side, as it is in the range of μW to mW. The low power availability adopts ultra low power consumption of the interface circuits, as the energy harvester consumes some power from the transducer to do the power conversion. This consumed power has a direct impact on the power efficiency which is the amount of extracted power at the super-capacitor side divided by the power available at the energy transducer side.

One of the biggest challenges in the system design of the power harvesters is the self-power mode (self-sustained operation) of the application unit, since this is the worst case that an energy harvester can work in. The harvester has to power the application unit at the absence of the input energy source, accordingly, the system should satisfy the following conditions [15],[16]. The first condition is that the system should guarantee that the extracted energy from the transducer should be greater than the average rate of change of energy consumption by the application unit, otherwise, the system will fade away and stop functioning. The second condition is that the harvester output buffer has to have the ability to supply the application at the time when the harvester suffers from power conversion drops due to the environmental variations.

1.4 Thesis Organization

The goal of this study is to investigate the design challenges for a power efficient energy harvesting in the micro-scale level used to supply a few mW power range. This is actually achieved through focusing on two essential parts of the system.

Chapter 2 is presenting a broad view of the system. It explains system blocks in details, literature architectures are discussed showing the advantages and disadvantages of them. Selection criteria of the available architectures are highlighted showing the limitations that arises when going down to the ultra low power harvesters. This chapter draws the decisions taken to develop an efficient design for micro-scale energy harvesters.

The first contribution is achieved through proposing a new control scheme that has the ability to track the maximum power available at the energy transducer side with small amount of power consumed in the control unit. The idea is based on two concepts, the first one is the negative feedback automatic tracking through realization of the system design equations, this tracking mechanism saves a lot of hardware. The second concept is forcing the control unit to work in the sub-threshold region, thus, it consumes very low power. These techniques are discussed in details in Chapter 3 with simulation results showing the robustness of the proposed design across process corners.

The second contribution is achieved through proposing a new architecture for the power converters using a new clocking scheme. The new design increases the output current of the converter over the proposed literature designs. Chapter 4 shows the detailed analysis of the new technique and views the simulation results that supports the new idea.

Chapter 5 draws the conclusion of this work and give some future recommendations for the system discussed here on various design levels. This is useful for physical verification issues.

Chapter 2

Background and Literature Review

This chapter is presenting the detailed explanation and understanding of each block in the system. First, it presents the different types of the available ambient energy resources and the corresponding energy transducers characteristics. Second, detailed system analysis is discussed with highlighting the different control architectures used in the literature. Third, the types of the available power converters are analyzed stating the best architecture used in the system.

2.1 Micro-scale Energy Transducers

Table 2.1 shows the energy density of various energy transducers depending on the transduction type. The energy density is measured in W/cm^3. It should be noticed that the solar energy transduction provides higher energy densities than their counterparts for other energy forms. It is very critical for system designers to understand the electrical characteristics of these transducers for efficient system

TABLE 2.1: Power Density of Various Energy Transducers [15]

Harvesting Technology	Power Density
Solar Cell (Outdoors at noon)	$15mW/cm^3$
Solar Cell (indoor lighting)	$1mW/cm^3$
Piezoelectric (shoe inserts)	$300\mu W/cm^3$
Vibration (small microwave oven)	$116\mu W/cm^3$
Thermoelectric ($10°C$ gradient)	$40\mu W/cm^3$
Acoustic noise (100 dB)	$960nW/cm^3$

design. The coming sections are investigating the characteristics of some energy transducers that can be used for energy harvesting.

2.1.1 Solar Photo-voltaic Cell

Solar cells (Photo-Voltaic (PV) cells) are the most popular devices for optical transduction, since they provide the highest energy density compared to their counterparts. Figure 2.1 [17] shows the equivalent circuit model of a PV cell; the curves shown in the figure are (I-V) characteristics and (P-V) characteristics. The PV cell is considered as a voltage limited current source. The current source represents the amount of generated current in the cell due to incident optical power. The diode represents the P-N junction. (R_p) represents the shunt resistor that models the leakage current at the junction, its value is usually high. (R_s) represents the silicon ohmic contacts, the higher the (R_s) value is, the lower slope of the (I-V) curve is at the constant voltage region. Conversely, the lower the (R_p) value is, the higher the slope of the (I-V) curve is at the constant current region.

The short circuit current (I_{sc}) is directly proportional to the incident optical power; the open circuit voltage (V_{oc}) is roughly constant at high illumination

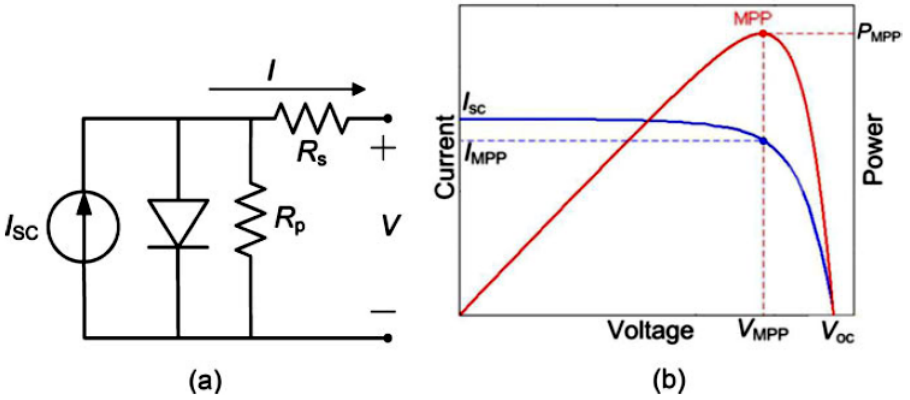


FIGURE 2.1: Photo Voltaic cell characteristics. (a)Equivalent electrical model. (b) I-V and P-V of a generic solar cell.[17]

conditions, but varies widely at low illumination conditions (i.e. below around $200W/m^2$). (I_{sc}) is nearly constant with temperature; where as (V_{oc}) linearly decreases with temperature increase. (P_{MPP}) represents the maximum power that can be generated from the PV cell at the operating conditions (also known as MPP: Maximum Power Point). Power decays rapidly on the right side of the MPP due to the fast decrease of the current in that region. The relationship between current and voltage of a single PV cell is described in Equation 2.1.

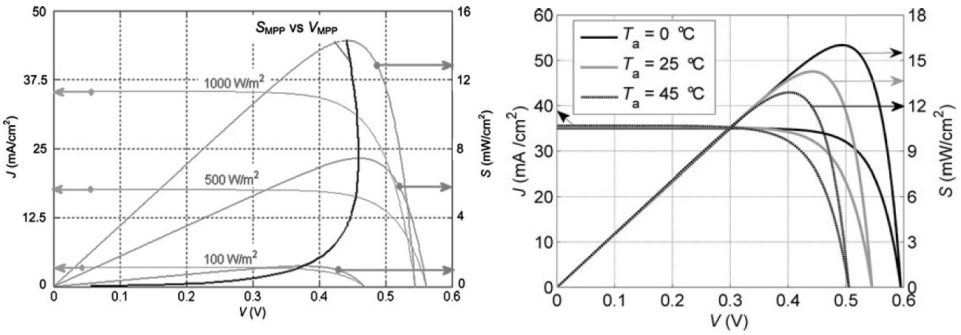
$$I = I_{ph} - I_0 \left(e^{\left(\frac{q\,(V + R_s I)}{n_d k T} \right)} - 1 \right) - \frac{V + R_s I}{R_p} \tag{2.1}$$

Where (I_{ph}) is the photo generated current that can be approximated by (I_{sc}). (I_0) is the saturation current of the diode. (q) is the charge of the electron. (n_d) is the ideality factor of the diode, which for silicon is usually between 1.2 and 1.8. (K) is the Boltzmann constant and (T) is the cell temperature in Kelvin. This equation can be rewritten as shown in Equation 2.2 in terms of current density (current/unit area), so by ignoring the effect of (R_s) and (R_p) :

$$J = J_{sc} - J_0 \left(e^{\left(\frac{qV}{n_d kT} \right)} - 1 \right) \tag{2.2}$$

By substituting for $V = V_{oc}$ then $J = 0$, one could get an expression for J_0. So after further simplification, the current density equation should be :

$$J = J_{sc} \left(1 - \frac{e^{\left(\frac{qV}{n_d kT} \right)} - 1}{e^{\left(\frac{qV_{oc}}{n_d kT} \right)} - 1} \right) \tag{2.3}$$



(a) **(b)**

FIGURE 2.2: I-V charactersitics (a) for differnt input light irradiance G. (b) for differernt temperature T.[17]

I-V characteristics are affected by 4 factors: temperature, isolation level, load characteristics and aging. Typical equations for temperature and irradiance dependence could be found in [17]. Figure 2.2(a) shows the variation of I-V and P-V curves across different incident irradiance (G) at $T = 25°C$, a locus for the maximum power point is also plotted on the same family of curves. Figure 2.2(b) shows the variation across temperature across constant input irradiance $G = 1000W/m^2$.

Since, the solar energy has abundant energy density [15], this work is focusing on the design of the front-end circuitry and discussing the challenges faced in each stage in the system. The photo-voltaic cell model used is an open source verilog-A

compact model [18], it has a set of customizable parameters that makes it easy to debug. It can be used also for modeling while comparing with a model extracted from a device simulator such as Centaurus or Comsol simulators. It can be also integrated into spice simulators to interface with circuits and systems. Figure 2.3 shows Power-Voltage curves for different input light irradiance. The locus of the maximum power point trajectory is also shown as a dotted line (i.e., MPP locus). Typical micro-solar panels give a power values up to the range of $3mW$ with an open circuit voltage up to $0.85V$. It should be noted that the target of the front-end system is to maintain the PV cell at its maximum power under any light intensity variation and also under any external changes(i.e., maintain it on the MPP locus), while delivering most of the extracted power to the load. The low power availability at the PV cell side dictates careful design for the control circuitry to consume the lowest possible power.

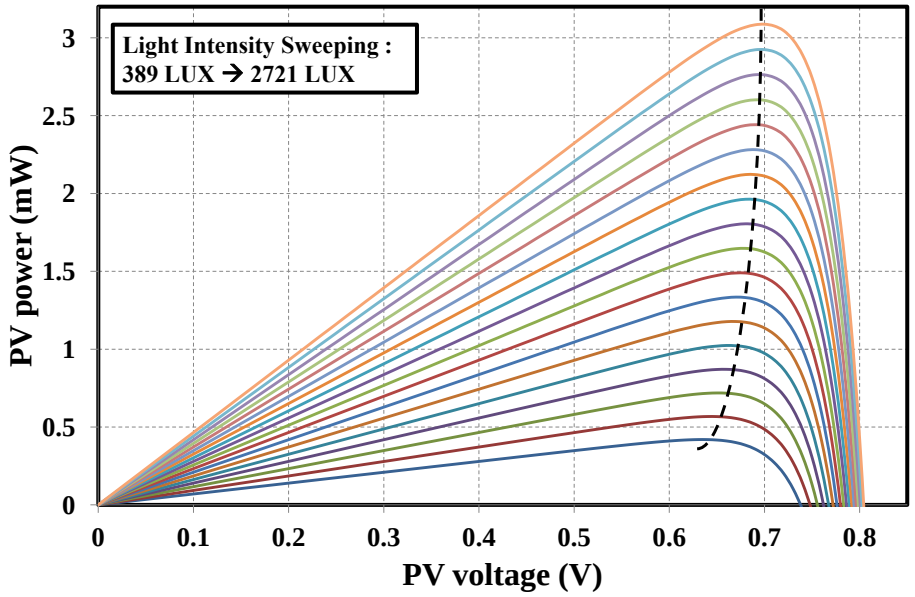


FIGURE 2.3: P-V characteristics of the QUCS integrated model

Since, we are dealing with light intensities at the solar cell side, it is important to show the transformation of the available electrical power to illuminance (Lux). Illuminance is a measure of how much luminous flux is spread over a given area. One can think of luminous flux (measured in lumens) as a measure of the total

amount of visible light present, and the illuminance as a measure of the intensity of illumination on a surface. A given amount of light will illuminate a surface more dimly if it is spread over a larger area, so illuminance (lux) is inversely proportional to area when the luminous flux (lumens) is held constant. Equation 2.4 shows the relationship between the illuminance (Lux) and the available electric power at the solar cell terminal.

$$E_{v(lx)} = \frac{P_{(W)} * \eta_{(lm/W)}}{A_{m^2}} \tag{2.4}$$

Where $(E_{v(lx)})$ is the illuminance in $lux(lx)$. $(\eta_{(lm/W)})$ is the luminous efficacy of the available light source in lumens per watt (lm/W). (A_{m^2}) is the area of the solar cell in square meters (m^2).

2.1.2 Microscale Thermoelectric Transcducer

The thermoelectric transducers (so called thermoelectric generators(TEG)) consist of multiple couples of p-type and n-type thermoelectric slices. These slices are connected thermally in parallel, however they are connected electrically in series. The way of alignment used in the structure is to save the surface area of the device. The thermal energy generated through the thermal gradient of seebeck effect [19] across the parallel slices, this effect forces the free carriers (i.e. electrons and holes) to drift towards the low temperature side, this motion produces a flowing current in the structure. It should be stated that micro-scale thermoelectric based harvesters are convenient for human-powered biomedical implants, as the thermal gradient between a human and air can be easily transformed into electrical power. Figure 2.4 shows the structure of a thermoelectric transducer.

The TEG open circuit voltages value is depending on the number of slices used, temperature gradient(ΔT) and Seebeck coefficient of the material used. A commercial (MPG-D655) TEG by Micropelt.Inc [20] is a live example for microscale

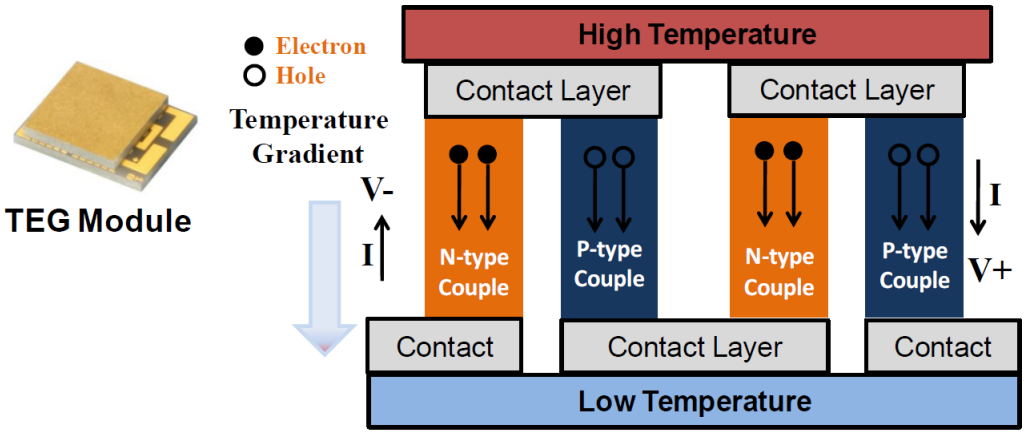


FIGURE 2.4: Device photograph of a thermoelectric Generator(TEG) and a cross section view with operation [10]

TEGs. It consists of 288 thermoelectric pairs, its open circuit voltage is $80mV/K$. Simulation results shown in Figure 2.5 are developed by a simulation tool developed by the company for simulating their products.

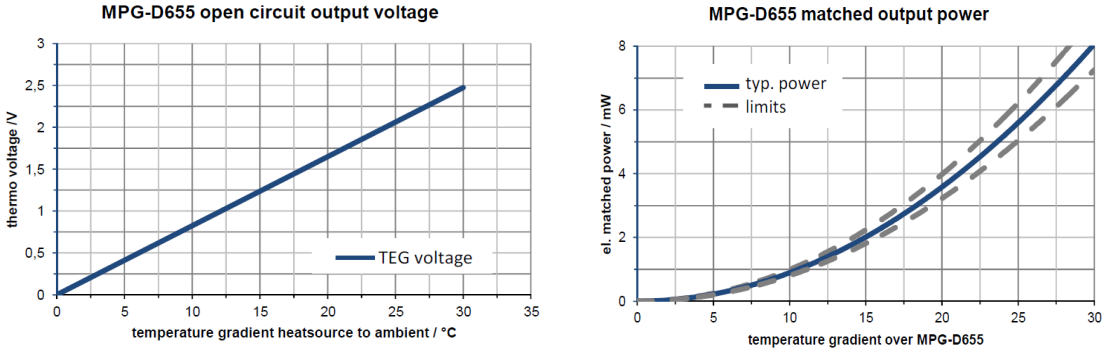


FIGURE 2.5: Simulation results for MPG-D655 (a)Open circuit voltage. (b)Matched output power [20]

2.1.3 Micro-scale Mechanical Energy Transducers

Mechanical vibrations occur in a a lot of surrounding applications like household machines. Microwave ovens and electrical sweepers are examples of those machines. According to a detailed study [11], results shows that vibration frequency

typical values is $\leq$ 200 Hz. Estimated output power from a mechanical-based energy harvesters of a microwave oven equals to $116\mu W/cm^3$.

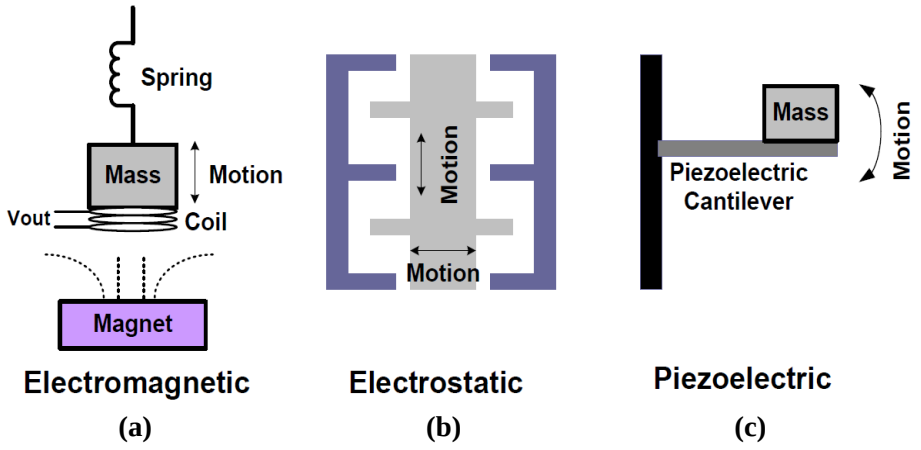


FIGURE 2.6: Three Kinds of Micro-Scale Vibration Energy Transducers [10]

Electromagnetic, electrostatic and piezoelectric conversions are three forms for mechanical energy transduction, as shown in Figure 2.6. The first type 2.6(a) produces an AC current passing through a coil, whenever there is a relative displacement between the coil and magnetic field. Due to the existence of bulky moving spring and magnet, this method is hard to be implemented in micro-scale energy harvesting systems [21]. Electrostatic conversion 2.6(b) is maintained by a vibration-driven variable capacitor. Vibrations lead to the capacitance variation and cause an electrical energy transduction [22]. This electrostatic mechanism is convenient for micro-scale system integration, but an additional voltage excitation is required for system ramp-up. Piezoelectric transduction 2.6(c) use materials with piezoelectric properties. Piezoelectric energy transducer utilizes the strain and deformation of a piezoelectric material. For example, low level mechanical vibrations leads to the continuous motion of mass, which is amounted on the surface of a piezoelectric cantilever. As the piezoelectric approach does not require a separate voltage source for starting up and hence is easily integrated in compact systems, this method has been gaining increasingly attentions.

2.1.4 Micro-Scale Electromagnetic Energy Transducer

There are many radio frequency (RF) signals such as Wi-Fi and radio broadcasting in our daily surroundings. Antenna is commonly used as a RF energy harvesting transducer, which converts ambient electromagnetic energy into electrical energy. Generally, an antenna is designed for a specific carrier frequency or a narrow carrier frequency band. Figure 2.7 shows a photograph of a typical antenna and its equivalent circuit model.

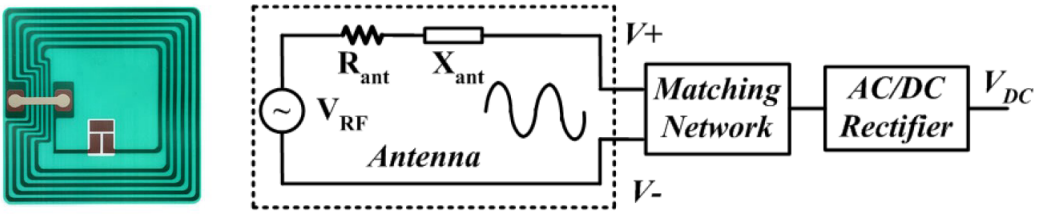


FIGURE 2.7: The Photograph of an Antenna and its Electrical Circuit Model [10]

The equivalent circuit of an antenna consists of a RF-induced voltage source (V_{RF}) and internal impedance (R_{ant}) and (X_{ant}). The magnitude of RF-induced voltage source depends on the ambient electromagnetic strength and the antenna design parameters (i.e., material, dimensions, thickness, and the number of turns). The internal impedance is sensitive and varying with the received signal frequency. As the output signal provided from an antenna is an AC signal, an AC/DC rectifier is required to perform rectification. As illustrated in Figure 2.7 to transfer maximum power from an antenna, impedance matching between the antenna and its matching network is of great importance.

2.2 DC-DC Power Converter Design

DC-DC converters, also known as power converters, have three different types. The low drop-out (LDO) voltage regulator is one of these types. LDO has the

advantages of offering low power supply noise, since it is a switching-free topology. However, its drop out voltage has to be small to provide high efficiency. It also do voltage step-down only. The second type of the power converters is the DC-DC buck-boost converters which can do voltage step-up or step-down conversion. They generate high power efficiency provided that the inductor used has a high quality factor, so they have to be implemented off-chip. This type of converter requires large area. It also generates electromagnetic interference (EMI) and power supply noise. The third type is the switched capacitor charge pump (SCCP). SCCP consists of MOS transistors and capacitors only and can do voltage step-up or step-down. SCCP has the advantage of low cost integration since there are no coils used. SCCP needs two non-inverting clock phases in order to do power conversion process.

The output voltage level of both transducers and the buffer determines whether step-up or step-down is taking place inside the power converter. For non-stacked DC output transducers with very low output voltage, step-up conversion is required to boost the voltage level of energy transducers. However, extracting energy from such ultra-low voltage sources dictates careful circuit design [23]. If an energy transducer outputs AC power, the power converter should perform AC-DC rectification before making DC-DC conversion.

The efficient design of multiple-input multiple-output (MIMO) power converters for hybrid energy transducers has also been explored [24],[25],[26]. The combination of multiple heterogeneous energy transducers can potentially decrease the temporal variability in generated power and increase the total amount of harvested energy in a given time duration, especially if the modalities involved are carefully selected. The basic idea of designing MIMO power converters is to merge multiple power converters into one combined structure using a single inductor. Using only one inductor decreases system cost and increases the power conversion efficiency. The drawback of such approach is the increase in the circuit design complexity and the overhead of managing power flow paths from multiple sources.

2.2.1 Charge Pump Topologies

There are mainly three kinds of charge pump topologies in literature for power conversion. The first proposed charge pump circuit is a Dickson charge pump that has a linear topology [27]. Moreover, a variety of optimized linear charge pumps were presented for low voltage applications [28],[29]. Figure 2.8 shows an N-stage linear charge pump that has an ideal voltage step up ratio of $(N+1)$. The input and output voltages of this charge pump are V_{IN} and V_{OUT}, respectively. ϕ and ϕ_B are non-overlapping clock signals for turning on/off these transistor switches. During each clock cycle, the charge from the previous stage is stored on an internal capacitor $(C_1, C_2 ... C_N)$ and is then transferred to the subsequent stages. At the final stage, the harvested charge from the previous stages is dumped into the energy buffer (C_{OUT}) for storage.

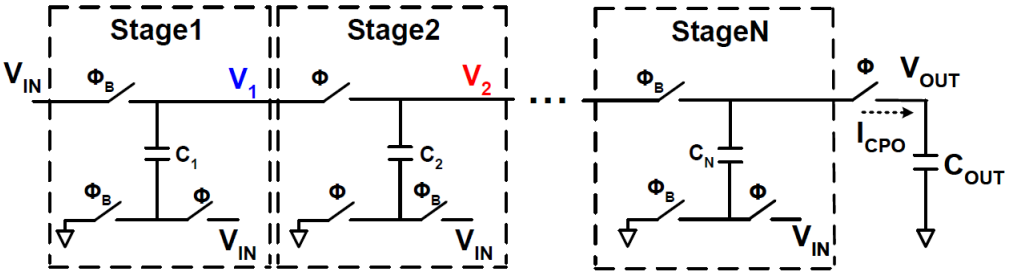


FIGURE 2.8: Schematic of an N-stage Linear Topology Charge Pump [10]

The average output current from an N-stage linear charge pump is given by [29],[30]:

$$I_{CPO} = f_{clk} Q_{avg} = \frac{1}{N} C f_{clk} \left[(N+1)V_{IN} - V_{OUT}\right] \tag{2.5}$$

This equation is derived based on the assumption that complete charge sharing is guaranteed within each clock cycle. It reveals a linear relationship between the charge pump output current (I_{CPO}) versus the switching frequency (f_{clk}), when the capacitor (C), energy transducer voltage (V_{IN}) and energy buffer voltage

(V_{OUT}) do not change. When the clock frequency is low, the output current varies linearly with the applied clock frequency. However, when the frequency increases beyond a certain value, the charge sharing becomes incomplete. Hence, the linear relationship between output current and switching frequency does not hold beyond the knee frequency.

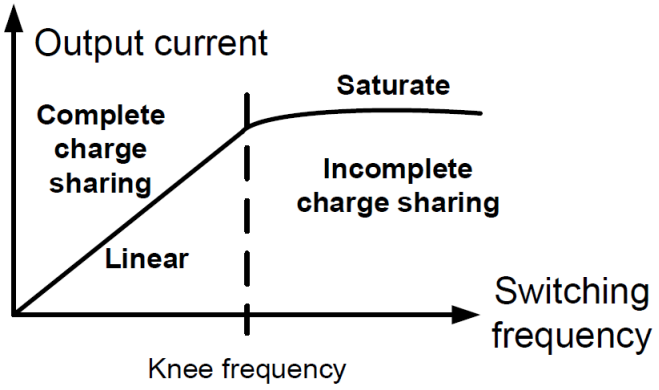


FIGURE 2.9: Output Current of Charge Pump vs. Switching Frequency [10]

Figure 2.9 illustrates the variation of charge pump output current with the switching frequency. The interface frequency between complete or incomplete charge sharing is marked as "knee frequency". Note that as an intrinsic property of a charge pump, the knee frequency is determined by the time constant of charge sharing paths.

In order to further improve the power conversion efficiency, cross-coupled charge pumps were proposed [31],[32]. Figure 2.10 shows the schematic of an N-stage cross-coupled charge pump. As shown in Figure 2.10, the basic component is one stage cross-coupled voltage doubler, where the internal voltages at nodes N_1 and N_2 perform the gate control for transistors M_1 and M_2. Charge pumps with higher voltage conversion ratios can be implemented by connecting multiple voltage doublers in series. However, as we will show later in this chapter, when the output voltage of energy transducer is very low (e.g., V_{IN} is lower than the threshold of transistors), the cross-coupled configuration fails to function normally. Thus, very little power can be extracted into the power converter and transferred to output.

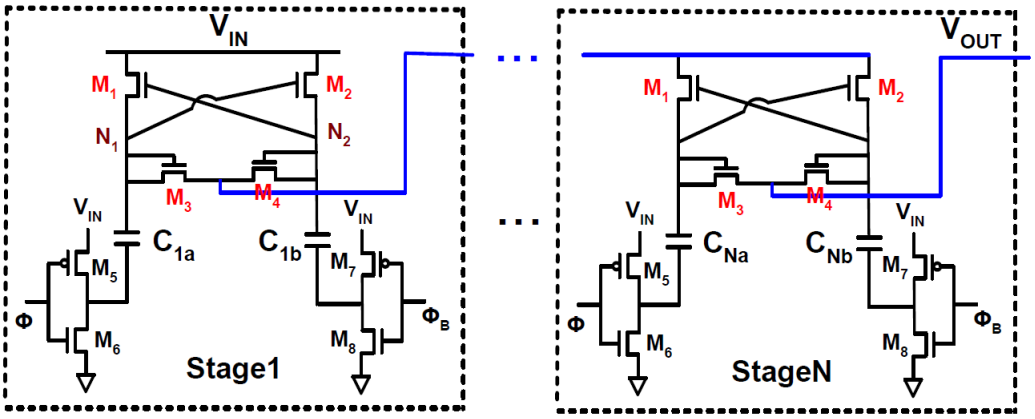


FIGURE 2.10: Schematic of an N-stage Cross-Coupled Charge Pump [10]

Exponential topology charge pump was firstly proposed for area-critical power conversion applications [33],[34]. Since its voltage conversion ratio exponentially increases with the number of stages, this topology is the most cost effective option for voltage step-up. Figure 2.11 shows the circuit structure of an N-stage exponential topology charge pump with an ideal voltage conversion ratio of 2^N. As we will discuss later in this chapter, the power transfer capability of an exponential topology charge pump is restricted and impeded by the first stage, because the charge sharing paths from input terminal only exists in the first stage. This implies that the power transfer capability of an exponential charge pump does not scale up with the increase of its number of stages.

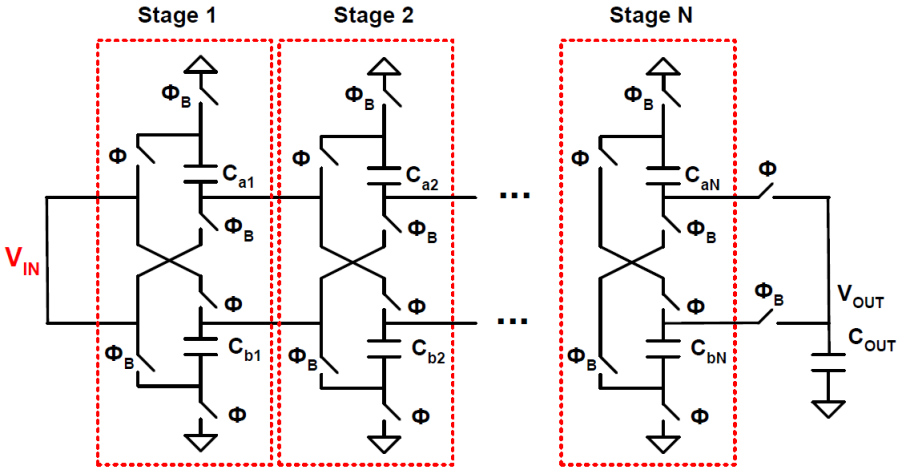


FIGURE 2.11: Schematic of an N-stage Exponential Charge Pump [10]

2.2.2 Inductive DC/DC Converters

Inductive DC/DC converter employs switching action on an inductor to transfer power from an input energy source to an output load. The energy from an input energy source is first transferred to an inductor for temporal energy storage, then it is switched from the inductor to the output load.

If the input voltage is higher than the output voltage, a buck converter is required and its schematic is shown in Figure 2.12. Transistor switches (S_1 and S_2) are controlled by clock signals to turn on/off periodically. Consider the start of a period $t = 0$ and the switch S_1 is closed (S_2 is opened). The converter enters state 1. The voltage across the inductor (V_L) is $V_{IN} - V_O > 0$, and the inductor current i_L increases linearly. When the duty cycle DT expires, S_1 is opened and S_2 is closed, the power converter enters state 2. The positive terminal of the inductor is now connected to GND, and the voltage V_L is $0 - V_O < 0$, and the inductor current i_L decreases for the rest of the period. Figure 2.12 also shows the inductor current waveform in both states. The switch $S1$ is the controlling switch that defines the duty cycle and can be implemented by an MOS transistor, as shown in Figure 2.12. For the switch S_2, it is observed that the inductor current at the end of state 1 is $i_L(DT) > 0$, and when S_2 is closed, current is forced from the GND to flow through the inductor to the output.

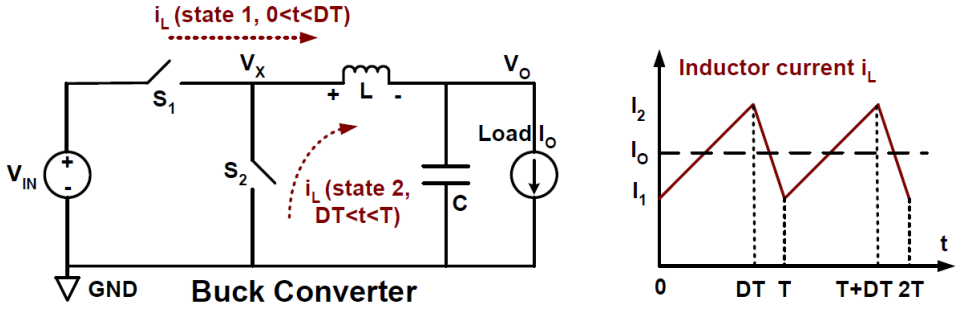


FIGURE 2.12: Schematic of a Buck Converter and Inductor Current Waveform [10]

If input voltage is lower than output voltage, a boost converter is required and its schematic is shown in Figure 2.13. Consider the start of a period $t = 0$ and the switch S_1 is closed (S_2 is opened). The converter enters state 1. The voltage across the inductor V_L is $V_{IN} > 0$, and the inductor current i_L increases. When the duty cycle DT expires, S_1 is opened and S_2 is closed, the converter enters state 2. The positive terminal of the inductor is connected to V_{IN}, and the voltage V_L is $V_{IN} - V_O < 0$, and the inductor current i_L decreases for the rest of the period.

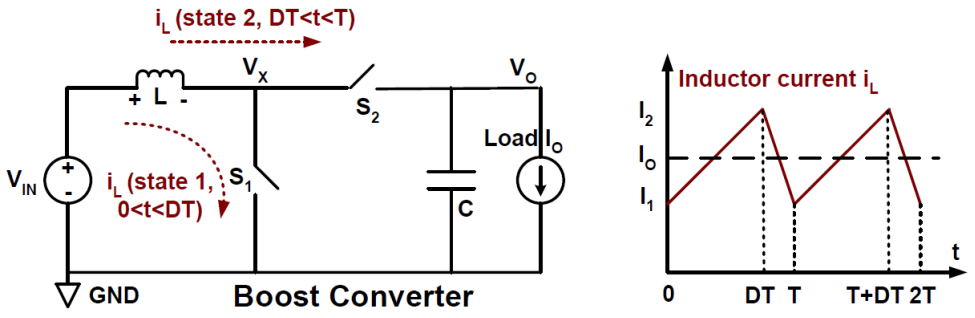


FIGURE 2.13: Schematic of a Boost Converter and Inductor Current Waveform [10]

Figure 2.14 shows a step up/down converter that gives an output voltage that is of opposite polarity of the input voltage V_{IN}. This topology is well known as the buck-boost converter. In order to keep i_L flowing in the same direction as in state 1, charge is taken out of the capacitor in state 2, therefore, the output voltage is negative ($V_O < 0$).

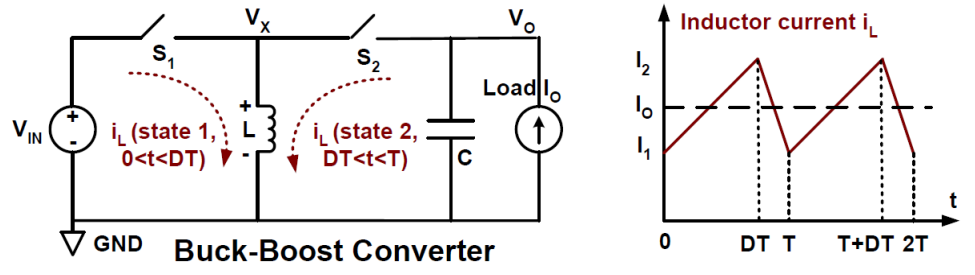


FIGURE 2.14: Schematic of a Buck-Boost Converter and Inductor Current Waveform [10]

For all three kinds of inductive DC/DC converters, the controlling switch S_1 is usually implemented by a large transistor, while the switch S_2 can be implemented

by a diode or a transistor. A diode can be viewed as a unidirectional switch that only allows current flowing in one direction. Depending on the load current value (I_O), there are two operation modes for inductive power converters. When load current is large enough, it operates in continuous conduction mode (CCM), as shown in Figure 2.12. Let us consider decreasing the load current I_O. The whole i_L waveform is shifted down and lower than before. If the load current is further decreased, eventually, the valley of i_L (I_1) will touch zero, and the converter is operated in the boundary conduction mode (BCM) as shown in Figure 2.15. Further decreasing the load will drive I_1 below zero, if a unidirectional switch (diode) is used or a reverse current control is applied for transistor switch S_2, i_L will not go negative and just stay at zero for the rest of the period. In this case, the power converter is operated in discontinuous conduction mode (DCM). Using a diode to implement the switch S_2 is a common choice in industry, as a diode is much cheaper than a power transistor. However, the diode drop of at least $0.3V$ reduces the power efficiency for low-power efficient applications, where the diode should be replaced by a power transistor for higher efficiency.

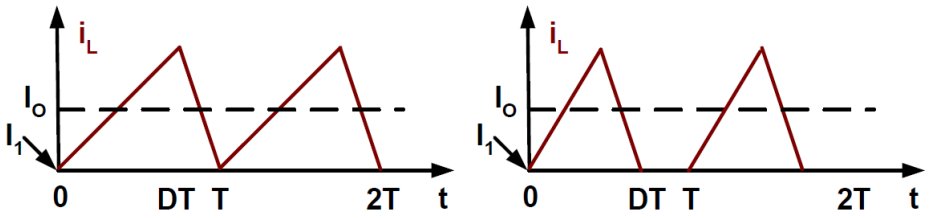


FIGURE 2.15: Boundary Conduction Mode and Discontinuous Conduction Mode [10]

An ideal DC/DC converter could achieve 100% power efficiency, if design components (inductor, capacitor and switches) are lossless. However, due to the parasitic resistances, a practical design suffers from significant switching loss and conduction loss, which reduce the power efficiency. Note that switching power loss is due to charging and discharging the gate capacitance of the switches, conduction power loss is due to the parasitic resistances of the switches, the inductor and the capacitor.

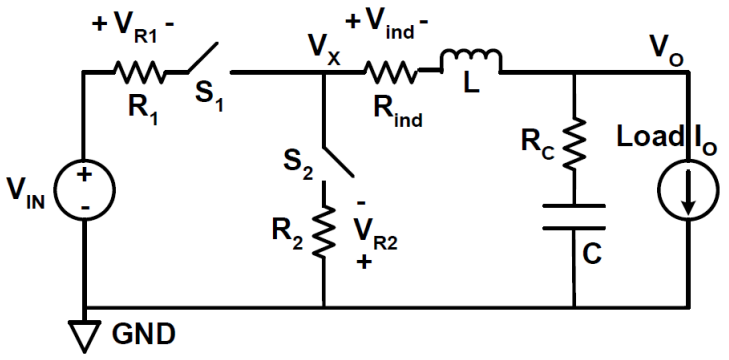


FIGURE 2.16: Buck Converter Circuit with Parasitic Resistances [10]

Figure 2.16 shows a practical circuit of buck converter with parasitic resistances. These parasitic resistances affect the current slopes in all states. In state 1, the switch S_1 is closed, and the voltage across the inductor V_L is $V_{IN} - V_{R1}(t) - V_{RL}(t) - V_O$. In state 2, the switch S_1 is open, and the voltage across the inductor V_L is $0 - V_{R2}(t) - V_{ind}(t) - V_O$.

2.3 Maximum Power Point Tracking Algorithms

As we have discussed before, the maximum output power point of a micro-scale energy transducer varies with the strength of the environmental energy sources (e.g., light irradiance for solar cell). It is desirable to ensure that energy harvesting systems operate at the maximum power point of energy transducers at any time, in order to maximize the amount of energy extracted. The most important design consideration for MPP tracking in micro-scale energy harvesting systems is to ensure that minimal power overhead is introduced. This is because the output power from a micro-scale energy transducer is very limited to begin with (in the range of tens of μW to a few mW), as much of this power as possible should be delivered for use by the output loading. This section provides an overview of low-overhead MPP tracking schemes that are well suited for micro-scale energy harvesting systems. The choice of which specific MPP tracking approach to

use depends on several factors such as the voltage range, cost constraints, power overhead, design complexity, whether the system is on-chip or off-chip, etc.

2.3.1 Design Time Component Matching

DTCM is a very simple approach and is adopted in the Heliomote solar harvesting wireless sensor node [15]. In this approach, the output of the solar cell is directly connected to a rechargeable battery with appropriate reverse current protection, therefore, the battery terminal voltage dictates the operating point of the solar cell. Near MPP operation is achieved through careful selection of the specific solar cell and battery used. For example, the Heliomote used two NiMH batteries in series, which resulted in a terminal voltage of around $2.8V$ when charged. The adopted solar panel had its MPP that varied between $2.5 - 3V$, therefore, the Heliomote always operated within a few tenths of a Volt of the solar cell's MPP. Although the approximate nature of this method results in a sub-optimal operating point, there is zero tracking overhead. This enables this scheme to perform almost as well as a more precise MPP tracking method that has additional power overhead in the tracking circuitry.

Clearly, this method is not applicable if other system constraints (e.g., size) mandate that only single junction solar cell can be used, where the solar terminal voltage is lower (e.g. $0.5V$) than the minimum operating voltage of a battery (e.g., $1V$). In addition, a super-capacitor terminal voltage usually has a larger variation range. Thus, the DTCM approach results in a larger deviation from the exact MPP point, when a super-capacitor is used as the energy storage buffer.

2.3.2 Reference Voltage Tracking

This maximum power point tracking method originated from empirical data analysis. Experimental measurements on some energy transducers have found an

approximately linear relationship between the MPP voltage of an energy transducer and its open circuit voltage (V_{OC}). This voltage ratio is about 0.75 for solar cells and 0.5 for thermoelectric generators. Based on the straightforward linear relationship, a simple method to estimate V_{MPP} at runtime is to momentarily disconnect the energy transducer from the load (causing an open circuit for the energy transducer) and sense V_{OC}, from which V_{MPP} can be computed. The energy transducer is made to operate at V_{MPP} by the interface circuit connected to it, which presents the appropriate load impedance to the energy transducer. This method is suitable for micro-scale energy harvesting systems because it involves simple open-loop control and does not require any intensive computations like hill climbing algorithms. The drawback of this approach is that the energy transducer is periodically disconnected from the load, which causes temporary power loss to the load. Further, there is a hardware cost (switches and control generation circuitry) involved in time multiplexing between normal operation and the open circuit mode of operation. Figure 2.17 shows a generic block diagram for the reference voltage tracking system.

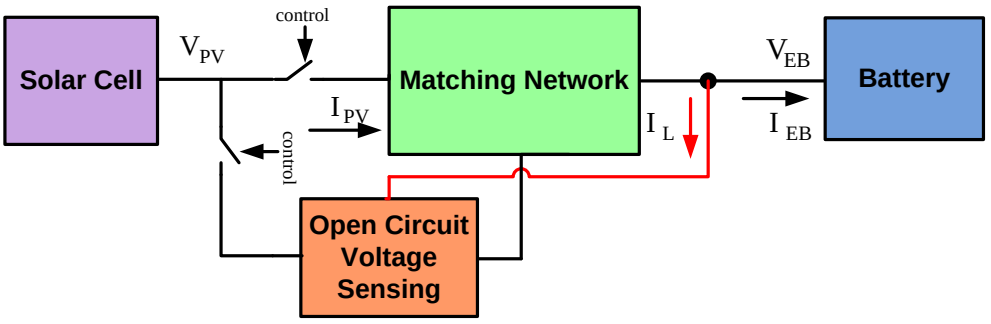


FIGURE 2.17: Reference Voltage Tracking System Block Diagram

To address these disadvantages, an improved design was presented in [35], where an additional energy transducer is used in the system as a pilot cell. The open circuit voltage of the pilot cell is used in place of the open circuit voltage of the main energy transducer. This eliminates the necessity for doing any open circuit voltage sensing on the main energy transducer. However, with this approach, the pilot cell should be carefully chosen to ensure that its feature is close to that of the

main energy transducer. More importantly, this approach is hard to implement for system-level MPP tracking, since the system MPP voltage is no longer linearly dependent on the open circuit voltage, when the impact of a power converter is considered. Figure 2.18 shows a generic block diagram for the pilot-based reference voltage tracking system.

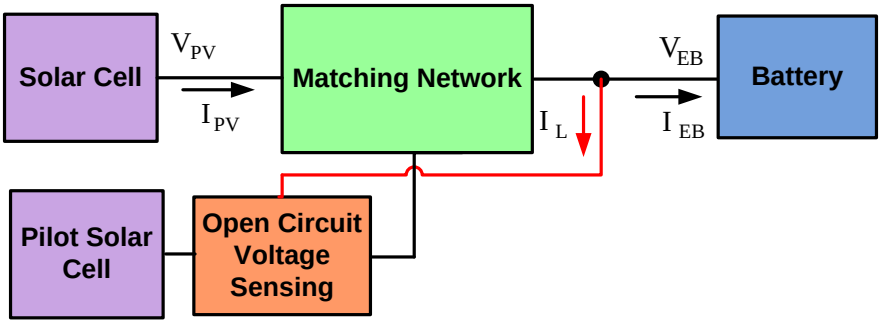


FIGURE 2.18: Pilot-Based Reference Voltage Tracking System Block Diagram

2.3.3 Hill-Climbing / Perturb-and-Observe

Hill-climbing and Perturb & Observe methods essentially have the same operating principle. Both methods adopt an iterative trial-and-error approach to track the MPP. During normal system operation, an MPP tracking procedure is periodically initiated. This procedure involves applying a small perturbation to the interface circuit either by varying the duty cycle of a boost/buck converter [36] or the switching frequency of a charge pump [30],[37]. This perturbation results in a small change in the operating point of the energy transducer as well as its output power. Assume, for illustration, that the perturbation results in an increase in the terminal voltage of the energy transducer. The output power is recorded and compared to the power output before the perturbation. If the perturbation results in a power increase, another perturbation in the same direction is performed. If the perturbation results in a power decrease, a perturbation in the opposite direction is performed that results in a decrease in terminal voltage. The process

is continuously repeated until the MPP is reached. In steady state, the system oscillates around the MPP.

There is a trade-off in the perturbation step size. A large step size corresponds to a rapid response to the environmental energy variation and faster convergence, but oscillates with a large swing near the MPP. A small step size can minimize the oscillation swing, but slow down the tracking speed and increase the tracking time. The iterative control procedure is usually implemented in software running on a micro-controller. To minimize the power and cost overhead introduced by a micro-controller, the researchers implement the P&O algorithm using a dedicated decision generation circuit [30],[37]. Figure 2.19 shows a generic block diagram for the Hill-Climbing / Perturb-and-Observe System. It can be shown that the control unit consists of three main blocks. The current/voltage sensing block is used for power sampling. The decision generation block is used for forcing the direction of perturbation towards the MPP. The voltage controlled oscillator is used for controlling the power converter for power matching in case of using a charge pump based power converter.

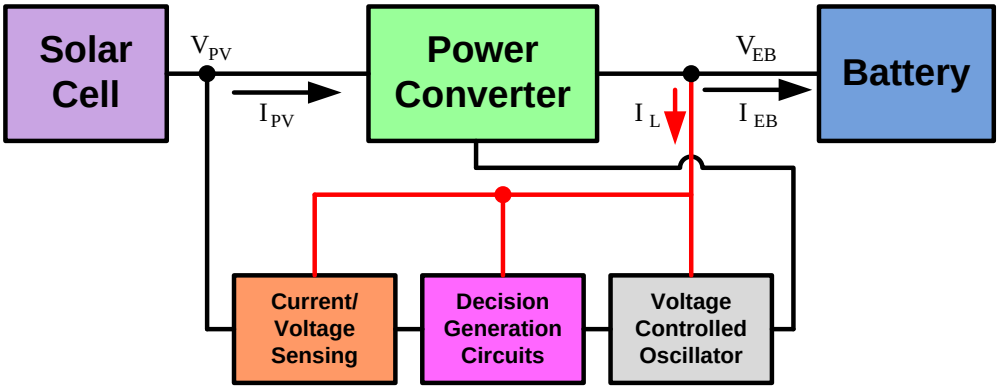


FIGURE 2.19: A Generic Block Diagram for Hill-Climbing / Perturb-and-Observe System

2.4 Application Unit Characterization

A typical wireless sensor node (WSN) can be modeled as load with four different states: transmitting, receiving, idle and off. Most of the time, a WSN is working in off mode. During a small period of time, it can do data processing, transmission and reception [17]. So, it can be concluded that the average load current that a WSN consumes is relatively small. Figure 2.20 shows a simplified load power model.

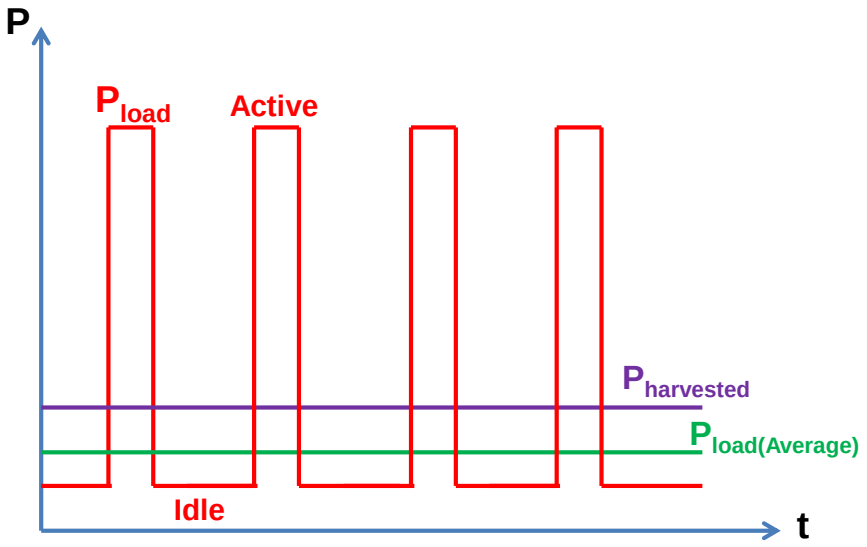


FIGURE 2.20: A Typical Wireless Sensor Node Power Characteristics

The power converter generates power greater than or equal to the average power required by the WSN ($P_{harvested} \geq P_{load(Average)}$). The main problem comes in the active mode, when huge power needed instantly to be supplied. The active mode power is higher than the harvested power by several orders of magnitude, that's why a super-capacitor or a rechargeable battery should be used in order to save the extra power generated during the idle mode. However, it should be guaranteed that the stored energy in the super capacitor is larger than the

difference between the instantaneous load power and the average harvested power ($E_{stored} \geq E_{load} - E_{harvested}$)[17].

Chapter 3

Exponential Tracking Based Microscale Energy Harvesting System

Different efforts were done on the maximum power tracking control. A typical energy harvester could be found in [37], where the design is mainly based on increasing the output current of the charge pump. So a current sensor is placed at the output to sample the current, then a decision generation circuit is used to find the next step whether to increase the voltage controlled oscillator (VCO) frequency or decrease it. This architecture is good in terms of PV cell voltage tracking efficiency, as it's a tracking system that adapts itself to the new operating point. It turns out to consume high power and area, due to the current sensing module which is a power hungry block, and a decision generation circuits to find the new operating point. The algorithm used in [37] is the hill climbing technique. Figure 3.1 shows the complete circuit realization of the control unit proposed in [37].

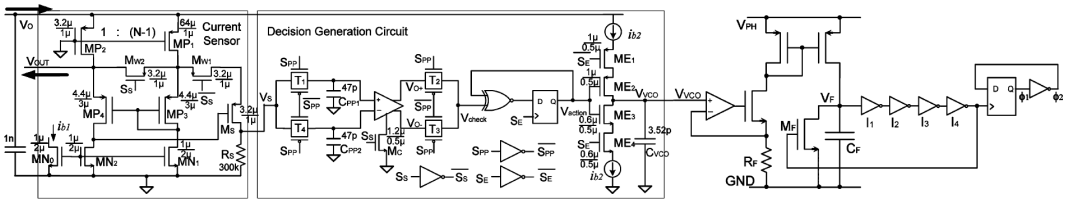


FIGURE 3.1: Control Unit implementation of [37]

Different approach is discussed in [38]. A DC-DC buck converter is used as a power converter, but it is not preferred to use an off-chip coil due to the area limitations of the energy harvester and the wireless sensor node as well. The design is based on ad-hoc adaptive technique, it dictates using of digitally-assisted circuitry for maximum power delivery that consumes extra power. Moreover, it uses current sensing circuits which are not desired in energy harvesting modules due to their large power consumption.

Another technique used for tracking is found in [39]. The approach is based on investigating the system design equations and finding a compact relationship between PV cell terminal voltage and the target operating frequency required for maximum power transfer. This technique is based on the negative feedback automatic tracking. The main advantage of this design is that there is no need for extra tracking circuitry. This design has two main disadvantages, first, the hardware implementation is mirror for an approximated relation which limits the dynamic range of the harvester, second, the author did not mention the design reliability across process corners which raises doubts about the physical verification. Figure 3.2 shows the complete circuit realization of the control unit proposed in [37]. It is worth stating that the control unit design approach is based on approximating the optimum frequency-voltage relationship in to linearized terms shown in Equation 3.1 , which is not a good option for efficient tracking over a wide dynamic range.

$$f_{clk,opt} = A * f(V_{MPP}) + B * f(V_{MPP})^2 \tag{3.1}$$

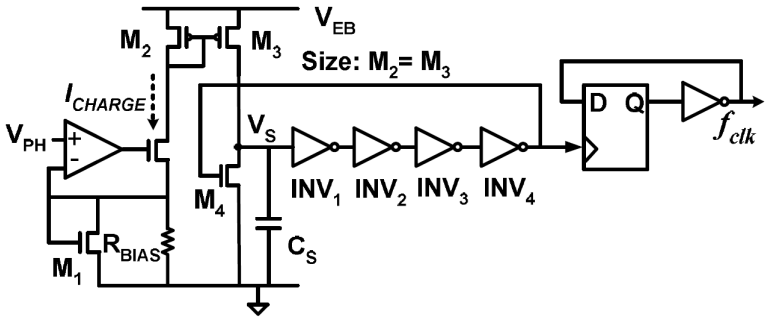


FIGURE 3.2: Control Unit implementation of [39]

In this Chapter, a new technique for maximum power point tracking is proposed. The idea is based on forcing the control unit to operate in the sub-threshold mode. This technique guarantees low power consumption for the control unit, thus an increase in power efficiency is predictable. The technique has two main drawbacks, first, the control unit suffers from process variations which changes the operating point of the system, accordingly the system is pulled out of tracking. This problem is fixed by using the adaptive body bias techniques as circuit techniques to make a variation-tolerant design. The second problem is that maintaining the control unit at the sub-threshold mode forces the charge pump flying capacitances to an increase in area, since the frequency range is shifted down. However, the photo-voltaic cell should see a matched time-varying input impedance all the time for efficient maximum power delivery. System design is based on [39]. System equations are highlighted in details, and control unit equations are derived. Since the design is suffering from process variations, adaptive body bias techniques [40] are used for a reliable design.

3.1 System Analysis

Figure 3.3 shows the block diagram of the micro-scale energy harvesting system[39]. This system is applicable to the solar energy transducers, and any other transducers that exhibits a maximum power trajectory across ambient power changes like

thermoelectric transducers.

Solar cell (PV cell) is used to convert the incident light power into electrical power. The power converter receives the electrical power and converts it to the energy buffer (super-capacitor or a rechargeable battery). Maximum power locking is maintained through the control unit, which directly sense the solar cell terminal voltage and force the system at its optimal performance. The output current I_O is divided into two portions; I_{EB} which is the current flow in the energy buffer, and I_L that flows in the control unit. it should be concluded that the power consumption in the control unit should be minimized for high power efficiency, and at the same time it should locks the PV cell at its maximum power capability.

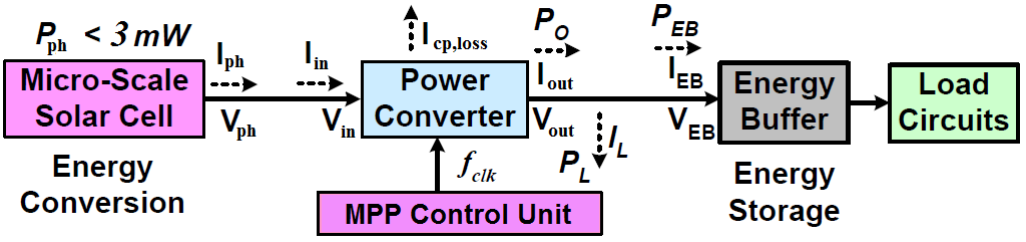


FIGURE 3.3: Block Diagram of the Solar Energy Harvesting System

3.1.1 Solar Cell Modeling

The electrical characteristics of a solar PV cell is modeled as [41]:

$$I_{ph} = I_{ph,sc} - I_{sat}\left[e^{q\left(\frac{V_{ph}+I_{ph}R_s}{n_dKT}\right)} - 1\right] - \frac{V_{ph}+I_{ph}R_s}{R_p} \tag{3.2}$$

In case of unloaded solar cell: $I_{ph} = 0$,$V_{ph} = V_{oc}$, one could get:

$$I_{ph,sc} = I_{sat}\left[e^{q\left(\frac{V_{oc}}{n_dKT}\right)} - 1\right] - \frac{V_{oc}}{R_p} \tag{3.3}$$

Equation 3.3 shows that increasing the input irradiance produces higher photodiode current and higher open circuit voltage V_{oc} as well. V_{oc} parameter is a good indicator for a light intensity variation. By substituting 3.3 in 3.2, and by ignoring R_s and R_p, since R_s is very small and R_p is very large, one could get:

$$I_{ph} = I_{sat}\left[e^{q\left(\frac{V_{oc}}{n_d KT}\right)} - e^{q\left(\frac{V_{ph}}{n_d KT}\right)}\right] \tag{3.4}$$

3.1.2 Charge Pump Power Converter Modeling

The power converter used in the design is a switched capacitor charge pump for cost effective design. The power converter is connected to a single solar cell that gives too low terminal voltage to supply the application units, so a voltage boosting operation should take place for generating a feasible supply voltage. The output and input currents of a typical charge pump is modeled as:

$$I_{out} = f_{clk} Q_{avg} = \frac{1}{M-1} f_{clk} C\left(M V_{in} - V_{out}\right) \tag{3.5}$$

$$I_{in} = M I_{out} + I_{cp,loss} = \frac{M}{M-1} f_{clk} C\left(M V_{in} - V_{out}\right) + f_{clk}\beta \tag{3.6}$$

Where M is the ideal voltage step-up ratio, C is the flying capacitance used in each stage, and f_{clk} is the switching frequency. V_{in} and V_{out} are the power converter‘s input and output voltages, respectively. β represents the power converter losses. Equation 3.6 is a generic expression for step-up power converters, it is applicable for linear or tree topology and for any input voltage level. The equivalent input impedance R_{in} of the power converter can be derived from Equation 3.7:

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{f_{clk}\left[\left(M - \frac{V_{out}}{V_{in}}\right)\frac{MC}{(M-1)} + \frac{\beta}{V_{in}}\right]} \tag{3.7}$$

As shown in 3.7, the input impedance of the charge pump is inversely proportional to the operating frequency. It should be noted also that this impedance is matched to the solar cell, so each input light intensity has a corresponding matched impedance value for maximum power. This impedance value has a corresponding frequency value, so the goal of the control unit is to search for the optimum frequency value that delivers maximum solar cell power at a given input light power.

3.2 Analysis of the Proposed Control Technique

In this section, a compact relationship between the operating frequency and the maximum power voltage value of the solar cell is derived based on the electrical models used in the previous section. The charge pump input current (I_{in}) is equal to the solar cell current (I_{ph}), and the charge pump input voltage (V_{in}) is equal to the solar cell voltage (V_{ph}). By equating Equation 3.6 by Equation 3.4, the charge pump switching frequency can be re-written as:

$$f_{clk} = \frac{I_{sat}\left(e^{q\left(\frac{V_{oc}}{n_d KT}\right)} - e^{q\left(\frac{V_{ph}}{n_d KT}\right)}\right)}{\frac{MC\left(MV_{ph} - V_{EB}\right)}{M-1} + \beta} \tag{3.8}$$

A simulation is done on cadence spice simulator using TSMC 65nm technology node to illustrate Equation 3.7. The photo-voltaic cell model in [18] is used. A tree topology charge pump is used as a power converter. Figure 3.4 shows the relationship between the solar cell voltage and the switching frequency at different

light intensities. It can be shown that at $f = 0Hz$, the charge pump voltage is equal to the corresponding open circuit voltage of the input light irradiance. When the frequency increases, the switching input impedance of the charge pump starts to decrease, thus the solar cell voltage starts to decrease as well. It can be concluded that that there is a point on each curve that corresponds to the maximum power out of the solar cell.

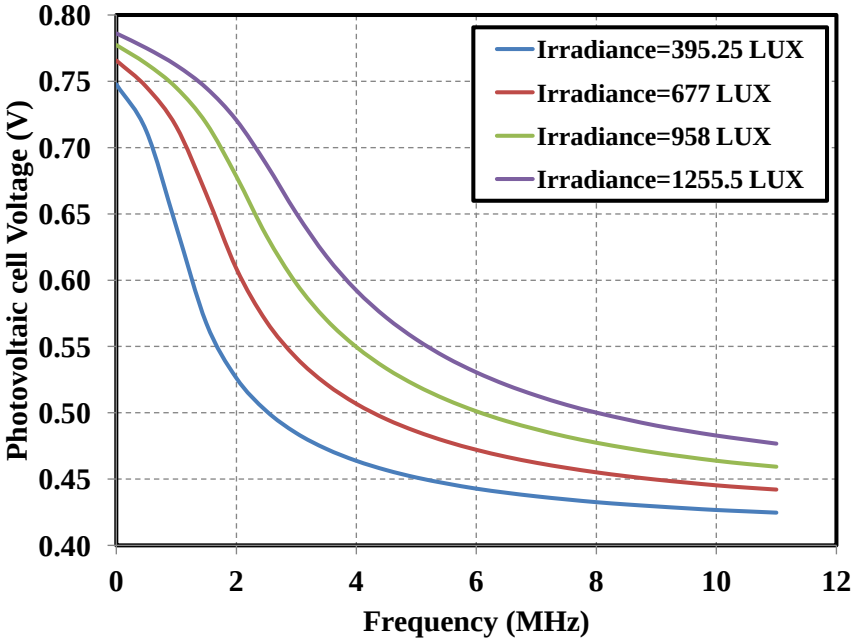


FIGURE 3.4: Relationship between solar cell voltage and power converter switching frequency

Figure 3.5 shows the output power across switching frequency for different light irradiance. It can be illustrated that there is a single frequency for each light intensity that delivers the maximum power, this frequency has a corresponding operating solar cell voltage (V_{MPP}), accordingly the control unit should operate at this point for any light intensity variation.

If ($V_{ph} = V_{MPP}$), this should guarantee a maximum power point operation on a closed loop system (i.e., as shown on a behavioral block diagram in Figure 3.6). Moreover, in literature research, the fractional open circuit tracking technique states that the ratio between the maximum power voltage value (V_{MPP})

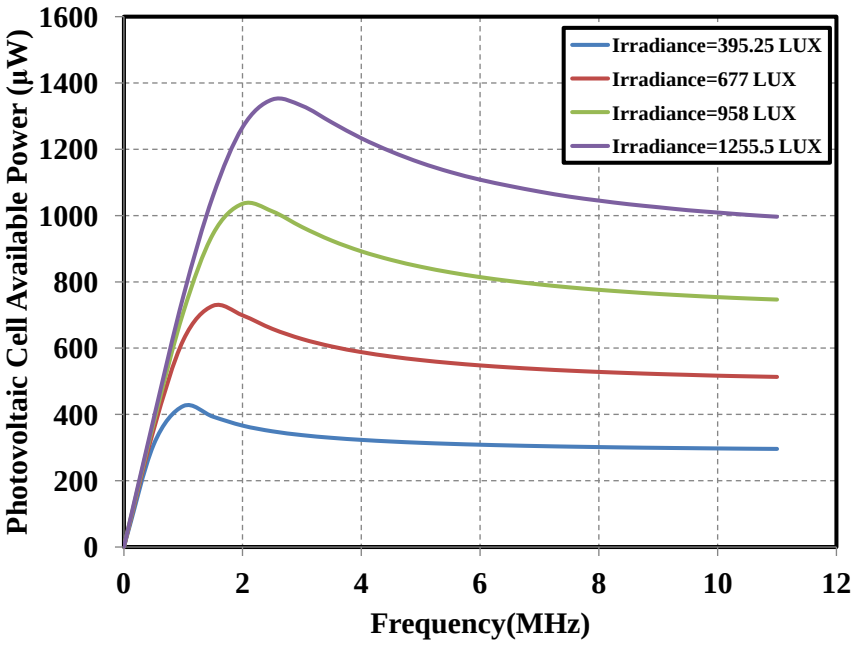


FIGURE 3.5: Relationship between solar cell available power and power converter switching frequency

and the open circuit voltage (V_{OC}) is constant and equal to (α) which is a device constant. So, if one substitute in Equation 3.8 by $V_{OC} = V_{MPP}/\alpha$, one could get the following:

$$f_{clk,opt} = \frac{I_{sat}\left(e^{q\left(\frac{V_{MPP}}{\alpha n_d KT}\right)} - e^{q\left(\frac{V_{MPP}}{n_d KT}\right)}\right)}{\frac{MC\,(MV_{MPP} - V_{EB})}{M-1} + \beta} \tag{3.9}$$

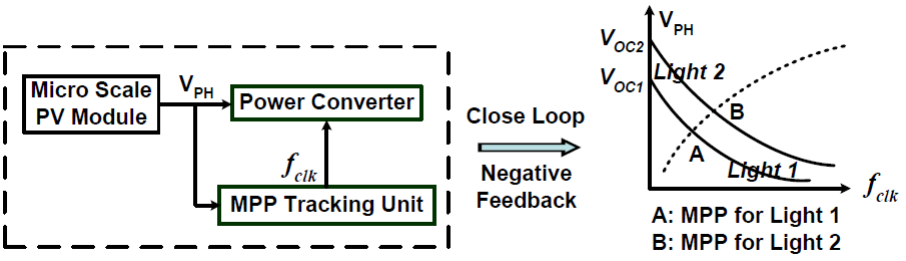


FIGURE 3.6: Closed loop Maximum power point process [10]

3.3 Control Unit Realization

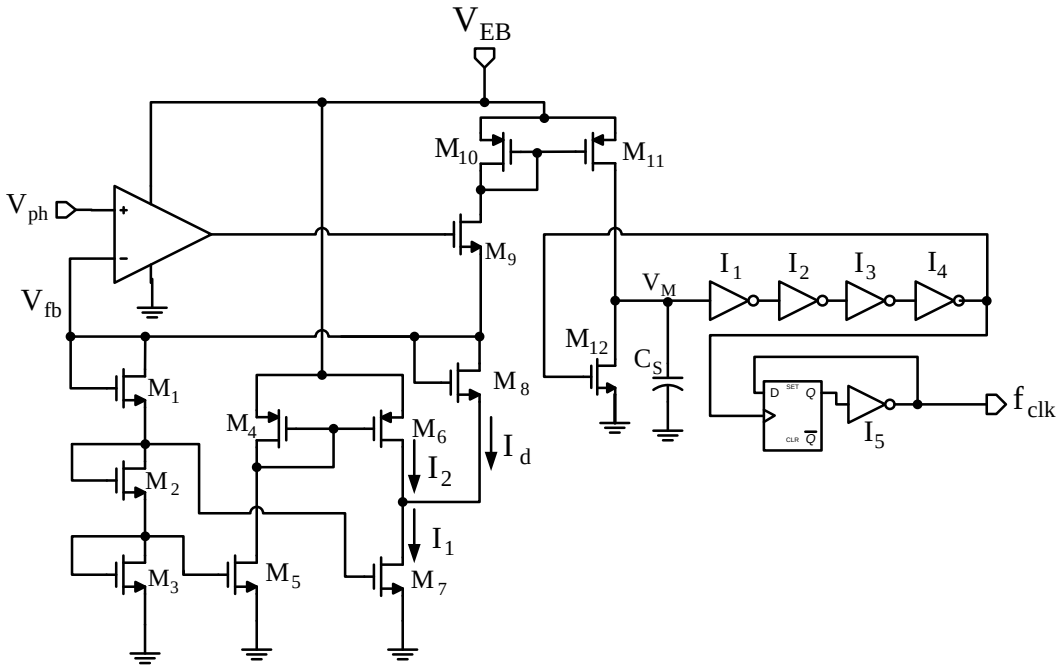


FIGURE 3.7: The proposed Sub-threshold Control Unit Implementation

In order to realize the relationship in 3.9, extra care should be taken in order to capture the relationship to a great extent without consuming power or area. Since, the relationship between the maximum power voltage value V_{MPP} and the switching frequency f_{clk} has an exponential nature, then the sub-threshold mode of operation is the best choice for realizing the hardware of the control unit. Sub-threshold operation guarantees two important characteristics for the energy harvesting systems. First, it adopts ultra low power operation for the control unit, so the overall power efficiency is expected to increase. Second, it will not take area overhead, since there is no need for sensing and decision generation circuits. A typical voltage controlled oscillator [37] is used with some modifications to maintain the sub-threshold mode of operation. Figure 3.7 shows the proposed sub-threshold mode based control unit. It can be shown that by some circuit techniques, optimal power extraction can be done.

3.3.1 Control Unit Analysis

In the previous section, a compact relationship is derived between the switching frequency (f_{clk}) and the maximum power point voltage value (V_{MPP}). In this part, analysis shows that the proposed circuit matches the exact compact derived equation of the control unit. Equation 3.9 has to be mapped to the voltage controlled oscillator (VCO) equation :

$$f_{clk} = \frac{I_d}{2V_M C_S} \tag{3.10}$$

The current (I_d) can be a subtraction of two currents using Kirchhoff's current law, they can be maintained by two transistors in the sub-threshold operation,so it needs careful design in order to verify the relation. Equation 3.9 can be approximated to:

$$f_{clk} \simeq K_1 \left(e^{\frac{K_2}{\alpha} V_{MPP}} - e^{K_2 V_{MPP}} \right) ; \alpha < 1 \tag{3.11}$$

Where (K_1) and (K_2) are constants. (V_{MPP}) is the locus of the maximum power solar cell voltage. (α) is the ratio (V_{MPP}/V_{OC}).

The transistor operating at sub-threshold region can be modeled as [42] :

$$I_D = I_s e^{\frac{V_{gs} - V_{th}}{nV_t}} \left(1 - e^{-\frac{V_{ds}}{V_t}} \right) \tag{3.12}$$

$$I_D \simeq I_s e^{\frac{V_{gs} - V_{th}}{nV_t}} \mid V_{ds} >> V_t \tag{3.13}$$

Where (V_{gs}) is the gate-source voltage. (V_{th}) is the threshold voltage. (V_t) is the thermal voltage. (I_s) is the transistor current at $V_{gs} = V_{th}$.

After substitution in Equation 3.10 by Equation 3.13, one could conclude the following:

$$f_{clk} = \frac{I_s \left(e^{\frac{V_{gs_7} - V_{th}}{nV_t}} - e^{\frac{V_{gs_6} - V_{th}}{nV_t}} \right)}{2V_M C_S} \tag{3.14}$$

By analogy between Equation 3.14 and Equation 3.9:

$$\begin{aligned} \frac{V_{gs_7} - V_{th}}{n} &= \frac{V_{MPP}}{\alpha n_d} \\ \frac{V_{gs_6} - V_{th}}{n} &= \frac{V_{MPP}}{n_d} \end{aligned} \tag{3.15}$$

$$\begin{aligned} V_{gs_7} - V_{th} &= \alpha \left(V_{gs_6} - V_{th} \right) \\ V_{eff_7} &= \alpha V_{eff_6} \end{aligned} \tag{3.16}$$

3.3.2 Control Unit Circuit Description

The proposed design shown in Figure 3.7 is divided in to two parts. The left part is the analog section. It translates the PV voltage change into a current change through the feedback Amplifier (i.e., the Op-Amp). The current mirror is used to replicate the current version to the right side. The right part is the digital section, it is a current controlled ring oscillator. The frequency range is controlled by the delay of the inverter, and frequency tuning is controlled by the

charging current of the capacitor (C_s). Since the output of the ring oscillator has a very small duty cycle (<10%), the output D-flip flop and the inverter are used to produce a 50 % duty cycle clock.

The charge pump needs two control clock signals. Since the output of the control unit is only one clock terminal, a non-overlap phase generator [29] is added to generate two inverted clock signals with non-overlapped periods. This is to prevent the switching leakage in the charge pump. A typical circuit is shown in Figure 3.8. The non overlap period is controlled by the delay of the cascaded inverters.

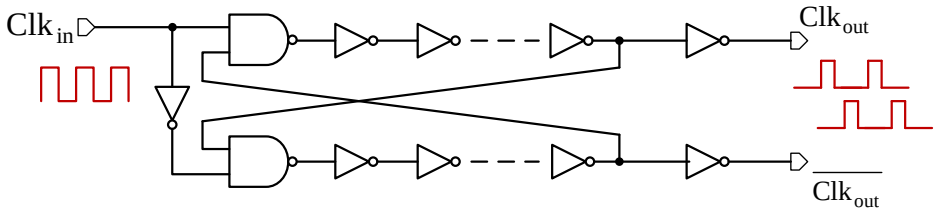


FIGURE 3.8: A Typical Non-overlapping Two Phase Generator

This design has an important advantage over the design in [39]; it approaches the ideal curve of the f-V relationship required for the maximum power delivery through realization of the frequency-Voltage exponential relationship, transistors (M_6, M_7) shown in Figure 3.7 are doing this job. They take their gate voltages through a potential divider, the divider is done by a stack of diode-connected transistors (M_1, M_2, M_3). The stack guarantees a sub-threshold operation for both (M_6, M_7), and also forces the overdrive voltage of those transistors to follow Equation 3.16. Since the Op-Amp has high open loop gain, thus, the voltage of (V_{ph}) is nearly equal the feedback voltage node. The current (I_d) is then mirrored to the digital right side, where there is a ring oscillator whose frequency is controlled by the transistor (M_8), the capacitor (C_S) and the voltage (V_M).

Figure 3.9 shows a DC sweep for the analog part of the control unit. During the Op-Amp lock range, the feedback voltage is changed linearly. (M_6) and (M_7) gate

voltages are derived from the feedback node (V_{fb}), where they are taking much smaller values. (I_d) is the subtraction of the two branches (I_1) and (I_2), it is the current in the left side of the current mirror. It can be seen that the generated current has an exponential nature with voltage variation.

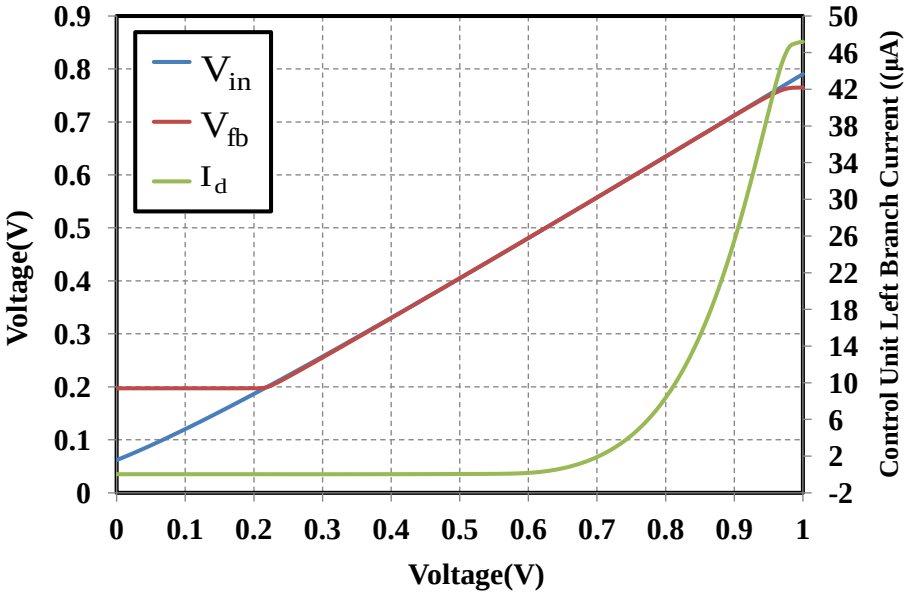


FIGURE 3.9: DC simulation for the left side of the control unit signals V_{in},V_{fb} and I_d

In order to show the effectiveness of the proposed design, another simulation is done comparing the design of [39] to the proposed one. The same simulation settings of Figure 3.9 is done for Chao Lu design [39] in Figure 3.10. The left branch current (I_d) of both designs is monitored between voltage range ($0.4V \rightarrow 0.8V$).

It can be shown that the proposed design shows an exponential nature, as the current near $0.4V$ is in the range of nA, whereas it's value near $0.8V$ is in the range of μA. The design of Chao Lu exhibits a quadratic nature with voltage, it's current values is in the range of μA. It is worth stating that the current produced by the proposed circuit is very low compared to the design proposed in [39]. Another simulation in Figure 3.11 shows the current behavior on a log scale with input voltage.

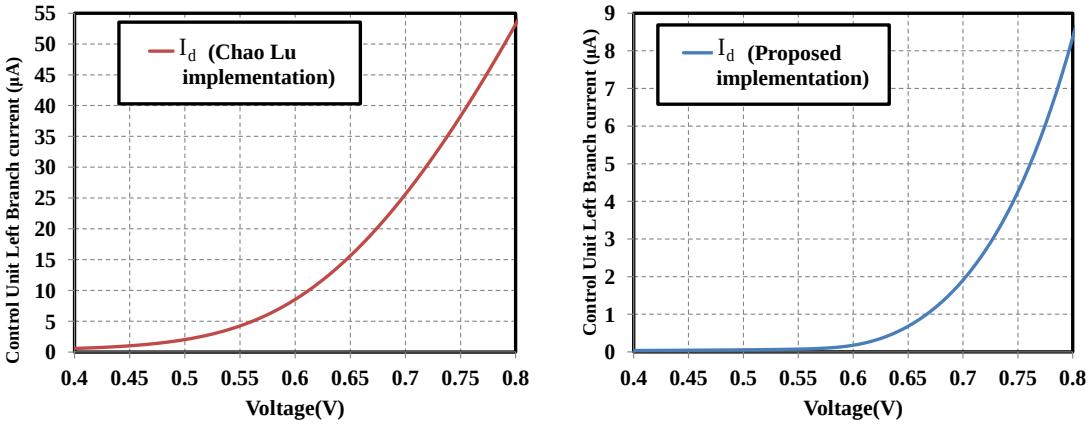


FIGURE 3.10: DC Simulation for the Left Branch Current I_d for Both Designs

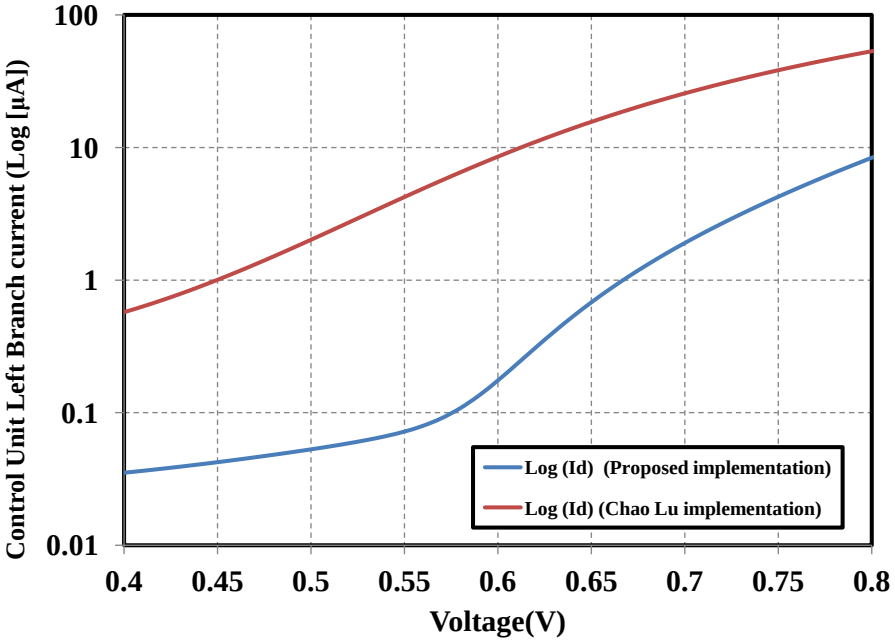


FIGURE 3.11: DC Simulation for the Left Branch Current $log(I_d)$ for Both Designs

3.3.3 Comparator Design

The Op-Amp used in the design is a typical two stage common source amplifier [43] shown in Figure 3.13. Compensation is used for stability issues. The design of the amplifier is targeting large open loop gain, therefore two stages are used. Since the power consumption is critical, the transistors channel length values are relatively large with small widths. This design procedure comes at the expense of the unity gain bandwidth, which in return will affect on the transient behavior of the entire system.

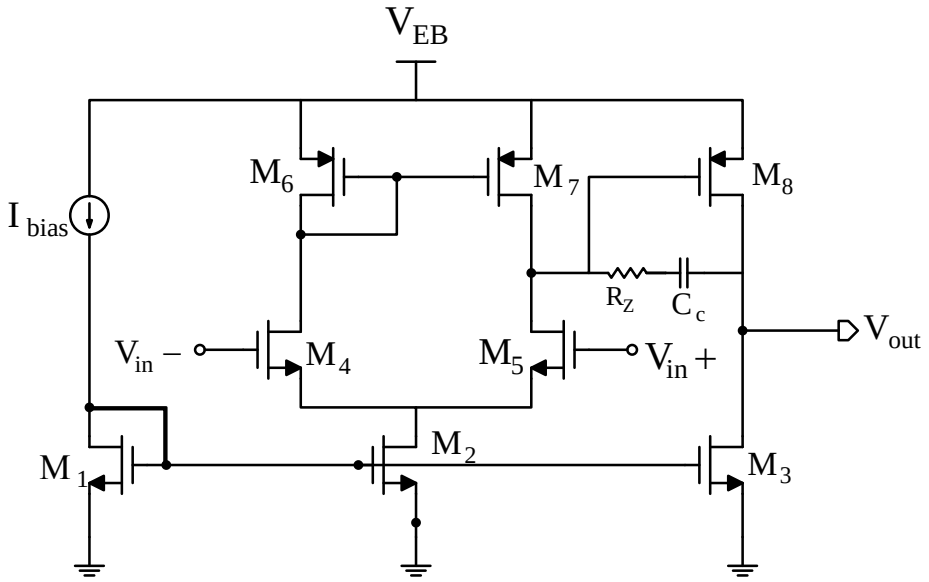


FIGURE 3.12: Two Stage Operational Transconductance Amplifier (OTA) Design with Compensation

Figure 3.13 shows the gain response and phase response of the (OTA) architecture used. The voltage gain is equal to $60.4dB$, unity gain bandwidth is equal $57MHz$, phase margin is equal to 59.3° and the power consumption is equal to $40\mu W$.

Another simulation is done for the analog part of the control unit, in order to test the loop stability. The feedback loop is broken, and the loop gain and phase

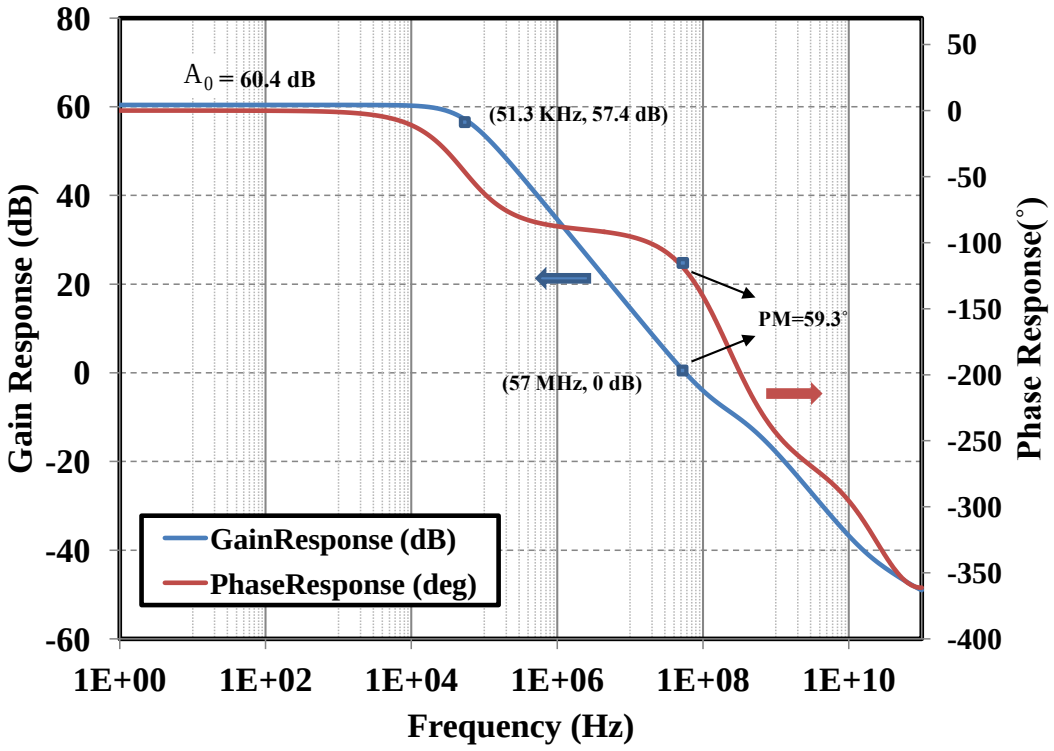


FIGURE 3.13: Gain Response and Phase Response of the (OTA) used in the Design

response are monitored in Figure 3.14. It can be illustrated that the loop is stable, since the loop phase margin is equal to 79.3°.

3.3.4 Flip-flop Design

The flip-flop adopted in the design is the true single phase clock based flip flop (TSPC). The design is based on [44]. This topology has many advantages, it works at high speeds, and it occupies small area and it consumes low power. The sizing of the pull up network is almost double the size of the pull down network [45]. The design of the TSPC flip flop is shown in Figure 3.15.

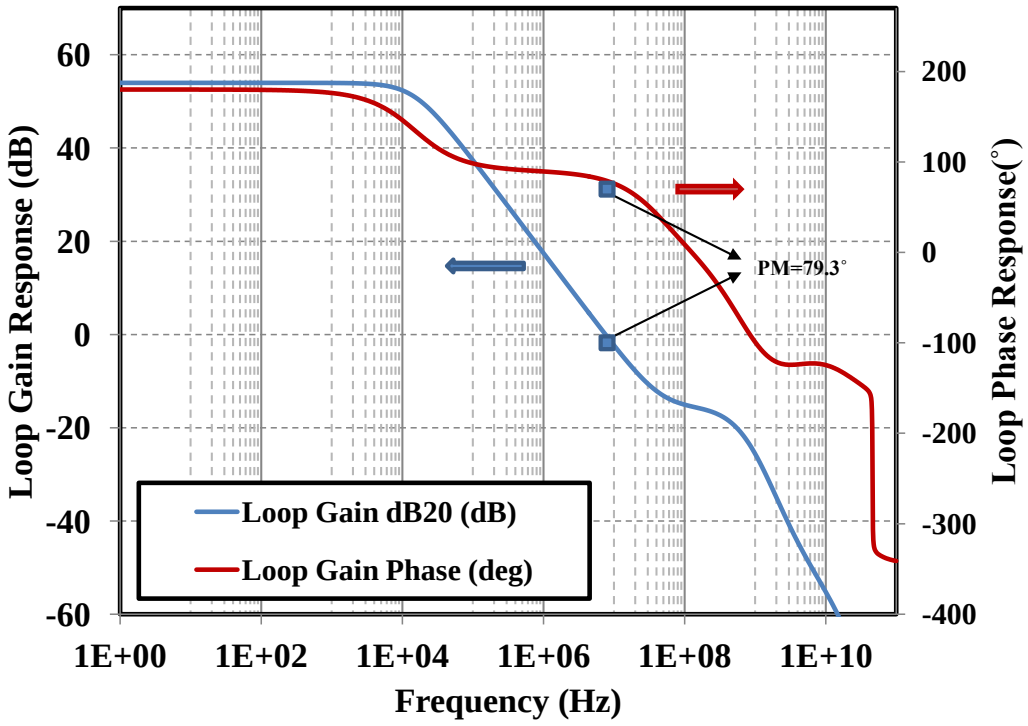


FIGURE 3.14: Gain Response and Phase Response of the feedback loop of the analog part

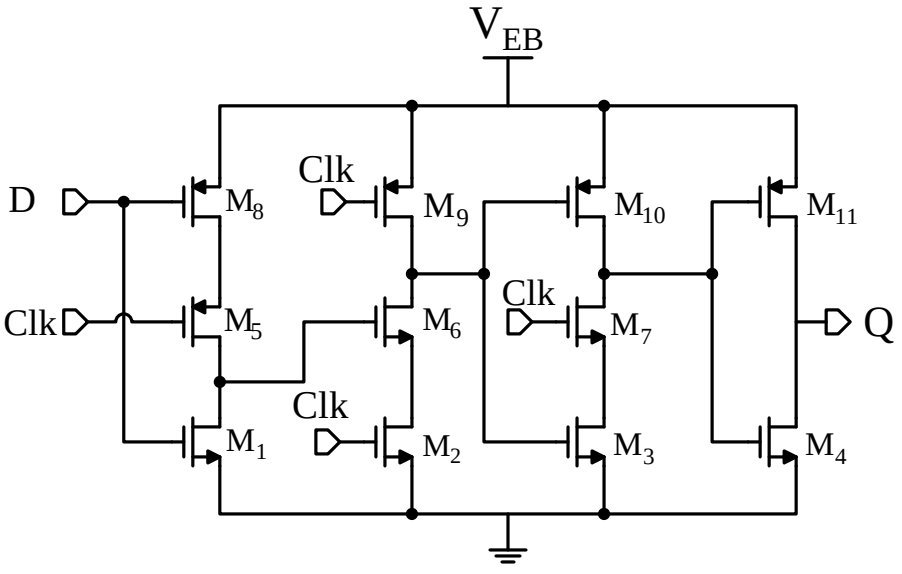


FIGURE 3.15: True Single Phase Clock based D-flip flop used in the Design

3.4 System Level Considerations

The tracking circuit has a direct impact on the power efficiency, so the power budget is very crucial for a power efficient design . This part is dealing with optimization techniques on the system and block level to find a practical solution for the power efficiency enhancement

One of the solutions that aims to decrease the control unit power is decreasing the supply voltage and re-adjust the sizing of the transistors to get the same correspondence of the frequency-voltage relationship. So if one decreases the output voltage level of the charge pump, it affects the power capability of the charge pump itself.

Decreasing control unit supply voltage has a great impact on the charge pump capacitance values, as their values have to be updated to get the right voltage values at the PV terminal. So basically, when the frequency range is decreased, the capacitance increases to get the same voltage level values. This solution consumes area on the silicon, however, it should provide higher power efficiency.

The first optimization is performed on the supply voltage of the control circuit. A capacitive divider shown in Figure 3.16 is used in lowering the supply voltage rather than taking the whole voltage. The output super-capacitor is used to mimic the voltage at $1.8V$. So, by lowering the supply voltage of the control circuit(i.e., $1.2V$), it should have a great impact on power consumption and the frequency range. A low resistive path is created between the control unit and the power converter output node, in order to dump the needed current by the control unit.

The second enhancement is done on the circuit level at the input of the control unit. Since it is not guaranteed to have the exact required PV voltage that corresponds to a certain frequency from the charge pump side (i.e., Frequency Offset), a source follower stage is added before the control unit to fix the frequency shift problem. Since $(V_{ph} - V_{CU_{in}})$ is controllable, then the frequency that corresponds

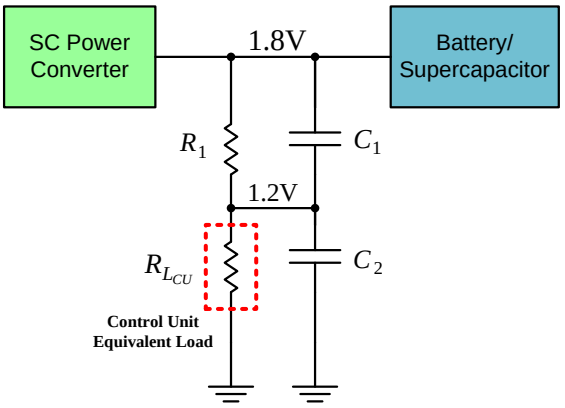


FIGURE 3.16: Capacitive divider Network needed for Control Unit Supply

to a certain (V_{ph}) can be changed. The source follower stage consumes around (1.2%) of the total control unit power. By controlling the transistors size and the resistance value, a controllable voltage shift is obtained. Figure 3.17 shows a typical source follower design.

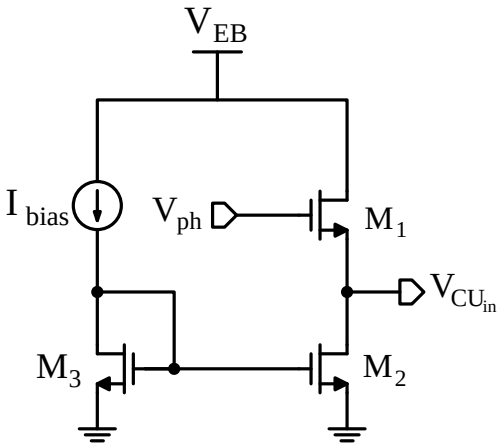


FIGURE 3.17: Typical Source Follower Stage

3.5 Simulation Results

3.5.1 Typical Simulation Results

This section views the simulation results for the design replication of [39] versus the simulation results for the new technique. The PV model used is an open source verilog-A model [18]. Transistors are used from industrial hardware calibrated TSMC 65nm technology node, and capacitors used in the design are MIM (Metal-Insulator-Metal) capacitors of the same technology.

The first simulation is showing the frequency range of each design. Figure 3.18 shows the entire frequency range at supply voltage ($1.2V$) and the source follower stage to the new proposed circuit. The control unit is tested alone first in order to verify functionality. Decreasing power consumption comes at the expense of increasing the charge pump area. As when the frequency decreases, the input impedance perturbation rate decreases. Accordingly the PV voltage approaches (V_{OC}) and the entire system loses locking. In order to make compensation, the charge pump capacitance has to be increased to decrease the overall input impedance, thus the PV voltage is then decreased. In order to save the area of the charge pump, the capacitor (C_S) in the digital side can be controlled to change the control unit gain, thus shifting the frequency range. Figure 3.18 shows the desired relationship required to maintain the charge pump at its maximum power capability versus the transfer characteristics for the charge pump. Figure 3.19 shows the same simulation for Chao Lu implementation [39].

The next set of simulation results presents the full system in a closed loop form, so that the proposed technique can verify its functionality on the top system level. The performance metrics of a typical energy harvester are the photo-voltaic available power, net energy buffer power, control unit frequency range, control unit power range and the harvester power efficiency.

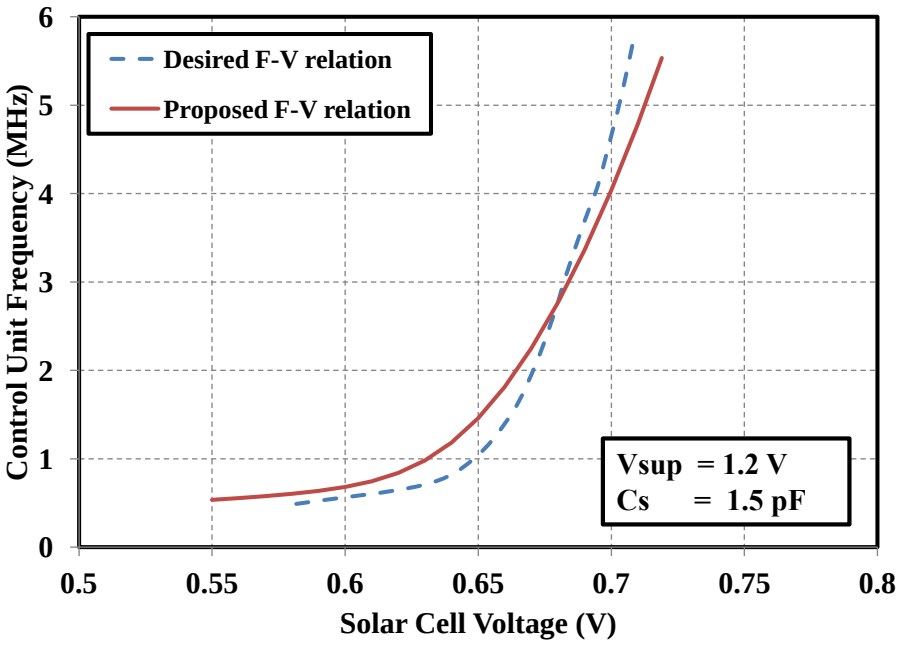


FIGURE 3.18: Frequency-voltage relationship of the proposed design versus the desired relation derived from the charge pump

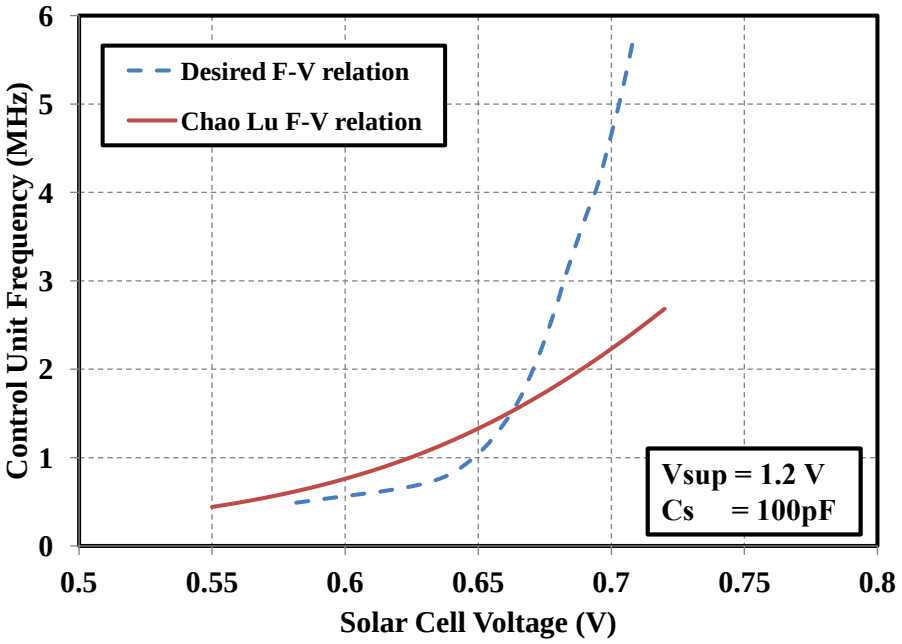


FIGURE 3.19: Frequency-voltage relationship of the proposed design versus Chao Lu relation derived from the charge pump

The most important metric in the design of the energy harvesters is the power consumption of the control unit, as this metric greatly affects the efficiency. Decreasing the frequency range of operation and the supply voltage leads to significant reduction of the dynamic power, in return the whole power consumption decreased. The power consumed in the control circuit is divided into two portions; static power comes from the left side (i.e. analog part), which is responsible for voltage to current conversion, dynamic power comes from the right side (i.e. digital part), which is responsible for current to frequency conversion. Figure 3.20 shows the consumed power range of the two designs. It is clear that the proposed design operates at much lower power ranges.

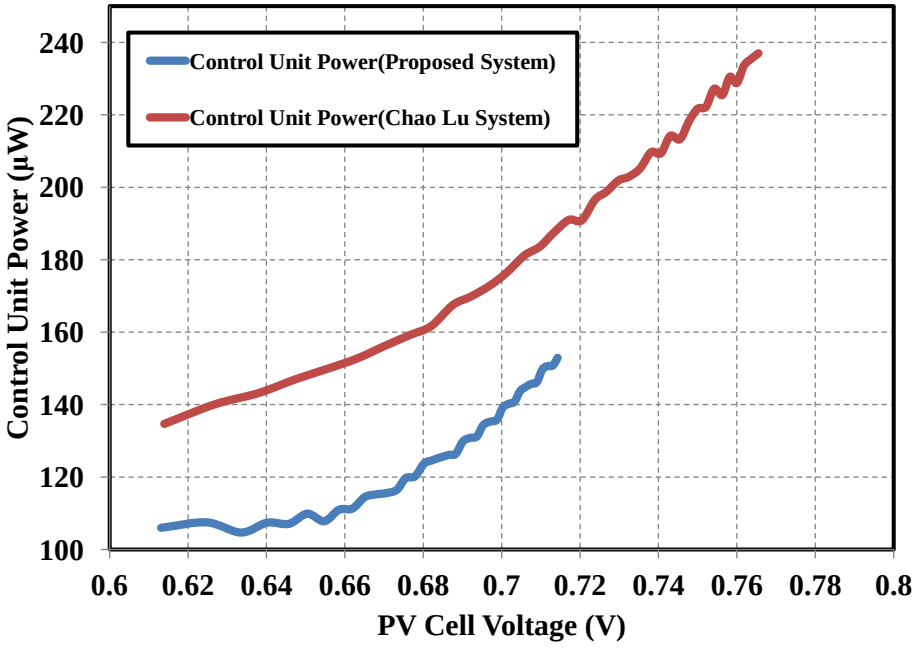


FIGURE 3.20: Control Unit Power consumed for both designs

The performance metric shown in Figure 3.21 is the photo-voltaic operating power across different light intensities. It can be shown that the proposed design tracks more efficient than Chao Lu design [39]. Efficient tracking provide more power extracted from the solar cell, which has a great impact on power efficiency.

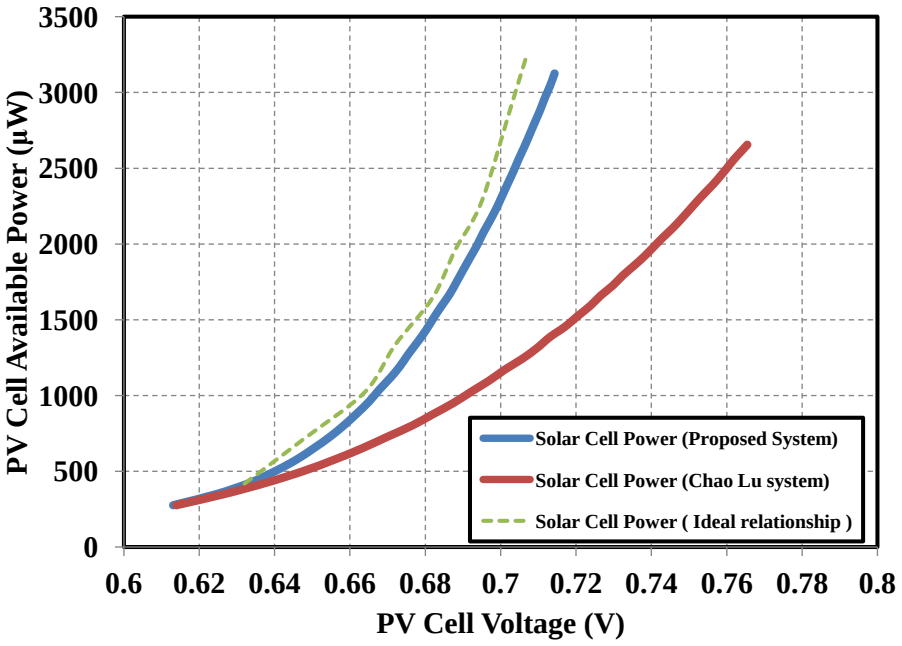


FIGURE 3.21: Photo-Voltaic Available Power for both Designs

The next simulation shows the entire frequency range of both designs. It can be illustrated that the proposed design efficiently verifies the exponential relationship between the charge pump frequency and the photo-voltaic cell terminal voltage, so it can be concluded that the control unit forces the charge pump to work at its maximum power capability.

Figure 3.23 shows the the net harvested power into the energy buffer of both designs, the design shows its reliability in terms of increased output power across large range of input light intensities.

Figure 3.24 shows the end-to-end power efficiency of both designs, the design proves its strong competence in terms of increased efficiency across large range of input light intensities.

The efficiency term has different approaches to be calculated. In this study, three different definitions for the efficiency are introduced. The power efficiency (η_{Power}) which is the ratio between the net output power (P_{out}) to the average input power (P_{in}). The second definition is the tracking efficiency (η_{MPP}) which is the

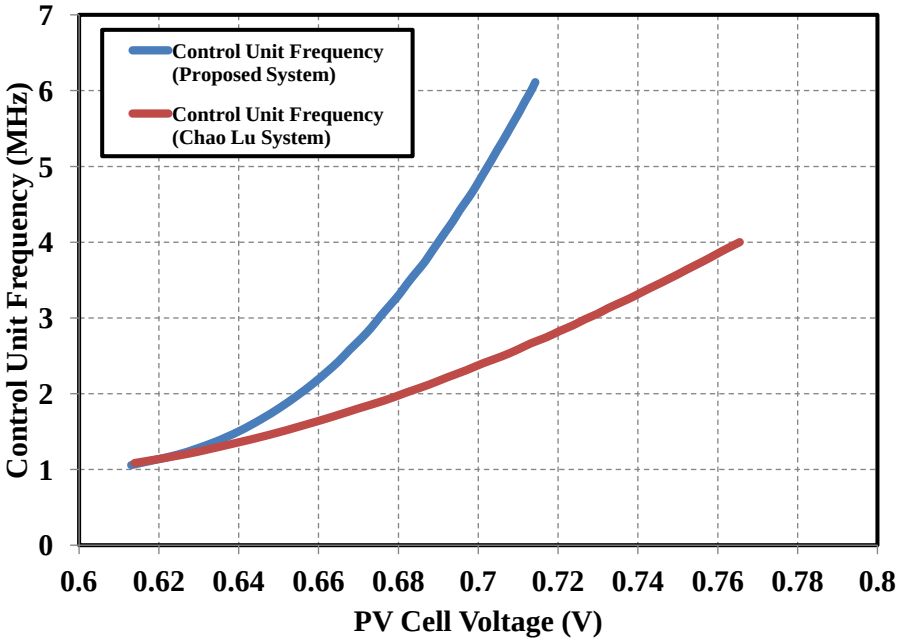


FIGURE 3.22: Control Unit Frequency range for both designs

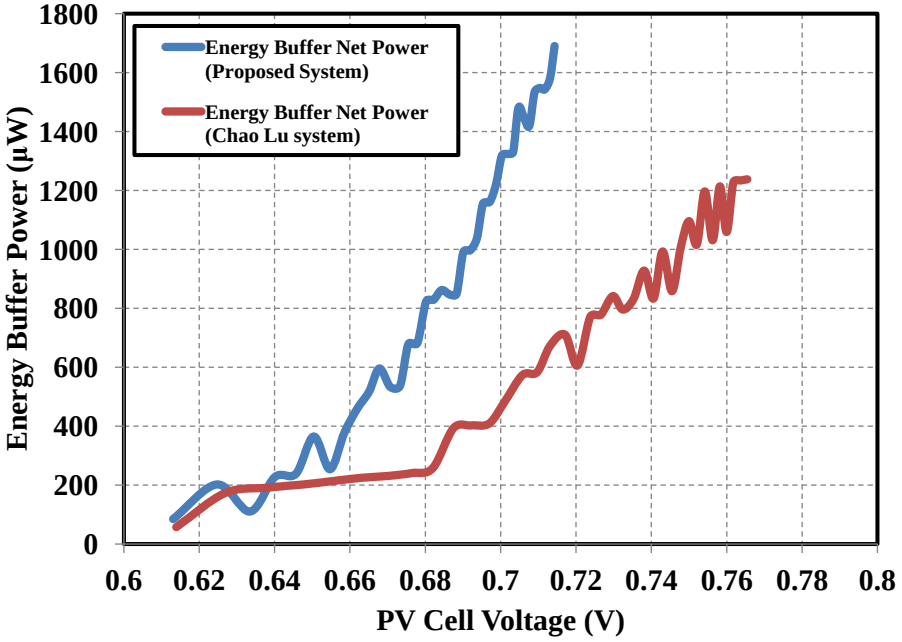


FIGURE 3.23: Net Output Harvested Power for both designs

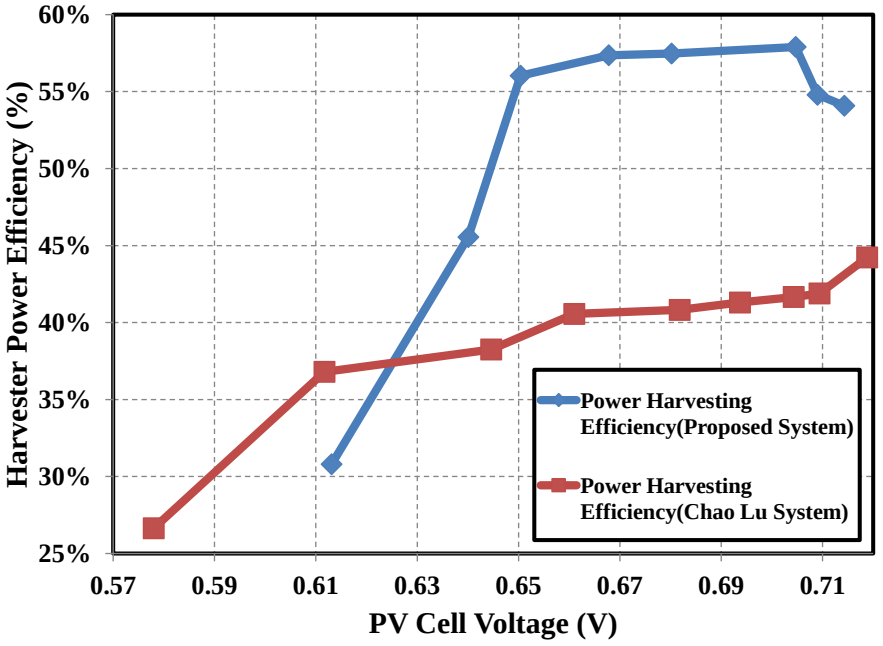


FIGURE 3.24: Power Efficiency of both designs

ratio between the operating photo-voltaic voltage value (V_{ph}) to the maximum power voltage value (V_{MPP}). The last definition is the characteristic efficiency (η_C) which is the ratio between the net output power (P_{out}) to the loss-free output power ($P_{out_{Max}}$). Actually, the last definition needs a focus in order to illustrate its importance.

According to [46], The optimum conversion ratio for a power-area efficient power conversion is derived as:

$$M_{opt} = 2\left(\frac{V_{out}}{V_{in}} - 1\right) \tag{3.17}$$

The optimum ratio is based on the output voltage but not the efficiency, That's why the new definition of the harvester efficiency is a characteristic to the power converter topology used. it could give a sense of how good the design is according to the used power converter. According to the optimum conversion ratio :

$$V_{out} = \left(\frac{M}{2} + 1\right) V_{in} \tag{3.18}$$

According to the power converter model, The output current is modeled as :

$$I_{out} = \frac{I_{in} - I_{cp,loss}}{M} \tag{3.19}$$

Power converter losses are ignored for simplicity, so the maximum possible efficiency is :

$$\eta_{Max} = \frac{\left(\frac{M}{2} + 1\right)}{M}; M \geq 2 \tag{3.20}$$

Since $M = 4$ so the maximum possible efficiency is ($\eta_{Max} = 75\%$).

Table 3.1 shows the tracking efficiency of the proposed design at different light samples. It can be shown that the proposed system can track the photo-voltaic cell efficiently with small shift from the required operating point.

TABLE 3.1: The Tracking Efficiency of the Proposed System at Different Light Samples

Light Intensity (LUX)	Operating PV Voltage(V_{PV})	MPP voltage (V_{MPP})	Tracking efficiency
389.87 LUX	$634mV$	$632mV$	99.68%
952.5 LUX	$668mV$	$664mV$	99.4%
1532 LUX	$687mV$	$679.4mV$	98.9%
2346 LUX	$705mV$	$688mV$	97.6%
2721 LUX	$712mV$	$695.5mV$	97.7%

Table 3.2 shows the characteristic efficiency of the proposed design at different light samples. It can be illustrated that the proposed system has the ability to harvest most of the power. The same definition still applies when getting the ratio between the operating power efficiency (η_{Power}) and the maximum possible efficiency (η_{Max}).

TABLE 3.2: The Characteristic Efficiency of the Proposed System at Different Light Samples

Light Intensity (LUX)	operating power efficiency (η_{Power})	maximum possible efficiency (η_{Max})	characteristic efficiency (η_C)
389.87 LUX	26%	75%	34.66%
952.5 LUX	57.4%	75%	76.53%
1532 LUX	50.7%	75%	67.6%
2346 LUX	58%	75%	77.3%
2721 LUX	52.1%	75%	69.46%

Since the dynamic behavior is important to test the tracking speed of the harvester, two simulations are carried out to test the transient behavior of the harvester system. The first simulation is done for a full range light intensity. Figure 3.25 shows photo-voltaic voltage response. Figure 3.26 monitors one of the phases of the clock frequency response. The second simulation is done for a random input light intensity. Figure 3.27 presents photo-voltaic voltage response. Figure 3.28 shows one of the phases of the clock frequency response. It can be illustrated that the harvester is working fine and it can tracks the maximum power efficiently. The maximum frequency for input light intensity variation can reach $500KHz$.

Table 3.3 summarizes the dynamic performance metrics.

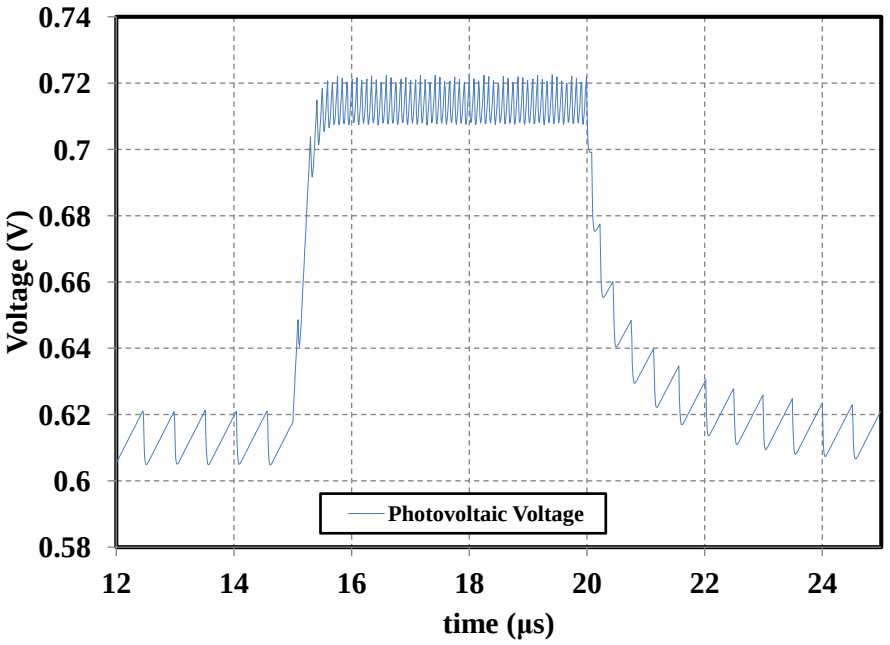


FIGURE 3.25: Photo-voltaic Voltage Response for Full Range Input Light Intensity

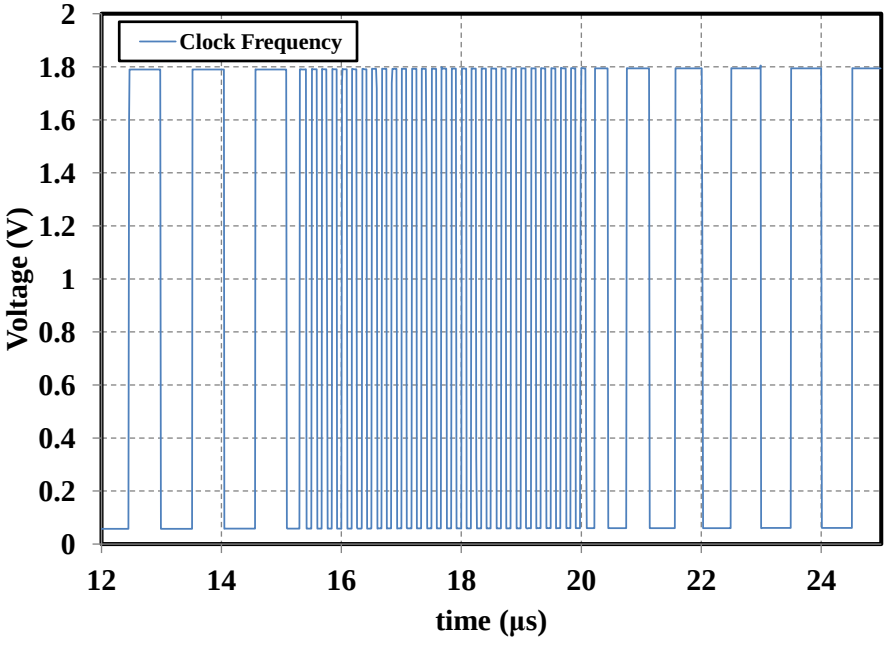


FIGURE 3.26: Clock Frequency Response for Full Range Input Light Intensity

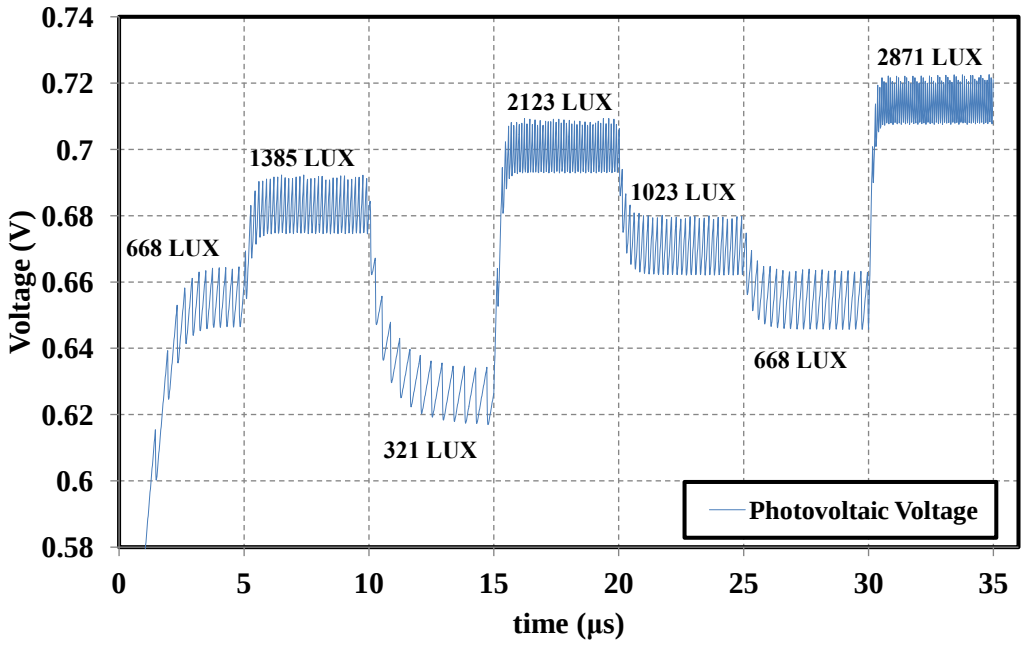


FIGURE 3.27: Photo-voltaic Voltage Response for Random Input Light Intensity

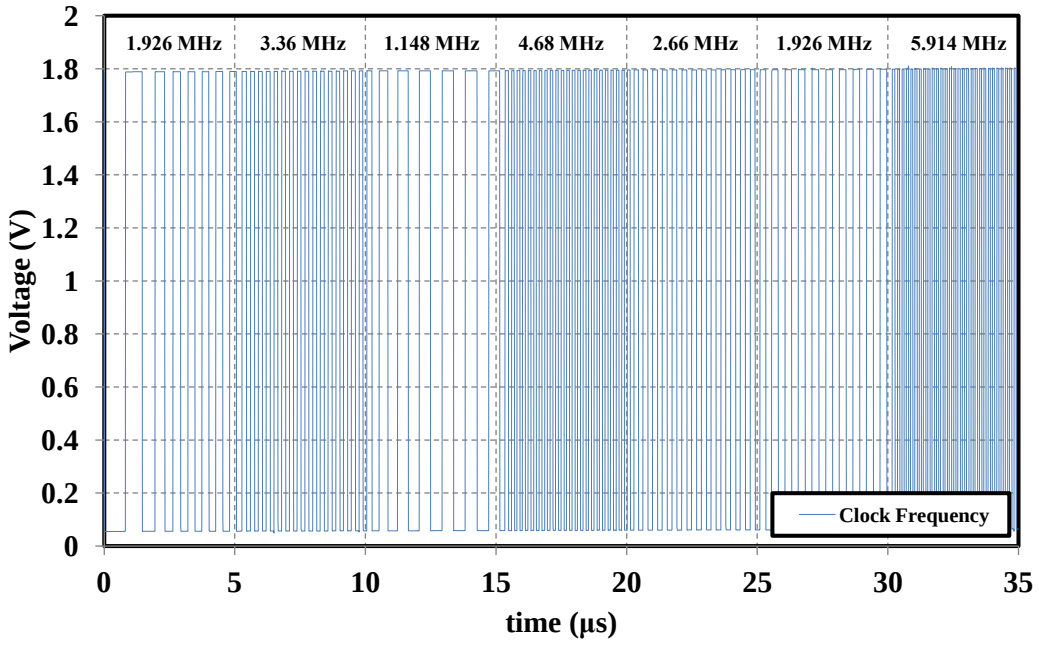


FIGURE 3.28: Clock Frequency Response for Random Input Light Intensity

TABLE 3.3: Dynamic performance metrics of the energy harvesting system over a full light range excitation

Dynamic Performance Metrics	Simulation Results
Rise/Fall time	$360ns/1.43\mu s$
Maximum Voltage Ripples	$15mV(2.4\%)$
Input Dynamic Range	$100mV$

Since, the proposed technique is based on [39]. It is important to make a comparison between both designs to show the importance of the proposed system. Table 3.4 shows the performance metrics of the two designs. it can be illustrated that the proposed approach achieves promising results.

TABLE 3.4: Performance Metrics of the Proposed Design versus Chao Lu Design [39]

Design Metric	[39](VLSID 2012)	Proposed Design
Control Unit Frequency	$6.25MHZ \rightarrow 11.11MHZ$	$1.06MHZ \rightarrow 6.11MHZ$
PV voltage range	$305mV \rightarrow 360mV$	$613mV \rightarrow 714mV$
Maximum PV power	$140\mu W \rightarrow 444\mu W$	$276\mu W \rightarrow 3.13mW$
Energy Buffer Power	$46\mu W \rightarrow 170\mu W$	$85\mu W \rightarrow 1.69mW$
Maximum Power Efficiency (η_{Power})	39.5%	58%
Output Capacitor	$1\mu F$	$1\mu F$
Energy Buffer Voltage	$0.9V$	$1.8V$
PV Open Circuit Voltage	$\leq 0.45V$	$\leq 0.75V$

A broader comparison should be also taken into consideration, since there are a lot of tracking algorithms with different tracking techniques. The proposed design is compared to another three available designs with different tracking approaches.

Table 3.5 shows a comparison between 4 different designs that uses the same transduction mechanism targeting miniature devices.

TABLE 3.5: Performance Metrics of Different Design Approaches

Design Metric	Design #1 (TVLSI 2009) [37]	Design #2 (ISCAS 2011) [47]	Design #3 (VLSID 2012) [39]	Proposed Design
Transcducer	Solar	Solar	Solar	Solar
MPPT Technique	Hill climbing(Current Sensing)	Hill climbing	Negative Feedback Tracking	Exponential Tracking
Power Converter	SC Charge Pump	SC Voltage Tripler	SC Charge Pump	SC Charge Pump
Sensing control parameter	Current	Voltage	No Sensing (Polynomial VCO)	No Sensing (Exponential VCO)
Maximum End-to-End Efficiency	67%	73.9%	39.5%	58%
Controller Power Overhead	$\geq 10\mu W$	$446\mu W$	$180\mu W$	$150\mu W$
Maximum Power Throughput	$780\mu W$	$1266\mu W$	$170\mu W$	$1700\mu W$
Technology	$0.35\mu m$	$0.13\mu m$	$45nm$	$65nm$
Battery/Super-capacitor feature	Battery	Super-capacitor	Super-capacitor	Super-capacitor

3.5.2 Process Corner Simulation Results

Since some transistors in the control circuit are operating at the sub-threshold mode, it is important to capture the process corners in order to test the functionality. The current equation of the sub-threshold mode includes the threshold voltage at the exponent power as shown in Equation 3.12, so the value of the current is

exponentially dependent on the threshold voltage value. Figures (3.29,3.30) shows the control unit frequency range and photo-voltaic available power range across process corners. Performance degradation appeared in non-typical corners.

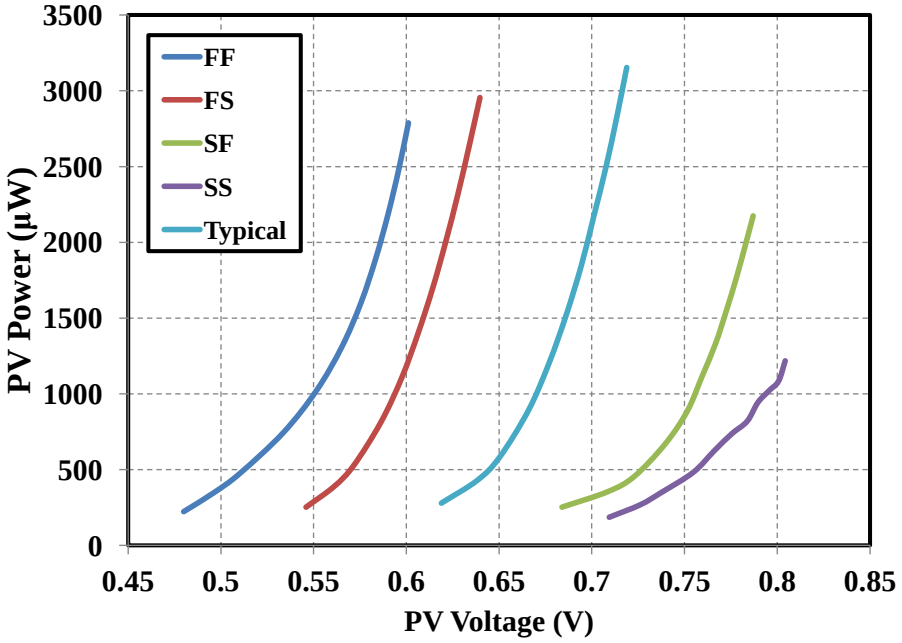


FIGURE 3.29: Photo-voltaic cell available power across corners

In order to overcome the problem of process variations, some sort of control has to be added to introduce a compensating effect of the operating corner after fabrication. For example, if the operating corner is the slow-slow corner shown in Figure 3.30, the Power-Voltage curve is shifted to the right side. So it is far away from the required locus, then the new control mechanism has to pull the curve to the left to coincide with the intended locus curve. On the other hand, if the operating corner is fast-fast corner shown in Figure 3.30, the Power-Voltage curve is shifted upwards. So it is far away from the required locus, then the new control technique has to push the curve downwards to match the desired locus curve. A new Adaptive technique is proposed in [40], where the proposed circuit is based on perturbing the bulk voltage of both NMOS and PMOS transistors. When V_{th_n} (i.e., NMOS threshold voltage) increases, V_{BN} (i.e., NMOS Bulk voltage) should increase to add an opposite effect to V_{th_n} and vice versa. The same scenario occurs

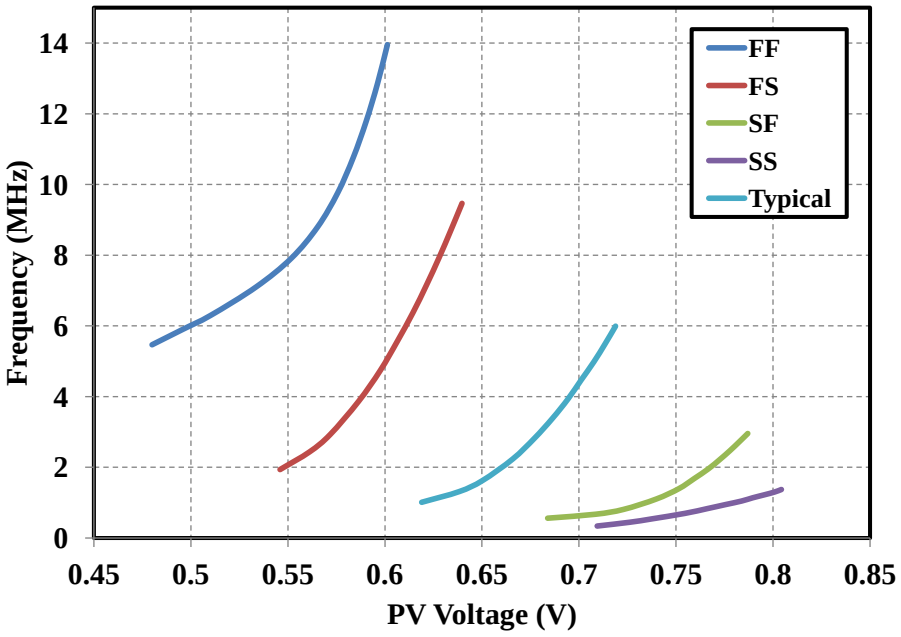


FIGURE 3.30: Control unit frequency range across corners

for the PMOS threshold voltage. Equations 3.21 through 3.25 [40] show the bulk voltage relationship with threshold voltage variations for both NMOS and PMOS transisors.

$$V_{th} = V_{th_o} + \Delta V_{th_{BB}} \tag{3.21}$$

$$\Delta V_{th_{BB}} = \gamma\left(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}\right) \tag{3.22}$$

$$V_{BS} = \frac{2\sqrt{2\phi_F}}{\gamma}(\Delta V_{th_{PV}}) - \frac{1}{\gamma^2}(\Delta V_{th_{PV}})^2 \tag{3.23}$$

$$V_{Bn} = \frac{2\sqrt{2\phi_{F_n}}}{\gamma_n}\left[V_{thn_e} - V_{thn_o}\right] - \frac{1}{\gamma^2}\left[V_{thn_e} - V_{thn_o}\right]^2 \tag{3.24}$$

$$V_{Bp} = V_{dd} - \frac{2\sqrt{2\phi_{F_p}}}{\gamma_p}\left[V_{thp_e} - V_{thp_o}\right] + \frac{1}{\gamma^2}\left[V_{thp_e} - V_{thp_o}\right]^2 \tag{3.25}$$

Where V_{th_o} is the threshold voltage under no body bias. V_{th} is the threshold voltage under body bias. $\Delta V_{th_{BB}}$ is the voltage increment due to body bias. (γ,γ_n,γ_p,ϕ_F,ϕ_{F_n},ϕ_{F_n}) are technology constants. V_{BS} is the Bulk-Source voltage

difference.$\Delta V_{th_{PV}}$ is the threshold voltage variation change. V_{Bn} is the NMOS body voltage. V_{Bp} is the PMOS body voltage. V_{thn_e}, V_{thp_e} are the NMOS, PMOS threshold voltages under process variations. V_{thn_o}, V_{thn_o} are the NMOS, PMOS threshold voltages under typical conditions.

In [40], circuit designs are proposed to implement Equations (3.24,3.25). One of the most power hungry blocks in the design is the squaring circuit found in [40]. Since power consumption is the most critical metric in the proposed design, the design used in [48] is more convenient. In [48], Equations(3.24,3.25) are linearized through curve fitting. The new linearized equations are simplified as follows:

$$V_{Bn} = A_n \left[V_{thn_e} - V_{thn_o}\right] \tag{3.26}$$

$$V_{Bp} = V_{dd} - A_p \left[V_{thp_e} - V_{thp_o}\right] \tag{3.27}$$

The new equations can be realized easily through the implementation of the summing Op-Amp based circuit shown in Figures (3.31,3.32).

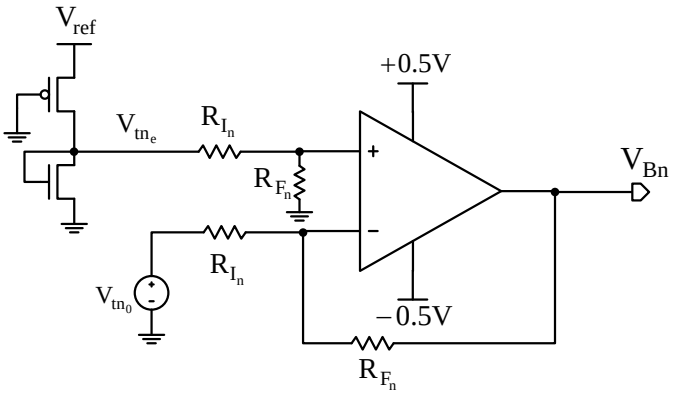


FIGURE 3.31: The adaptive body bias circuit design for NMOS transistors

The resistance values are chosen according to the transistor parameters shown in Table.

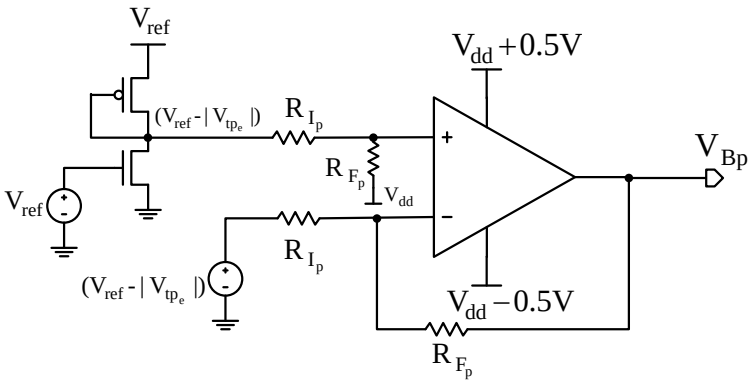


FIGURE 3.32: The adaptive body bias circuit design for PMOS transistors

TABLE 3.6: 65-nm Technology Information

Technology Parameters	NMOS	PMOS
V_{th_o}(V)	0.352	-0.204
ϕ_F(V)	0.467	0.439
γ (dimentionless)	0.296	0.174

Transfer function of both designs are initially tested to verify the concept of the adaptive body bias. DC sweep is done with an ideal input voltage source instead of the threshold sensing circuit. Figure 3.33 shows the transfer characteristics of the adaptive body bias circuit for NMOS transistors. Figure 3.34 monitors the transfer characteristics of the adaptive body bias circuit for PMOS transistors. Resistance values used are shown on each plot.

The whole circuit is tested across corners to test its response across threshold voltage variation. The sensing circuit is connected to the amplifier stage, the sensed voltage and the bulk voltage are monitored. Figure 3.35 shows the process corners simulation for the adaptive body bias circuit for NMOS transistors. Figure 3.36 shows the process corners simulation for the adaptive body bias circuit for PMOS transistors.

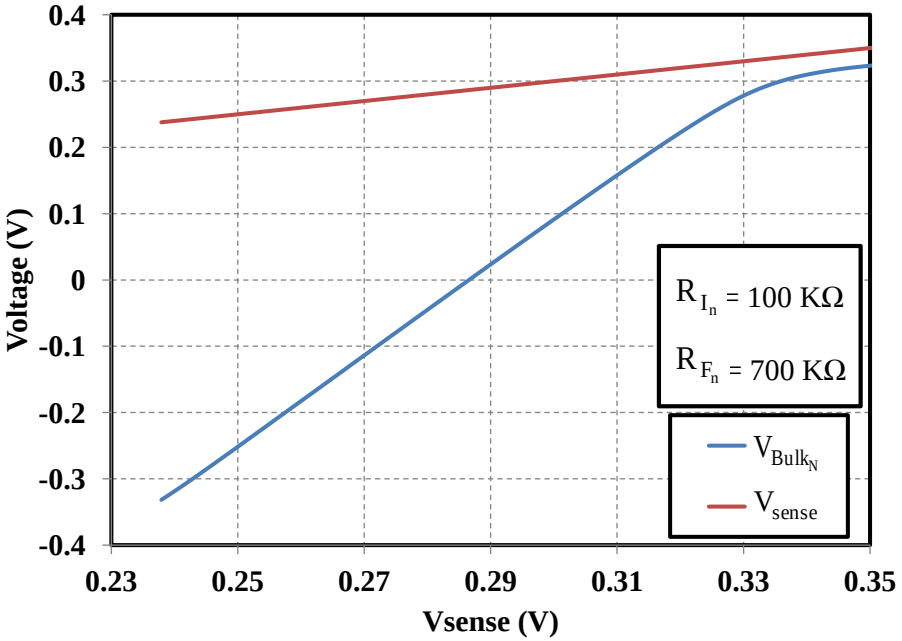


FIGURE 3.33: Transfer characteristics of the adaptive body bias circuit for NMOS transistors

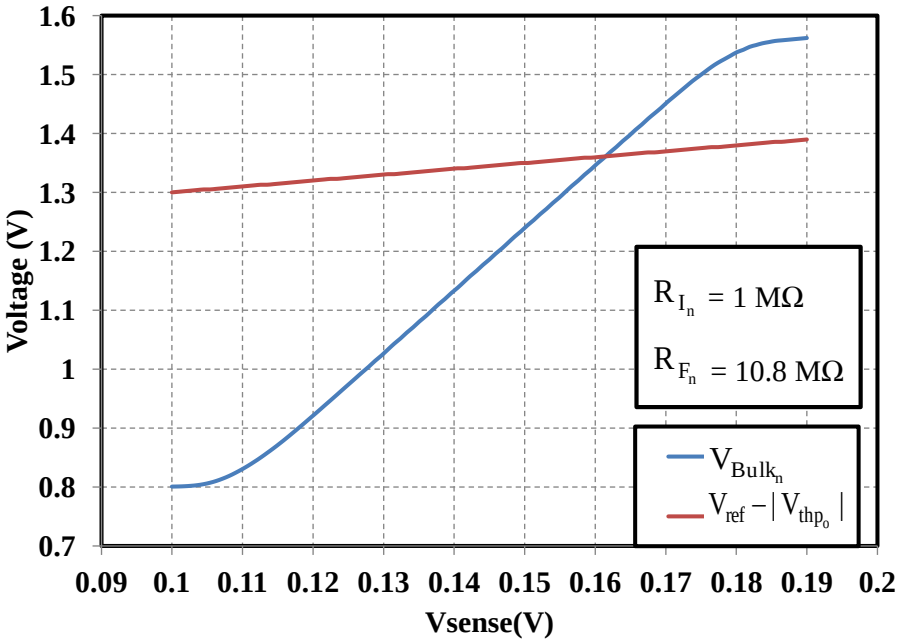


FIGURE 3.34: Transfer characteristics of the adaptive body bias circuit for PMOS transistors

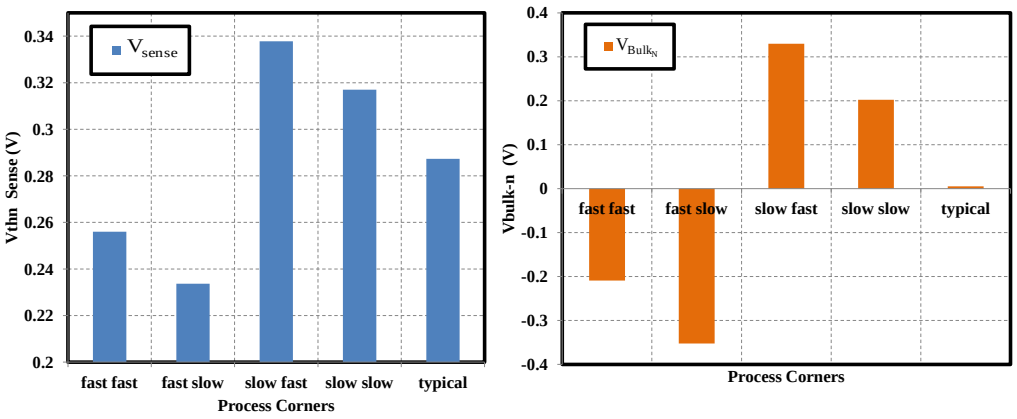


FIGURE 3.35: Process corners simulation for the adaptive body bias circuit for NMOS transistors

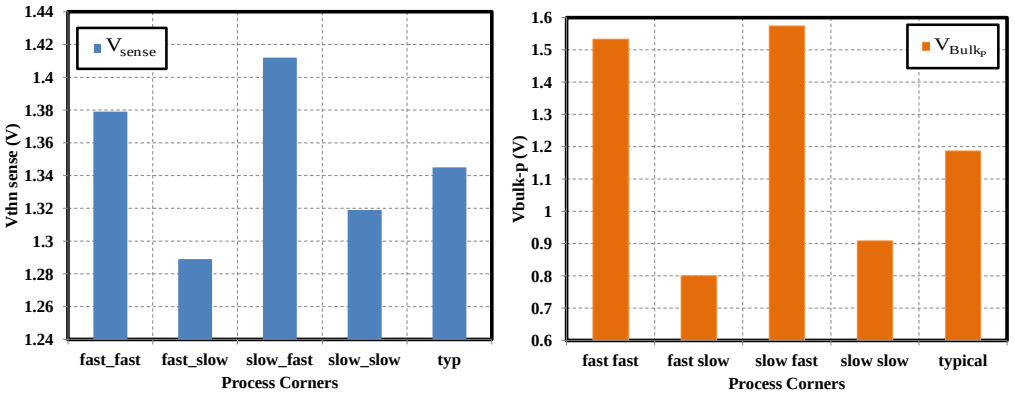


FIGURE 3.36: Process corners simulation for the adaptive body bias circuit for PMOS transistors

The adaptive body bias circuits are integrated with the harvester full system, and process corner simulations are reported. Figure 3.37 shows the photo-voltaic available power across corners after adding the adaptive body bias circuits. Figure 3.38 shows the control unit frequency range across corners after adding the adaptive body bias circuits, it can be shown that the adaptive techniques made a significant improvement for the circuit performance.

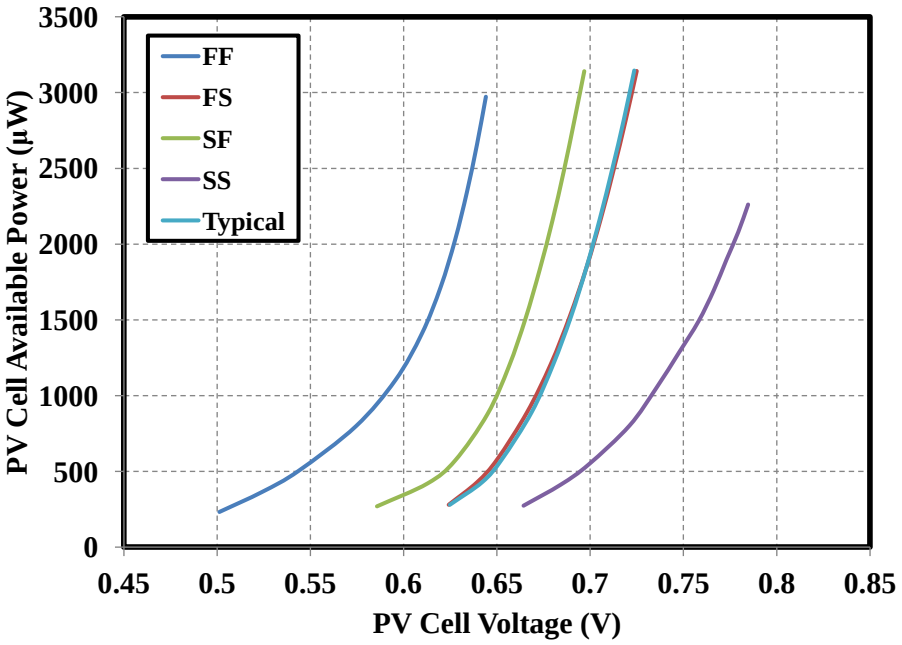


FIGURE 3.37: Process corners simulation for the adaptive body bias circuit for NMOS transistors

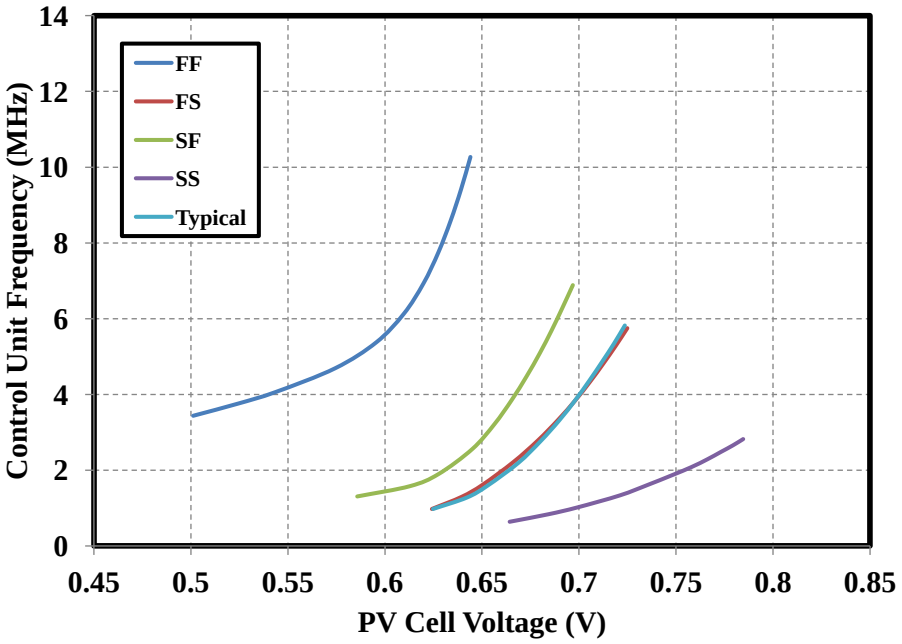


FIGURE 3.38: Control unit frequency range across corners after adding the adaptive circuits

3.6 Conclusion

This chapter presents a new technique for maximum power locking of a solar based energy harvester. The system blocks are discussed. The technique is analyzed through system equations. Simulation results show how efficient the new technique tracks the maximum possible power across different input light intensities. The design shows its reliability in terms of hardware cost by removing current sensing and decision generation circuits. Circuit limitations are discussed. Process corners are highlighted, some circuit design changes are proposed to overcome the process variations. The power consumption of the adaptive circuits is verified to be low enough, so the power efficiency can not be affected greatly.

This chapter provides a guideline to the power management engineers for designing the control unit using the negative feedback concept. Once the characteristics of the solar cell is completely studied, then the designer has to make some circuit tweaking to match the maximum power capability of the available solar cell. Different design parameters are discussed here to reach the final compact relation between the solar cell terminal voltage and the charge pump switching frequency. The generalized form of this relation can be rewritten as:

$$f_{clk} \simeq K_1 \left(e^{\frac{K_2}{\alpha} V_{MPP}} - e^{K_2 V_{MPP}} \right) + f(K_3); \alpha < 1 \tag{3.28}$$

The designer has three coefficients to tweak and get a matched performance to the attached solar cell. Table 4.2 shows the circuit parameters dependencies for the three coefficients, in order to provide a design framework for this technique.

TABLE 3.7: Control Unit coefficients dependenices

Coefficicents	Circuit parameters correspondence
K_1	$\frac{1}{V_m C_s}$ (i.e. ring oscillator parameters)
K_2	V_{eff} of the transistors responsible for current subtraction
K_3	V_{gs} of the transistor responsible for level shifting in the source follower circuit

Chapter 4

Multi-level Clock based Switched Capacitor Charge Pump

4.1 Introduction

One of the most important blocks in the power management modules is the power converter. There are many types of power converters such as charge pumps. The proposed designs are suitable for solar energy harvesting targeting WSNs, since energy transducers give ultra low terminal voltages. These voltage values have to be boosted up to a voltage level that can supply the WSN. The goal of this chapter is to increase the charge pump output current and power efficiency as well.

Power converters, also known as DC-DC converters, have three different types. The low drop-out (LDO) voltage regulator is one of these types. LDO has the advantage of offering low power supply noise, since it is a switching-free topology. However, its drop out voltage has to be small to provide high efficiency, and it also do voltage step-down only. The second type of the power converters is the DC-DC buck boost converters which can do voltage step-up or step-down

conversion. They generate high power efficiency provided that the inductor used has a high quality factor, so they have to be implemented off-chip. This type of converter requires large area. It also generates electromagnetic interference (EMI) and power supply noise. The third type is the switched capacitor charge pump (SCCP). SCCP consists of MOS transistors and capacitors only and can do voltage step-up or step-down. SCCP has the advantage of low cost integration, since there are no coils used. SCCP needs two non-inverting clock phases in order to do power conversion process. There has been an extensive research on the development of the SCCP. The first invented linear charge pump is Dickson charge pump [27]. There are other optimized linear charge pumps that can be found in [29],[28]. Other degrees of optimization are done on finding the optimum number of stages based on the V_{in} and V_{out} values as investigated in [49],[50],[46]. Figure 4.1 shows a 3-stage linear charge pump topology, it can be shown that the voltage is boosted across each stage. Charge pump design has many performance metrics, the most important metrics are knee frequency (the frequency at which the output current reaches $(1/\sqrt{2})$ of the maximum current value), power capability, and switching/conduction power losses of the charge sharing switches. The operation of the charge pump is based on charge sharing between the flying capacitances, thus careful design of switches and capacitor sizes is needed for efficient power delivery. Area is also an important constraint in the charge pump design, so the sizes should not be very large. They should also verify the functionality.

4.2 Background

The SCCP design enhancements are discussed in the literature. Design metrics of a typical SCCP are very important for efficient power conversion. The first design metric is the knee frequency of the SCCP which is defined by the frequency at which the charge sharing between the flying capacitors is incomplete. After this frequency, the output current saturates with increasing the frequency. Before this

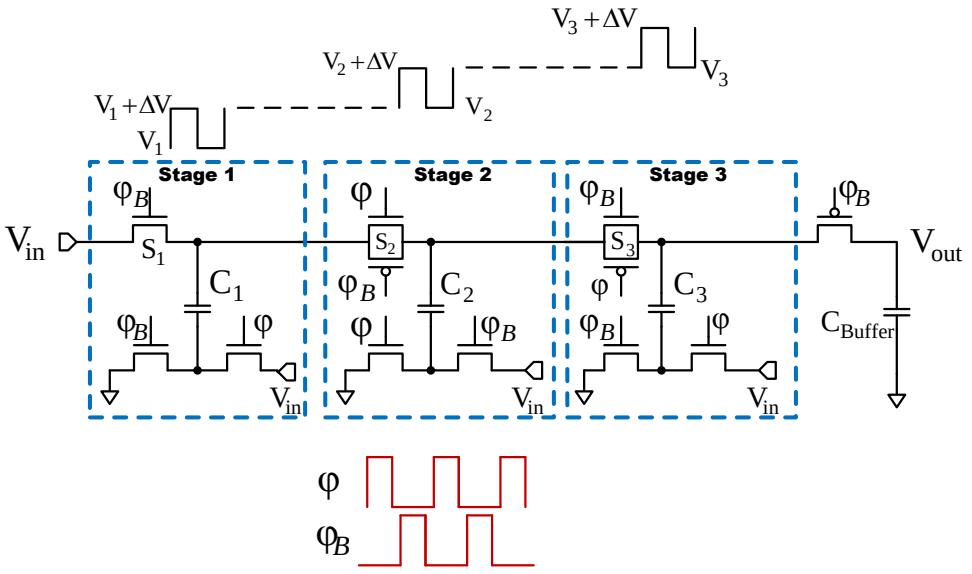


FIGURE 4.1: A 3-stage Linear Charge Pump

frequency, the output current is linear with increasing the frequency. The SCCP output current equation of a linear charge pump shown in Fig 4.1 is defined by [37],[29]:

$$I_{CPO} = f_{clk} Q_{avg} = \frac{1}{N} C f_{clk} \left[(N+1) V_{in} - V_{out} \right]; N = 3 \tag{4.1}$$

Where f_{clk} is the operating frequency. Q_{avg} is the average pumped charge to the buffer. C is the value of the flying capacitors used. V_{in} is the input voltage value. V_{out} is the target amplified voltage at the buffer side.

The knee frequency of the SCCP is determined by the worst case time constant of the charging paths. This is mainly determined by the ON resistance of the MOS transistors and the values of the flying capacitors. The ON resistance can be modeled as a voltage controlled switch [51]:

$$\begin{aligned} R_{ON} &= \frac{1}{\mu C_{ox}\frac{W}{L}[V_{gs} - V_{th} - \frac{1}{2}V_{ds}]} \\ &= \frac{1}{\mu C_{ox}\frac{W}{L}[V_g - V_{th} - \frac{1}{2}(V_d + V_s)]} \end{aligned} \tag{4.2}$$

Where R_{ON} is the ON resistance of the MOS switch. μC_{ox} is a technology constant. $\frac{W}{L}$ is the switch size. V_{gs} is the gate-source voltage difference. V_{th} is the threshold voltage. V_{ds} is the drain-source voltage difference.

In [51], a new architecture is proposed based on the ON resistance equation. Since the drain and source voltage increase across subsequent stages, the ON resistance becomes smaller. So the expected ON resistance of the last stage is expected to be high, moreover, the MOS conduction loss is modeled as [52]:

$$P_{conduction} = \frac{{I_{on}}^2}{\mu C_{ox}\frac{W}{L}[V_g - V_{th} - \frac{1}{2}(V_d + V_s)]} \tag{4.3}$$

Where I_{on} is the ON current of the MOS switch.

It can be shown that decreasing the ON resistance should also decrease the conduction power loss, thus the output power is expected to be increased.

The design in [51] is based on regulating the stages in a tree manner, such that the sum of drain and source voltages decreases with respect to the basic linear charge pump. Figure 4.2 [51] shows the distribution of the stages. In one phase, $C_1$is charged through the input voltage, whereas in the other phase, the charge is then pumped to C_3 and charge sharing occurs through S_2. The same scenario occurs between C_2 and C_3, however in this case, the charge stored in C_2 and C_3 are pumped to the output if ($V_{N_5} > V_{out}$). The main contribution of [51] is summarized in Table 4.1, it can be illustrated that ($V_s + V_d$) in the tree topology is smaller

than that in the linear topology. The current-frequency relationship is plotted in Figure 4.3 [51] showing that the tree topology has higher knee frequency.

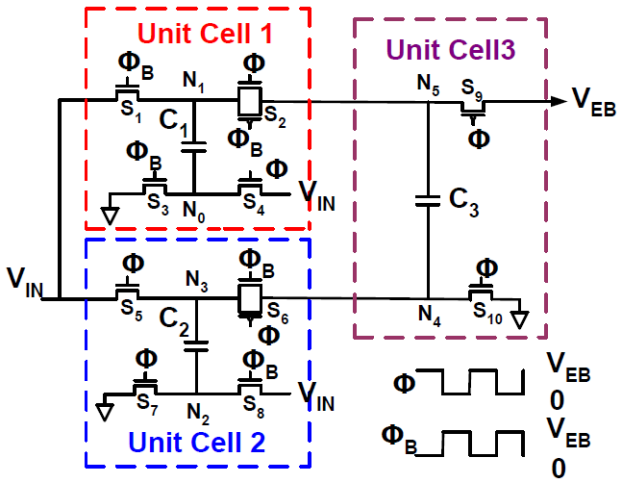


FIGURE 4.2: A 3-stage Linear Charge Pump [51]

TABLE 4.1: Linear Versus Tree Charge Pump Stage Voltages

Groups	Voltages before the charge sharing	
	Linear Topology ($V_s + V_d$)	Tree Topology ($V_s + V_d$)
S_1 and C_1	$V_{buffer} - 2V_{source}$	$V_{buffer} - 2V_{source}$
S_2 and C_2	V_{buffer}	$V_{buffer} - 2V_{source}$
S_3 and C_3	$V_{buffer} + 2V_{source}$	V_{buffer}

4.3 Multi-level Clock Generation Circuit Design

This section deals with the new circuit techniques to enhance the knee frequency of the linear charge pump as well as the output current. The proposed technique is the multi-level clock based linear charge pump, the idea deals with increasing the

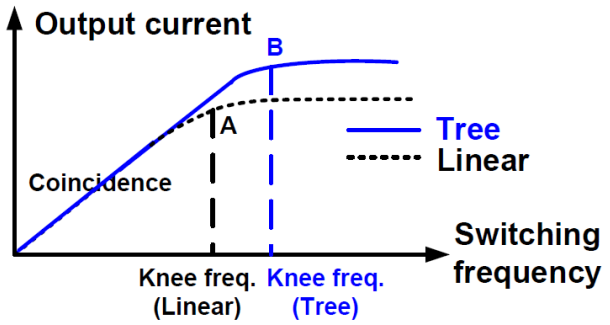


FIGURE 4.3: Knee frequency comparison between both designs [51]

driving clock voltage across the stages to increase the gate voltages of the switches (V_g).

The proposed design is similar to [51], however, it is dealing with increasing V_g rather than decreasing ($V_d + V_s$). Since the gates of the MOS switches are derived by clock generator, so the most logical solution is to increase the voltage level of this clock phases according to their driving stages. This technique should guarantee a lowered ON resistance during charge sharing according to Equation 4.2, accordingly the knee frequency and the output power are expected to be increased.

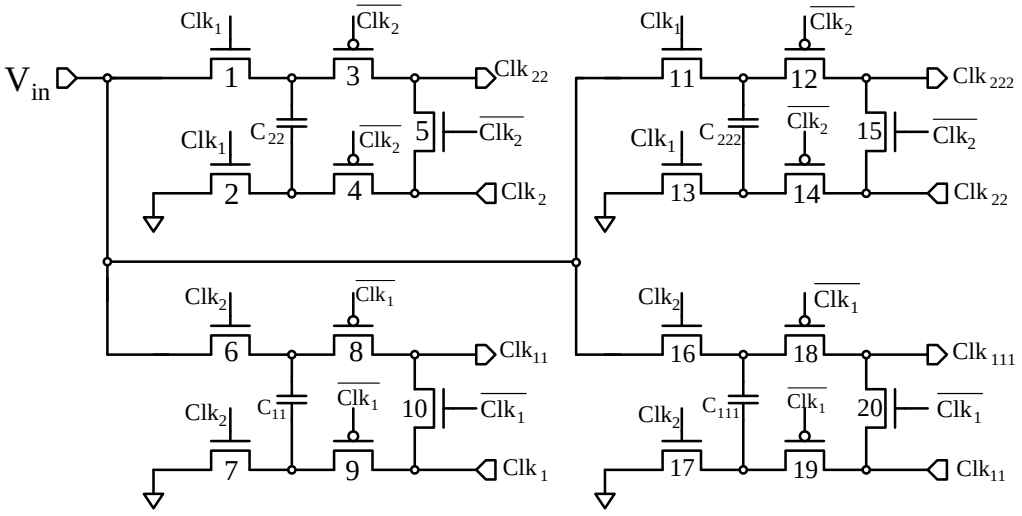


FIGURE 4.4: Multi-level Clock Generator Circuit for a 3-Stage Charge Pump

Figure 4.4 shows the proposed multi-level clock phase generator, this generator applied to the 3-stage linear SCCP shown in Figure 4.1. The design of the circuit is based on two original non-overlapping clocks (Clk_1, Clk_2). Those clocks are applied only to the first stage. The generated (Clk_{11}, Clk_{22}) are applied to the second stage. Accordingly, The generated (Clk_{111}, Clk_{222}) are applied to the final stage. In order to generate Clk_{22} from Clk_2. The capacitor C_{22} is initially charged through (M_1, M_2) in the previous phase, then the voltage is boosted-up on the next phase through (M_3, M_4) producing an amplified version of Clk_2. The pass transistor M_5 is inserted to guarantee a grounded output while charging C_{22} in the previous phase. The proposed design guarantees perfect pull up through (M_3, M_4) and perfect pull down through M_5 [45]. The same scenario is applied to (Clk_{11}). Similarly, (Clk_{111}, Clk_{222}) are generated, however the excitations are the new amplified versions. The size of this circuit should be small enough to prevent power consumption from the input source and maximize the absorbed power by the charge pump.

Figure 4.5 displays the original clock phases of the charge pump. It can be shown that the inverted version is needed in order to perform the multi-level clock generation.

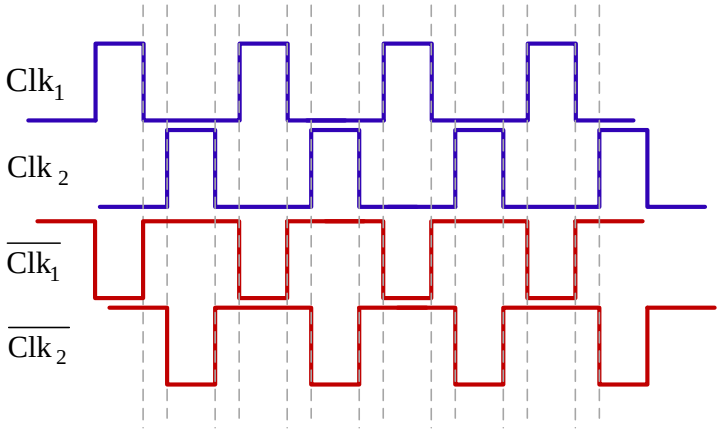


FIGURE 4.5: Clock excitations of the Multi-level Clock Generator

Figure 4.6 shows the new clock phases after adding the new circuit. The input voltage is set to $0.3V$, which is the typical voltage of the PV cell in case of micro-scale solar energy harvesting. The output super capacitor is set to $1V$. it is clear from Figure 4.6 that clock voltage can get higher values than the output buffer voltage, whereas, in [51] all the clock phases of all stages are having the same voltage level of the output super-capacitor.

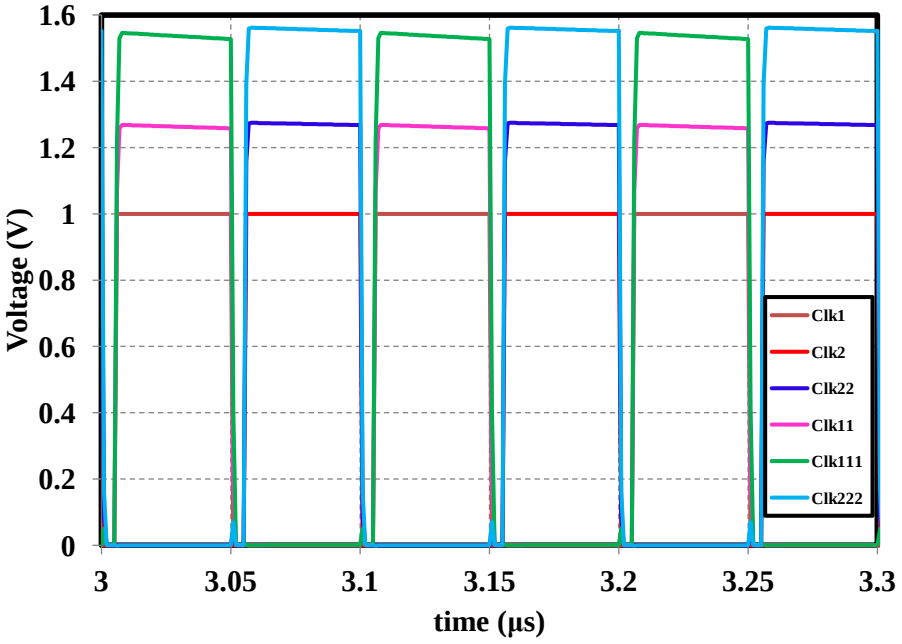


FIGURE 4.6: The Six Clock Phases Generated by the Multi-Clock Generator

The drawback of this technique is that it can't be suitable for PV cells that exhibit relatively high open circuit voltage (V_{oc}), as the gate voltage is limited by the device oxide breakdown voltage. Accordingly, the number of stages is limited by the value of the open circuit voltage value. If V_{oc} is small, the number of stages before breakdown increases, accordingly, If (V_{oc}) is large, the number of stages before breakdown decreases. Since the technology node used in TSMC 65nm, the gate breakdown value is around $2.2V$ (calculated by simulations). The maximum number of stages for the simulation done in Figure 4.6 is N=6.

4.4 Simulation Results

This section is dealing with the simulation results of the proposed enhancement. The test bench settings are stated. Limitations of the proposed technique are also discussed.

The test bench is based on Figure 4.1 and Figure 4.4 to create a new charge pump. The input voltage is set to 3 different values $(0.27V, 0.3V, 0.33V)$ for ultra low input voltages. The switch size is set to $200\mu M$ width, the capacitor size is set to $500pF$.

Figure 4.7 shows the charge pump output current versus the clock frequency for 3 different input voltages $(0.27V, 0.3V, 0.33V)$ for the linear charge pump and the same for the proposed technique. It can be shown that the proposed design delivers higher knee frequency at different input voltages compared to the basic linear topology.

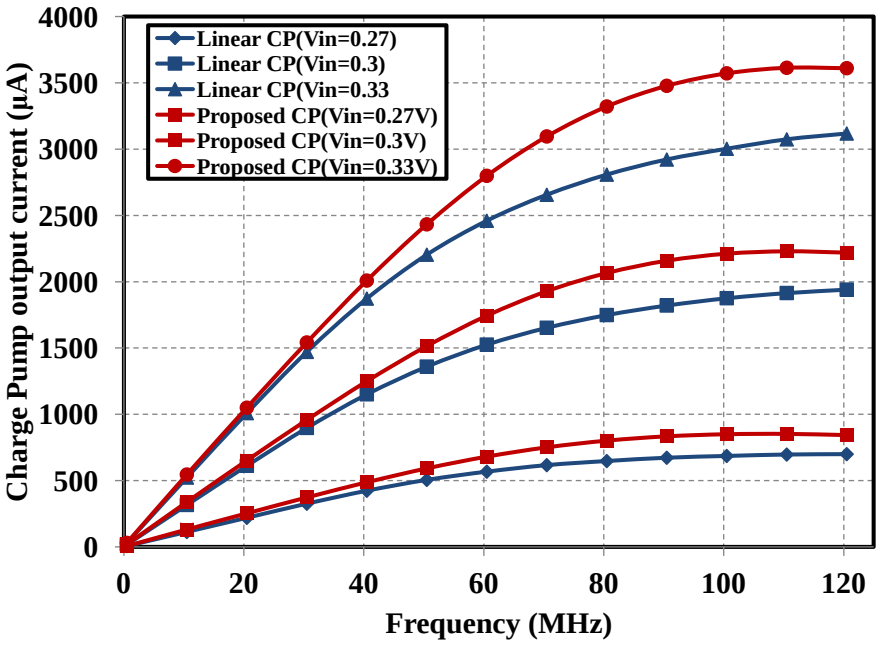


FIGURE 4.7: Charge pump output current for linear CP versus the proposed CP for different input voltages

Figure 4.8 shows the charge pump output current versus the clock frequency for 3 different input voltages $(0.27V, 0.3V, 0.33V)$. The simulation is done for the tree topology proposed in [51] versus the proposed charge pump. It can be shown that the new technique saturates at much higher knee frequencies than the tree topology CP. It should be noted that the multi-level clock generator circuit is consuming some dynamic power from the source so the transferred power to the charge pump is smaller. This phenomenon affects the power efficiency, when the new technique is integrated in an energy harvesting system. The area overhead of the capacitors is (13%), and the area overhead of the transistors is (1.6%). It can be concluded also that increasing the gate voltage of the linear CP is more efficient than using single level clock for the tree CP.

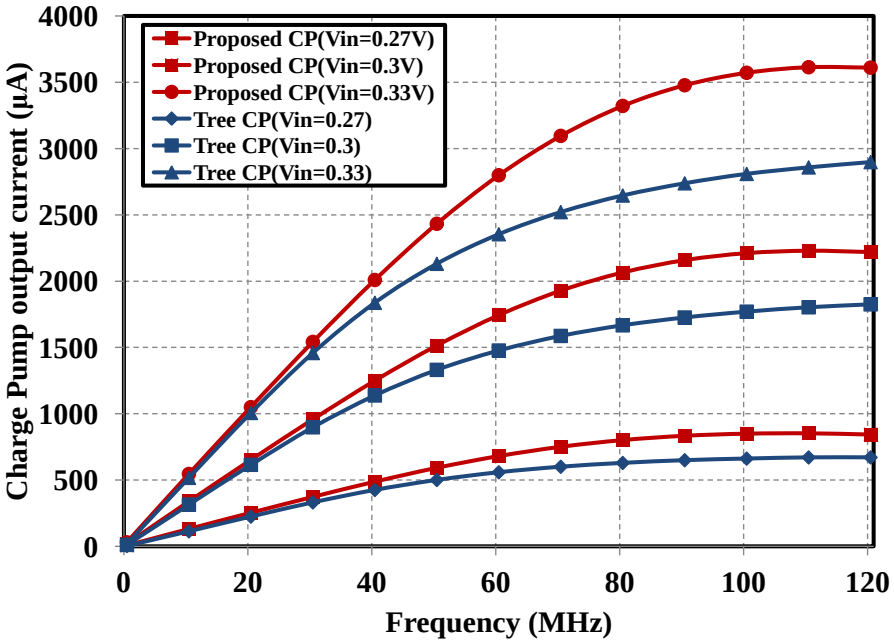


FIGURE 4.8: Charge pump output current for the proposed charge pump versus tree topology charge pump for different input voltages.

From the simulation results, it can be concluded that some circuit design changes enhance the power capability of the linear charge pump. Since the power converter is a critical part in designing power harvesters, it is good to test the charge pump across process corners in order to test the reliability of the converter.

Five different simulations are done for input voltage equals to $0.3V$. Figure 4.9 shows the six simulated corners: typical-typical, fast-fast, slow-slow, slow-fast and fast-slow.

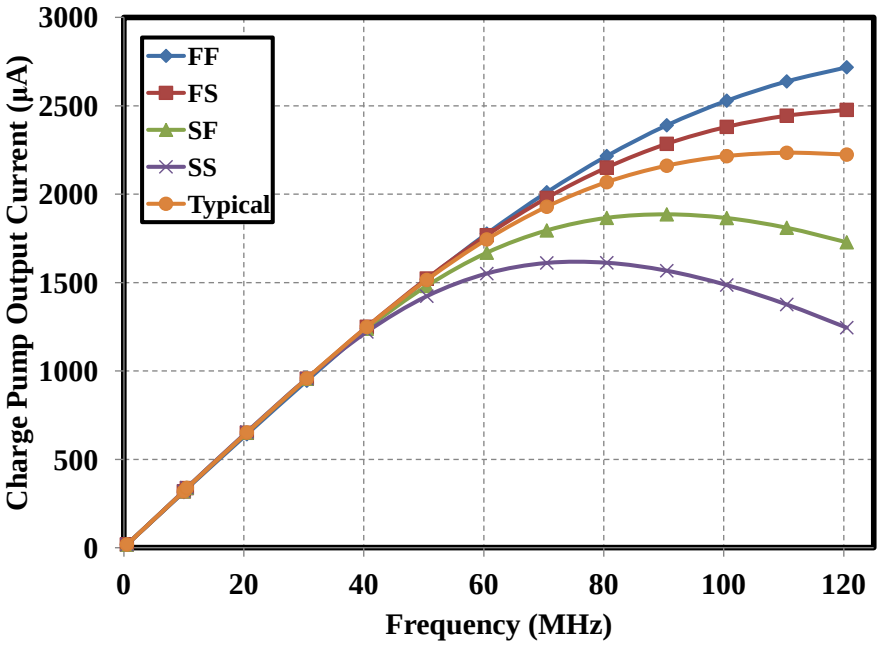


FIGURE 4.9: Process corner simulation for the proposed charge pump

From Figure 4.9, it can be illustrated that the charge pump is working fine below the knee frequency, and starts to deviates from the nominal curve after the knee frequency. The reason behind this phenomenon is that at low frequency, the effect of threshold voltage variation on the ON MOS resistance is weak and complete charge sharing takes place. Whereas at high frequency, the threshold voltage variation starts to dominate on the ON MOS resistance significantly, since incomplete charge sharing takes place. The output current starts to deviates obviously.

Table 4.2 summarizes the maximum output current and the knee frequency of the linear, Tree and the multi-level clock charge pumps. It can be shown that the proposed charge pump shows a good performance in terms of power capability with a small overhead in area. Since the process corners are simulated, it shows

TABLE 4.2: Comparison Table between Linear CP, Tree CP and Proposed CP. ($C = 10pF$, $L = 60nm$, $W = 400nm$)

	Input Voltage	Linear Charge Pump	Tree Topology Charge Pump	Multi-level Clock Charge Pump
Maximum Output Current	$0.27V$ $0.3V$ $0.33V$	$700\mu A$ $1.94mA$ $3.12mA$	$670\mu A$ $1.83mA$ $2.9mA$	$850\mu A$ $2.2mA$ $3.6mA$
Knee Frequency	$0.27V$ $0.3V$ $0.33V$	$49.3MHz$ $50.5MHz$ $50.5MHz$	$47.2MHz$ $48.6MHz$ $47.7MHz$	$55.5MHz$ $54MHz$ $53.25MHz$
Area Overhead	$0.27V$ $0.3V$ $0.33V$	$1200(WL)+$ $150C$	$1200(WL)+$ $150C$	$1200(WL)+$ $170C$

that the proposed charge pump can be verified physically. It should be noted that the overall area of the proposed charge pump is decreased, since the PMOS devices in the transmission gate is removed. The added circuitry for the multi-level clock generator is not as large as the PMOS devices that are removed, this criterion gives an advantage to the proposed design.

4.5 Conclusion

New circuit implementation is proposed in this chapter for an optimized linear charge pump. The idea is based on decreasing the ON resistance of the MOS switches during charge sharing. This is in order to increase the power capability of the charge pump and to increase the knee frequency. The controlling parameter in decreasing the ON resistance is the gate voltage of the switches. It is controlled by generating a Multi-level clock phases across the subsequent stages, in order to compensate for the increase in the source and drain voltage across each stage.

The concept is verified by implementing a switched capacitor circuit responsible for generating higher voltage levels of the input clock phases. The circuit shows its reliability across process corners. Future work can be summarized in integrating the charge pump in an energy harvesting system, to verify its performance for efficient power delivery on the system level.

Chapter 5

Conclusion and Future Recommendations

5.1 Conclusion

This work presents a new design approach and frame work for the microscale solar energy harvesting system targeting miniature devices like wireless sensor networks. Background and literature work are discussed in details. The possible research points are illustrated showing the effectiveness of the proposed techniques. The Control unit design is analyzed through system equations, the circuit realization is very close to the required control technique. The new tracking technique offers sub-threshold operation to some parts of the circuit which have a great impact on the power efficiency and at the same time provides the required tracking efficiency across large range of input light. Comparison with literature systems is also presented.

New circuit techniques are also presented for enhancing the output power of the switched capacitor charge pumps. the proposed design shows its good performance in terms of power capability compared to the basic linear topology and the tree

topology that are already proposed. the drawback of the proposed technique is that it needs extra hardware but not dense, it takes some power from the source to regenerate the amplified versions of the clock phases of the subsequent stages

5.2 Future Recommendations

Future work of this study can be categorized for different abstract levels. Some enhancements on the system level should be done to prevent power loss at the interface between the blocks of the system. Some enhancements must be done for each block independently to get the best performance of each block alone.

First, The proposed system should be transfered to the physical verification stage in order to test the reliability of the proposed techniques and also compare the system area to the literature work.

The control unit can be further optimized to operate in the nW power consumption. This update kills the speed of the whole system, however, very high power efficiency is predictable. another drawback of this new system is that the charge pump flying capacitance dramatically increase in order to maintain power matching at the solar cell side.

One of the most important enhancement is using a different power converter to do a conversion process. Since, the switched capacitor charge pumps can not reach 100 % power efficiency due to the structure of the converter itself, it would be applicable if a DC-DC buck boost converter is desgined with an active coil realization through negative impednace converters. Figure 5.1 shows a conceptual realization of the active coil generation. The excellence of this technqiue is that the advantages of the buck-boost converter can be done all on-chip. Active coils has many drawbacks. They need a DC bias which might not be an option. The quality factor of the coil is very small which directly impacts on the power efficiency.

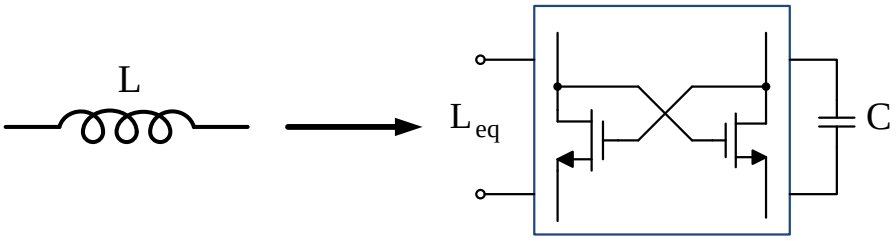


FIGURE 5.1: Active Coil Generation Concept

One of the most important system design issues is that there is no option for an initiall charge in the supercapacitor. Accordingly, one should find a solution for a start-up circuit for charging the super-capacitor to reach the required initial voltage. floating gate transistor based circuits is a good solution that one has to figure it out.

The remaining blocks of the system have to be designed and integrated for a complete power management. First, the supercapacitor should be replaced by a rechargeable battery with integrated energy management to regulate the follow of energy between the battery and the load. The load should also be modeled to be integrated with the whole system to test the reliability of the complete system.

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Appendix A

Photovoltaic Cell Verilog-A Model

```
// Qucs compact photodiode model
// The structure and theoretical background to the photodiode
// Verilog..a model are presented in the Qucs photodiode report .
//
// This is free software ; you can redistributeit and/or modify
// it under the terms of the GNU General Public License as published by
// the Free Software Foundation ; either version 2 , or ( at your option )
// any later version .
//
// Copyright (C) , Mike Brinson , mbrin72043@yahoo . co . uk , October 2008.
//
` include " disciplines . vams "
` include "constants . vams "
module photodiode (Anode , Cathode , Light ) ;
inout Anode , Cathode , Light ;
electrical Anode , Cathode , Light ;
electrical n1 ;
`define attr(txt)(*txt*)
//
parameter real N=1.35 from [ 1e-6: inf ]
` attr(info="photodiode emission coefficient " );
parameter real Rseries=1e-3 from [ 1e-6: inf ]
` attr(info="series lead resistance" unit = "Ohm");
parameter real Is =0.34e-12 from [ 1e-20: inf ]
```

```
` attr(info="diode dark current" unit="A" );
parameter real Bv=60 from [ 1e-6: inf ]
` attr(info="reverse breakdown voltage" unit="V");
parameter real Ibv=1e-3 from [ 1e-6: inf ]
` attr(info="current at reverse breakdown voltage" unit="A");
parameter real Vj=0.7 from [ 1e-6: inf ]
` attr(info="junction potential" unit="V" );
parameter real Cj0=60e-12 from [ 0:inf ]
` attr(info="zero-bias junction capacitance" unit="F");
parameter real M=0.5 from [ 1e-6: inf ]
` attr(info="grading coefficient");
parameter real Area=1.0 from [ 1.0:inf ]
` attr(info="diode relative area");
parameter real Tnom=26.85 from [-273:inf ]
` attr(info="parameter measurement temperature" unit="Celsius");
parameter real Fc=0.5 from [ 1e-6:inf ]
` attr (info="forward-bias depletion capacitance coefficient");
parameter real Tt=10e-9 from [ 1e-20:inf ]
` attr(info="transit time" unit="s");
parameter real Xti=3.0 from [ 1e-6:inf ]
` attr(info="saturation current temperature exponent") ;
parameter real Eg= 1. 16 from [ 1 e..6: i n f ]
` attr(info="energy gap " unit="eV" ) ;
parameter real Responsivity=0.5 from [ 1e-6: inf ]
` attr(info=" responsivity " unit="A/W" ) ;
parameter real Rsh=5e8 from [ 1e-6:inf ]
` attr(info="shunt resistance " unit="Ohm" ) ;
parameter real QEpercent=80 from [ 0:100 ]
` attr(info="quantum efficiency "unit="\%" ) ;
parameter real Lambda=900 from [ 100:2000 ]
` attr(info="light wavelength "unit="nm" ) ;
parameter integer LEVEL=1 from [ 1:2 ]
` attr(info="responsivity calculator selector" ) ;
parameter real Kf=1e-12 from [ 0:inf ]
` attr(info="flicker noise coefficient" ) ;
parameter real Af=1.0 from [ 0:inf ]
` attr(info="flicker noise exponent");
parameter real Ffe=1.0 from [ 0:inf ]
` attr(info="flicker noise frequency exponent");
//
real A, B, T1 , T2 , F1 , F2 , F3 , Rseries_Area , Eg_T1 , Eg_T2 ,
real Vt_T2 , Vj_T2 , Cj0_T2 , Is_T2 , GMIN;
real I1 , I2 , I3 , I4 , I5 , Id , V1 , Q1, Q2, fourkt , TwoQ, Res1 ,
real Res2 , Res , Vt , I_flicker ;
real con1 , con2 , con3 , con4 , con5 , con6 ;
```

```
// Model branches
branch (Anode,n1) b6 ;
branch ( n1,Cathode) b1 ;
//
analog begin
// Model equations
@( initial step )
begin
Rseries_Area=(Rseries+1e-10)/Area ;
A=7.02e-4;
B=1108.0;
T1=Tnom+273.15;
T2=\$temperature ;
Vt=`P_K*300.0/ `P_Q ;
Vt_T2=`P_K*T2/`P_Q ;
F1=(Vj/(1-M))*(1-pow((1-Fc),(1-M))) ;
F2=pow((1-Fc ) , (1+M) ) ;
F3=1-Fc*(1+M) ;
Eg_T1=Eg-A*T1*T1/(B+T1 ) ;
Eg_T2=Eg-A*T2*T2/(B+T2 ) ;
Vj_T2=(T2/T1)*Vj-2*$vt*ln (pow((T2/T1 ),1.5))-((T2/T1)*Eg_T1-Eg_T2) ;
GMIN=1e-12;
Cj0_T2=Cj0*(1+M*(400e-6*(T2-T1)-(Vj_T2-Vj )/Vj)) ;
Is_T2=Is_*pow( (T2/T1),( Xti /N))*limexp(-(Eg_T1)/$vt*(1-T2/T1)) ;
Res1=(QEpercent != 0) ? QEpercent*Lambda/1.2398 e5 : Responsivity ;
Res2=QEpercent*Lambda/1.2938 e5 ;
Res=(LEVEL==1) ? Res1 : Res2 ;
con1=-5.0*N*Vt ;
con2=Area*Is_ T2 ;
con3=Area*Cj0_T2 ;
con4=Fc*Vj ;
con5=Fc*Vj_T2 ;
con6=Bv/Vt_T2 ;
```