The American University in Cairo

School of Science and Engineering

A programmable receiver front-end for multi-band multi-standard applications

A Thesis Submitted to

Electronics Engineering Department

In partial fulfillment of the requirements for

the degree of Master of Arts/Science

By Hoda Ahmed Abdelsalam

Under the supervision of:

Prof.YeheaIsmail

Dr. Emad Hegazi

Dr. Hassan Mostafa

November/2014

Cairo, Egypt

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Thesis Supervisor

Affiliation:

Date _____

_____

Thesis first Reader

Affiliation:

Date _____

_____

Thesis Second Reader

Affiliation:

Date _____

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Department Chair

Date _____

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Dean of SSE

Date _____

DEDICATION

From Deep of My heart

To: My beloved Mother, My husband, My family, My dear friends Sarah and Sally

ACKNOWLEDGMENTS

ABSTRACT

OF THE THESIS OF

Hoda Ahmed Ahmed Abdelsalam Elbanna   for   Master of Science

Major: Electronics Engineering

The American University in Cairo

Title: A programmable receiver front-end for multi-band multi-standard applications

Supervisor: Prof. Yehea Ismail   Co-Supervisor: Dr. Emad Hegazi, Dr.Hassan Mostafa

Nowadays, wireless communication devices need a compact wireless receiver, so that it can access all the available services at any time and at any location with minimum power consumption and compact area. The desire for covering all the service specifications tremendously increases the demand for multi-band/multi-standard wireless receivers. A reconfigurable receiver comes to give a hand. In this work, a universal programmable multi-band multi-standard receiver using CMOS technology is proposed. The receiver aims to target LTE specifications on the frequency range (700MHz-2.4GHz) as a case study to prove the concept of supporting multi-bands. The receiver is tested over three different frequencies 500MHz, 1GHz and 2GHz to prove its programmability. Sampling receivers and impedance translation technique are the main factors to approach the desired programmable receiver front-end. The receiver uses a quadrature band-pass charge sampling filter programmed via its controlling clocks. It forms the signal path which selects the signal, down-converts it to IF frequency and subsamples the signal decreasing the sampling frequency of the proceeding ADC. By adjusting the controlling clocks of the switches, the filter center frequency is maintained at the desired frequency. A time varying matching network based on impedance translation technique is used for multi-frequencies matching and further selectivity enhancing the receiver's linearity. The receiver front-end architecture achieves a NF of (7: 9) dB, a gain of (23: 28) dB, an out-of-band IIP3 of (-1.9 : -5.5) dBm and an in-band IIP3 of (-1.9 : -5.7) dBm across the tested frequencies. The design is tested across process corners. The layout of the design occupies 0.45mm^2. The design is tested post layout to prove its reliability.

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List of abbreviations

CMOS: complementary metal oxide semiconductor

LTE: Long Term Evolution

NF: Noise Figure

IIP3: Inter-modulation Intercept Point

RF: Radio Frequency

LNA: Low Noise Amplifier

IF: Intermediate Frequency

DSB: Double Sided Band

SSB: Single Sided Band

P1dB: 1dB compression point

BDR: Blocking Dynamic Range

SFDR: Spurious Free Dynamic Range

IM: Inter-modulation

LPF: Low Pass Filter

I/Q: In-phase/ Quadrature

IR: Image Rejection

BW: Bandwidth

SNR: Signal to Noise Ratio

CMFB: Common Mode Feedback

FIR: Finite Impulse Response

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1. Introduction

1.1. Motivation

The demand for multi-band multi-standard receivers used for soft-ware defined radio applications [1] has been increasing for over a decade. The conventional receivers require narrow band selective filter with off chip components such as SAW filter and passive LC matching network with inductors and capacitors. These components are inherently narrow band hard to tune [2, 3]. Filtering limits the blockers and hence relaxes the linearity requirements. Eliminating the off-chip band pass selective filter implies high linearity requirements. Different ideas are proposed in the literature for receiving several widely spaced bands. Multi-path narrow-band front-end architecture is one of the well-known receivers where one path is powered on at a time [4, 5]. This design consumes large area on/off chip and large power consumption. Wideband receivers [6, 7] and sampling receivers [8, 9& 10] also come to offer a solution, however they have moderate linearity and poor matching. Another idea is to transfer the signal sampling and analog-to-digital (A/D) interface from the baseband to RF side, in order to enable further signal processing to take place in the digital domain. Digital signal processing allows elimination of the non-idealities of analog signal processing, such as device noise and non-linearity. However, this dictates a high speed ADC in the receiver's front-end with high sampling frequency and large dynamic range. This requires tough specifications of the ADC design and consumes very high power. Connecting the antenna directly to a CMOS passive mixer without LNA [11, 12] can provide significant benefits, such as achieving extremely low power consumption and increasing the tuning range and linearity. However they have low in-band linearity and high power consumption.

1.2.Objective

The objective of this work is to implement a programmable receiver front-end architecture with high linearity to compensate for the eliminated off-chip band pass filter. The idea of charge sampling proves to be a good proposal for the receiver front-end signal path. It gives gain to the signal, has good linearity and low noise figure, it subsamples the signal and down-converts it to low IF frequency. By adjusting the controlling clocks of the sampler, the receiver is able to support certain frequency band. The usage of time-varying matching network satisfies good tunable matching with further selectivity enhancing the receiver's linearity. The proposed receiver front-end architecture targets LTE specifications on the band of (700MHz – 2.4GHz) as a case study. The receiver front-end architecture programmability should be tested, in order to prove its capability of supporting multi bands of frequencies. The design is tested at three frequencies 500M, 1G and 2G.

1.3.Thesis Organization

Chapter one includes an introduction to multi-band multi-standard receivers, its role in wireless communication and the objective of this research. Chapter two gives an overview on the existing receiver architectures, the main specifications of any receiver and LTE standard (the targeted case study) specifications. Chapter three describes the proposed receiver architecture, explains the idea of charge sampling and the time varying matching network. Afterwards, it analyzes the architecture regarding its noise, linearity, input power matching and programmability. verilogA language is used for behavioral modeling of the architecture. Chapter four shows the circuit implementation of the charge sampling filter (the transconductor and the switches), the matching network and the digital circuitry generating the controlling clocks of both the sampler and the matching network. The pre layout simulation results of the design at typical conditions as well as across process corners are shown in chapter five. The layout of the design and post layout simulations is presented in Chapter six. Finally the conclusion is shown.

2. Wireless receivers background

2.1. Specifications of receivers

Gain, NF, in-band, out-of-band linearity and input matching are the most important performance metrics that define the RF performance of the receiver. There is a clear trade-off between these parameters with respect to each other and with respect to area and power consumption. The target of any receiver is to achieve the specifications of the desired standards with reasonable area and power.

2.1.1. RF gain

The gain can be voltage or power gain. In case of having the input and the output on the same chip, the voltage gain is considered. Any receiver should be able to amplify the signal to be represented at the output with reasonable amplitude, also it should have low noise figure with relaxing the noise specs of the following blocks. Usually LNA exists at the beginning of any receiver, in order to amplify the signal with low noise.

2.1.2. Noise Figure (NF)

NF is defined as the ratio of the signal to noise ratio (SNR) at the input to that at the output, accordingly NF is representing the noise added to the input referred noise floor. NF formula is given in Eqn.2.1

$$NF = output\_noise - 10\log(B) - Gain - 10\log(KT) \tag{2.1}$$

Where, output_noise is representing the output integrated noise in dB, B is the bandwidth, Gain is the gain of the receiver in dB, K is Boltzmann constant and T is the absolute temperature in Kelvin. (KT) is the thermal noise floor in dBm/Hz and it is equal to -174 dBm/Hz at the room temperature.

The above equation can represent DSB NF or SSB NF according to the definition of the receiver's gain and output noise. Both the signal and the image bands can be folded on the same IF frequency. If the output noise and the gain result from both the signal and the image, then the NF in the equation is representing DSB NF. If the output noise and

the gain result from only one side band, then the NF is representing SSB NF. The SSB NF is 3 dB higher than DSB NF.

2.1.3. Linearity

Linearity requirements of the receiver are characterized by many parameters; P1dB compression point, third order intermodulation product (IIP3), Blocker Dynamic Range (BDR) and Spurious Free Dynamic Range (SFDR).

P1dB is the input power at which the output power decreases by 1 dB less than the expected output power of the receiver. The expected output power is the product of the input power multiplied by the receiver gain. Fig.2.1 is showing P1dB representation.

IIP3 results due to the products of two input blockers. If there are two input blockers at f1 and f2 with the receiver's non linearity shown in Eqn. 2.2 & 2.3, they can intermodulate resulting in in-band intermodulation products at the frequencies of $(2f_2-f_1)$ and $(2f_1-f_2)$ which lie within the input frequency band. IIP3 is defined as the input power value at which the input power is equal to the power of the intermodulation products, while OIP3 is the output intermodulation product .It is equal to IIP3 multiplied by the receiver's gain.

$$V_{out} = a(V_{in})^2 + b(V_{in}) + c \tag{2.2}$$

$$V_{out} = a(V_1\sin(w_1t) + V_2\sin(w_2t))^2 + b(V_1\sin(w_1t)) + c \tag{2.3}$$
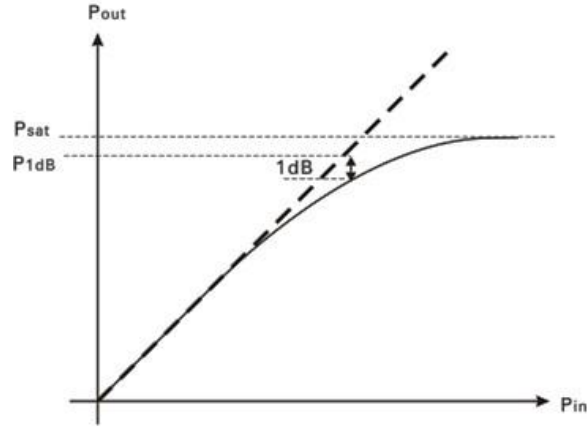
Fig. 2.1 P1dB compression point curve

Fig.2.2 shows the scenario when one of the intermodulation product frequencies overlap with the signal band. This leads to distortion of the desired signal. IIP3 formula is given in Eqn.2.4; where P_{in} is the power of the input signal. P_{IM3} is the input referred power of the third order intermodulation component, it is the output power of one of the two components $(2f_2-f_1)$ or $(2f_1-f_2)$ in dBm minus the receiver's gain.

$$IIP3 = \frac{3}{2} P_{in} - \frac{1}{2} P_{IM3} \qquad (2.4)$$

Another important definition for linearity measurement is the dynamic range, which is the ratio between the strongest and the weakest signals the receiver can process. Spurious free dynamic range (SFDR) and the blocking dynamic range (BDR) are important for any receiver. The lower limit is set by the sensitivity. The upper limit in case of SFDR is set by the maximum receiver input level at a two tone test for which the third-order intermodulation product is below the noise floor. For BDR calculation; the upper limit is the P1dB compression point. The equations of the SFDR and BDR are shown in Eqns. 2.5 & 2.6 respectively.

$$SFDR = \frac{2}{3}(IIP3 - Noise\_Floor) \qquad (2.5)$$

$$BDR = P_{1dB} - (Noise\_Floor) \qquad (2.6)$$
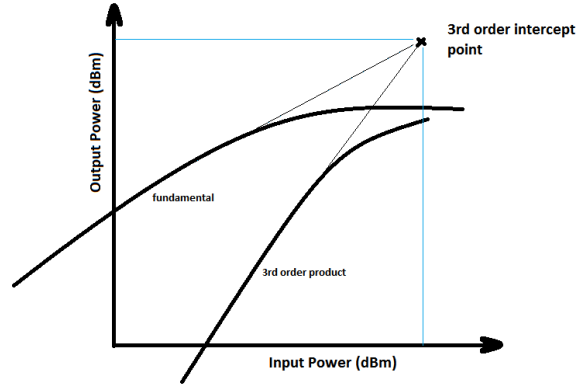
Fig. 2.2 IIP3 curve

2.1.4. Power matching

Any receiver front-end should include matching network in order to match the input power, accordingly most of the carried power passes in the receiver. Matching is measured by S11 which is the reflection coefficient at the antenna side. Fig.2.3 shows the two-port network and Eqn.2.7 is showing the s-parameters matrix. Eqn.2.8, 2.9 and 2.10 shows the definition of S11 (input reflection coefficient at port 1 at a_2=0).
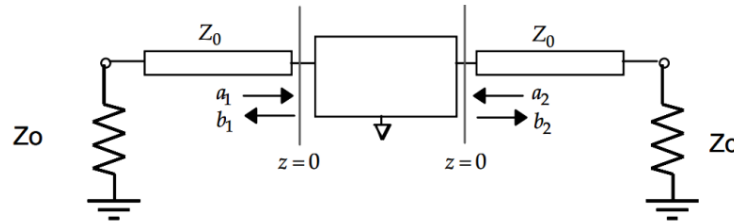
Fig. 2.3Two port network with the propagating waves

$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (2.7)$$

$$b1 = S_{11}a1 + S_{12}a2 \qquad (2.8)$$

$$\Gamma_1 = \frac{b_1}{a_1} \tag{2.9}$$

$$S_{11} = \frac{b_1}{a_1}\big|_{a_2=0} \tag{2.10}$$

2.2. Receivers architectures

Receivers are divided in to two main categories; narrow band receivers and wide-band receivers. Narrow band receivers are based on the conventional receiver design including highly selective band pass filter, LNA and mixers like Super heterodyne, zero IF receiver and low IF receivers. Wide band receivers include multiple parallel narrow band receiver front-ends, wide-band receiver front-end using wide-band LNA, sampling receivers and receivers based on mixer first technique.

2.2.1. Narrow band receivers

Narrow band receivers are based on the conventional receiver architecture composed of BPF, LNA and mixer. They include super heterodyne receiver, Zero IF Receiver and Low IF receiver.

2.2.1.1. *Super heterodyne receiver*

Super heterodyne receiver architecture [13, 14] is shown in Fig.2.4. RF filter is used to attenuate the out-of-band blockers and the image. A narrow-band front-end LNA with a matching network of passive components is used to provide the signal with gain and with low noise. An external image reject filter is used to attenuate the image frequency. The mixer down converts the signal from RF frequency to IF frequency. Off chip IF filter is used to select the desired channel.
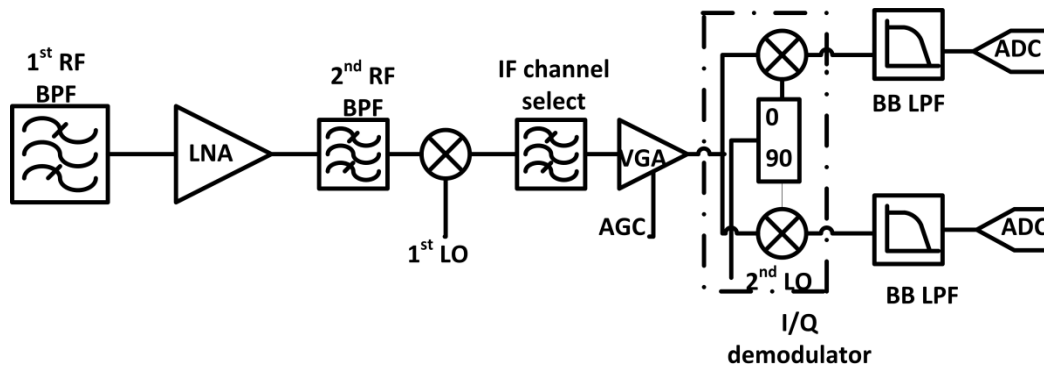
Fig. 2.4 Super heterodyne receiver

2.2.1.2. *Zero IF receiver*

Zero IF receiver [3], [15] block diagram is shown in Fig.2.5. The small size and low cost high on-chip integration degree give zero IF receivers a great importance. Here, RF frequency is down-converted directly to base band. The image reject filter is eliminated as the image frequency is also zero. Channel selection is performed through LP filters. This has several advantages; there is no need for high Q image-reject filter, moreover the IF SAW channel select filter is replaced with low pass filter at base band. The problem is the DC offset [16], it results from the LO leakage from the LO port to the mixer RF input. This leakage is down converted to DC; this is called self-mixing, this unwanted DC offset can saturate the following stages. Another problem is the flicker noise at low frequencies (1/f noise of the mixer) [17].
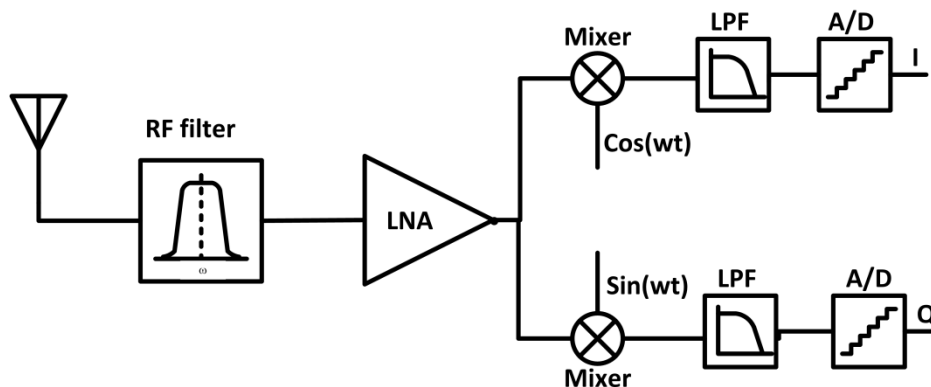
Fig. 2.5 Zero IF receiver

2.2.1.3. *Low IF receiver*

In this receiver [15, 18, 19] shown in Fig.2.6; the RF frequency is down-converted to low IF frequency (few mega Hz). This is better than zero IF receiver in avoiding the problems of DC offset and flicker noise. Using I/Q image reject mixer with a poly-phase filter with low Q instead of high Q IR (Image rejection) filter is also counted as an advantage.
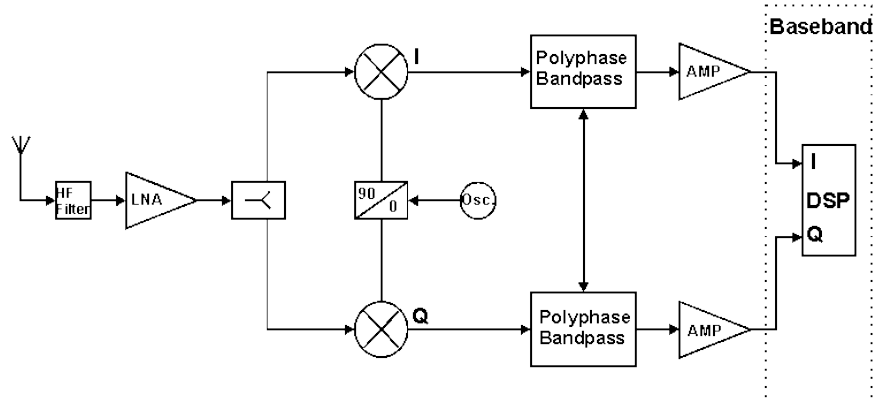
Fig. 2.6 Low IF receiver

2.2.2. Wide-band receivers

These receivers are able to support many frequency bands, they include multiple parallel narrow-band receiver front-ends, wide-band receivers using wide-band LTE, sampling receivers and receivers based on mixer first technique.

2.2.2.1. *Multiple parallel narrow-band front-ends*

This is based on implementing multiple front-ends [4], [5] as shown in Fig.2.7. Each of them is powered on at a time and responsible to support a certain frequency band. However it consumes large on/ off chip area and has high power consumption as well.

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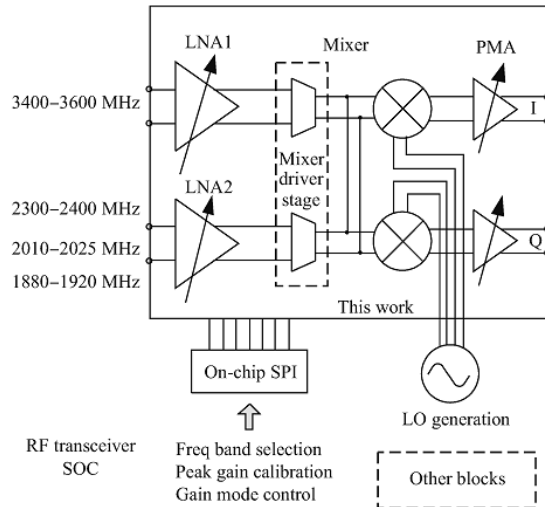
Fig. 2.7 Multiple Parallel narrow-band receiver front-ends

2.2.2.2. *Wide-band receiver front-end*

Wide-band receiver front-ends are based on implementing wide-band LNAs [6, 7], this is to support multi-bands with achieving the required specs. They provide moderate linearity and poor matching.

2.2.2.3. *Sampling receivers*

The conventional receiver front-end is replaced by another structure which samples the signal at RF frequency, down converts it to IF frequency or base band frequency to be processed in the base band. However it has poor matching and moderate linearity [8, 9, 10]. The structure of sampling receivers is shown in Fig.2.8 [9].
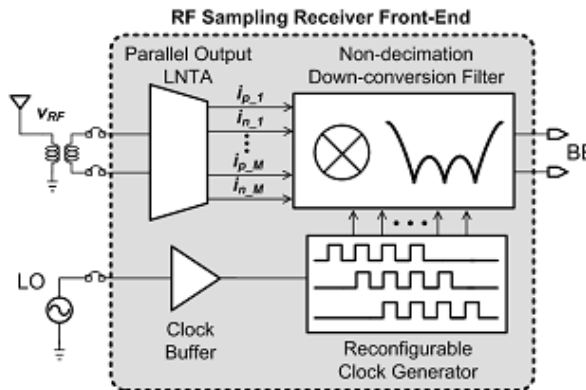
Fig. 2.8 Sampling Receiver Front-End

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2.2.2.4.   *Mixer first receiver architecture*

In this architecture shown in Fig.2.9 [20]; the LNA is translated to the base band side. It depends on impedance translation technique [11, 12]. The impedance effect in the base-band side is translated to the RF side. Resistances and capacitances giving low pass filter response in the base-band side results in band pass filter around the LO frequency in the RF side. This provides matching and filtering at the tuned LO frequency, accordingly, it leads to low NF, good matching and high out of band linearity at this frequency. However it has large power consumption and poor in band linearity.
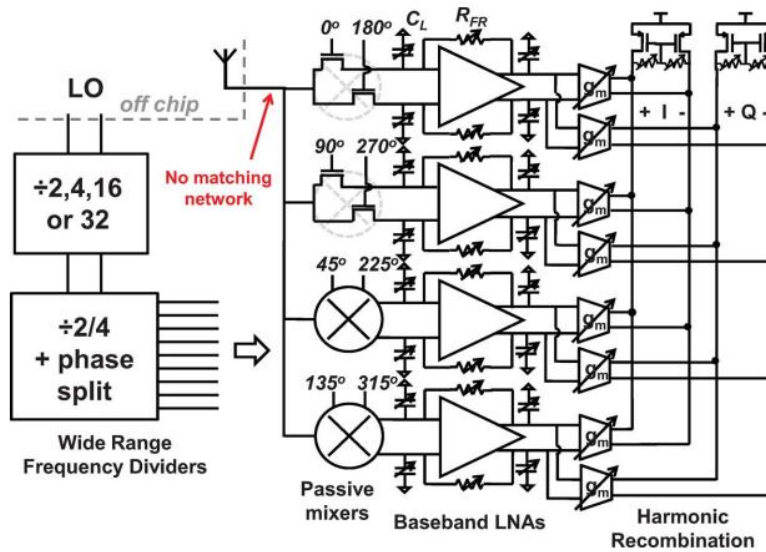
Fig. 2.9 Mixer first receiver

2.3. The targeted case study (LTE Specifications)

In this work, LTE is targeted as a case study to prove the concept of supporting multi frequency bands. LTE is chosen as a proof of concept as it is the most popular standard nowadays; also it covers multi frequency bands.

The LTE standard frequency bands ranges from 700MHz to 2.4GHz and the advanced LTE reaches till 6GHz. The uplink and down link frequency bands are shown in Table 2-1 [21]. The LTE channel bandwidth can be 1.4MHz, 3MHz, 5MHz, 10MHz,

15MHz and 20MHz. It should be noted that for a receiver to be able to support LTE standard, it should achieve LTE specifications of noise figure, out-of-band and in-band linearity on the whole frequency range (for all LTE bands).

2.3.1. Noise Figure

Noise Figure = $174 + pin_{min} - 10log(BW)$ - SNR_{min}, where 174 dBm is the noise floor, Pin_{min} is the required minimum sensitivity; Table 2-2 [22] is showing the minimum sensitivity for different channel bandwidth, BW is the channel bandwidth and SNR_{min} is the minimum signal to noise ratio.

For 10MHz channel bandwidth, Pin_{min} = -94 dBm with considering the SNR = 1dB, the noise figure can be calculated to be 9dB [23], with considering a margin for the insertion loss of the duplexer and RF module, the required NF can range from 7-9 dB.

LTE Band	Uplink eNode B receive UE transmit			Downlink eNode B transmit UE receive			Duplex mode
1	1920 MHz	–	1980 MHz	2110 MHz	–	2170 MHz	FDD
2	1850 MHz	–	1910 MHz	1930 MHz	–	1990 MHz	FDD
3	1710 MHz	–	1785 MHz	1805 MHz	–	1880 MHz	FDD
4	1710 MHz	–	1755 MHz	2110 MHz	–	2155 MHz	FDD
5	824 MHz	–	849 MHz	869 MHz	–	894 MHz	FDD
6	830 MHz	–	840 MHz	875 MHz	–	885 MHz	FDD
7	2500 MHz	–	2570 MHz	2620 MHz	–	2690 MHz	FDD
8	880 MHz	–	915 MHz	925 MHz	–	960 MHz	FDD
9	1749.9 MHz	–	1784.9 MHz	1844.9 MHz	–	1879.9 MHz	FDD
10	1710 MHz	–	1770 MHz	2110 MHz	–	2170 MHz	FDD
11	1427.9 MHz	–	1452.9 MHz	1475.9 MHz	–	1500.9 MHz	FDD
12	698 MHz	–	716 MHz	728 MHz	–	746 MHz	FDD
13	777 MHz	–	787 MHz	746 MHz	–	756 MHz	FDD
14	788 MHz	–	798 MHz	758 MHz	–	768 MHz	FDD
17	704 MHz	–	716 MHz	734 MHz	–	746 MHz	FDD
18	815 MHz	–	830 MHz	860 MHz	–	875 MHz	FDD
19	830 MHz	–	845 MHz	875 MHz	–	890 MHz	FDD
...							
33	1900 MHz	–	1920 MHz	1900 MHz	–	1920 MHz	TDD
34	2010 MHz	–	2025 MHz	2010 MHz	–	2025 MHz	TDD
35	1850 MHz	–	1910 MHz	1850 MHz	–	1910 MHz	TDD
36	1930 MHz	–	1990 MHz	1930 MHz	–	1990 MHz	TDD
37	1910 MHz	–	1930 MHz	1910 MHz	–	1930 MHz	TDD
38	2570 MHz	–	2620 MHz	2570 MHz	–	2620 MHz	TDD
39	1880 MHz	–	1920 MHz	1880 MHz	–	1920 MHz	TDD
40	2300 MHz	–	2400 MHz	2300 MHz	–	2400 MHz	TDD

Table 2-1 LTE up link and down link bands

Channel BW	UE reference sensitivity level
5MHz	-97.3dBm
10MHz	-94.3dBm
15MHz	-92.5dBm
20MHz	-91.3dBm

Table 2-2 minimum sensitivity for different frequency bands

2.3.2. Out-of-band linearity

Out-of-band linearity is measured by the out-of-band intermodulation products; it depends on the transmitter leakage in case of FDD (Frequency division multiplexing) as well as maximum input power at the antenna in case of TDD (time division multiplexing). The interferers are located further than the desired band by more than 20MHz.

The interferer signals power ranges from -44dBm to -15 dBm according to the offset frequency. The interferer power is -44 dBm for 15MHz- 60MHz offset, -30 dBm for 60MHz- 80MHz offset and -15 dBm for offset greater than 85MHz [24].The transmitter leakage depends on the transmitted signal power and the duplexer isolation.

Out-of-band intercept point (IIP3) is calculated as -10 dBm for 10MHz channel bandwidth for FDD, assuming the Tx leakage of -30 dBm for 10MHz channel bandwidth till -6 dBm for 1.4MHz channel bandwidth [23].

Out-of-band intercept point (IIP3) is calculated for TDD assuming the maximum input power level at the antenna of -25 dBm and giving room of 12 dB, P1dB is -13dBm and IIP3 is higher than P1dB by 10dB, so IIP3 should be -3 dBm. For FDD depending on duplexer isolation of 50 dB and transmitter leakage power of 23 dBm and a room of 10 dB, P1dB is calculated as the transmitted power subtracted from it the duplexer isolation to be -16 dBm and IIP3 is higher by 10 dB to be -6 dBm[25].

2.3.3. In-band linearity

In-band linearity is measured by in-band intermodulation products, it results from cross modulation of other channels on the same band and CW interferers in the same band. The interferers are located at frequencies away from the desired band by less than 20MHz.

As shown in Table 2-3 [22], for 10MHz channel bandwidth, the interferers are CW signal of -46 dBm located at $(\frac{BW}{2} + 7.5MHz)$ away from the desired signal. The modulated signal of bandwidth 5MHz has power equals to -46 dBm at double the frequency of CW.

In-band IIP3 can be calculated as $\frac{1}{2}(3P_{int} - P_{IMD3})$, Pint = -46 dBm, for P_{IMD3}, it can be calculated based on Eqn.2.11 [24] or Eqn.2.12 [23]. By using Eqn2.11 for a 10MHz channel BW with substituting for the noise floor of -104 dBm for a 10MHz channel BW, Rx margin of 6 dB for a 10MHz channel BW and the modulated channel bandwidth of 5MHz; the P_{IMD3} is calculated to be -102.24 dBm accordingly IIP3 is -17.88 dBm [24]. By using Eqn2.12 [23] for a 10MHz channel BW with substituting for the maximum input power of -88 dBm which is the sensitivity level added to it 6dB (the Rx margin), SNR_{min} of 1 dB and 3rd order intermediation contribution to SNDR of 0.25; the P_{IMD3} is calculated to be -95 dBm accordingly the IIP3 is -21.5 dBm [23].

Parameter		Channel bandwidth				Unit
		5MHz	10MHz	15MHz	20MHz	
Propagation condition		Static				-
Wanted signal characteristic		QPSK, code rate:1/3				-
Wanted signal mean power		<REFSENS>+6		<REFSENS>+7	<REFSENS>+9	dBm
Interfering signal 1	Characteristic	CW				-
	Mean power	-46				dBm
	Few offset	10	12.5	15	17.5	MHz
Interfering signal 2	Characteristic	5MHz BW modulated				-
	Mean power	-46				dBm
	Few offset	20	25	30	35	MHz

Table 2-3interferers and blockers for different channel bandwidths

$$10\log_{10}(10^{\frac{noise\_floor + Rx\ margin}{10}} - 10^{\frac{noise\_floor}{10}}) - 10\log_{10}(\frac{targeted\ channel\ BW}{modulated\ channel\ BW})$$

(2.11)

$P_{IMD3} = (senistivity\_level+Rx\_margin)+10\log_{10}(3^{rd}$ order intermediation contribution to SNDR) - SNR_{min}

(2.12)

3. The proposed receiver front-end architecture

3.1.Structure of the proposed architecture

The proposed architecture block diagram is shown in Fig.3.1. A single path of the quadrature charge sampling filter and the matching network are shown. The filter center frequency is adjusted through its controlling clocks. It provides high linearity, low noise figure, image rejection, sub sampling, down-conversion to IF frequency and gives gain to the signal at the desired frequency. It is composed of a transconductor (Gm) converting the input differential RF voltage to current, which will be integrated on the sampling capacitances. A time varying matching network is used for tunable matching and selectivity. Adjusting the controlling clocks determines the frequency at which the matching will be held.
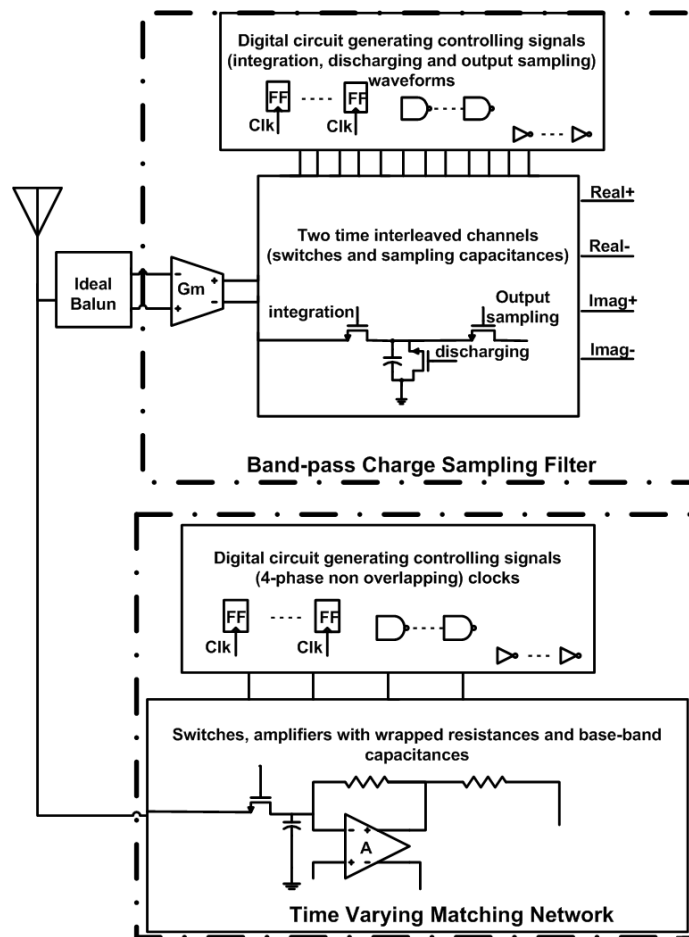
Fig. 3.1The block diagram of the proposed Receiver front-end architecture

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3.2. Charge sampler

3.2.1. Charge sampling technique

Current sampling gains more interest than voltage sampling, because it has lower noise figure and better selective anti-aliasing filtering effect.

Integrating the current in certain time interval T_i (the integration time) on a sampling capacitance, then sampling the resulting voltage to the output in the output phase gives a low pass sinc filter response shown in Fig.3.2 [26] with notches at multiples of $(\frac{1}{T_i})$, where T_i is the sample integration time. In Fig.3.3; the input voltage is converted to current by the trans-conductor (Gm).It is then integrated on the sampling capacitance when the clock *integ* is ON. Afterwards, the resulting voltage is sampled to the output when the clock *out* is ON. Finally the sampling capacitance is discharged. Fig.3.4 is showing the waveforms controlling the switches
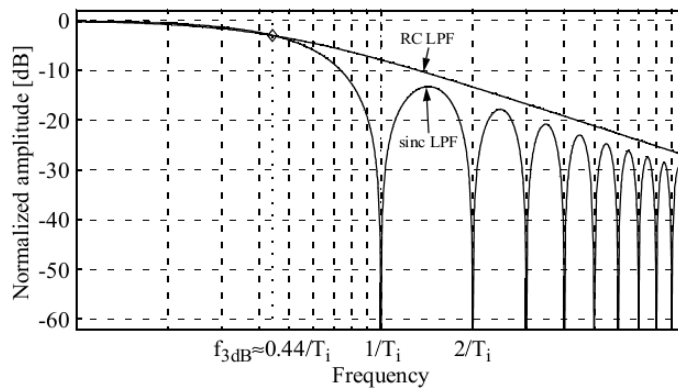
Fig. 3.2 LPF Sinc Filter response
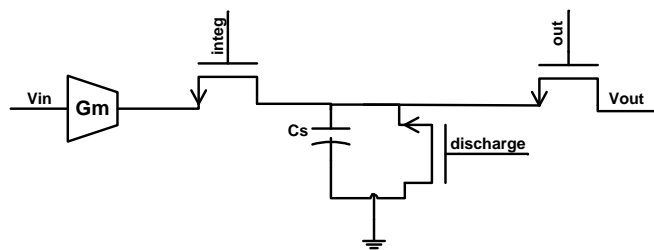
Fig. 3.3 Charge sampling technique
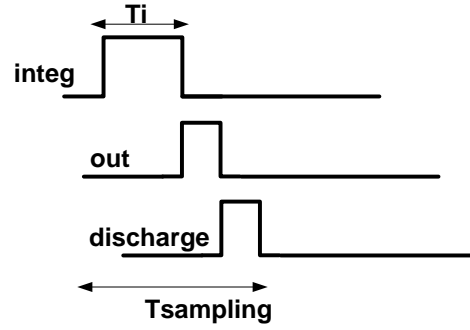
Fig. 3.4 Controlling clocks of the charge sampler

The transfer function of the resulting sinc low pass filter response is given in Eqn. 3.1 [26, 27]. This gives dc voltage gain of $\frac{G_m T_i}{C_s}$, where G_m is the transconductance, C_s is the sampling capacitance and T_i is the integration time. For an optimal anti-aliasing filtering effect, the sampling time of the sampler should be equal to the integration time to have the filter's notches at multiples of the sampling frequency. However the sampling time should count for the output sampling time, the capacitances discharging time in addition to the integration time. Time-interleaved integrating operation, shown in Fig.3.5, gives a hand to solve this problem. This is done by having the first channel in the integration phase, while having the second channel in the sampling-to-output and the discharging phases and vice versa as shown in Fig.3.6.

$$H(f) = \left| H_{SINC}(f) \right| = \frac{G_m}{C_S} \cdot \left| \frac{\sin(\pi f T_i)}{\pi f} \right| \tag{3.1}$$

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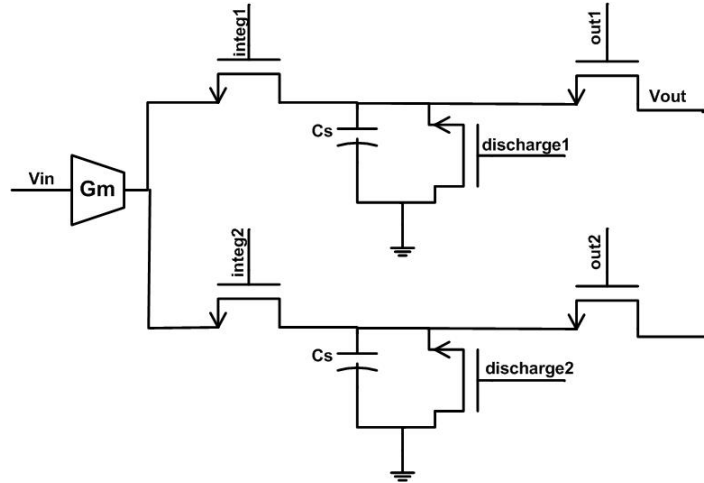
Fig. 3.5 Time interleaved integrating operation
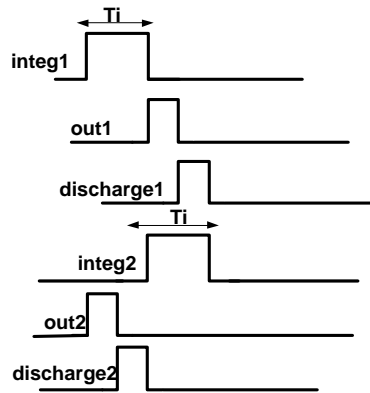
Fig. 3.6 Controlling clocks of time interleaved integration operation

3.2.2. FIR filtering effect

Integrating successive N current samples on the sampling capacitance in the integration phase, then sampling them to the output at the sampling rate f_s, gives additional FIR filtering response with sampling frequency f_{sFIR}. The sampling period of this FIR filter is T_f, which is the time difference between two successive samples. The output sampled voltage on the capacitance is read out after the accumulation of the N current samples [26, 27]. The resulting FIR filter response shown in Fig.3.7 [26] has notches on multiples of $(1/NT_f)$. Fig.3.8 is showing the controlling clocks of a charge-

domian filter with embedded FIR filtering response. The transfer function of charge-domain FIR sampling filter is shown in Eqn.3.2 [26]. The DC voltage gain of the charge-sampling FIR filter response is $\dfrac{N\,G_m\,T_i}{C_s}$
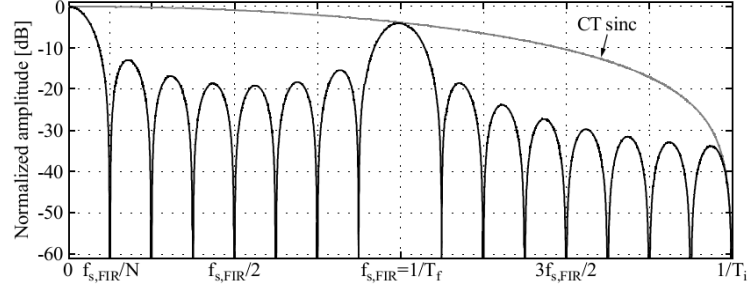
Fig. 3.7 FIR charge sampling sinc filter response
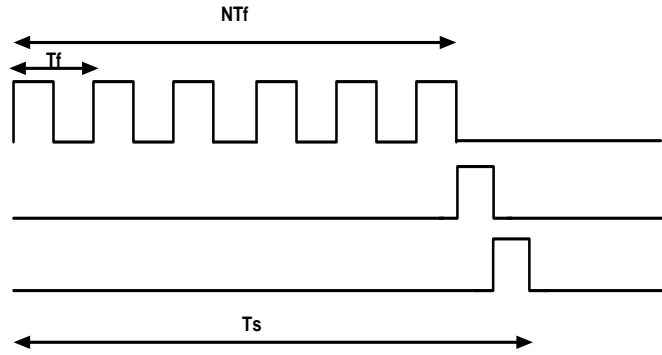
Fig. 3.8Controlling clocks for FIR charge sampling filte

$$H(f) = \frac{V_{out}(f)}{V_{in}(f)} = \frac{G_m}{C_s} \cdot \frac{1 - e^{-j2\pi f T_i}}{j2\pi f} \cdot \sum_{K=0}^{N-1} h_K \cdot z^{-K}\big|_{z = e^{j2\pi f T_f}} \tag{3.2}$$

3.2.3. Quadrature band-pass charge sampling FIR filter

Multiplying the impulse response of the FIR LPF by $e^{\frac{jn\pi}{2}}$ translates it to a band-pass FIR filter centered on $f_c = \dfrac{1}{4T_f}$ [26, 27], where T_f is the time between two successive samples. This is implemented by multiplying the integrated samples by successive sequences of +1,+j,-1 and −j , which means that the real channel samples are multiplied

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by successive sequences of +1,0,-1 and 0 , whereas the imaginary channel samples are multiplied by 0,+1,0 and -1. The current samples are integrated alternately on the real and imaginary channels sampling capacitances. The negative sign is implemented by cross coupling the positive and negative signal paths with a pair of additional switches. The implementation of this quadrature band-pass FIR filter is shown in Fig.3.9. The controlling clocks of the sampler are shown in Fig.3.10. This quadrature band-pass filter shown in Fig.3.11 [26] down-converts the signal to low IF frequency or to DC (the band-pass filter frequency acts as LO frequency), subsamples the signal and provides good image rejection as it has notch at $-f_c$ suppressing the image band. The DC voltage gain of the band-pass filter at f_c is $\frac{2\sqrt{2}\,G_m\,NT_i}{\pi C_s}$.
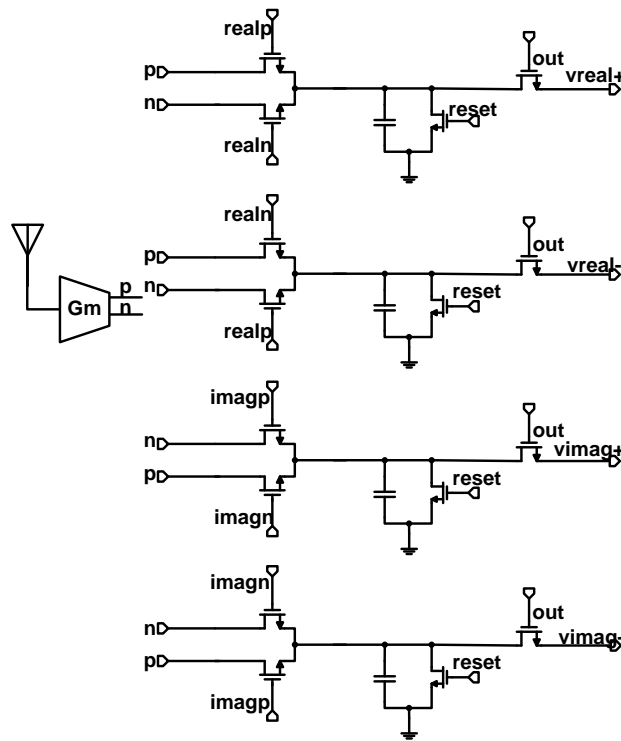
Fig. 3.9 The implementation of the band-pass charge sampler
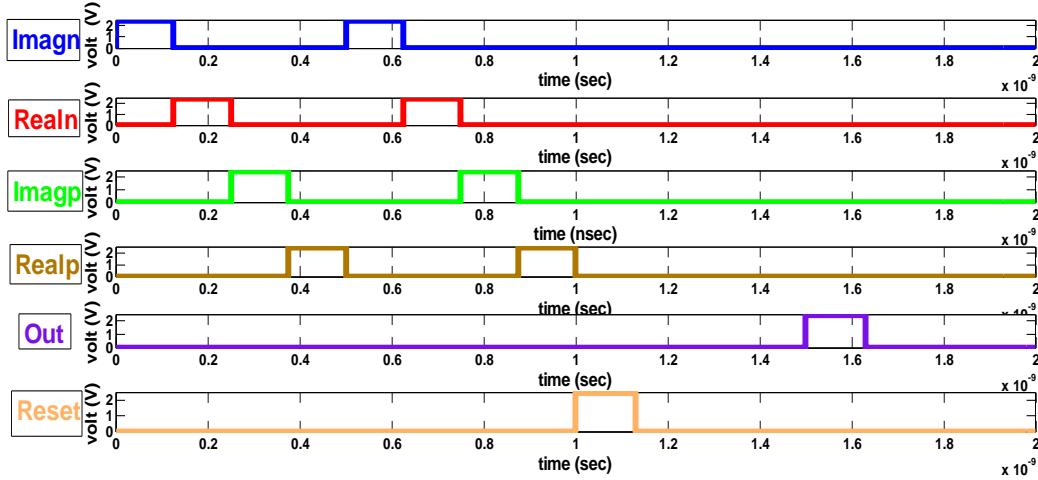
Fig. 3.10 The controlling clocks of the band-pass FIR charge sampler
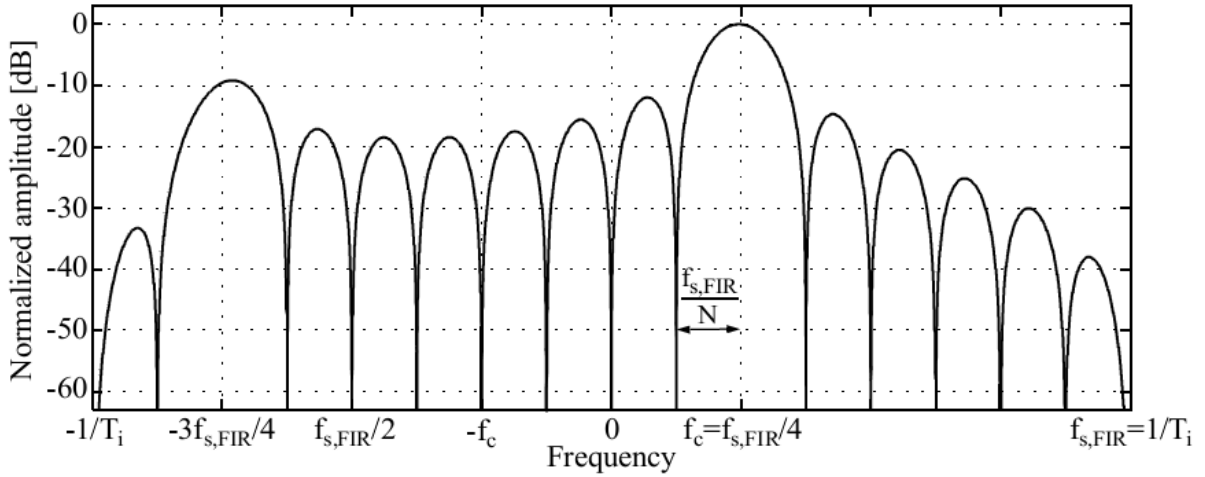
Fig. 3.11 The frequency response of the quadrature band-pass FIR charge sampler

3.2.4. The used time-interleaved quadrature band-pass FIR charge sampling

In the proposed architecture, two time interleaved channels of a quadrature band-pass FIR filter are used to form the receiver signal path. It down-converts the signal to IF frequency, provides good image rejection, sub-samples the signal decreasing the sampling frequency of the following ADC to $\frac{1}{NT_f}$. It also has good anti-aliasing effect by placing the filter's notches on multiples of the sampling frequency and has low noise figure with good linearity. Fig.3.12 is showing the used time

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interleaved quadrature band-pass FIR filter. The clocks controlling the two channels at 2GHz, where Ti is 125 psec are shown in Fig.3.13; here T_f (the time between two successive integrated samples) is equal to the integration time (T_i). At each channel, 8 current samples of successive sequences of +1, +j,-1 and –j are integrated on the sampling capacitances to the output.
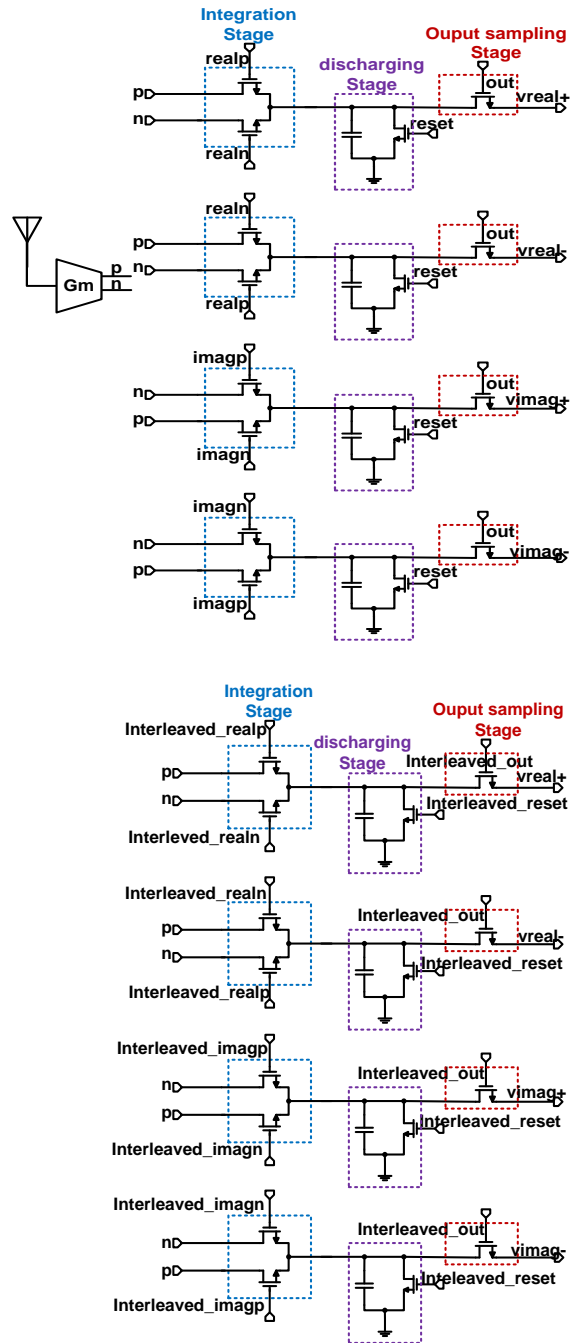
Fig. 3.12 The time-interleaved quadrature band-pass charge sampler

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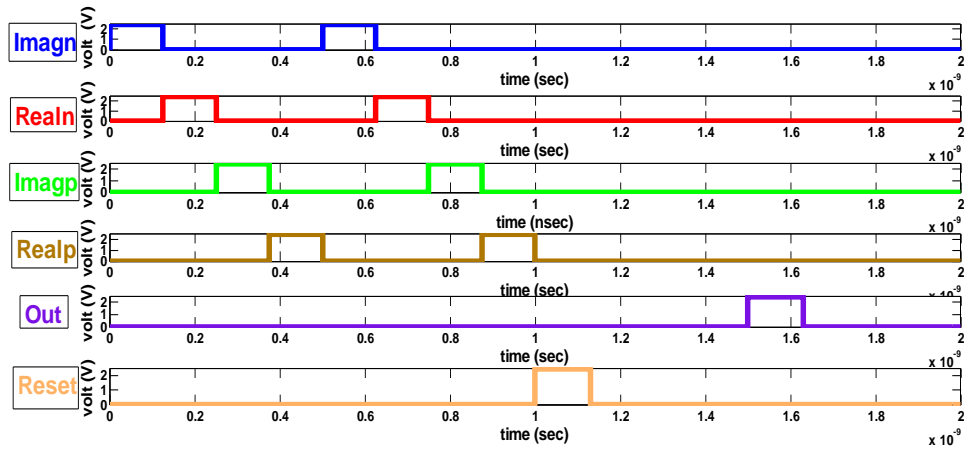
(a)
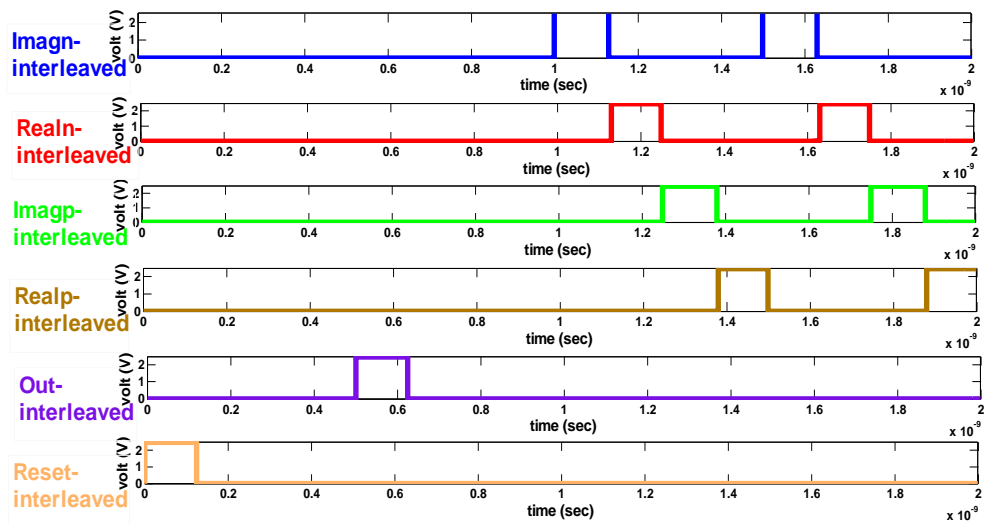
(b)

Fig. 3.13a&b The controlling clocks of the first channel of the band-pass charge sampler and the second channel respectively

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3.3.   Time varying matching network

In conventional receivers, passive network of inductors and capacitors is used for this purpose. The problem showed up in multi-band multi-standard receivers as these components are inherently narrow band. To have the matching guaranteed at different frequencies, the matching network should be tunable. Since, passive networks are hard to tune, in this architecture; a programmable matching network based on impedance translation technique is used.

3.3.1. Impedance translation technique

The matching network shown in Fig.3.14 [20] is based on implementing the matching network in the base-band side and translating its effect to the RF side. The design consists of bi-directional passive switches controlled by 25% duty-cycle non-overlapping clocks and followed by parallel combination of resistance and capacitance. The low pass filter (LPF) effect of the resistance with the capacitance in the base-band side is translated to band-pass filter centered at the LO frequency in the RF side providing more selectivity enhancing the receiver's linearity.
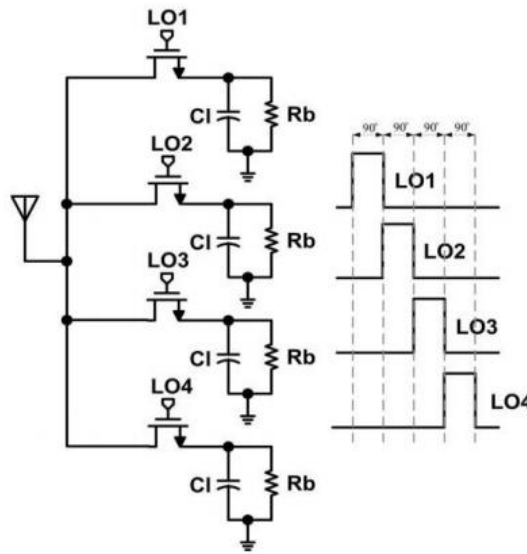
Fig. 3.14 Matching network based on impedance translation technique

The impedance seen by the antenna is shown in Fig.3.15, where R_{sw} is the switch resistance, (γR_b) is the scaled version of the base-band resistance, R_b is the base band resistance, γ counts for the translation effect and R_{sh} is the resistance counting for the

harmonic re-radiation effect. The base-band voltage is remixed with LO odd harmonics and re-radiated to the antenna, this is considered as losses represented by a shunt resistance in parallel with R_b. As the radiations increase, the shunt resistance value decreases and its effect becomes more severe. The usage of quadrature clocks eliminates the image of each harmonic. This indicates that in order to make the matching controlled by the base-band resistance (R_b) value, the switch resistance R_{sw} should be much smaller than R_b and R_{sh} should be much higher than R_b. Controlling the base-band resistance value does control the matching. The capacitance value controls the selectivity of the translated band-pass filter. As the capacitance increases, the band-width of the translated band-pass filter decreases, increasing its selectivity.
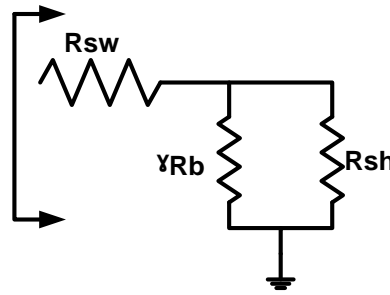
Fig. 3.15 The input impedance seen by the antenna

3.3.2. Final matching network

The final matching network used is shown in Fig.3.16 [20], [28]. The base-band resistance is implemented by a resistance wrapped around an amplifier, in order to decrease its noise contribution by the gain value of the amplifier. This configuration matches the real part of the antenna impedance. The cress-crossed feed-back resistance between the in-phase and quadrature channels is counting for the matching of the imaginary part of the impedance. The imaginary part is resulting from the effect of the base-band capacitance, the parasitics of the pads and the bond wires at the antenna side. These parasitics lead to shifting of the matching notch from the desired frequency.
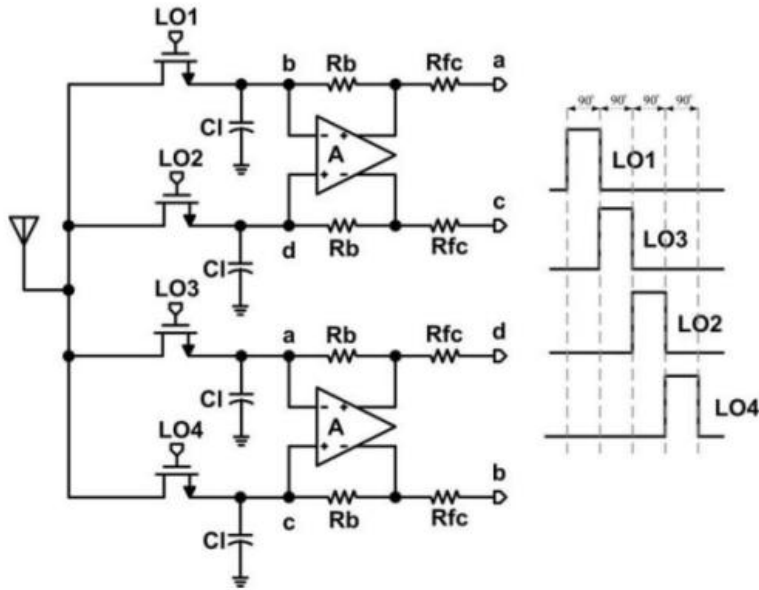
Fig. 3.16 The final matching network

3.4. Programmability analysis

Programmability is achieved easily here as both blocks, the quadrature band-pass FIR charge sampling filter and the matching network, are controlled by the driving clocks.

For the charge sampling filter; by adjusting the sample integration time (T_i), the band-pass FIR charge sampling filter center frequency ($f_c = \frac{1}{4T_i}$) is controlled to be maintained at the desired Local oscillator frequency.

Controlling the number of integrated samples determines the position of the filter's notches and the bandwidth of the signal pass band. It affects the sampler's gain, consequently affecting the receiver's noise figure (NF) and linearity.

By adjusting the LO frequency of the controlling clocks of the matching network, the tunable matching and selective BPF are settled at the desired LO frequency. By tuning the base-band resistance (R_b), the complex part matching resistance (R_{fc}) and the capacitance value, power matching, noise figure matching and selectivity can be controlled.

3.5. Noise analysis

The noise of the band-pass FIR charge sampling filter is added to that of the time varying matching network. The noise of the band-pass FIR charge sampling filter results from the transconductor (G_m) noise (producing both flicker and thermal noise) and the switches thermal noise, the main contributor is the transconductor. The total noise figure is also affected by the receiver's gain which implies the effect of the transconductance value (G_m), N (number of integrated samples) and C_s (the sampling capacitance).

The noise of the time varying matching network includes the noise of the base-band resistances divided by the amplifier's gain value, in addition to the switches and amplifier noise, also the shunt resistance effect losses deteriorates the total Noise Figure (NF). The resistances and capacitances in the matching network are chosen based on trade off between the power matching resistance and noise figure matching resistance.

The resulting noise figure has a bell shape. High noise figure at low frequencies occurs due to the flicker noise of the trans-conductor with small contribution of the amplifier in the matching network, and then the noise decreases to the value of the thermal noise of the charge sampler that is added to that of the matching network. Finally, the noise figure increases at higher frequencies, due to the matching network parasitics. These parasitics will affect the higher harmonics decreasing the value of $Z_{sh.}$

3.6. Linearity analysis

The quadrature band-pass FIR charge sampling filter provides good in-band and out-of-band linearity. The main contributor is the transconductor. Linearity is much more improved due to the matching network selectivity. The capacitance in the matching network affects the receiver's linearity as the capacitance increases; the receiver is able to achieve better linearity.

3.7. Power matching analysis

The matching ideally is controlled by the resistances and capacitances of the matching network, but practically the impedance seen by the antenna is a parallel combination of the matching network translated impedance and the trans-conductor input impedance. The transconductor input impedance should be large enough, to make the matching controlled by the matching network. The base-band resistance value (R_b)

controls the S11 magnitude, the base-band capacitance (C_l) controls the bandwidth of the matching and R_{fc} controls the position of the matching treating the problem of slide shifting from the LO frequency due to the parasitic effect. The matching network parameters are chosen based on a tradeoff between power matching and noise figure matching.

3.8.VerilogA modeling of the architecture

The architecture is behaviorally modeled using verilogA to check its functionality and ability to achieve the required specs. Each block is represented by a verilogA model.

The parameters of the transconductor, integrating switches, discharging switches and sampling-to-output switches are shown in Table 3-1.The sampling capacitance is chosen to be 65fF. The number of integrated samples (N) is chosen to be 8 based on a trade-off between noise figure and linearity.

Block	G_m (S)	Output current noise (A^2 /Hz)	ON resistanse (Ω)	OFF resistance (Ω)	IIp3 (dBm)
Transconductor	50m	$3.3136*10^{-22}$	-	-	-8
Integration_switches	-	$3.3136*10^{-22}$	50	1G	-10
Discharging_switches	-	$1.3807*10^{-22}$	120	10G	25
Sampling to output switches		$2.549*10^{-22}$	65	1G	0

Table 3-1 Charge sampler model parameters

Modeling of the matching network includes the model of the switches, where the most important property of the switches to be modeled is its bidirectional nature. The representing parameters are the switch resistances of 20Ω and the noise current of each switch of $8.284*10^{-22}$. The amplifier is represented by gain of 40 dB (relation between the input voltage and the output voltage) and its noise of $3.3136*10^{-19}$. The base band

resistance (R_b) is 25K, the complex part matching resistance (R_{fc}) is 76K and the base band capacitance (C_l) is 10p.

      For 2GHz input frequency, The PAC gain of the receiver shown in Fig.3.17 is 57 dB as calculated from Eqn.3.3. S11 of the receiver is less than -10 dB at 2GHz as shown in Fig.3.18 and noise figure is shown in Fig.3.19. It doesn't have the expected bell shape as the model is counting only for the thermal noise. The IIP3 for two input signals of frequencies 2.1GHz and 2.12GHz is -1.7dBm as shown in Fig.3.20. The P1dB (1dB compression point) for an input frequency of 2.1GHz is -10.5 dBm as shown in Fig.3.21. Table 3-2 is summarizing the model's results.

$$\text{PAC Gain} = \frac{2\sqrt{2}\,G_m\,NT_i}{\pi\,C_s} = \frac{2\sqrt{2}*50*10^{-3}*8*125*10^{-12}}{\pi*62.5*10^{-15}} \tag{3.3}$$
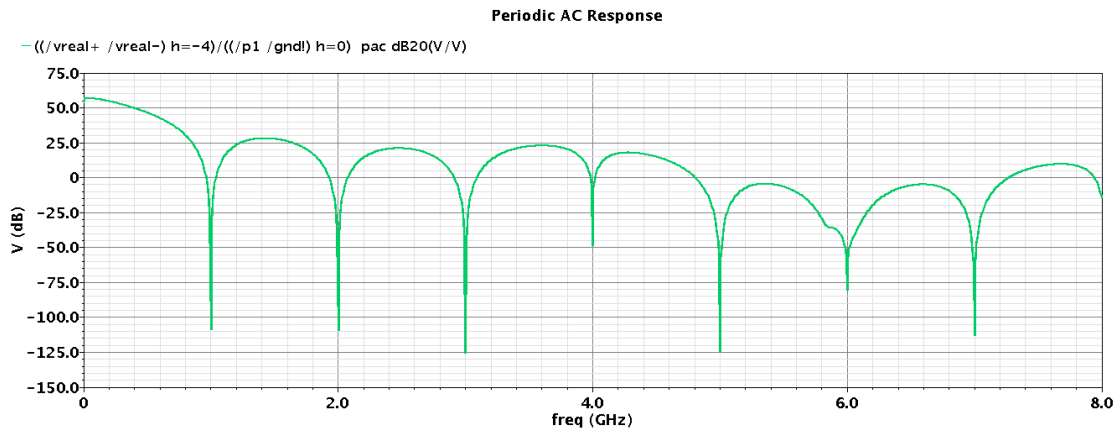
Fig. 3.17 The PAC gain at 2GHz input frequency

Periodic S-Parameter Response

Fig. 3.18 S11 at 2GHz

Periodic Noise Response
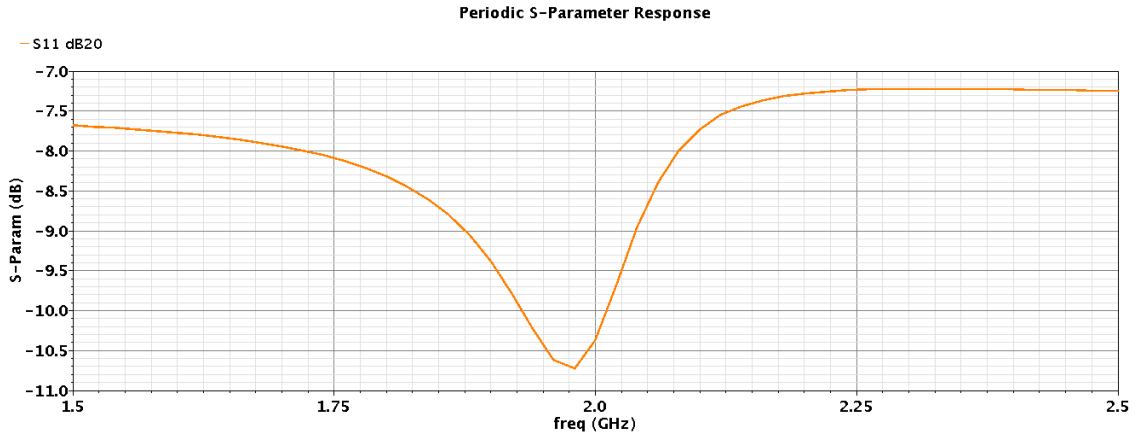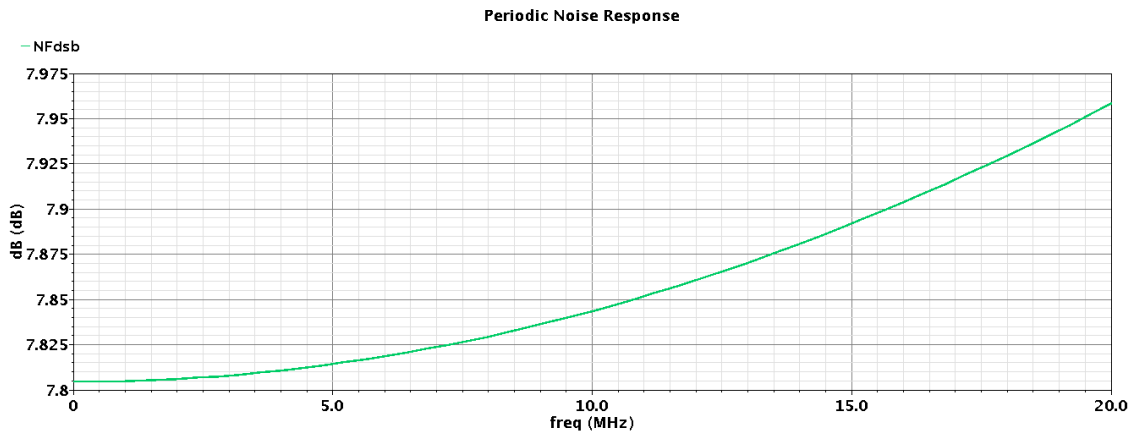
Fig. 3.19 Noise Figure at 2GHz

Quasi-Periodic AC Response
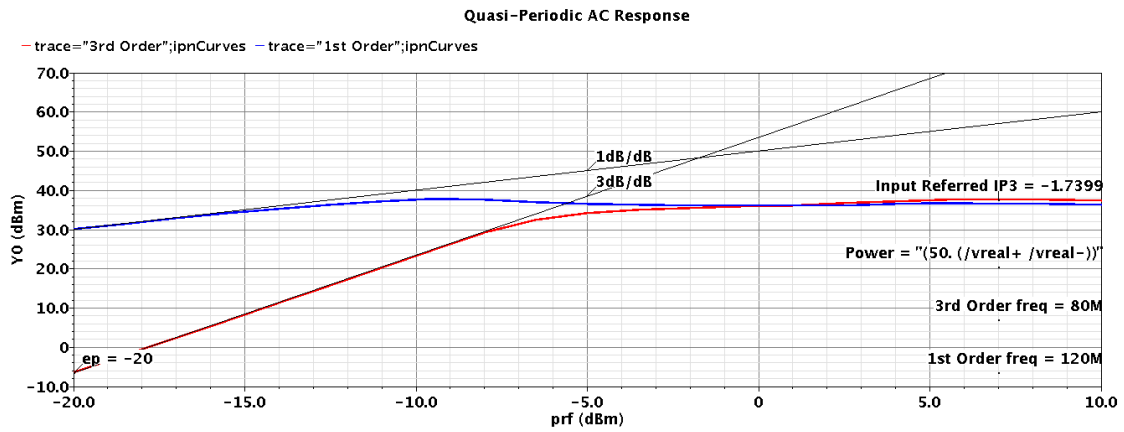
Fig. 3.20 IIp3 for inputs at 2.1GHz and 2.12GHz
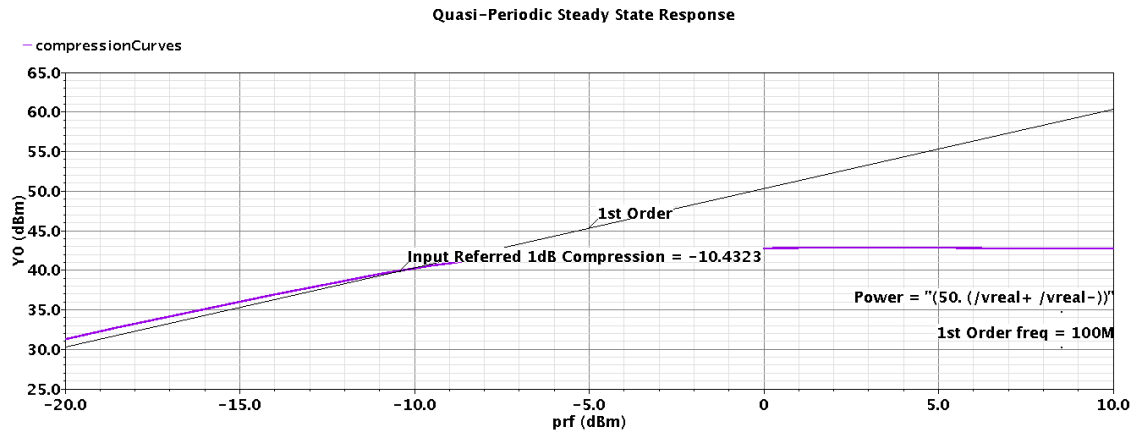
Fig. 3.21P1dB for an input of 2.1GHz frequency

specs	
Gain (dB)	57
S11 (dB)	-10
NF (dB)	7.8
IIP3 (dBm)	-1.7
P1dB (dBm)	-10.5

Table 3-2 The behavioral model results

4. Circuit implementation

4.1. The charge sampler transconductor and switches design

The transconductor is designed with low noise, high linearity, high output resistance and low output capacitance. This is to let the current pass in the integrating switches instead of being lost in the trans-conductor output impedance. Folded cascode trans-conductor shown in Fig.4.1 with its common mode feed-back (CMFB) circuit is chosen for its high linearity and high output resistance. The DC current consumption of the G_m is 7.5mA for high linearity and low noise. The input differential pair should have high gm to supply sufficient current to the integrating switches of the sampler for a proper gain to achieve low total Noise Figure and high linearity. The large devices in the design are distributed to many fingers (90 to 140) to be easily matched in the layout.
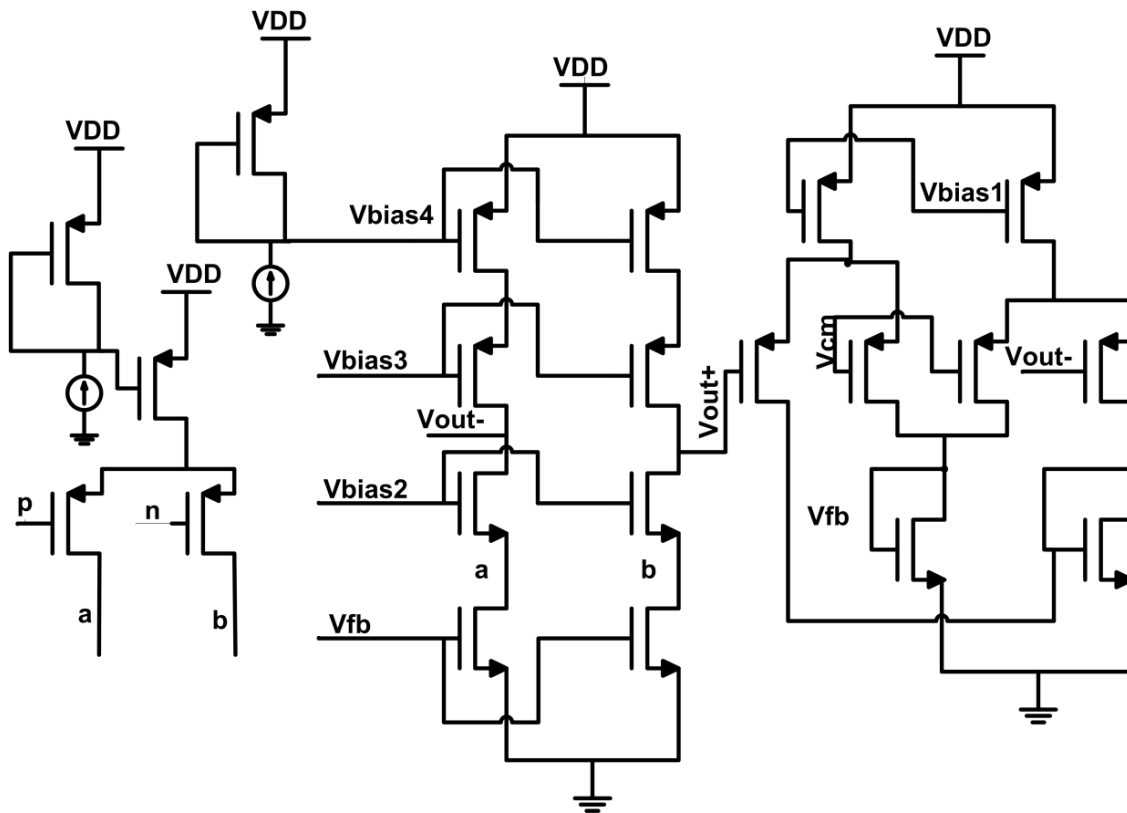
Fig. 4.1 Transconductor circuit design

The transconductor is designed with good linearity, the linearity is tested at the three targeted frequency bands. It has IIP3 of -6.4 dBm for input frequencies of 2.1GHz and 2.12GHz as shown in Fig.4.2, IIP3 of -8 dBm for input frequencies of 1.1GHz and 1.12GHz as shown in Fig.4.3 and IIP3 of -11dBm for input frequencies of 550MHz and 570MHz as shown in Fig.4.4.For P1dB , it has -18dBm for input frequency of 2.1GHz as shown in Fig.4.5 , -20dBm for input frequency of 1.1GHz as shown in Fig.4.6 and -21 dBm for 550MHz input as shown in Fig.4.7.
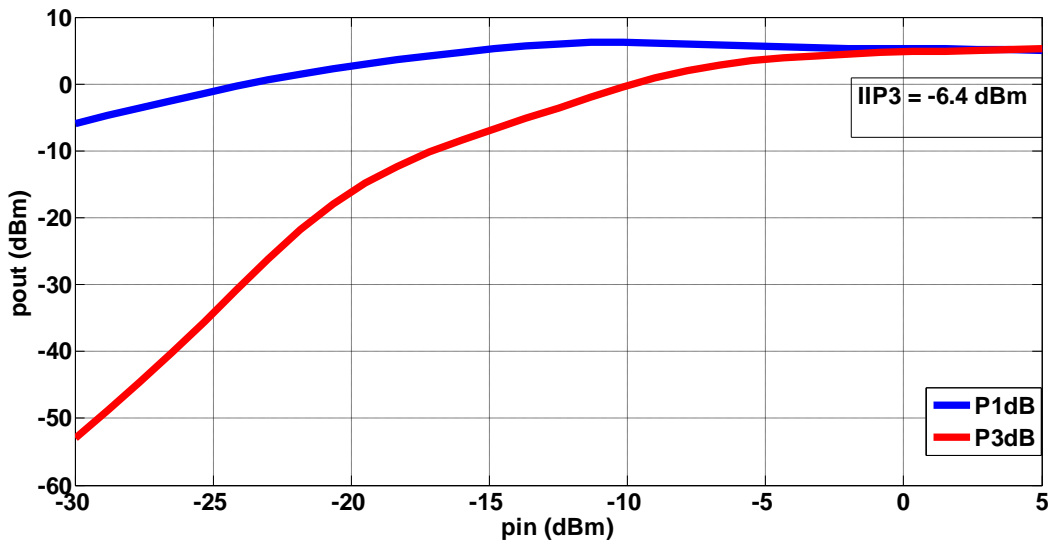
Fig. 4.2 IIP3 for two signals of 2.1GHz and 2.12GHz frequencies
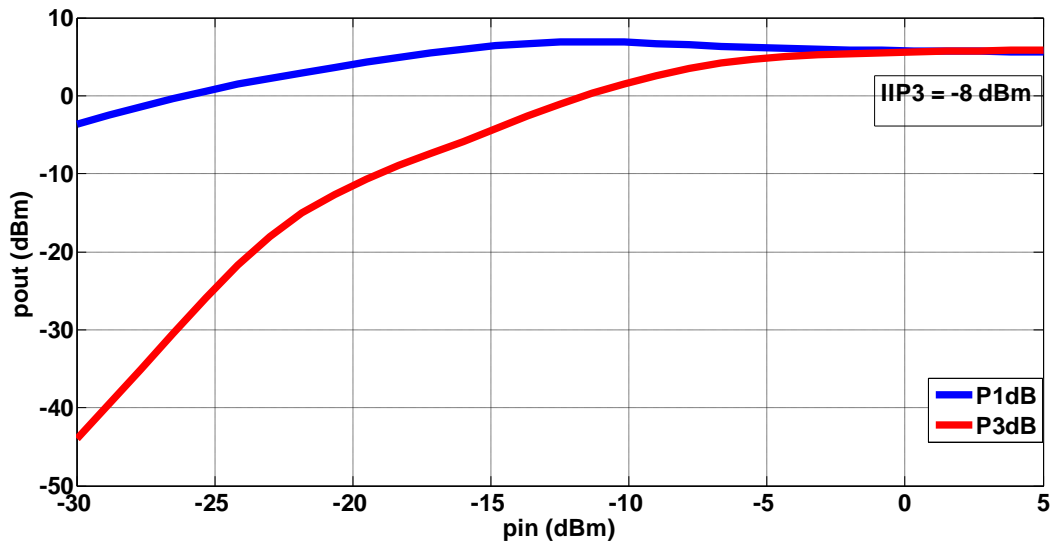
Fig. 4.3 IIP3 for two signals of 1.1GHz and 1.12GHz frequencies
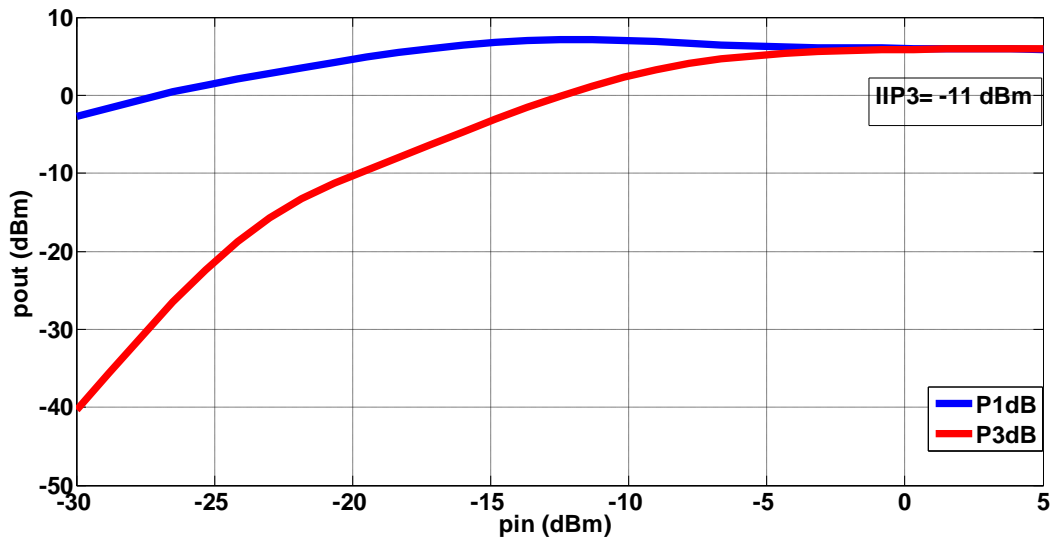
Fig. 4.4 IIP3 for two signals of 550MHz and 570MHz frequencies
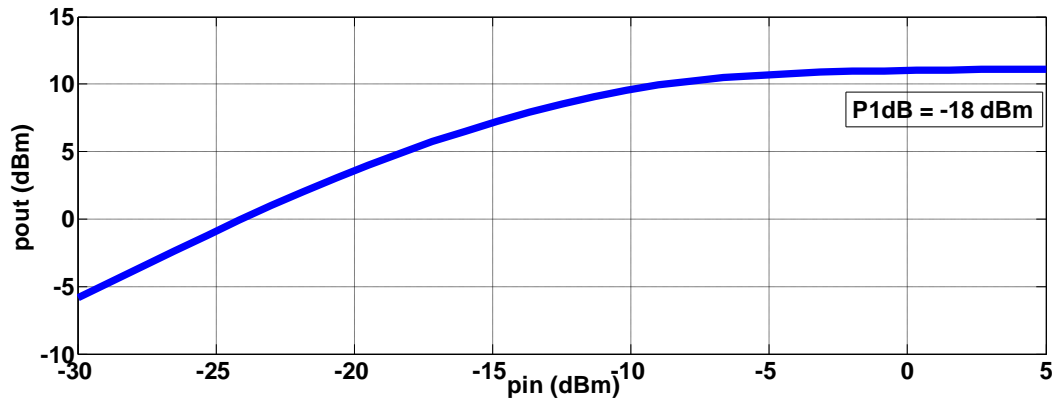
Fig. 4.5 P1dB for input frequency of 2.1GHz
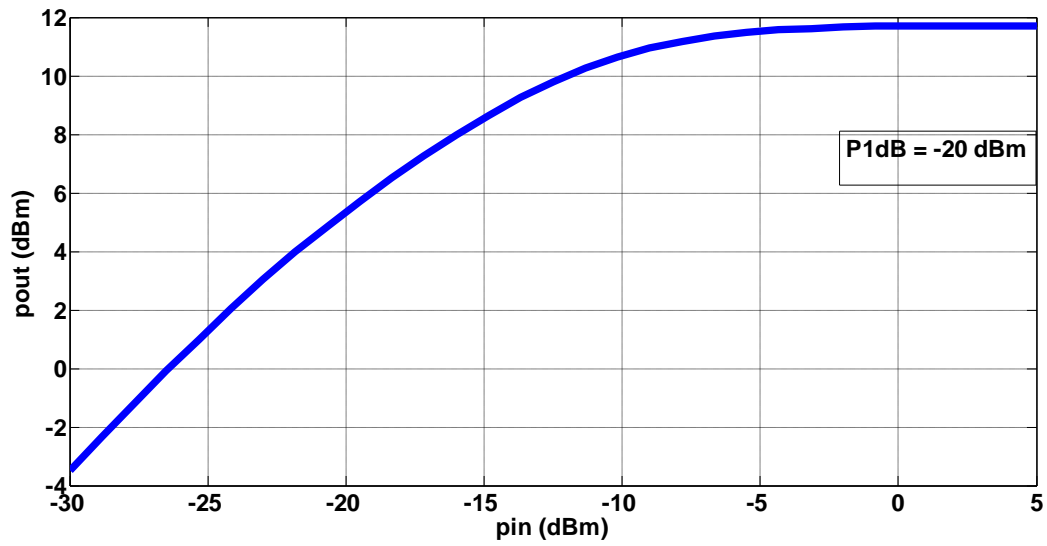
Fig. 4.6 P1dB for input frequency of 1.1GHz
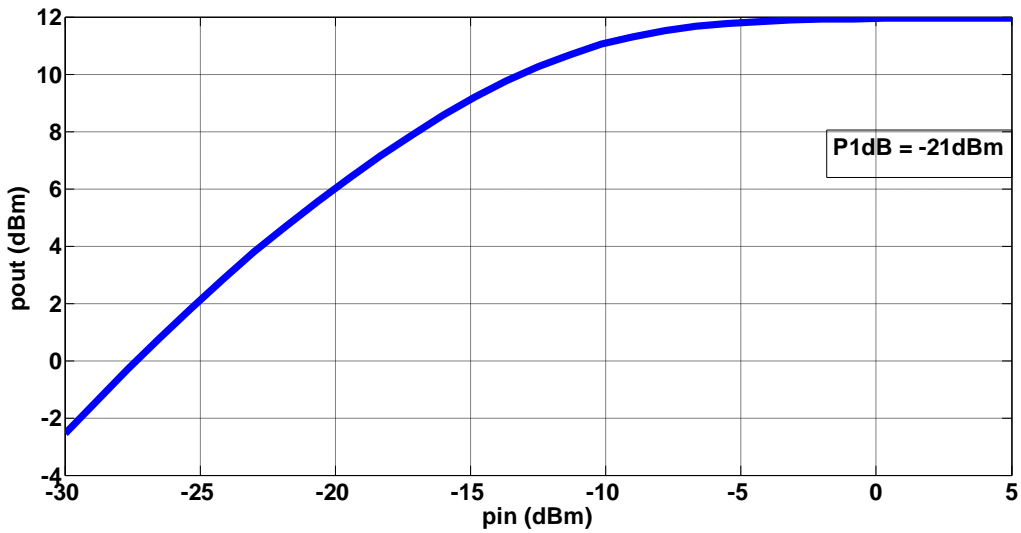
Fig. 4.7 P1dB for input frequency of 550MHz

The transconductor is designed with low noise especially at the targeted frequency range from 500MHz to 3GHz, that's why the corner frequency of it is less than 100MHz. The noise analysis of the transconductor is shown in Fig.4.8. The graph is zoomed on the targeted band (500MHz – 3GHz) in Fig.4.9. The output noise of the transconductor at 2GHz is 294 aV^2/Hz, 484 aV^2/Hz at 1GHz and 585 aV^2/Hz at 500MHz.
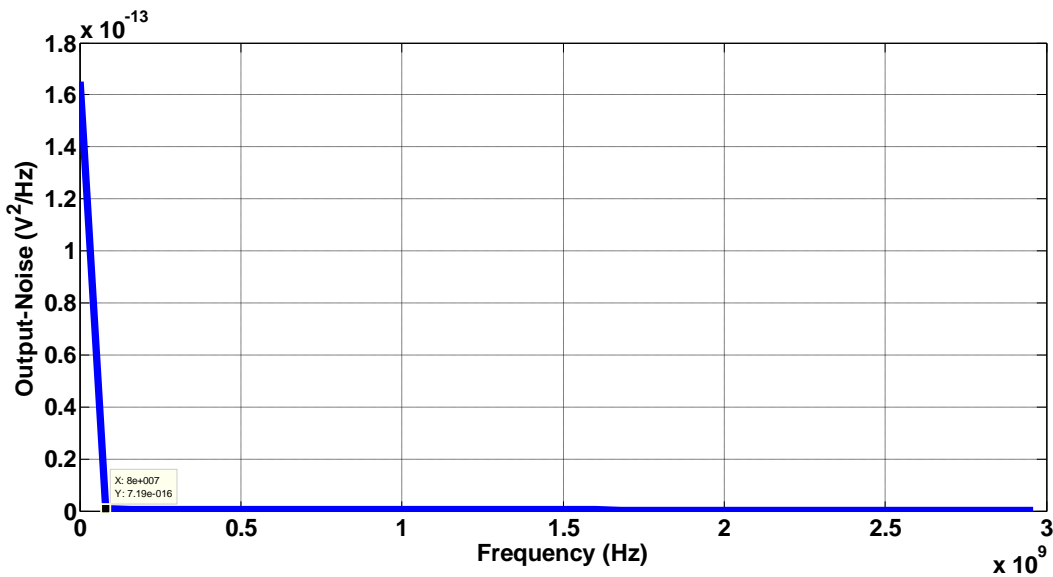
Fig. 4.8 The transconductor output-noise versus frequency
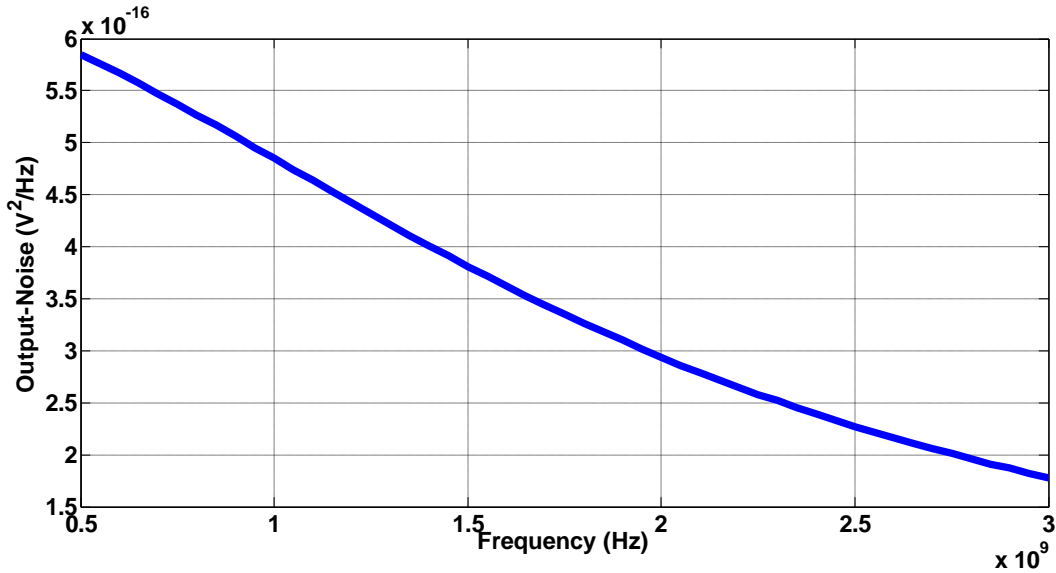
Fig. 4.9 The transconductor output noise zooming on (500MHz – 3GHz)

The sampler's switches are I/O devices for its better linearity and low on resistance, this is to allow most of the current to pass in the switches. The sizes of the switches are chosen so that they have low on resistance and low drain and source capacitance.

At low frequencies, the current is distributed between the trans-conductor output resistance and the integrating switch resistance [29]. At moderate frequencies, the current distribution is based on the combination of the transconductor output resistances/capacitances and the switch resistance/capacitance series with the sampling capacitance. At high frequencies, most of the current is passing in the integrating switch path, as long as the sampling capacitance is much higher than the trans-conductor output capacitance. The trans-conductor output resistance and capacitance (the sizes of the devices at the output node), the switch on resistance and capacitance (the sizes of the switches) and the sampling capacitance are chosen so that the AC current passing in the switches integrated on the sampling capacitance is high enough sufficient for the desired gain on the frequency range from 500MHz to 3GHz based on the required noise figure and linearity specs. It is obvious that the sampling capacitance determines the amount of current passing in the integrating switch and at the same time the gain equation is function of it, so its value will be chosen based on a tradeoff between both. The AC

current passing in the switches and integrated on the sampling capacitors is shown in Fig.4.10.
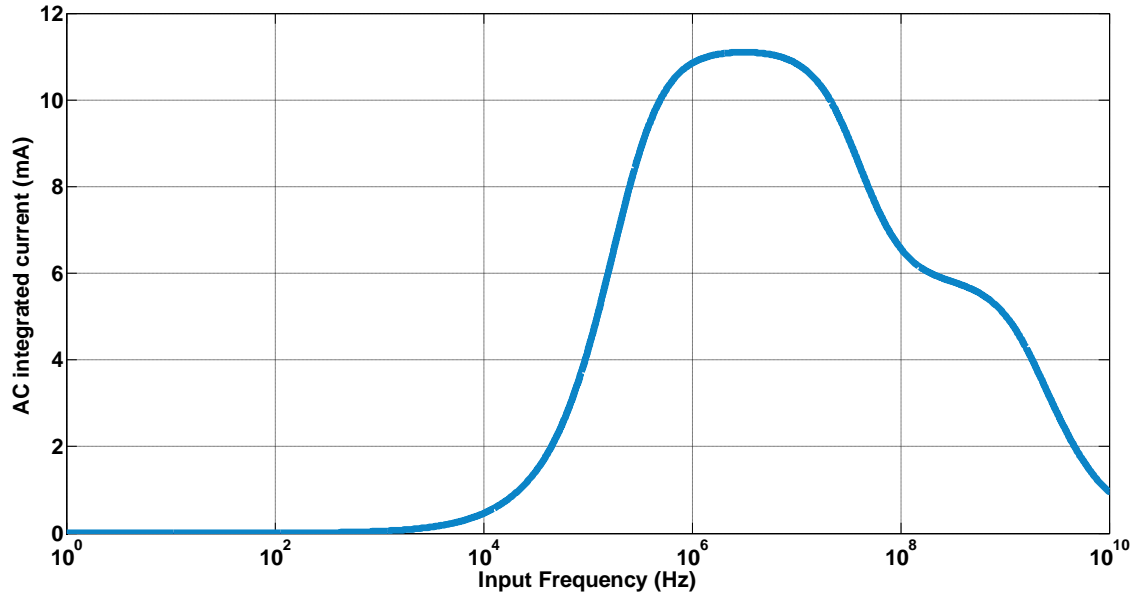
Fig. 4.10 The AC integrated current

4.2. Time varying matching network

The matching network with the amplifiers is shown in Fig.4.11. The switches widths are chosen large enough to decrease the switch resistance (R_{sw}), this is to make the impedance matching controlled by adjusting the base-band resistance. The base-band resistance is represented by the resistance R_b divided by the amplifier gain (A). The sizes of the switches, the base-band resistances and the amplifier gain are chosen based on trade-off between the matching (S11) and the noise figure (NF). The base-band resistance should be adjusted to be within the value of power matching and Noise Figure matching.
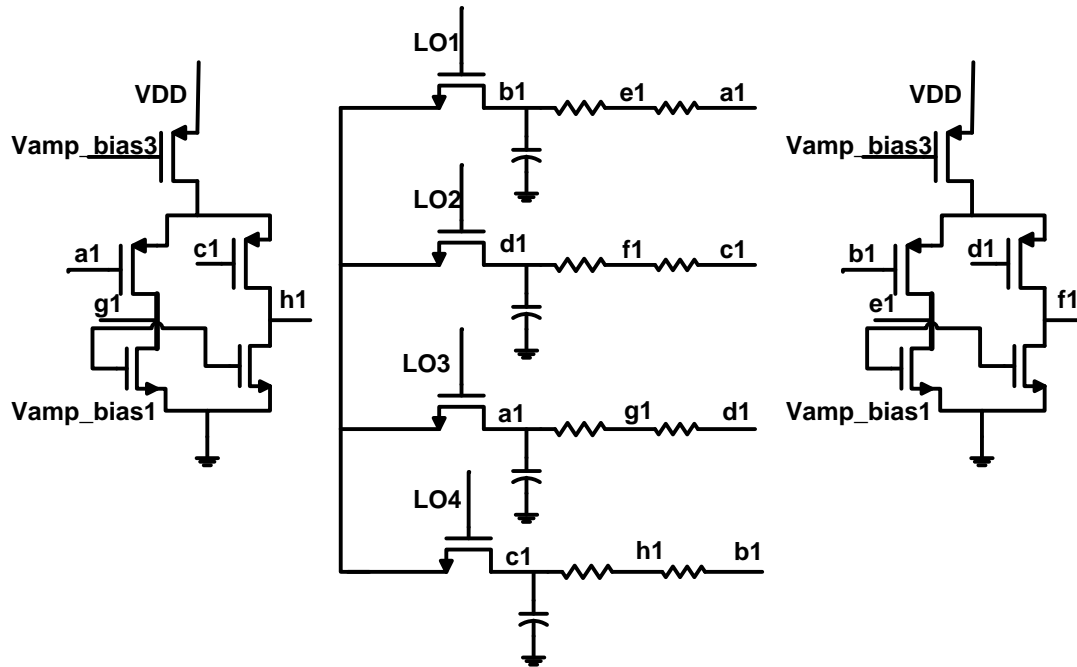
Fig. 4.11 The schematic of the matching network and its amplifiers

4.3. The digital circuitry generating the charge sampler's controlling clocks

The controlling clocks shown in Fig 3.13a & b reveals the need for four non-overlapping clocks delayed with T_f with respect to each other to control one channel integration switches. Each clock has two successive pulses of width equal to the integration time (T_i) with time difference of $3T_i$ in between in one half of the sampling period, then zero in the other half. While another two clocks each of one pulse of width equal to T_i for the output sampling and discharging phases are on at this time. The circuit is tested at 1GHz frequency standard which means *clk* and *clk_bar* are 2GHz frequency as shown in Fig 4.13.

The circuit includes a divider with two successive differential flip flops, one controlled by *clk* and the other is controlled by *clk_bar* .The output of the second flip flop is fed back to the input of the first flip-flop as shown in Fig.4.12 to generate 4 90° phase-shifted 50% duty-cycle clocks (*Q1, Q1_bar, Q2 and Q2_bar*) of half the *clk* frequency shown in Fig.4.14.The in-phase clocks (*Q1&Q1_bar*) clocks are ANDed with *clk_bar*

and the quadrature clock cycles (*Q2 & Q2_bar*) are ANDed with *clk* resulting in 4 90° phase-shifted 25% duty cycle clocks (*out1,out2, out3 & out4*) shown in Fig.4.15. *Q1 & Q1_bar* are the controlling clocks of the successive differential divider generating 4 90° phase-shifted 50% duty-cycle clocks(*Q3, Q3_bar,Q4 and Q4_bar*) shown in Fig.4.16 of half the controlling clock *Q1*frequency. The quadrature clocks (*Q4 & Q4_bar*) are the controlling clocks of the following divider generating 4 90° phase-shifted 50% duty-cycle clocks(*Q7, Q7_bar,Q8 and Q8_bar*) shown in Fig.4.17 of half the controlling clock *Q4* frequency. The frequency of the clocks *Q8 and Q8_bar* is equal to the sampling frequency, so by ANDing each of them with each clock of (*out1, out2, out3 & out4*), the required integration pulses of the first channel (*imagn, realn, imagp* and *realp*) and that of the second channel (*imagn_interleaved, realn_interleaved, imagp_interleaved* and *realp_interleaved*) can be obtained as shown in Fig.4.18& 4.19.

For the first channel; the output sampling clock is generated by ANDing the clock *realn_interleaved* with *Q3* whereas, the discharging clock is generated by ANDing *realn_interleaved* with *Q3_bar*. Fig.4.20 is showing the sampling-to-output and discharging pulses of the first channel.

For the second channel; the sampling-to-output clock is generated by ANDing *realn* with *Q3* and whereas, the discharging clock is generated by ANDing *realn* with *Q3_bar*. Fig.4.21 is showing the sampling-to-output and discharging pulses of the second channel.

Buffers of cascaded inverters are added between different blocks to buffer the output of each, as the output of each block will be loaded by the capacitance of the following block. The addition of buffers with minimum sizes makes each block see small load capacitance which doesn't affect the performance. The block diagram generating the integration, sampling-to-output and discharging clocks is shown in Fig.4.22.
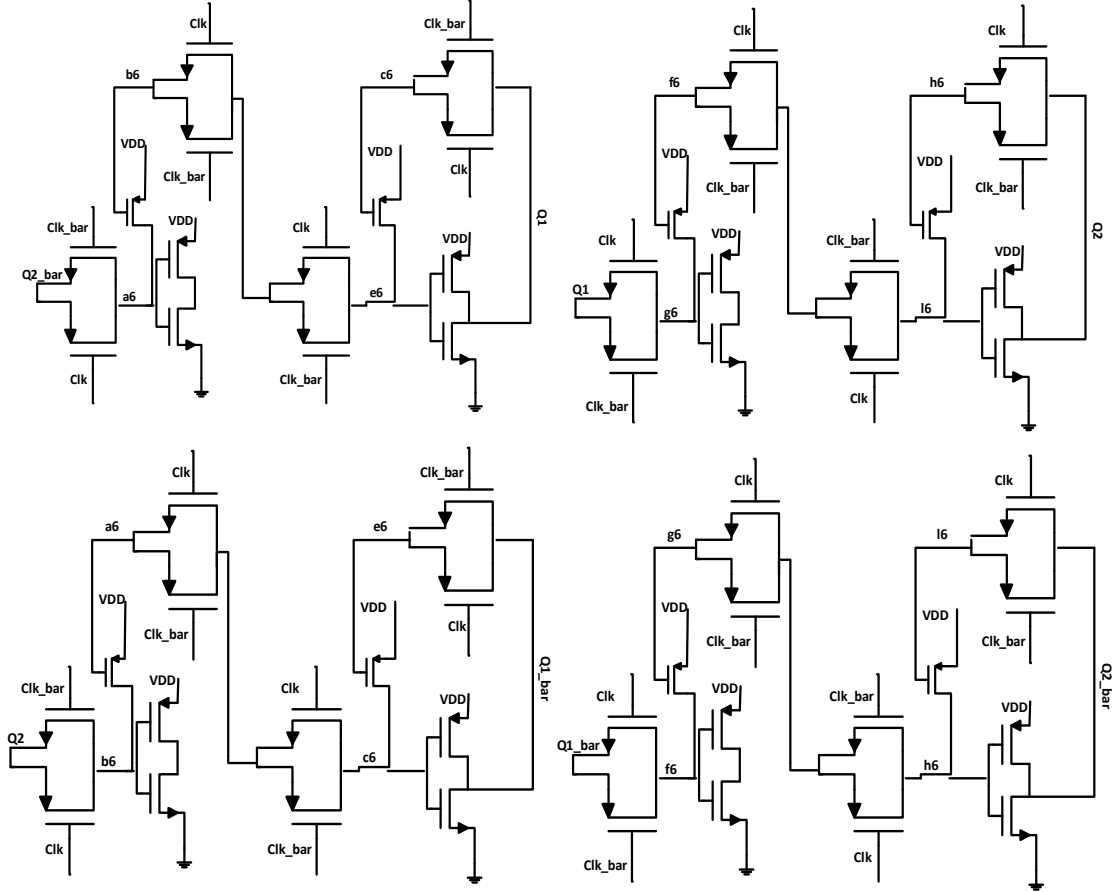
Fig. 4.12 The divider with 2 successive flip-flops feed-backed to each other
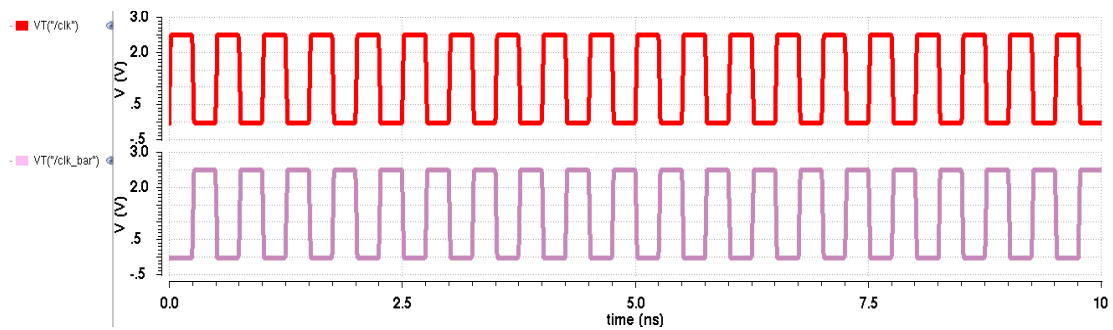
Fig. 4.13 clk and clk_bar
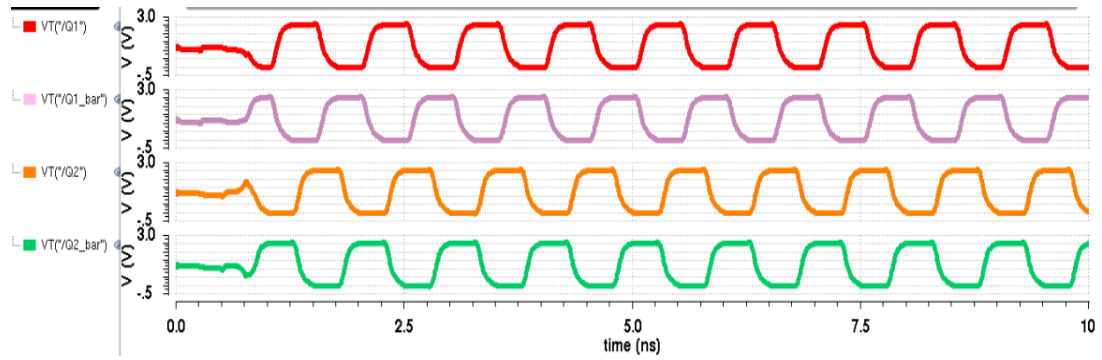
Fig. 4.14Quadrature 50% duty cycle Q1,Q2,Q1_bar and Q2_bar
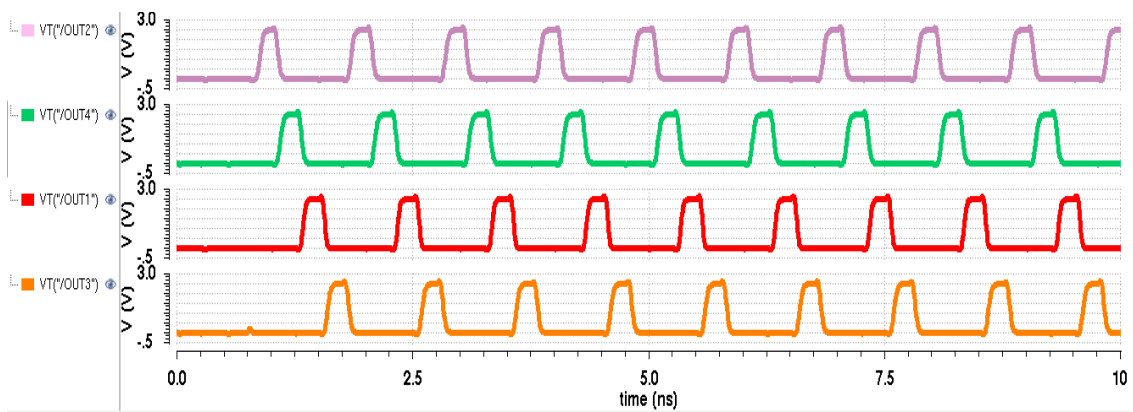
Fig. 4.15Non-overlapping 25% duty-cycle clocks out1,out2,out3 and out4
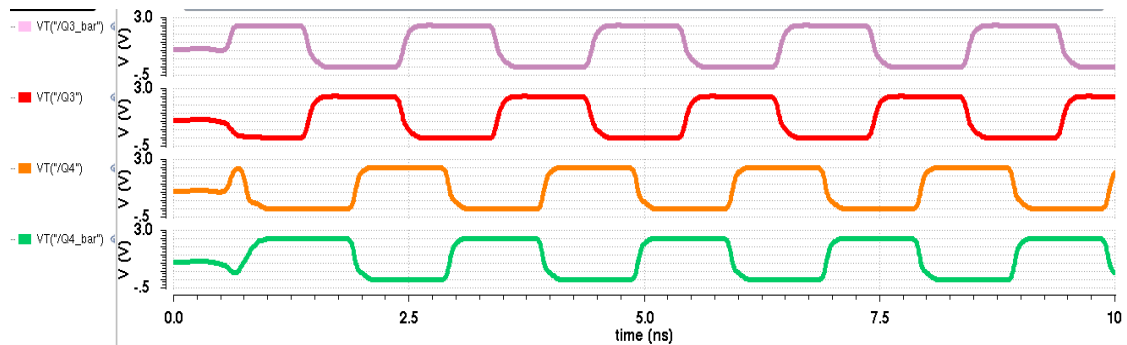
Fig. 4.16Qudrature 50% duty-cycle Q3,Q3_bar,Q4 and Q4_bar
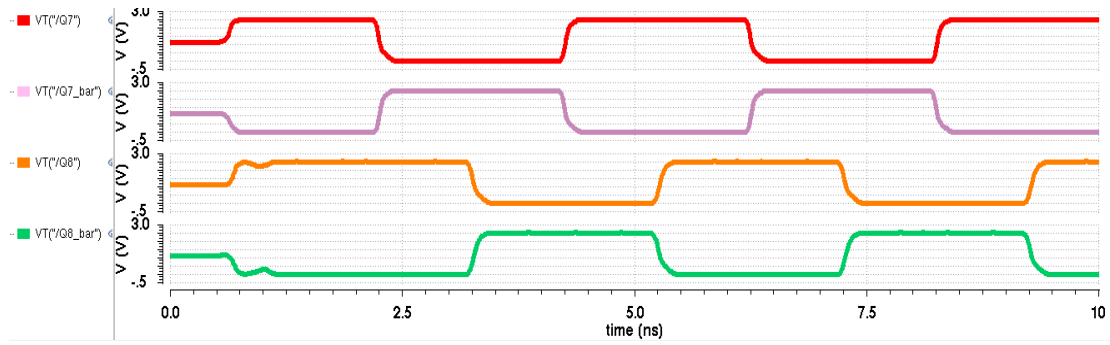
Fig. 4.17Quadrature 50% duty-cycle clocks Q7,Q7_bar,Q8 and Q8_bar
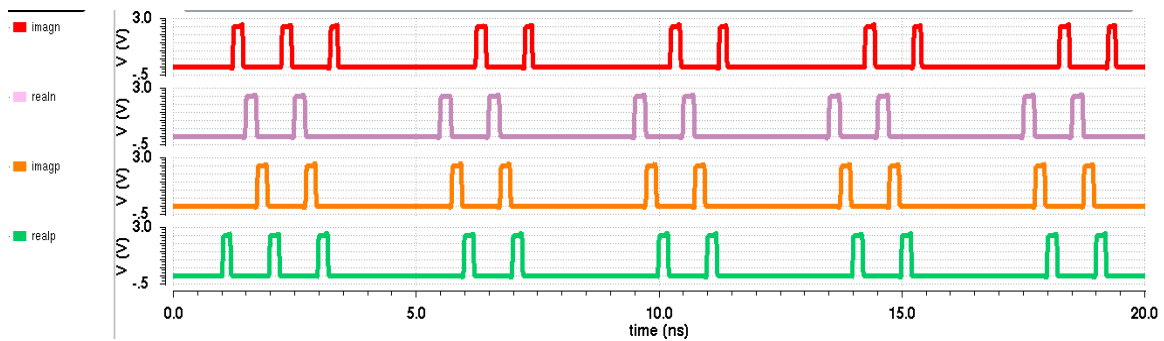
Fig. 4.18The integration pulses of the first channel
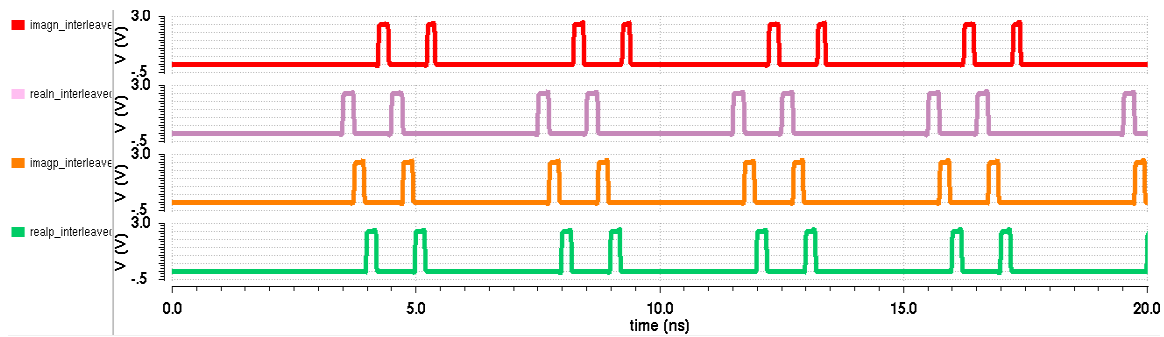
Fig. 4.19The integration pulses of the second channel
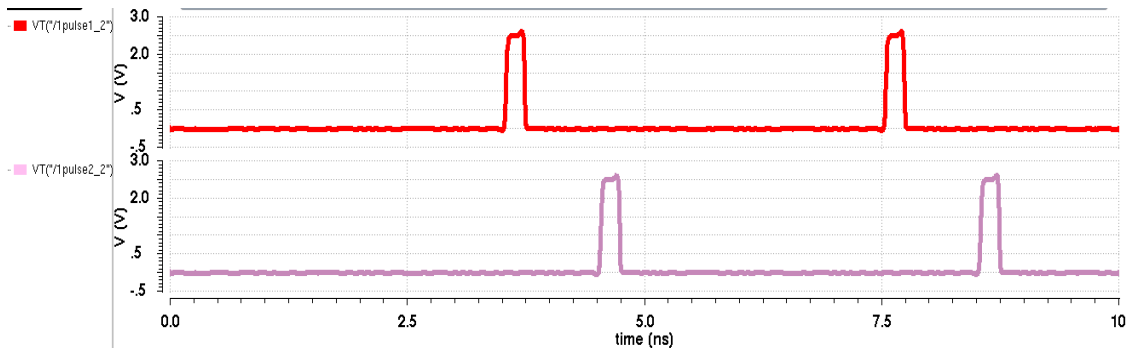
Fig. 4.20The sampling-to-output and discharging clocks of the first channel
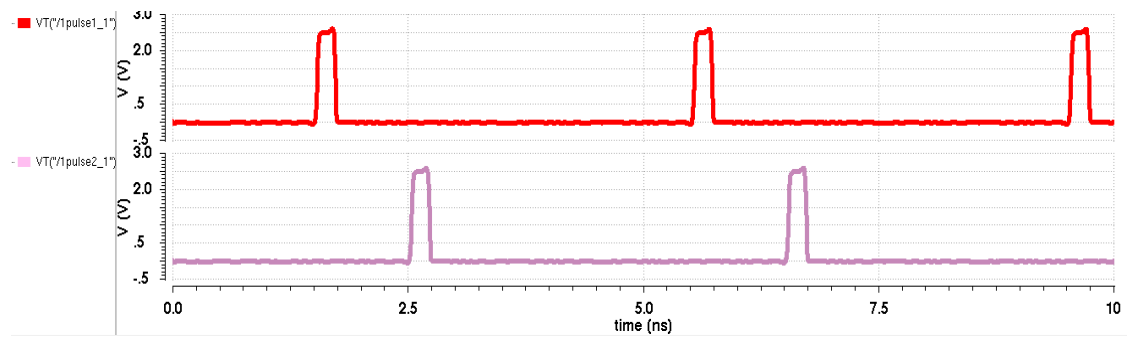
Fig. 4.21The sampling-to-output and discharging clocks of the second channel
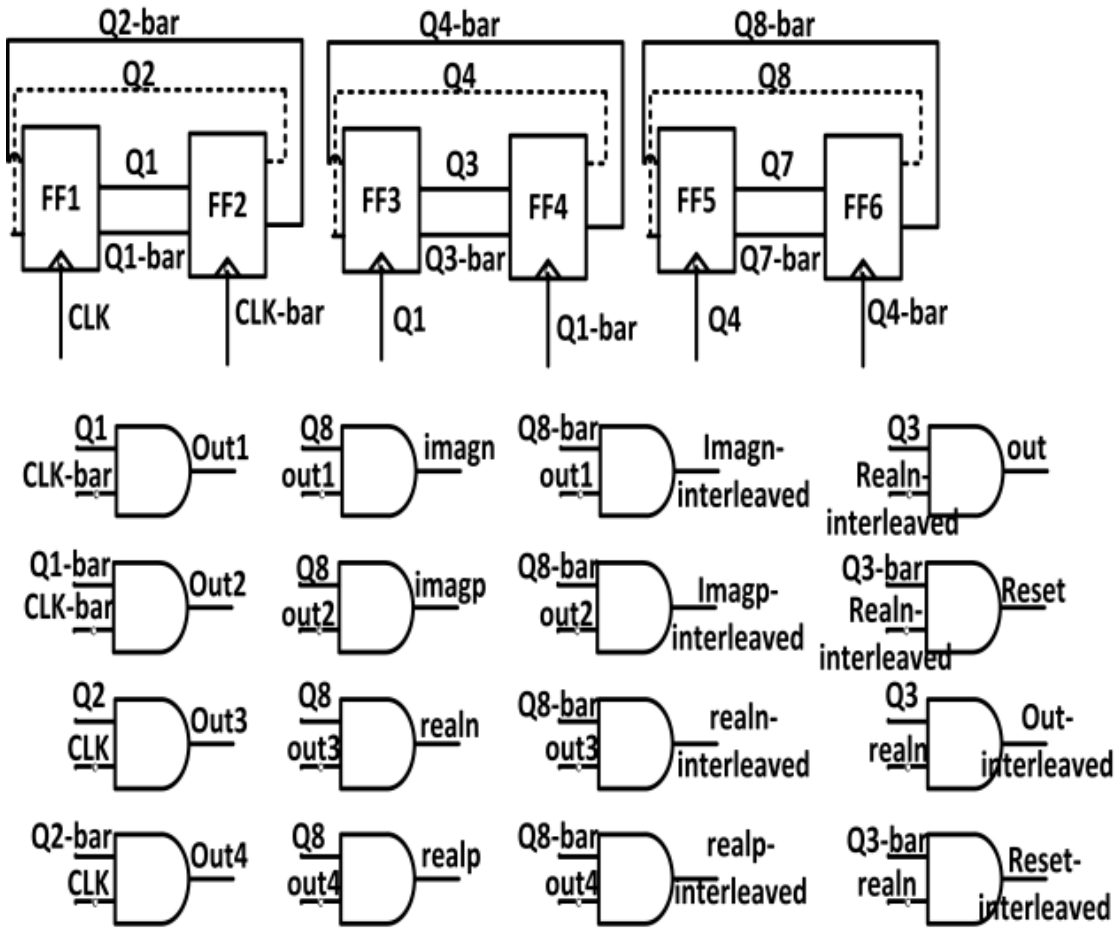
Fig. 4.22The block diagram of the digital circuitry generating the integration clocks of one channel

4.4. The digital circuitry generating the MN controlling clocks

The matching network needs four non-overlapping 25% duty cycle clocks with LO frequency. The circuit includes a divider with two successive differential flip flops, one controlled by *clk_MN* and the other is controlled by *clk_bar_MN* .The output of the second one is fed back to the input of the first flip-flop as shown in fig.4.12 to generate 4 90° phase-shifted 50% duty-cycle clocks (*Q1_MN, Q1_bar_MN,Q2_MN and Q2_bar_MN*) of half the *clk_MN* frequency shown in Fig.4.23. The controlling clocks here are of 2GHz frequency, as the *clk_MN* frequency is double the Local oscillator (LO) frequency. The in-phase clocks (*Q1_MN& Q1_bar_MN*) clocks are ANDed with the controlling *clk_bar_MN* and the quadrature clock cycles (*Q2_MN & Q2_bar_MN*) are ANDed with *clk_MN* resulting in 4 90° phase-shifted 25% duty cycle clocks (*oLO1, LO2, LO3 and LO4*) shown in Fig.4.24. The block diagram of the digital circuit is shown in Fig.4.25.
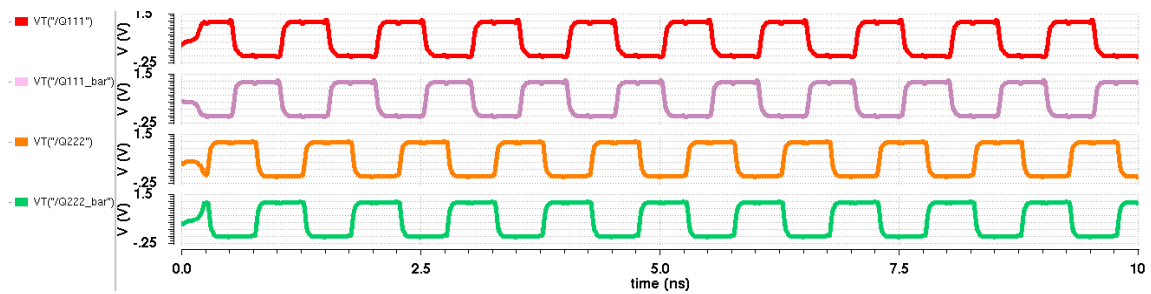
Fig. 4.23 The quadrature 50% duty-cycle (Q1_MN,Q1_bar_MN,Q2_MN and Q2_bar_MN
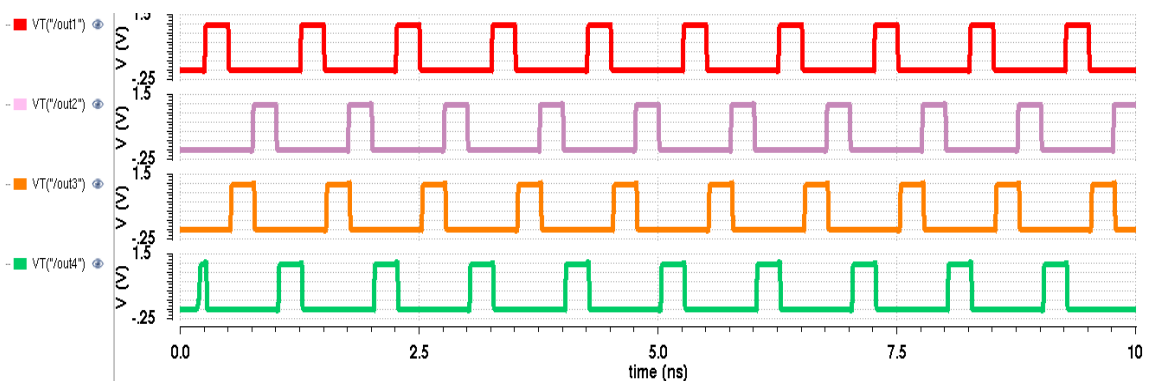
Fig. 4.24 Non-overlapping 25% duty-cycle clocks (out1_MN,out2_MN,out3_MN and out4_MN
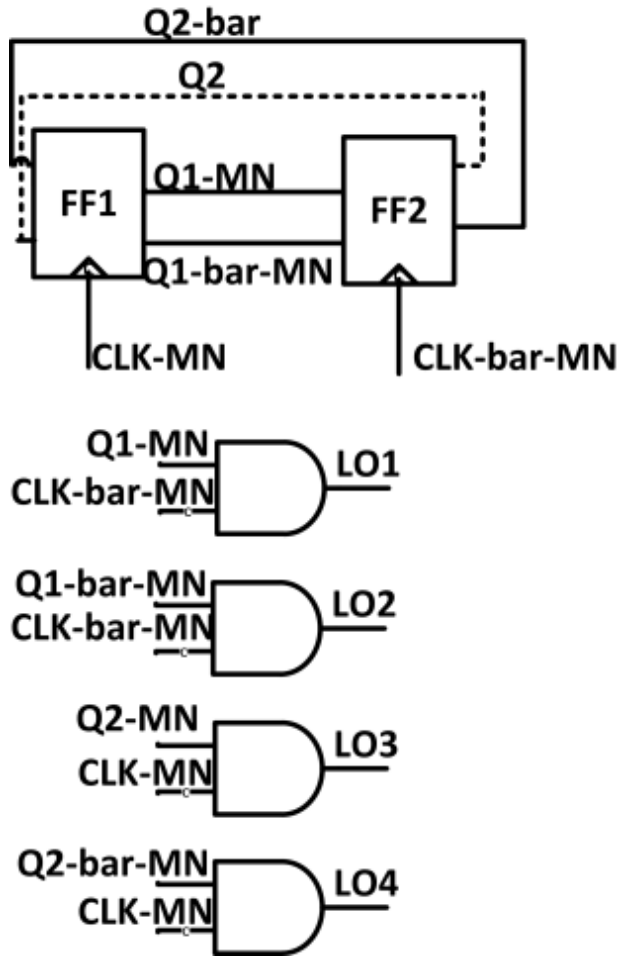
Fig. 4.25The digital circuitry generating the MN controlling clocks

5. Pre layout simulation results of the proposed architecture

The architecture is tested over three different frequencies (500MHz, 1GHz and 2GHz) to prove its programmability and capability of achieving the required specs of linearity, noise figure, gain and matching of the targeted standards on different frequency bands.

5.1. Noise Figure results

Noise Figure has a bell shape, NF is high at low frequencies due to flicker noise which is dominated by the transconductor (Gm) noise then NF decreases due to thermal noise of the charge sampler added to that of the matching network, finally NF increases again at high frequencies due to the increase of the parasitcs effect at these frequencies. We are interested in the middle region as the targeted IF frequency is 10MHz.

Targeting LTE standard as a case study; the required noise figure is 9dB as shown in chapter2 which implies that the noise figure at all frequencies should be less than or equal 9dB.

5.1.1. Noise Figure at 2GHz

Fig.5.1 is showing the noise figure of the architecture versus the output frequency (1MHz to 100MHz) for input frequencies from 2.001GHz to 2.1GHz. NF @ 10MHz (the targeted IF frequency) is 7.8 dB.

Fig. 5.1 Noise Figure at input frequencies (2.001GHz – 2.1GHz)

5.1.2. Noise Figure at 1GHz

Fig.5.2 is showing the noise figure of the architecture versus the output frequency (1MHz to 100MHz) for input frequencies from 1.001GHz to 1.1GHz. NF @ 10MHz (the targeted IF frequency) is 7.9 dB.
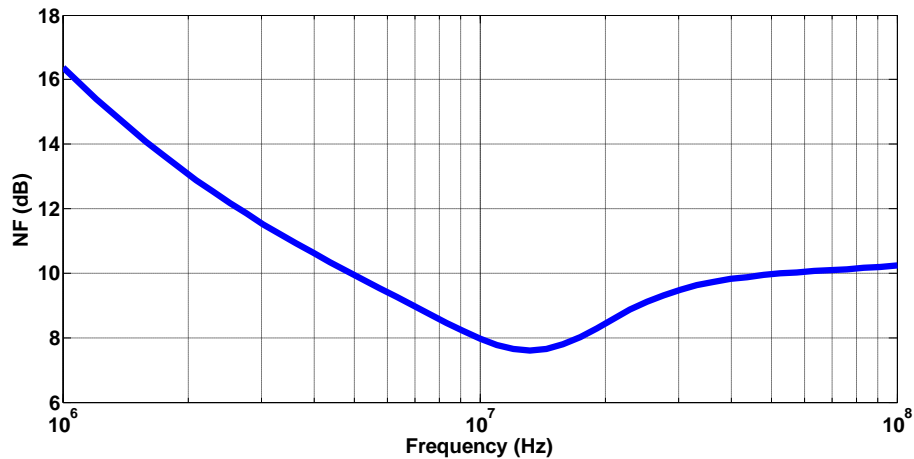
Fig. 5.2Noise Figure at input frequencies (1.001GHz – 1.1GHz)

5.1.3. Noise Figure at 500MHz

Fig.5.3 is showing the noise figure of the architecture versus the output frequency (1MHz to 100MHz) for input frequencies from 501MHz to 600MHz. NF @ 10MHz (the targeted IF frequency) is 9 dB.
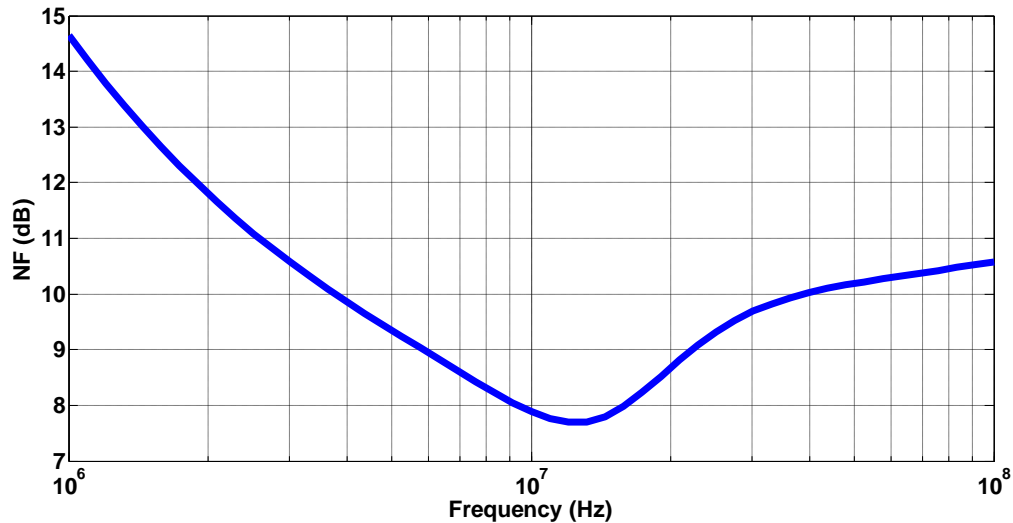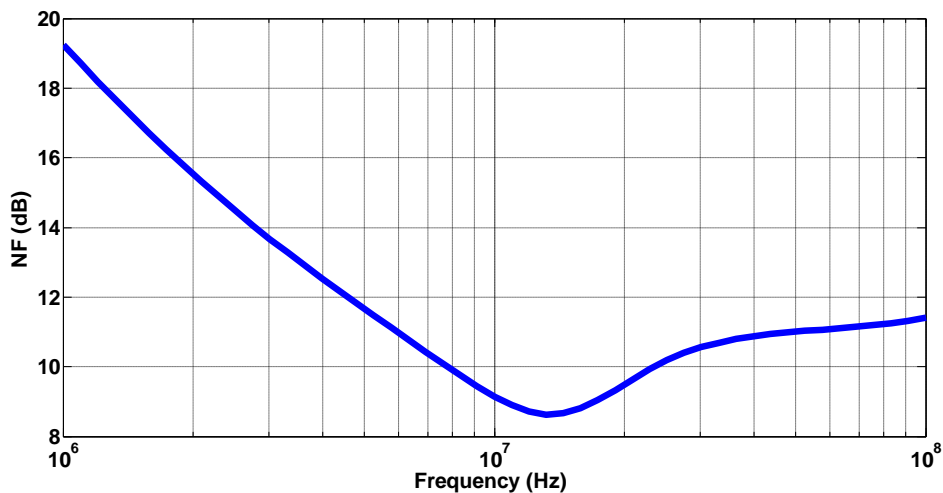

Fig. 5.3Noise Figure at input frequencies (501MHz – 600MHz)

5.2.Linearity results

The linearity of any block is represented by P1dB and IIP3; the design should provide good linearity indicated by the values of P1dB and IIP3 at different frequencies.

The linearity is mainly dominated by the charge sampler especially the trans-conductor should provide high linearity and it's enhanced by the time varying matching network due to its further selectivity.

Linearity can be out of band linearity and in band linearity; out of band linearity is when the blocker signals are outside the desired band to be received (> 20MHz) and in band linearity is when the blocker signals are within the desired band (< 20MHz).

5.2.1.   Out- of-band P1dB and IIP3 for 2GHz frequency band

Out-of-band P1dB of the architecture is -12 dBm for input blocker of frequency 2.1GHz as shown in Fig.5.4.

Fig. 5.4 Out-of-band P1dB for input signal of 2.1GHz

Out-of-band IIP3 is tested for two input signals of frequencies of 2.1GHz and 2.12GHz giving third order intermodulation component at 80MHz resulting in out-of-band IIP3 of -1.9 dBm as shown in Fig.5.5.

Fig. 5.5Out of band IIp3 for input signals with frequencies of 2.1GHz and 2.12GHz

5.2.2. Out- of-band P1dB and IIP3 for 1GHz frequency band

Out-of-band P1dB of the architecture is -14 dBm for input blocker of frequency 1.1GHz as shown in Fig.5.6.

Fig. 5.6 Out-of-band P1dB for input signal with frequency 1.1GHz

Out of band IIP3 is tested for two input signals of frequencies of 1.1GHz and 1.12GHz giving third order intermodulation component at 80MHz resulting in out-of-band IIP3 of -3 dBm as shown in Fig.5.7.

Fig. 5.7Out-of-band IIP3 for input signals with frequencies 1.1GHz and 1.12GHz

5.2.3. Out- of-band P1dB and IIP3 for 500MHz frequency band

Out-of-band P1dB of the architecture is -16 dBm for input blocker of frequency 550MHz as shown in Fig.5.8.

Fig. 5.8Out-of-band P1dB for input signal with frequency 500MHz

Out-of-band IIP3 is tested for two input signals of frequencies of 550MHz and 570MHz giving third order intermodulation component at 30MHz resulting in out-of-band IIP3 of -5.652 dBm as shown in Fig.5.9

Fig. 5.9 Out-of-band IIP3 for input signals with frequencies of 550MHz and 570MHz

5.2.4. In-band P1dB and IIP3 for 2GHz frequency band

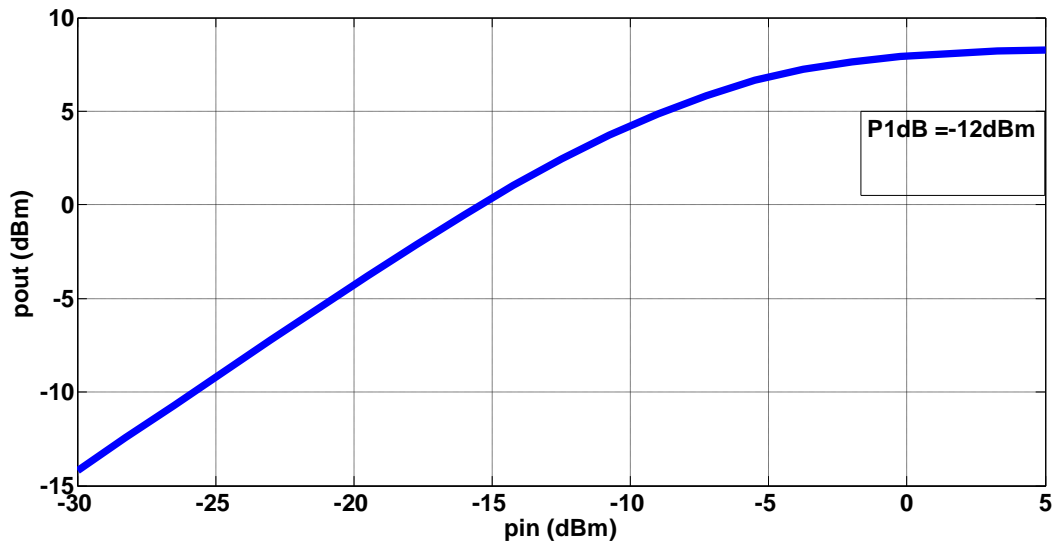In-band P1dB of the architecture is -13.5 dBm for input blocker of frequency 2.001GHz as shown in Fig.5.10.

Fig. 5.10 In-band P1dB for input signal of frequency 2.001GHz

In-band IIP3 is tested for two input signals of frequencies of 2.001GHz and 2.003GHz giving third order intermodulation component at 5MHz resulting in in-band IIP3 of -1.45 dBm as shown in Fig.5.11.
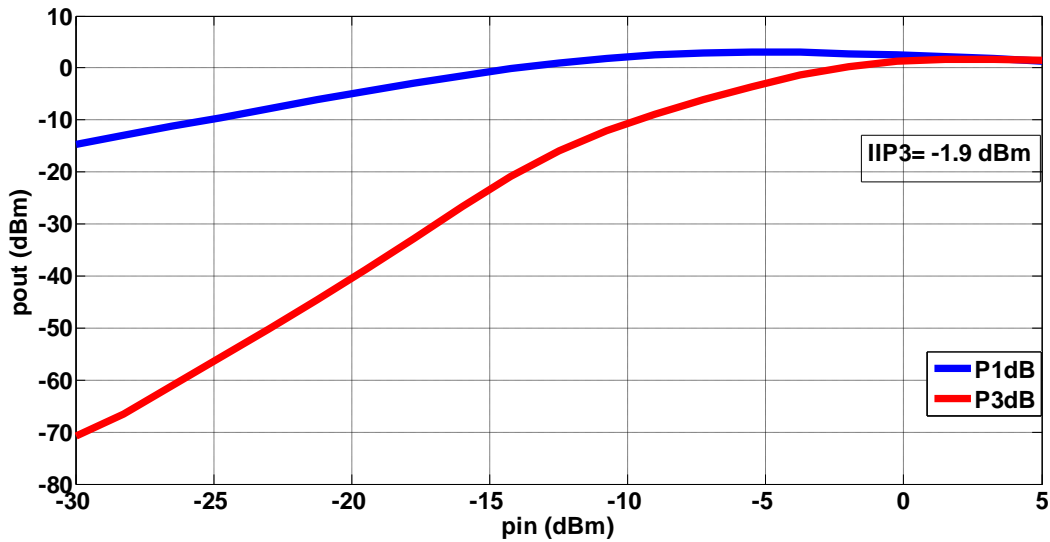
Fig. 5.11 In-band IIP3 for input signals with frequencies of 2.001GHz and 2.003GHz

5.2.5. In-band P1dB and IIP3 for 1GHz frequency band

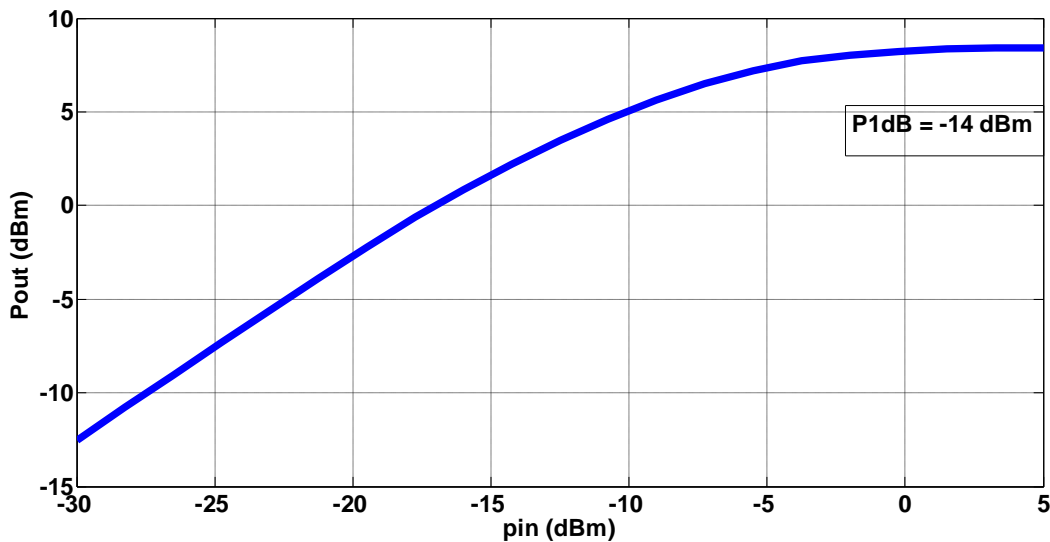In-band P1dB of the architecture is -16.5 dBm for input blocker of frequency 1.001GHz as shown in Fig.5.12.

Fig. 5.12In-band P1dB for input signal of frequency 1.001GHz

In-band IIP3 is tested for two input signals of frequencies of 1.001GHz and 1.003GHz giving third order intermodulation component at 5MHz resulting in in-band IIP3 of -4.3497 dBm as shown in Fig.5.13.
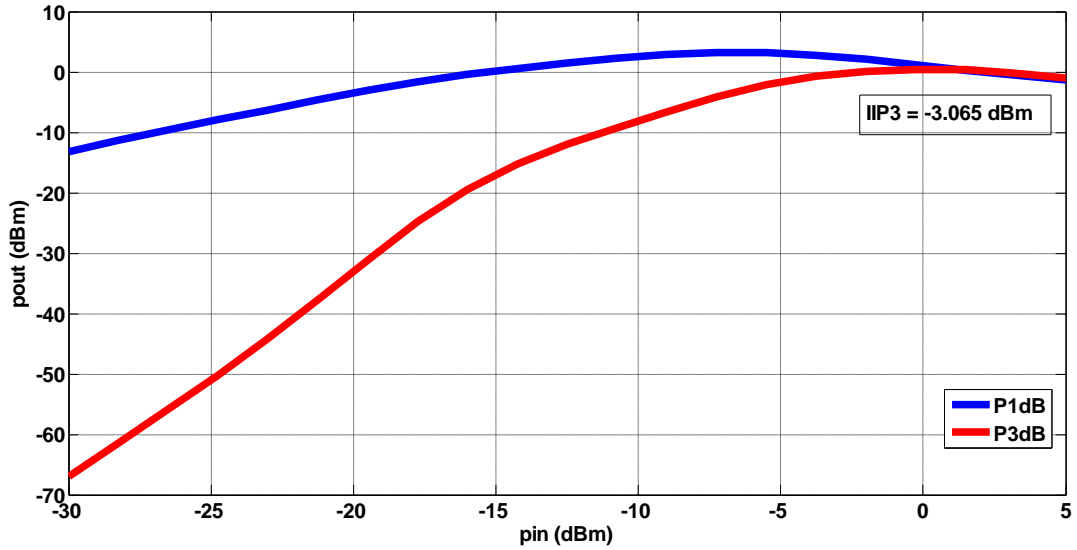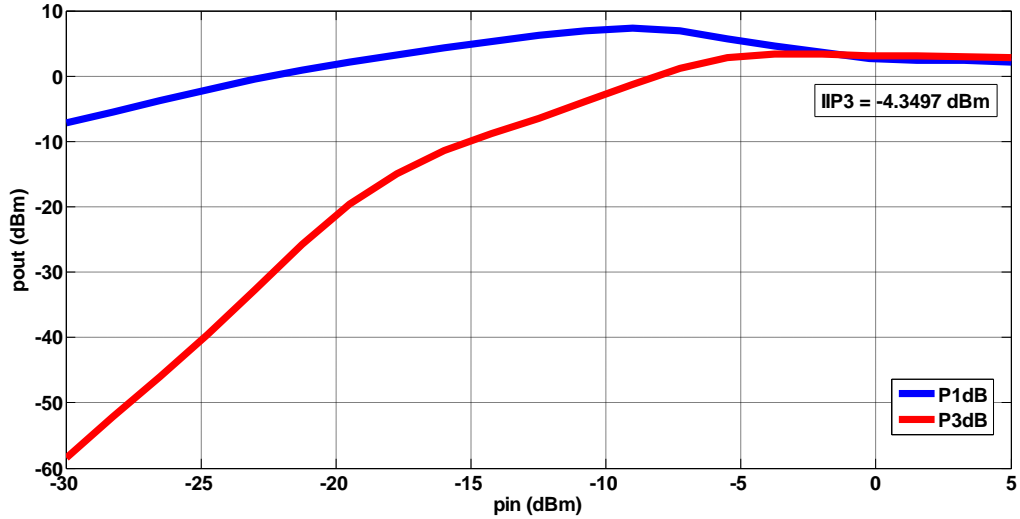

Fig. 5.13 In-band IIP3 for input signals with frequencies of 1.001GHz and 1.003GHz

5.2.6. In-band P1dB and IIP3 for 500MHz frequency band

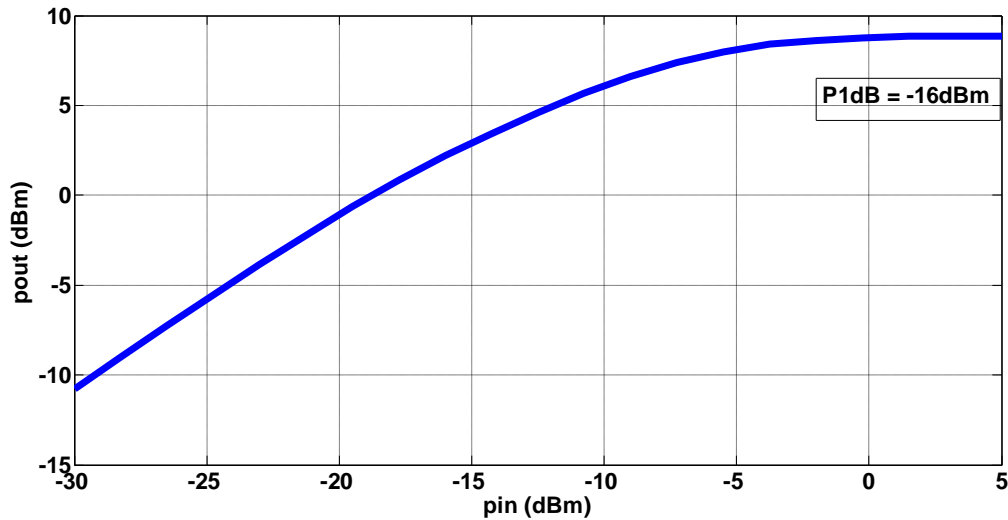In-band P1dB of the architecture is -18 dBm for input blocker of frequency 501MHz as shown in Fig.5.14.
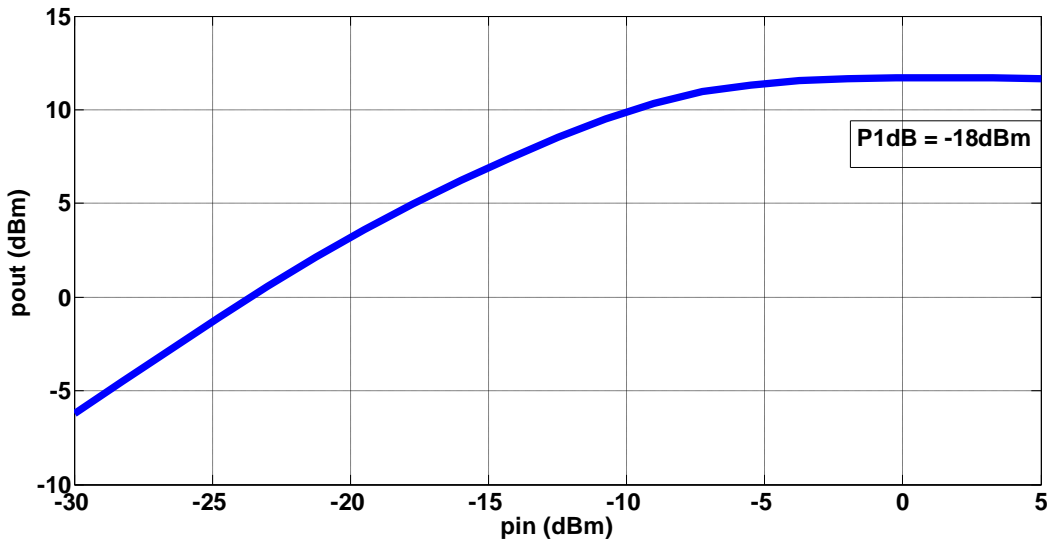
Fig. 5.14In-band P1dB for input signal of frequency 501MHz

In-band IIP3 is tested for two input signals of frequencies of 501MHz and 503MHz giving third order intermodulation component at 5MHz resulting in in-band IIP3 of -5.75897 dBm as shown in Fig.5.15.
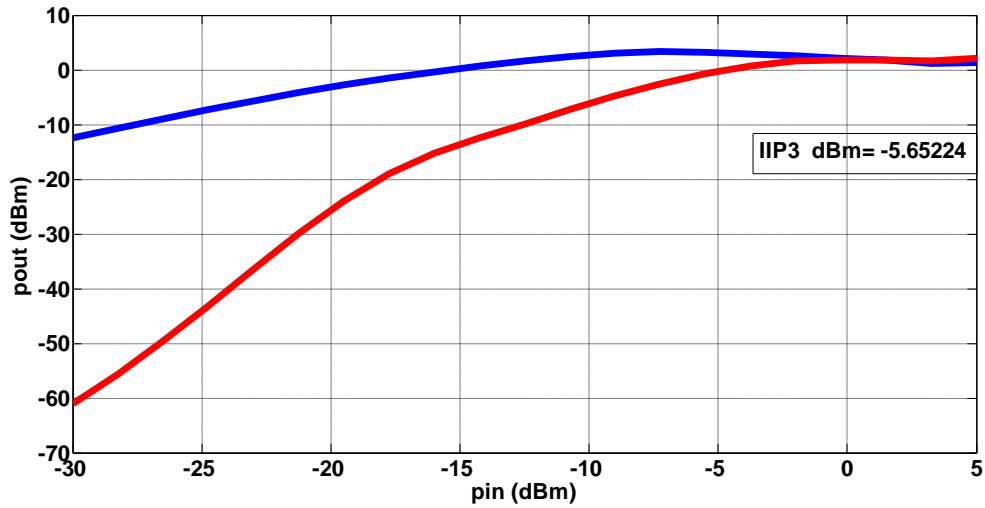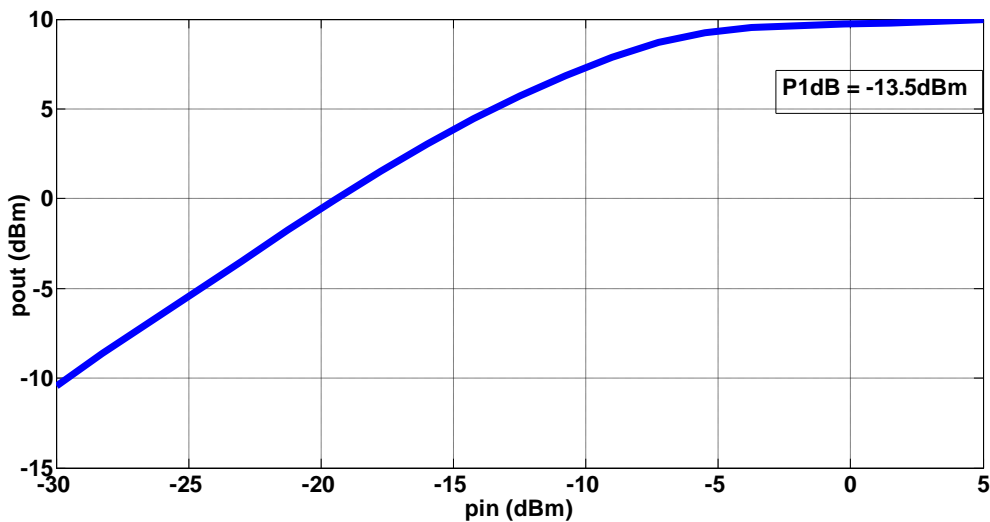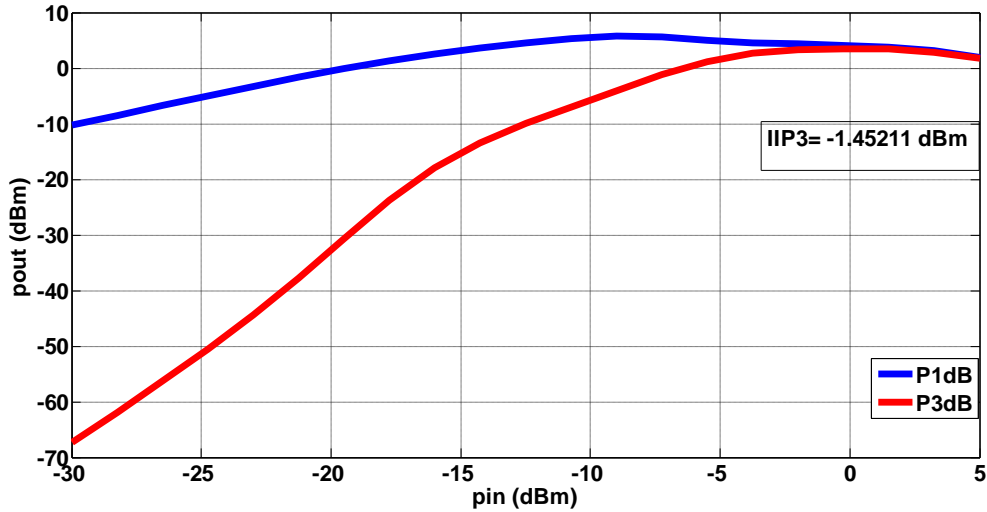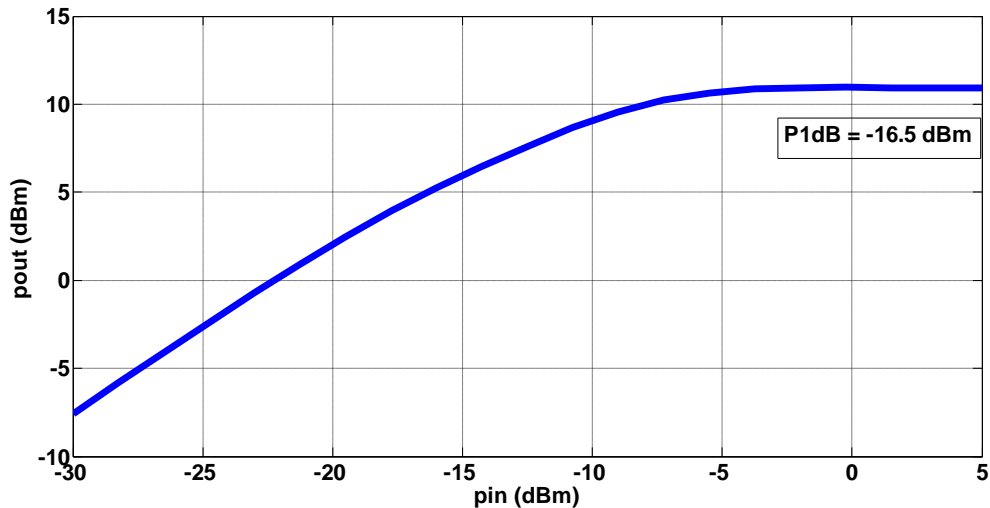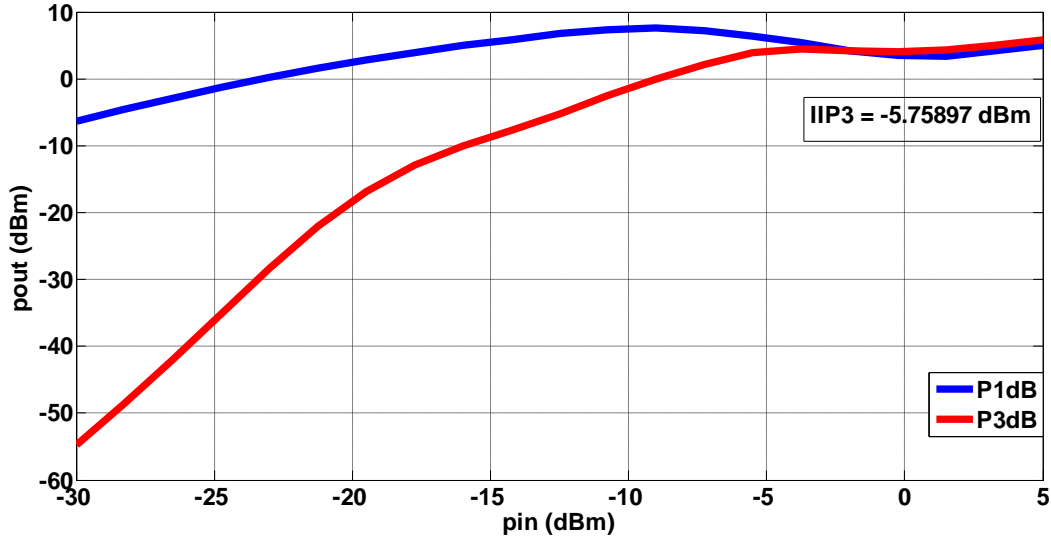

Fig. 5.15 In-band IIP3 for input signals with frequencies of 501MHz and 503MHz.

5.3. Gain

The gain of the proposed receiver front-end is controlled by the charge sampler's gain which depends on the G_m of the transconductor, the sampling capacitance (C_s), the number of the integrated samples (N) and finally the integration time (T_i).

For G_m of nearly 5mS, C_s of 300fF, N=8 and T_i=125 psec; the PAC gain at 2GHz input frequency is equal to 23.5 dB by substituting in the formula below.

$$\text{Gain} = \frac{2\sqrt{2}\,NG_m T_i}{\pi C_s} = \frac{2\sqrt{2}*8*5*10^{-3}*125*10^{-12}}{\pi*300*10^{-15}}$$

As the frequency decreases, the integration time (T_i) is higher, however, the integration switches are represented by resistances which means that the transconductor current will be distributed between its output resistance and the integration switch resistance decreasing the amount of the integrated current that's why the PAC gain doesn't increase by the expected value with the increase of the integration time.

5.3.1. The PAC gain for 2GHz frequency band

Fig.5.16 shows the PAC gain of the proposed receiver front-end versus the output frequency for input frequency from (2GHz to 10GHz). As it is obvious from the figure below, the DC gain is 23.5 dB and the notches are at multiples of $\frac{1}{8T_i}$ ($\frac{1}{8T_i}$ = 1GHz).

Fig. 5.16 PAC gain for input frequency from 2GHz to 10GHz

5.3.2. The PAC gain for 1GHz frequency band

Fig.5.17 shows the PAC gain of the proposed receiver front-end versus the output frequency for input frequency from (1GHz to 10GHz). As it is obvious from the figure below, the DC gain is 27 dB and the notches are at multiples of $\frac{1}{8T_i}$ ($\frac{1}{8T_i}$ = 500MHz).
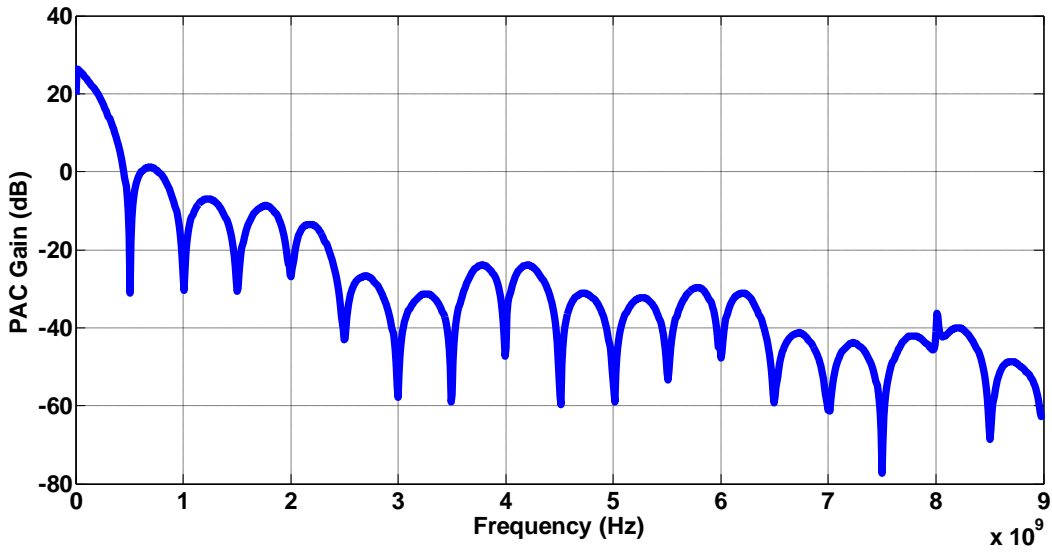
Fig. 5.17PAC gain for input frequency from 1GHz to 10GHz

5.3.3. The PAC gain for 500MHz frequency band

Fig.5.18 shows the PAC gain of the proposed receiver front-end versus the output frequency for input frequency from (500MHz to 5GHz). As it is obvious from the figure below, the DC gain is 25 dB and the notches are at multiples of $\frac{1}{8T_i}$ ($\frac{1}{8T_i} = 250$MHz).
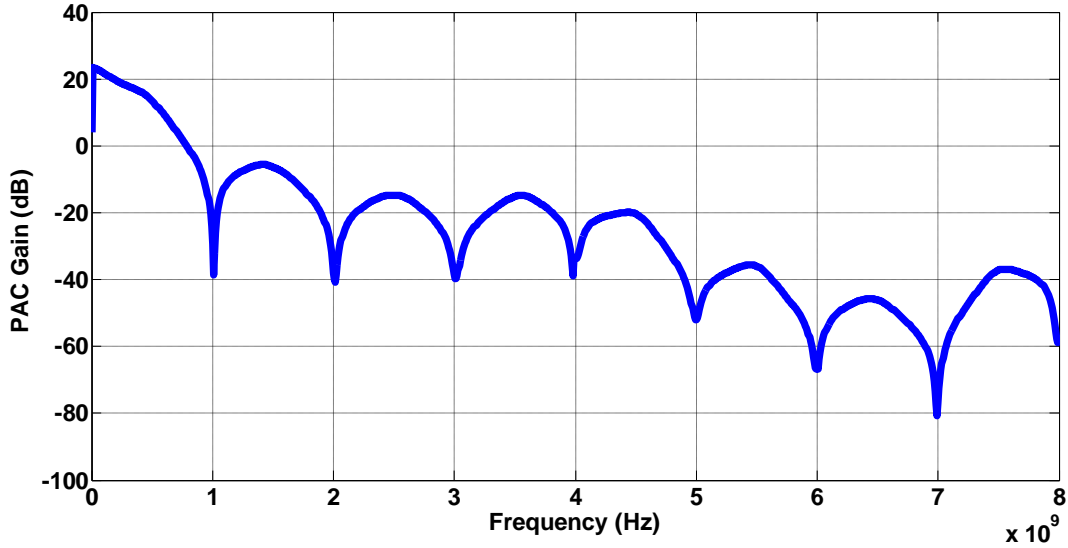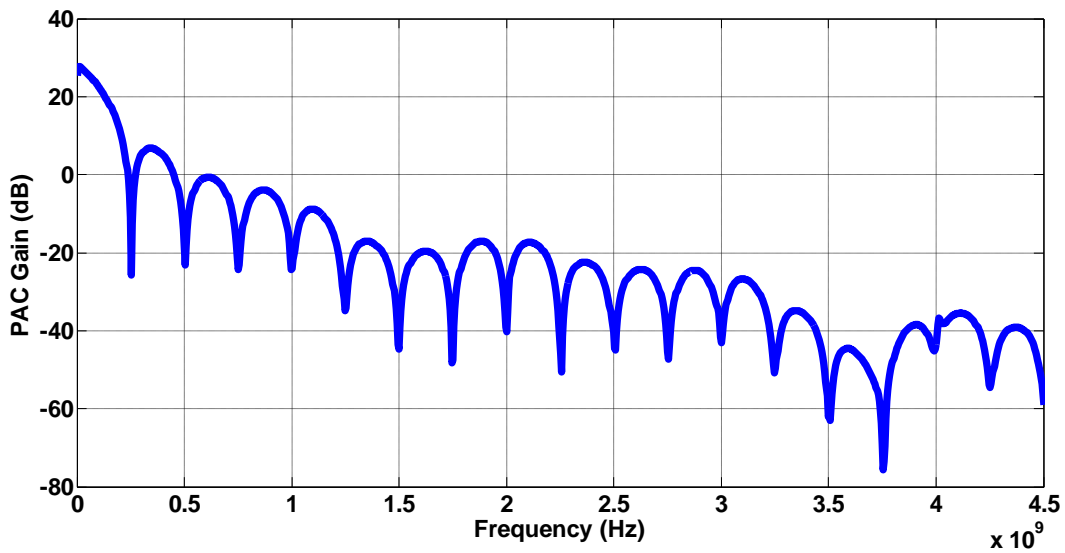

Fig. 5.18 PAC Gain for input frequency of 500MHz to 5GHz

5.4.Input power matching

The matching is ideally controlled by the translated impedance of the time varying matching network. The matching network parameters are chosen based on a trade-off between the matching and noise figure. R_{fc} is 500Ω, R_b= 90KΩ and cap=45pF. In reality the impedance seen by the antenna is the translated impedance of the time varying matching network in parallel with the transconductor input impedance. In order to have the matching controlled by the time varying matching network the transconductor have to be designed with high input impedance. Matching is indicated by S11.

5.4.1. S11 for 2GHz frequency band

As shown in Fig.5.19, the S11 of the proposed receiver front-end architecture at 2GHz is -10 dB indicating good matching at this frequency.
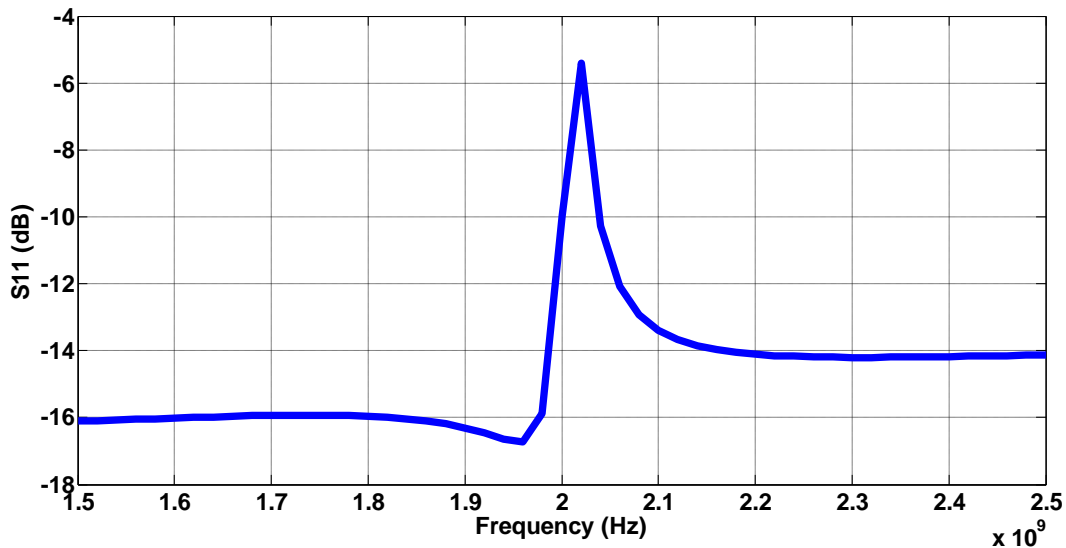
Fig. 5.19 S11 at input frequencies from 1.5GHz to 2.5GHz

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5.4.2. S11 for 1GHz frequency band

As shown in Fig.5.20, the S11 of the proposed receiver front-end architecture at 1GHz is -10 dB indicating good matching at this frequency.

Fig. 5.20 S11 at input frequencies from 500MHz to 1.5GHz

5.4.3. S11 for 500MHz frequency band

As shown in Fig.5.21, the S11 of the proposed receiver front-end architecture at 500MHz is -10 dB indicating good matching at this frequency.
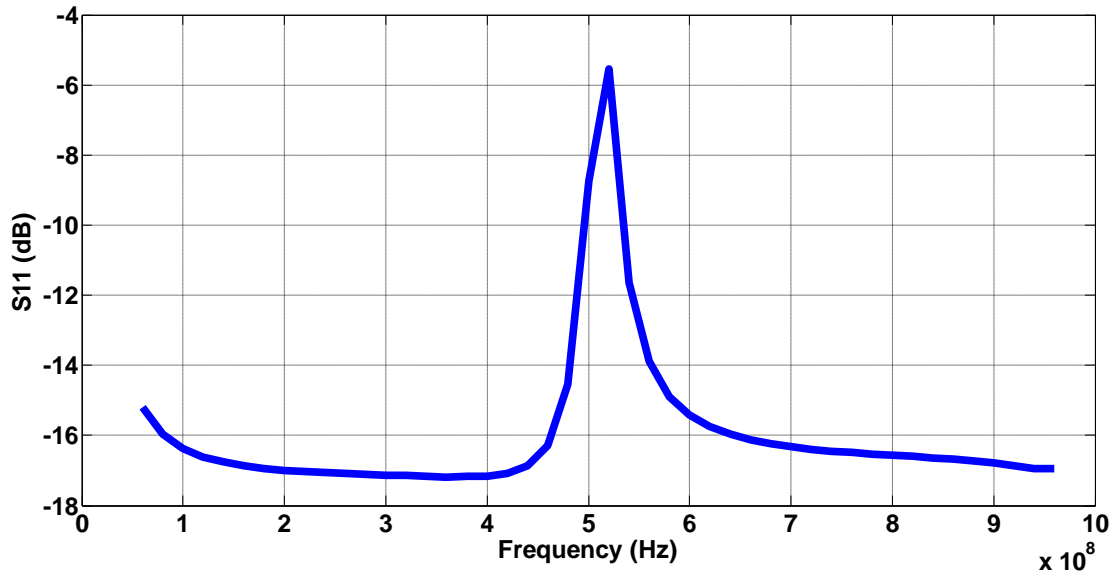
Fig. 5.21S11 at input frequencies from 0 to 1GHz

5.5.Corners analysis

The design is implemented on Global Foundries (GF) kit; this kit has different corner analysis, in addition to the well known process corners fast-fast (ff), slow-slow (ss), fast-slow(fs) and slow-fast (sf) (the first adjectiv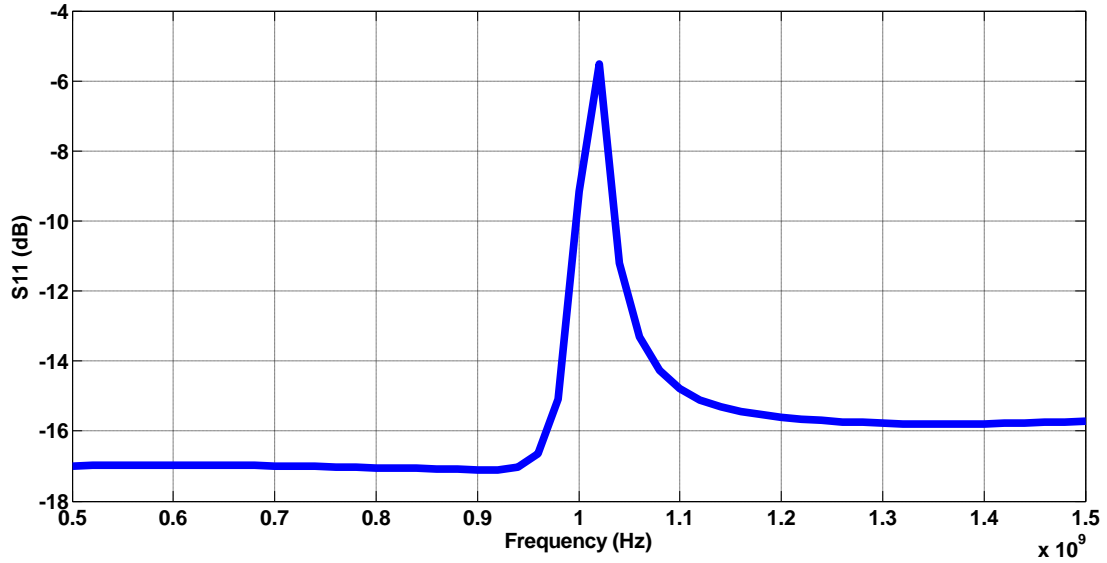e is describing pmos and the second one is describing nmos) there is a third letter which can be g standing for global process variations determined by random distributions which gives the same results as that of the normal well known process corners, p standing for passive mismatch determined by random distributions with a unique set of values for each instance of the model or f standing for FET doping and geometric mismatch effects determined by random distributions with a unique set of values for each instance of the model. The results across all process corners are shown in this section.

5.5.1. Noise Figure at 2GHz across all process corners

In this section, the noise figure of the proposed architecture for input frequency of 2GHz is shown across all the process corners in three different conditions f, p and g. The most effective condition on the noise figure for this design is f as the design is differential afterwards, the p condition.

5.5.1.1. *Noise Figure at 2GHz at fff, ffp and ffg corners*

The noise figure of the proposed architecture at 2GHz at fast-fast (ff) process corner with the three different flavors fff,ffg and ffp is shown in Fig.5.22. NF at 10MHz (the targeted IF frequency) at fff is 9.4 dB, at ffp is 8.2dB and at ffg is 8.2dB.

Fig. 5.22Noise figure at 2GHz at fff,ffg and ffp

5.5.1.2.   *Noise Figure at 2GHz at ssf, ssp and ssg corners*

The noise figure of the proposed architecture at 2GHz at slow-slow (ss) process corner with the three different flavors ssf,ssg and ssp is shown in Fig.5.23. NF at 10MHz (the targeted IF frequency) at ssf is 8.3 dB, at ssp is 7.7dB and at ssg is 7.6 dB.

Fig. 5.23Noise figure at 2GHz at ssf,ssg and ssp

5.5.1.3. *Noise Figure at 2GHz at fsfand fsg*

The noise figure of the proposed architecture at 2GHz at fast-slow (fs) process corner with the two different flavors fsf and fsg is shown in Fig.5.24. NF at 10MHz (the targeted IF frequency) at fsf is 7.6 dB and at fsg is 7.7 dB.
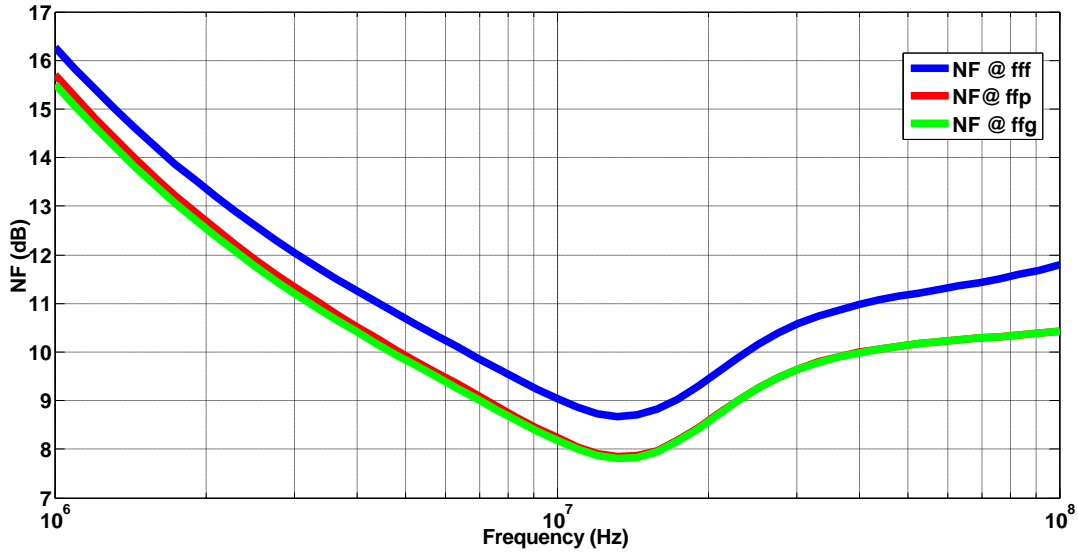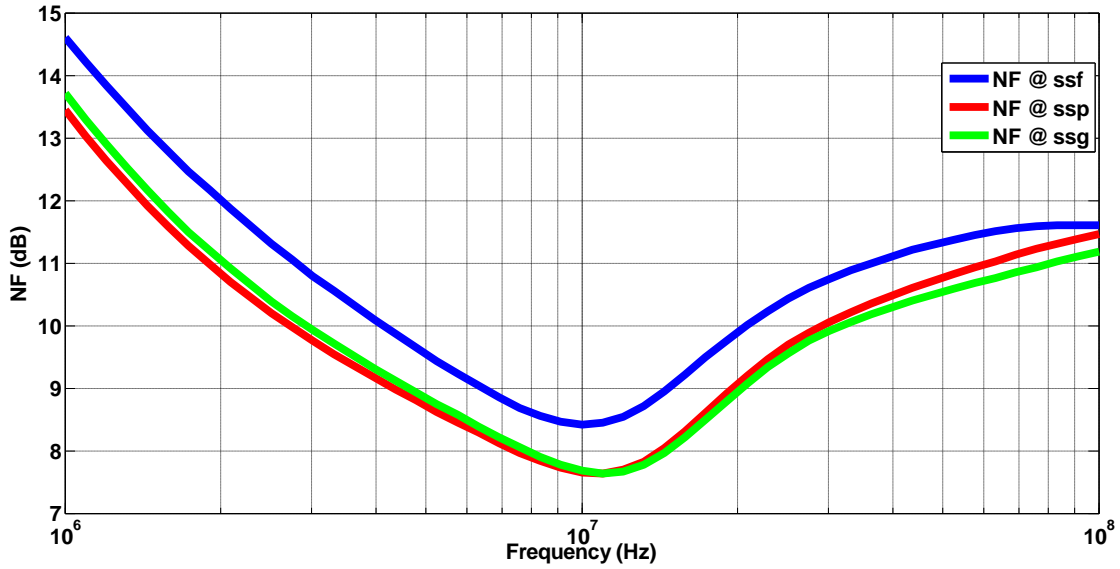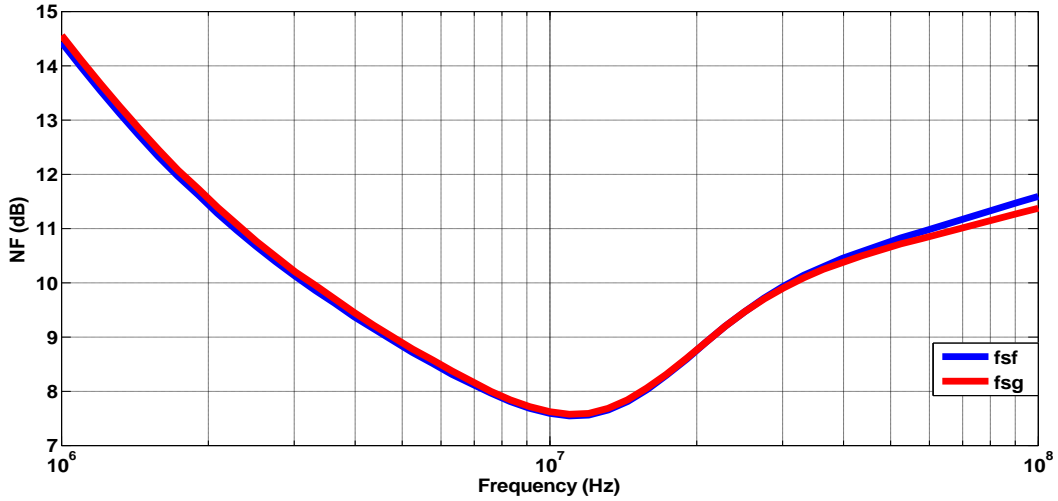

Fig. 5.24 Noise figure at 2GHz at fsf and fsg

5.5.1.4. *Noise Figure at 2GHz at sff and sfg*

The noise figure of the proposed architecture at 2GHz at slow-fast (sf) process corner with the two different flavors sff and sfg is shown in Fig.5.25. NF at 10MHz (the targeted IF frequency) at sff is 8.6 dB and at sfg is 8.7 dB
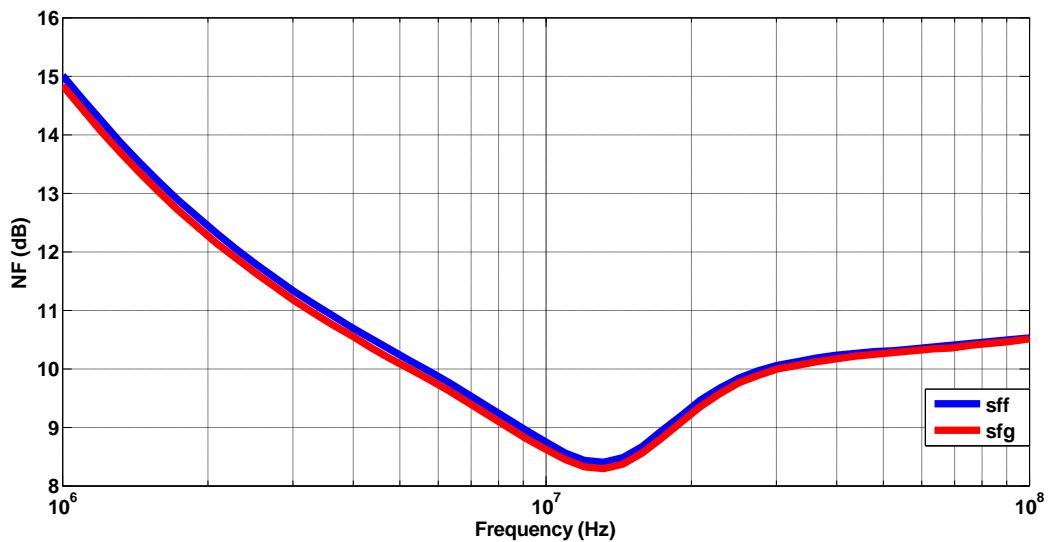
Fig. 5.25NF at 2GHz at sff and sfg

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5.5.2. Out-of-band P1dB and IIP3 at 2GHz at all process corners

In this section, the out-of-band P1dB of the proposed architecture for input frequency of 2.1GHz and out-of-band IIP3 for two input frequencies of 2.1GHz and 2.12GHz are shown across all process corners in three different conditions f, p and g.

5.5.2.1. Out-of-band P1dB and IIP3 at 2GHz at fff, ffp and ffg

Out-of-band IIP3 of the proposed architecture for input frequencies of 2.1GHz and 2.12GHz is -2.94998 dBm at fff, -2.15825 dBm at ffp and -1.86815 dBm at ffg as shown in Fig.5.26.

Fig. 5.26Out-of-band IIP3 for two input frequencies of 2.1GHz and 2.12GHz at fff,ffp and ffg.

Out-of-band P1dB of the proposed architecture for an input frequency of 2.1GHz is -11.8 dBm at fff, -11.2 dBm at ffp and -11.17 dBm at ffg as shown in Fig.5.27.

Fig. 5.27 Out-of-band P1dB for input frequency of 2.1GHz at fff,ffp and ffg.

5.5.2.2. *Out-of-band P1dB and IIP3 at 2GHz at ssf, ssp and ssg*

Out-of-band IIP3 of the proposed architecture for two input frequencies of 2.1GHz and 2.12GHz is -6.5 dBm at ssf, -5.2 dBm at ssp and -4 dBm at ssg as shown in Fig.5.28.

Fig. 5.28 Out-of-band IIP3 for two inputs of frequencies 2.1GHz and 2.12GHz at ssf, ssp and ssg

Out-of-band P1dB of the proposed architecture for an input frequency of 2.1GHz is -14.7 dBm at ssf, -14.5 dBm at ssp and -14 dBm at ssg as shown in Fig.5.29.

Fig. 5.29 Out-of-band P1dB for input frequency of 2.1GHz at ssf, ssp and ssg

5.5.2.3. *Out-of-band P1dB and IIP3 at 2GHz at fsf and fsg*

Out-of-band IIP3 of the proposed architecture for input frequencies of 2.1GHz and 2.12GHz is -4.4 dBm at fsf and -2.956 dBm at fsg as shown in Fig.5.30.
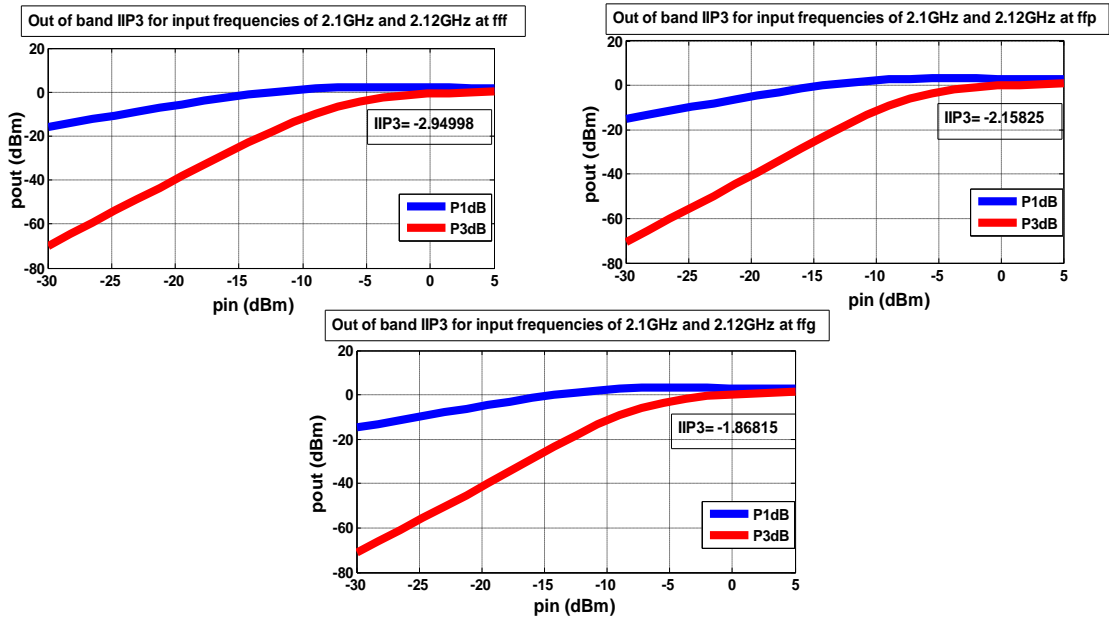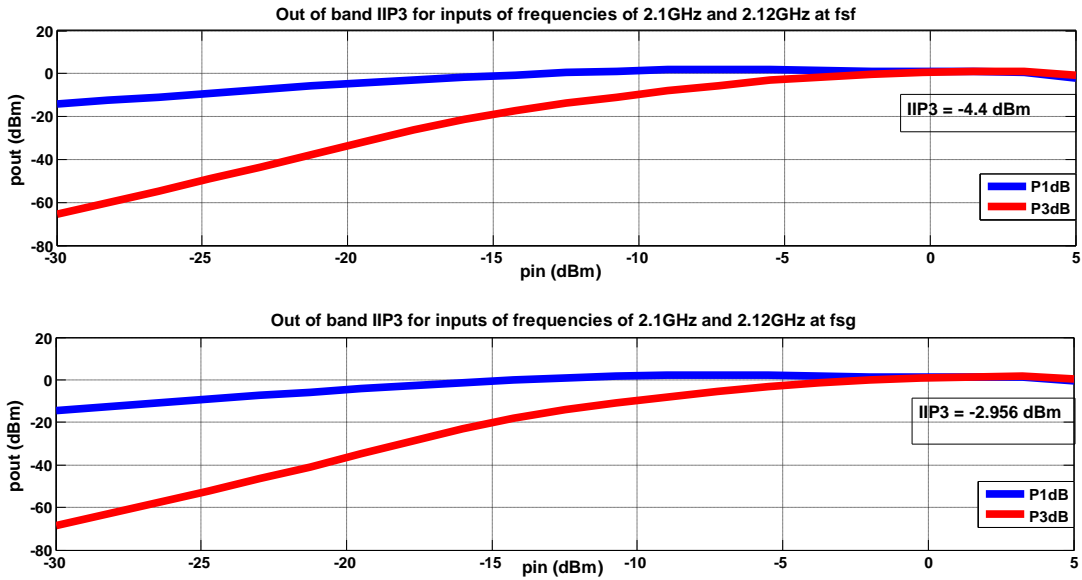

Fig. 5.30 Out-of-band IIP3 for input frequencies of 2.1GHz and 2.12GHz at fsf and fsg

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Out-of-band P1dB of the proposed architecture for an input frequency of 2.1GHz is -14.278 dBm at fsf and -13.53 dBm at fsg as shown in Fig.5.31.
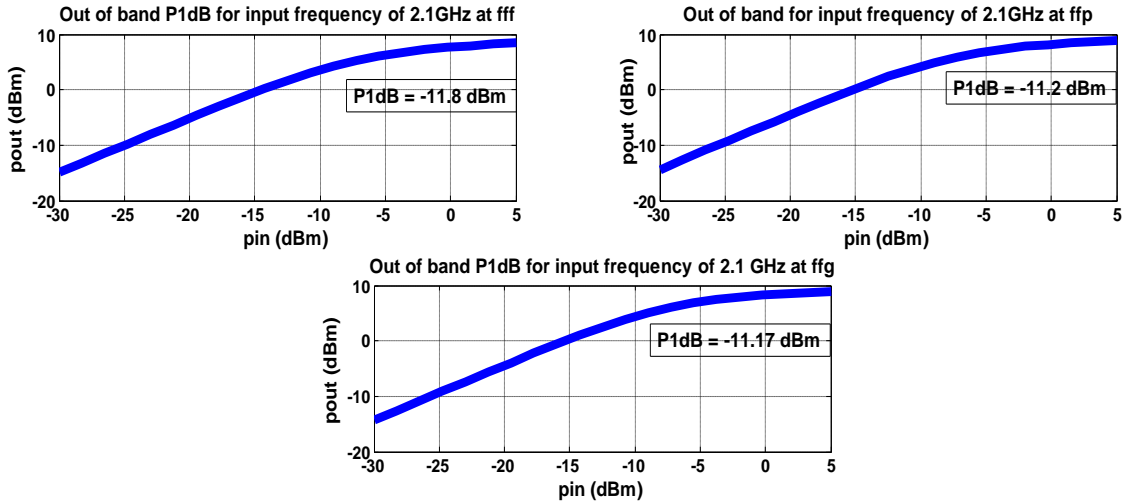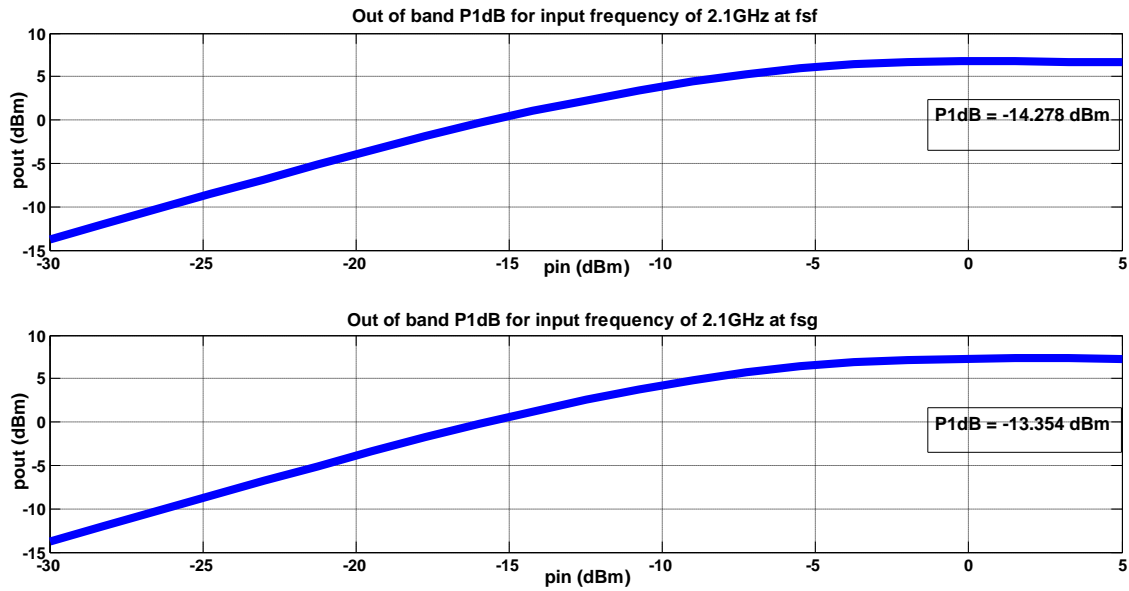

Fig. 5.31Out-of-band P1dB for input frequency of 2.1 GHz at fsf and fsg

5.5.2.4. *Out-of-band P1dB and IIP3 at 2GHz at sff and sfg*

Out-of-band IIP3 of the proposed architecture for input frequencies of 2.1GHz and 2.12GHz is -2.128 dBm at sff and -2.462 dBm at sfg as shown in Fig.5.32.
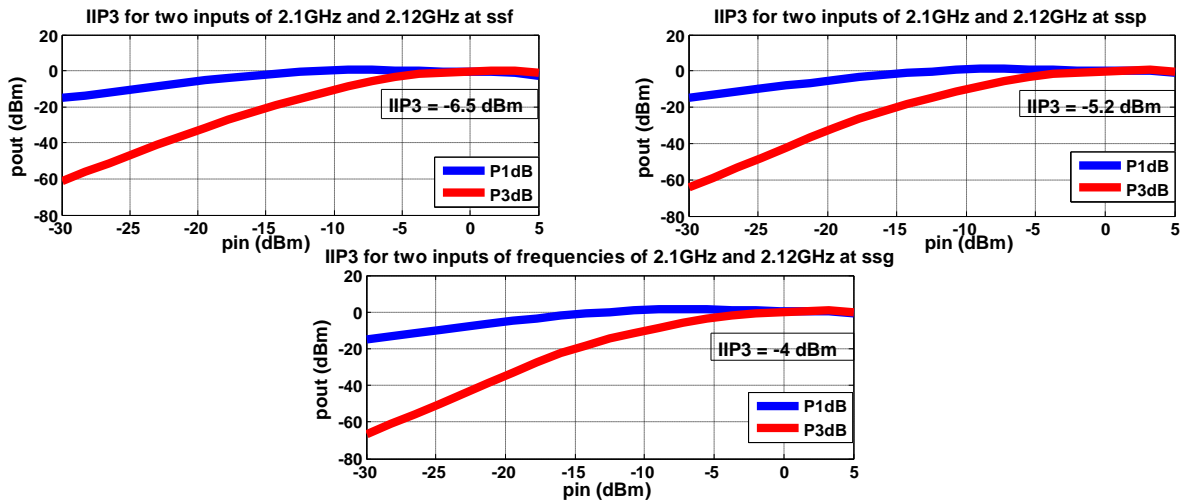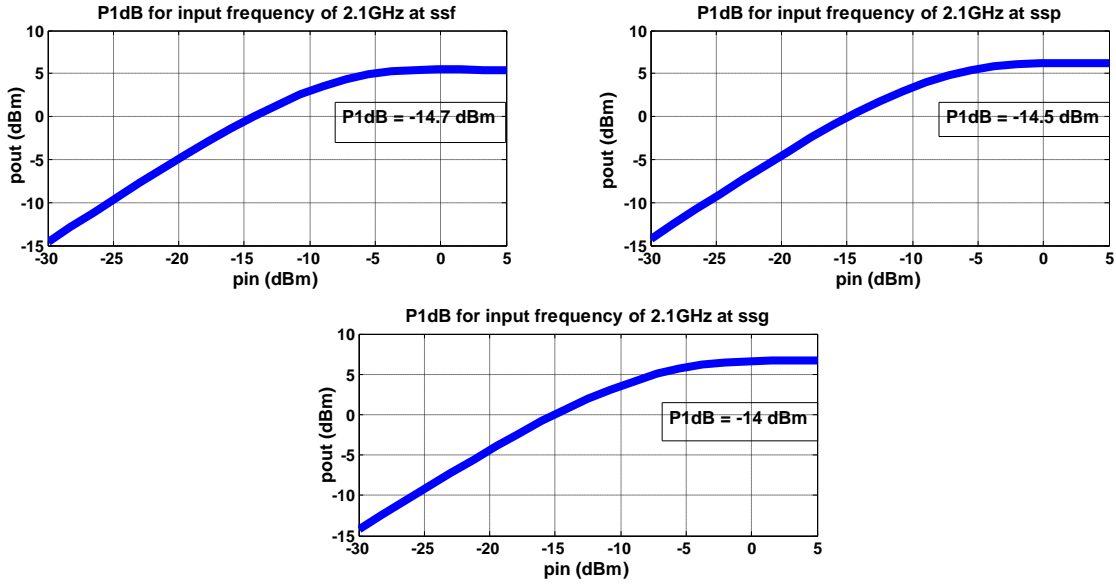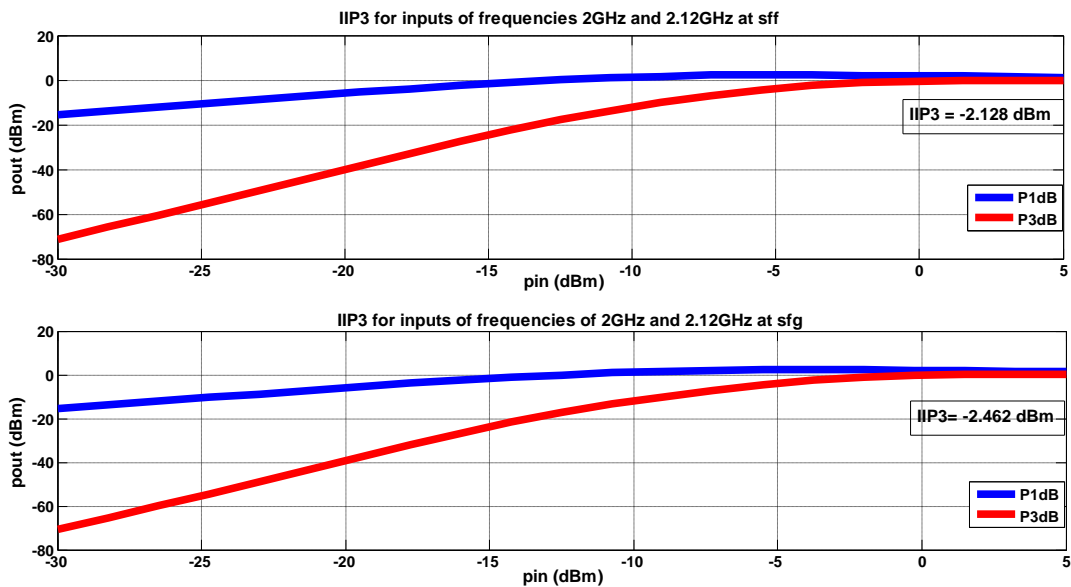

Fig. 5.32 Out-of-band IIP3 for two inputs of 2.1GHz and 2.12GHz at sff and sfg

Out-of-band P1dB of the proposed architecture for an input frequency of 2.1GHz is -12 dBm at sff and -12.334 dBm at sfg as shown in Fig.5.33.

Fig. 5.33 Out-of-band P1dB for input frequency of 2.1GHz at sff and sfg

5.5.3. Matching for 2GHz input at all process corners

In this section, S11 of the proposed architecture for input frequency of 2GHz is shown across all process corners in three different conditions f, p and g.

5.5.3.1. *S11 for 2GHz input frequency at fff, ffp and ffg*

S11 of the proposed architecture at 2GHz is -11.5 dB at fff, -11 dB at ffp and -10 dB at ffg as shown in Fig.5.34.
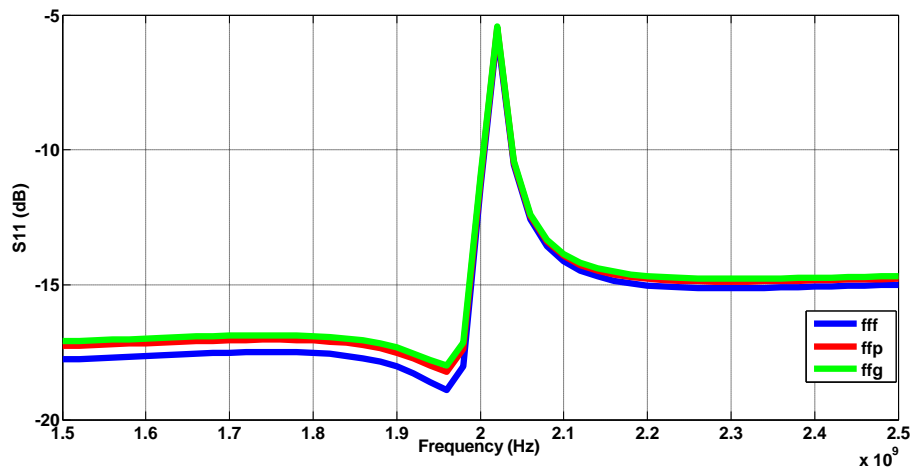
Fig. 5.34 S11 at 2GHz at fff,ffp and ffg.

5.5.3.2. *S11 for 2GHz input frequency at ssf, ssp and ssg*

S11 of the proposed architecture at 2GHz is -9 dB at ssf, -9.5 dB at ssp and -10 dB at ssg as shown in Fig.5.35.
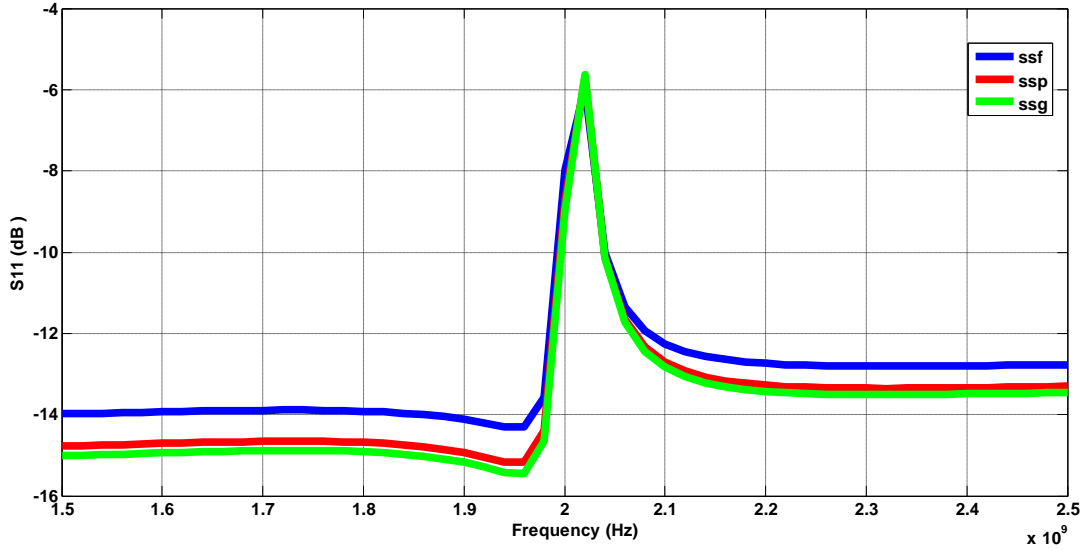
Fig. 5.35S11 at 2GHz at ssf,ssp and ssg.

5.5.3.3. *S11 for 2GHz input frequency at fsf and fsg*

S11 of the proposed architecture at 2GHz is -10 dB at fsf and -10 dB at fsg as shown in Fig.5.36.
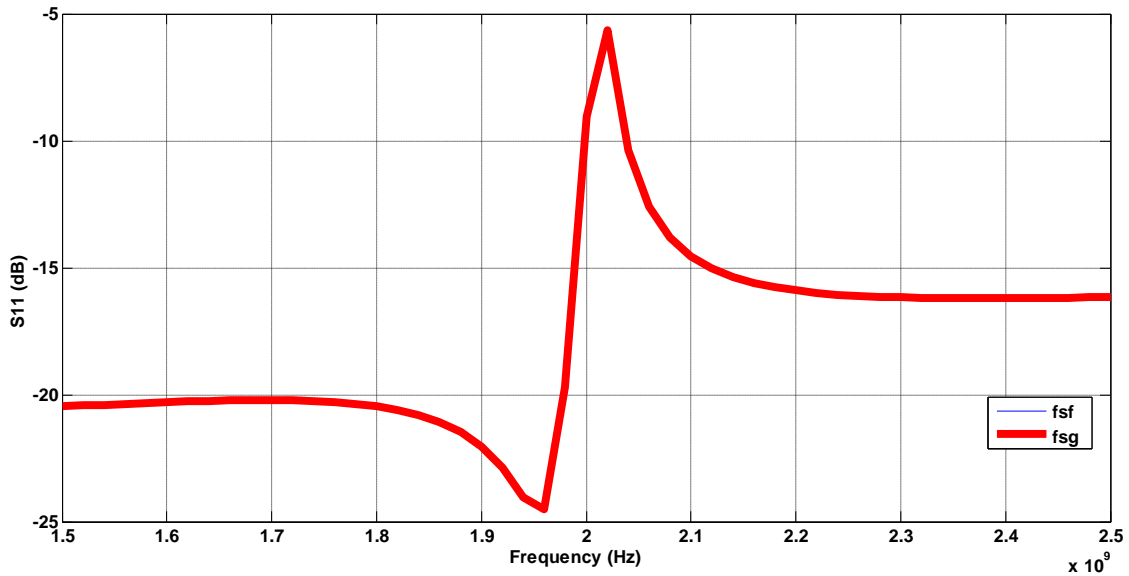
Fig. 5.36 S11 at 2GHz at fsf and fsg.

5.5.3.4. *S11 for 2GHz input frequency at sff and sfg*

S11 of the proposed architecture at 2GHz is -10 dB at sff and -10 dB at sfg as shown in Fig.5.37.
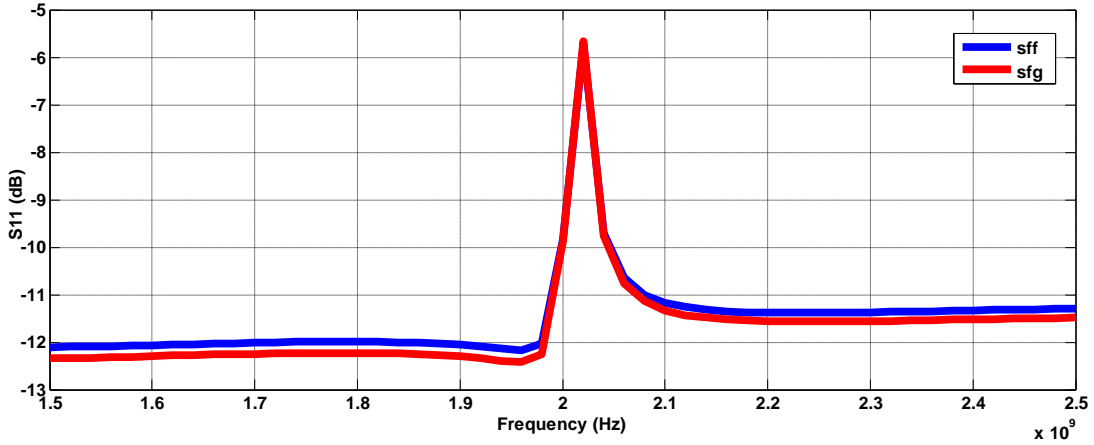
Fig. 5.37S11 at 2GHz at sff and sfg.

5.5.4. In-band IIP3 and P1dB for 2GHz input at all process corners

In this section, the in-band P1dB of the proposed architecture for input frequency of 2.001GHz and in band IIP3 for two input frequencies of 2.001GHz and 2.003GHz are shown across all process corners in three different conditions f, p and g.

5.5.4.1. *In-band P1dB and IIP3 for 2GHz input frequency at fff, ffg and ffp*

In-band IIP3 of the proposed architecture for inputs of 2.001GHz and 2.003GHz is -4.394 dBm at fff, -3.5dBm at ffp and -3.067 dBm at ffg as shown in Fig.5.38.

Fig. 5.38In-band IIP3 for input frequencies of 2.001GHz and 2.003GHz at fff, ffg and ffp

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In-band P1dB of the proposed architecture for input frequency of 2.001GHz is -14 dBm at fff, -12.9 at ffp and -12.5 dBm at ffg as shown in Fig.5.39.
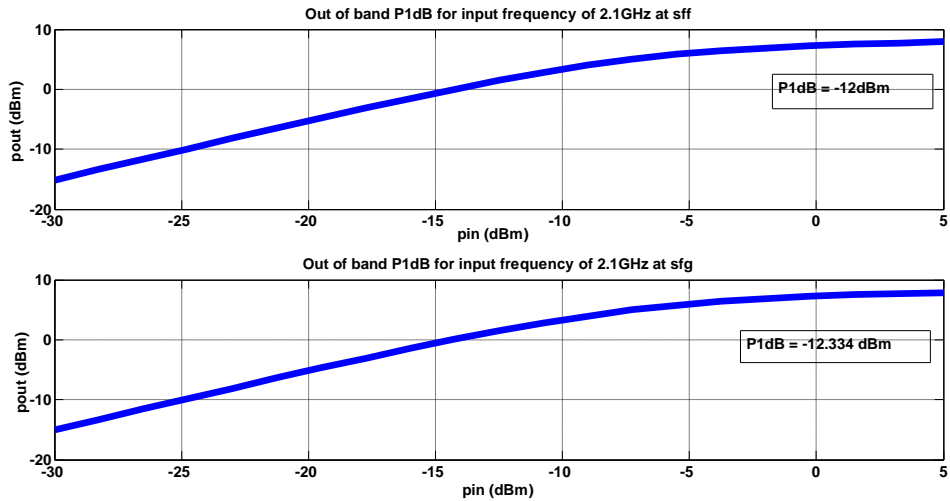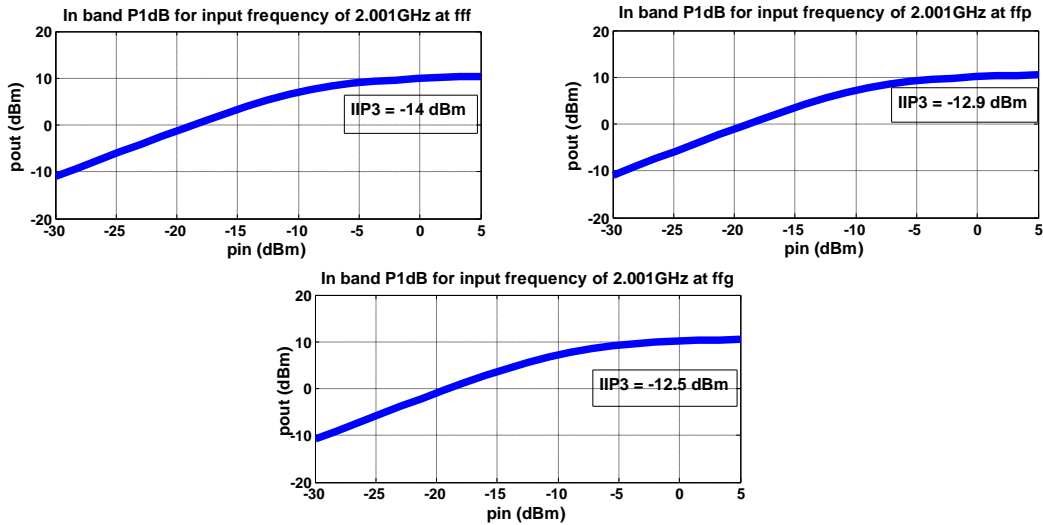

Fig. 5.39In-band P1dB for input frequencies of 2.001GHz and 2.003GHz at fff, ffg and ffp

5.5.4.2. *In-band P1dB and IIP3 for 2GHz input frequency at ssf, ssg and ssp*

In-band IIP3 of the proposed architecture for inputs of 2.001GHz and 2.003GHz is -9.358 dBm at ssf, -7 dBm at ssp and -4.916 dBm at ssg as shown in Fig.5.40.
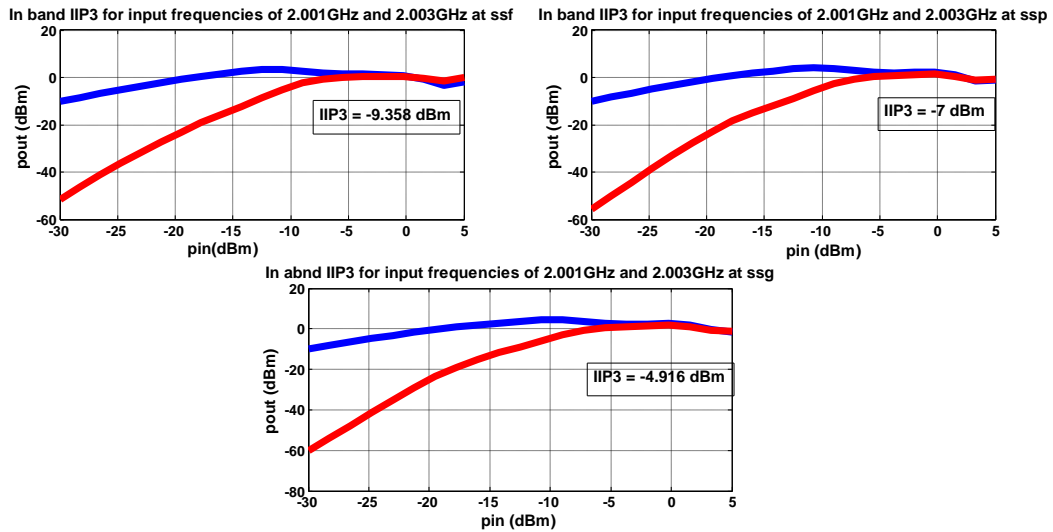
Fig. 5.40 In-band IIP3 for input frequencies of 2.001GHz and 2.003GHz at ssf, ssg and ssp

In-band P1dB of the proposed architecture for input frequency of 2.001GHz is -17 dBm at ssf, -16.8at ssp and -16 dBm at ssg as shown in Fig.5.41.
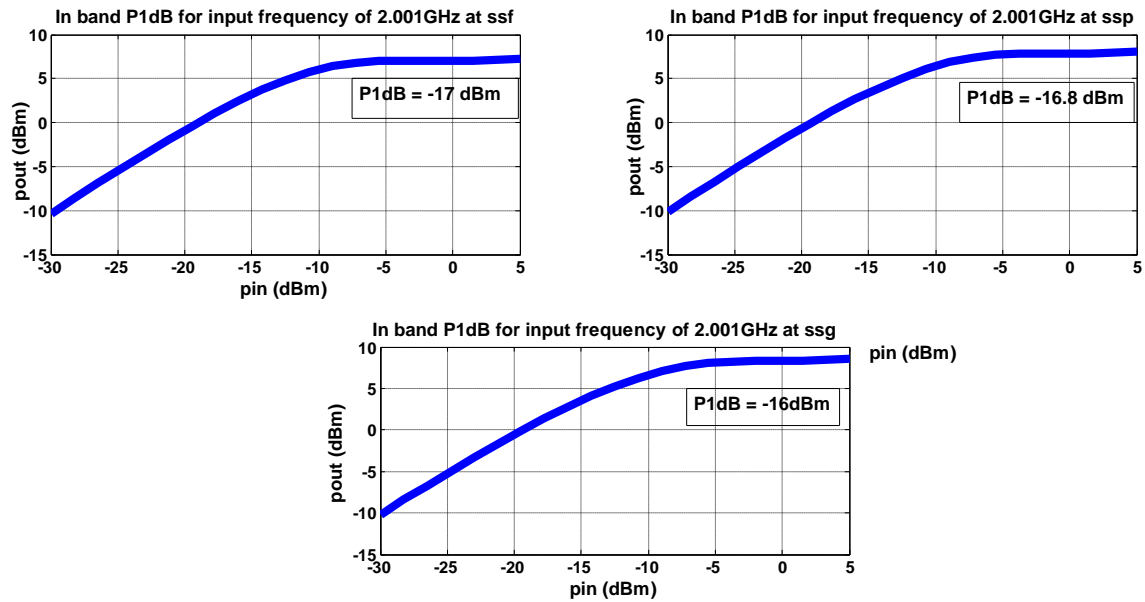
Fig. 5.41In-band P1dB frequency for input of 2.001GHz at ssf, ssg and ssp

5.5.4.3. *In-band P1dB and IIP3 for 2GHz input frequency at fsf and fsg*

In-band IIP3 of the proposed architecture for inputs of 2.001 GHz and 2.003GHz is -6.258 dBm at fsf and -3.717 dBm at fsg as shown in Fig.5.42.
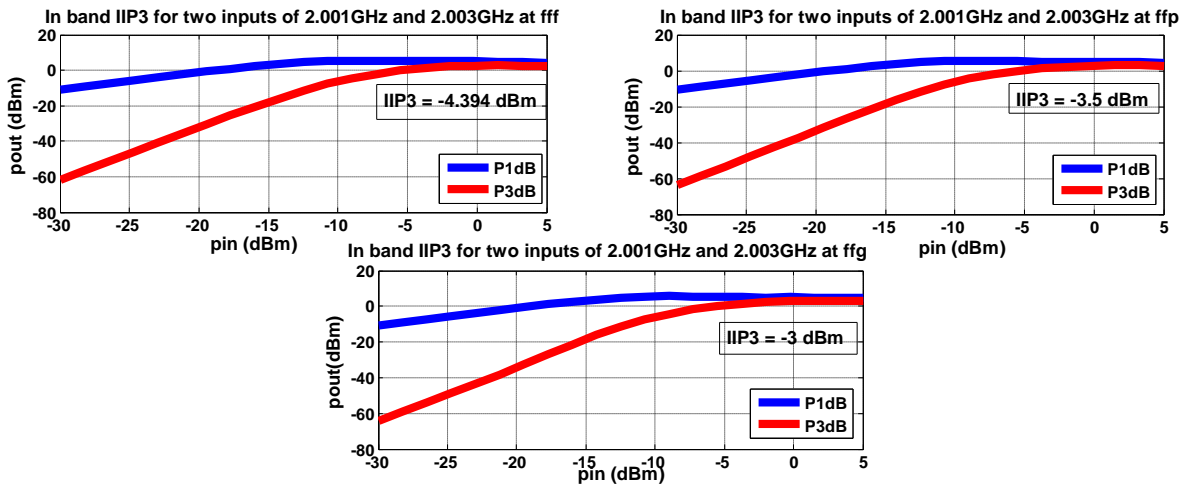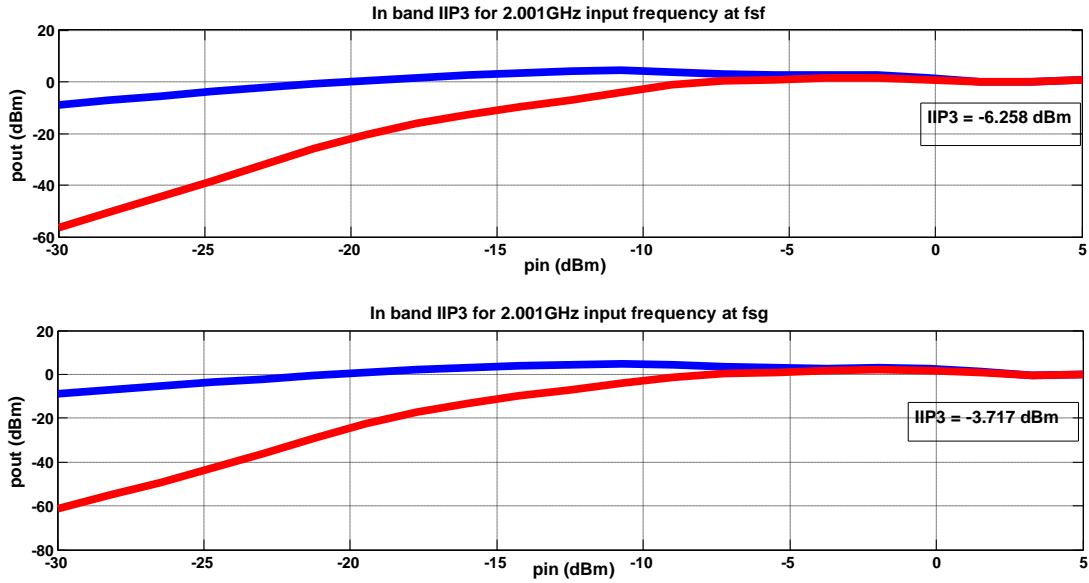
Fig. 5.42In-band IIP3 for input frequencies of 2.001GHz and 2.003GHz at fsf and fsg

In-band P1dB of the proposed architecture for input frequency of 2.001GHz is -17.162 dBm at fsf and -16.018 dBm at fsg as shown in Fig.5.43.
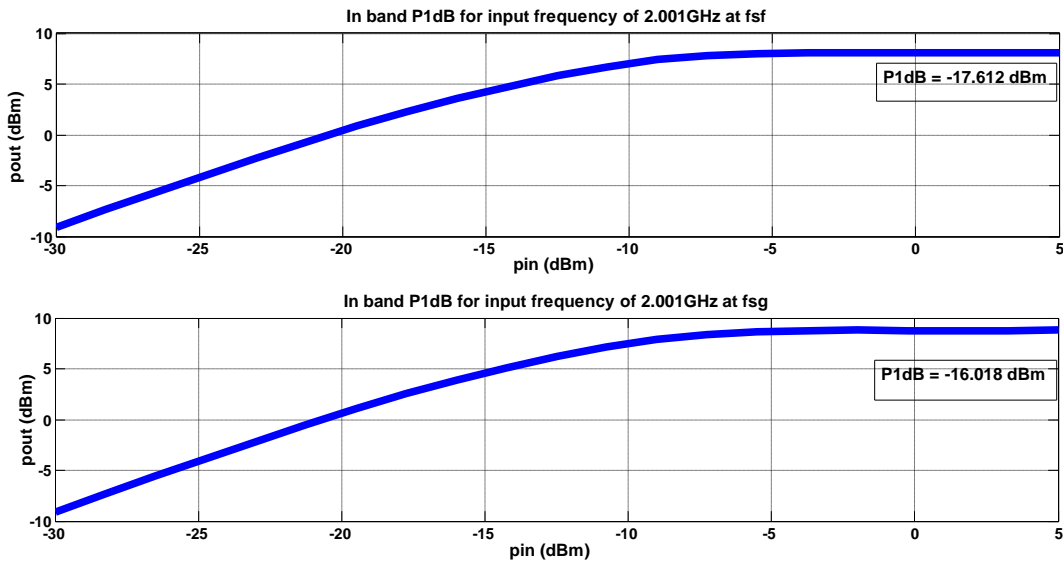
Fig. 5.43 In-band P1dB for input frequency of 2.001GHz at fsf and fsg

5.5.5. Noise Figure for 1GHz frequency at all process corners

In this section, Noise figure of the proposed architecture for input frequency of 1GHz is shown at all the process corners in three different conditions f, p and g.

5.5.5.1. *NF for 1GHz input at fff, ffg and ffp corners*

The noise figure of the proposed architecture at 1GHz at fast-fast (ff) process corner with the three different flavors fff,ffg and ffp is shown in Fig.5.44. NF at 10MHz (the targeted IF frequency) at fff is 8.7 dB, at ffp is 8.6dB and at ffg is 8.5dB.

Fig. 5.44NF for input frequencies from 1.001Ghz to 1.1GHz at fff, ffg anf ffp

5.5.5.2. *NF for 1GHz input frequency at ssf, ssp and ssg*

The noise figure of the proposed architecture at 1GHz at slow-slow (ss) process corner with the three different flavors ssf,ssg and ssp is shown in Fig.5.45. NF at 10MHz (the targeted IF frequency) at ssf is 8.17 dB, at ssp is 7.3 dB and at ssg is 7.4 dB.
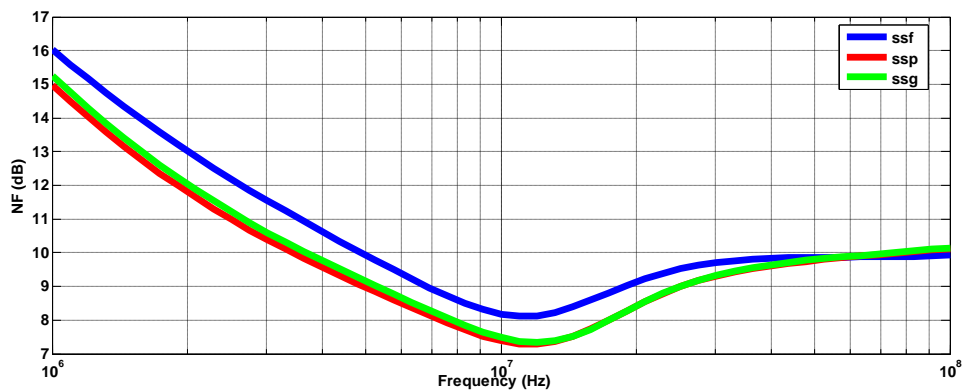
Fig. 5.45NF for input frequencies from 1.001GHz to 1.1GHz at ssf, ssp and ssg

5.5.5.3.   *NF for 1GHz input frequency at fsf and fsg*

The noise figure of the proposed architecture at 1GHz at fast-slow (fs) process corner with the two different flavors fsf and fsg is shown in Fig.5.46. NF at 10MHz (the targeted IF frequency) at fsf is 7.4 dB and at fsg is 7.4 dB.
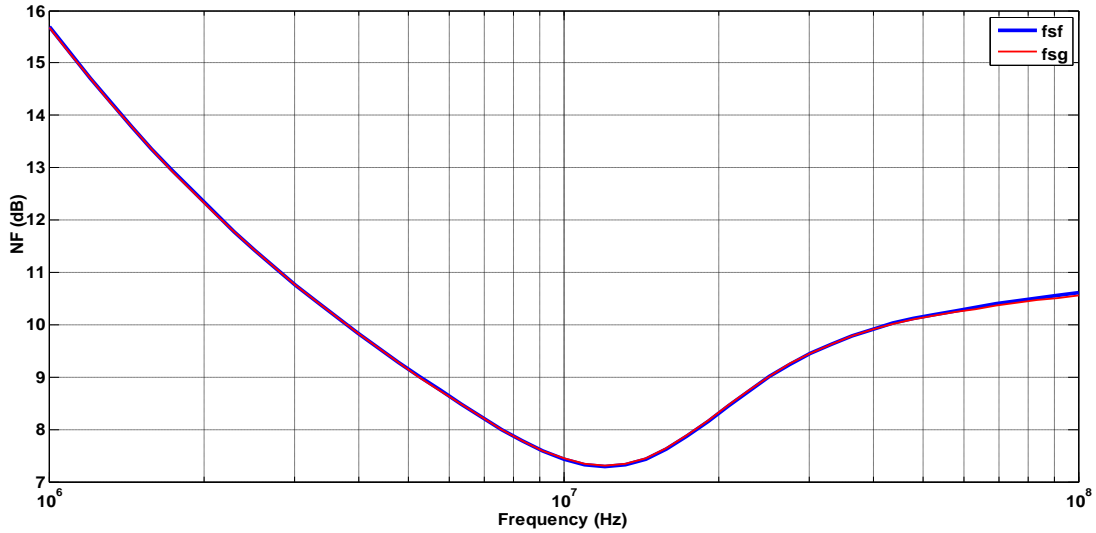
Fig. 5.46NF for input frequencies from 1.001GHz to 1.1GHz at fsf and fsg

5.5.5.4 NF for 1GHz input frequency at sff and sfg

The noise figure of the proposed architecture at 1GHz at slow-fast (sf) process corner with the two different flavors sff and sfg is shown in Fig.5.47. NF at 10MHz (the targeted IF frequency) at sff is 9 dB and at sfg is 8.9 dB.
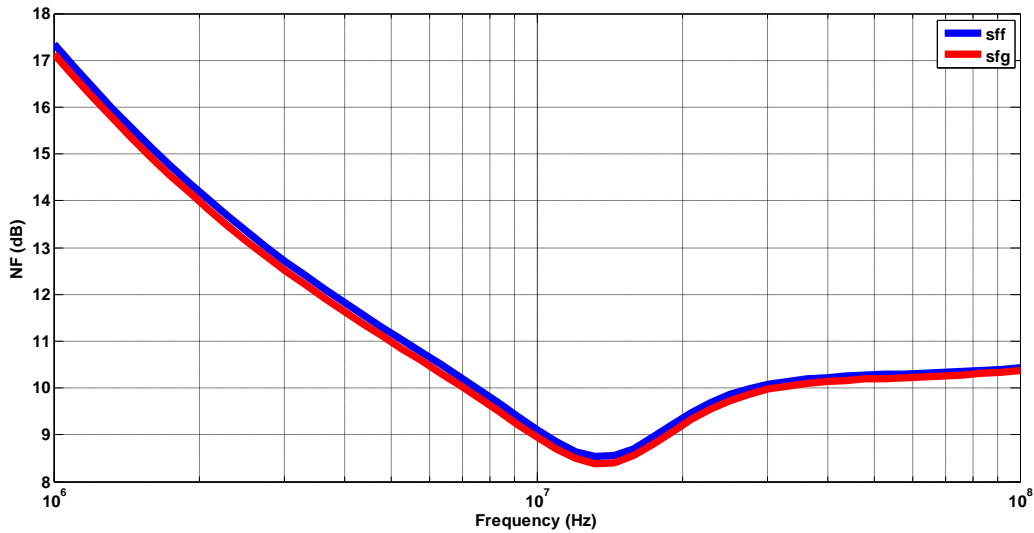
Fig. 5.47NF for input frequencies from 1.001GHz to 1.1GHz at sff and sfg

5.5.6. S11 for 1GHz frequency at all process corners

S11 of the proposed architecture for 1GHz frequency input at all process corners is shown in this section.

5.5.6.1. *S11 for 1GHz input frequency at fff, ffp and ffg*

S11 of the proposed architecture at 1GHz is -10.3 dB at fff, -10 dB at ffp and -10 dB at ffg as shown in Fig.5.48.

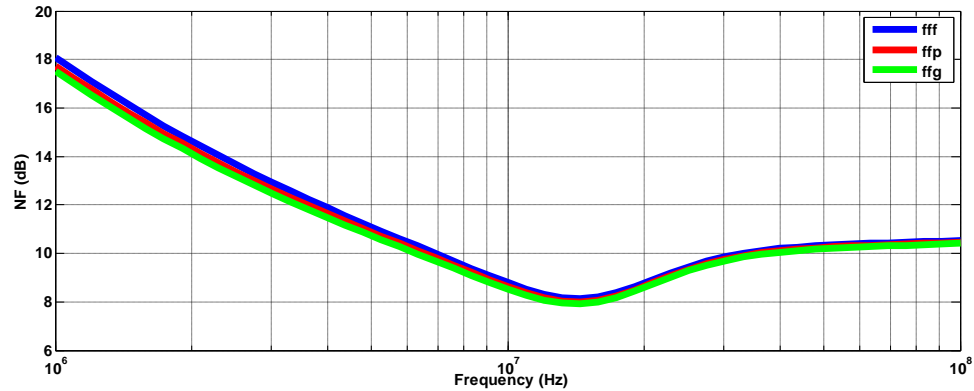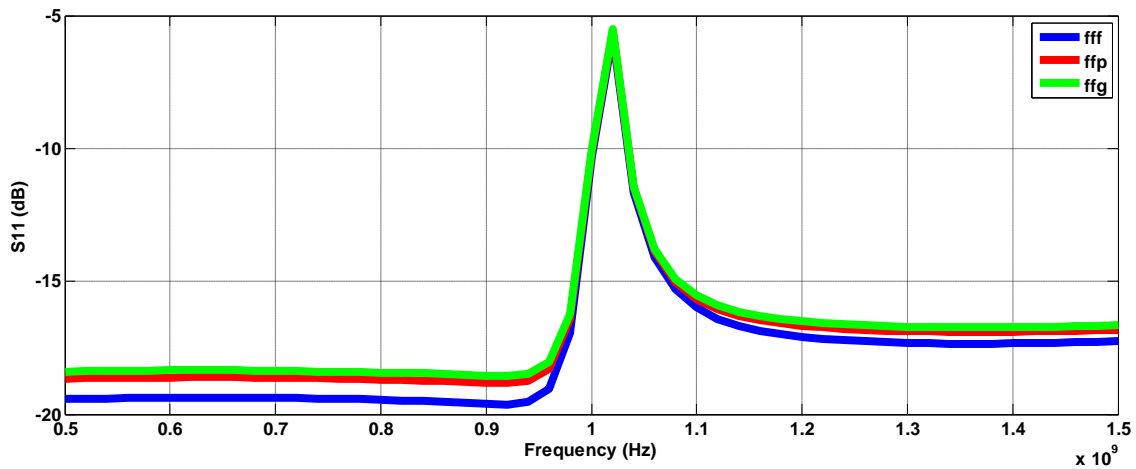Fig. 5.48S11 for input frequency of 1GHz at fff, ffp and ffg

5.5.6.2. *S11 for 1GHz input frequency at ssf, ssp and ssg*

S11 of the proposed architecture at 1GHz is -9 dB at ssf, -9 dB at ssp and -9 dB at ssg as shown in Fig.5.49.
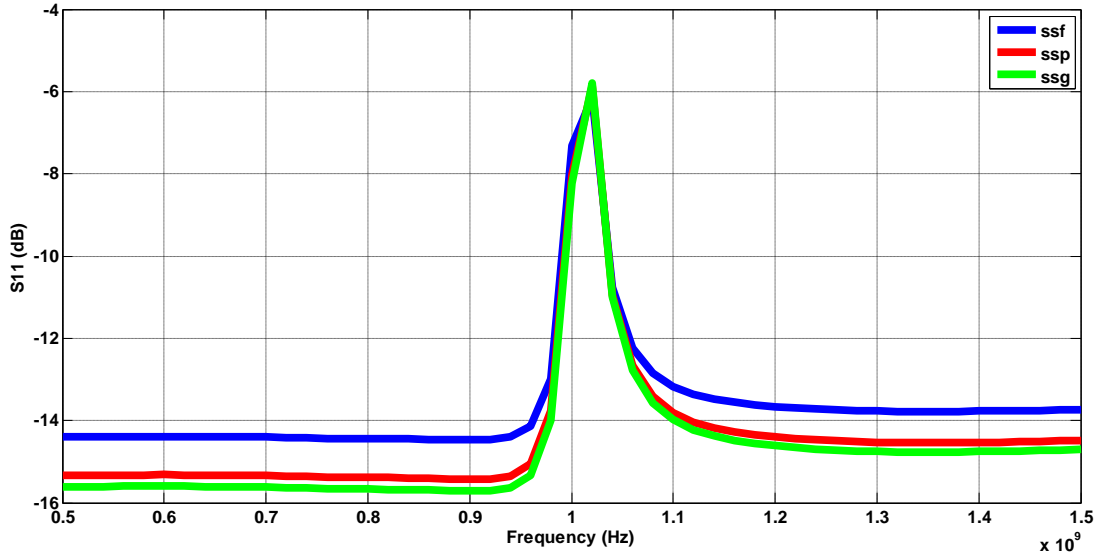
Fig. 5.49S11 for input frequency of 1GHz at ssf, ssp and ssg

5.5.6.3. *S11 for 1GHz input frequency at fsf and fsg*

S11 of the proposed architecture at 1GHz is -9 dB at fsf and -9 dB at fsg as shown in Fig.5.50.
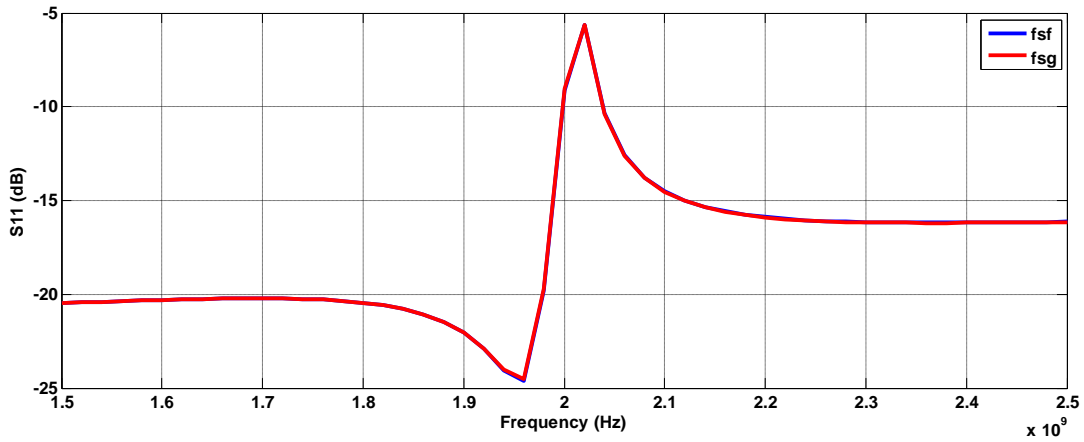
Fig. 5.50S11 for input frequency of 1GHz at fsf and fsg

5.5.6.4. *S11 for 1GHz input frequency at sff and sfg*

S11 of the proposed architecture at 1GHz is -10 dB at sff and -9.5 dB at sfg as shown in Fig.5.51.
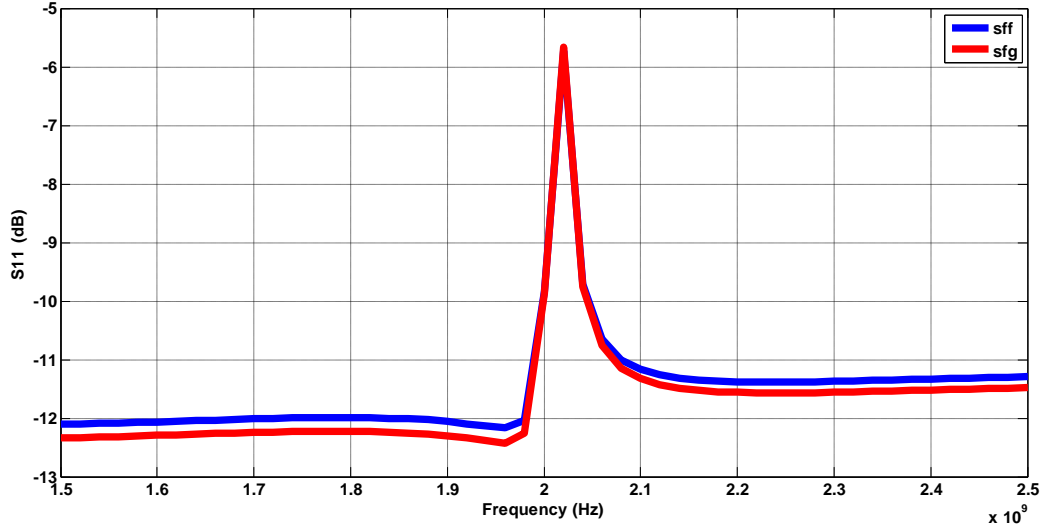
Fig. 5.51 S11 for input frequency of 1GHz at sff and sfg

5.5.7. Out-of-band IIP3 and P1dB for 1GHz input at all process corners

In this section, the out-of -band P1dB of the proposed architecture for input frequency of 1.1GHz and out of band IIP3 for two input frequencies of 1.1GHz and 1.12 GHz are shown at all the process corners in three different conditions f, p or g.

5.5.7.1. *Out-of -band P1dB and IIP3 for 1GHz input frequency at fff, ffg and ffp*

Out-of-band IIP3 of the proposed architecture for inputs of 1.1 GHz and 1.12GHz is -4.495 dBm at fff, -3.847 dBm at ffp and -3.264 dBm at ffg as shown in Fig.5.52.

Fig. 5.52 IIP3 for input frequencies of 1.1GHz and 1.12 GHz at fff, ffp and ffg

Out-of -band P1dB of the proposed architecture for input frequency of 1.1 GHz is -13.342 dBm at fff, -12.976 dBm at ffp and -12.799 dBm at ffg as shown in Fig.5.53.

Fig. 5.53Out-of-band P1dB for input frequency of 1.1GHz at fff, ffp and ffg

5.5.7.2. *Out-of -band P1dB and IIP3 for 1GHz input frequency at ssf, ssg and ssp*

Out-of-band IIP3 of the proposed architecture for inputs of 1.1 GHz and 1.12GHz is -10 dBm at ssf, -8.935 dBm at ssp and -7.361 dBm at ssg as shown in Fig.5.54.

Fig. 5.54Out-of-band IIP3 for input frequencies of 1.1GHz and 1.12GHz at ssf, ssp and ssg

Out-of-band P1dB of the proposed architecture for input frequency of 1.1 GHz   is -17.5 dBm at ssf, -17.3 dBm at ssp and -17 dBm at ssg as shown in Fig.5.55.

Fig. 5.55Out-of-band P1dB for input frequency of 1.1GHz at ssf, ssp and ssg

5.5.7.3. *Out-of -band P1dB and IIP3 for 1GHz input frequency at sff and sfg*

Out-of-band IIP3 of the proposed architecture for inputs of 1.1 GHz and 1.12 GHz is -4 dBm at sff and -4.247 dBm at sfg as shown in Fig.5.56.

Fig. 5.56Out-of-band IIP3 for input frequencies of 1.1GHz and 1.12GHz at sff and sfg

Out-of-bandP1dB of the proposed architecture for input frequency of 1.1 GHz   is -13.569 dBm at sff and -14.056 dBm at sfg as shown in Fig.5.57.
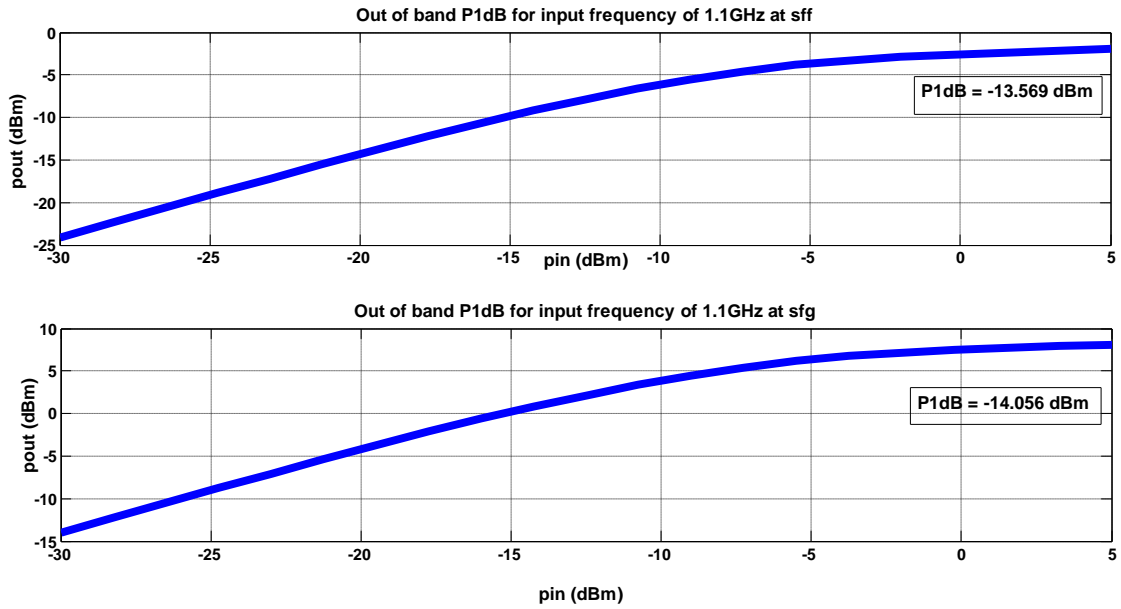
Fig. 5.57 Out-of-band P1dB for input frequency of 1.1GHz at sff and sfg

5.5.7.4. *Out-of -band P1dB and IIP3 for 1GHz input frequency at fsf and fsg*

Out-of -band IIP3 of the proposed architecture for inputs of 1.1 GHz and 1.12GHz is -8.064 dBm at fsf and -5.631 dBm at fsg as shown in Fig.5.58.

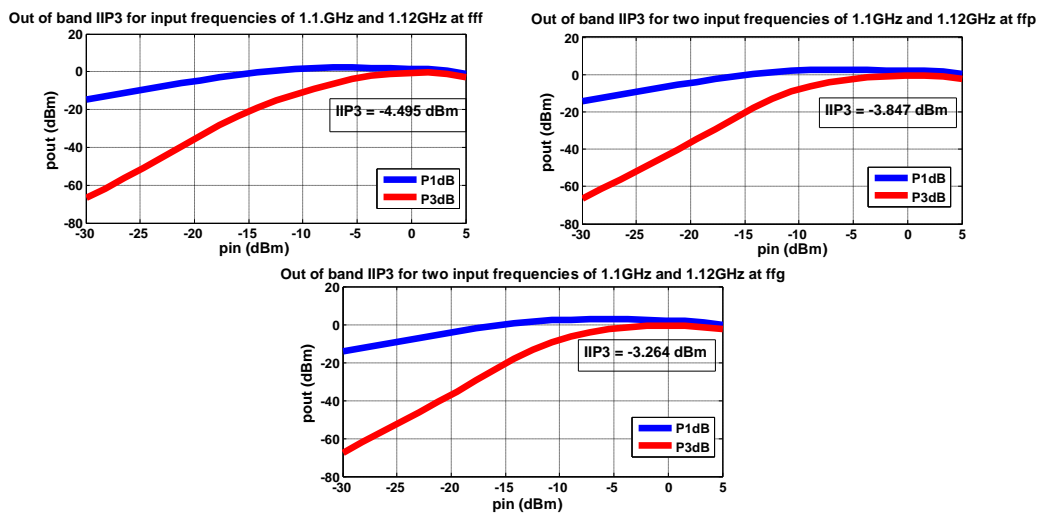Fig.5.58 Out of band IIP3 for input frequencies of 1.1GHz and 1.12GHz at fsf and fsg

Out-of-bandP1dB of the proposed architecture for input frequency of 1.1 GHz   is -17.679 dBm at fsf and -16.543 dBm at fsg as shown in Fig.5.59.

Out of band p1dB for input frequencies of 1.1GHz at fsf

P1dB = -17.679 dBm

Out of band P1dB for input frequency of 1.1GHz at fsg

P1dB = -16.543 dBm

Fig.5.59Out-of-band P1dB for input frequency of 1.1GHz at fsf and fsg

5.5.8. In -band P1dB and IIP3 for 1GHz input frequency at all process corners
In this section, the in-band P1dB of the proposed architecture for input frequency of 1.001GHz and in band IIP3 for two input frequencies of 1.001GHz and 1.003 GHz are shown across all the process corners in three different conditions f, p and g.

5.5.8.1.   *In-band P1dB and IIP3 for 1GHz input frequency at fff, ffp and ffg*
In-band IIP3 of the proposed architecture for inputs of 1.001 GHz and 1.003GHz is -5.365 dBm at fff, -4.786 dBm at ffp and -4.227 dBm at ffg as shown in Fig.5.60.

Fig.5.60In band IIP3 for input frequencies of 1.001GHz and 1.003GHz at fff, ffp and ffg

In-band P1dB of the proposed architecture for input frequency of 1.001 GHz is -14.962dBm at fff, -14.447 dBm at ffp and -14.543 dBm at ffg as shown in Fig.5.61.
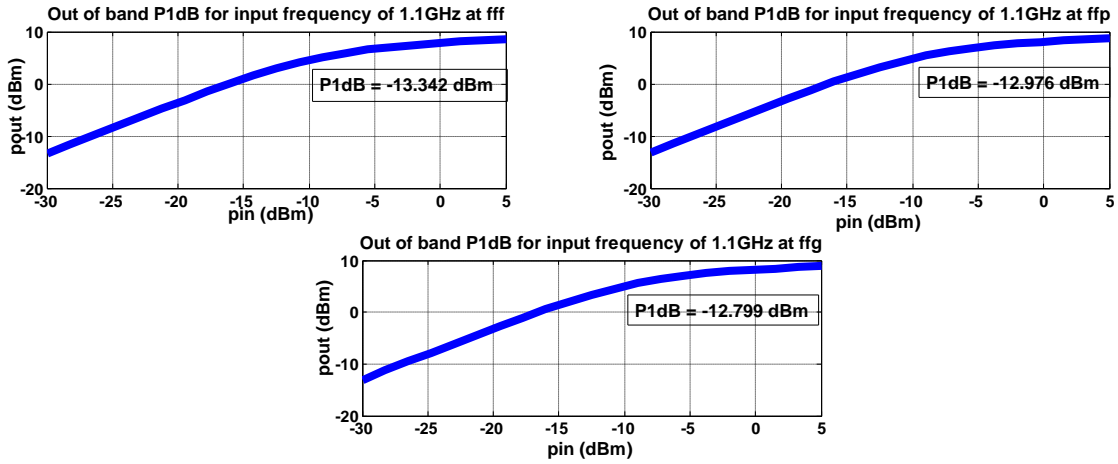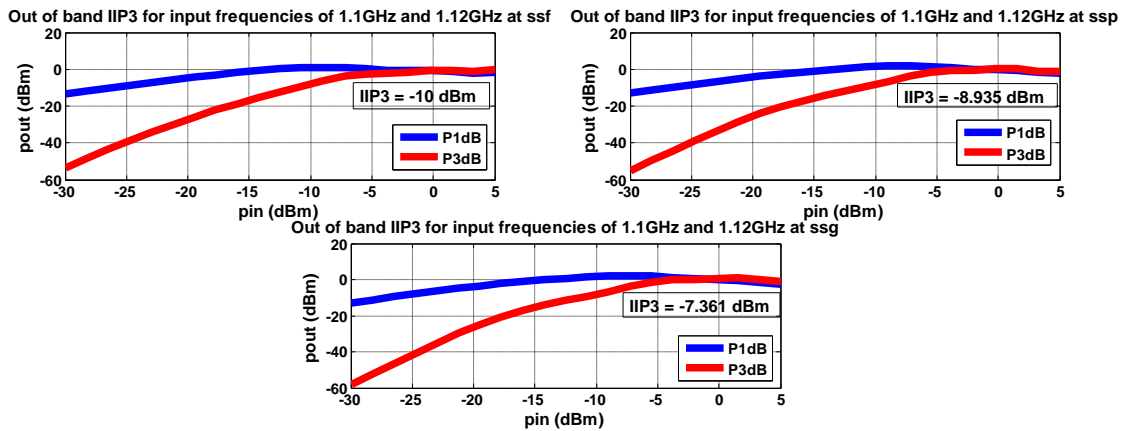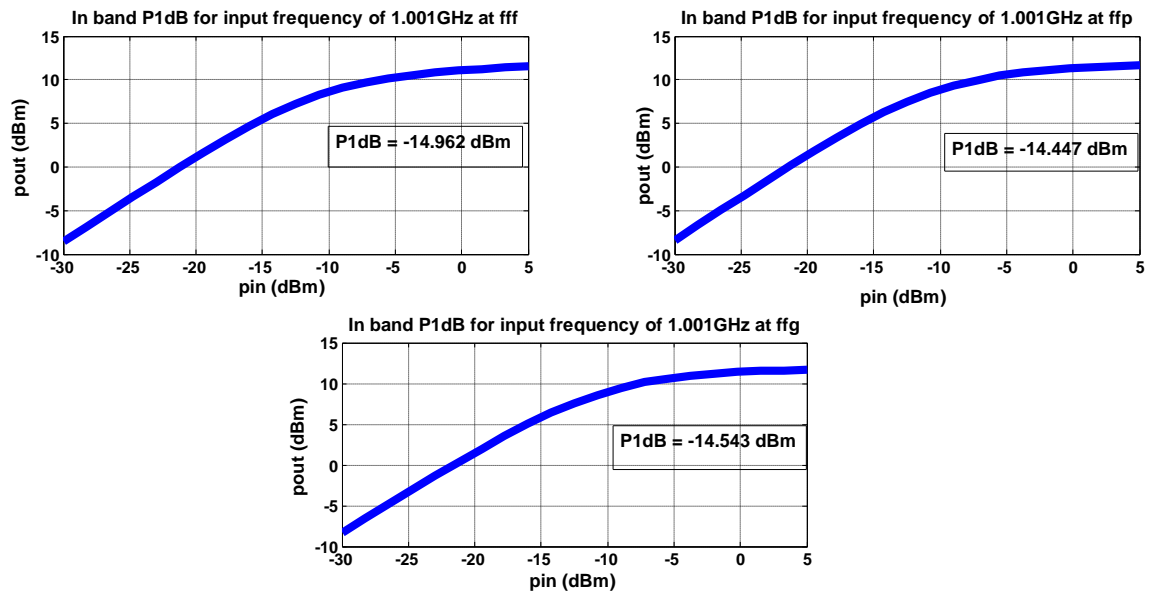

Fig.5.61In band P1dB for input frequency of 1.001GHz at fff, ffp and ffg

5.5.8.2. *In -band P1dB and IIP3 for 1GHz input frequency at ssf, ssp and ssg*

In-band IIP3 of the proposed architecture for inputs of 1.001 GHz and 1.003GHz is -12.323 dBm at fff, -12.27 dBm at ffp and -10.58 dBm at ffg as shown in Fig.5.62.

Fig.5.62In band IIP3 for input frequencies of 1.001GHz and 1.003GHz at ssf, ssp and ssg

In-band P1dB of the proposed architecture for input of 1.001 GHz is -19.971dBm at ssf, -20.507 dBm at ssp and -19.883dBm at ssg as shown in Fig.5.63.
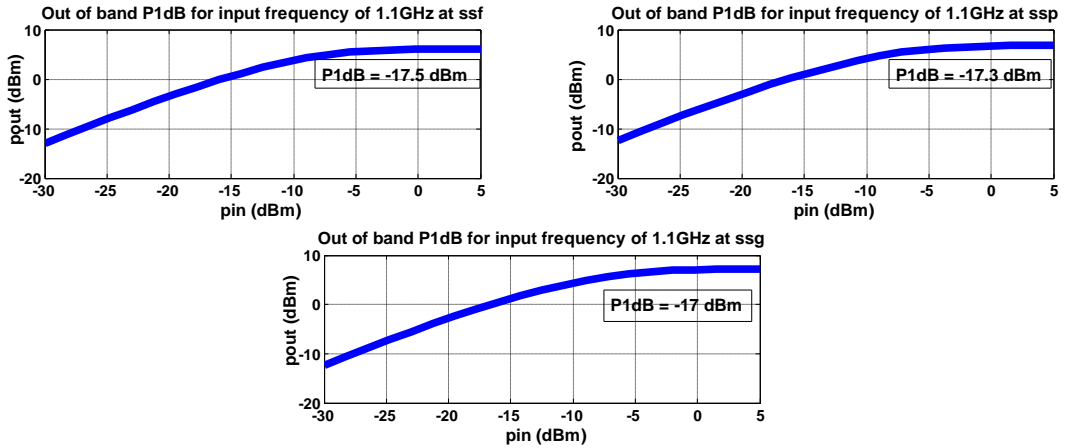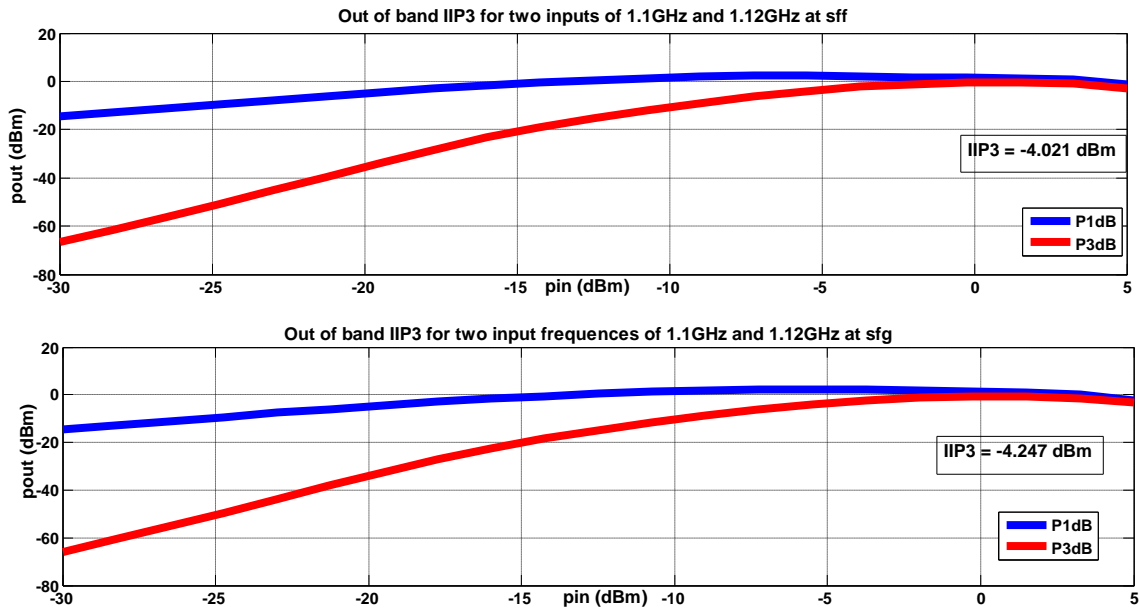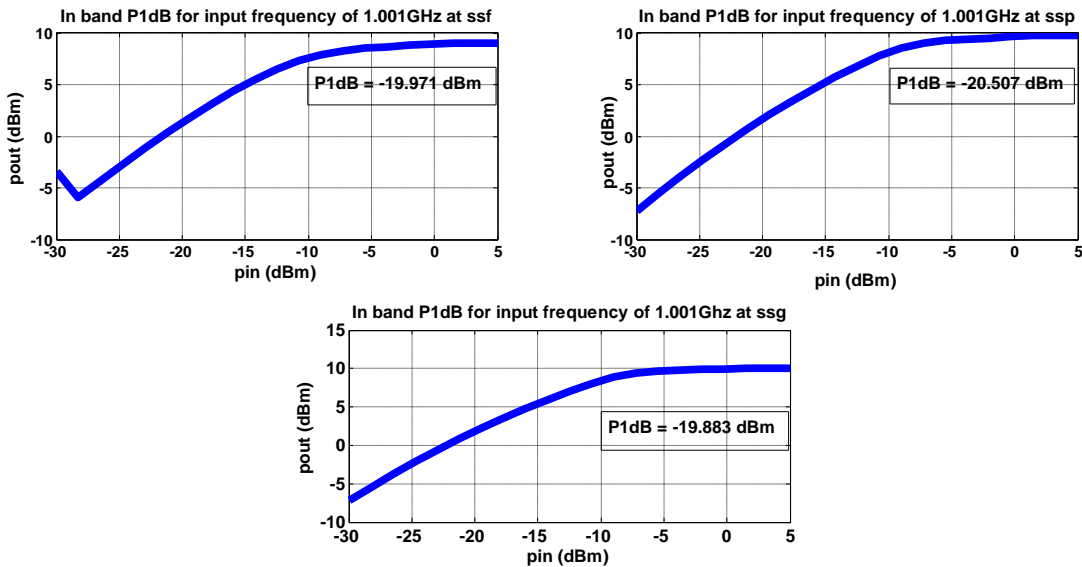

Fig.5.63In band P1dB for input frequency of 1.001GHz at ssf, ssp and ssg

5.5.8.3. *In-band P1dB and IIP3 for 1GHz input frequency at fsf and fsg*

In-band IIP3 of the proposed architecture for inputs of 1.001 GHz and 1.003GHz is -12.96 dBm at fsf and -9.596 dBm at fsg as shown in Fig.5.64.
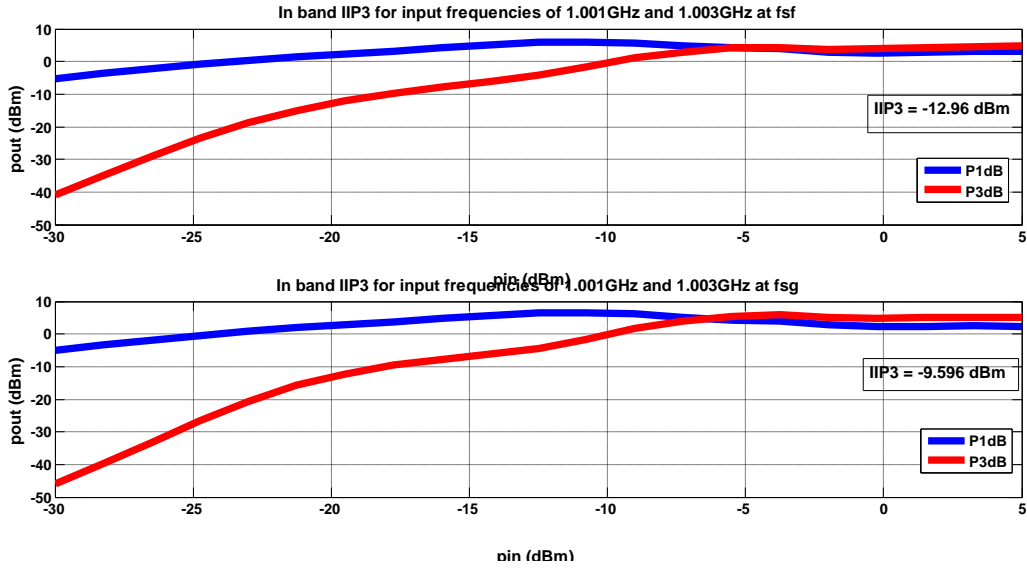
Fig.5.64In band IIP3 for input frequencies of 1.001GHz and 1.003GHz at fsf and fsg

In-band P1dB of the proposed architecture for input of 1.001 GHz is -21.317 dBm at fsf and -20.252 dBm at fsg as shown in Fig.5.65.
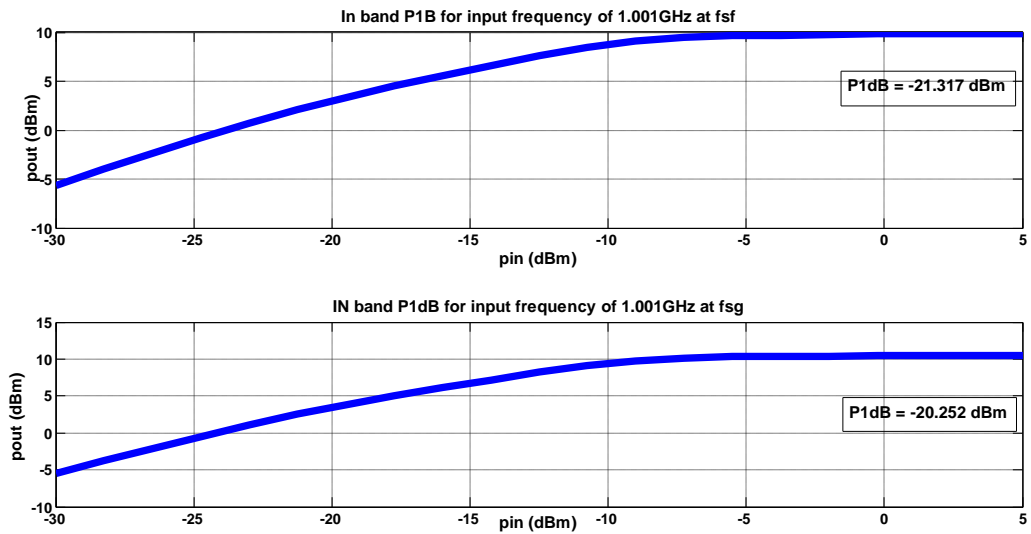
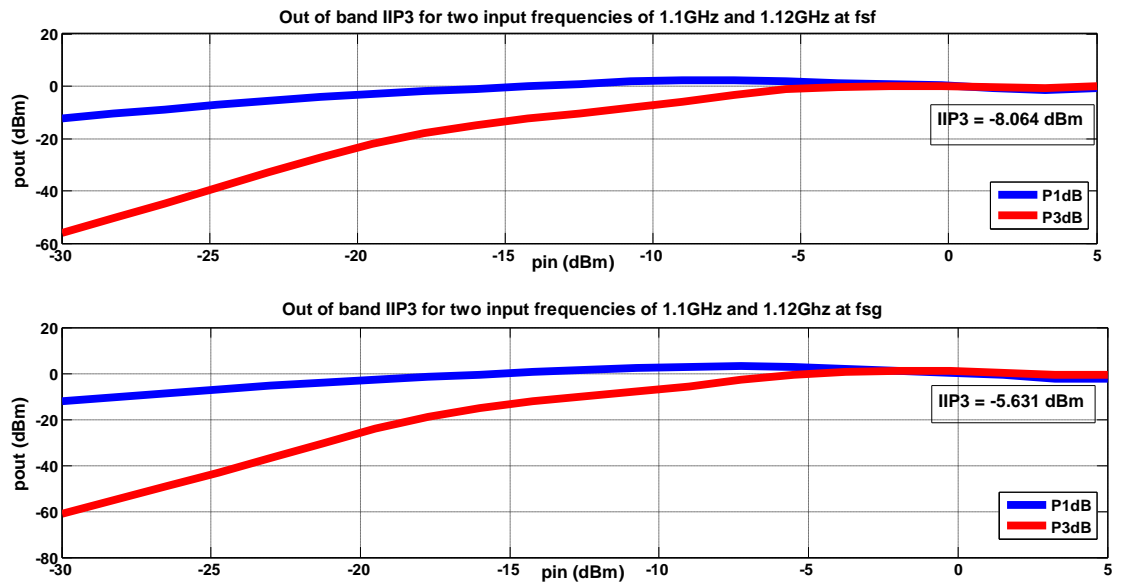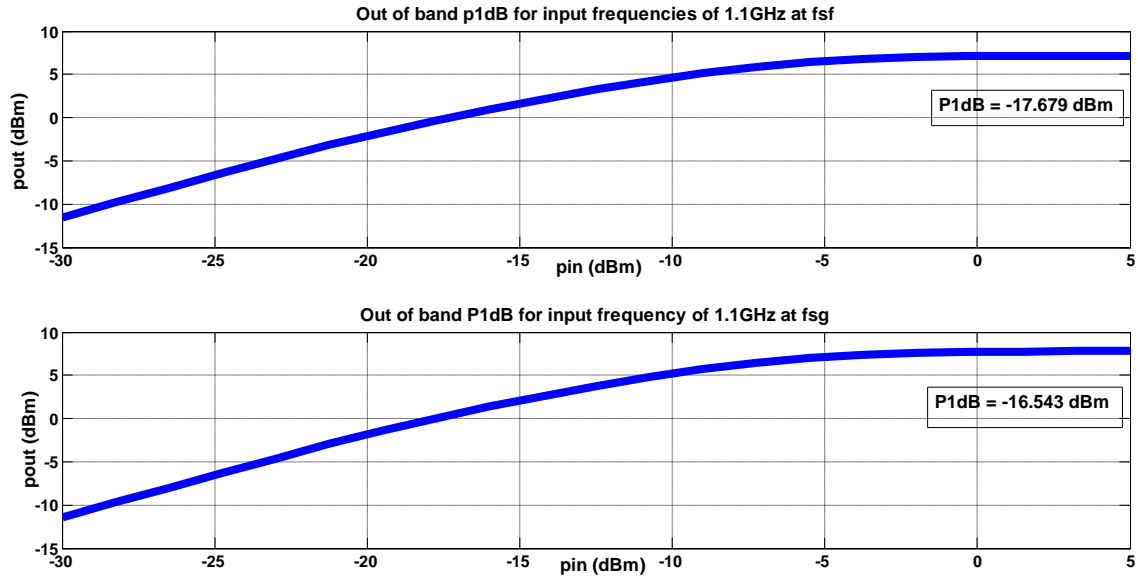Fig.5.65In band P1dB for input frequency of 1.001GHz at fsf and fsg

5.5.8.4. *In -band P1dB and IIP3 for 1GHz input frequency at sff and sfg*

In-band IIP3 of the proposed architecture for inputs of 1.001 GHz and 1.003GHz is -4.459 dBm at sff and -4.977 dBm at sfg as shown in Fig.5.66.
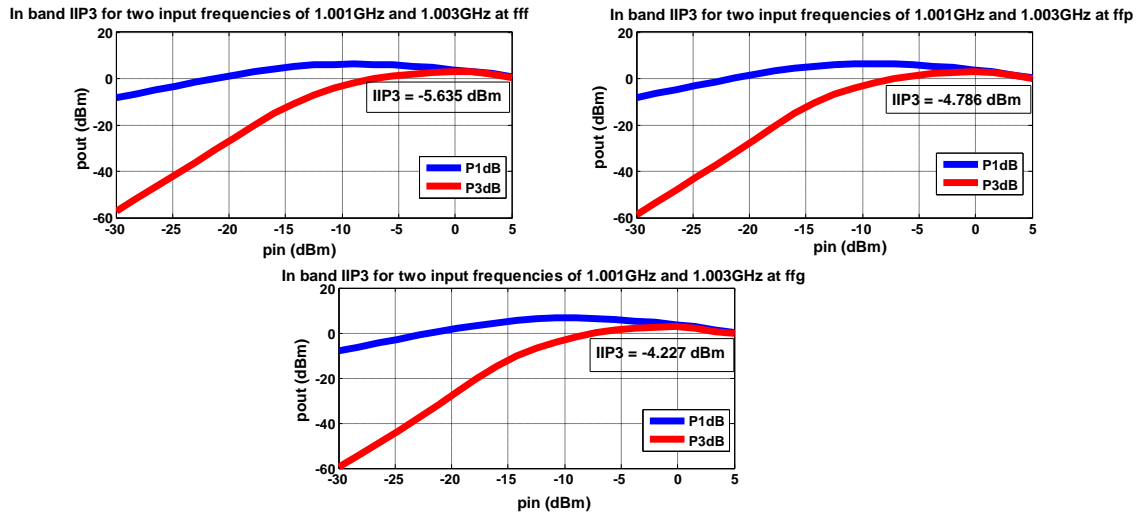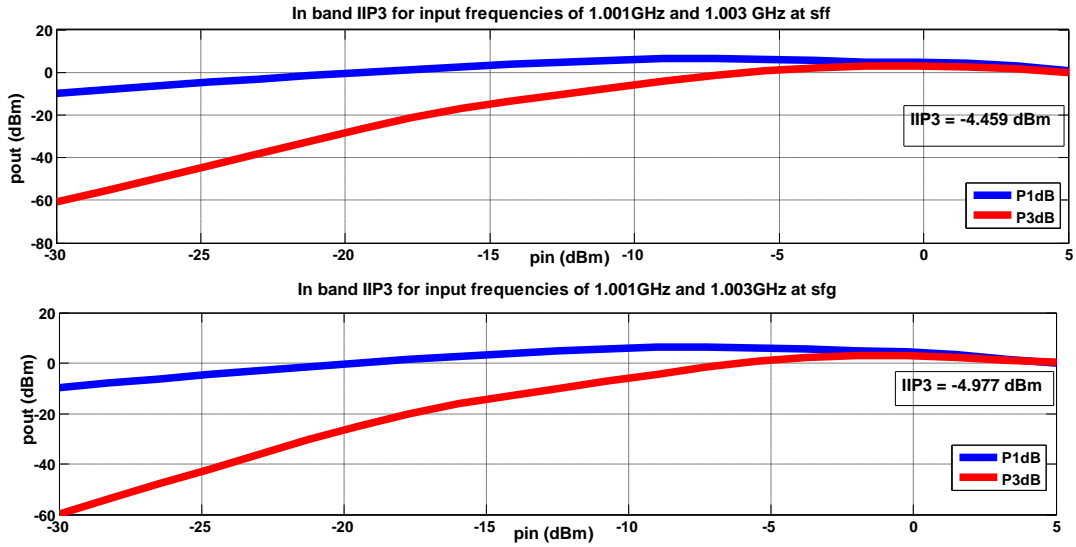

Fig.5.66In band IIP3 for input frequencies of 1.001GHz and 1.003GHz at sff and sfg

In-band P1dB of the proposed architecture for input of 1.001 GHz is -14.682 dBm at sff and -15.446 dBm at sfg as shown in Fig.5.67.
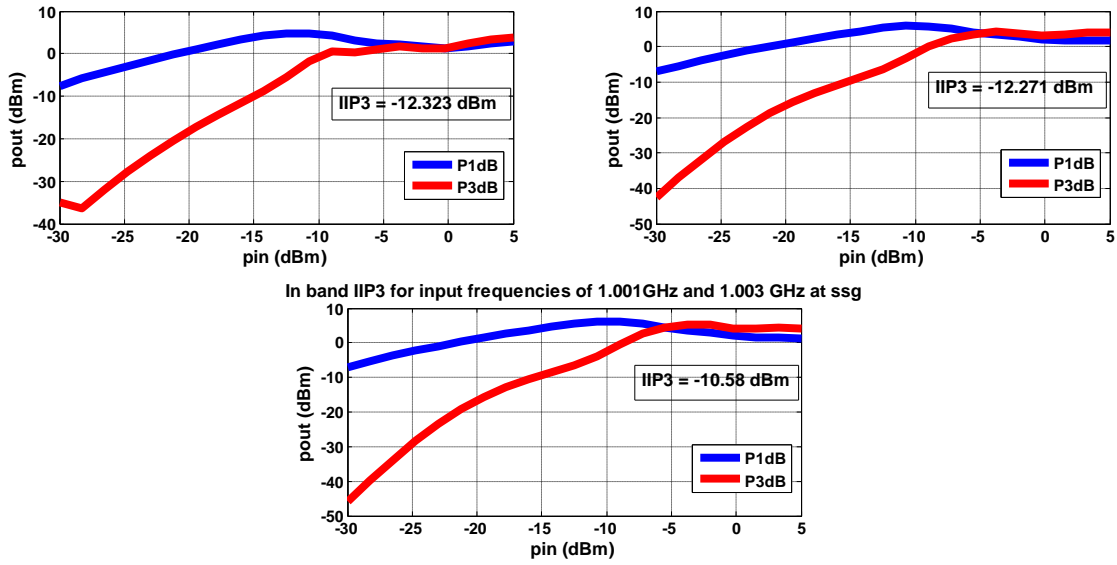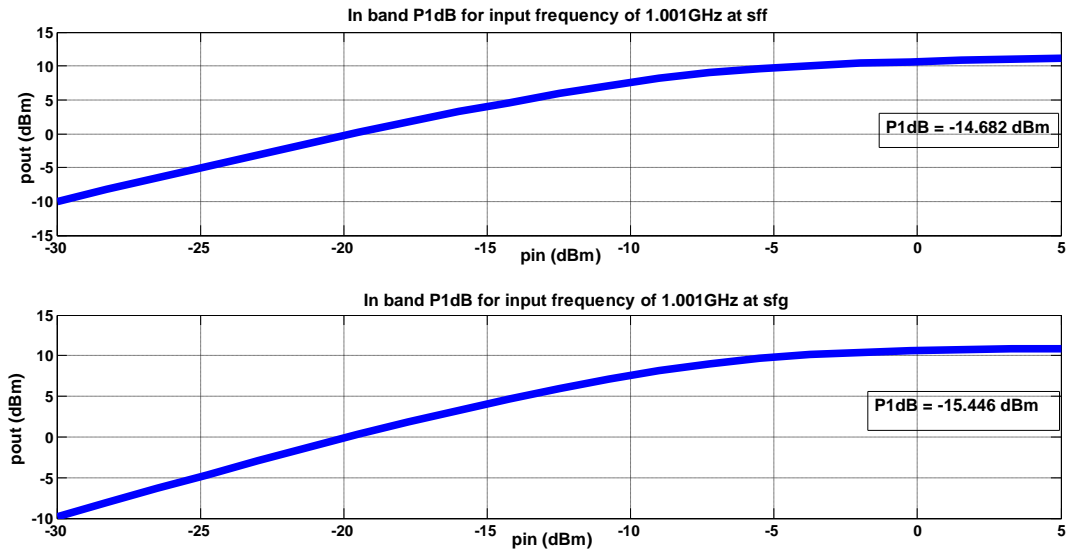

Fig.5.67In band P1dB for input frequency of 1.001GHz at sff and sfg

6. Layout and post layout simulations

In this chapter the layout of the design with its blocks are shown and each block is tested post layout with the rest of the blocks in schematic view due to the difficulty of simulating the whole system post layout. The layout of the whole design is shown in Fig.6.1. It consumes $0.45mm^2$ (870u X 540u).

First the layout of different blocks is shown then testing the transconductor post layout with the integration switches and matching network in schematic views after that the integration switches and the matching network are post layout with the transconductor in schematic view. Each time NF, S11, in band and out of band IIP3 are measured.
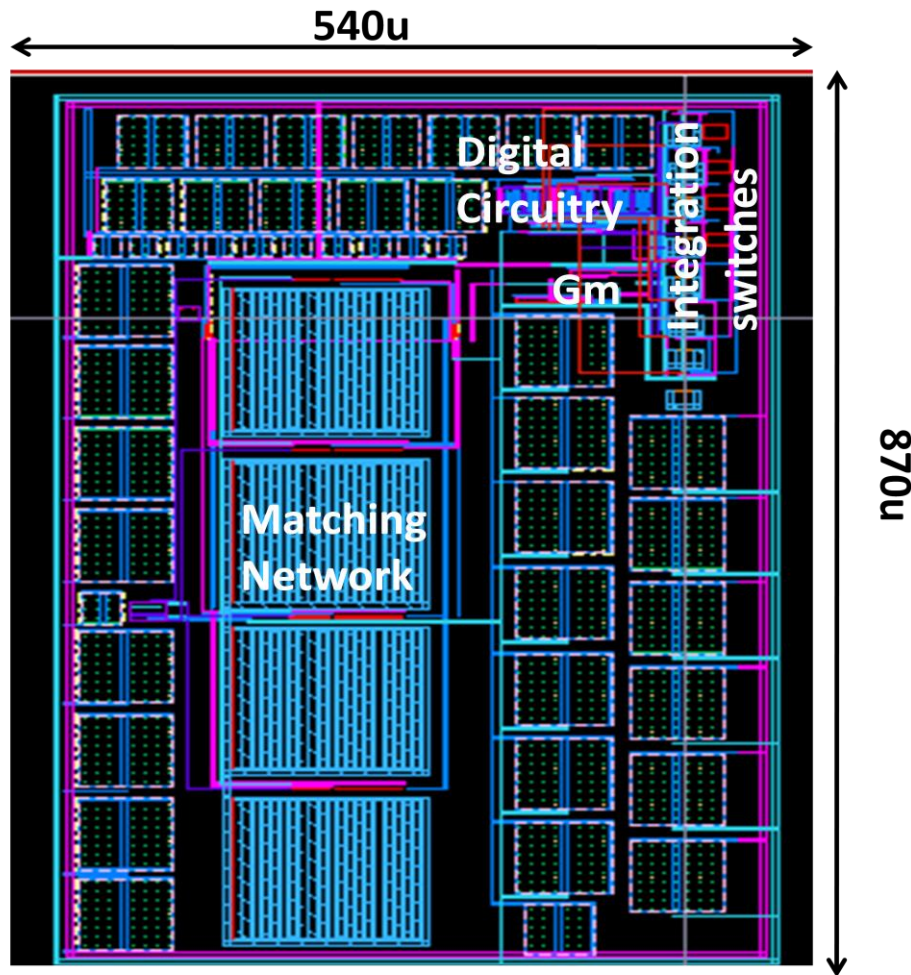
Fig.6.1 The whole design layout

6.1.Layout of different blocks

6.1.1. Layout of the transconductor (G_m)

Layout of the transconductor is shown in Fig.6.2, the design is differential so matching is very important, that's why large width transistors are divided to many fingers and they are inter-digitated.

What affects the design here is the parasitic resistance as most of the current is lost in it, so the routing is done using thick metal. The area of the transconductor is (116u * 45u).
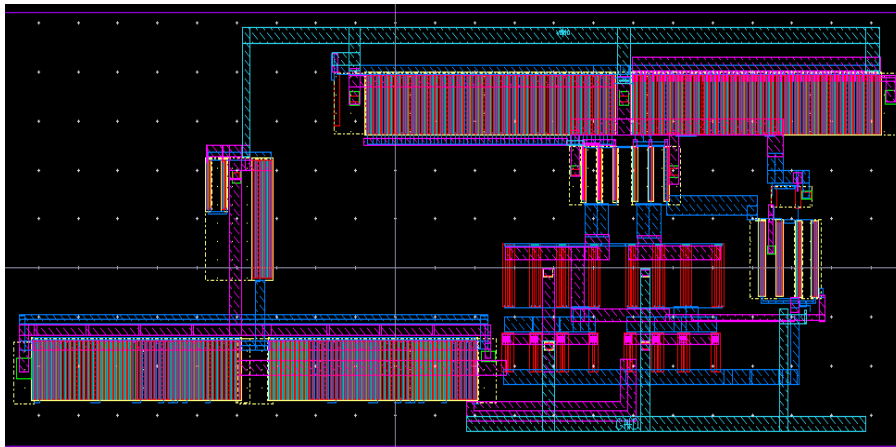
Fig.6.2 Layout of the transconductor (G_m)

6.1.2. Layout of the integration switches

The layout of the integration, sampling-to-output, discharging switches and the sampling capacitances is shown in Fig.6.3 The area of this block is (307u*75u). The sampling capacitance using mim caps consumes most of the area.

Fig.6.3 Layout of the integration switches

6.1.3. Layout of the matching network (MN)

The sizes of the matching network switches increase after layout as the effective base band resistance after layout increases due to the effect of the parasitic resistance, so the width of the transistors increases to consequently reduces the switch resistance to compensate this effect. The layout of the matching network is shown in Fig.6.4. The area of the matching network is (715u * 217u), the base band capacitance using mim caps consume most of the area.
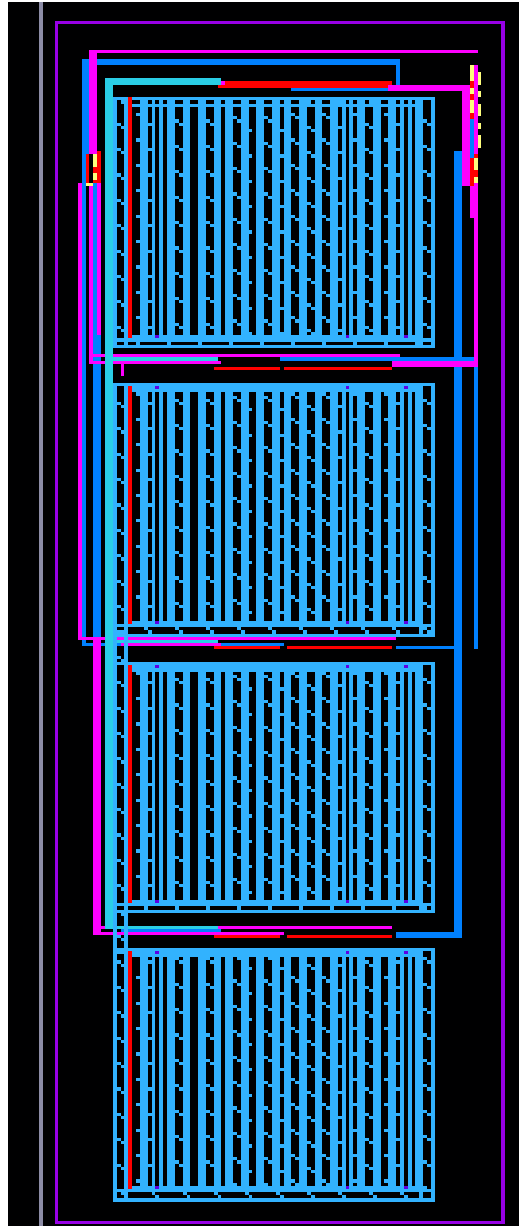
6.4 Layout of the matching network

6.1.4. Layout of the digital circuitry

The layout of the digital circuitry generating the charge sampler's and the time varying matching network clocks is shown in Fig.6.5. The circuit generating the matching network clocks is made of short length devices so it is easier in supporting higher frequencies than that is generating the charge sampler's clocks which are made of I/O devices. Due to the effect of the parasitic capacitance, the sizes of the transistors increase after layout in order to be able to drive the proceeding stages.
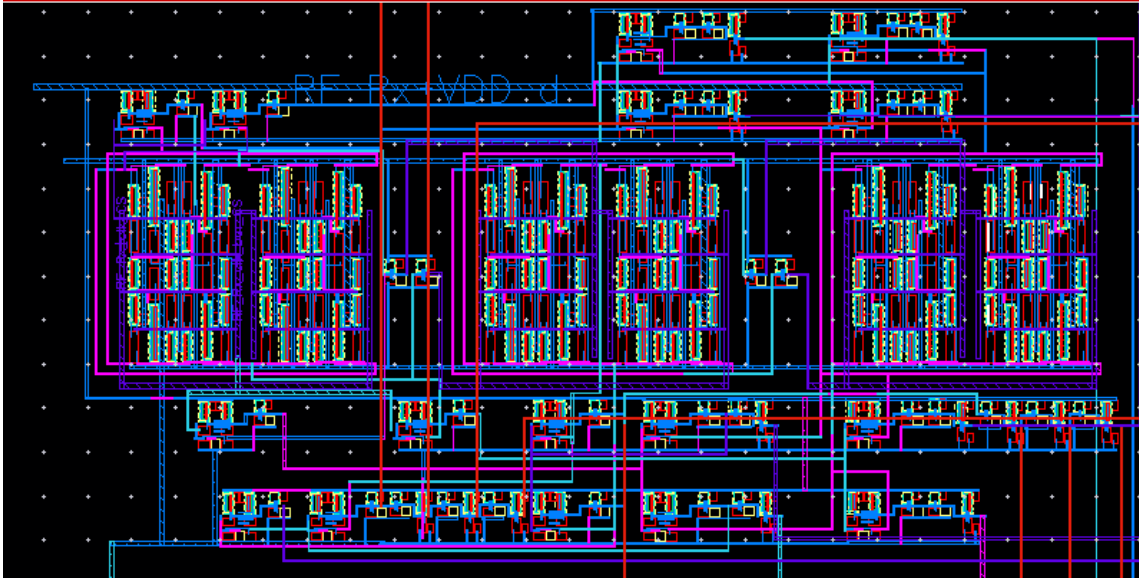
6.5 Layout of the digital circuitry

6.2.Post layout simulation of different blocks

In this section each block is tested post layout with the other blocks in schematic view and that is due to the difficulty of simulating the whole system post layout and the specs of noise figure, matching, in band and out of band linearity are checked at each time.

6.2.1. Post layout simulation of transconductor (G_m)

Testing the transconductor post layout with the integration switches and the matching network in schematic views for two different frequency bands 1GHz and 2GHz results in noise figure of 8.3 dB as shown in Fig.6.6, S11 of -11.5 dB as shown in Fig.6.7 at 2GHz frequency band, out-of-band IIP3 of -4.436 dBm for input frequencies of 2.1GHz and 2.12GHz as shown in Fig.6.8 and in-band IIP3 of -7.18 dBm for input frequencies of 2.001GHz and 2.003GHz as shown in Fig.6.9, NF of 8.5 dB as shown in Fig.6.10, S11 of -10 dB as shown in Fig.6.11 at 1GHz, out-of-band IIP3 of -7.992 dBm for input frequencies of 1.1GHz and 1.12GHz as shown in Fig.6.12 and in-band IIP3 of -10 dBm for input frequencies of 1.001GHz and 1.003GHz as shown in Fig.6.13.

Fig.6.6 Noise Figure at 2GHz with G_m post layout

Fig.6.7 S11 at 2GHz with G_m post layout

Fig.6.8 Out-of-band IIP3 for input frequencies of 2.1GHz and 2.12GHz with G_m post layout
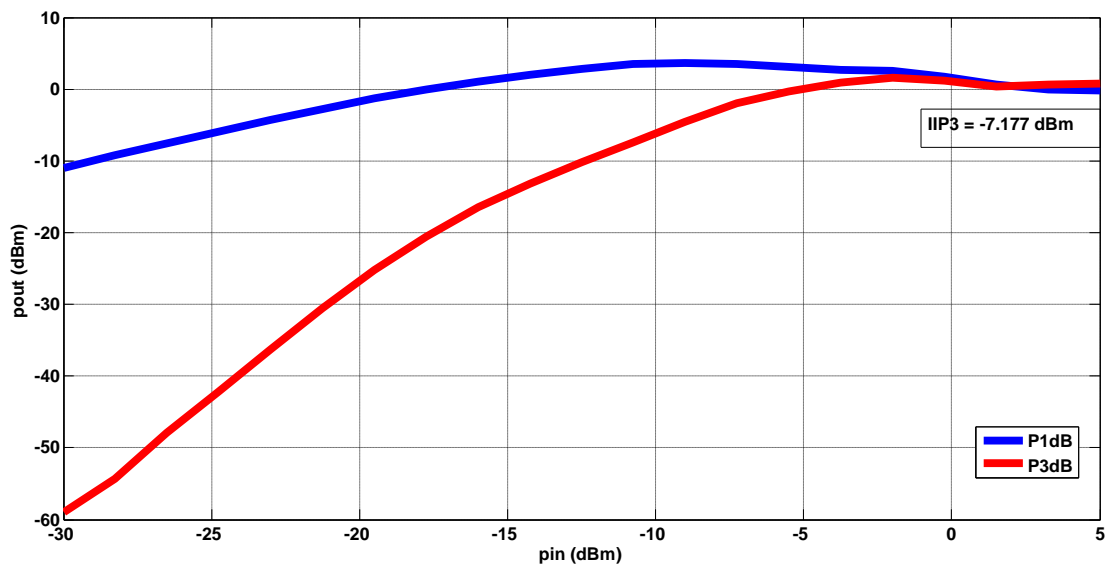
Fig.6.9 In-band IIP3 for input frequencies of 2.001GHz and 2.003GHz with G_m post layout

Fig.6.10 Noise Figure at 1GHz with G_m post layout
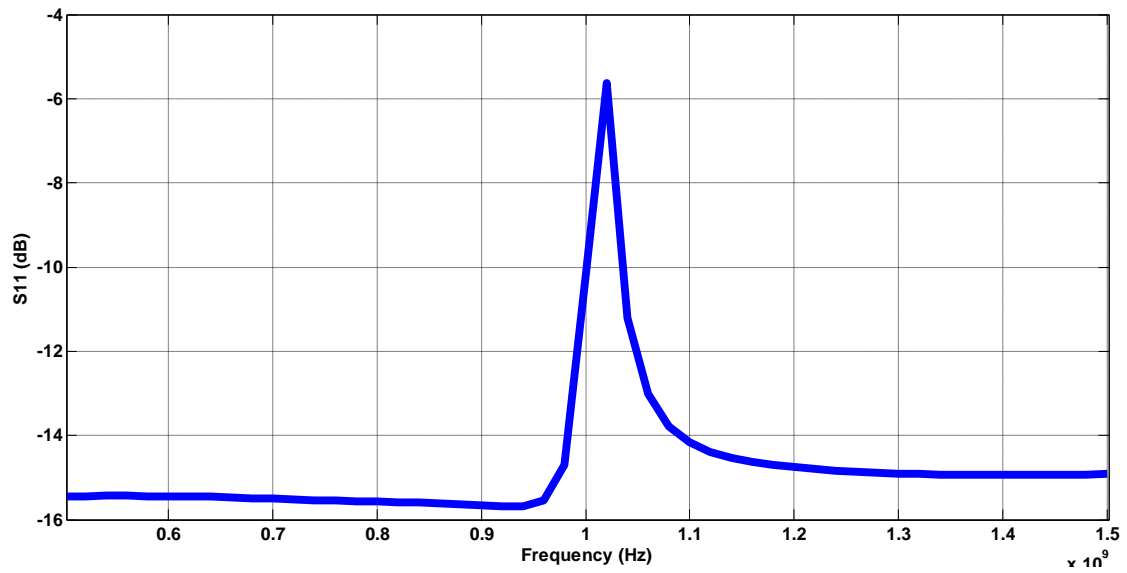
Fig.6.11 S11 at 1GHz with G_m post layout

Fig.6.12 Out-of-band IIP3 for input frequencies of 1.1GHz and 1.12GHz with G_m post layout
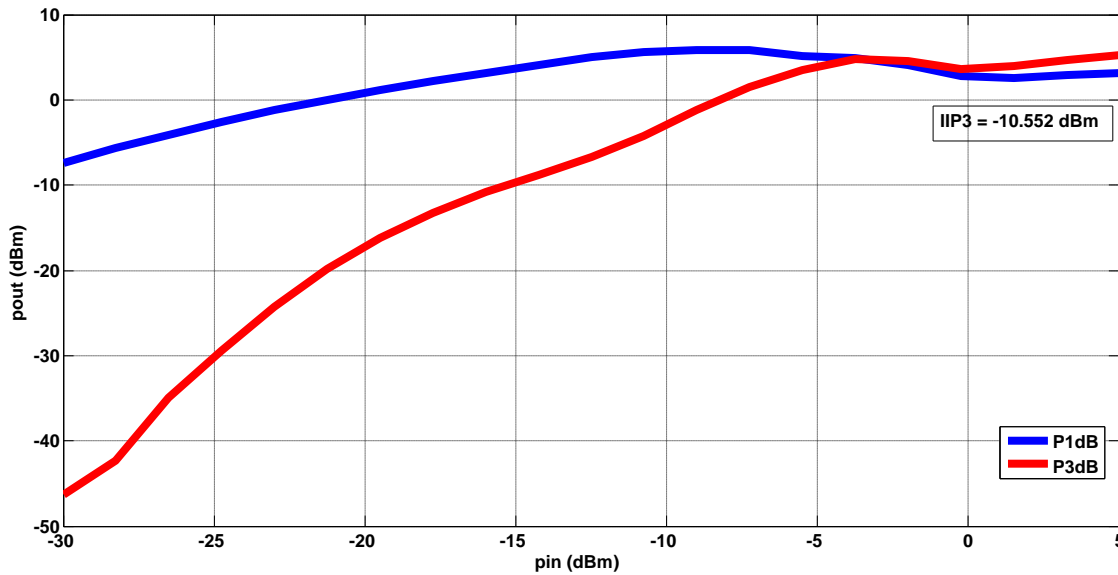
Fig.6.13 In-band IIP3 for input frequencies of 1.001GHz and 1.003 GHz with G_m post layout

6.2.2. Post layout simulation of the integration switches and matching network

Testing the switches and matching network post layout with the transconductor in schematic view results in Noise Figure of 7.9 dB as shown in Fig.6.14 and S11 of -9 dB as shown in Fig.6.15 at 2GHz frequency band, out-of-band IIP3 of -5.706 dBm for input frequencies of 2.1GHz and 2.12GHz as shown in Fig.6.16 and in-band IIP3 of -5.235

dBm for input frequencies of 2.001GHz and 2.003 GHz as shown in Fig.6.17, noise figure of 8.3 dB as shown in fig.6.18 and S11 of -9 dB as shown in Fig.6.19 at 1GHz frequency band, out-of-band IIP3 of -7.429 dBm for input frequencies of 1.1GHz and 1.12GHz as shown in Fig.6.20 and in-band IIP3 of -8.665 dBm for input frequencies of 1.001GHz and 1.003GHz as shown in Fig.6.21.
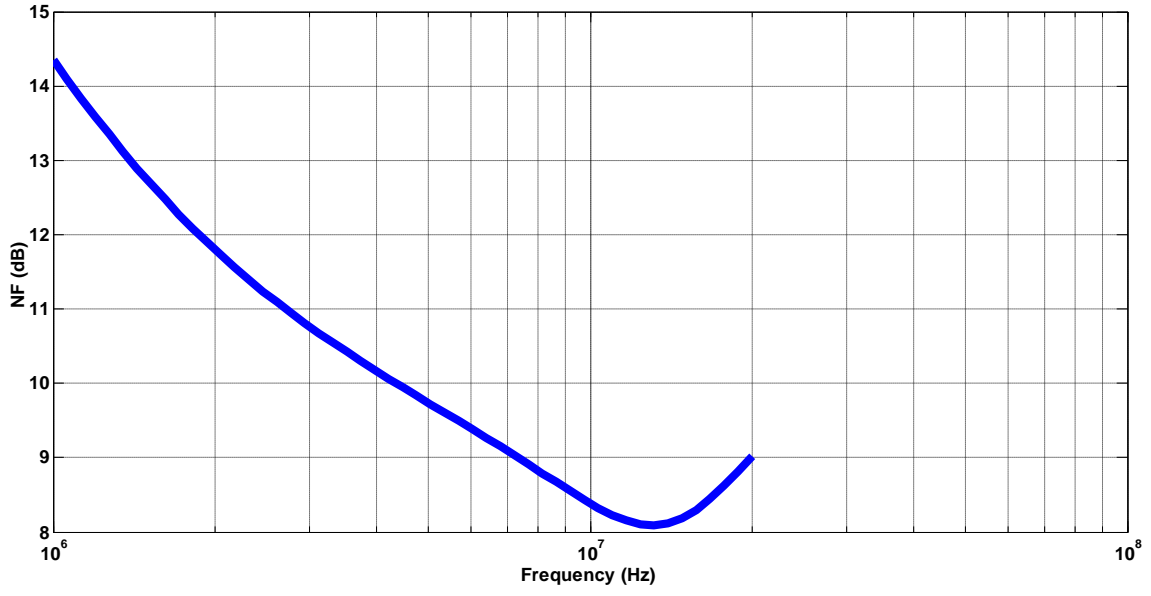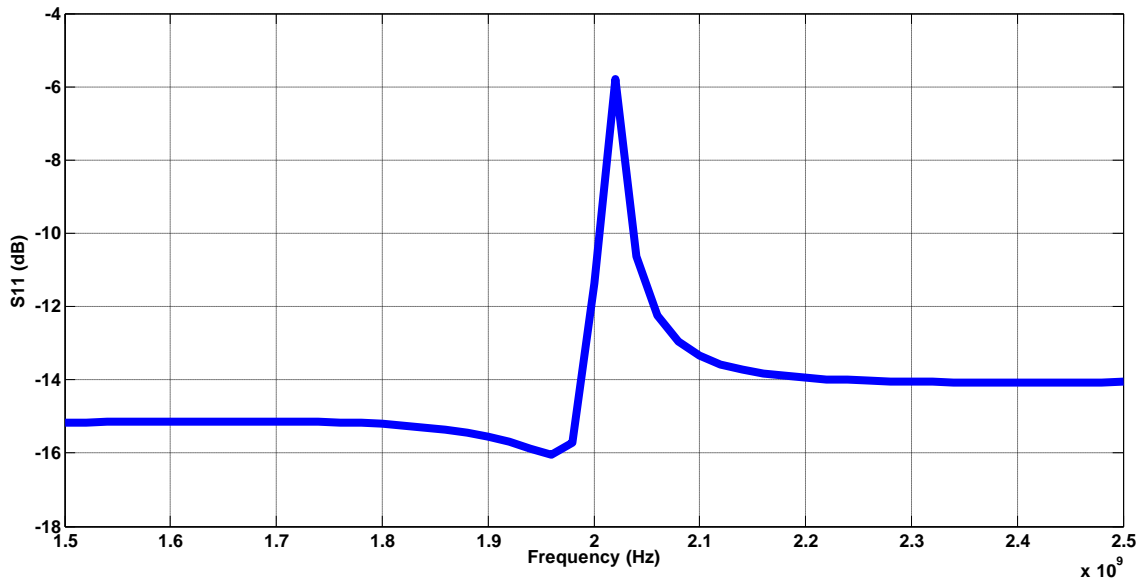

Fig.6.14 Noise Figure at 2GHz with switches and matching network post layout
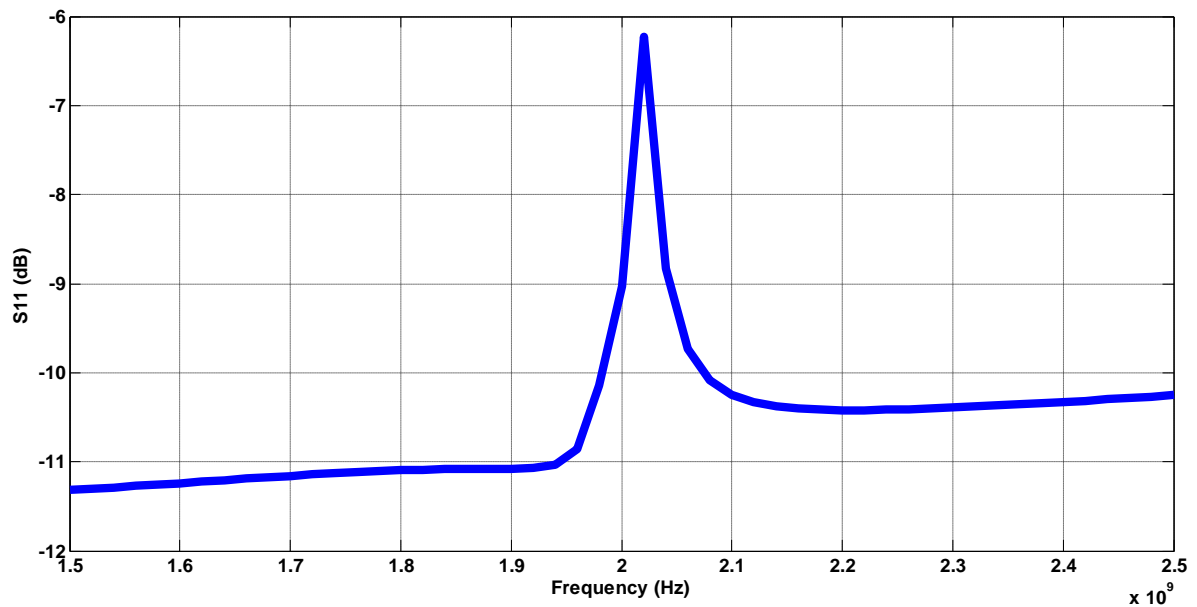
Fig.6.15 S11 at 2GHz with switches and matching network post layout
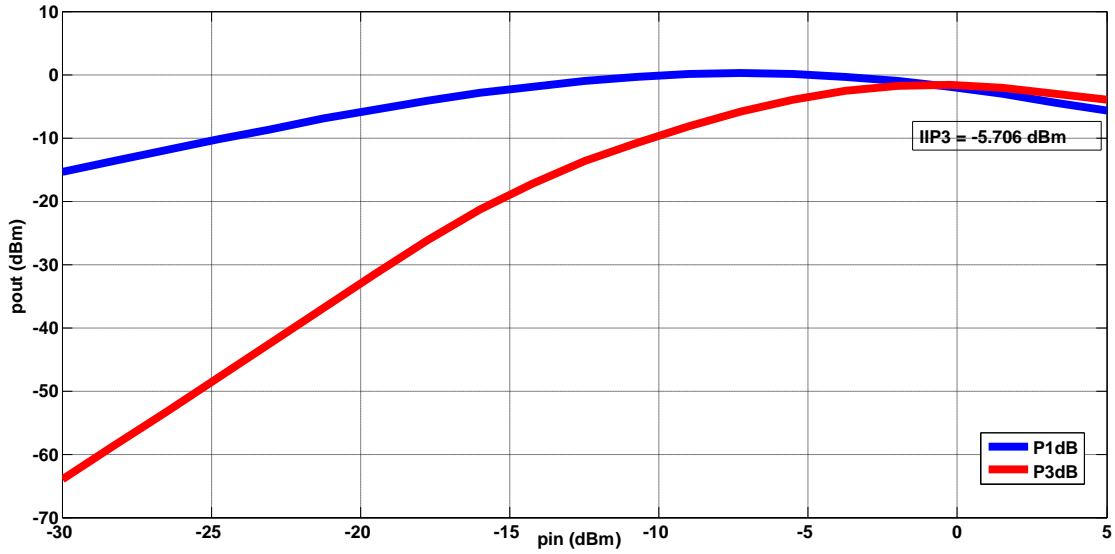
Fig.6.16 Out-of-band IIP3 for input frequencies of 2.1GHz and 2.12GHz with switches and MN post layout
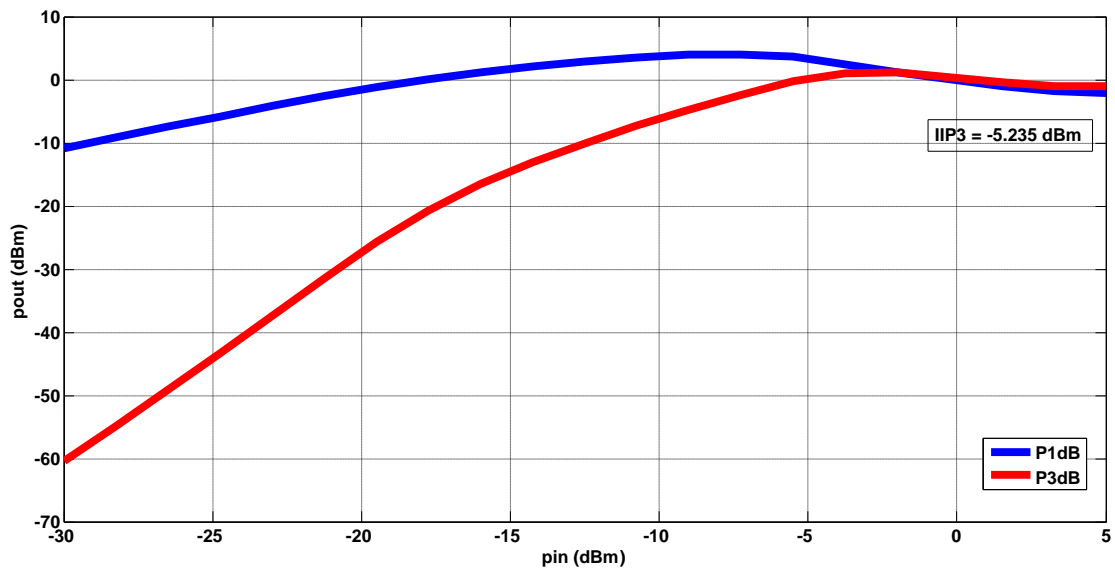
Fig.6.17 In-band IIP3 for input frequencies of 2.001GHz and 2.003 GHz with switches and matching network post layout

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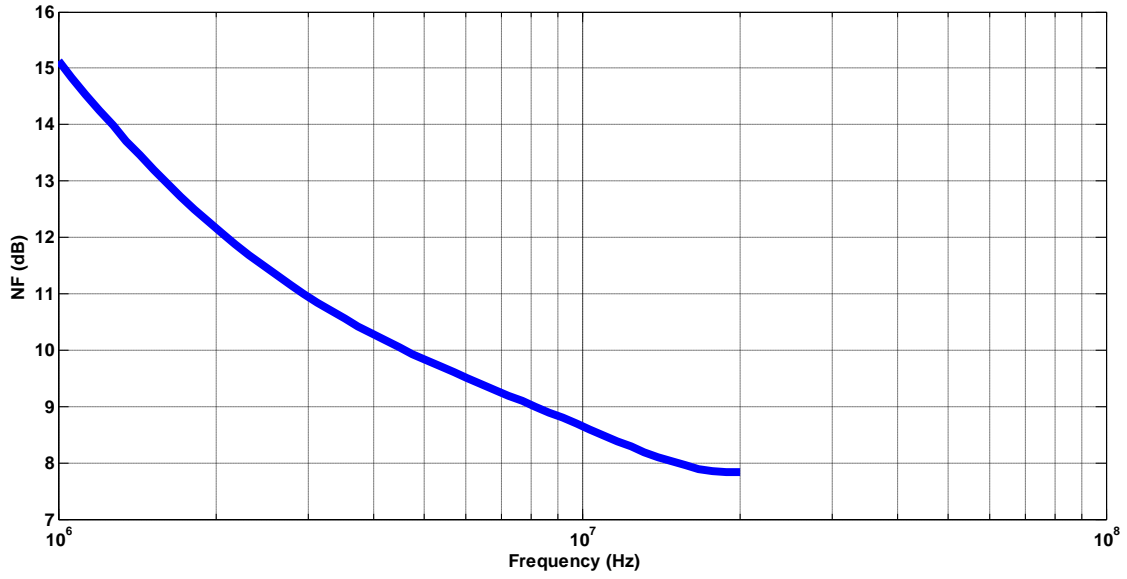
Fig.6.18 Noise Figure at 1GHz with switches and matching network post layout
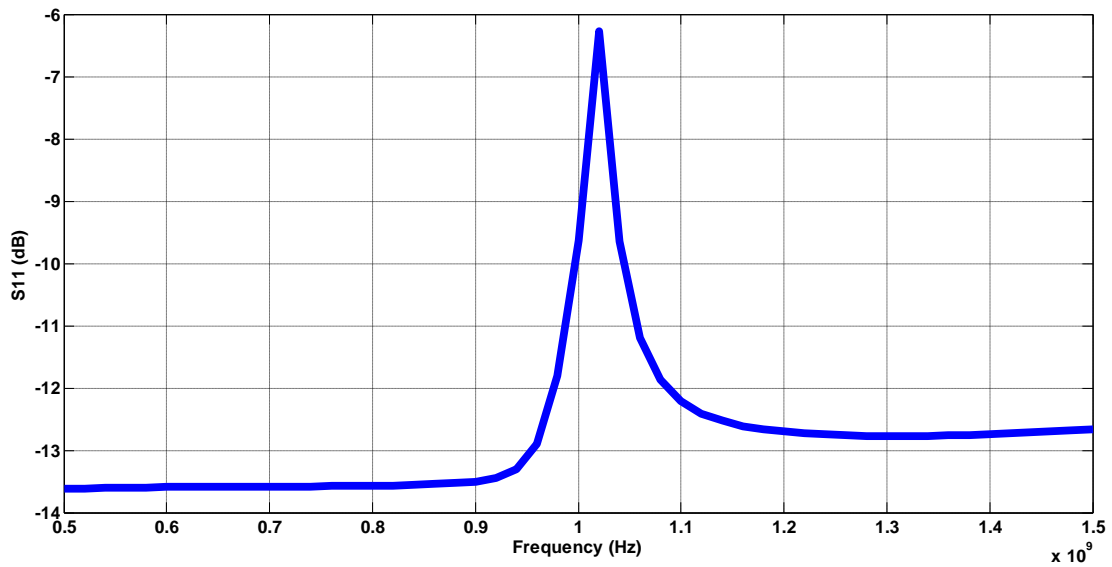
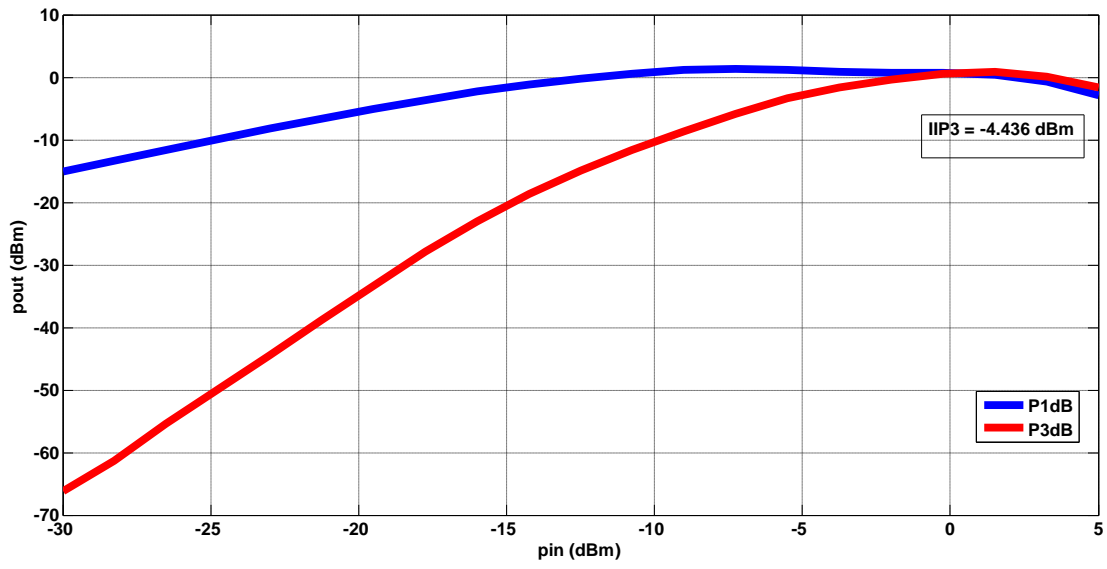Fig.6.19 S11 at 1GHz with switches and matching network post layout
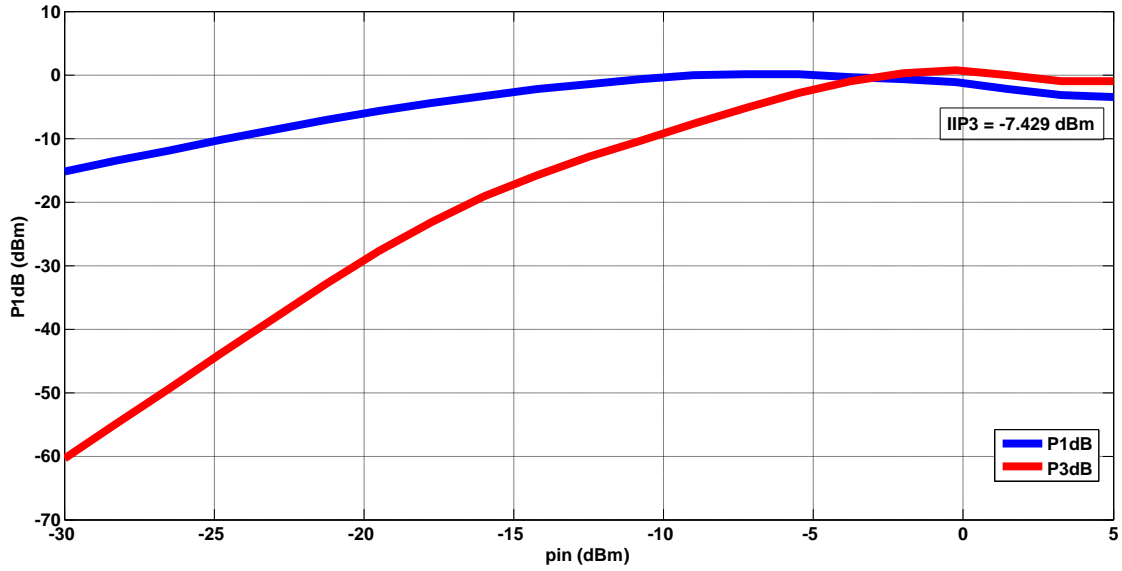
Fig.6.20 Out-of-band IIP3 for input frequencies of 1.1GHz and 1.12GHz with switches and MN post layout

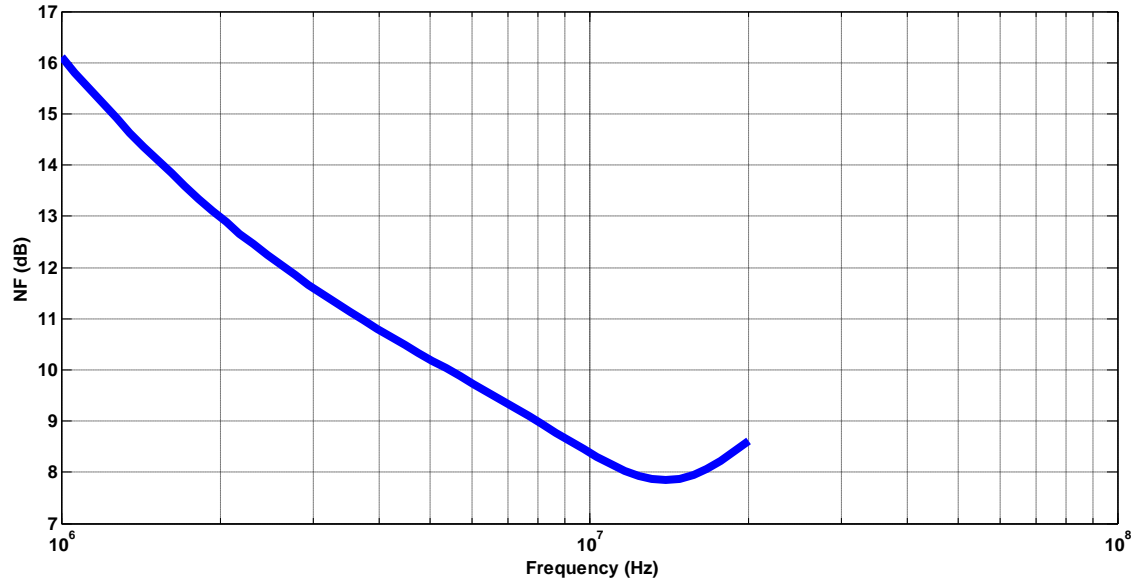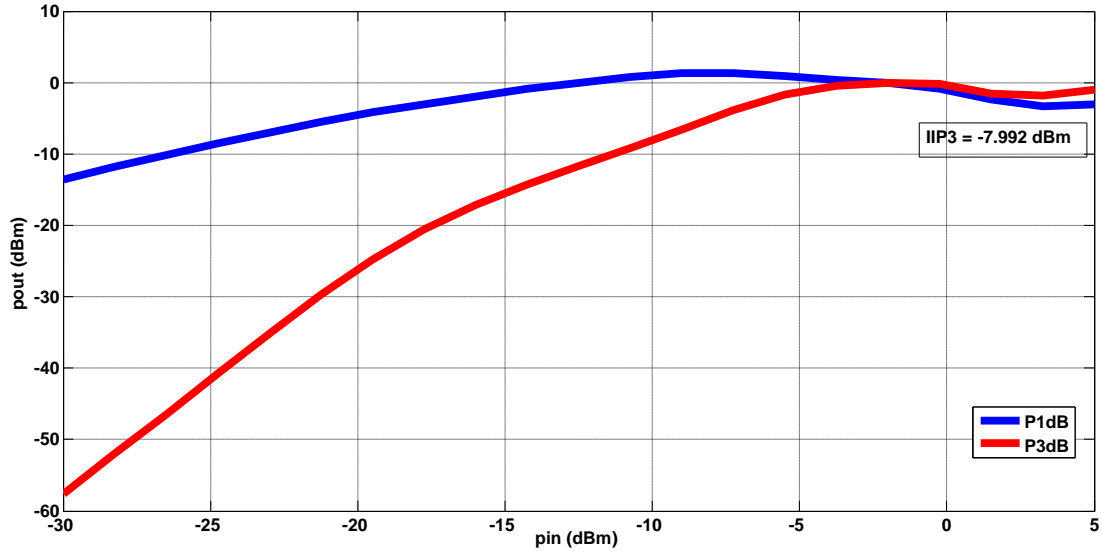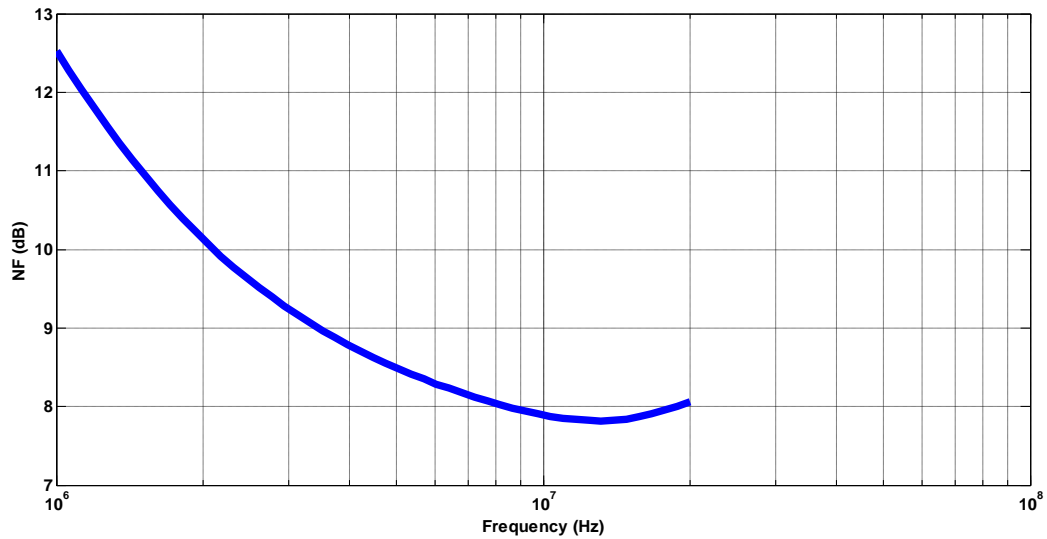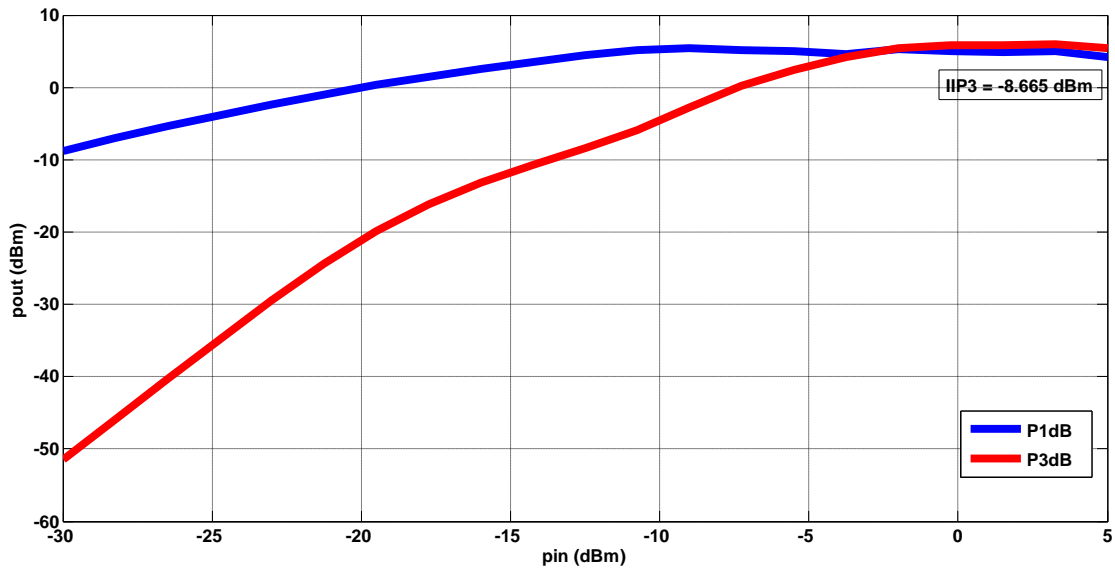Fig.6.21 In-band IIP3 for input frequencies of 1.001GHz and 1.003 GHz with switches and matching network post layout

6.3. Comparison between pre and post layout simulations

Pre and post layout results for 2GHz frequency are compared in Table 6-1 and for 1GHz frequency are compared in Table 6-2. As it is clear from the comparison below; the noise figure with post layout transconductor increases due to the decrease of the current consumed in it due to the effect of the parasitic resistances. Linearity also depends on the passing current that's why it decreases with the post layout transconductor. For post layout switches and the matching network, the matching is affected due to the effect of the parasitic resistances and capacitances and also the linearity is deteriorated as the matching network selectivity will be affected with the parasitic resistances and capacitances.

	All schematic	G_m post layout + rest schematic	Integration_switches + MN post layout
NF (dB)	7.8	8.3	7.9
S11 (dB)	-10	-11.5	-9
Out of band IIP3 (dBm)	-1.9	-4.436	-5.706
In band IIP3 (dBm)	-1.45	-7.18	-5.235

Table 6-1 Comparison between pre and post layout simulations at 2GHz

	All schematic	G_m post layout + rest schematic	Integration_switches + MN post layout
NF (dB)	7.9	8.5	8.3
S11 (dB)	-10	-10	-9
Out of band IIP3 (dBm)	-3	-7.992	-7.429
In band IIP3 (dBm)	-4.349	-10	-8.665

Table 6-2 Comparison between pre and post layout simulations at 2GHz

7. Conclusion

The aim of this work is to implement a programmable receiver front end controlled by adjusting the controlling clocks of the receiver's blocks to be able to receive different frequency bands. By controlling the clocks of the charge sampler (the integration pulse width) and the clocks of the time varying matching network, the receiver is able to receive a certain frequency band.

The proposed front-end architecture target is to achieve LTE specifications of noise figure, in band and out of band linearity on the frequency range of (700MHz – 2.4GHz) as a case study. The architecture is tested over three different frequencies 500MHz, 1GHz and 2GHz and the receiver's specs are checked at each frequency to prove the programmability of the proposed architecture.

This receiver solves the problem of moderate linearity and poor matching in sampling receivers and wide-band receivers.

The receiver achieves better linearity than the other wide-band designs as in this design; the receiver's linearity is controlled by the transconductor and is more enhanced by the time varying matching network selectivity.

This design has better matching than other designs. Matching is based on a programmable matching network instead of a wide-band one. Good matching can be held at multi-bands.

Targeting other wireless communications standards is considered as a future work. This design can receive any frequency band of any standard. By adjusting the controlling clocks of the design, the band pass filter response and the matching are held at the desired frequency. By adjusting the number of integrated samples (N), the sampling capacitance (C_s), the receiver's gain is controlled consequently the receiver's noise and linearity according to the required specs. Adjusting the resistances and capacitances values in the matching network controls the matching, noise and linearity due to its further selectivity.

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