DESIGN OF READ/WRITE CIRCUITS SUITABLE FOR MEMRISTOR-BASED MEMORY ARRAYS

By

Mohamed Sayed Ahmed Mohamed Elshamy

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2014

DESIGN OF READ/WRITE CIRCUITS SUITABLE FOR MEMRISTOR-BASED MEMORY ARRAYS

By

Mohamed Sayed Ahmed Mohamed Elshamy

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications

Under the Supervision of

Prof. Dr. Mohamed Sameh Saied

Professor of Electronics

Electronics and Communications Department

Faculty of Engineering, Cairo University

Dr. Hassan Moustafa Hassan

Doctor of Electronics

Electronics and Communications Department

Faculty of Engineering, Cairo University

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2014

DESIGN OF READ/WRITE CIRCUITS SUITABLE FOR MEMRISTOR-BASED MEMORY ARRAYS

By

Mohamed Sayed Ahmed Mohamed Elshamy

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications

Approved by the Examining Committee:

_____

Prof. Dr. Mohamed Sameh Saied, Thesis Main Advisor

_____

Prof. Dr. Mohamed Fathi, Internal Examiner

_____

Prof. Dr. Hassanein Amer Hamed, External Examiner

Professor of Electronics at Electronics and Communications Department
Faculty of Engineering, American University in Cairo (AUC)

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2014

Engineer's Name:	Mohamed Sayed Ahmed Mohamed Elshamy
Date of Birth:	21/3/1986
Nationality:	Egyptian
E-mail:	eng_melshamy@hotmail.com
Phone:	+2 0122 2589213
Address:	12, Alabour st., from Elbalsem, Materya
Registration Date:	10/10/2010
Awarding Date:	......./......./...........
Degree:	Master of Science
Department:	Electronics and Communications

Supervisors:

Prof. Dr. Mohamed Sameh Saied

Dr. Hassan Moustafa Hassan

Examiners:

Prof. Dr. Hassanein Amer Hamed   (External examiner)

Prof. Dr. Mohamed Fathi   (Internal examiner)

Prof. Dr. Mohamed Sameh Saied   (Thesis main advisor)

Title of Thesis:

DESIGN OF READ/WRITE CIRCUITS SUITABLE FOR MEMRISTOR-BASED MEMORY ARRAYS

Key Words:

Memristor; Read/write; Memory; nonvolatile; Memory arrays

Summary:

Memristor, which known as the missing fourth circuit element, is a potential candidate for the next-generation memory. Memristor has received extra attention in the last few years. In this thesis presents three novel Read/Write circuits suitable for Memristor-based memory arrays. The advantages of the proposed Read/Write circuits are threefold. Firstly, two of the proposed circuits have non-destructive successive reading cycle capability. Secondly, it occupies less die area. Finally, the proposed Read/Write circuits have less power consumption and delay time compared to other Read/Write circuits.

Acknowledgments

I am truly surprised when I think of how much I have learned and all of the rich experiences I have been blessed with over the course of my Master degree. For this, I am grateful to all those who not only helped me in my pursuit of my MSc degree, but have made the past few years so very memorable.

Dedication

"To my parents, whose unbounded sacrifices have brought me this far."

Mohamed Elshamy

Table of Contents

List of Tables

List of Figures

Nomenclature

1D1M	one Diode one Memristor
1T1C	one Transistor one Capacitor
1T1M	one Transistor one Memristor
1T1MTJ	one Transistor one Magnetic Tunneling Junction
ASIC	Application Specific Integrated Circuit
CBRAM	Conductive Bridge Random Access Memory
CIP	Current-In-Plane
CMOL	hybrid CMOS/nanoelectronic circuit
DRAM	Dynamic Random Access Memory
EBL	Electron Beam Lithography
FERAM	Ferroelectric Random Access Memory
FPGA	Field Programmable Gate Array
LER	Line Edge Roughness
LTD	Long Term Depression
LTP	Long Time Potentiation
MIM	Metal Insulator Metal
MIT	Metal Insulator phase Transition
MRAM	Magnetoresistive Random Access Memory
mrFPGA	memristor based re-configurable Field Programmable Gate Array
MTJ	Magnetic Tunneling Junction
NVM	Non Volatile Memory
PCRAM	Phase Change Random Access Memory
PLA	Programmable Logic Array
PMC	Programmable Metallization Cell
RAM	Random Access Memory
RDD	Random Discrete Doping
RP	Reverse Polarity
RRAM	Resistive Random Access Memory
SEM	Scanning Electron Microscope
SRAM	Static Random Access Memory
STT-MRAM	Spin Transfer Torque Magnetoresistive Random Access Memory
TMR	Tunneling Magneto Resistance
UWB	Ultra Wide Band

Abstract

Emerging non-volatile universal memory technology is vital for providing the huge storage capabilities required by the nano-computing facilities. The recently found memristor, "the missing fourth circuit element", is a potential candidate for the next-generation memory and has received extra attention in the last few years. In this work, a literature review of different physical realizations of the memristor is discussed. Following that, a comparison between two of the most promising physical realizations is conducted. Also, different memristor-based applications are reviewed showing that the memory application is the most promising one. Besides, memristor-based memory Read/Write circuit design considerations are demonstrated. Current literatures show destructive reading issue when using the memristor as a memory element. This work is targeting at solving this issue by providing three novel Read/Write circuit designs to facilitate the reading and writing operation of the memristor device. The proposed circuits exhibit lower power consumption and less delay when compared to recently published Read/Write circuits. In addition, two of the proposed circuits have the advantage of non-destructive successive reading cycles capability as well as occupying small layout area.

Chapter 1: Introduction

1.1   Motivation

Recent years have seen considerable research interest in memristor. Using symmetry arguments, memristor has been recognized as the first practical implementation of the missing fourth fundamental circuit element predicted by Leon Chua in 1971 [1]. As known, the basic circuit elements such as resistance (R), capacitance (C), and inductance (L), interpret the relationships between fundamental electrical quantities such as voltage (v), current (i), charge (q), and flux (ϕ). For instance, R relates v and i, capacitance relates q and v, and inductance relates ϕ and i. As shown in Figure 1.1, L. Chua argued that there exists a missing link between ϕ and q, which is called Memristance [1]. This new element relates the magnetic flux to the electric charge by changing its resistance as charges pass through it. By definition, a linear memristor acts like a resistor. However, as the ϕ-q relation is nonlinear, the device behavior differs from that of a resistor.

The main difference between a memristor and a resistor is that memristance is a function of charge, which depends on the hysteretic behavior of current/voltage profile [2]. In other words, memristance depends on the integral over the time of the applied stimuli on the device terminals. Also, it differs from capacitor as, memristor has a unique capability to accumulate charges passing through the device whether it is driven by constant or varying current and/or voltage source. On the other hand, capacitors must be driven with a varying current and/or voltage source to accumulate the passing charges.
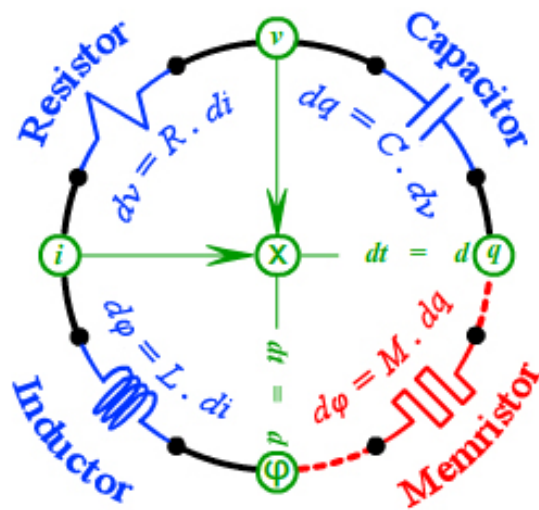
Figure 1.1: Four fundamental circuit elements: R, C, L, and M (which is the missing fourth element that Chua argued for [1]).

Moreover, memristor has gained more focused attention in several articles written by the father of the memristor, Leon Chua, and his colleague Kang [3–8]. In [3], the memristor term has been developed to a more generalized concept named memristive, showing that memristive systems can not be described by one equation. Two equations, at least, are required to totally describe a memristive system. One equation to describe the system

1

memristance and the other one to show how the state variable response to the applied stimuli. It is also shown that memristors are characterized by a pinched hysteresis loop. The pinched hysteresis loop demonstrates the memristive system response to the applied frequency. As shown in Figure 1.2, there is a non-linear dependence on voltage at low frequencies, explicit hysteresis at higher frequencies, and hysteresis avalanche at very high frequencies.
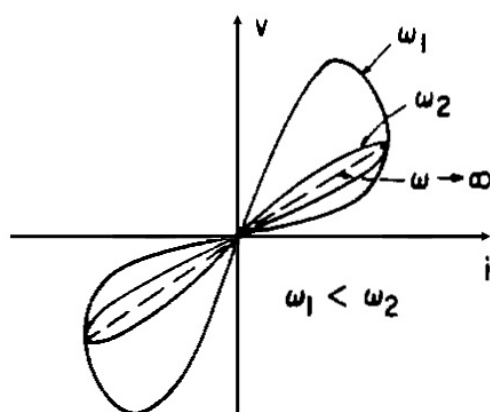
Figure 1.2: Frequency response of Pinched hysteresis loop in memristive systems [3].

After nearly 40 years specifically on May 2008, a research team for information and quantum systems in HP labs under R. Stanly Williams' supervision announced the first physical memristor realization [9]. Memristor is proposed as a bipolar two terminal nano-scale device whose resistance depends on the magnitude, polarity, and the pulse width of the applied voltage [10].

Figures 1.3-a and 1.3-b show the physical structure of a memristor device and its equivalent circuit model. The device is composed of a TiO_2 thin film of length D, sandwiched between two metal contacts. There are two layers in the TiO_2 film. One layer is highly resistive pure TiO_2 (un-doped layer), and the other layer is filled with oxygen vacancies, which makes it highly conductive (doped layer). The doped region has low resistance while the un-doped region has much higher resistance. The state variable w in such devices has been introduced to be the length of the doped semiconductor region along the thickness of the thin film. The dynamical behavior of w is governed by the drift diffusion of ionized dopants such as oxygen vacancies.
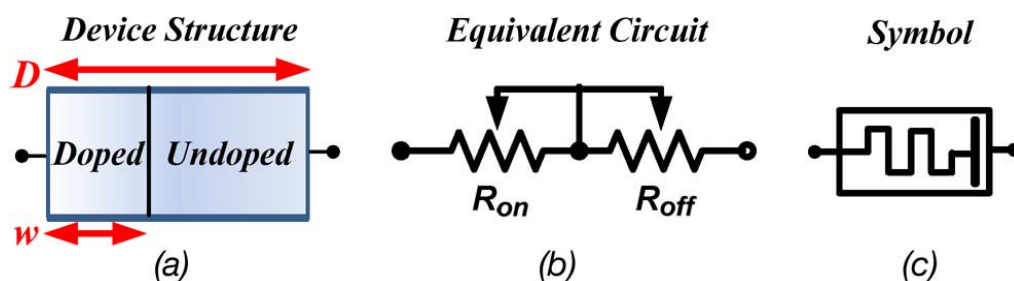
Figure 1.3: (a) Memristor device structure, (b) Equivalent circuit model, and (c) Memristor symbol [11].

Applying a voltage on the memristor terminals will force the ions to migrate and this

changes the thickness of the oxygen deficient layer. In other words, when an external bias voltage, v, is applied across the device, the electric field repels the positively charged oxygen vacancies in the doped layer into the pure TiO_2 layer and the state length w is changed [11]. Hence, the device total resistivity changes. If the doped region extends to the full length D (i.e., w/D = 1.0), the total resistivity of the device is dominated by the low resistivity region, with a value denoted by R_{on}. On the other hand, when the un-doped region extends to the full length D (i.e., w/D = 0), the total resistivity of the device is dominated by the high resistivity region, with a value denoted by R_{off}.

Figure 1.3-c displays the memristor symbol. The orientation of the symbol follows the equivalent circuit in 1.3-b, where R_{on} is at the left and R_{off} is at the right. The polarity matters in memristor circuits. If a bias condition excites the memristance to increase, the reverse connection of the memristor decreases the memristance, which is equivalent to reversing the polarity of the biasing source [12].

The introduction of this new memristor device has revived the research interest in the memristor physical realization. Recently, researchers have proposed several promising fabrications of the memristor devices based on different materials [13–17]. Beside the solid state device, magnetic technology may provide the other prospective technology to build a memristive system. Nanoscale spintronic memristor which depends on spin torque induced magnetization motion and spin transport at semiconductor/ferromagnet junction had been proposed in [16]. Spintronics take the advantage of the intrinsic spin of the electron and its related magnetic moment, besides its fundamental electronic charge in solid-state systems.

Spintronic memristor proposed in [17] is an integration between memristive device and spintronic device. In the introduced spin torque memristors [17], the resistance reliance upon the combination of current/voltage is achieved through a mixing of magnetoresistance and spin torque induced magnetization motion. Based on magnetoresistance principle, the resistance of the submitted spintronic memristor is resolved by its magnetization state. The magnetization state of the device is varied by current electron spin through spin torque induced magnetization motion. The total device magnetization state is determined by the integration effect of electron spin excitations. Therefore, the device resistivity depends upon the accumulation effects of current/voltage profile.

The physical realization of memristors spurred a great interest in the research community. Memristors are considered as one of the possible future alternatives to current CMOS technology. It is stated by Williams that, memristors can potentially replace the CMOS transistors in the future while providing better performance [18, 19]. Memristor-based technology provides much better scalability and higher utilization [20]. Also, memristors consume much less power than transistors as they do not require power to retain state and they are leakage-free [21]. In addition, the small size of memristors (less than 10nm for two terminals memristor) will improve the scalability of integrated circuits significantly. These unique characteristics of memristors give them an important role in shaping the future of semiconductors as they possess many advantages over the conventional CMOS transistors. Despite its advantage, memristors face a big challenge on process variation control during the manufacture procedure because of its nano-scale dimensions.

In light of its properties and compatibility with CMOS technology , memristors have attracted many researchers to develop memristor-based applications. Several articles in the literature have adopted memristors in Programmable Logic Arrays (PLAs) [22–25],

and analog circuit applications [26, 27]. The most amazing results have indicated that applying a train of periodic pulses to memristor-based electronic circuits makes these circuits capable of emulating the brain functions such as learning and anticipating. Such learning circuits can be utilized in several applications in various research areas such as neural networks, fuzzy logic, Neuromorphic applications, and artificial intelligences [28–35]. Also, it can be used in sensors [36], secure communications [37], counters [38], and even more.

1.2 Memory Effects in Memristor

The significance of memory may adopt different concepts in miscellaneous cases. For example, when talking about humans, generally it means the act of recalling past experiences. In the case of computer, it means the capability to save digital information to be used in calculations. Actually, looking closer to these two examples, or any other case where the "memory" concept is used, leads to realize that all contexts share a common thread that allows a general definition as follows: Memory is the ability to store the state of a system at a given time, and access such information at another time. The procedure of storing such information can be realized in different manners. In the brain, for example, the information seems to be stored in the synapses or connections that are established among different neurons via the chemicals that are released when the synapses are excited by ionic potentials [39]. In the present known memories, it uses a bit of information which may be stored as a charge in a capacitor or transistor gate [40] or as a spin polarization in a certain magnetic materials [41]. In fact, all these examples show that a memory state is associated with some dynamical properties of the ingredients of the used materials, namely electrons and ions. Actually, a closer look will demonstrate that history-dependent particularity is related to how electrons and/or ions rearrange their state in a certain material under the effect of external disturbances. There are different memory types: volatile versus nonvolatile; fast versus slow; low capacity versus high capacity; and cheap versus expensive. Nowadays, memory is a part from almost all electronic devices such as computers, robots, FPGAs, and so on, which makes the demand on high speed and density memories increased.

A number of papers have recently been published [42–44] that have presented chips with both high speed access and high density. In [42], the authors demonstrated a high-speed STT-MRAM chip fabricated in 0.13μm CMOS with a read access time of 8ns and write access time of 12ns. In [43], the authors presented a 64Mb STT-MRAM test chip with a 30ns cycle time. Furthermore, in [44], the authors presented an analysis showing how a 1Gb STT-MRAM chip with 10ns read/write access is achievable in todays technology. All of these works have made use of the standard 1 Transistor, 1 Magnetic Tunneling Junction (1T1MTJ) cell. However, current CMOS-based memory technology faces several hurdles in its pursuit to meet the increasing demand for faster processing and larger data size. For example, SRAM, the most widely used on-chip memory, due to its fast access time and relatively small size, is reaching its physical limits in achieving higher densities and lowering power consumption. In addition, the progress in utilizing other emerging memory technologies, such as EDRAM, MRAM, and PCRAM, slow due to their lack of compatibility with CMOS, their slow access time, and their limited scalability. It is stated by Williams that, memristors can potentially replace the CMOS transistors in

future application while occupying less chip area, consuming less power, and providing better performance [18, 19]. Thus, memristors can play an important role in improving the scalability and efficiency of existing memory technology. The nonvolatile advantage of memristors places them as highly ranked candidate for the next generation of universal memories technology. Memristor-based memories exhibit higher storage density than hard drives with access times close to those of SRAM memories. It has been declared that memristor devices can be scaled down beyond 10nm and memristor-based memories can achieve high data storage density close to 100 Gb/cm^2, which is higher than current advanced flash memory technologies [23, 45]. Several literature makes use of the mimrestor as a digital single bit memory as in [12, 46, 47]. Despite its advantage, reading stored data from the memristor is a challenge. This is due to the accumulative property of memristors. So, repeated reading cycles disturb the stored data as in [12, 46, 47] and hence a refreshment circuit is a must.

1.3   Thesis Objectives

In this thesis, the physics behind the operation of TiO_2 and spintronic memristor are discussed. Then a comparison between the two devices is introduced based on this analysis. Also, an appropriate model from the literature to predict the TiO_2 response in memory cells is explained.

On a separate front, novel Read/Write circuits have been introduced to allow the integration of the memristor device as a memory element. Two of the proposed circuits have the advantage of non-destructive reading process and eliminate the need of refreshment drivers as required by the previous Read/Write circuits such as [12]. Also, the proposed Read/Write circuits exhibit faster access times, less power consumption, and smaller layout area (i.e., higher storage density) than the circuit introduced in [12]. After that the dynamics of the proposed circuits in an array are tested showing the memory cell response and the needed power consumption.

The contributions of this thesis are the following:

1. Providing a background about memristors.

2. Characterizing and modeling of the TiO_2 memristor behavior and spintronics memristor behavior, where a comparison between the two types is submitted.

3. Proposing novel non-destructive Read/Write circuits based on TiO_2 memristor.

1.4   Thesis Outline

The remaining chapters of this thesis are organized as follows:

- Chapter 2 provides a background.

- Chapter 3 describes different types of memristors and provides a comparison between the most promising memristive systems (i.e., TiO_2 and spintronic memristor).

- Chapter 4 discusses different memristor applications and shows a literature review on Read/Write circuits for memristor based memory cells.

- Chapter 5 introduces novel non-destructive Read/Write circuit and compares the simulation results with previous published results.

- Chapter 6 concludes the thesis and provides the future directions for this work.

Chapter 2: Background

Non-Volatile Memory (NVM) devices maintain the data even after removing the power supply. Magnetic tapes, floppy disks, optical disks, and flash memories are classified as NVM devices. For the time being, solid-state based NVM devices like flash memories have become the most common media for storing the data. Generally, Solid-State NVM devices have a small footprint, large storage capacity, low power consumption, low latency, and very good rugged properties that make them the best storage media for portable devices. Unlike other NVM devices (i.e., magnetic and optical storage devices), the solid-state memories do not require the physical movement of the read head to attain the segment where the data is stored as what has happened in magnetic and optical storage systems and hence the read and write operations in these systems (i.e., solid-state storage systems) are much faster. On the other side, and similar to the magnetic and optical memory devices, solid-state NVM devices store the data without needing power to maintain the data.

Despite its advantages, current NVM technologies are much slower than volatile ones (like Random Access Memory (RAM)), which makes NVM devices not suitable for very fast data access applications like processor cache memory (i.e., Static Random Access Memory (SRAM)) or computers' main memory (i.e., Dynamic Random Access Memory (DRAM)). However, they introduce better speed advantage than other non-volatile devices (i.e., hard disk and optical devices). Referring to the International Technology Roadmap for Semiconductors (ITRS) report (ITRS 2007) [48], it is assumed that, by 2019, 16nm half-pitch non-volatile memory cells will provide a capacity of around 46Gb/cm^2, assuming 100 per cent area efficiency.

Nevertheless, current memory technologies have limitations which are inconsistent with new technologies (i.e., Digital cameras, Mobile phones, and Computers) where higher storage capacity, faster access time, lower power consumption, and less cost are highly required. Based on Moore's law, and as shown in Figure 2.1, the number of transistors per chip doubled every 18 months approximately [49, 50]. But the trend of depleted electronics and the need for higher storage capacity shows that Moore's law is not enough and more Moore or even more than Moore is needed as displayed in Figure 2.2 [51].

Therefore, new non-volatile memory technologies like Phase Change Random Access Memory (PCRAM), Resistive Random Access Memory (RRAM), Magnetoresistive Random Access Memory (MRAM), and Ferroelectric Random Access Memory (FERAM) were introduced to replace the well known NVM technology.

2.1   Emerging Non-Volatile Memory Technology

To reduce the gap between what is needed from memories and what present memory technologies offer, new non-volatile memory (NVM) technologies had been put under research. Most of these technologies are in different phases of realization. Some are still in premature research stages, others have working prototypes, and some of them are already entering into commercial manufacturing.

Microprocessor Transistor Counts 1971-2011 & Moore's Law

Figure 2.1: Plot of CMOS transistor counts against dates of introduction. Note the logarithmic vertical scale; the line corresponds to exponential growth with transistor count doubling every two years [50].

2.1.1 Phase-Change RAM (PCRAM)

Phase-Change Random Access Memory (also known as PCRAM, PRAM or PCM) is one of the most known under research new memory technology. The principle of phase-change memory has been known since the 1960s, but only recent discoveries of phase-change materials with faster crystallization speeds led to the possibility of commercially feasible memory technology. Phase change materials such as chalcogenides (i.e., $Ge_2Sb_2Te_5$ (GST)), can crystallize in less than 100ns [52]. This materials (phase-change materials) have two different phases, with distinguished characteristics [52]:

1. High electrical resistivity used to characterize the amorphous phase.

2. Low electrical resistivity used to characterize the crystalline phase.

These two states (i.e., crystalline phase and amorphous phase) can be frequently and swiftly changed by heating the material. Applying a high-power electrical pulse on the device makes it amorphous, as the device is quickly heated and quenched. On the other

Figure 2.2: More Moore and more than Moore [52].

hand, if the device is heated above its crystallization temperature by a moderate power pulse with a longer duration, it will turn to the crystalline phase. Therefore, the writing speed is determined by the duration of the applied pulse, which varies according to the crystallization speed of the material being used. Based on [52, 53], reflectivity varies up to 30%, and resistivity changes up to five orders of magnitude.
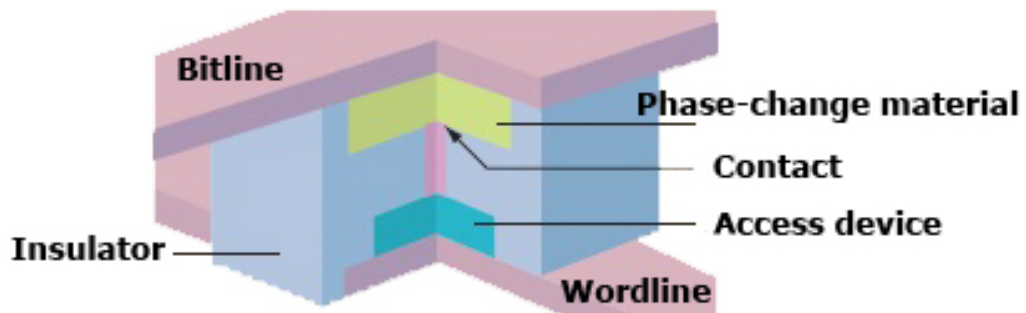
Figure 2.3: A cross sectional area of a Phase-Change Random Access Memory [53].

Phase-change materials can be used to build a memory cell as shown in Figure 2.3. The device is SET by crystallizing the material and RESET by making it amorphous. PCRAM turns from logic zero to logic one and vice-versa without the need for an ERASE operation which is needed in the flash memory. Considering the big difference in resistance, phase-change materials may be used as a binary memory cell (single-level cell) or even to store more than binary state (multi-level cell) [53, 54].

PCRAM prototypes show the device ability to work in the 20nm scale. However, considerations had been taken to scale down the device to 9nm, while DRAM probably will not be able to scale down beyond 40nm [53, 54]. Set and Reset latency are reported as 150ns and 40ns, respectively [54]. For the consumed energy, the device consumes 480μW during the RESET operation, while the SET operation consumes 90μW. For the reading

9

operation latency and consumed power it is 48ns and 40μW, respectively [54]. As noticed from PCRAM read and write latency, PCRAM read and write latency are slower than DRAM read and write latency [54].

As the current passing through the phase-change material during the writing cycles, the device contacts have a thermal expansion and contraction and hence the device endurance is bounded [54, 55]. PCRAM write endurance had been reported to vary from 104 to 109 write cycles [54, 55]. Despite its disadvantage (i.e., access latency limitation, energy consumption, and endurance), PCRAM can concerned as a Flash memory where further development is required in order to replace the DRAM [54, 56].

2.1.2   Magnetoresistive RAM (MRAM)

Magnetoresistive Random Access Memory (also known as MRAM and Magnetic RAM) is considered as NVM device since the 1990s. This device takes advantage of magnetoresistive effect that occurs in magnetic tunneling junction (MTJ). It is deployed as two layer of ferromagnetic material where a third thin oxide layer is placed in between those layers as shown in Figure 2.4. One layer of the ferromagnetic layers, known as reference layer, has a fixed magnetic direction, while the second layer, known as free layer, has magnetic direction controlled by the aid of a magnetic field or by passing a polarized current through the device. If both ferromagnetic layers (i.e., the reference layer and the free layer) have the same magnetic direction, then the resistance of the MTJ is low. On the other hand, the overall device resistance is high when both layers have different magnetic directions. In this way, the device overall resistance can be controlled.
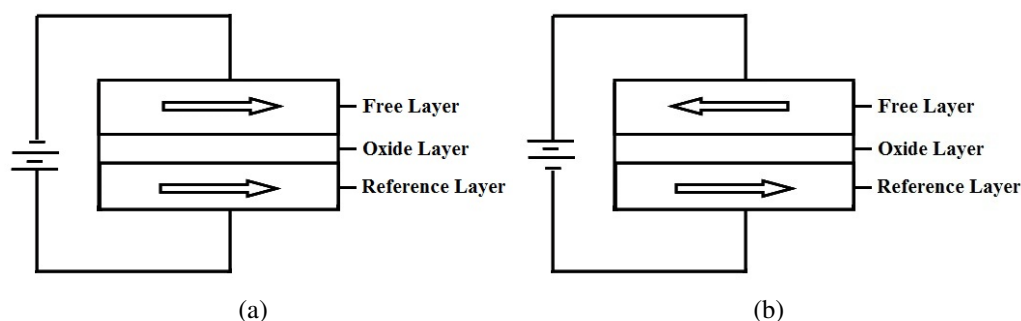
Figure 2.4: An MTJ device where (a) shows the device low resistance state as the magnetic direction in the two ferromagnetic material is parallel and (b) shows the device high resistance state as the magnetic direction in the two ferromagnetic material is anti-parallel.

This phenomenon is known as tunneling magneto-resistance (TMR) [53, 57, 58]. Present MRAMs fabrication suffers from some limitations (like density and energy limitations). According to these limitations which impair the device capacity, MRAMs have some difficulties to compete with existing memory technologies (i.e., DRAM or Flash). Despite that, Spin Transfer Torque Random Access Memory (STT-MRAM) is considered one of the most promising MRAM architectures. STT-MRAM promises to overcome conventional MRAM limitations [58].

2.1.3 Ferroelectric RAM (FRAM)

Ferroelectric random access memory (also known as FeRAM, F-RAM or FRAM) is one of the mature alternatives for the non-volatile memory technologies that shows the same functionality offered by DRAMs and flash memories. It has received a great interest in the research community since the 1980s. It uses the same DRAM construction (i.e., one transistor one capacitor (1T1C)) as shown in Figure 2.5. Unlike the DRAM, FRAM uses a ferroelectric layer instead of a dielectric layer in order to deploy the capacitor which retains the data.
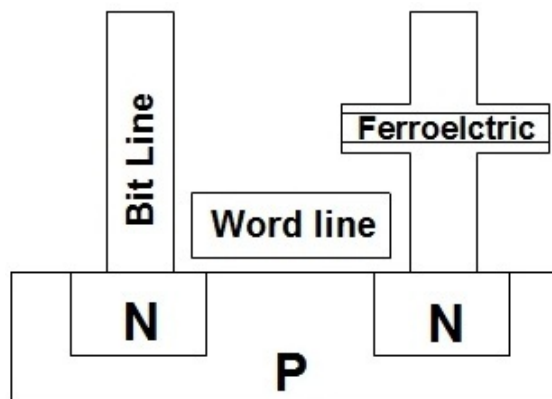
Figure 2.5: A cross sectional area of FRAM device.

Because of the FRAM advantages over conventional NVM such as low-voltage operation, low power usage, fast write time [59], and high read/write endurance (i.e., more than 10^{16} as reported in [60]), several prototype devices based on FRAM had been reported like 256kb FRAM [61], 1Mb FRAMs [62–64], and a ferroelectric memory embedded microcontroller [65]. On the other hand, FRAM devices have limitations on storage capacity. Hence, FRAM presents lower storage density than flash memory.

2.1.4 Resistive RAM (RRAM)

Resistive random access memory (also known as RRAM or ReRAM) takes advantage of the resistance variations to retain the stored data. Regardless the truth that PCRAM uses the same technique to store the data, this term (i.e., RRAM) is used to define a different set of devices. This set of devices may be divided into two groups [53]:

1. Insulator resistive memory:
   It uses metal oxide materials to make use of the advantage of its bipolar resistance switching characteristics. One of the most promising devices in this category is the memristor, which will be discussed in details throughout this research.

2. Solid-electrolyte memory:
   It uses a solid-electrolyte containing mobile metal ions sandwiched between cathode and anode to maintain the data. Also known as Programmable Metallization Cell (PMC) or Conductive Bridge RAM (CBRAM).

Table 2.1: Brief comparison between emerging non-volatile memories.

Comparison aspect	PCRAM	RRAM (Memristor)	MRAM (STT-MRAM)	FERAM
Development	Advanced	Early	Advanced	Advanced
Read Time (*ns*)	12	< 50	35	45
Write Time (*ns*)	100	0.3	35	65
Energy Per Bit Access (*pJ*)	100	2	0.02	3.4
Density (Gb/cm^2)	12	154-309	1.2	0.14
Endurance	10^8	10^{15}	$> 10^{15}$	10^{15}

The previous different non-volatile technologies are briefly compared and summarized in Table 2.1.

As shown in Table 2.1, memristor has better write time, density, and endurance [66, 67]. Interestingly, memristors have extremely high density of more than 110GB/cm^2 and 460GB/cm^2 for 10nm and 5nm half-pitch devices, respectively [10, 68].

In the next section, we will concentrate our attention on the memristor, which is currently the most promising RRAM technology under research [9].

2.2 Memristors

At 1971, young scientist interested in nonlinear systems and equations surprised the world with a new discovery. Leon Chua has introduced to the world a new fundamental passive element named memristor [1]. The name of the device is a composite of two words, memory and resistor, which totally describe the function of the device. It works like a resistor where its value changed based on the applied stimulus. If the stimulus is switched off, the device keeps its last resistance value. By other words, it is a nonlinear resistor with a memory.

Chua found an answer to his wondering in a missing relation between the four fundamental circuit quantities; electric voltage (v), electric current (i), electric charge (q), and magnetic flux (φ). According to Faradays law of induction, the flux is the time integral of the voltage. On the other hand, the charge is defined as the time integral of the current. For the remaining equations, they are based on the three fundamental passive elements (i.e., Resistor (R), Capacitor (C), and Inductor (L)). Resistor relates the voltage and the current (*dv= R . di*), capacitor relates the charge and the voltage (*dq = C . dv*), and inductor relates the current and the flux (*dφ = L . di*). Despite these relations, there is a missing relation where the flux and the charge are directly related. Chua predicted a fourth element that

defines this relation as ($d\varphi = M \cdot dq$), where M is the memristance.

Besides using mathematical equations to demonstrate the new concept, Chua goes an extra mile by emulating the device. A mutator circuit with the aid of a nonlinear resistor is used to emulate the memristor process as shown in Figure 2.6-b.

(a)

(b)

(c)
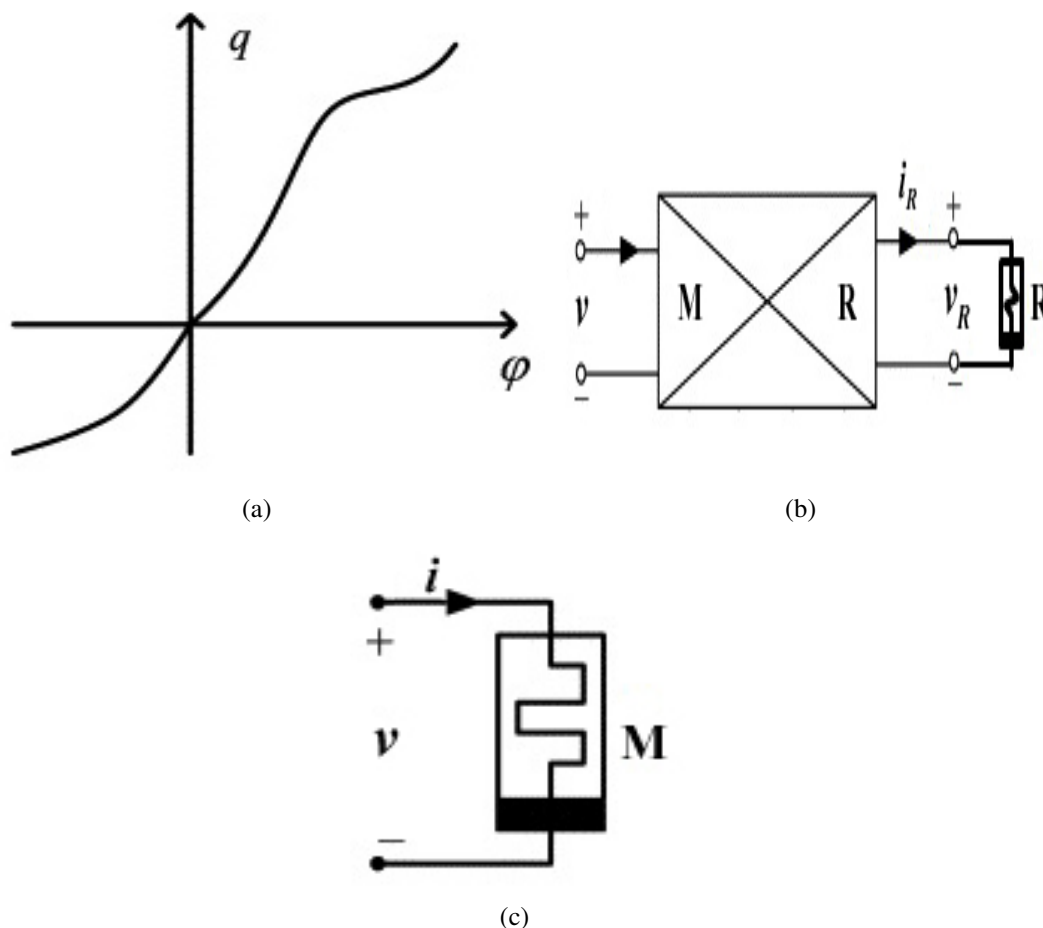
Figure 2.6: The proposed symbol for memristor and its basic realization. (a) the φ-q curve, (b) memristor basic realization where an M-R mutator terminated by nonlinear resistor R is used to emulate the device operation, (c) memristor symbol [1].

According to the proposed emulator and the derived mathematical equations, the new device has the following properties:

1. Fundamental element:
   The memristor operation cannot be performed by any of neither the three fundamental elements nor a circuit only based on those elements. To emulate the device operation, a hybrid circuit of active and passive components is needed. Consequently, memristor is a fundamental element.

2. Passive element:
   The device is fully characterized by two equations, (2.1) and (2.2) if the device is controlled by the charge [1],

$$v(t) = M(q(t)) \times i(t) \tag{2.1}$$

$$M(q) = d\varphi(q)/dq \tag{2.2}$$

where, $M(q)$ is the memristance, v is the applied voltage, and i is the current passing through the device; or described by (2.3) and (2.4), if it is controlled by the flux [1],

$$i(t) = G(\varphi(t)) \times v(t) \tag{2.3}$$

$$G(\varphi) = dq(\varphi)/d\varphi \tag{2.4}$$

where, $G(\varphi)$ is the memductance. So, the instantaneous power (p) is characterized by,

$$p(t) = v(t) \times i(t) = M(q(t)) \times [i(t)]^2 \tag{2.5}$$

Thus, the device is considered a passive element if and only if M(q) ≥ 0, which is the only solution of the device according to the φ-q curve (shown in Figure 2.6-a) that describes the device. In other words, the device is incapable of energy gain or consumption.

3. Analog device:
   Memristor has a unique signal processing characteristic, where the memristance is depending on the time integral of the current passing through the device or the voltage applied on the device terminals. So, memristance is a time varying quantity which depends on the total net charge over the time. This dependency gives the device its analogy criteria.

4. Nonlinear criterion:
   Based on linear system definition, the system variable, which is in this case the memristance, can be written or solved by a linear combination of independent components, or in other words the system has a certain output for a certain input. Based on (2.2) and (2.4), memristance depends on the φ-q relation and the time integral of stimuli (voltage and current), where the linearity principle cannot be applied.

5. Stimuli dependence:
   Memristance value depends on the applied stimuli (voltage or current) regardless of the source shape. This fact comes from the device unique signal processing property. The only thing that matters is the net applied injection and the period of this injection.
   Due to the integration of the applied segments done by the device, the source shape (e.g., triangle, pulse, or sine wave) does not make any difference but only the applied net charge counts.

14

An electromagnetic commentary of memristor properties is supplied to ratification of the possibility of finding such a device. Also Chua applies some theorem like Closure theorem and Existence and Uniqueness theorem to prove the possibility of inventing such a device.

Besides the aforementioned, some uninhabitable applications are submitted like modeling an amorphous ovonic threshold switch, modeling an electrolytic E-cell, and signal processing application (e.g., generating a staircase waveform).

Later, Chua and Kang expand the definition of the memristor to a more general definition named memristive system [3]. According to the new definition, some systems and devices are considered as special cases of memristive systems such as thermistors, discharge tubes, and ionic systems described by Hodgkin-Huxley circuit model [3]. Even new general equations, that fully describe the memristive systems, are introduced as

$$\dot{x} = f(x, u, t) \tag{2.6}$$

$$y = g(x, u, t)\, u \tag{2.7}$$

where, u and y are the input and output of the system respectively, x is the state of the system, and t is the time. If the current (i) and the voltage (v) define the input (u) and the output (y) of the system respectively, then a memristive system is represented by

$$\dot{x} = f(x, i, t) \tag{2.8}$$

$$y = R(x, i, t) \times i \tag{2.9}$$

where, R represents the system resistivity.

Besides the above mentioned properties and based on the new analysis, some new properties were added,

6. I-V Characteristic curve:
   The memristive system I-V characteristic curve under periodic stimulus is represented by a double valued Lissajous figure, where any value of the current (i) has at most two distinct values of the voltage (v) and the figure is symmetric hysteresis around the origin [3] as shown in Figure 2.7.
   Thus, applying a current source

$$i(t) = I cos\omega t \tag{2.10}$$

   where, I is the current passing through the device and ω is the frequency, will cause two corresponding voltage values (v_1 and v_2) for each current value (i) depending on the passing current direction. Assume the system has a low memristance value and a positive current is passing through it, then the system will have low voltage drop (v_1). On the other hand, if the system memristance is maximum and the same current magnitude is passing in the reverse direction, the system will have large voltage drop (v_2).

   According to the I-V curve symmetry, there will be two equally resistive value ($R(x,i) = R(x,-i)$) under the same periodic current source.

15
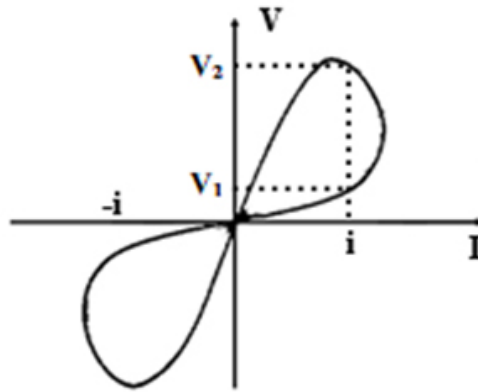
Figure 2.7: Double valued lissajous figure with symmetry around the origin (hysteresis loop) [5].

The Lissajous figure with the previous properties (double valued and symmetrical around the origin) is defined as a hysteresis loop which is considered as memristive system imprint.

7. Frequency response:
The nonlinear criterion depends on the frequency hence, using DC source ($\omega = 0$) makes $f(x,i)$ in (2.8) equal to zero and the system will act as a time invariant current controlled nonlinear resistor, where the system state is highly dependent on time.

On the other hand, the system degenerates to a linear time invariant resistor as the frequency increases towards infinity [3]. As seen in Figure 1.2, there is an inverse relation between the applied frequency and the non-linearity of the system.

To physically realize the device according to the previous device analysis and properties, Chua suggested that to physically deploy the device a nonlinear material should be used. By using a nonlinear material the device characteristics in general will be defined and a physical memristor will be made.

In [9], R. S. Williams introduced a two-terminal Titanium dioxide (TiO_2) nano-scale device that follows the memristive characteristics defined by L. Chua. Later on, many devices have been argued as another physical realization of memristors [13, 16, 65, 69].

16

Chapter 3: Memristive Systems

Recently, after the announcement of HP's memristor, memristive systems gained a great interest where many systems show memristive behavior are introduced. These systems have different memristance mechanisms like thermal effects, chemical reactions, ionic transfer, spin polarization, and phase transitions. Some of these systems were early introduced in [3] (i.e., thermistors and ionic systems). Other systems were studied during the last 10-15 years for the sake of resistive-switching memory development. Resistive-Switching memory research began in 1962 when Hickmott observed a hysteresis behavior in oxide insulators [70]. After that, Simmons and Verderber examined the resistance switching mechanism in thin silicon monoxide (SiO) film sandwiched between two metal electrodes [71]. It was also tested in TiO_2 devices by Argall [72]. However, resistive switching devices were not recognized as memristive systems until 2008 [9]. After that other memristive systems such as spintronic devices [17, 20], phase-transition materials [73, 74] and polaronic systems [75] were introduced. Below, memristive properties of a variety of physical memristive systems are discussed.

3.1   Polymeric Memristor

Dynamic doping of polymer and inorganic dielectric-like materials that improved the switching characteristics and retention required to create functioning nonvolatile memory cells was described in [76]. The device was fabricated by placing a passive layer between electrode and active thin film as shown in Figure 3.1. The passive film improves the extraction of metal ions from the electrode and preferable to have good electronic and ionic conductivity to enhance the memory operation. The switching and retention manner of the passive layer is neither stable nor reproducible because of the randomness of the filament formation and commonly need high voltage (10-20 V) corresponding to high electric field in order to extract metal ions from the metallic electrodes [76]. These large voltage value are accompanied by localized Joule heating, and hence complicating scalability and power issues. Using superionic materials for this layer (i.e., passive layer) allow for considerable decrease in the needed voltages for ion extraction and switching (from $\sim$ 10V to 0.2-0.5 V), thereby causing a reduction in the accompanying heating [76].
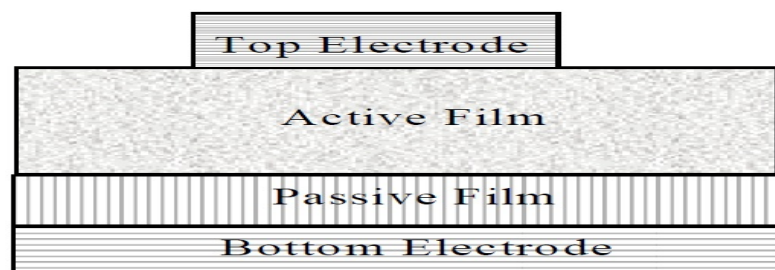
Figure 3.1: Schematic showing four thin-film layer which represents the device structure of polymeric memristor [77].

The switching operation is done in two steps. First the forming step, then the programming step. Forming is unique, where ions are extracted from the electrode and transported

or injected into the active layer. In the second step, a conductive bridge is formed and then broken in a repetitive manner (representing programming and erasing operations) in response to the applied electric field [76].

Figure 3.2 shows the I-V characteristic curve, where the memory cell at the beginning has a large resistance ($\sim 20 M\Omega$) and the device is considered in the OFF state. After reaching a threshold voltage ($\sim 1V$), the device switches to a low resistance ($\sim 20k\Omega$) and the device is considered in the ON state. This operation can be repeated more than 106 cycles and hence endurance of > 106 cycles is achieved [76].
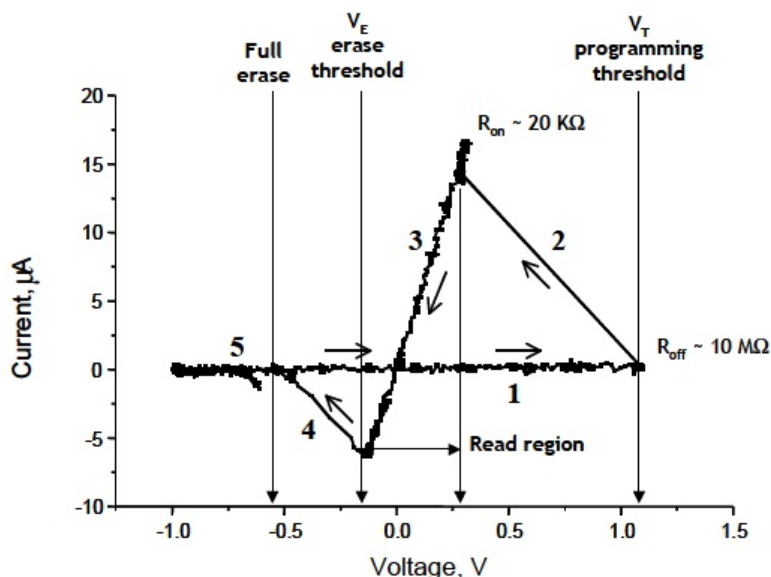
Figure 3.2: Schematic showing four thin-film layers which represents the device structure of polymeric memristor [77].

3.2 Metal-insulator Phase Transition Memristive Systems

Complicated interactions between charge, lattice, and spin degrees of freedom in strongly reacting electron materials lead to resistance switching effect [77, 78]. Currently a vanadium dioxide-based devices have been used to deploy memristive systems that contain this oxide [73]. The memristive behavior is driven by the metal-insulator phase transition (MIT) of this material [79, 80].

As portrayed in Figure 3.3, the device is fabricated from a thin film of VO_2 deposited on a sapphire substrate and connected to two electrodes [81]. The operation temperature was selected near the onset of the phase transition (340K), as VO_2 properties are very sensitive to temperature changes, where a high amplitude voltage pulses (50V) are used to increase the VO_2 temperature for short periods of time, thus promoting the MIT [81]. This triggers pulses resulting in a nanoscale metallic regions development within the insulating host, increasing in number and size to form a percolative transition [82].

The VO_2 memristive systems have two state variables, the resistance and the temperature [81]. Thus, the resistivity of the system changed as the device temperature changed.
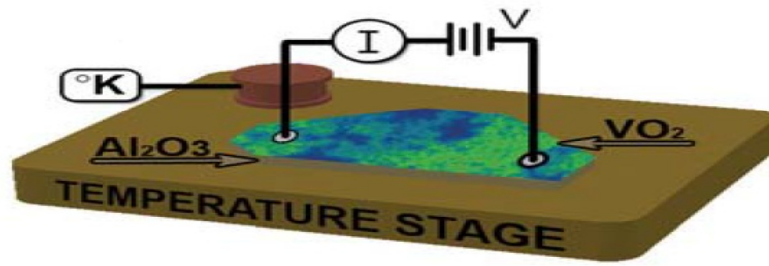
Figure 3.3: Schematic showing a phase transition driven memristive device [82].

Therefore, applying a voltage pulse to the vanadium dioxide results in local heating and hence the system resistance decreases as shown in Figure 3.4.
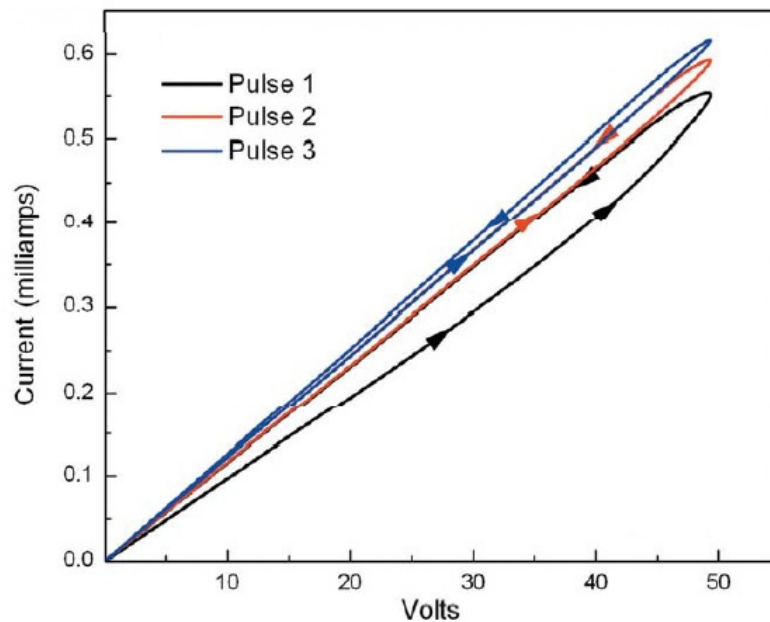
Figure 3.4: Hysteresis I-V curves under which three ramped voltage pulses are applied [82].

Recently, reversible resistance switching is observed in MIT materials at low temperatures, where the resistance switching effect is explained by Joule heat induced transition between charge-ordered insulator and ferromagnetic metal phases [83]. This transition was shown to be a bidirectional transition and can be uniquely controlled by current pulse pairs [83]. By this way, low and high resistance states become nonvolatile. However, it is demonstrated in [83] that the resistance switching has a considerable frequency dependence. This property is regular for memristive systems but the hysteresis in this particular material is not suitable for room temperature applications [81].

3.3   Resistance Switching Memristors

Recently, the resistance switching effect was observed in diverse classes of materials (i.e., TiO_2, CuO, and NiO) [81]. In 2008, R. S. Williams introduced a two-terminal titanium

dioxide (TiO_2) nano-scale device that follows the memristive characteristics defined by L. Chua [9]. TiO_2 thin film memristor was proposed as a two terminal device whose resistance depends on the magnitude, polarity, and the pulse width of the applied voltage [9].

The device is fabricated as a cube of a non-volatile programmable impedance material (i.e, titanium dioxide (TiO_2)) with 40-50 nanometer length (*L*), 40-50 nanometer width (*W*), and 3-30 nanometer thickness (*D*) sandwiched between two platinum electrodes of 2-3 nanometer thickness. The titanium dioxide cube is divided into two layers, the lower layer acting as an insulator where the oxygen ions are twice the titanium ions. By contrast, the upper layer is missing 0.5% of its oxygen ions (TiO_{2-x}) and acting as a semi-conductor as shown in Figure 3.5-a.

The device acts like a switch with a resistance ratio of 1000, which means that the ratio between the OFF state to the ON state is 1000 to 1 (normally, R_{on} and R_{off} are in the range of ohm and kilo ohm, respectively), placed in crossbar architecture. The crossbar architecture is a fully connected net of orthogonal nano-wires, where the contact point between any two perpendicular wires represents a switch as shown in Figure 3.5-b.

(a)

(b)
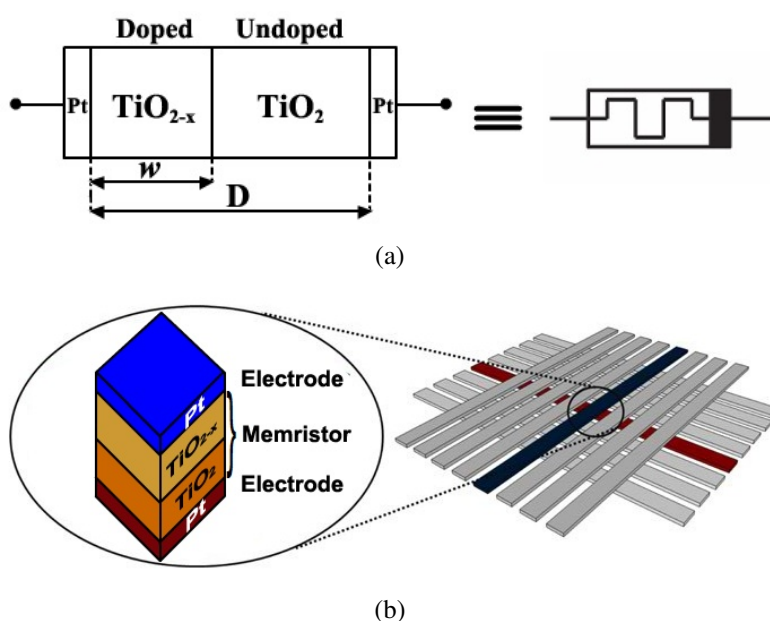
Figure 3.5: Memristor structure and symbol. (a) memristor architecture and the circuit corresponding symbol. (b) memristor crossbar architecture showing memristor location between two perpendicular nano-wires.

Figure 3.6 shows a typical hysteresis loop of this memristive systems. The I-V loop maps the switching characteristics of the device. The device shows about 10^6s memory storage possibility and the capability to operate after 4000 physically flexed times [84]. The device resistance for both ON and OFF states can be increased by multiple consecutive mechanical deformations of the device, where the ON/OFF ratios is almost unchanged. Therefore, this device has the ability to be used in flexible lightweight portable electronic devices [84].
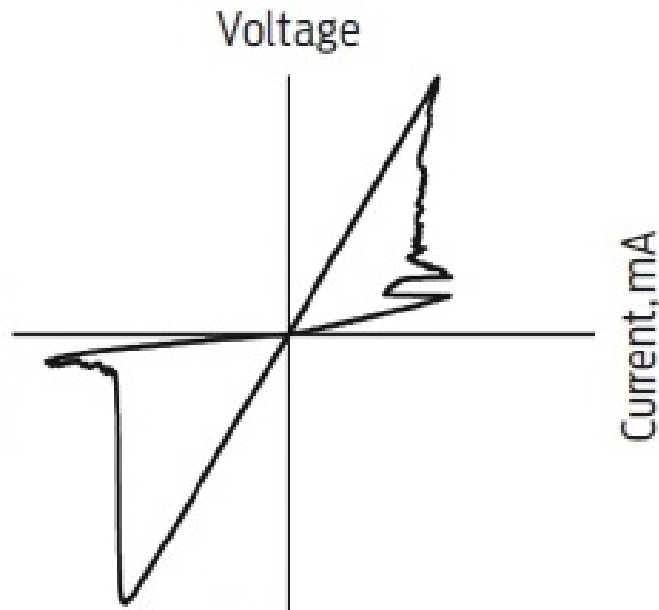
Figure 3.6: Applying symmetrical alternating-current voltage bias results in the I-V hysteresis loop [10].

3.4 Spintronic Memristors

Memory is not necessarily restricted to structural or charge properties but may also come from the spin degree of freedom. Three different spintronic systems had been studied in [16] showing their memristive effect through nano-scale magnetic electronic systems (i.e., thin-film magnetic tunneling junction (MTJ) under spin-torque excitations, thin film magnetic element with varying width (w) and constant thickness (h), and long spin valve with domain wall motion). The most promising magnetic realization of the memristor is the one introduced in [17].

Spintronic memristor consists of a long spin-valve strip which includes two ferromagnetic layers: reference layer and free layer. The magnetization direction in the reference layer is fixed by coupling it to a pinned magnetic layer. A domain-wall divides the free layer into two segments that have opposite magnetization directions. These layers are made from a ferromagnetic material (e.g., Molybdenum (Mo) and Cobalt (Co)) with 130-1000 nm length (D), 10-20 nm width (z), and 7-70 nm thickness (h). This composition is placed between two metal contacts with 2-3 nm thickness as in Figure 3.7 [17].

The device resistivity is varying from low resistance (R_L) to high resistance (R_H) based on the applied spin polarized current direction. Normally $R_L = 5$ kΩ and $R_H = 6$ kΩ [17]. Accordingly, the device has a resistance ratio of 1.2.

The spintronic memristor I-V curve is not unique as noticed in Figure 3.8. However, the spintronic memristor can not be simply modeled as a non-linear resistor of which the resistance is determined by the magnitude of the applied voltage on the device. This is because, the I-V curve shape depends on the historical status of the applied voltage (i.e., frequancy and amplitude of the applied voltage) [17].
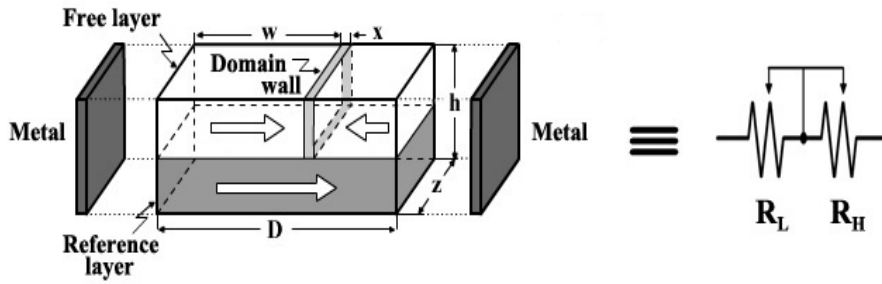
Figure 3.7: Spintronic memristor based on magnetic-domain-wall motion and the equivalent circuit.
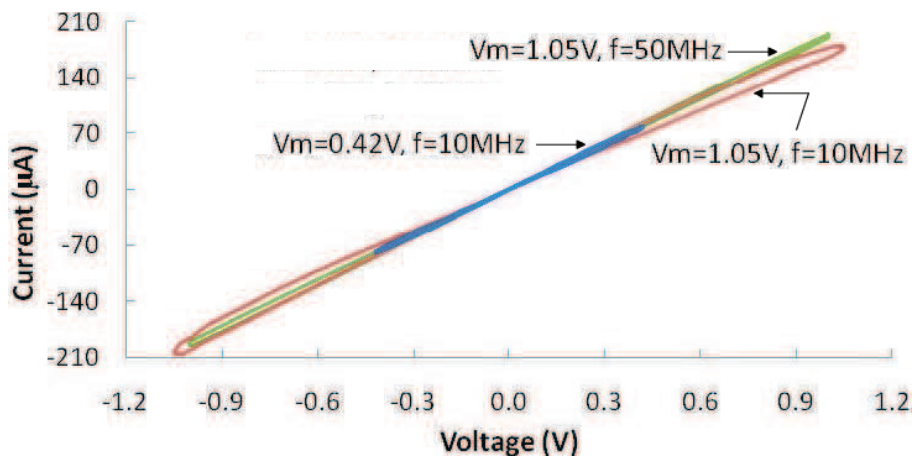
Figure 3.8: I-V curve of the spintronic memristor with sinusoidal voltage excitation [17].

3.5   Comparison between TiO_2 Memristor and Spintronic Memristor

In this section, a brief comparison between the most promising devices (i.e., Resistance switching memristor "TiO_2 memristor" and spintronic memristor). These devices considered as promising ones because they offer working prototypes and have many submitted applications in the literature [12, 18, 23–27, 34, 36–38, 46, 47, 68, 85].

3.5.1   Working Principle

Titanium dioxide (TiO_2) is considered as a wide-band gap semiconductor material with auto-doped characteristics. In other words, if some oxygen atoms have been taken out from the material, then the device will be a semiconductor device with slightly mobile vacancies. Applying a voltage will cause these mobile vacancies to move from one side to another inside the material, causing the material resistance to increase or decrease based on the polarity of the applied voltage.

When applying a positive voltage on the top electrode in Figure 3.5-b, the positively charged oxygen deficiencies will be repelled toward the bottom electrode as shown in Figure 3.9-a. Thus w, which is the doped layer width, will increase and hence increasing
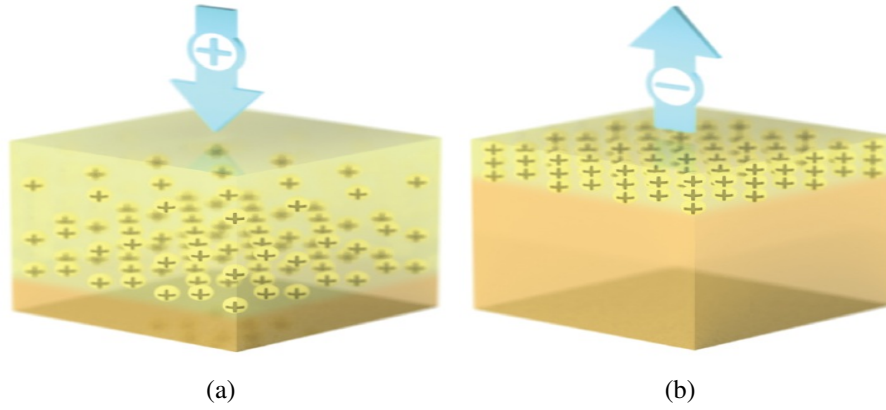
Figure 3.9: Voltage effect on TiO_2 memristor a) when applying positive voltage b) and when applying negative voltage [2].

the semiconductor layer width compared to the insulator layer width, causing the system total memristance to decrease.

On the other hand, applying a negative voltage on the upper electrode in Figure 3.5-b, will cause the positively charged oxygen deficiencies in the semiconductor layer to be attracted to the upper electrode as shown in Figure 3.9-b. Respectively, w will be shrinking and hence the insulator layer width will increase, therefore the total memristance of the device will increase.

Generally, the boundary between the two layers, semiconductor and insulator layer, may be considered as a moving wall, where the direction of the wall movement depends on the polarity of the applied voltage. Therefore, the device is totally described by two equations [9],

$$V = R(w) \times i \tag{3.1}$$

$$\frac{dw}{dt} = \mu_v \, i \, \frac{R_{on}}{D} \tag{3.2}$$

where, V is the applied voltage, R(w) is the system resistance as a function of w, i is the current passing through the device, w is the doped layer width, μ_v is the dopant drift mobility, D is the total device length, and R_{on} is the ON resistance of the device when w = D. Therefore, the width of the doped region (w) represents the state variable of the system.

On the other hand, spintronic memristor is based on the spin torque caused by the magnetization motion and spin transport at semiconductor/ferromagnet junction. Spintronic devices get advantage of the radical spin of the electrons and its related magnetic moment, beside its fundamental electron charge in solid devices.

The device is divided into two layers, reference layer and free layer. The magnetization direction in the reference layer is fixed by connecting to a pinned magnetization layer. Position of the domain-wall in the free layer can be changed by passing a driving current, and hence the total memristance of the device changes. The driving current is polarized by the aid of the reference layer. This conduction mode is called current-in-plane (CIP) geometry.

23

Electron spin direction in the domain-wall is rotated based on the magnetization exchange interaction. This interaction occurs when a spin polarized current passes. Thus, electron spin creates a reaction torque on the domain wall causing its motion. Therefore, applying a polarized current in the same direction of the magnetization in the reference layer will cause the domain-wall to move in the same direction. Accordingly, both layers (i.e., reference and free layer) magnetization orientation will be parallel. Hence, the system resistivity will be low (R_L) as shown in Figure 3.10-a. On the other hand, passing the polarized current in the opposite direction to the magnetization in the reference layer will cause the domain-wall to move in the reverse direction. Consequently, the magnetization orientation in both layers will be anti-parallel. Hence, the system total resistivity will be high (R_H) as shown in Figure 3.10-b.

(a)   (b)
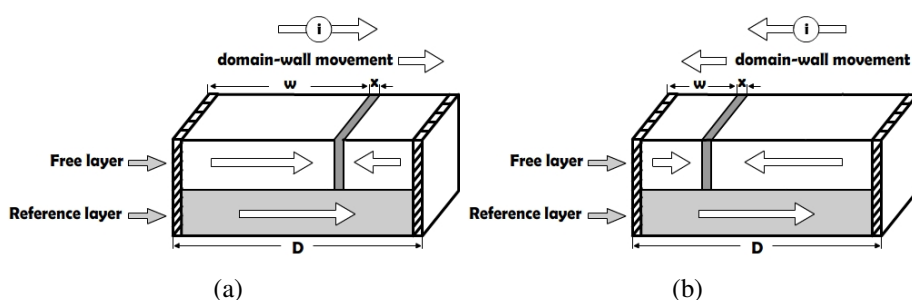
Figure 3.10: Voltage effect on spintronic memristor when the passing current (a) causing the magnetization direction in the free layer to be parallel to the magnetization direction in the reference layer (b) and when causing the magnetization direction in the free layer to be anti-parallel to the magnetization direction in the reference layer.

Subsequently, the memristance of spintronic memristor is governed by the domain-wall position and the spin polarized current. Therefore, the system can be totally described by [17],

$$V = R(w) \times i \tag{3.3}$$

$$\frac{dw}{dt} = \frac{\Gamma_v}{h \times z} i \tag{3.4}$$

where, V is the applied voltage, R(w) is the device resistance as a function of w, i is the current passing through the memristor, w is the domain-wall position, Γ_v is the domain-wall velocity coefficient, and h and z are the device thickness and width, respectively. Hence, the position of the domain-wall (w) represents the state variable of the system. Note that, the spin torque excitation is a localized effect, where the torque is generated by a localized spin polarized current passing through the device. This localized effect gives the device better scalability and simpler device architecture [2].

3.5.2 Device Properties

In light of the analysis of both devices (i.e., TiO$_2$ and spintronic memristor) introduced in [2, 8–11, 16, 17, 20, 86–89], the devices properties can be summarized as follows,

1. Nano-scale device
   Titanium dioxide is a well known material for decades, but no one thought about it as a non-volatile programmable impedance material because of the high electric field needed to move the oxygen atom for a sensible distance even in the micro scale devices. The oxygen atom slowness may be the reason of this issue. But because of the device nano-scale, the oxygen atoms will be free to move inside the device with a sensible rate, where the device resistance changed according to this movement. Accordingly, getting smaller getting better as the device characteristics are enhanced (e.g., faster response time and lower applied voltage).

   For spintronic devices, they are typically fabricated in the sub-micron scale. According to the device fabrication in nano-scale, memristive effect of the device has shown up. But it is worth mentioning that, the device scaling down has length limitation which can not be exceeded. The domain-wall thickness (x) is one of these limitations. Also, the macroscopic nature of the magnetic devices makes it hard to be scaled down. This is because if there is a single defect in the device structure, a large amount of bits is rendered unusable [2].

2. Bipolar device
   Based on the previous discussion, memristor state, for both TiO_2 and spintronic, is depending on the polarity of the applied voltage and hence the device memristance.

3. Great resiliency and reliability when power is interrupted
   Memristors store data as resistance. This resistance depends on the oxygen atoms' movement in TiO_2 memristors or the electron spin and magnetization direction in spintronic memristors caused by the applied stimulus. Thus if this stimulus is turned off, the oxygen atoms' position or magnetization direction will save its last position. So, if a memory device is made totally from memristors (i.e., memory cells, memory array peripherals, and sense amplifiers), then cutting off the power does not matter as the device will save its last state until the power is restored and hence the device has a better reliability.

4. Memristance consideration
   Migration between doped region low resistance and un-doped region high resistance in TiO_2 represents the system resistivity, named memristance, as,

$$R(w) = R_{off} - \frac{(R_{off} - R_{on})\, w}{D} \qquad (3.5)$$

where, R_{off} is the device resistance when w = zero. Because of the device non-linearity, (3.5) is not valid at the device boundaries. Therefore, the system memristance described as [90],

$$R(w) = \frac{R_0}{w_0} \left[\, w_0 - \frac{\mu_v \rho}{A} \int_0^t i(t)\, dt\, \right] \qquad (3.6)$$

where, R_0 and w_0 are the resistance and width of un-doped region respectively, ρ is the resistivity of the TiO_2, A is the cross-section area, and i is the current passing through the device. Accordingly, memristance is not discrete, instead it is

25

continuous over the time.

Based on (3.6), memristance depends on the device parameters such as, material resistivity, the cross-section area, and the width of the doped region to the width of the un-doped region . Respectively, These parameters determine the maximum and the minimum limitations of the device resistivity.

Similarly for spintronic memristors, the device memristance is based on two factors: the ratio between the two segments length in the free layer, and the magnetization direction in the free layer with respect to the magnetization direction in the reference layer. Ignoring the domain-wall thickness (x), if w = D, then the magnetization direction in the free layer and the reference layer will be anti-parallel, and hence the system resistivity will be high (R_H). On the other hand, if w = zero, then the magnetization direction in the free layer and the reference layer will be parallel, and the system resistivity will be low (R_L). Generally, the system memristance M(w) can be described as [17],

$$M(w) = [\ R_H \times w + R_L\ (D - w)\ ] \tag{3.7}$$

As the domain-wall position (w) is a function in the domain-wall velocity and the passing current, then it can be described as [17],

$$w = \Gamma_v \int_0^t i_{eff}\ dt \tag{3.8}$$

$$\text{as,} \quad i_{eff} = \begin{cases} i & i \geq i_{cr} \\ 0 & i < i_{cr} \end{cases}$$

where, i_{eff} is the effective current, and i_{cr} is the critical current value after which the domain-wall will start moving. Accordingly, (3.7) can be rewritten as,

$$M(w) = [\ R_L \times D + (R_H - R_L)\ \Gamma_v \int_0^t i_{eff}\ dt\ ] \tag{3.9}$$

Therefore, the applied current can not change the system memristance until it is equal to or greater than the critical current value. Hence, a small sensing current can be used for reading the stored data without disturbing it.

As shown in (3.9), the system memristance depends upon the current integration which makes it continuous over the time.

5. High data density

Because of the device nano-scale, TiO_2 memristor has better scalability than CMOS technology, which means more devices can be arranged in the same area that is used for the known CMOS technology, and hence more data can be stored. Besides, the device memristance continuity makes it possible to store multiple bits instead of one bit as in the conventional memory devices.

Another important feature of the device is the ability to be vertically stacked given more devices to be arranged, and hence more data to be stored [10].

Also, spintronic memristor is a nano-scale device, therefore more devices can be arranged in less area than the known CMOS technology, subsequently more data can be stored. Furthermore, the device potentiality to store multiple bits in the memristance range gives the system higher data density.

6. Frequency response

As predicted by Chua, there is a reverse relation between the device non-linearity and the frequency. Both TiO_2 and spintronic memristor applying this relation as shown in Figure 3.11 and 3.8, respectively. Increasing the frequency of the external applied voltage leads to a smaller $q(t)$ with respect to w(t), thus the hysteresis behavior of the memristor is decreased until asymptotically passing over to the characteristic curve of the conventional resistor [91].
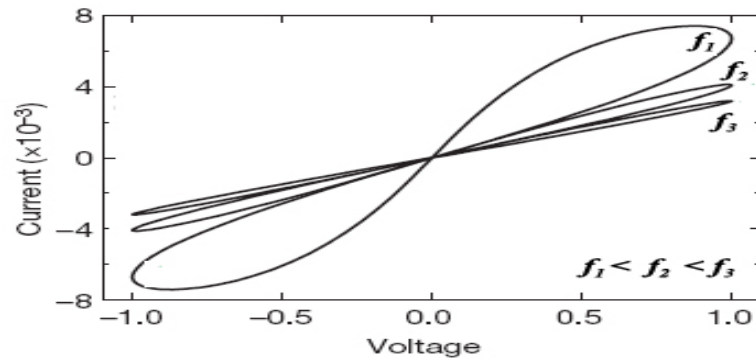
Figure 3.11: Applying symmetrical alternating-current voltage bias results in double-loop I-V hysteresis that collapses to a straight line for high frequencies [9].

7. Asymmetry ON/OFF switching behavior

The time needed for OFF and ON switching is noticed to be different in TiO_2 memristors, as the OFF switching is slower than the ON switching for the same applied voltage. This attitude is due to the interaction of diffusion and drift on the internal electric field [86].

Starting with the OFF state (high resistance state), when applying positive voltage on the top electrode in Figure 3.5-b, the positively charged oxygen ions are repelled toward the bottom electrode, and thus the doped layer increases. This increasing will increase the diffusion current acting in the opposite direction to the drift current as stated in Fick's law, also the internal electric field is opposite to the applied field, and hence the ions slow down. Eventually, the total velocity goes to zero, and hence the maximum value of w is reached. On the other hand, when a negative bias is applied on the top electrode in Figure 3.5-b, the externally applied field, the internal field of the oxygen ions, and the diffusion current will all act in the same direction, thus dramatically speeding up the OFF switching compared to the ON switching for the same applied voltage [86] as seen in Figure 3.12.

This asymmetry behavior is not present in spintronic devices, where the ON/Off switching behavior is the same for the same applied voltage.

27
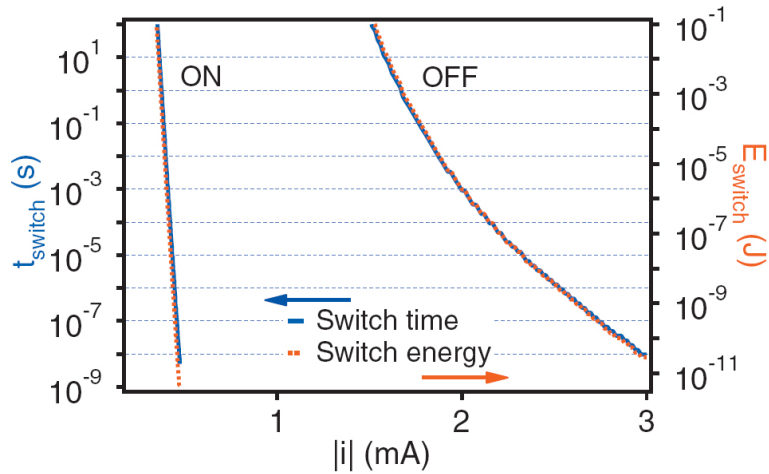
Figure 3.12: Calculations of switching time and energy using constant-current magnitude switching times for ON and OFF switching events. The ON and OFF states are chosen as w_{on}=1.2 nm and w_{off}=1.8 nm to reflect a resistance switching ratio of 500. These results demonstrate the asymmetry between the ON and OFF switching behavior and show that the switching energy decreases exponentially with the applied current [87].

Despite that TiO$_2$ device achieves most of the memristor characteristics predicted by Chua, it does not provide a direct relation between the magnetic flux (φ) and the charge (q). According to Sally Adee [10], "The actual definition of memristance is more general. Linking electric charge and magnetic flux is one way to satisfy the definition, but it is not the only one. In fact, it turns out you can bypass magnetic interaction altogether. Chua's general memristance definition has two parts. The first equation defines how the memristor's voltage depends on current and a state variable, that is a quantity that measures some physical property of a device. The second equation expresses how the changing state variable (the TiO$_2$'s thickness in this case) depends on the amount of charge flowing through the device". Also, because of the device nano-scale dimensions, the device fabrication is complex and faces some issues when merged with CMOS technology.

On the other side, spintronic memristor provides a direct relationship between the charge (q) and the magnetic flux (φ). This relation rises from the fact that spintronics utilizes the intrinsic spin of the electron and its associated magnetic moment, in addition to its fundamental electronic charge in solid state device [2].
Despite spintronic memristor advantage, it is more difficult to be fabricated because of the presence of the moving domain-wall. Till now there is no announcement about the release date of a physical realization of the spintronic memristor or even the material that will be used in the fabrication process. Also, i_{cr} in (3.6) is considered as an intrinsic electrical parameter, and hence an experimental calibration is needed to determine its value. Besides, Γ_v in (3.6) is related to the device structure which means any structure variation in the fabrication process will affect the memristance value. Also, thermal magnetic noise, which rises from thermal fluctuation, is another issue faced by spintronic memristor. Thermal magnetic noise represents the main source of noise and limitation on the recording density [88].

Table 3.1: Comparison between TiO_2 thin film and spintronic memristor.

Comparison aspect	TiO_2 thin film	spintronic memristor
width, length, thickness (nm)	40-50, 40-50, 3-30	10-20, 130-1000, 7-70
Data Denisty (Gbit/cm^2)	62-776	2-102
System state variable	Doped region width	Domain-wall position
I-V hysteresis loop	Close to the one predicted by Chua	Not close to the predicted one
Consumed energy	Lower than known flash memory	Close to the known flash memory
R_{on} to R_{off} ratio	1000	1.2
Current-Voltage relationship	$\frac{R_0}{w_0}\left[w_0 - \frac{\mu_v \rho}{A}\int_0^t I(t)\,dt \right]$	$R_L \times D + (R_H - R_L)\,\Gamma_v \int_0^t i_{eff}\,dt$
Access Time	very low	low
Integration with CMOS	Needed new technology	Many technologies exist
q to φ relationship	Not direct relation	Direct relation
Fabrication flexibility	Difficult	Too difficult
Experimental calibration	Not needed	Needed
Reading device memristance	Difficult	Easy
Thermal Noise	Does not affect	Affect

Because of the devices nano-scale (i.e., TiO_2 and spintronic memristor), manufacturing process fluctuation control is a key challenge. Accordingly, the electrical characteristics of both devices will be varied. However, as both memristors are thin film deposition based technology, the local randomness of random discrete doping (RDD) is not considerable as geometry variations [90].

It is detailed in [90], based on the latest line edge roughness (LER) characterization method for electron beam lithography (EBL) technology from top-down scanning electron microscope (SEM) measurement that, thickness variations show much more significant impact on the memristive behavior such as voltage drop and the change in memristance in TiO_2 thin film, while the impact of LER on the memristive parameters in spintronic memristor is larger than thickness variations [90].

3.5.3 Summery of the Comparison

In light of the previous discussion, Table 3.1 gives a brief comparison between the TiO_2 and spintronic memristor. As noticed from Table 3.1, TiO_2 memristors have smaller size and hence more data can be stored. Also, it has faster access time than spintronic memristors and better switching characteristics because of the large R_{on} to R_{off} ratio. On the other hand, spintronic memristors can be easily integrated with CMOS technology. Also because of the presence of critical current (i_{cr}), memory cells based on spintronic memristor have

better capabilities for reading the stored data without disturbing it. Therefore, the TiO_2 memristor is adopted through this thesis.

Chapter 4: Memristor Models and Applications

A lot of well evidenced circuit implementations based on TiO$_2$ thin film memristors have been published. For facilitating these applications and availability testing, different memristor models based on the real device published data were submitted [33, 92–97]. These models can be classified into three main categories, mathematical models to facilitate the device simulation within the Matlab simulation tools, Spice models, and Verilog-A models for device simulation with spice tools like Cadence Spectre tool.

The device applications cover both digital and analog domains [26, 28, 68, 98–104]. Memristors used in digital circuit applications like non-volatile memory, signal processing, programmable logic, and control systems. Furthermore, memristors are potentially used for stateful logic implication, allowing a replacement for CMOS-based logic computation. In the analog regime, memristor based applications depend on the availability of continuously programming the device impedance. In this domain the device is used in applications concerned with analog signal processing, learning circuits, programmable analog circuits, and neuromorphic circuits. Below, such models and applications are discussed, showing the most promising ones.

4.1 Memristor Models

4.1.1 Mathematical Models

An analysis of the existing submitted memristor mathematical models were discussed in [92], where the predicted behavior of memristor using these models is compared to the real device published properties. Three main models (i.e., Linear model, nonlinear model, and exponential model) were analyzed, compared, and converted into Matlab code in [92]. Linear model is the basic model where the TiO$_2$ thin film memristor is considered as a linear device. This model suffers from two main shortcomings, first the state variable (i.e., width of the doped region (w)) is not bounded by the device limitations (i.e., zero and the device total length (D)). Besides, the model does not take into account the device non-linearity [92]. As a trial to deal with memristor non-linearity property, a nonlinear model was presented. It adds a non-linear window function $F(x)$ (i.e., Strukov, Joglekar, or Biolek window function) to the state variable to bound it within the device boundaries. Biolek's window function is added to the state variable. In this way, the reversed bias will move back the state variable after reaching either boundary, and hence the window function behaves differently in each voltage bias direction [92]. A more advanced model (exponential model) is also discussed. The exponential model fully fits the experimentally measured I-V characteristic curve of memristor, where at the OFF state the I-V curve behaves like a P-N junction, and at the ON state the I-V curve follows a tunneling process [92]. These models (i.e., Linear, Non-linear, and Exponential model) are briefly compared in Table 4.1.

31

Table 4.1: Summery of the comparison between the three models discussed in [93].

Comparison aspect	Linear	Nonlinear	Exponential
Bounded by boundary condition	No	Yes	Yes
Using Window function	No	Yes	Yes
Non-linearity	Linear	Nonlinear	Highly nonlinear
Sensitivity to voltage	Linear	Linear	Nonlinear
Switching Time	Symmetric	Symmetric	Symmetric (polarity-dependence Resistance)

4.1.2   Spice Models

A lot of spice models had been developed and published in the literature to simulate the device behavior [91, 93–96]. The submitted model in [93] had been developed and tested on simple circuits (i.e., low pass filter and integrator circuit) while the results are compared with the expected ones. The submitted I-V characteristic curve is similar to the predicted normal hysteresis loop of TiO_2 thin film memristor, however the model does not bound the state variable changes within the device limits.

A better model was submitted in [94], where the state variable change is limited to the device boundaries because of the usage of window function. Also, the hysteresis loop becomes more linear as the applied frequency increases. Therefore, the resulting output compared with the real device published hysteresis shows much similarity, especially at the hard switching conditions. The main disadvantage of the submitted model is that, generally it is not safe to let the Spice engine determine the initial values of the memristor automatically, because it can cause unstable and invalid simulation [94].

One of the most popular spice models in the literature is the one published in [95]. The model managed to model the real I-V curve, where the hysteresis loop becomes linear as the frequency increases and also have asymmetric ON/OFF switching time as the OFF switching time is slower than the ON switching time. This model is developed as a spice subcircuit with parameters like the initial resistance (R_{INIT}), the device OFF and ON resistances (R_{OFF} and R_{ON}), the width of the thin film (D), the dopant mobility μ_v, and the exponent p of the window function, where this parameters value can be passed to the subcircuit as an argument [95]. Besides, the model concludes the direct computation of the time integrals of electrical voltage (flux) and of electric current (charge), which define the memristor. The main issues of this model are the modulation of the boundary effects and the difference between the behavior of the model in some concrete regimes of the operation and the anticipated behavior of the real circuit element [95]. The authors refer the boundary effect issue to the used window function, where a new window function that solves this issue was submitted. For the difference in the behavior in some regimes, the authors thought it may be due to the current method of modeling nonlinear dopant drift [95].

A comparison between the three models is drawn in Table 4.2, where model 1 represents the model submitted in [93], model 2 represents the model submitted in [94], and model 3 represents the model submitted in [95].

Table 4.2: Summary of the comparison between the three spice models submitted in [94-96].

Comparison aspect	Model 1	Model 2	Model 3
Bounded by boundary condition	No	Yes	Yes
Using Window function	No	Yes	Yes
Frequency response	Not affect	Affect	Affect
Switching Time	Symmetric	Symmetric	Asymmetric
Spice code	Absent	Present	Present

4.1.3 Verilog-A Models

A Verilog-A code had been written for different published models (i.e., Linear, Non linear ion drift, and Simmons tunneling barrier model) and submitted in [97]. In addition, a new computationally-efficient memristor device model, based on modification and simplification of Simmons Tunnel Barrier Model [105] (one of the most accurate memristor models in the literature at the expense of long computational time), is proposed to fit the TiO_2 thin film memristor. A comparison between these different models is drawn in Table 4.3.

Table 4.3: Summary of the comparison between different memristive device models submitted in [98].

Comparison aspect	Linear ion drift	Nonlinear ion drift	Simmons tunneling barrier	TEAM
State variable	$0 \leq w \leq D$ Doped region physical width	$0 \leq w \leq 1$ Doped region normalized width	$a_{off} \leq x \leq a_{on}$ Undoped region width	$x_{off} \leq x \leq x_{on}$ Undoped region width
Control mechanism	Current	Voltage	Current	Current
I-V relationship	Explicit	Explicit	Ambiguous	Explicit
Matching memristive definition	Yes	No	No	Yes
Model accuracy	Lowest	Low	Highest	High

Among all the proposed Verilog-A models in [97], this work will basically adopt Threshold Adaptive Memristor Model (TEAM model) in all of the following simulations due to the following reasons:

1. **Model simplicity, generality and flexibility**
   TEAM model adopts simple and easy-to-understand equations to model the memristor device and exhibit some fitting parameters. These fitting parameters make it easier to expand the model to handle different material characteristics in order to model other memristor devices.

2. **Computationally-efficient, and Sufficiently-accurate model**
   TEAM model is one of the fastest memristor device models in the literature [97]. Simmons tunnel barrier is the best known accurate physical model of TiO_2 memristive devices [86, 97]. However, this high accuracy of the Simmons model makes the model complex and difficult to manipulate. TEAM model is based on the simplification of the Simmons model to provide high-accuracy and short computational time. The average error of the TEAM model compared to the Simmons model is 0.2% [97].

3. **Model Suitability for circuit design**
   Since the TEAM model is implemented in Verilog-A hardware description language, it is suitable to be integrated in Spice simulations.

The selection of the TEAM model to simulate the memristor behavior is based on conducting a comprehensive test on different memristor models. The test results proved the previous advantages of the TEAM model over other models proposed in [97]. Another important concern of the model is the window function utilization. As discussed earlier, the window function is used to fit the boundary conditions and due to the significant nonlinearity variations in w, the used window affects the performance of the model. Therefore, a comprehensive test on different proposed window functions in [97] and its effect on the model performance has been conducted to select the proper window function with respect to the chosen model. TEAM window shows better performance, better nonlinear dopant drift at device boundaries, and better nonlinear I-V characteristics when integrated with the TEAM model as compared to other literature window functions used in [97]. Accordingly, the TEAM window is selected to be adopted with the selected TEAM model for all the after-mentioned simulations.

4.2   Memristor Applications

As memristor-based technology provides much better scalability and overall lower power consumption, many memristor-based applications were submitted in the literature like,

1. Neuromorphic circuits
   One of the most important and exciting applications is neuromorphic circuits. Neuromorphic circuits are meant to emulate the human or animal brain. In neuromorphic circuits, memristors are used as synapses which connect neurons to each other and store information. As discussed in Chapter 3, the nano size of TiO_2 memristor is

very valuable for this application since the intensity of memristors in a chip needed to be the same of the intensity of synapses in human brains [106]. Thus, using memristors in the fabrication of an artificial neural network of a small size such as the biological brain becomes possible.

A remarkable property of biological synapses is the spike-timing-dependent plasticity [107]. In reality, when a post-synaptic signal attains the synapse prior to the possible action of the pre-synaptic neuron, the synapse offers long term depression (LTD), specifically its strength decreases based on the time difference between the post-synaptic and the pre-synaptic signals. On the contrary, when the post-synaptic possible behavior attains the synapse after the pre-synaptic possible behavior, the synapse goes through the long-time potentiation (LTP), specifically the signal transmission between the two neurons increases as the time difference between the pre-synaptic and the post-synaptic signals increases. This general description of biological synapses may be implemented using memristors [108]. There are three different aspects in artificial neural networks: using an overlap of asymmetric pulses [106, 108], employing additional CMOS circuitry to track pulse timing [99], and utilizing higher-order memristive systems with intrinsic pulse-timing tracking capability [108].
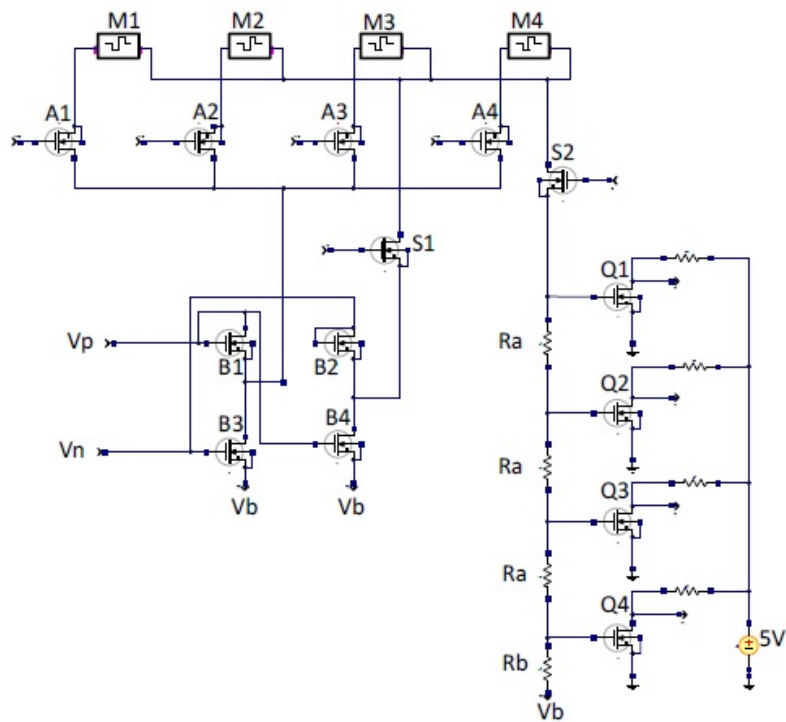
Figure 4.1: Memristor read and write circuit that incorporates the circuits discussed in the previous sections [102].

Recently, different circuits exhibiting neuromorphic disposal of different types and complexities based on memristors were submitted [28, 99–101]. In [101] a Read/Write circuit for neuromorphic applications was introduced as shown in Figure 4.1. The submitted circuit has the capability for dialing with multiple spikes, where the write circuit responsibility is to shift the state variable with an amount equal to

the applied spikes. There are two different polarities of the applying spikes, where the positive one increase the state of the device and the negative one decrease it. While for the reading process, reading pulses are applied to read the stored data. In this architecture CMOS transistors were used as switches for writing to or reading from the selected device. Also it is used for comparing the reading impedance with several resistance and hence determine the stored data. The authors proved their circuit capabilities by simulations, where Matalb is used for applying the synapses on their own memristor model in the Cadence Spectre simulation tools.

2. Signal Processing

A signal processing system is known to be realized by attaching a crossbar array with programming circuitry and signal input circuitry, which provide a linear transformation from a set of input signals, to a set of output signals.

As memristor resistance can be continuously programmed by the amount of the applied stimulus, memristors can be used as a practical realization for a fine-resolution programmable resistor that is needed by many different circuit implementations for supporting multi-standards. Also, it is used as a compensation for process, voltage, and temperature (PVT) variations [102]. Furthermore, memristors act like linear resistors for high frequency input signals, while showing unique properties for low frequencies. Applications like waveform generation, signal filtering, communications, and pattern recognition take advantage of this unique property of the memristors. Such applications were submitted in [26, 68, 102].

An Ultra Wide Band (UWB) receiver had been developed and submitted in [68]. The remarkable procedure of this coherent receiver is the comparison between the reference waveform and the received waveform. The correlation operation of the reference signal with the input signal is elaborated and the output of this computation is used directly. As displayed in Figure 4.2, the UWB receiver is formed of N equal steps, each step proceed an n part of the input signal. The receiving process passes by four steps. In the first one, the reference waveform is stored in the N capacitors, while all the memristors state programmed by V0. For programming memristor state by V0, memristors terminals are connected to V0 and the ground for a sufficient time. Then, the stored voltage on the capacitors are used for programming the memristors. In the third step, the RF signal is passed through the transmission line. Finally, the switches labeled with number '4' get closed and the resulting current at the output is measured.

A programmable gain amplifier was introduced in [102]. As shown in Figure 4.3, the amplifier is designed with 0.18 μm CMOS process together with a memristor. The memristor is used as a programmable impedance to facilitate programming the load resistance and hence the output voltage gain. To control the load memristor impedance, a coded pulse train is used to adjust the memristance value and hence the amplifier gain. The only limitation of this design is the limited switching speed of the memristor. This limitation comes from the fact that, the driving frequency is needed to be higher at least 10 times than the minimum required frequency for fully switching the memristor. In this way, the memristor can be considered as a linear programmable resistance holding its last programming resistance value.

36
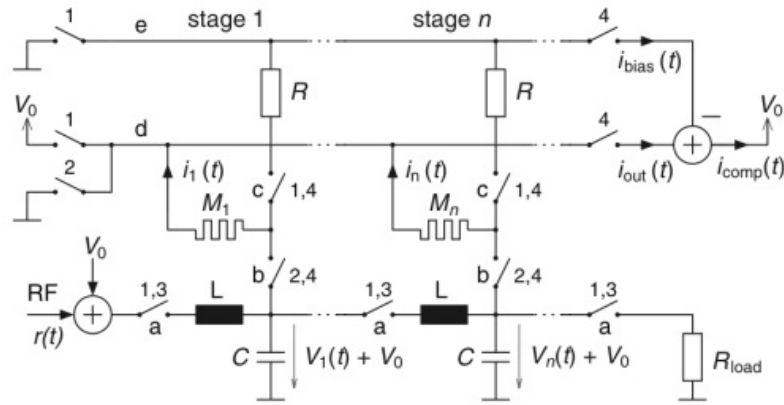
Figure 4.2: UWB recevier circuit diagram submitted in [68].
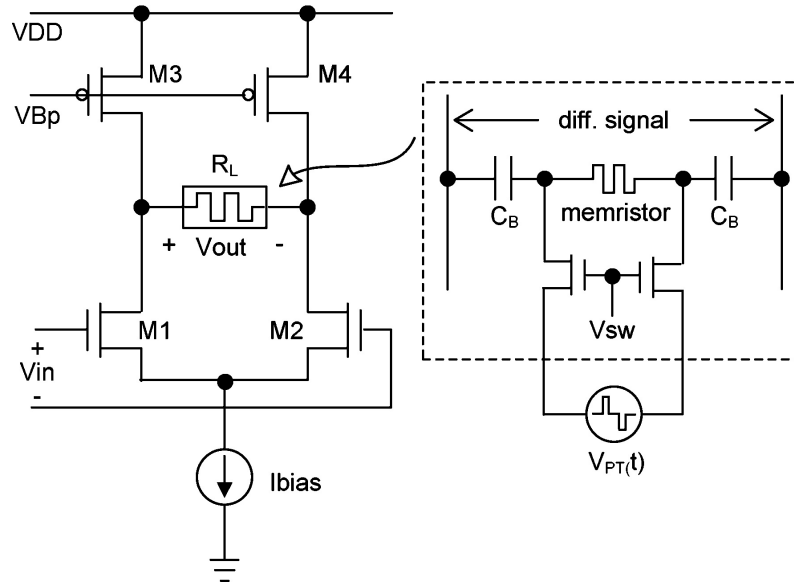
Figure 4.3: Circuit schematic of programmable gain amplifier using memristor, where R_L is the equivalent resistance of the pulse-programmed memristance [103].

3. Logic Circuits

   Another important application of memristors is the logic circuit realization. Memristors are used as switches and/or programmable resistors in a data routing network, and even can be used to carry out logic operations. A potential of using hybrid CMOS/nanoelectronic (CMOL) circuits have been used in the field of image processing [103] and field-programmable gate array (FPGA) [104]. CMOL low level structure is shown in Figure 4.4. Based on efficiency analysis, memristive FPGAs have much better energy efficiency and faster when compared with similar circuits based only on conventional COMS technology [98].

   In particular, [109] presents a memristor-based re-configurable Field Programmable Gate Array (mrFPGA) as shown in Figure 4.5. The submitted design depends on the existing CMOS compatible memristor fabrication process. The conventional FPGA suffers a lot from its programmable interconnects. One reason of this issue is the substantial use of SRAM as the programming bits, multiplexers (or pass transistors),
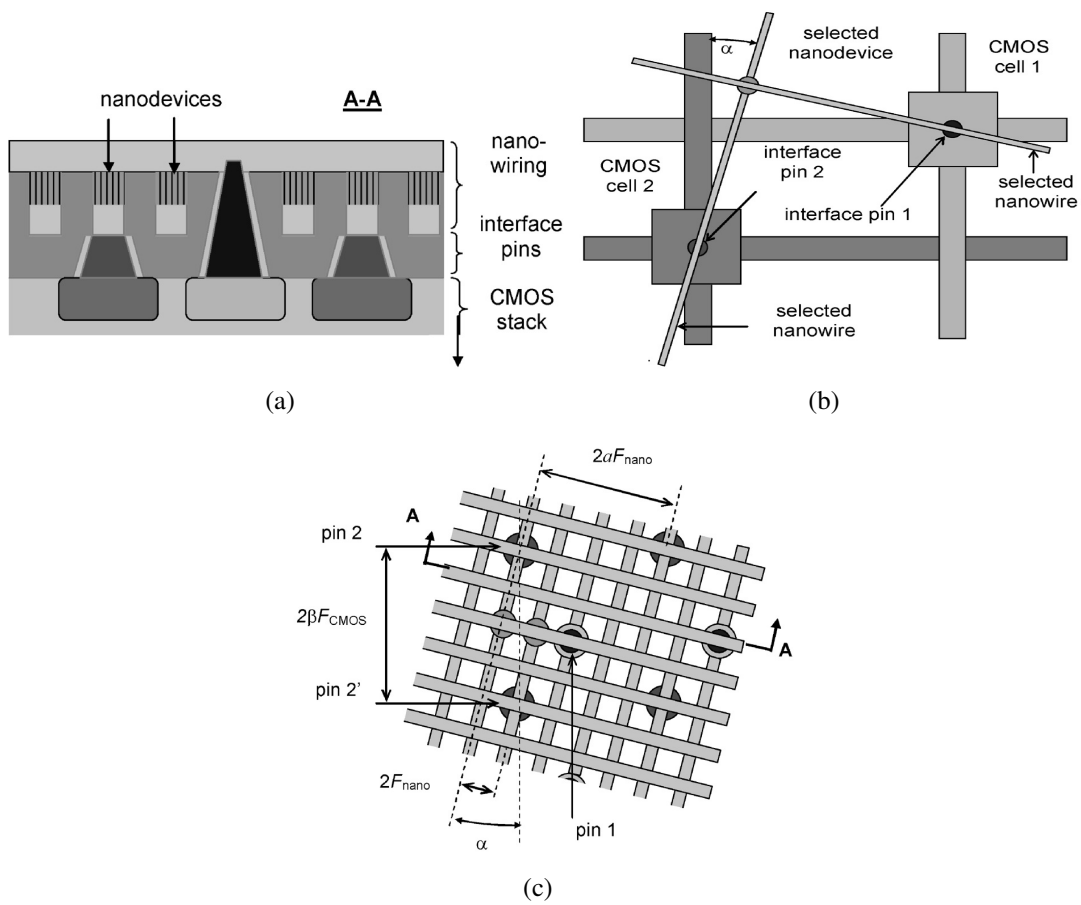
Figure 4.4: Low-level structure of the generic CMOL circuit: (a) schematic side view; (b) the idea of addressing a particular nanodevice, and (c) zoom-in on several adjacent pins to show that any nanodevice may be addressed via the appropriate pin pair [105].

and buffers in the interconnects. As known, an SRAM cell has six transistors and has the possibility to only store one-bit of data. Therefore, the needed area for the storage circuit is large leading to area overhead for the FPGA programmability and hence an extended routing path and larger interconnect delay. Besides, SRAM is a volatile memory device, which means that the device consumes power even during the stand-by. With the novel use of memristors in mrFPGA interconnects rather than memory cells, the proposed architecture reduces the gap between FPGAs and Application Specific Integrated Circuits (ASICs) in area, delay, and power [109].
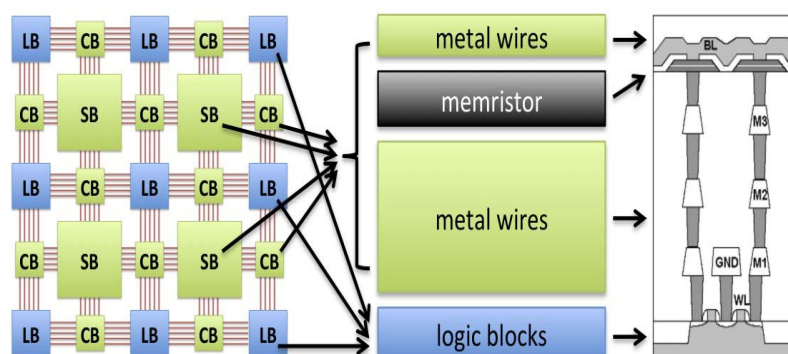
Figure 4.5: mrFPGA architecture: The programmable routing structure is built up with metal wires and memristor which are fabricated on top of logic blocks in the same die according to existing memristor fabrication structures [109].

Using only memristors and metal wires as the programmable interconnects in mrFPGA allows the fabrication of interconnects over logic blocks and hence a considerable reduction in the total area and interconnect delay [109]. The main issue of this design is the absence of buffers. Consequently, the increase of the interconnect distance leads to a quadratic increase in the interconnect delay. However, this issue may undermine the benefit brought out by the significant reduction of the overall area and interconnect delay in the case of large FPGAs but the authors addressed this issue and submitted an improved mrFPGA in [109], where an adaptive buffer insertion in the interconnects was possible. To get the optimal solution of insertion choice for each buffer in the routing network, the authors suggested using an idea from the buffer placement algorithm in ASIC [109]. By using this algorithm, it is easier to decide the best positions of the buffers in the interconnects of an mrFPGAs, where dynamic programming is used to achieve the lowest interconnect time delay. Evaluating area, performance, and power consumption of mrFPGA based on the 20 largest MCNC benchmark circuits, show that mrFPGA achieves 5.18x area savings, 2.28x speedup, and 1.63x power savings over conventional FPGAs [109].

4. Digital Memory
The non-volatile digital memory is the most straightforward and underdeveloped application of memristors. Memristors are expected to replace Flash memory in the near future [40], therefore the newly research efforts are mainly concerned with this digital memory application development [12, 46, 47, 85, 110]. Actually, based on the device characteristics, storing the data on the device can be easily encoded within the memristive state as, for example, the low resistance state represents logic

'1' while the high resistance state represents logic '0'. Also, as the variation in the device's resistance is continuous, there is an opportunity for using the device as a multistate memory device [111, 112].

Figure 4.6 portrays a single bit Read/Write circuit that had been proposed in [12]. This circuit is based on memristor device analysis and mathematical modeling that had been introduced in [12]. A Read/Write enable switch is used to control whether Read or Write operation is to be performed. The write circuit is used to change the state of the memristor device by connecting the writing voltage source to the device terminals. For the reading process, the circuit is divided into two stages, convert stage and sense amplifier stage. During the convert stage, the stored data is measured and interpreted as a voltage signal that is amplified and converted to a digital output through the sense amplifier stage.
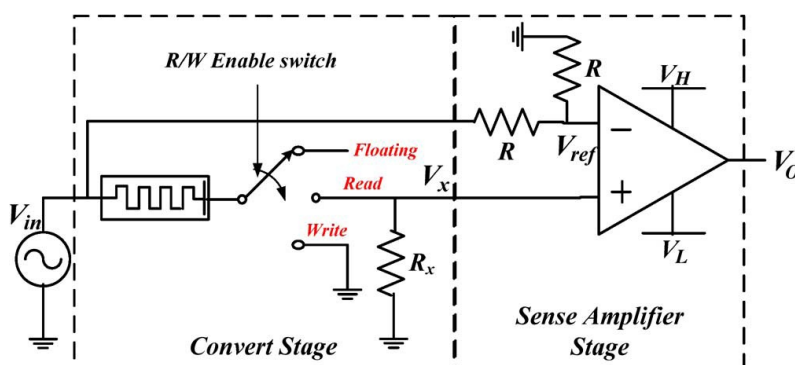
Figure 4.6: Circuit architecture of the Memristor-based memory cell. Read/Write (R/W) enable switch is connected to ground for writing process and is switched to V_x for the reading process. The comparator in the sense amplifier stage compares V_x with the reference voltage $V_{ref} = 0.5 \times V_{in}$. If $V_x > V_{ref}$, the output voltage $V_o = V_H$ which represents logic '1'. Similarly, $V_o = V_L$ if $V_x < V_{ref}$ [13].

Despite its simple operation, the circuit has several disadvantages concerning the used read pattern and its effect on the internal state which will be discussed in details later on. In [12], solutions had been suggested to these issues such as limiting the stored data level so that it does not reach the device boundary or utilize a refreshment circuit to return the internal state of the device to its nominal value. It is also stated in [12] that, the circuit can be used in SRAMs by using the same peripherals used with the conventional CMOS technology.

An adaptive Read, Write, and Erase method is adopted in [47] for a memristor-based crossbar memory array as shown in Figure 4.7. First, models for the device parameters and the crossbar array components parameters (i.e., memristor width, dopant mobility in the device, MUX/DEMUX, Metal-Insulator-Metal (MIM) diodes, and nano-wire characteristics), are presented. Based on these models, a functional Verilog-A model is developed and utilized to simulate the whole circuit.

As displayed in Figure 4.7, Reverse Polarity (RP) is used to select the flow path of the current according to its connection with the data and Read circuitry. By this method the current can flow in both directions and the requirement for a negative voltage signal is avoided. In other words, instead of using positive and negative

40

voltage signal to program the memristor, the flow of the current in both directions through the memristor device is capable of performing the same operation.

Read circuitry is the key idea of the whole circuit design as it is used to read from and write to the device. It is a generic block used to equalize, charge, and sense the output to determine if the device is switched ON or OFF. Operation of reading the state is performed in two cycles. In the first cycle, the current flows to determine the state while in the second cycle, the current flows in the opposite direction to restore the initial state. According to this destructive reading, the need for a refreshment process is a must for this design. After sensing the data, the output is supplied to the sense amplifier to define the data as a full swing digital output.

In fact, the utilization of the read circuit for the writing process makes the number of read cycles needed to write logic '1' different from the number of cycles needed to write logic '0'. Hand calculations show that, the device needs almost 21 read cycles to write logic '1', while it only needs 6 cycles to write logic '0'. Analysis of the circuit has shown that, it is better to enlarge the difference between the two states, so that the device does not reach the high state (logic '1') until w = D, where D is the device total width of the TiO_2 thin film and w is the width of the doped region, or the low state (logic '0') until w = 0.

Simulations are conducted on a 16 x 16 crossbar showing the advantage of using MIM diode to isolate the individual devices in the array. Another approach to limit the leakage current by applying a reference voltage on the selected and unselected devices is also presented. In this circuit, V_{ref} is connected to the memristor device under operation whereas other memristor devices are connected to the ground.
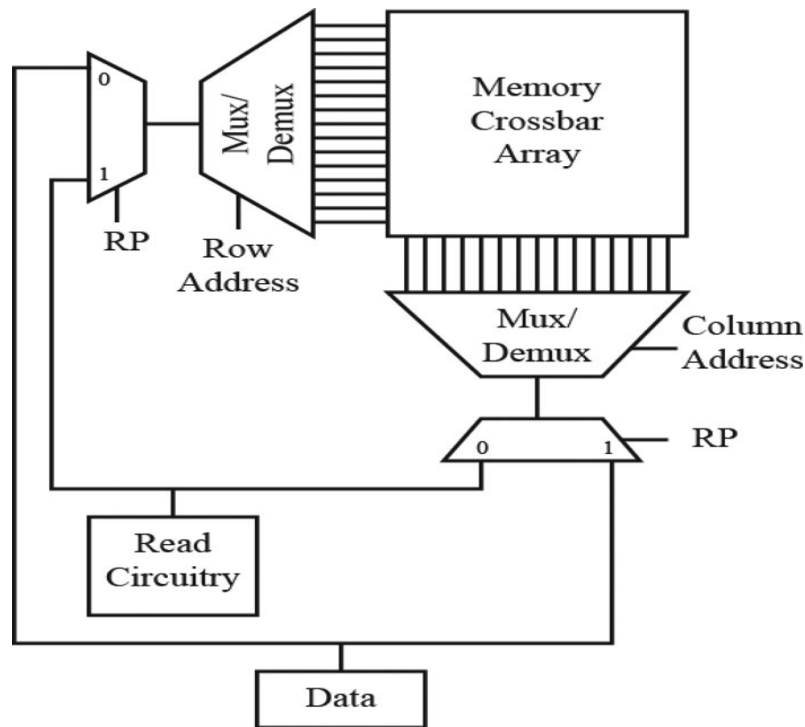
Figure 4.7: Top level block diagram of the circuit proposed in [110].

Another memristor-based memory design was introduced in [110]. The authors

introduced an observation about the memristor's asymmetric energy consumption by detailed analysis of the transient power consumption. Based on this perception, a dual element memristor based memory is introduced. Memory cell consists of two memristors where one is used to store the data as it is written and the other is used to store the complementary data. Each memristor is individually written. While in the reading process, both memristance values are compared to read the stored data. Based on energy optimization and partial programming, authors in [110] presented four different optimization schemes where one scheme was claimed to save the energy by 80%. Also, [110] introduced different optimization schemes for speed and resistance distinguishability to apply on the dual element circuit to make it suitable for different applications as each one of these schemes provided a solution to one of the memristor design constraints (i.e., resistance distinguishability between the high resistance and low resistance, reading or writing latency, voltage usage for reading or writing memristors, and energy consumption). Each one of those schemes has its advantages and drawbacks which make it suitable for some applications and not suitable for others.

Chapter 5: Memory design insights and new proposed circuits

In this chapter Memristor-based Memory Design Insights are discussed. Based on this insights, three Read/Write memristor-based memory cells are proposed.

5.1 Memristor-based Memory Design Insights

5.1.1 Design Considerations

In light of the device analysis introduced in Chapter 3, the design considerations of using a memristor in the realization of a memory cell are summarized as follows:

1. **Nano-scale constraints**
   Because of the device nano-scale, the oxygen atoms are free to move inside the device with a sensible rate, where the device resistance is changing according to this movement. On the other hand, manufacturing process fluctuations control is a key challenge. It is detailed in [90], based on the latest line edge roughness (LER) characterization method for electron beam lithography (EBL) technology from top-down scanning electron microscope (SEM) measurement that, thickness variations show significant impact on the memristive behaviors such as voltage drop and the change in the memristance value. Also, integration of the device with CMOS technology may face some issues because of the differences in the devices scales.

2. **Bipolar device**
   As the device state depends on the direction of the passing current, hence good attention should be given to the current direction passing through the device during the reading process, the writing process, or the idle state. Otherwise, a wrong data may be written or erased during such processes.

3. **Device non-volatility**
   Memristors store the data as a resistivity. This resistance depends on the oxygen atoms movement, which is caused by the applied stimulus. Thus, if this stimulus is switched off, the oxygen atoms keep its last position. The non-volatile advantage of the device, which makes the device a good candidate for memory applications, may be lost during the memory cell design. This loss comes from designing a memory circuits based on volatile elements (i.e., Latches) beside the memristor.

4. **Consumed energy and time**
   The main important constraints in any electronic system design are the energy consumption (E) and the response time (t). The consumed energy can be computed as in [86]:

$$E = \int \frac{i \times v(w)\, dw}{\dot{w}} \qquad (5.1)$$

From (3.2) and (5.1), it is obvious that the consumed energy (E) decreases exponentially as the current passing through the device (i) increases. Accordingly, the heat is decreased. Also, the time required to switch a device between two states ($\triangle t$) can be computed as in [86]:

$$\triangle t = \int \frac{dw}{\dot{w}} \qquad (5.2)$$

which indicates, due to (3.1), (3.2), and (5.2), that the time decreases exponentially as the applied current increases. Figure 3.12 shows the relation between the applied current (i), the consumed energy (E), and the switching time (t).

Therefore, writing logic '1' may need more voltage than writing logic '0'. This is because the nonlinear memristor I-V characteristics as illustrated in Figure 3.6.

5. **Memristance swithing**
Migration between doped region low resistance and un-doped region high resistance represents the system resistivity, named system memristance as in (3.6). Accordingly, memristance is not discrete, instead it is continuous over the time.

It is important to mention that, the electrodes nano size results in a series resistance in the range of kOhms, while the device ON resistance is in the range of Ohms. Therefore, the series resistance is larger than the device ON resistance and hence, the device (i.e., switching material TiO_{2-x}) consumed more current to reset [113]. This consumed current results in increasing the power consumption.

6. **High density memories design**
Because of the device nano-scale, memristor has better scalability, which means more devices can be arranged in the same area that is used for the known CMOS technology, and hence more data is stored. Besides, device memristance continuity makes it possible to store multiple bits instead of one bit as in conventional memory devices.

7. **Frequency response**
There is a reverse relation between the TiO_2 memristor non-linearity and the frequency as shown in Figure 3.11.

Therefore, using a higher frequency input source degenerates the device non-linearity, and hence make the system design easier.

8. **Asymmetric ON/OFF switching behavior**
The time needed for OFF and ON switching are noticed to be different, as the OFF switching time is slower than the ON switching time for the same applied voltage as shown in Figure 3.12. This attitude is due to the interaction of diffusion and drift on the internal electric field [114].

9. **Stimulus dependence**
Memristance value depends on the total charge injection regardless the source shape, this fact comes from the device unique signal processing criteria. The only thing that matters is the net applied injection and the period of the applied stimuli.

5.1.2 Memristor in Memory Arrays

Memristor nano-sizing and its attractive non-volatile criteria make it an appealing memory solution that might finally replace the presently used flash memory and SRAM. As the memristor is a modest two-terminal nano device that can be used to store multiple bits, it can be used to create a crossbar memory structure with extremely high density, leading to an extra data storage solution than the known memories.

Utilizing the memristor in a crossbar memory array is not an easy task because of its accumulative property. Based on the non-idealism of the devices used in the memory array structure and its consequence (i.e., sneak paths and leakage current), memristor internal state may dramatically change and hence the stored data.

Sneak paths effect is decreased by connecting the unused rows and columns to the ground instead of leaving them floating as displayed in Figure 5.1. Grounding these rows and columns set routes for the sneaking currents to the ground instead of the memory elements. This solution will just limit the sneak paths effect not totally eliminate it because portion of the sneak current will find its direction to the ground through the memory elements. However, this solution decreases the total system resistance as these ground paths act as parallel resistances across the system and hence the equivalent system resistance decreases [66].
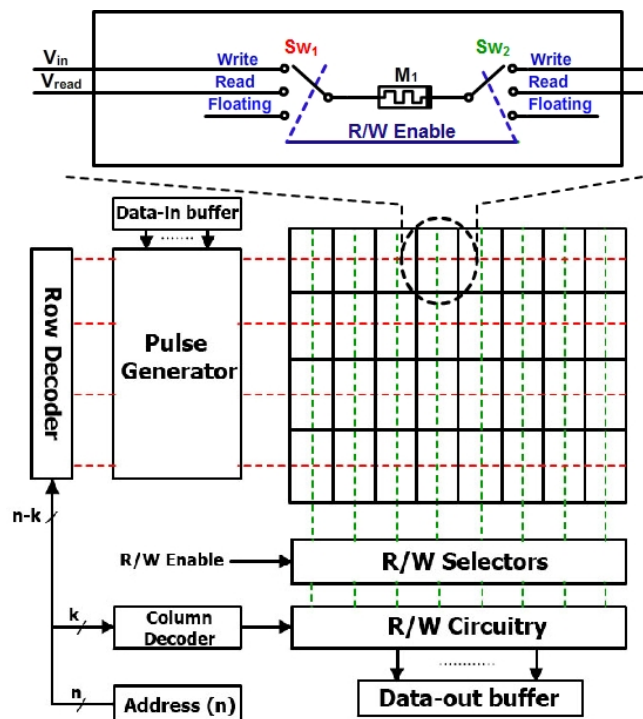
Figure 5.1: Memory crossbar array where the unused memristor terminals are floating.

While grounding the arrays floating terminals does not solve the sneak paths problem, it does marginally improve the noise margin as mentioned in [66]. It is also stated in the same research that, grounding all the floating terminals will cause a huge power consumption while the sneak paths issue are not totally solved.

Unfolded crossbar memory array architecture where each memristor has a separate column (displayed in Figure 5.2-a) solves the problem at the expense of the memory density. It is stated in [66] the density is decreased by a factor equal to the number of rows.

Another method to solve the sneak paths problem mentioned in [66] is to use one diode with each memristor (1D1M) as shown in Figure 5.2-b. This configuration (1D1M) increases the delay of the system because of the added capacitive loads. Also, the output swing will be decreased due to the diode threshold voltage. Using Metal Insulator Metal (MIM) diodes instead of the conventional diodes will provide a better isolation as stated in [115].

(a)   (b)
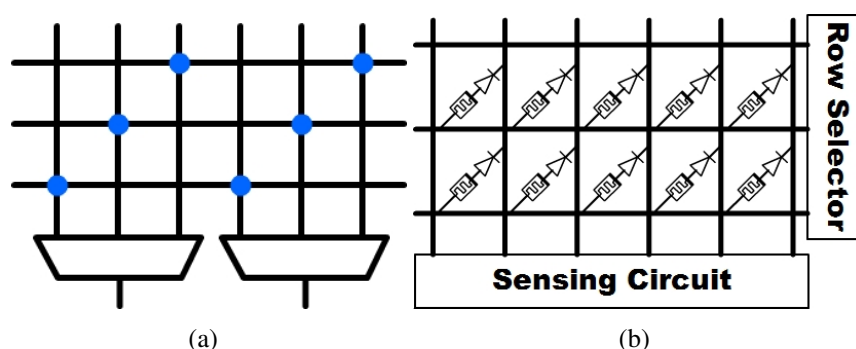
Figure 5.2: Crossbar memory array architecture in (a) unfolded architecture and (b) 1D1M architecture.

Using one transistor one memristor (1T1M) crossbar memory array architecture is also discussed in [66]. It solves the sneak paths issue but it also wrecks the crossbar memory density because of the transistor micro-scale. To reduce this problem, memristors can be vertically stacked on the transistors and a mixed crossbar of nano-wires and micro-wires are used.

All the previously discussed solutions will eliminate or at least reduce the sneak paths problem at the expense of another factor (i.e., power consumption, data density, or delay time). The sneak paths problem is highly considerable because of the fact that, the crossbar architecture consists of two terminal memristor as the memory element. Using a three terminal memristor instead of the two terminal will dramatically reduce the sneak paths problem if it does not eliminate it.

Three terminal memristor is introduced in [116]. It comprises source electrode, drain electrode, gate electrode, and active region. The active region contains an undoped region (i.e., TiO_2) used for transporting and hosting dopants to control the flow of electrons from the source to the drain (or vice versa), and a doped region (i.e., TiO_{2-x}) acting as a source of dopants for the undoped region. The source and the drain are physically connected to the undoped region and the gate is connected to the doped region. Applying a sufficient voltage with the right polarity to the gate will either inject or eject dopants into or out of the undoped region from the doped region. In other words, an applied bias on the gate is needed to change the switch status from ON to OFF state or conversely. Thus, applying voltage on the gate will electrically connect or disconnect the source and the drain to each other in a non-volatile manner. So, it has the same working principle of the two terminal memristor except that, applying a sufficient voltage with the right polarity on the gate is

needed to either inject or eject dopant into or out of the undoped region. Thus, applying voltage on the gate will electrically connect or disconnect the source and the drain to each other in a non-volatile manner. Thus, it acts as the known transistors with the advantage of memristors (i.e., nano-scale device and nonvolatile property). In addition, it has an all-planar geometry as shown in Figure 5.3-a or a stacked geometry as shown in Figure 5.3-b, depending on their application and the practicalities of the layout of the circuit in which it will be used in.

(a)   (b)
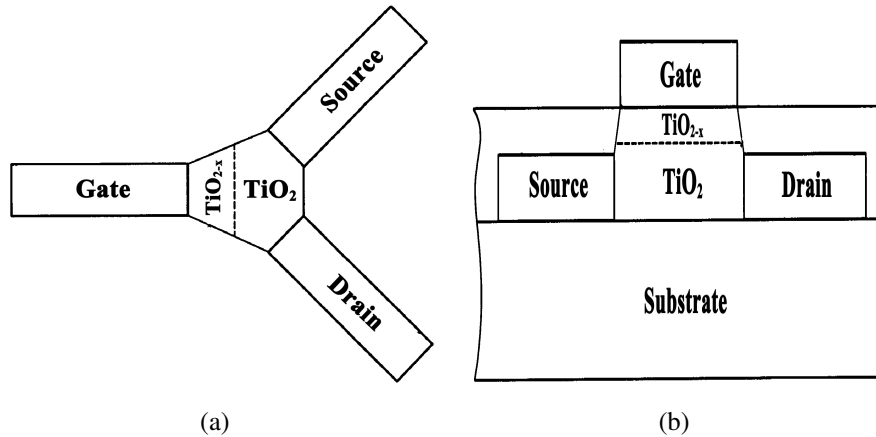
Figure 5.3: Three terminal memristor geometry (a) planar geometry (b) stacked geometry [117].

5.2 New Proposed Circuits

5.2.1 First Proposed Circuit

A new Read/Write for memristor-based memory cell is proposed in Figure 5.4. The proposed design deals with the memristor as a single bit memory element, so only two logic levels (i.e., logic '1' and logic '0') are being stored. As normalized width (w_n), which equal to w/D, varies from zero to one, then theoretically, setting {w_n = 0 to 0.5} is adopted to define the high resistive state while setting {w_n = 0.5 to 1.0} is adopted to define the low resistive state. Due to circuit parameters non-ideality and leakage current, the output pattern should be defined such that some safety margin is allowed. Accordingly, the high resistive state (memristor device is OFF) is defined by setting {w_n = 0 to 0.4} and the low resistive state (memristor device is ON) is defined by setting {w_n = 0.6 to 1.0}. The region {w_n = 0.4 to 0.6} is left as a safety margin where the memristor device in this region is considered undefined [12]. Correspondingly, the best w_n values for the high resistive state and the low resistive state are one and zero, respectively, whereas the worst case values are 0.6 and 0.4, respectively.

5.2.1.1 Writing Operation

The Write circuit is implemented by connecting the writing voltage source across the memristor terminals. This is done by connecting SW_1 to the input voltage (V_{in}) and SW_2
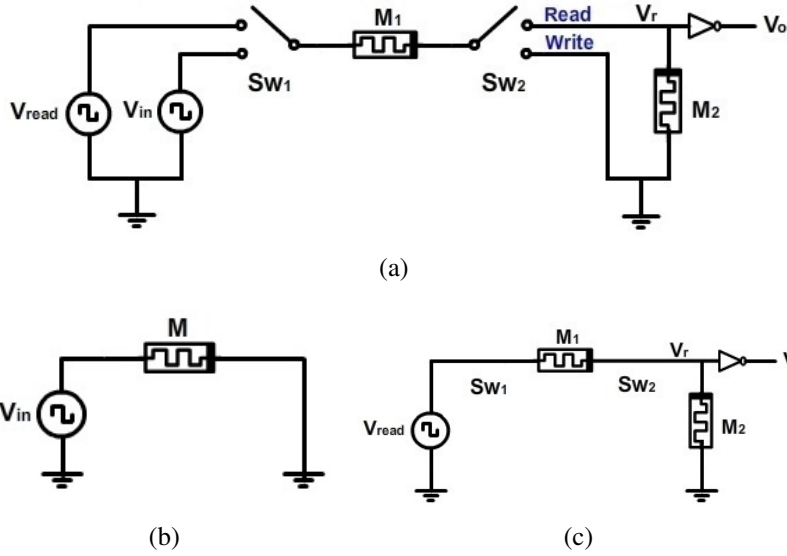
Figure 5.4: Proposed Read/Write circuit for a Memristor-based memory where, (a) the proposed circuit (b) writing data circuitry (c) reading data circuitry.

to the ground as shown in Figure 5.4-b. In [9, 10], it has been shown that, the memristor state depends on the applied voltage magnitude, polarity, and pulse duration as given by (3.2). Thus, there is a need to clearly define these parameters (i.e., voltage magnitude, polarity, and pulse duration) to be able to fully switch the internal device state from one state to the other during the writing process. The nonlinear I-V characteristics of the memristor device make the required pulse duration and voltage magnitude, that change the device from the low resistive state to the high resistive state, different from the required values for the reverse process [9, 10]. These writing voltage parameters can be adaptively selected according to the state needed to be written on the memristor (i.e., write logic one or logic zero). Alternatively, the voltage magnitudes and pulse durations required for writing logic '0' and for writing logic '1' are calculated, where the highest values are selected to perform both writing operations, which are denoted by V_{wr} for the voltage magnitude and T_{wr} for the pulse duration as portrayed in Figure 5.5.

It should be noticed that, the previous writing voltage parameters values are chosen with respect to the best case defined by the output pattern (i.e., w_n is either zero or one). However, other values can be used under the condition of forcing w_n to be in one of the defined regions (low resistive state region or high resistive state region). In addition, there is a trade-off between the applied voltage magnitude and the pulse duration (i.e., if the applied voltage magnitude is decreased then the required pulse duration increases and vice versa). Hence, the value of V_{wr} and T_{wr} should be selected to have the lowest possible voltage magnitude with the highest response scheme. Taking the power consumption in consideration, it is preferable to adopt the lowest V_{wr} which keeps w_n in one of the defined regions.

Besides, writing logic '1' need more voltage than writing logic '0'. This is because of the memristor nonlinear I-V characteristics as mentioned before in memristor-based memory design insights section.
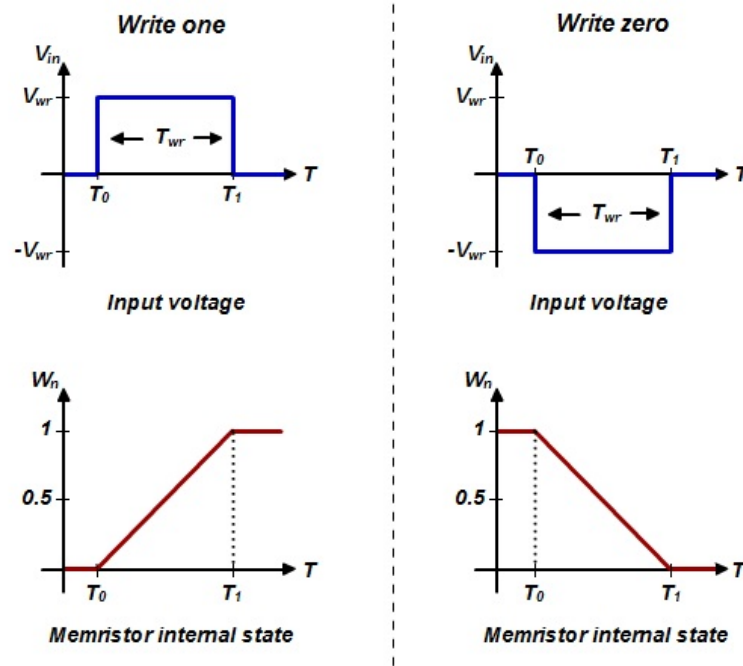
Figure 5.5: Applying positive voltage to write logic '1' (left) and applying a negative voltage to write logic '0' (right).

5.2.1.2 Reading Operation

From the brief literature review previously introduced in Chapter 4, it is obvious that the key challenge in any memristor-based non-volatile memory application is the Read circuit. This is because the applied Read voltage may disturb the stored data due to the accumulative property of memristors. In the proposed Read/Write circuit, the reading process starts by connecting SW_1 and SW_2 to the input read voltage V_{read} and V_r, respectively as portrayed in Figure 5.4.c. For reading the stored data, a positive voltage, denoted by V_{read} is applied and two different scenarios are considered (i.e., whether the stored data is logic '1' or logic '0') as shown in Figure 5.6.

The applied voltage is simply divided between M_2 (which is used as a load resistor and placed to be in the OFF state all the time) and the memory element M_1. Using a memristor as a load resistance aims to make use of the advantage of the device small size and compatibility with the overall circuit design. Based on the stored data, V_r may be bigger or less than $V_{read}/2$ and hence the output of the inverter varies between high output voltage (V_H) and low output voltage (V_L). The output is considered logic zero if $V_O = V_L = 0V$, and considered logic one if $V_O = V_H = 1V$.

5.2.1.3 Simulation Results

The proposed Read/Write circuit behavior is verified by using Cadence Spectre simulation tools. The CMOS peripherals are implemented by TSMC 130nm CMOS technology which adopts industrial hardware-calibrated transistor model card that has been declared by the TSMC foundry to be Silicon verified. The memristor model is an important part of these simulations, where TEAM model is used based on the previous discussed reasons.
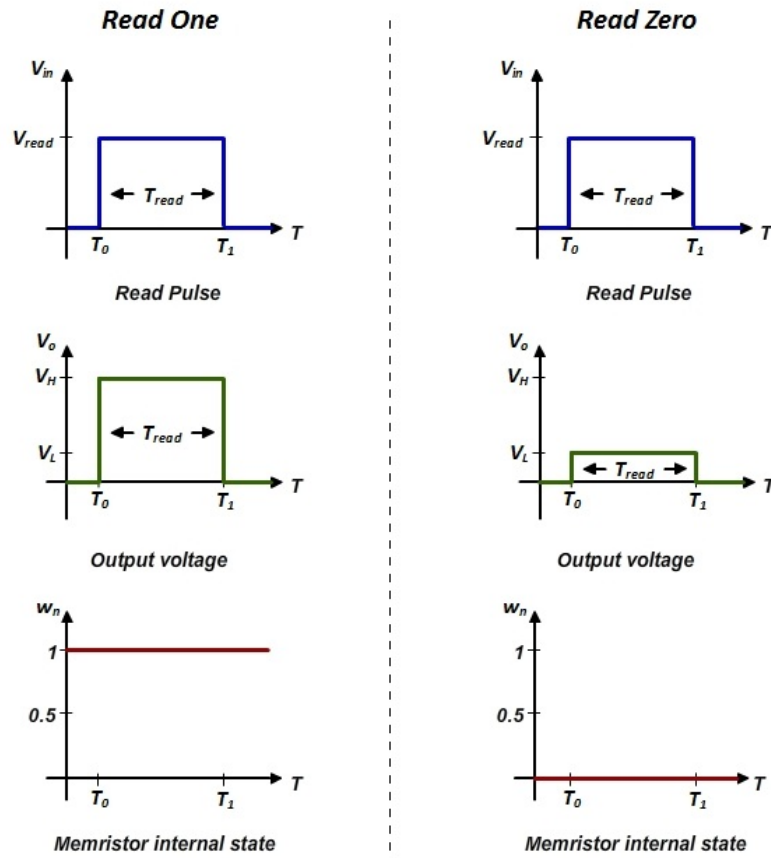
Figure 5.6: The effect of the applied voltage on the output voltage and the memory cell state. Left side displays reading logic '1' operation whereas the right side shows reading logic '0' operation.

Table 5.1: Memristor TEAM model main parameters values [98]

Parameter	Value
D	$3nm$
μ_v	$10e^{-14}m^2V^{-1}sec^{-1}$
R_{on}	100Ω
R_{off}	$2M\Omega$
i_{on}	$-1nA$
i_{off}	$+1nA$

1. Writing Operation Simulation Results

   In this part, the memristor state changes from one state to another (i.e., from the low resistive state to the high resistive state or vice versa) are simulated. In these simulations, the worst case change in the memristor state (i.e., changing w_n from 0 to 1.0 or from 1.0 to 0) is adopted. The main memristor parameters are tabulated in Table 5.1 [97]. According to the used model and window function, the device needs 2.35V to be applied for 3ns to fully change the internal state of the device. Figures 5.7-a and 5.7-b show the possible initial state and the device response to the applied voltage.

   The applied voltage is shown in Figure 5.7 as V_{in}, the output voltage is shown as V_o, and the internal states of memristors M1 and M2 are portrayed as w_n of M1 and w_n of M2, respectively. It is clear from Figure 5.7 that, during the writing operation there is no voltage presented at V_o, which gives an immunity against accidental reading during the writing process. Also the internal state of the load memristor M2 did not change and only the state of the memory cell (i.e., memristor M1) was changed as desired.

2. Reading Operation Simulation Results

   For testing the device internal state, a small sensing voltage (1V) for a small period of time (3ns) is applied. This applied voltage disturbs one of the device states. This is because if a positive voltage is used then logic zero is disturbed while logic one is not affected and vice verse for using negative voltage.

   It is stated in [12] that using a double pulse with equal duration and magnitude but with opposite polarity will eliminate the effect off applying the sensing current. In fact this read pattern may eliminate the sensing current effect. This is because the asymmetry criteria of the device.Figure 5.8-a and Figure 5.8-b display the testing results.

   As shown in Figure 5.8-a and Figure 5.8-b, the reading process is a challenge in memristor-based memory circuit design. In Figure 5.8-a the internal state of the device changed for reading logic zero as w/D varies from 0 to 0.4. However, the output of the circuit is still acceptable as the output pattern is big enough (i.e., w/D = 0-0.4). On the other hand, the device state for logic one still the same as the reading process uses the same voltage polarity for the writing one.

   Based on the previous discussion, a refreshment circuit may be needed to maintain logic zero state. Another solution is to rewrite logic zero after the reading process. The writing circuit can be triggered after reading logic zero to rewrite the device internal state. Despite its advantage of maintaining the device internal state after reading logic zero, it increases the delay time of the circuit.

3. Memory array

   Portrayed in Figure 5.1 the introduced memristor memory array with peripheral circuits which are similar to SRAM peripherals [117, 118]. The way to access the memristor memory cell is normally similar to the well known SRAM. The data is written to the cells or read from it by the proposed write or read scheme.
   The array is normally folded into fewer rows of more columns. Because of the very skinny shape of the arrays, it is hard to fit the chip into floor plan. Figure
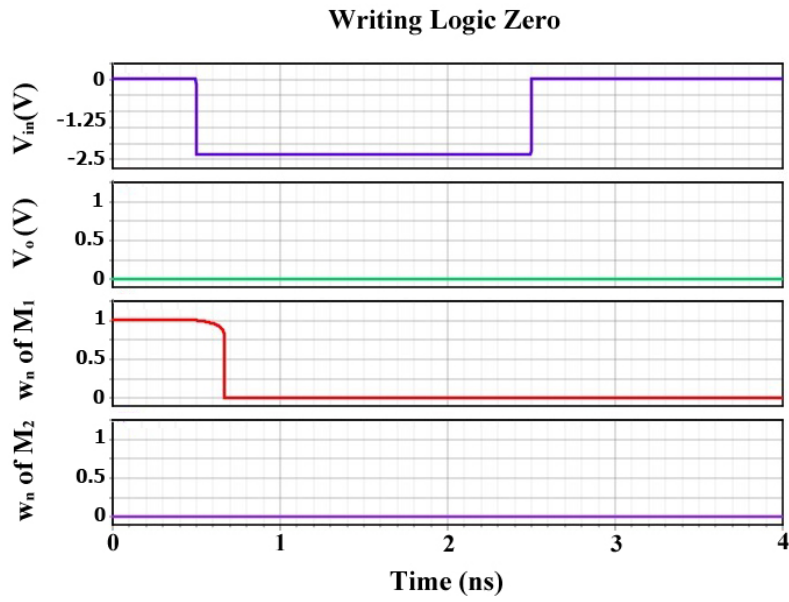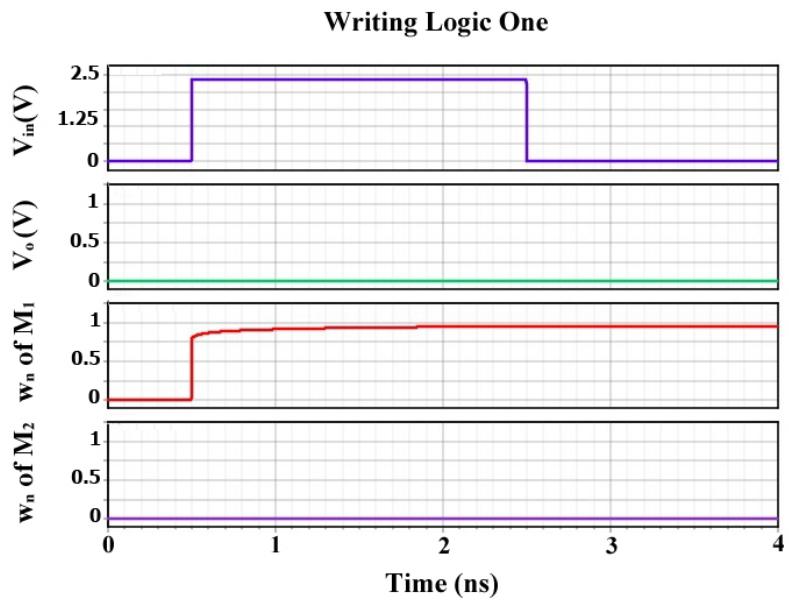
Figure 5.7: Writing operation for worst case change in the initial state of the memory device for writing (a) logic '1' and (b) logic '0'. Also shown the effect of the applied bias voltage (V_{in}) on the output voltage and the internal state of memristors M1 and M2.

5.1 represents a folding design, where the pulse generator produces read or write pattern signals. When a read operation is performed, read enable signal triggers the pulse generator to produce the read pattern. On the other hand, during the write operation, the pulse generator produces write-one pulse or write-zero pulse based on the incoming data, which stored in the input buffer (Data-in buffer). Also, the selector units turn the memristor cells to the ground for a write operation or to the read circuitry for a read operation. R/W Enable signal manages the R/W selector to
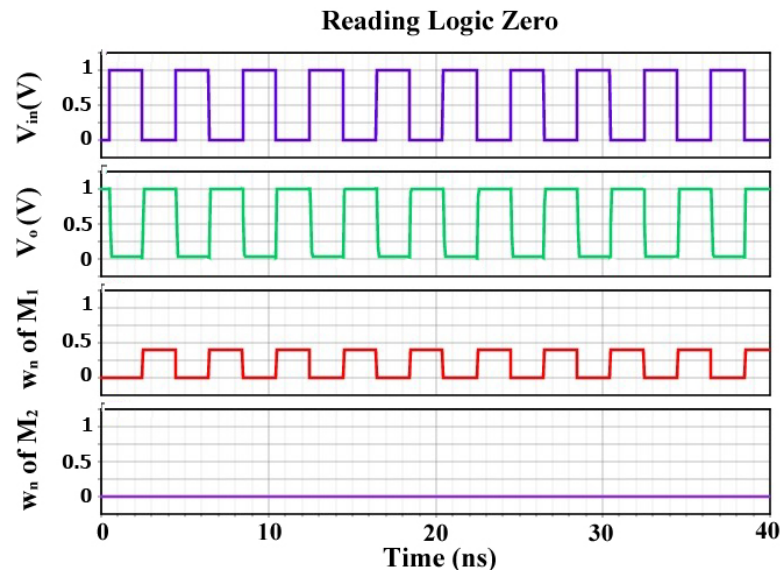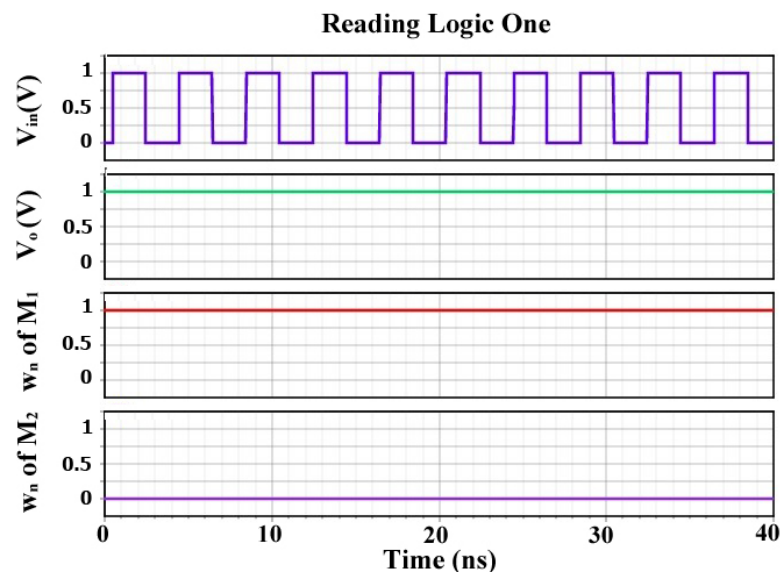
Figure 5.8: Testing the device internal state in case of (a) logic zero, or (b) logic one is stored.

switch between the Read and Write circuitry based on the needed operation (read or write operation).

For the writing operation, the pulse generator generates write pulses to the memory array based on the stored data value in the data-in buffer. At the same time, the selectors switch the appropriate column lines to the ground. The unselected lines will be floating, and thus there are no changes in the unselected cells.
For the reading operations, the pulse generator produces the read signals. Simultaneously, the selectors turn every selected column to the Read circuitry, while the resulting voltage drop across the load memristor is captured by the data-out buffer.

Table 5.2: Comparison between the reviewed solutions for the sneak paths problem in the first proposed circuit.

Comparison aspect	Floating Array	Half-Grounded Array	Grounded Array	1D1M Array	1T1M Array
Consumed Power while Reading Logic Zero (μw)	35	64	81.2	95.95	54.95
Consumed Power while Reading Logic One (nw)	96	373	375	646.1	515
Sneak Paths effect on the un-selected devices internal state (%)	10-30	8-29	5-25	0	0-15
Applied voltage for reading process	V_{read}	V_{read}	V_{read}	$V_{read} + V_d$	$V_{read} + V_T$
Expected Area	Normal	Normal	Normal	Large	Micro-size

4. Testing the sneak paths problem

   The proposed circuit had been used to build 4x4 memory array to test the sneak paths effect on the internal state of the un-selected devices. Sneak paths have a dramatic effect on the devices that store logic zero as the circuit uses a positive voltage for the reading process. The aforementioned solutions are implemented while the consumed power and the sneak paths effect are tested. The consumed power is calculated by

$$P = \frac{1}{T} \int_0^T I \times V \qquad (5.3)$$

   where, P is the consumed power, V is the applied voltage, I is the current passing through the device and T is the pulse duration.

   Table 5.2 summaries the consumed power, expected area, minimum, and maximum sneak paths effect on the un-selected devices internal states. Taken into consideration that, the sneak paths effect varies from marked impact to ignored impact based on the distance between the device under test and other devices. As stated in Table 5.2, 1D1M and 1T1M configuration need an extra voltage than the normal values to be applied for the reading process to compensate the voltage drop on the diode (V_d) and the transistor threshold voltage (V_T), respectively.

5.2.2 Second Proposed Circuit

A novel Read/Write circuit with non-destructive reading scheme is proposed in Figure 5.9. The proposed design deals with the memristor as a single bit memory element, where the two logic levels (i.e., logic '1' and logic '0') are defined just like the previous circuit.
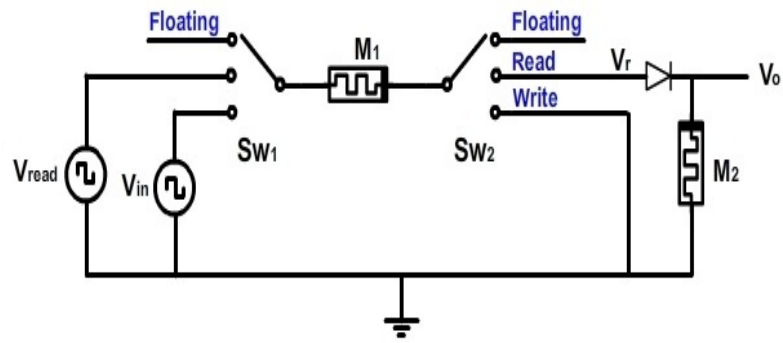
Figure 5.9: Proposed non-destructive Read/Write circuit for a memristor-based memory.

As illustrated in Figure 5.9, the circuit consists of two memristors, two switches, and a diode. Hence, the circuit mainly depends on the memristor to make use of the advantage of its small layout area and low power consumption.

5.2.2.1 Writing Operation

The Write circuit is implemented as shown in Figure 5.4-b, where all the previously defined parameters (i.e., w_n, logic '1' defined region, logic '0' defined region, and undefined region) are the same.

It should be noticed that, the polarity of memristor M1 is chosen to take advantage of the non-linearity criteria of the memristor. As discussed before in memristor-based memory design insights section and presented in [86], the time needed to switch ON the device is larger than the switching OFF time. Accordingly, as memristor M1 is used with the proposed polarity in Figure 5.9, the circuit will have more immunity to the leakage current.

5.2.2.2 Reading Operation

The proposed read circuit is shown in Figure 5.10. For reading the stored data, a positive voltage, denoted by V_{read} (i.e., $V_{in} = V_{read}$ during the reading process) is applied for T_{read} pulse duration and two different scenarios are considered based on the stored data.
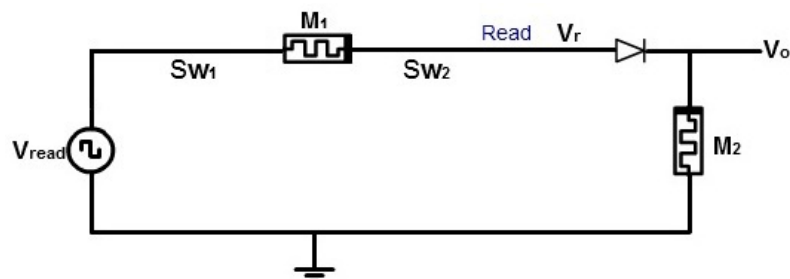
Figure 5.10: The proposed non-destructive Read/Write circuit during the reading operation.

1. **The stored data is logic '1':**
   In this scenario, memristor M1 in the ON state (low resistive state) and the voltage

55

drop on it is small and hence V_r almost equal to V_{read} which is designed larger than 0.7V to allow the current to flow through the diode and memristor M2. In As in the previous circuit, memristor M2 is used as a load resistor to get benefit of the memristor properties (i.e., small size, low power consumption, less heat, high resistivity in the OFF state, and compatibility with the circuit design) over the conventional resistor.

The output voltage drop on M2 (denoted by V_o) indicates which data is stored on the memory cell (i.e., if $V_o = V_L$, logic '0' is stored and if $V_o = V_H$, logic '1' is stored). As noticed in Figure 5.10, memristor M2 is positioned to be always in the high resistive state. The output voltage, $V_o = V_H$, is given by:

$$
\begin{aligned}
V_o(= V_H) &= \underbrace{V_r - n \times V_T \times \ln(\frac{I_d}{I_{sat}})}_{V_d} \\
&= I_d \times R_{off}|_{M2}
\end{aligned}
\qquad (5.4)
$$

where, V_o is the output voltage, V_d is the diode voltage drop, I_d is the diode ON current, I_{sat} is the diode saturation current, n is the diode ideality factor, and V_T is the thermal voltage ($= K_B T/q \approx 26$ mV at room temperature). The value of V_H should be designed as large as possible compared to V_L.

The value of $V_o = V_H$ should be designed as high as possible to distinguish reading logic '1' state from reading logic '0' state (i.e., V_H should be designed as large as possible compared to V_L). The utilization of memristor M2 in the high resistive state value provide a large load resistance which achieve this distinguishing objective even for small I_d values. The calculation of $V_o = V_H$ is obtained by solving the nonlinear equations given in (5.4) iteratively.

2. **The stored data is logic '0':**
   In this scenario, memristor M1 in the OFF state (high resistive state) and the voltage drop on it is extremely large and hence V_r is very small. V_{read} is designed so that after the voltage drop on M1, V_r is less than 0.7V and hence the diode switches OFF and acts as an open circuit where no current flows through M2. Thus, the output voltage will be low ($V_o = V_L$).

The non-destructive feature of the proposed circuit does exist because the reading voltage will affect memristor M1 only during reading logic one, there will be no effect during reading logic zero because the diode will act as an open circuit and hence no current will flow through the memory element (M1). As the circuit use a positive voltage to write logic one then the reading voltage polarity and the writing voltage polarity is the same. The only main concern is to choose V_{read} so that it turns ON the diode while reading logic one and OFF while reading logic zero. Also, The diode is used to make sure that the current flows through the load memristor M2 in one direction to maintain its OFF state and also to provide immunity to the memory Read/Write circuit against the leakage currents.

5.2.2.3 Simulation Results

The circuit is simulated with the same parameters (i.e., D, μ_v, R_{on}, R_{off}, i_{on}, and i_{off}) and models (i.e., TEAM model for memristor) used for simulating the previous circuit.

1. Writing Operation Simulation Results
   In this part, simulation is performed with the same conditions as the previous circuit. As both circuits use the same writing technique, the simulation results are the same as shown in Figures 5.11 and 5.7.

(a)

(b)
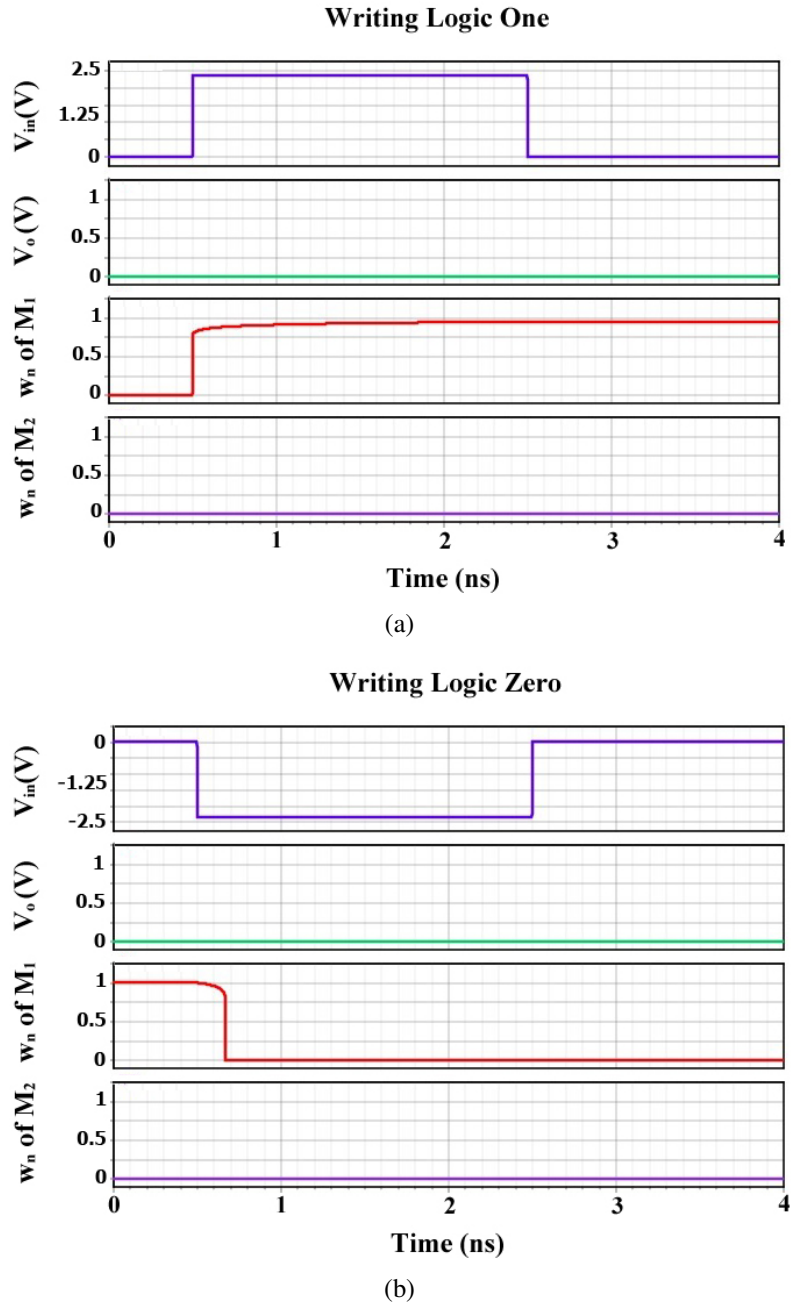
Figure 5.11: Writing operation simulation results for writing (a) logic '1' and (b) logic '0'.

Also, the circuit has immunity against the accidental reading during the writing process as there is no voltage presented at the output during the writing operation.

Besides, the internal state of the load memristor M2 during the writing process is the same, while the state of the memory cell (i.e., Memristor M1) was changed.
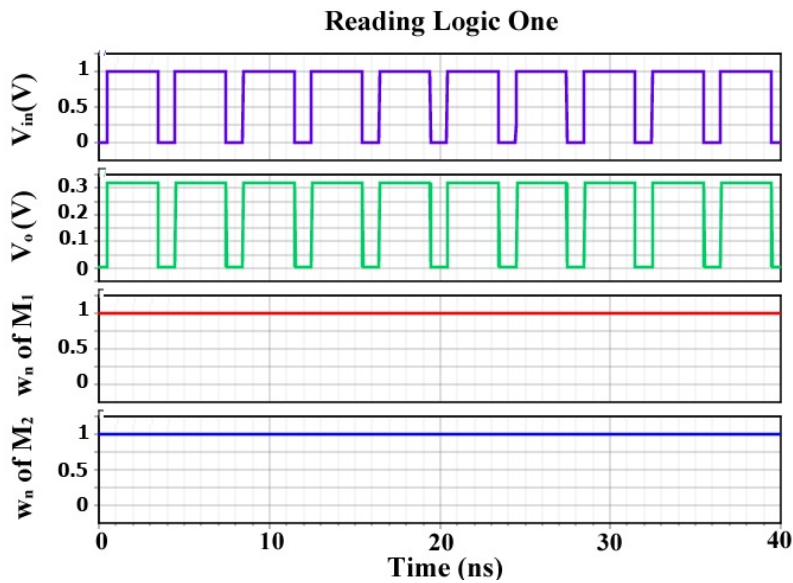
(a)
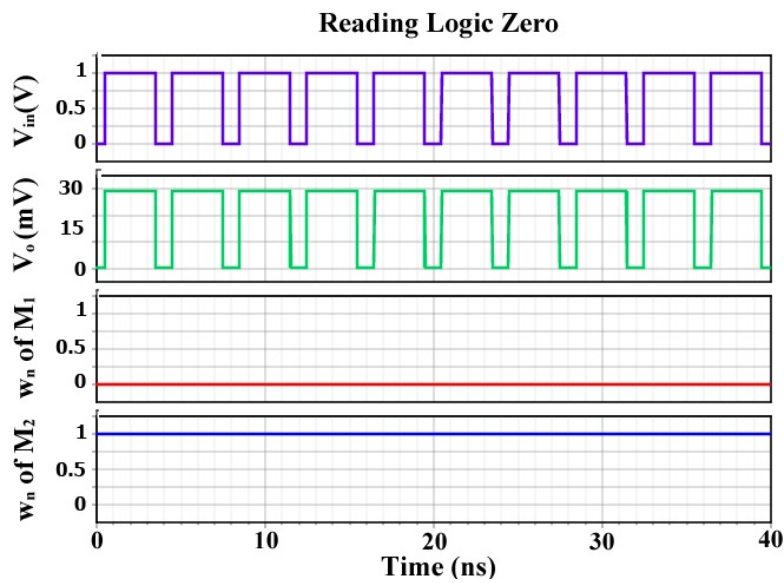
(b)

Figure 5.12: Reading the internal state of the memory cell for the case of (a) logic '1' and (b) logic '0'.

2. Reading Operation Simulation Results

The reading mechanism is conducted by applying a 1V voltage pulse for 3ns to investigate the stored data on the memory cell. The results proved that the reading operation did not disturb the internal state of the memristor device. Figures 5.12-a and 5.12-b show the output voltage for reading logic '1' and logic '0', respectively.

As illustrated in Figure 5.12, the reading mechanism neither changed the internal state of memristors M1 nor M2, and V_o varied as memristor M1 internal state varied

Table 5.3: Comparison between the reviewed solutions for the sneak paths problem in the second proposed circuit.

Comparison aspect	Floating Array	Half-Grounded Array	Grounded Array	1D1M Array	1T1M Array
Consumed Power while Reading Logic Zero (μw)	8.29	19.46	76	80	49.15
Consumed Power while Reading Logic One (nw)	33.15	96.38	135.75	278.69	87.5
Sneak Paths effect on the un-selected devices internal state (%)	8-25	7-23	2.5-20	0	0-13
Applied voltage for reading process	V_{read}	V_{read}	V_{read}	$V_{read} + V_d$	$V_{read} + V_T$
Expected Area	Normal	Normal	Normal	Large	Micro-size

from low resistive state (i.e., $V_o = V_H = 0.3$V), which representing logic '1' to high resistive state (i.e., $V_o = V_L = 0.03$V), which representing logic '0'. Also it is shown that, the successive reading operations did not disturb the internal state of the memory cell, which is the main contribution of the proposed Read/Write circuit as most circuits introduced in the literature such as [12, 47, 110] need refreshment technique to restore the original data after successive reading operations. The proposed Read/Write circuit provides non-destructive reading operations without the need for refreshing circuits because both the reading and writing voltages have the same polarity.

3. Memory array
The proposed circuit can be used in deploying memory arrays such as the previous proposed circuit. So that, the circuit use the same SRAM peripherals (i.e., data-in buffer, data-out buffer, R/W selectors, row decoder, column decoder, pulse generator, and write circuitry) as discussed before except that the read circuitry is replaced with the new proposed one.

4. Testing the sneak paths problem
Conducting the same simulation set used for testing the sneak paths effect on the previous proposed circuit, Table 5.5 summarize the sneak paths effect simulation results on the new proposed circuit.

5.2.3 Third Proposed Circuit

A modified version of the second proposed circuit is shown in Figure 5.13, where a third switch (SW_3) to control the polarity of the applied read voltage based on the stored data is added.
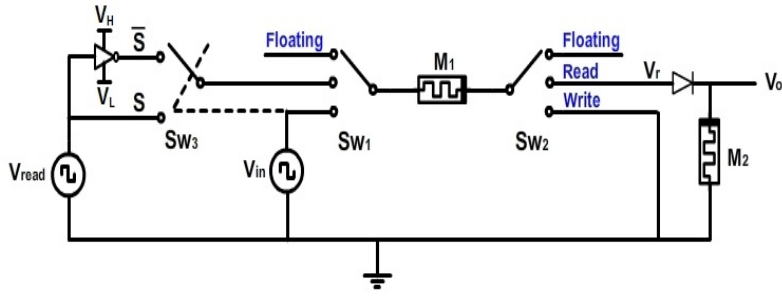
Figure 5.13: A modified version of the proposed non-destructive Read/Write circuit.

5.2.3.1 Writing Operation

The writing circuit is the same one shown in Figure 5.4-b. However, during the writing process the position of SW_3 is selected. SW_3 position is controlled by the input writing signal. For instance, when logic '1' is written, switch SW_3 is positioned to connect the input read voltage (i.e., terminal S as shown in Figure 5.13), when applied, to the memristor terminal. On the other hand, when logic '0' is written, switch SW_3 is positioned to connect to the inverted input read voltage (i.e., terminal $\overline{S}$ as shown in Figure 5.13) to the memristor terminal.

5.2.3.2 Reading Operation

In the proposed circuit, the reading process starts by connecting switch SW_3 either to terminal S or terminal $\overline{S}$ (this action should be performed during the writing operation by connecting SW_3 to S if logic '1' is written or connecting SW_3 to $\overline{S}$ if logic '0' is written) and SW_2 is connected to V_r as portrayed in Figure 5.14. For reading the stored data, a positive voltage, denoted by V_{read} is applied and two different scenarios are considered (i.e., whether the stored data is logic '1' or logic '0').
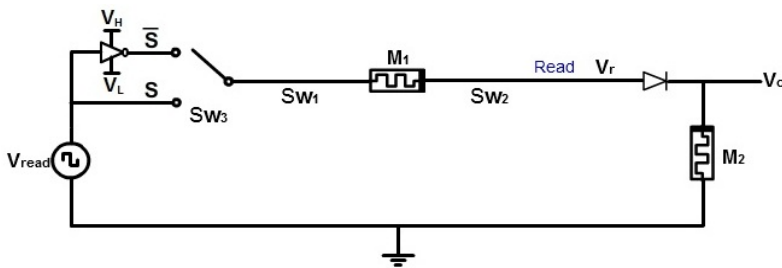
Figure 5.14: The proposed Read/Write circuit during the reading operation, when SW_3 is connected to terminal S or terminal $\overline{S}$ and SW_2 is connected to V_r. Applying the positive voltage V_{read} results in a similar positive voltage at terminal S and a negative voltage at terminal $\overline{S}$. Depending on SW_3 position, V_r will be positive or negative, which makes the diode ON or OFF and V_o to vary from V_L to V_H.

1. **The stored data is logic '1':**
   For reading logic one, M1 in the ON state (low resistive state) and SW_3 is connected

60

to S terminal during the writing process. Therefore, the circuit acts as the previous one before the modification.

2. **The stored data is logic '0':**
   In this scenario, M1 in the OFF state (high rseistive state) and SW_3 is connected to $\overline{S}$ terminal and accordingly the input Read voltage, V_{read}, polarity is inverted. The polarity of the read voltage is inverted due to the used inverter (shown in Figure 5.14), which is programmed to have V_L equal to -1V. Memristor M1 is in the OFF state (i.e., high resistive state). This high resistive value of M1 makes high voltage drop across the memristor M1 besides, applying negative voltage on the diode P-terminal leads the diode to be in the OFF state and the output voltage, $V_o = V_L \approx$ 0V. The applied Read voltage is a pulse with a voltage magnitude equal to V_{read} and a pulse duration equals T_{read}. Then, T_{read} should be larger than the time needed to have a valid output level as shown in Figure 5.6.

This technique, in which switch SW_3 is set to S or $\overline{S}$ during the writing operation, is called "Read monitor write circuit", which adopts non-destructive reading method. The non-destructive feature of the proposed circuit does exist because the reading voltage polarity and the writing voltage polarity are the same due to the utilization of SW_3 which monitors the writing voltage polarity. Moreover, if the internal state of the memory device is disturbed, the Read pattern helps to restore the original state.

This modification is performed to solve the diode issue. The previous circuit non-destructive property exists because the diode acts as an open circuit when the applied voltage is less than V_d. This action exists only in ideal diodes but for the real ones it will pass current even if the applied voltage is less than V_d as shown in Figure 5.12-b. As shown in Figure 5.12-b the memory cell internal state was not disturbed for 10 successive reading cycles, however it may be disturbed after more reading cycles. Therefore, using SW_3 helps the reading process to use the same voltage polarity that is used during the writing process as well as making the proposed circuit completely non-destructive.

5.2.3.3 Implementation of SW$_3$

It is obvious that the key idea of the circuit design is the implementation of switch SW_3. It may be implemented using a CMOS latch. Using a latch will be on the expense of the non-volatile advantage of the memristor. Another solution, which is adopted in the proposed circuit, is using a three terminal memristor. By connecting the input write voltage to the gate terminal of the three terminal memristor, it will work as described in the previous section and should be able to connect or disconnect the desired terminals in a non-volatile manner.

5.2.3.4 Simulation Results

1. Writing Operation Simulation Results
   Because of the writing circuitry is the same, as only the Read circuitry is modified, the simulation results is the same presented in Figure 5.11.

2. Reading Operation Simulation Results
   The reading mechanism is conducted by applying a pulse of 1.0V for 2ns to investigate the stored data on the memory cell. Ten Read cycles are applied in Figure

5.15 to show that successive reading operations do not disturb the internal state of the memory cell. The results proved that the reading operation does not disturb the internal state of the memristor. Figures 5.15-a and 5.15-b show the output voltage for reading logic '1' and logic '0', respectively.
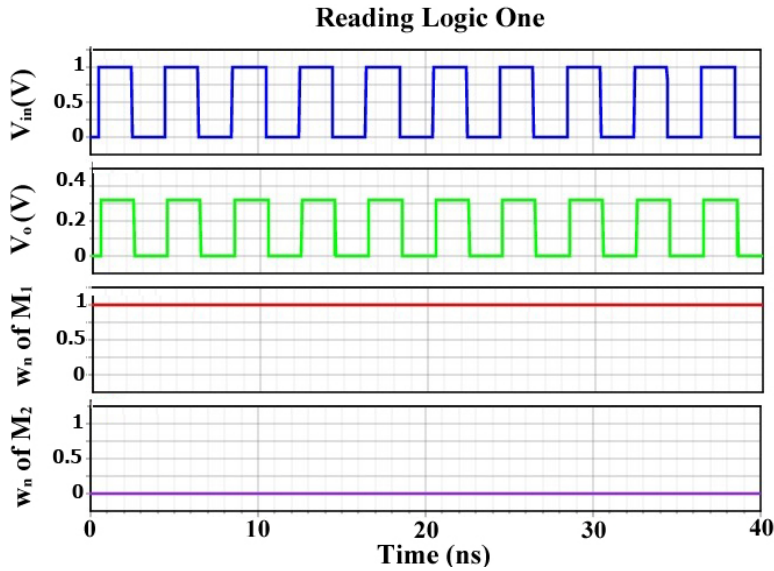
(a)
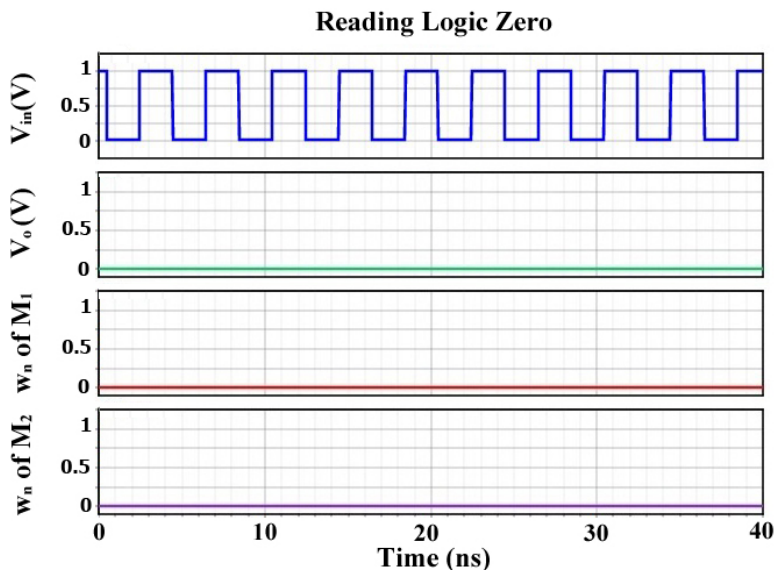
(b)

Figure 5.15: Reading the internal state of the memory cell for the case of (a) logic '1' and (b) logic '0'. Also shown the effect of the applied Read voltage (V_{read}) on the output levels and the internal state of memristors M1 and M2.

As shown in Figure 5.15, the reading mechanism neither changes the internal state of memristor M1 nor M2, and V_o varies from the high resistive state (i.e., $V_o = V_H$ = 0.3V) to the low resistive state (i.e., $V_o = V_L = 0V$).The proposed Read/Write circuit provides non-destructive reading operations without the need for refreshing circuits because both the reading and writing voltages have the same polarity.

Table 5.4: Comparison between the reviewed solutions for the sneak paths problem in the third proposed circuit.

Comparison aspect	Floating Array	Half-Grounded Array	Grounded Array	1D1M Array	1T1M Array
Consumed Power while Reading Logic Zero (μw)	9.95	23.35	91.4	96	59
Consumed Power while Reading Logic One (nw)	24	96.6	98	200.3	63.32
Sneak Paths effect on the un-selected devices internal state (%)	5-20	5-18	3-15	0	0-10
Applied voltage for reading process	V_{read}	V_{read}	V_{read}	$V_{read} + V_d$	$V_{read} + V_T$
Expected Area	Normal	Normal	Normal	Large	Micro-size

3. Memory array
   As the proposed circuit is a modification from the second proposed circuit, it can be used in deploying memory arrays such as the previous circuit. The circuit can use the same array peripherals (i.e., data-in buffer, data-out buffer, R/W selectors, row decoder, column decoder, pulse generator, and R/W circuitry) as discussed before except that adding SW_3 to each memory cell in the array.

4. Testing the sneak paths problem
   Conducting the same simulation set used for testing the sneak paths effect on the previous proposed circuit, Table 5.4 summarizes the sneak paths effect simulation results on the modified proposed circuit.

   As noticed in Table 5.4, adding SW_3 has a major effect in reducing the sneak paths effect and also reducing the power needed to read logic one. On the other hand, adding SW_3, increase the layout area and the consumed power while reading logic zero.

5.3 Comparison of the proposed circuits with Previously Published Read/Write Circuits

In this section, a comparison between the new proposed circuits and the Read/Write circuit introduced in [12] is conducted. The circuit in [12] is chosen to be compared with the new proposed circuits due to the availability of the circuit architecture and simulation design setup in [12] whereas most of the other published Read/Write circuits are at the block diagram level with no clear circuit architecture or simulation setup.

The comparison is divided into two main parts. First, the Read/Write circuit introduced in [12] is simulated using the Verilog-A TEAM model presented in [97] following the

same design setup used to simulate the proposed circuits for a fair comparison. Then, the two circuits performance metrics are compared such as power consumption, layout area, and access time delays.

The circuit in [12] has the following Write/Read mechanisms:

1. **Writing mechanism**

   In the writing process, the writing voltage source is connected directly across the memristor terminals, which is done by setting the Read/Write switch in Figure 4.6 to the write position. The time needed to alter the device state from the low resistive state to the high resistive state is denoted by $T_{w1}^{O_H}$, so if a suitable positive pulse is applied for this duration or longer, the device is turned to the high resistive state as shown in Figure 5.16.

   On the other hand, to switch the device from the high resistive state to the low resistive state, a time equal to $T_{w0}^{O_L}$ is needed as shown in Figure 5.16. Similarly, applying a certain negative pulse for this duration or longer switches the device from the high resistive state to the low resistive state. It is claimed in [12] that a 1V pulse with 4ns duration is capable of completely changing the device state to its quixotic values (i.e., w equals to D for the low resistive state or w equals to zero for high resistive state).
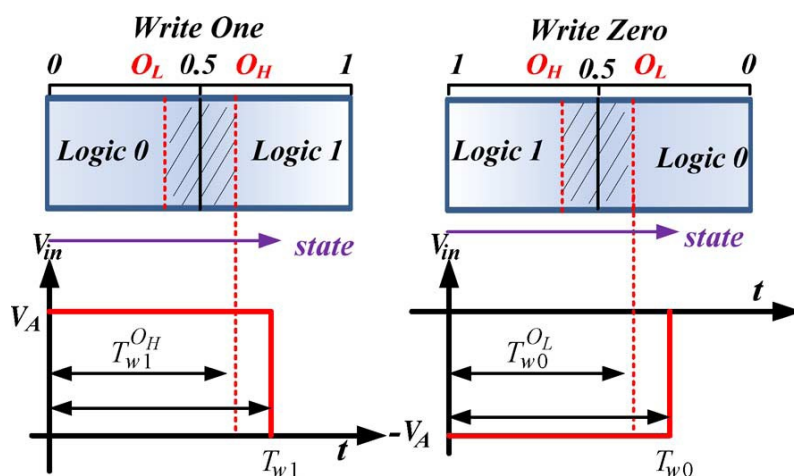
Figure 5.16: Write signals (bottom) and corresponding memristor states (top) [13].

2. **Reading mechanism**

   Reading the stored data on the memristor is not as easy as writing it, because the reading voltage disturbs the stored data. To start reading, R/W enable switch connects the memristor with V_x as shown in Figure 4.6, then a double pulse equal in duration and magnitude but with opposite polarity is applied. The applied double pulse starts with the negative pulse followed by the positive pulse. Accordingly, the net injected charges are equal to zero at the end of each Read cycle and the initial state remains as is. This reading mechanism is illustrated in Figure 5.17.

   The process is performed in two stages, (1) the convert stage and (2) the sense amplifier stage. During the convert stage, the reading voltage is divided between
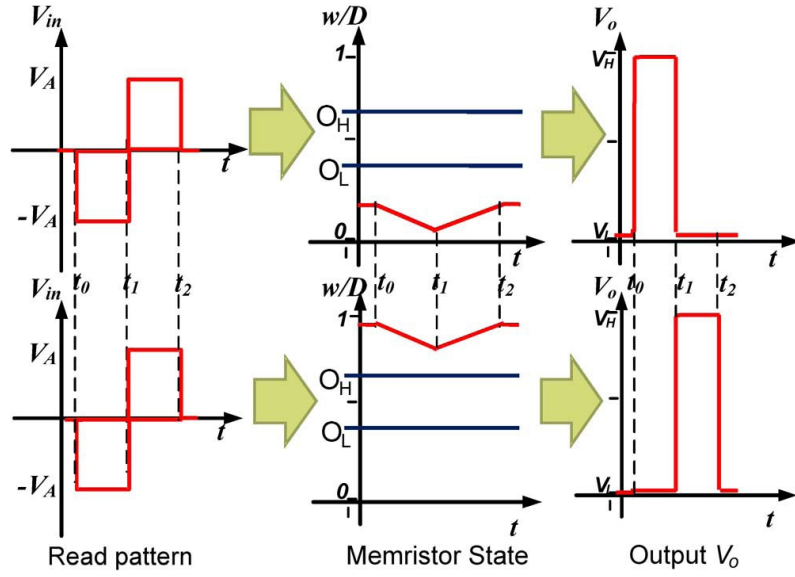
Figure 5.17: Graphical illustration for the reading scheme in [13]. (top) Read pattern, memristor state, and output voltage when the memristor is storing logic '0'. (bottom) Read pattern, memristor state, and output voltage when the memristor is storing logic '1' [13].

the memristor and the load resistor. The drop voltage across the load resistor is compared to V_{ref} to identify the memristor state. The memristor state is identified as V_H if the memristor stores logic '1' and V_L if the memristor stores logic '0'. The load resistance value is chosen to distinguish between high and low resistive states. Based on the simulation setup in [12], $V_{ref} = V_{in}/2$ is used as the threshold voltage between the two states at which $w_n = 0.5$. To achieve the desired value of V_{ref}, the load resistance, R_x, is designed as follows:

$$R_x = \frac{R_{on} + R_{off}}{2} \tag{5.5}$$

Therefore, if w_n is less than 0.5, V_x is less than V_{ref} causing the sense amplifier to generate V_L. On the other hand, if w_n is larger than 0.5, the sense amplifier output equals to V_H. The sense amplifier is designed to produce the low level output voltage, $V_L = 0V$, and the high level output voltage $V_H = 1.0V$.

Figures 5.18-a and 5.18-b show the effect of one read cycle on the internal state of the memristor device for the circuit presented in [12]. These figures illustrate why this circuit needs refreshment circuit as well as other Read/Write circuits in the literature need. For example, for reading logic '0' operation, the internal state w_n of the memristor changes during the first reading half-cycle from 0 to 0.25. Then during the second reading half-cycle, w_n does not recover its original value at zero but becomes close to 0.15. Accordingly, successive reading cycles will result in disturbance of the stored data in the memristor device and a refreshment circuit is a must.

Table 5.5 illustrates the comparison between the proposed circuits and the circuit introduced in [12]. The consumed power is calculated by (5.3), where the delay is
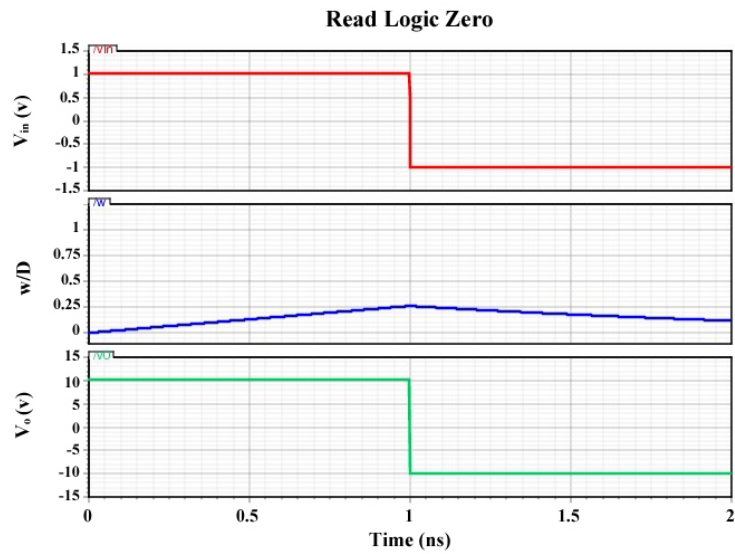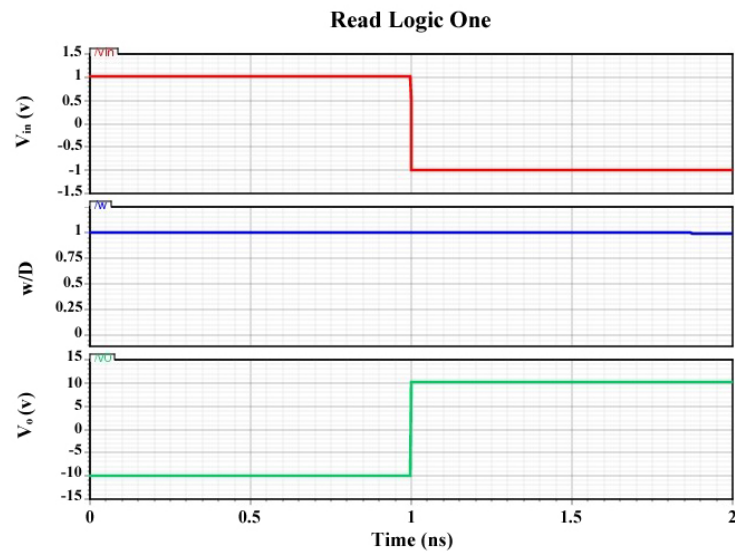
Figure 5.18: Reading cycle for the circuit in [13] when reading (a) logic '0' and (b) logic '1'.

calculated using the delay calculation mechanism integrated in the simulation tool. The proposed circuit consumes less power than the circuit in [12]. The high power consumption in the circuit introduced in [12] is due to the op-amp used in the sense amplifier design as well as the resistors. However, the proposed circuits are capable of reducing this power consumption by factors of 20.5% and 84% for writing '1' and writing '0' cases, respectively. On the other hand, the second proposed circuit is capable of reducing the power consumption for reading logic '1' and '0' by 28.3% and 81.6%, respectively, while the third proposed circuit can reduce the consumed power for reading logic '1' and '0' by 48.2% and 77.9%, respectively.

As seen in Table 5.5, writing logic '0' consumed more power than writing logic
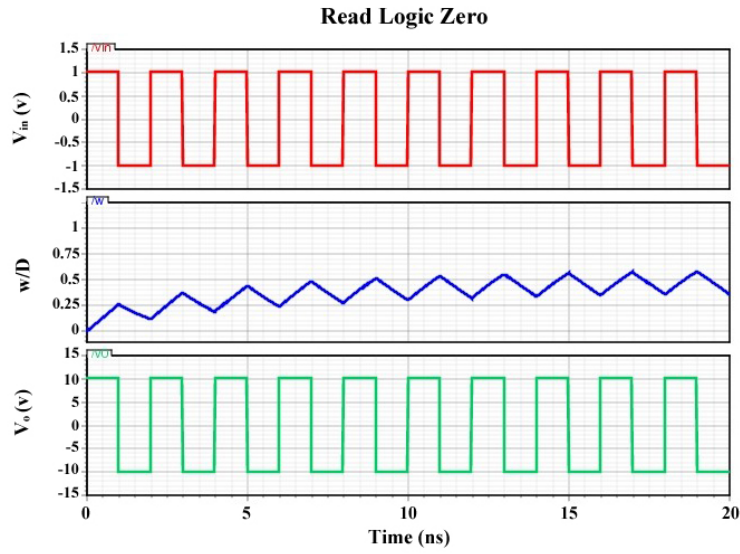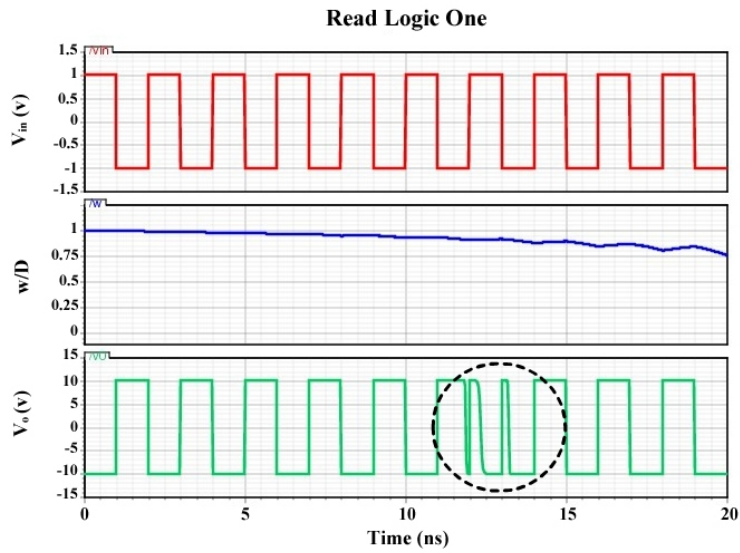
Figure 5.19: 10 successive reading cycles are adopted for the circuit in [13] when reading (a) logic '0' and (b) logic '1'. It is clear that the circuit in [13] internal state is disturbed and the stored logic value is destroyed.

'1'. This is because most of the applied voltage is lost in the nanowire electrodes. The electrodes' nano size resulted in a series resistance in the range of $K\Omega$, while the device ON resistance is in the range of Ohm. Therefore, the series resistance is greater than the device ON resistance and hence, the device (i.e., switching material TiO_{2-x}) consumed more current to reset [113].

It is also noticed in Table 5.5 that, the writing time delay is the same for the proposed circuits and the circuit in [12] because they are using the same writing technique. However, the reading delay time for the proposed circuits is much less than that of the circuit in [12] by, at least, factors of 99.6% and 98.7% for reading '1' and reading '0' cases, respectively.
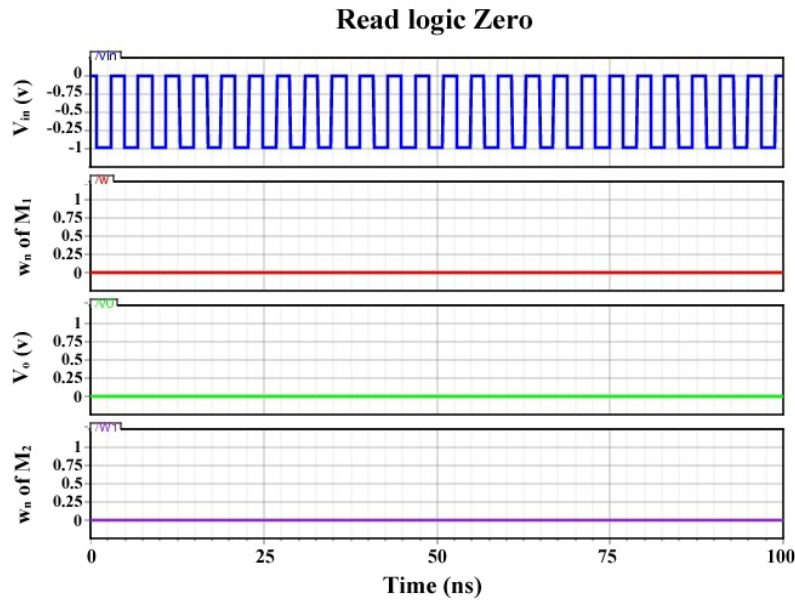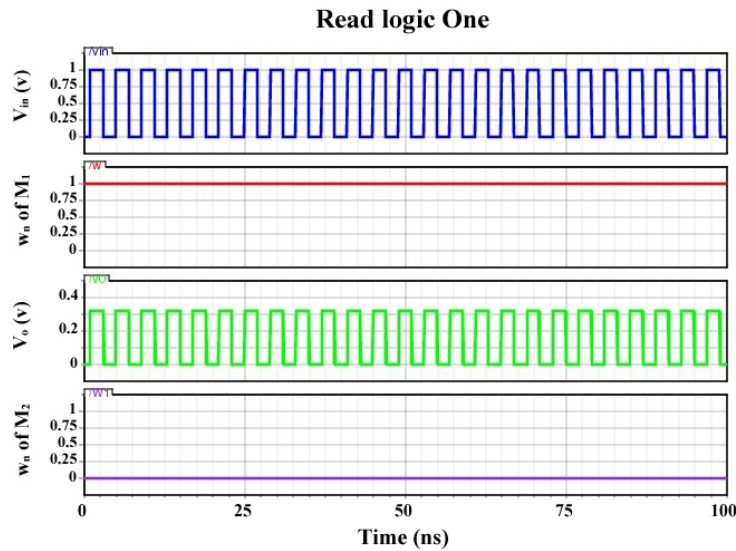
Figure 5.20: 50 successive reading cycles are adopted for the proposed circuit when reading (a) logic '0' and (b) logic '1'. It is clear that the proposed circuit maintains the internal state of the memory cell and the stored logic value is kept as is.

The reduction in the delay time is mainly because the proposed circuits convert the internal state of the memristor device directly to the output voltage without the need for the sense amplifier circuit, which decreases the large reading time needed by the proposed circuit in [12]. Moreover, the output voltage during the read operation from the circuit in [12] is only available during the second reading half-cycle as shown in Figure 5.18. This introduces more latency delay during the read operation and also increases the reading operation power consumption.

68
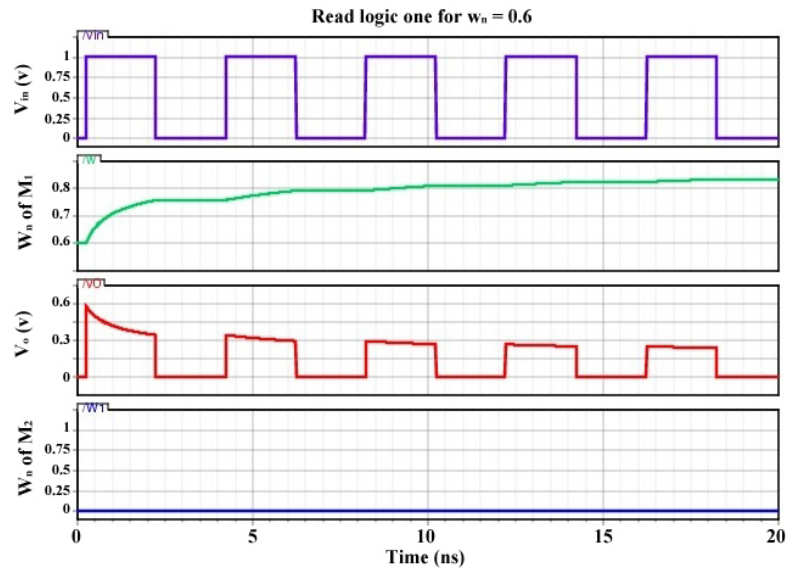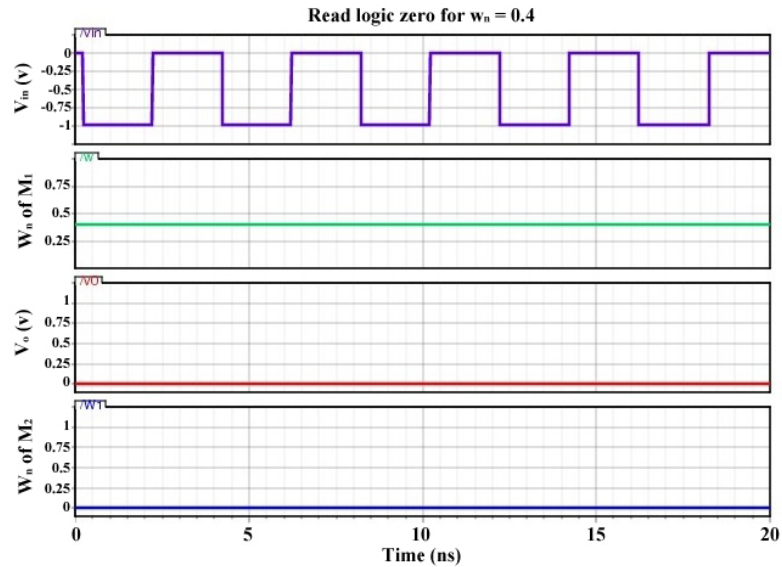
Figure 5.21: Reading stored data at worst case a) reading logic '0' for $w_n = 0.4$ and b) reading logic '1' for $w_n = 0.6$.

The main strength of the second and the third proposed circuits is the non-destructive successive reading feature and that no refreshment circuits are needed as required for the first proposed circuit and the circuit in [12]. This had been verified by applying 50 successive reading cycles to the Read/Write circuit in [12] and the proposed circuits. Figures 5.19-a and 5.19-b display the reading operation for 10 successive reading cycles for the circuit in [12] showing the internal state disturbance when reading logic '0' and when reading logic '1', respectively. Also, Figure 5.19-b highlights the output flipping when reading logic '1' after only 7 successive reading cycles. Also, Figures 5.20-a and 5.20-b display the reading operation for 50 successive reading cycles for the third proposed circuit when reading logic '0' and when reading logic '1', respectively. It is clear that

Table 5.5: Comparison between the proposed circuit in this article and the circuit introduced in [13].

Comparison aspect	1st proposed circuit	2nd proposed circuit	3rd proposed circuit	Circuit in [13]
Power for Writing '1' (μW)	31.28	31.28	31.28	39.37
Power for Writing '0' (mW)	8.6	8.6	8.6	54
Power for reading '1' (W)	0.488 μ	1.37 p	0.99 p	1.91 p
Power for reading '0' (μW)	3.58	0.25	0.3	1.36
Delay time for writing '1' (psec)	424.9	424.9	424.9	424.9
Delay time for writing '0' (psec)	186.7	186.7	186.7	186.7
Delay time for reading '1' (psec)	10.9	0.55	15	4000
Delay time for reading '0' (psec)	70.8	9.78	54.8	4000
Refreshment needed	Yes	No	No	Yes

the internal state of the circuit in [12] is disturbed and the stored logic value is destroyed. However, the second and the third proposed circuits maintain the stored value state and no disturbance occurs. Moreover, the same reading mechanism had been repeated for 500 reading cycles and the stored data did not change. Accordingly, the refreshment circuit is a must for the circuit in [12] whereas the second and the third proposed circuits do not require any refreshment circuits due to this non-destructive feature.

For the third proposed circuit, applying the reading scheme is not only non-destructive but it also might help to restore the stored data if the memristor is storing logic one as shown in Figure 5.21-a. On the other hand, when the memristor is storing logic zero, the reading scheme maintains the stored data as shown in 5.21-b. The scheme could not restore the data in the case of logic zero because of the diode which suppresses the negative voltage and hence no current flows.

The first proposed approach consists of one inverter, two memristors, and two switches, while the second proposed approach comprising one diode, two memristors, and two switches. For the third proposed approach, it is made of one inverter, one diode, two memristors, and three switches. The approach in [12] consists of one memristor, three

resistors, one comparator, and one switch. The layout area of the proposed designs are estimated to be 16.19 μm^2 (i.e., 4.3μm^2 (inverter) + 0.09 μm^2 (two memristors) + 11.8 μm^2 (two switches)) for the first proposed circuit, 63.49 μm^2 (i.e., 51.6μm^2 (diode) + 0.09 μm^2 (two memristors) + 11.8 μm^2 (two switches)) for the second proposed circuit, and 73.79 μm^2 (i.e., 4.3μm^2 (inverter) + 51.6μm^2 (diode) + 0.09 μm^2 (two memristors) + 17.8 μm^2 (three switches)). However, the estimated layout area of the design proposed in [12] equals 1841.645 μm^2 (i.e., 0.045 μm^2 (one memristor) + 135.7 μm^2 (three resistors) + 1700 μm^2 (comparator) + 5.9 μm^2 (one switch)). This illustrates how the proposed approach reduces the area overhead of the R/W circuit by at least factor of 24X. The main advantage of the proposed designs is the exclusion of the comparator which occupies large layout area.

Chapter 6: Discussion and Conclusions

6.1   Contributions

In this thesis, an overview of the physics behind different memristors types is discussed in light of the current state of the art and provides a comparative review between two of the most promising memristor physical realizations (i.e., TiO_2 thin film memristor and spintronic memristor). The currently published memristor-based applications was reviewed showing the importance of using memristors in memory applications. This importance comes from the facts that, it is a straight forward application based on the memristor characteristics and leakage in the current memory technology to cover the huge storage capabilities required by the nano-computing facilities. The current submitted Read/Write circuits for memristor-based memory applications suffer from read-disturbance. This is because of the accumulative property of the device. Therefore, the reading voltage may disturb the stored data. This problem is analyzed and memristor-based memory design insights is introduced. Based on these insights, three novel designs of Read/Write circuits for memristor-based memory cell are proposed. Two of the proposed circuits have the advantages of non-destructive successive reading cycles, less power consumption, less delay time, and smaller layout area, as compared to recently published Read/Write circuit in [12]. All these advantages are verified by comprehensive simulations by using Cadence Spectre while adopting TSMC 130nm industrial hardware-calibrated CMOS transistor model card. The TEAM model had been used for the memristor device due to its accuracy and simplicity. The proposed circuits were tested for 500 successive read cycles where the stored data did not change. Besides, the proposed circuits reduce the power consumption by factors of 20.5%, 84%, 77.9%, and 48.2% for writing '1', writing '0', reading '1', and reading '0' cases, respectively when compared with the circuit proposed in [12]. These is because the proposed circuits neither use comparator nor resistor. Moreover, the reading delay time for the proposed circuit is much less than that of the circuit in [12] by factors of 99.6% and 98.7% for reading '1' and reading '0' cases, respectively. It has been also demonstrated that the circuit in [12] does not maintain its stored data after 7 successive reading cycles (i.e., the stored data is flipped from logic '1' to logic '0') whereas the proposed circuits are capable of maintaining the stored data for large number of successive reading cycles (limited by the leakage current).

6.2   Published/Submitted papers

1. M. Elshamy, H. Mostafa, and M. Sameh Said, "Comparative review of the TiO2 and the spintronic memristor devices," *Canadian Conference on Electrical and Computer Engineering (CCECE'2014)*, Toronto, Canada, IEEE, pp. 317-322, 2014.

2. M. Elshamy, H. Mostafa, and M. Sameh Said, "A novel non-destructive readout circuit for memristor-based memory arrays," *IEEE Canadian Conference on Electrical and Computer Engineering (CCECE'2014)*, Toronto, Canada, IEEE, pp. 312-316, 2014.

3. M. Elshamy, H. Mostafa, and M. Sameh Said, "Design considerations/insights for memristor-based memory arrays," *IEEE International Conference on Engineering and Technology (ICET'14)*, In Press (accepted in 21 Jan. 2014).

4. M. Elshamy, H. Mostafa, and M. Sameh Said, "New non-destructive read/write circuit for memristor-based memories," *IEEE International Conference on Engineering and Technology (ICET'14)*, In Press (accepted in 21 Jan. 2014).

5. M. Elshamy, H. Mostafa, and M. Sameh Said, "Novel non-destructive read/write circuit for memristor-based memory arrays," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, In Press (accepted in 11 Nov. 2014).

6.3   Future Work

This thesis provides a foundation for much future work in the areas of spintronic memristor modeling and design of memristor-based memory cells. For spintronic modeling, the device analysis and equations in this thesis are inconclusive, and so more analysis must be done to propose such a model. Another important modeling goal is to encapsulate the effects of design variations for both spintronic and thin film TiO_2 memristor; these effects play dominant role because of the nonlinear I-V curve for memristors, in particular the asymmetric ON/OFF switching time in the thin film TiO_2 memristor and so these effects need to be modeled.

With regards to the device analysis, as explained in Chapter 3, the device can be used in multi-bit memory design. Alternative read and write techniques that would not disturb the stored data can be explored.

Also, using memristor to build other architectures like FinFET need to be explored. Finally, fabrication of different test chips comprising the different proposed circuits and testing the read disturb immunity theorized in this work would be necessary.

References

[1] L. O. Chua, "Memristor-the missing circuit element," *IEEE Transaction Circuits Theory*, vol. 18, pp. 507–519, Septemper 1971.

[2] X. Wang and Y. Chen, "Patent relevant to spintronic memristor," *Recent Patent on Electrical Engineering*, vol. 3, pp. 10–18, January 2010.

[3] L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proc. IEEE*, vol. 64, pp. 209–223, Febrauary 1976.

[4] L. O. Chua, "Device modeling via basic nonlinear circuit elements," *IEEE Transaction Circuits Systems*, vol. CAS-27, pp. 1014–1044, November 1980.

[5] L. O. Chua, "Nonlinear circuits," *IEEE Transaction Circuits Systems*, vol. CAS-31, pp. 69–87, January 1984.

[6] L. O. Chua, "Nonlinear circuit foundations for nanodevices, part I: The four-element torus," *Proc. IEEE*, vol. 91, pp. 1830–1859, November 2003.

[7] M. Itoh and L. O. Chua, "Memristor oscillators," *J. Bifurcation Chaos*, vol. 18, pp. 3183–3206, November 2008.

[8] M. D. Ventra, Y. V. Pershin, and L. O. Chua, "Circuit elements with memory: Memristors, memcapacitors and meminductors," *Proc. IEEE*, vol. 97, pp. 1717–1724, October 2009.

[9] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, May 2008.

[10] R. S. Williams, "How we found the missing memristor," *Spectrum IEEE*, vol. 45, pp. 28–35, December 2008.

[11] J. J. Yang, M. D. Picket, X. M. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nature Nanotechnology*, vol. 3, pp. 429–433, July 2008.

[12] Y. Ho, G. M. Huang, and P. Li, "Dynamical properties and design analysis for nonvolatile memristor memories," *IEEE Transactions on Circuits and Systems I*, vol. 58, pp. 724–736, April 2011.

[13] Erokhin, Victor, Fontana, and P. Marco, "Electrochemically controlled polymeric device: a memristor (and more) found two years ago," July 2008.

[14] M. Crupi, L. Pradhan, and S. Tozer, "Modelling neural plasticity with memristors," *IEEE Canadian Review*, pp. 10–14, 2012.

[15] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, M. Bibes, A. Barthlmy, and J. Grollier, "A ferroelectric memristor," *Nature Materials*, vol. 11, pp. 860–864, Septemper 2012.

[16] X. Wang, Y. Chen, H. Xi, H. Li, and D. Dimitrov, "Spintronic memristor through spin-torque-induced magnetization motion," *IEEE Electron Device Letter*, vol. 30, pp. 294–297, March 2009.

[17] Y. Chen and X.Wang, "Compact modeling and corner analysis of spintronic memristor," *Proc. Int. Symp. IEEE/ACM NANOARCH*, pp. 7–12, March 2009.

[18] J. Borghetti, Z. Li, J. Straznicky, X. Li, D. A. A. Ohlberg, W.Wu, D. R. Stewart, and R. S.Williams, "A hybrid nanomemristor/transistor logic circuit capable of self-programming," *Proc. Nat. Acad. Sci. USA*, vol. 106, pp. 1699–1703, February 2009.

[19] G. Snider, P. Kuekes, and R. S. Williams, "CMOS-like logic in defective, nanoscale crossbars," *Nature Nanotechnology*, vol. 15, pp. 881–891, June 2004.

[20] O. Kavehei, Y. Kim, A. Iqbal, K. Eshraghiam, S. F. Al-Sarawi, and D. Abbott, "The fourth element: Characteristics, modelling, and electromagnetic theory of the memristor," *Proceeding of the Royal Society A-Mathematical Physical and Engineering Sciences*, vol. 466, pp. 2175–2202, August 2010.

[21] *International Technology Roadmap for Semiconductor*, 2010.

[22] P. J. Kuekes, D. R. Stewart, and R. S. Williams, "The crossbar latch: Logic value storage, restoration, and inversion in crossbar circuits," *Journal of Applied Physics*, vol. 97, pp. 034301–034301–5, February 2005.

[23] T. Raja and S. Mourad, "Digital logic implementation in memristor-based crossbar," *International Conference on Communications, Circuits and Systems (ICCCAS)*, pp. 23–25, July 2009.

[24] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'memristive' switches enable 'stateful' logic operations via material implication," *Nature*, vol. 464, pp. 873–876, April 2010.

[25] E. Lehtonen and M. Laiho, "Stateful implication logic with memristors," *International Symposium on Nanoscale Architecture*, pp. 33–36, July 2009.

[26] Y. Pershin and M. D. Ventra, "Practical approach to programmable analog circuit with memristors," *IEEE Transaction on Circuits Systems I*, vol. 57, pp. 1857–1864, August 2009.

[27] M. Laiho and E. Lehtonen, "Arithmetic operations within memristor based analog memory," *International Workshop on Cellular Nanoscale Networks and Their Applications (CNNA)*, pp. 1–6, February 2010.

[28] Y. V. Pershin and M. D. Ventra, "Experimental demonstration of associative memory with memristive neural networks," *Neural Network*, vol. 23, pp. 881–886, May 2010.

[29] M. Itoh and L. O. Chua, "Memristor cellular automata and memristor discrete-time cellular neural networks," *International Journal on Bifurcation Chaos*, vol. 19, pp. 3605–3656, May 2009.

[30] G. S. Snider, "Spike-timing-dependent learning in memristive nanodevices," *International Symposium on Nanoscale Architecture*, pp. 85–92, June 2008.

[31] B. Linares-Barranco and T. Serrano-Gotarredona, "Memristance can explain spike-time-dependent-plasticity in neural synapses," *Nature Proceedings*, March 2009.

[32] J. Rajendran, H. Manem, and G. S. Rose, "NDR based threshold logic fabric with memristive synapses," *IEEE Conference on Nanotechnology (IEEE-NANO)*, pp. 727–728, July 2009.

[33] M. J. Sharifi and Y. M. Banadaki, "General spice models for memristor and application to circuit simulation of memristor-based synapses and memory cells," *Journal of Circuits, Systems and Computers*, vol. 19, pp. 407–424, April 2010.

[34] A. Afifi, A. Ayatollahi, and F. Raissi, "Implementation of biologically plausible spiking neural network models on the memristor crossbar-based CMOS/nano circuits," *Proceedings of the European Conference on Circuit Theory and Design*, pp. 563– 566, August 2009.

[35] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Letter*, vol. 10, p. 12971301, March 2010.

[36] X. Wang, Y. Chen, Y. Gu, and H. Li, "Spintronic memristor temperature sensor," *IEEE Electron Device Letters*, vol. 31, pp. 20–22, January 2010.

[37] W. Wang, G. Wang, and D. Tan, "A new memristor based chaotic circuit," *International Workshop on Chaos-Fractals Theories and Applications (IWCFTA)*, pp. 57–60, October 2011.

[38] P. Zhou, B. Zhao, Y. Zhang, J. Yang, and Y. Chen, "MRAC: A memristor-based reconfigurable framework for adaptive cache replacement," *International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp. 207–208, October 2011.

[39] E. R. Kandel, J. H. Schwartz, and T. M. Jessell, "Principles of neural science," 2000.

[40] S. K. Lai, "Flash memories: Successes and challenges," *IBM Journal of Research and Development*, vol. 52, pp. 529–535, July 2008.

[41] A. M. Bratkovsky, "Spintronic effects in metallic, semiconductor, metaloxide and metalsemiconductor heterostructures," *Reports on Progress in Physics*, vol. 71, p. 026502, January 2008.

[42] D. Halupka, S. Huda, W. Song, A. Sheikholeslami, K. Tsunoda, C. Yoshida, and M. Aoki, "Negative-resistance read and write schemes for STT-MRAM in $0.13\mu m$ CMOS," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 256–257, February 2010.

[43] K. Tsuchida, T. Inaba, K. Fujita, Y. Ueda, T. Shimizu, Y. Asao, T. Kajiyama, M. Iwayama, K. Sugiura, S. Ikegawa, T. Kishi, T. Kai, M. Amano, N. Shimomura, H. Yoda, and Y. Watanabe, "A 64 Mb MRAM with clamped-reference and adequate-reference schemes," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 258–259, February 2010.

[44] E. Chen, D. Apalkov, Z. Diao, A. Driskill-Smith, D. Druist, D. Lottis, V. Nikitin, X. Tang, S. Watts, S. Wang, S. A. Wolf, A. W. Ghosh, J. W. Lu, S. J. Poon, M. Stan, W. H. Butler, S. Gupta, C. K. A. Mewes, T. Mewes, and P. B. Visscher, "Advances and future prospects of spin-transfer torque random access memory," *IEEE Transactions on Magnetics*, vol. 46, pp. 1873–1878, June 2010.

[45] A. Dayal, P. Li, and G. Huang, "Robust sram design via joint sizing and voltage optimization under dynamic stability constraints," *Journal of Low Power Electronics*, vol. 6, pp. 66–79, April 2010.

[46] P. Vontobel, W. Robinett, P. J. Kuekes, D. R. Stewart, J. Straznicky, and R. S.Williams, "Writing to and reading from a nano-scale crossbar memory based on memristors," *Nanotechnology*, vol. 20, pp. 1–21, October 2009.

[47] I. E. Ebong and P. Mazumder, "Self-controlled writing and erasing in a memristor crossbar memory," *IEEE Transactions on Nanotechnology*, vol. 10, pp. 1454–1463, November 2011.

[48] *International Technology Roadmap for Semiconductors*, 2007.

[49] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, pp. 114–117, April 1965.

[50] *http://en.wikipedia.org/wiki/Moore's_law#cite_note-Moore1965paper-1*.

[51] *International Technology Roadmap for Semiconductors*, 2012.

[52] S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y. C. Chen, R. M. Shelby, M. Salinga, D. Krebs, S. H. Chen, H. L. Lung, and C. H. Lam, "Phase-change random access memory: A scalable technology," *IBM Journal of Research and Development*, vol. 52, pp. 465–479, July 2008.

[53] G. W. Burr, B. N. Kurdi, J. C. Scott, C. H. Lam, K. Gopalakrishnan, and R. S. Shenoy, "Overview of candidate device technologies for storage-class memory," *IBM Journal of Research and Development*, vol. 52, pp. 449–464, July 2008.

[54] B. C. Lee, E. Ipek, O. Mutlu, and D. Burger, "Architecting phase change memory as a scalable DRAM alternative," *International Symposium on Computer Architecture (ISCA)*, pp. 2–13, June 2009.

[55] P. Zhou, B. Zhao, J. Yang, and Y. Zhang, "A durable and energy efficient main memory using phase change memory technology," *International Symposium on Computer Architecture (ISCA)*, pp. 14–23, June 2009.

[56] B. C. Lee, P. Zhou, J. Yang, Y. Zhang, B. Zhao, E. Ipek, O. Mutlu, and D. Burger, "Phase-change technology and the future of main memory," *IEEE Micro*, vol. 30, pp. 131–141, February 2010.

[57] X. Dong, X. Wu, G. Sun, Y. Xie, H. Li, and Y. Chen, "Circuit and microarchitecture evaluation of 3D stacking magnetic RAM (MRAM) as a universal memory replacement," *Proceedings of the 45th annual Design Automation Conference*, pp. 8–13, June 2008.

[58] M. H. Kryder and C. S. Kim, "After hard drives - what comes next?," *IEEE Transactions on Magnetics*, vol. 45, pp. 3406–3413, October 2009.

[59] *http://en.wikipedia.org/wiki/Ferroelectric_RAM*.

[60] Y. Chung, B.-G. Jeon, and K.-D. Suh, "A 3.3-V, 4-Mb nonvolatile ferroelectric RAM with selectively driven double-pulsed plate read/write-back scheme," *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 35, pp. 697–704, May 2000.

[61] T. Sumi, N. Moriwaki, G. Nakane, T. Nakakuma, Y. Judai, Y. Uemoto, Y. Nagano, S. Hayashi, M. Azuma, E. Fujii, S. I. Katsu, T. Otsuki, L. McMillan, C. P. de Araujo, and G. Kano, "A 256 kb nonvolatile ferroelectric memory at 3 V and 100 ns," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 268–269, February 1994.

[62] H. Koike, T. Otsuki, T. Kimura, M. Fukuma, Y. Hayashi, Y. Maejima, K. Amantuma, N. Tanabe, T. Masuki, S. Saito, T. Takeuchi, S. Kobayashi, T. Kunio, T. Hase, Y. Miyasaka, N. Shohata, and M. Takada, "A 60-ns 1-Mb nonvolatile ferroelectric memory with a nondriven cell plate line write/read scheme," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1625–1634, November 1996.

[63] W. Kraus, L. Lehman, D. Wilson, T. Yamazaki, C. Ohno, E. Nagai, H. Tamazak, and H. Suzuki, "A 42.5 mm^2 1 Mb nonvolatile ferroelectric memory utilizing advanced architecture for enhanced reliability," *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 242–245, June 1998.

[64] T. Miyakawa, S. Tanaka, Y. Itoh, Y. Takeuchi, R. Ogiwara, S. M. Doumae, H. Takenakal, I. Kunishima, S. Shuto, O. Hidaka, S. Ohtsuki, and S. I. Tanaka, "A 0.5 μ m 3 V 1T1C 1 Mb FRAM with a variable reference bitline voltage scheme using a fatigue-free reference capacitor," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 104–105, February 1999.

[65] T. Fukushima, A. Kawahara, T. Nanba, M. Matsumoto, T. Nishimoto, N. Ikeda, Y. Judai, T. Sumi, K. Arita, and T. Otsuki, "A microcontroller embedded with 4 Kbit ferroelectric non-volatile memory," *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 46–47, June 1996.

[66] M.A.Zidan, H. A. H. Fahmy, M. M. Hussain, and K. N. Salama, "Memristor-based memory: The sneak paths problem and solutions," *Microelectronics Journal*, pp. 176–183, February 2013.

[67] T. Perez and C. Rose, "Non-volatile memory: Emerging technologies and their impacts on memory systems," *Technical Report*, September 2010.

[68] K. Witrisal, "Memristor-based stored-reference receiver - the UWB solution?," *Electronics Letters*, vol. 45, pp. 713–714, July 2009.

[69] M. Crupi, L. Pradhan, and S. Tozer, "Modelling neural plasticity with memristors," *IEEE Canadian Review*, vol. 68, pp. 10–14, 2012.

[70] T. W. Hickmott, "Low-frequency negative resistance in thin anodic oxide films," *Journal of Applied Physics*, vol. 33, p. 2669, February 1962.

[71] J. G. Simmons and R. R. Verderber, "New conduction and reversible memory phenomena in thin insulating films," *Proceedings of the Royal Society A*, pp. 77–102, October 1967.

[72] F. Argall, "Switching phenomena in titanium oxide thin films," *Solid State Electronics*, vol. 11, pp. 535–541, May 1968.

[73] T. Driscoll, H.-T. Kim, B.-G. Chae, M. D. Ventra, and D. N. Basov, "Phase-transition driven memristive system," *Applied Physics Letters*, vol. 95, pp. 043503–1–3, July 2009.

[74] T. Driscoll, H.-T. Kim, B.-G. Chae, B.-J. Kim, Y.-W. Lee, N. M. Jokerst, S. Palit, D. R. Smith, M. D. Ventra, and D. N. Basov, "Memory metamaterials," *Science*, vol. 325, pp. 1518–1521, September 2009.

[75] A. S. Alexandrov and A. M. Bratkovsky, "Polaronic memory resistors strongly coupled to electrodes," *Physical Review B*, vol. 80, p. 115321, September 2009.

[76] J. H. Krieger and S. M. Spitzer, "Non-traditional, non-volatile memory based on switching and retention phenomena in polymeric thin films," *Non-Volatile Memory Technology Symposium*, pp. 121–124, 2004.

[77] D. S. Kim, Y. H. Kim, C. E. Lee, and Y. T. Kim, "Colossal electroresistance mechanism in a $Au/Pr_{0.7}Ca_{0.3}MnO_3/Pt$ sandwich structure: Evidence for a mott transition," *Physical Review B*, vol. 74, p. 174430, November 2006.

[78] M. Quintero, P. Levy, A. G. Leyva, and M. J. Rozenberg, "Mechanism of electric-pulse-induced resistance switching in manganites," *Physical Review Letters*, vol. 98, p. 116601, March 2007.

[79] E. Arcangeletti, L. Baldassarre, D. D. Castro, S. Lupi, L. Malavasi, C. Marini, A. Perucchi, and P. Postorino, "Evidence of a pressure-induced metallization process in monoclinic VO_2," *Physical Review Letters*, vol. 98, p. 196406, May 2007.

[80] M. M. Qazilbash, A. A. Schafgans, K. S. Burch, S. J. Yun, B. G. Chae, B. J. Kim, H. T. Kim, and D. N. Basov, "Electrodynamics of the vanadium oxides VO_2 and V_2O_3," *Physical Review B*, vol. 77, p. 115121, March 2008.

[81] Y. V. Pershin and M. D. Ventra, "Memory effects in complex materials and nanoscale systems," *Advances in Physics*, vol. 60, pp. 145–227, November 2011.

[82] A. Sharoni, J. G. Ramrez, and I. K. Schuller, "Multiple avalanches across the metal-insulator transition of vanadium oxide nanoscaled junctions," *Physical Review Letters*, vol. 101, p. 026404, July 2008.

[83] Z. B. Yan, K. F. Wang, S. Z. Li, S. J. Luo, and J.-M. Liu, "Reversible resistance switching in $La_{0.225}Pr_{0.4}Ca_{0.375}MnO_3$: The joule-heat-assisted phase transition," *Applied Physics Letters*, vol. 95, p. 143502, October 2009.

[84] N. Gergel-Hackett, B. Hamadani, B. Dunlap, J. Suehle, C. Richter, C. Hacker, and D. Gundlach, "A flexible solution-processed memristor," *IEEE Electron Device Letters*, vol. 30, pp. 706–708, July 2009.

[85] Y. Ho, G. Huang, and P. Li, "Nonvolatile memristor memory: Device characteristics and design implications," *Proc. IEEE/ACMInt. Conf. Comput. Aided Design (ICCAD)*, pp. 485–490, November 2009.

[86] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, and R. S. Williams, "Switching dynamics in titanium dioxide memristive devices," *Journal of Applied Physics*, vol. 106, pp. 1–6, October 2009.

[87] W. Yi, F. Perner, M. S. Qureshi, H. Abdalla, M. D. Pickett, J. J. Yang, M.-X. M. Zhang, G. Mederios-Ribeiro, and R. S. Williams, "Feedback write scheme for memristive switching devices," *Applied Physics A*, vol. 102, pp. 973–982, March 2011.

[88] H. Akimoto, H. Kanai, Y. Uehara, T. Ishizuka, and S. Kameyama, "Analysis of thermal magnetic noise in spin-valve GMR heads by using micromagnetic simulation," *Journal of Applied Physics*, vol. 97, p. 10N705, May 2005.

[89] M. A. Mohamed, N. Inami, E. Shikoh, Y. Yamamoto, H. Hori, and A. Fujiwara, "Fabrication of spintronic device by direct synthesis of single-walled carbon nanotubes from ferromagnetic electrodes," *Science and Technology of Advanced Materials*, vol. 9, pp. 1–5, July 2008.

[90] M. Hu, H. Li, Y. Chen, X. Wang, and R. E. Pino, "Geometry variations analysis of TiO_2 thin-film and spintronic memristors," *IEEE Design Automation Conference (ASP-DAC)*, pp. 25–30, January 2011.

[91] D. Batas and H. Fiedler, "A memristor spice implementation and a new approach for magnetic flux-controlled memristor modelling," *IEEE Transactions on Nanotechnology*, vol. 10, pp. 250–255, March 2011.

[92] H. Elgabra, I. A. Farhat, A. S. A. Hosani, D. Homouz, and B. Mohammad, "Mathematical modeling of a memristor device," *International Conference on Innovations in Information Technology (IIT)*, pp. 156–161, March 2012.

[93] M. Mahvash and A. C. Parker, "A memristor SPICE model for designing memristor circuits," *IEEE International Midwest Symposium on Circuits and Systems*, pp. 989–992, August 2010.

[94] A. Rak and G. Cserey, "Macromodeling of the memristor in SPICE," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, pp. 632–636, April 2010.

[95] Z. Biolek, D. Biolek, and V. Biolkova, "Spice model of memristor with nonlinear dopant drift," *radio engineering*, vol. 18, pp. 210–214, 2009.

[96] H. Abdalla and M. D. Pickett, "Spice modeling of memristors," *IEEE International Symposium on Circuits and Systems*, pp. 1832–1835, May 2011.

[97] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: Threshold adaptive memristor model," *IEEE Transactions on Circuits and Systems I*, vol. 60, pp. 211–221, January 2013.

[98] A. C. Cabe and S. Das, "Performance simulation and analysis of a CMOS/nano hybrid nano processor system," *Nanotechnology*, vol. 20, p. 165203, March 2009.

[99] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, and P. Mazumder, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Letters*, vol. 10, pp. 1297–1301, March 2010.

[100] F. Alibart, S. Pleutin, D. Guerin, C. Novembre, S. Lenfant, K. Lmimouni, C. Gamrat, and D. Vuillaume, "An organic nanoparticle transistor behaving as a biological spiking synapse," *Advanced Functional Materials*, vol. 20, pp. 330–337, January 2010.

[101] C. Yakopcic, T. M. Taha, G. Subramanyam, and S. Rogers, "Multiple memristor read and write circuit for neuromorphic applications," *Proceedings of International Joint Conference on Neural Networks*, pp. 2676–2682, July-August 2011.

[102] S.-M. K. S. Shin, K. Kim, "Memristor applications for programmable analog ICs," *IEEE Transactions on Nanotechnology*, vol. 10, pp. 266–274, March 2011.

[103] D. B. Strukov and K. K. Likharev, "Reconfigurable hybrid CMOS/nanodevice circuits for image processing," *IEEE Transactions on Nanotechnology*, vol. 6, pp. 696–710, November 2007.

[104] D. Strukov and K. Likharev, "CMOL FPGA: A cell-based, reconfigurable architecture for hybrid digital circuits using two-terminal nanodevices," *Nanotechnology*, vol. 16, pp. 888–900, April 2005.

[105] J. G. Simmons, "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film," *Journal of Applied Physics*, vol. 34, pp. 1793–1803, January 1963.

[106] G. S. Snider, "Cortical computing with memristive nanodevices," *SciDAC Review*, vol. 10, pp. 58–65, 2008.

[107] R. C. Froemke and Y. Dan, "Spike timing-dependent synaptic modification induced by natural spike trains nature," *Nature*, vol. 416, pp. 433–438, January 2002.

[108] Y. V. Pershin and M. D. Ventra, "Neuromorphic, digital, and quantum computation with memory circuit elements," *Proceedings of the IEEE*, vol. 100, pp. 2071–2080, June 2012.

[109] J. Cong and B. Xiao, "mrFPGA: A novel FPGA architecture with memristor-based reconfiguration," *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 1–8, June 2011.

[110] D. Niu, Y. Chen, and Y. Xie, "Low-power dual-element memristor based memory design," *International Symposium on Low-Power Electronics and Design (ISLPED)*, pp. 25–30, August 2010.

[111] H. Kim, M. P. Sah, C. Yang, and L. O. Chua, "Memristor-based multilevel memory," *International Workshop on Cellular Nanoscale Networks and their Applications (CNNA)*, pp. 1–6, February 2010.

[112] H. Manem and G. S. Rose, "A read-monitored write circuit for 1T1M multi-level memristor memories," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2011.

[113] Q. Xia, M. D. Pickett, J. J. Yang, X. Li, W. Wu, G. Medeiros-Ribeiro, and R. S. Williams, "Two- and three-terminal resistive switches: Nanometer-scale memristors and memistors," *Advanced Functional Materials*, vol. 21, pp. 2660–2665, July 2011.

[114] D. B. Strukov, J. L. Borghetti, and R. S. Williams, "Coupled ionic and electronic transport model of thin-film semiconductor memristive behavior," *Small*, vol. 5, pp. 1058–1063, May 2009.

[115] M. J. Lee, Y. Park, B. S. Kang, S. E. Ahn, C. Lee, K. Kim, W. Xianyu, G. Stefanovich, J. H. Lee, S. J. Chung, Y.-H. Kim, C.-S. Lee, J.-B. Park, and I.-K. Yoo, "2-stack 1D-1R cross-point structure with oxide diodes as switch elements for high density resistance RAM applications," *Proceedings IEEE International Electron Devices Meeting*, pp. 771–774, December 2007.

[116] R. S. Williams, "Multi-terminal electrically actuated switch," *U.S. Patent 0079029*, April 2008.

[117] F. Lai and Y. L. Chuang, "A new design methodology for multiport sram cell," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 41, pp. 677–685, November 1994.

[118] G. M. Huang, W. Dong, Y. Ho, and P. Li, "Tracing SRAM separatrix for dynamic noise margin analysis under device mismatch," *IEEE International Behavioral Modeling and Simulation Workshop (BMAS)*, pp. 6–10, September 2007.

Appendix A: Memristor verilog-A model [97]

```
////////////////////////////////////////////////
// VerilogA model for memristor
//
// kerentalis@gmail.com
// Dimafliter@gmail.com
// skva@tx.technion.ac.il
//
// Technion - Israel institute of technology
// EE Dept. December 2011
//
////////////////////////////////////////////////
'include "disciplines.vams"
'include "constants.vams"
// define meter units for w parameter
nature distance
access = Metr;
units = "m";
abstol = 0.01n;
endnature
discipline Distance
potential distance;
enddiscipline
module Memristor(p, n,w_position);
input p;//positive pin
output n;//negative pin
output w_position;// w-width pin
electrical p, n,gnd;
Distance w_position;
ground gnd;
parameter real model = 2;
// define the model:
// 0 - Linear Ion Drift;
// 1 - Simmons Tunnel Barrier;
// 2 - Team model;
// 3 - Nonlinear Ion Drift model
parameter real window_type=2;
// define the window type:
// 0 - No window;
// 1 - Jogelkar window;
// 2 - Biolek window;
// 3 - Prodromakis window;
// 4 - Kvatinsky window (Team model only)
```

```
parameter real dt=0;
// user must specify dt same as max step size in
// transient analysis & must be at least 3 orders
//smaller than T period of the source
parameter real init_state=0.5;
// the initial state condition [0:1]
////////////// Linear Ion Drift model //////////////
//parameters definitions and default values
parameter real Roff = 200000;
parameter real Ron = 100;
parameter real D = 3n;
parameter real uv = 1e-15;
parameter real w_multiplied = 1e8;
// transformation factor for w/X width
// in meter units
parameter real p_coeff = 2;
// Windowing function coefficient
parameter real J = 1;
// for prodromakis Window function
parameter real p_window_noise=1e-18;
// provoke the w width not to get stuck at
// 0 or D with p window
parameter real threshhold_voltage=0;
// local variables
real w;
real dwdt;
real w_last;
real R;
real sign_multply;
real stp_multply;
real first_iteration;
////////////// Simmons Tunnel Barrier model //////////////
//parameters definitions and default values
//for Simmons Tunnel Barrier model
parameter real c_off = 3.5e-6;
parameter real c_on = 40e-6;
parameter real i_off = 115e-6;
parameter real i_on = 8.9e-6;
parameter real x_c = 107e-12;
parameter real b = 500e-6;
parameter real a_on = 2e-9;
parameter real a_off = 1.2e-9;
// local variables
real x;
real dxdt;
real x_last;
```

```
///////////////////TEAM model/////////////////////
parameter real K_on=-8e-13;
parameter real K_off=8e-13;
parameter real Alpha_on=3;
parameter real Alpha_off=3;
parameter real IV_relation=0;
// IV_relation=0 means linear V=IR.
// IV_relation=1 means nonlinear V=I*exp..
parameter real x_on=0;
parameter real x_off=3e-09; // equals D
// local variables
real lambda;
/////////////Nonlinear Ion Drift model /////////////
parameter real alpha = 2;
parameter real beta = 9;
parameter real c = 0.01;
parameter real g = 4;
parameter real N = 14;
parameter real q = 13;
parameter real a = 4;
analog function integer sign;
//Sign function for Constant edge cases
real arg; input arg;
sign = (arg >= 0 ? 1 : -1 );
endfunction
analog function integer stp; //Stp function
real arg; input arg;
stp = (arg >= 0 ? 1 : 0 );
endfunction
/////////////////// MAIN ///////////////////////
analog begin
if(first_iteration==0) begin
w_last=init_state*D;
// if this is the first iteration,
//start with w_init
x_last=init_state*D;
// if this is the first iteration,
// start with x_init
end
/////////////Linear Ion Drift model /////////////
if (model==0) begin // Linear Ion Drift model
dwdt =(uv*Ron/D)*I(p,n);
//change the w width only if the
// threshhold_voltage permits!
if(abs(I(p,n))<threshhold_voltage/R) begin
w=w_last;
```

87

```
dwdt=0;
end
// No window
if ((window_type==0) || (window_type==4)) begin
w=dwdt*dt+w_last;
end // No window
// Jogelkar window
if (window_type==1) begin
if (sign(I(p,n))==1) begin
sign_multply=0;
if(w==0) begin
sign_multply=1;
end
end
if (sign(I(p,n))==-1) begin
sign_multply=0;
if(w==D) begin
sign_multply=-1;
end
end
w=dwdt*dt*(1-pow(2*w/D- 1,2*p_coeff))+w_last+sign_multply*p_window_noise;
end // Jogelkar window
// Biolek window
if (window_type==2) begin
if (stp(-I(p,n))==1) begin
stp_multply=1;
end
if (stp(-I(p,n))==0) begin
stp_multply=0;
end
w=dwdt*dt*(1-pow(w/D-stp_multply,2*p_coeff))+w_last;
end // Biolek window
// Prodromakis window
if (window_type==3) begin
if (sign(I(p,n))==1) begin
sign_multply=0;
if(w==0) begin
sign_multply=1;
end
end
if (sign(I(p,n))==-1) begin
sign_multply=0;
if(w==D) begin
sign_multply=-1;
end
end
```

```
w=dwdt*dt*J*(1-pow(pow(w/D- 0.5,2)+0.75,p_coeff))+w_last+sign_multply*p_window_noise;
end // Prodromakis window
if (w>=D) begin
w=D;
dwdt=0;
end
if (w<=0) begin
w=0;
dwdt=0;
end
//update the output ports(pins)
R=Ron*w/D+Roff*(1-w/D);
w_last=w;
Metr(w_position) <+ w*w_multiplied;
V(p,n) <+ (Ron*w/D+Roff*(1-w/D))*I(p,n);
first_iteration=1;
end // end Linear Ion Drift model
////////// Simmons Tunnel Barrier model ////////////
if (model==1) begin // Simmons Tunnel Barrier model
if (sign(I(p,n))==1) begin
dxdt =c_off*sinh(I(p,n)/i_off)*exp(- exp((x_last-a_off)/x_c-abs(I(p,n)/b))-x_last/x_c);
end
if (sign(I(p,n))==-1) begin
dxdt =c_on*sinh(I(p,n)/i_on)*exp(-exp((a_on-x_last)/x_c-abs(I(p,n)/b))-x_last/x_c);
end
x=x_last+dt*dxdt;
if (x>=D) begin
x=D;
dxdt=0;
end
if (x<=0) begin
x=0;
dxdt=0;
end
//update the output ports(pins)
R=Ron*(1-x/D)+Roff*x/D;
x_last=x;
Metr(w_position) <+ x/D;
V(p,n) <+ (Ron*(1-x/D)+Roff*x/D)*I(p,n);
first_iteration=1;
end // end Simmons Tunnel Barrier model
/////////////////////// TEAM model /////////////////////
if (model==2) begin // TEAM model
if (I(p,n) >= i_off) begin
dxdt =K_off*pow((I(p,n)/i_off-1),Alpha_off);
end
```

```
if (I(p,n) <= i_on) begin
dxdt =K_on*pow((I(p,n)/i_on-1),Alpha_on);
end
if ((i_on<I(p,n)) && (I(p,n)<i_off)) begin
dxdt=0;
end
// No window
if (window_type==0) begin
x=x_last+dt*dxdt;
end // No window
// Jogelkar window
if (window_type==1) begin
x=x_last+dt*dxdt*(1-pow((2*x_last/D- 1),(2*p_coeff)));
end // Jogelkar window
// Biolek window
if (window_type==2) begin
if (stp(-I(p,n))==1) begin
stp_multply=1;
end
if (stp(-I(p,n))==0) begin
stp_multply=0;
end
x=x_last+dt*dxdt*(1-pow((x_last/D-stp_multply),(2*p_coeff)));
end // Biolek window
// Prodromakis window
if (window_type==3) begin
x=x_last+dt*dxdt*J*(1- pow((pow((x_last/D-0.5),2)+0.75),p_coeff));
end // Prodromakis window
//Kvatinsky window
if (window_type==4) begin
if (I(p,n) >= 0) begin
x=x_last+dt*dxdt*exp(-exp((x_last-a_off)/x_c));
end
if (I(p,n) < 0) begin
x=x_last+dt*dxdt*exp(-exp((a_on-x_last)/x_c));
end
end // Kvatinsky window
if (x>=D) begin
dxdt=0;
x=D;
end
if (x<=0) begin
dxdt=0;
x=0;
end
lambda = ln(Roff/Ron);
```

```
//update the output ports(pins)
x_last=x;
Metr(w_position) <+ x/D;
if (IV_relation==1) begin
V(p,n) <+ Ron*I(p,n)*exp(lambda*(x-x_on)/(x_off-x_on));
end
else if (IV_relation==0) begin
V(p,n) <+ (Roff*x/D+Ron*(1-x/D))*I(p,n);
end
first_iteration=1;
end // end Team model
///////////// Nonlinear Ion Drift model /////////////
if (model==3) begin // Nonlinear Ion Drift model
if (first_iteration==0) begin
w_last=init_state;
end
dwdt = a*pow(V(p,n),q);
// No window
if ((window_type==0) ―― (window_type==4)) begin
w=w_last+dt*dwdt;
end // No window
// Jogelkar window
if (window_type==1) begin
w=w_last+dt*dwdt*(1-pow((2*w_last- 1),(2*p_coeff)));
end // Jogelkar window
// Biolek window
if (window_type==2) begin
if (stp(-V(p,n))==1) begin
stp_multply=1;
end
if (stp(-V(p,n))==0) begin
stp_multply=0;
end
w=w_last+dt*dwdt*(1-pow((w_last-stp_multply),(2*p_coeff)));
end // Biolek window
// Prodromakis window
if (window_type==3) begin
w=w_last+dt*dwdt*J*(1-pow((pow((w_last- 0.5),2)+0.75),p_coeff));
end // Prodromakis window
if (w>=1) begin
w=1;
dwdt=0;
end
if (w<=0) begin
w=0;
dwdt=0;
```

```
end
//change the w width only if the
// threshhold_voltage permits!
if(abs(V(p,n))<threshhold_voltage) begin
w=w_last;
end
//update the output ports(pins)
w_last=w;
Metr(w_position) <+ w;
I(p,n) <+ pow(w,N)*beta*sinh(alpha*V(p,n))+c*(exp(g*V(p,n))- 1);
first_iteration=1;
end // end Nonlinear Ion Drift model
end // end analog
endmodule
```

Appendix B: Adding Verilog-A to Cadence Spectre simulation tools

1. Create new library and name it as displayed in Figures B.1 and B.2.
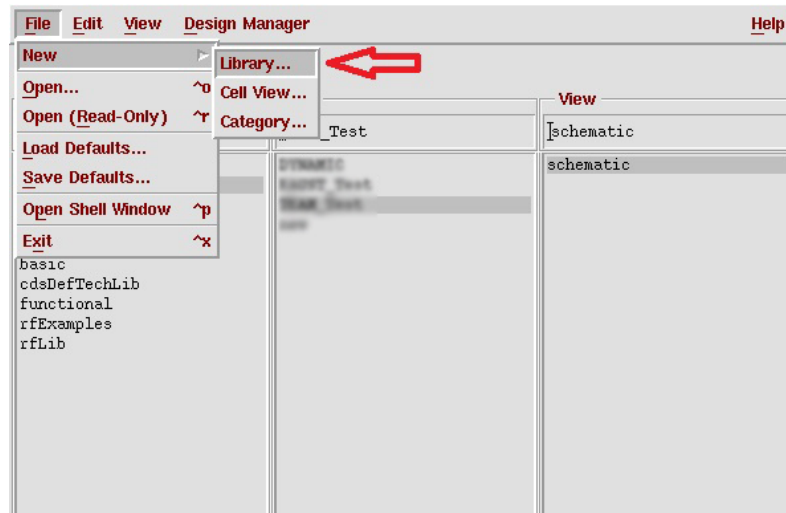

Figure B.1: Create new library.

2. Create file to add the verilog-A code as displayed in Figures B.3 and B.4.

3. Copy and paste the verilog-A code to the new file and save it as displayed in Figures B.5.

4. Draw a symbol for the verilog-A code and save the symbol to use it in different circuits design as displayed in Figures B.6.
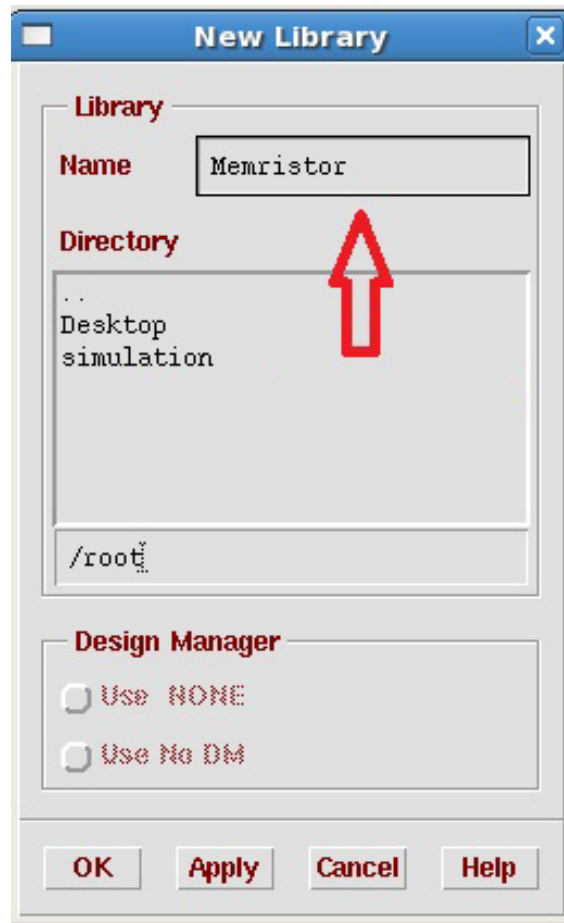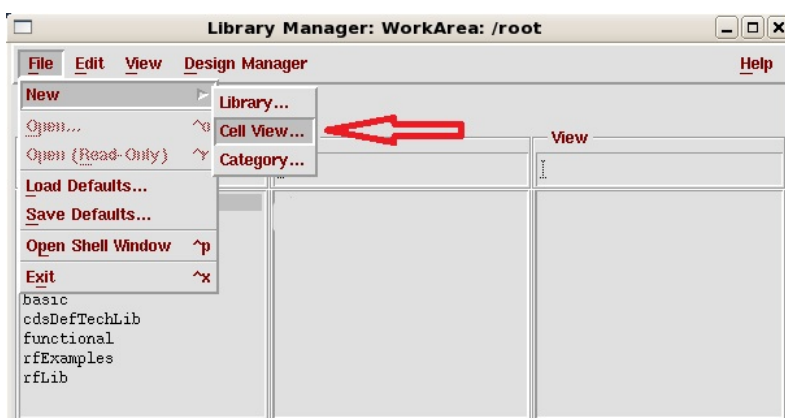
Figure B.2: Naming the new library.

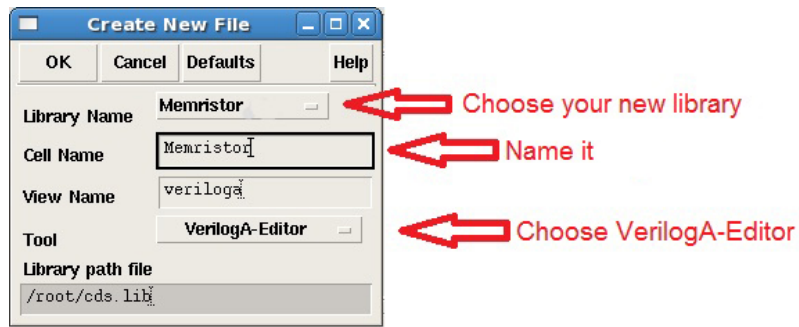Figure B.3: Create new file to add the code.
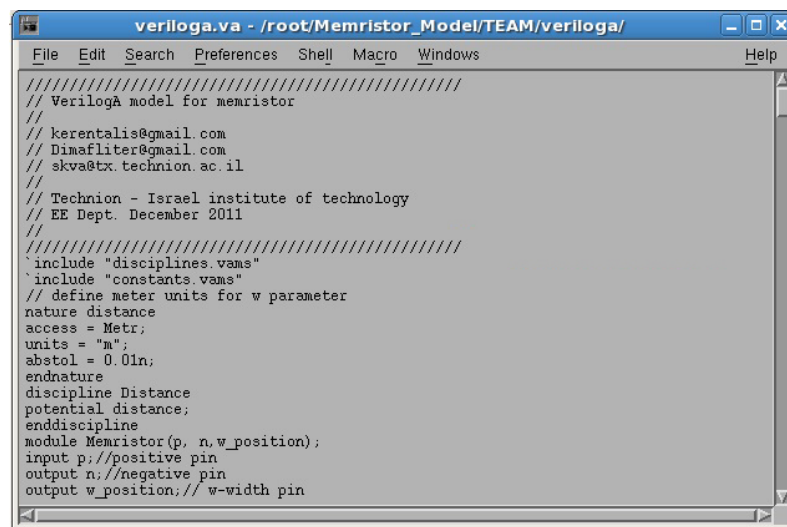
Figure B.4: Appropriate choices for creating the new file.

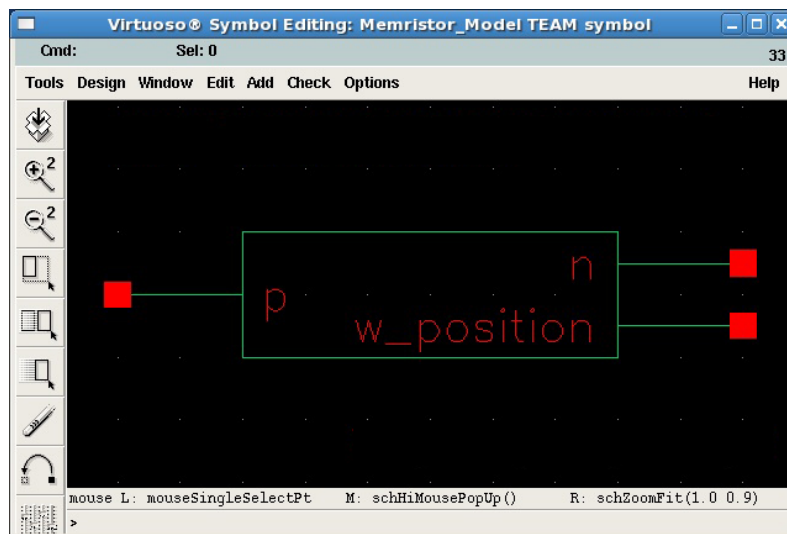Figure B.5: Copy and paste the verilog-A code to the new file.

Figure B.6: Draw a symbol for the verilog-A code.

95

الملخص

إنشـاء تقنيـة ذاكـرة شاملة ثابتة هو أمر حيـوي لابد منه لتوفير قدرات تخزينيه ضخمـة مطلوبـة لوسائل الحوسبـة النانويـة. الذاكـرة ذات المقاومة (ممرستور)، "عنصـر الدائرة الرابـع المفقـود"، المكتشفة حديثا هو المرشح المحتمل لذاكرة الجيل التالي والتي أصبحت محـل إهتمـام بالـغ في السنوات القليلـة الآخيـرة. يرجع ذلك الاهتمـام بالممرستور لمميزاته التى تتضمـن: صغر الحجم, إستهلاك طاقـه أقل من التكنولوجيا المستخدمه حاليا, قدرة الممرستور على تغيير مقاومته بناء على قيمة التيار المار خلاله مع الاحتفاظ بتلك القيمه عند قطع مصدر التيار بالأضافه إلى قلة تكلفة تصنيع الممرستور. في هذا البحث، تمت مراجعة اشكال مختلفه من التقنيـات المقترحـه لتصنيع الممرستور، كما تم إجراء مقارنـة بين أفضل تقنيتين لتصنيع الممرستور و الحصـول عليه كمنتـج مادي. أيضا، تم ذكر التطبيقات المختلفة المعتمدة على الممرستور مع أيضاحها و بيان افضل تلك التطبيقات. أحد اهم تلك التطبيقات هو استخدام الممرستور كعنصر ذاكره لتخزين البيانات. أستخدام كعنصر ذاكره لتخزين البيانات يعتبر تطبيق يستفيد بشكل مباشر من مميزات الممرستور. الأبحـاث المنشوره حاليا توضح مشكلة أستخدام الممرستور كعنصر للذاكرة. تكمن تلك المشكلـه فى عمليـة قراءة البيانات المخزنه على الممرستور و تأثير عمليـة القراءه على البيانات المخزنه، حيث انه من الممكن تدمير البيانات المخزنـة على الممرستور خلال عملية القراءة كما يظهر فى تلك الابحـاث المنشوره حديثا. يهدف هذا البحـث في الأساس إلى حل هذة المشكلـة وذلك من خـلال نقطتين رئيسيتيـن. تتنـاول النقطه الأولـى الإعتبارات التى يجب مراعتها عند تصميـم دوائر القراءة/الكتابـة من/على دوائر الذاكـرة المعتمدة على الممرستور. حيث تم طرح تلك الاعتبارات مع إيضاح كيفية الاستفاده منها او تجنب حدوث مشكلات عند أستخدام الممرستور كعنصر ذاكره لتخزين البيانات. و من ثم، تم استخدام تلك الاعتبارات فى تصميـم ثلاث دوائـر قراءة/كتابة جديدة لحل مشكلة تدمير البيانات المخزنـه على الممرستور خلال عملية القراءة بالإضافة إلى تسهيل عملية القراءة والكتابة من و إلى جهاز الممرستور المستخدم كعنصر للذاكرة. بنـاءا على عمليـات المحاكاه المعتمده على اخر البيانات المنشورة حديثا عن الممرستور, أظهرت دائرتين من الثـلاث دوائر المقدمـه فى هذا البحث قدرتها على حل تلك المشكلـه المتعلقه بتدمير

البيانات المخزنه على الممرستور عند أجراء عملية القراءه. كما تُظهر الدوائر المقدمة إستهلاك طاقة أقل و زمن تأخير أقل مقارنة بدوائر القراءة/الكتابة المنشورة حديثا. بالإضافة إلى ذلك، تشغل الدوائر المقدمة مساحة تصميم صغيرة.

و تتكون الرساله من الفصول التاليه:

الفصل الاول يتناول مقدمه عن موضوع البحث (ممرستور).

الفصل الثانى يحتوى على مسح عام على ما توصلت إليه التكنولوجيا الحديثه فى مجال الذاكره الرقميه.

الفصل الثالث به شرح تفصيلى للأنواع المختلفه للممرستور كما يقدم مقارنه بين اشهر نوعين من تلك الانواع.

الفصل الرابع يناقش التطبيقات المختلفه التى تعتمد على الممرستور. كما يعرض مسح عام على الاوراق البحثيه التى تعرض دوائر القراءه/الكتابه من/على الذاكره المعتمده على الممرستور كعنصر ذاكره لحفظ البيانات مع شرح مبسط لأهم التقنيات و الأساليب المستخدمه مع ايضاح ما تواجهه تلك الدوائر من مشكلات.

الفصل الخامس يقدم دوائر جديده القراءه/الكتابه من/على الذاكره المعتمده على الممرستور كعنصر ذاكره لحفظ البيانات. كما يقدم مقارنه بين نتائج المحاكاه الخاصه بالدوائر المقترحه فى الرساله و نتائج المحاكاه للدوائر السابقه.

الفصل السادس و هو ملخص لأهم الوسائل المستخدمه و المعروضه في الرساله. كما يحتوى عرض لأهم النتائج التي تحتويها الرساله و كذلك عرض الأبحاث المنشوره و أهم الأضافات و الخطط المستقبليه لاستكمال العمل.

مهندس:	محمد سيد أحمد محمد الشامى
تاريخ الميلاد:	١٩٨٦/٣/٢١
الجنسية:	مصرى
تاريخ التسجيل:	٢٠١٠/١٠/١٠
تاريخ المنح:	............/...../.....
القسم:	الالكترونيات و الاتصـالات الكهربيـة
الدرجة:	ماجستير

المشرفون:

ا.د. محمد سـامح سعيد

د. حسن مصطفى حسن

الممتحنون:

أ.د. حسنين عامر حامد   (الممتحن الخارجي)

أ.د. محمد فتحى   (الممتحن الداخلي)

أ.د. محمد سـامح سعيد   (المشرف الرئيسي)

عنوان الرسالة:

تصميـم دوائر كهربائيـة مناسبــه لبرمجـة مصفوفات الذاكره المعتمـده على المقاومـه ذات الذاكـره (ممرستـور).

الكلمات الدالة:

الذاكره النانو ، ممرستور ، دائرة، قراءه/كتابه

ملخص الرسالة:

المقاومه ذات الذاكره (ممرستور)، و المعروفه بالعنصر المفقود الرابع، تعتبر مرشح محتمل للجيل القادم من الذاكره. لاقى الممرستور اهتمام كبير من المجتمع البحثى خلال السنين القليله الماضيه. تقدم تلك الرساله ثلاث دوائر مناسبه للاستخدام فى مصفوفات الذاكره المعتمده على الممرستور. تتميز دوائر القراءه/الكتابه المقدمه بثلاث ميزات اساسيه. أولا، دائرتين من الثلاث دوائر المقدمه تمتاز بميزة القراءه دون التأثير على المعلومات المخزنه. تعتبر تلك الميزه هى الاهم لما تعانيه الدوائر المقترحه حاليا من مشكلة تدمير البيانات المخزنه على الممرستور عند قرائتها. ثانيا، الدوائر المقدمه تشغل مساحه صغيره مقارنة بما تم نشره من دوائر مسبقا. و أخيرا، الدوائر المقدمه اقل استهلاكا للطاقة و لها زمن تأخير أقل مقارنة بأخر ما تم نشره من دوائر قراءه/كتابه من/على الممرستور.

تصميــم دوائر كهربائيـــة مناسبـــه لبــرمجـــة مصـفـوفـات الـذاكــره المعتمـــده على المقاومـه ذات الذاكــره (ممرستـور)

اعداد

محمـد سيـد أحمـد محمـد الشــامى

رسالة مقدمة إلى كلية الهندسة ـ جامعة القاهرة
كجزء من متطلبات الحصول على درجة ماجستير العلوم
في
الالكتــرونيـات و الاتصـــالات الكهـربيــــة

يعتمد من لجنة الممتحنين:

المشرف الرئيسى	الاستاذ الدكتور: محمـد سامـح سعـيد
الممتحن الداخلي	الاستاذ الدكتور: محمد فتحـى
الممتحن الخارجي	الاستاذ الدكتور: حسنيـن عامر حامـد

أستاذ الالكترونيات بقسم الالكترونيات و الاتصالات الكهربية
كلية الهندسة ـ الجامعة الأمريكيه بالقاهرة

كليــة الهندسـة ـ جامعـة القاهـرة
الجيزة ـ جمهوريـة مصر العربيــة
٢٠١٤

تصميـم دوائر كهربائيــة مناسبــه لبـرمجــة مصفوفــات الذاكـره
المعتمــده على المقاومــه ذات الذاكــره (ممـرستـور)

اعداد

محمـد سيـد أحمـد محمـد الشـامى

رسالة مقدمة إلى كلية الهندسة ـ جامعة القاهرة
كجزء من متطلبات الحصول على درجة ماجستير العلوم
في
الالكتـرونيـات و الاتصـــالات الكهـربيــة

تحت اشراف

<table>
<tr><td>أ.د. محمـد سامـح سعيـد</td><td>د. حسـن مصطفـى حسـن</td></tr>
<tr><td>...........................</td><td>..........................</td></tr>
<tr><td>أستاذ الالكترونيات بقسم الالكترونيات و
الاتصالات الكهربيــة
كلية الهندسة ـ جامعة القاهرة</td><td>مدرس الالكترونيات بقسم الالكترونيات و
الاتصالات الكهربيــة
كلية الهندسة ـ جامعة القاهرة</td></tr>
</table>

كليــة الهندسـة ـ جامعـة القاهـرة
الجيزة ـ جمهوريـة مصـر العربيـة
٢٠١٤

تصميــم دوائـر كهـربائيــة مناسبــه لبـرمجــة مصفـوفـات الذاكـره
المعتمــده على المقاومــه ذات الذاكــره (ممرستـور)

اعداد

محمــد سيــد أحمــد محمــد الشــامى

رسالة مقدمة إلى كلية الهندسة ـ جامعة القاهرة
كجزء من متطلبات الحصول على درجة ماجستير العلوم
في
الالكتـرونيـات و الاتصـــالات الكهـربيــة

كليــة الهندسـة ـ جامعـة القاهـرة
الجيزة ـ جمهوريـة مصر العربيــة
٢٠١٤