2018 30th International Conference on Microelectronics (ICM)

# Multi-Bit RRAM Transient Modelling and Analysis

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***Abstract*—Memristors have gained significant attention in various applications due to their unique properties, especially in nonvolatile memory technologies. Thus, there exist many mathematical and compact models that aim to simulate the behavior of memristors accurately. In this work, a comparative study on the capability of different memristor models for transient multi-bit memristive memory simulation is conducted. Moreover, this paper proposes a window function that improves the accuracy of memristor models based on the filament-growth theory. Simulation results reveal the enhancements of the proposed window function and highlight the advantages and the disadvantages of the studied models in transient analysis.**

***Keywords—RRAM, Memristor model, Switching dynamics, Verilog-A, Window function.***

## I. Introduction

Memristor is an electrical component that is capable of controlling the flow of electric charges in a circuit and can keep memory about the amount flowen, it was first introduced in 1971 by Professor Chua [1]. Memristive devices are promising for many applications and are expected to replace CMOS transistors [2]. Its known applications include, but not limited to, building logic circuits [3], neural networks neuromorphic devices [4], and nonvolatile memory arrays [5]. Memristor represents an ideal alternative for CMOS memory architectures due to its low power, high density, non-volatility, high speed, and analog behavior [2]. This analog behavior enables the storage of more than one bit in a single memristor memory cell.

After the first device was fabricated in 2008 [6], HP labs presented the first memristor model assuming two variable resistors connected in series [7]. Through the following years, many studies have been conducted to propose descriptive models for memristors [8-12]. Compatible read/write circuits are designed based on these models [13-15]. Despite the availability of many memristor models; there are several challenges to enhance accuracy, convergence, and reduce computational complexity. This paper investigates the applicability of existing memristor models in transient multi-bit memory simulations; moreover, it proposes a modification for existing models to improve their mimicry for actual devices based on experimental insights [16]. Despite the availability of many comparative studies that evaluate the performance of memristor models, to the best of our knowledge, this is the first study based on the transient response of the memristor.

The rest of this paper is structured as follows. First, in Section II, different available memristor models are reviewed. Section III presents the proposed modification for the Stanford model and the motivation behind it. Verification and simulation results of the different memristor models are presented in Section IV. Section V draws the conclusion.

## II. Review of Existing Memristor Simulation Models

Available memristor models share the same basic formulation, where the resistance of the memristor is controlled by a state variable which changes in accordance to an applied external bias. The available models define hard boundary limits on this state variable to guarantee that the memristor device switches between two definite states.

### A. Simmons Tunnel Barrier Model

This is the most accurate model for simulating $TiO_2$ memristive devices; however, its accuracy degrades upon modeling other memristor families. It is a physical model that exhibits nonlinear and asymmetric switching characteristics [8]. In this model, the memristor active layer is modelled as a resistor in series with an electron tunnel barrier, and the state variable is defined as the width of the tunneling barrier.

### B. VTEAM Model

This is a simple generic model that aims to simplify the mathematical formulation of the Simmons Tunnel Barrier Model. The VTEAM model is based on two basic assumptions. First, there is a value for a threshold voltage that must be exceeded to change the state variable and second, the VTEAM model approximates the exponential dependence of the rate of change of the tunneling barrier thickness on the applied voltage. This dependency is modelled as a polynomial function that depends only on the applied voltage and independent of the current state variable [9]. In addition, the VTEAM model has the flexibility to have a linear or an exponential dependency between the state variable and the applied voltage.

### C. Stanford Model

Stanford model is a generic physics-based compact model that describes the switching mechanism of bipolar memristive devices as the growth of a conductive filament [11]. The state variable is presented by the gap size, which is the distance between the tip of the filament and the top electrode. In this model, the current exhibits exponential dependence on the state variable. The rate of change of the state variable is calculated considering the drift electric field, local temperature effects due to Joule heating, and temperature-enhanced oxygen ion migration.

### D. Arizona State University (ASU) Modification

This model is mainly based on the same physical formulation as Stanford model; however, it differs in its implementation. ASU modification aims to limit the rate of

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change of the state variable so that it is bounded by the same upper and lower boundaries as the state variable [12]. Therefore, the switching behavior becomes time invariant. On the contrary, the Stanford model limits only the state variable, but the rate of change of the state variable is boundless which might result in convergence errors and instable transient simulations.

## III. Proposed Modification

It has been experimentally observed that higher values of set current (Iset) require higher values of reset voltage (Vreset) [16]. This has been interpreted due to the formation of longer and more stable conducting filaments which requires higher reset voltages to rupture these filaments. This contradicts the modification presented by ASU; thus, during transient analysis, there is a dependency of the set and reset voltages on their preceding transition, which suggests that the switching behavior of memristive devices is bounded by narrow resistance bands for $R_{OFF}$ and $R_{ON}$ rather than single values.

Besides, accurate modeling of memristive devices with Stanford model requires accurate measurement of gap thickness during switching which requires complicated experimental setup [17].

Thus, in this work, a weighted window function is proposed which has minimal impact as long as the gap is within the assigned limitations; however, it degrades the ability of the state variable to surpass the boundaries which can be used according to (1) as illustrated in Fig. 1(a). Thus, the gap is no longer limited by the assigned lower and upper boundaries; it is limited by the oxide thickness, which is accurately controlled during the fabrication step.

There are a variety of functions that can be used to implement the window function as shown in Table I. For simplicity, the window function proposed shall be referred to as Zewail City (ZC) modification.

$$\frac{d(gap')}{dt} = \frac{d(gap)}{dt} * W_{zc} \qquad (1)$$

For implementation, Butterworth function is used, as it adds only two fitting parameters to the system, it is computationally efficient and more controllable as shown in Fig. 1(b, c) compared to other candidate functions, and it is

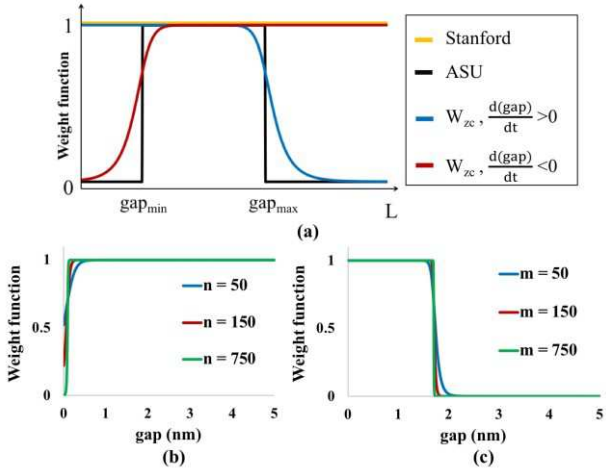


Fig.1. (a) Illustration of the proposed window function behavior compared to the Stanford model implementation and ASU modification implementation. (b) Butterworth function controllability for $\frac{d(gap)}{dt} < 0$. (c) Butterworth function controllability for $\frac{d(gap)}{dt} > 0$. Fig. 1(b, c) are plotted for $gap_{min}$ = 0.1nm, $gap_{max}$ = 1.7 nm, and L = 5nm.

symmetric as the weight of the function at the upper and lower boundaries is $\frac{1}{\sqrt{2}}$.

## IV. Verification and Simulation Results

For verification and unified comparison, the different models including the proposed ZC modification are fitted to the experimental data of IMEC $HfO_x$-based memristor [18-20] as shown in Fig. 2. The relative root mean square (RMS) error is used to evaluate the fitting of these models as described in [9]. Calculated relative root mean square (RMS) error of fitted models is given in Table II. The proposed ZC modification exhibits a fitting error less than 5%.

For simulation, Verilog-A models [21-23] are simulated on Cadence virtuoso with TSMC 130 nm CMOS technology file. The fitting parameters used for simulated models and ZC modification Verilog-A code are available at [24]. A 2V sinusoidal signal at 5Hz is used for IV characterization of the models, the NMOS transistor has a minimum length of 130 nm, a width of 155 nm, and the compliance current is 10 µA.

TABLE I. Proposed Candidate Functions for Window Function Implementation

*Butterworth function*

$$W_{zc} = \begin{cases} \dfrac{1}{\sqrt{1+\left(\dfrac{L+gap_{min}-gap_i}{L}\right)^{n}}} & , \ \dfrac{d(gap)}{dt} < 0 \\ \dfrac{1}{\sqrt{1+\left(\dfrac{gap_i}{gap_{max}}\right)^{m}}} & , \ \dfrac{d(gap)}{dt} > 0 \end{cases}$$

*Gaussian function*

$$W_{zc} = \begin{cases} 1-e^{-\left(\frac{gap_i}{gap_{min}}\right)^{x}} & , \ \dfrac{d(gap)}{dt} < 0 \\ e^{-\left(\frac{gap_i}{gap_{max}}\right)^{y}} & , \ \dfrac{d(gap)}{dt} > 0 \end{cases}$$

*Hyperbolic Tangent function*

$$W_{zc} = \begin{cases} \tanh^{p}\left(\dfrac{gap_i}{gap_{min}}\right) & , \ \dfrac{d(gap)}{dt} < 0 \\ 1 - \tanh^{q}\left(\dfrac{gap_i}{gap_{min}}\right) & , \ \dfrac{d(gap)}{dt} > 0 \end{cases}$$

*Generalized Logistic function*

$$W_{zc} = \begin{cases} \left(1+e^{-\left(\frac{gap_i}{gap_{min}}\right)^{s}}\right)^{-\alpha} & , \ \dfrac{d(gap)}{dt} < 0 \\ 1-\left(1+e^{-\left(\frac{gap_i}{gap_{max}}\right)^{t}}\right)^{-\beta} & , \ \dfrac{d(gap)}{dt} > 0 \end{cases}$$

Where L is the oxide thickness, $\frac{d(gap)}{dt}$ is the gap derivative, $gap_{min}$ and $gap_{max}$ are the lower and upper estimations for the boundaries respectively, and $gap_i$ is the instantaneous value of the gap.

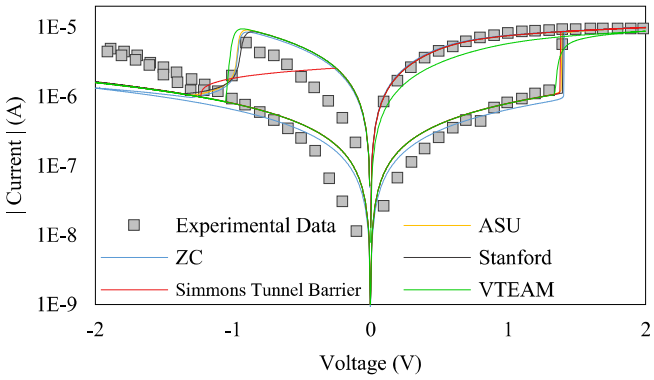


Fig. 2. IV characteristic of different models fitted to IMEC $HfO_x$ -based RRAM devices [17-19].

These different models are tested in a transient analysis for multi-bit writing capability. The transient signal is composed of 6 reset pulses different in amplitude and 6 set pulses equal in amplitude and high enough to set the memristor to its lowest resistance state as shown in Fig. 3(a). Reset pulses are applied to write different states according to this writing sequence: 100 kΩ, 600 kΩ, 1.25 MΩ (ROFF), 1.25 MΩ, 600 kΩ, and 100 kΩ. Set pulses are applied for erasing between every two successive writes to set the resistance state to RON (86.6 kΩ) following the Erase-before-RESET method [25]. Fig. 3(b). shows the response of all studied models excluding Stanford model during the transient analysis.

Stanford model implementation requires varying the set and reset pulses needed to reach the same states as the sequence used for testing other models. Through tuning, it is found that the accuracy of the amplitude of the pulses should be within 1μV. (i.e., any slight change in the applied voltage by this accuracy results in incorrect behavior). Fig. 3(c) shows the response of the Stanford model with pulses' amplitudes tuned with 1μV and 1mV accuracy. It is clear from Fig. 3(c) that an accuracy of 1mV results in an incorrect behavior of the memristor device.

As illustrated in Fig. 3(b), Simmons Tunnel Barrier Model, VTEAM, and ASU modified model show consistency in the transient analysis; however, it has been experimentally verified that during transient experiments the reset and set voltages lead to different states [16]. For reset the resistance state to 1.25 MΩ, ASU model shows a sharp change in the resistance which might lead to inaccurate measurement for writing time. Thus, ZC modification leads to reaching a resistance state higher than 1.25 MΩ with smooth transition which is physically more acceptable [16]. On the other hand, Stanford model shows extreme sensitivity to the applied bias with a diverging response as indicated by Fig. 3(c). In agreement with [16], Fig. 3(b) confirms that ZC modification is capable of doing transient analysis with non-divergent time variant behavior.

Fig. 4 shows the response of the different models to a train of reset pulses, the pulses are equal in amplitude and duration. In VTEAM, the rate of change of the state variable is independent of the instantaneous state unless a complex window function is used [12]. This is shown in the linear dependence of the resistance state on pulse number. All the other models show acceptable response; however, Simmons Tunnel Barrier model exhibits early saturation.

In order to verify the capability of these different models in multi-bit memory simulations, the 1T1R structure shown in

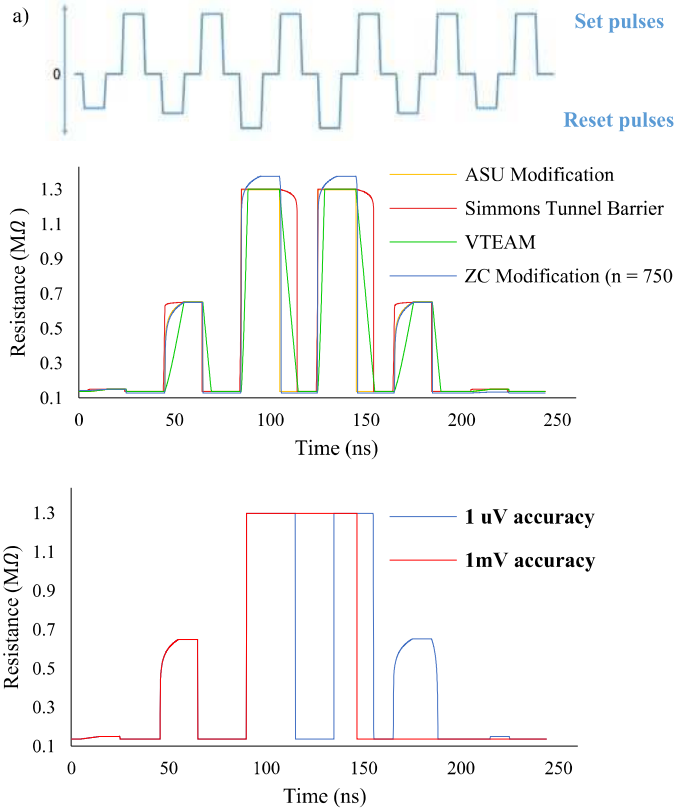


Fig. 3. (a) Sketch of input signal for transient analysis. (b) Transient analysis response of all studied models excluding Stanford model. (c) Stanford model response to input signal with different accuracies of time variant biases.

Fig. 5(a) is used. The top electrode of the memristor is connected to the set pulses' source. The MOSFET resistance is controlled with a DC bias on the gate, and the source terminal is connected to the reset pulses' source [25]. The reset pulse duration is 10 nS with $\tau_{rise}/\tau_{fall}$ time of 1nS; however, the reset pulse amplitude is varied from 0 to 2V with a linear step of 25mV. Fig. 5(b) shows the resistance state dependence on the reset pulse amplitude. In agreement with our fitting to the experimental data, Fig. 5(b) confirms that the slope of the reset transition in the IV curve is a sufficient indicator for the number of states that is achieved by each model.

## V. Conclusion

In this paper, a novel window function is proposed to be used with filament-growth based models to overcome their limitations in transient analysis. The advantages of the proposed modifications are:

- It eliminates the limits on the gap thickness which cannot be measured accurately [17]. Alternatively, it uses the thickness of the oxide layer as the limiting factor which can be characterized and controlled during fabrication.

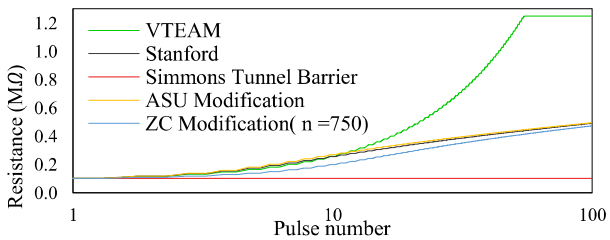


Fig. 4. Resistance state accumulation due to a train of pulses simulated with different models.

- Unlike other memristor models which have definite high resistance state (HRS) and low resistance state (LRS), ZC modified model introduces the concept of having narrow bands of HRS and LRS. This agrees with the experimental results reported by [16].
- ZC modified model shows a non-divergent time variant set and reset response in the transient analysis; thus, it overcomes both the extreme limitations of the Stanford model and the ASU modified model.
- ZC modified model has the capability of handling high bias conditions with a converging solution.

The proposed modification is not limited only to multi-bit memory simulations; however, its advantages enable better mimicry to actual memristive devices behavior.

TABLE II. ROOT MEAN SQUARE ERROR OF FITTED MODELS

| Model | Simmons Tunnel Barrier | VTEAM | Stanford | ASU Modification | ZC Modification |
|---|---|---|---|---|---|
| Error | 3.45% | 4.94% | 4.74% | 3.96 % | 4.83% |

## VI. ACKNOWLEDGMENT

This work was partially funded by ONE Lab at Zewail City of Science and Technology, Egypt and Cairo University, Egypt, Academy of Scientific Research and Technology (ASRT), and Mentor Graphics.

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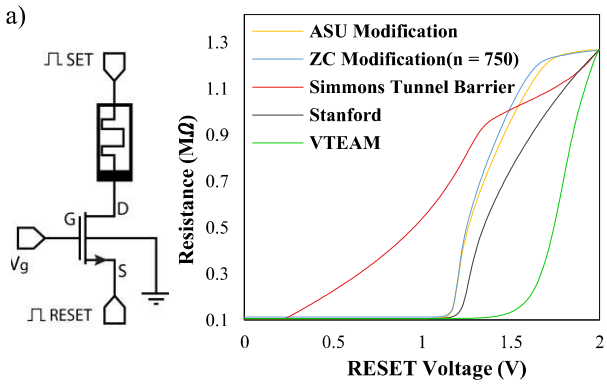


Fig. 5. (a) 1T1R configuration used for simulations. (b) Multistate writing behavior of different models.

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