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A Low-Power High-Efficiency Inductive Link Power Supply for Neural Recording and Stimulation System-on-Chip

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In this paper, a low-power high-efficiency inductive link power supply (ILPS) for neural recording and stimulation system-on-chip (SoC) is proposed that delivers 24 mW with 82% power conversion efficiency (PCE). The proposed CMOS power regulator is composed of a self-startup active voltage doubler rectifier (AVD) and a self-biased low dropout regulator (LDO). In addition, a modified low-power self-startup bandgap reference (BGR) circuit is utilized with dual-supply voltages to bias both the LDO circuit and the neural recording and stimulation SoC. The PCE of the AVD is improved through an on-chip calibration comparator for timing control. A prototype of the proposed ILPS is implemented using UMC 0.13 μm CMOS technology where the active implementation area is 0.06 mm^2. Using 2 $V_{IN,peak}$ at 13.56 MHz, a low-power ILPS is implemented to supply the proposed SoC by 1.2 V and achieve a high-power supply rejection ratio (PSRR) of -20 dB at 20 MHz. Finally, the overall quiescent current of the proposed ILPS from the AVD output and the low dropout regulator (LDO) output equal 7.5 μA and 8.5 μA, respectively.

Keywords: Low-Power, Active Voltage Doubler, Bandgap, Low-Dropout Regulator, Wireless Powering, Inductive Link, Self-Biased, Self-Startup, Zero-Power Startup, Energy Efficient Platforms, Biomedical Implants.

1. INTRODUCTION

Recently, implantable medical devices (IMDs) are growing widely for the treatment of intractable diseases or disorders, especially neurological ones. Figure 1 portrays a neural IMD that is used to record the neural signals through a multi-channel electrode array with a neural recording system-on-chip (SoC) where it amplifies and digitizes the neural signals to be processed using a digital processer to detect and predict the seizure. Based on the digital processing, the decision is taken for the neural stimulation sharing the same electrode array. These IMDs usually consume high-power in order of several milli-watts. Thus, a long-term reliable power supply is required to avoid the frequent surgery for the battery replacement.[1–3] However, the current battery technology lifetime is unable to sustain for a long time. Therefore, wireless power transfer (WPT) is considered as a good candidate to either power on IMDs or charge the backup batteries.[4]

Through the past few decades, inductive links have been the common method for WPT to IMDs.[4–14] In addition, ultrasonic links show a promising power conversion efficiency (PCE) for powering mm-sized IMDs.[3] Inductive and RF links have recently been modified for WPT to mm-sized neural IMDs.[11–14] A near-field inductive link power supply (ILPS) can be divided into three main blocks as follows: (1) power amplifier amplifies the RF signal to drive the near-field coils, (2) near-field coils transmit the RF signal through the skin, and (3) power regulator converts the received signal into DC voltage to supply the IMD. The power regulator consists of a rectifier circuit (active or passive) and a low-dropout regulator (LDO). In the reported CMOS ILPSs,[4–14] active rectifiers with power MOS devices, comparators, and offset control circuits are adopted to convert the AC power into DC power. Since the power MOS devices have the advantage of both turn ON and off delays, and the comparators are required

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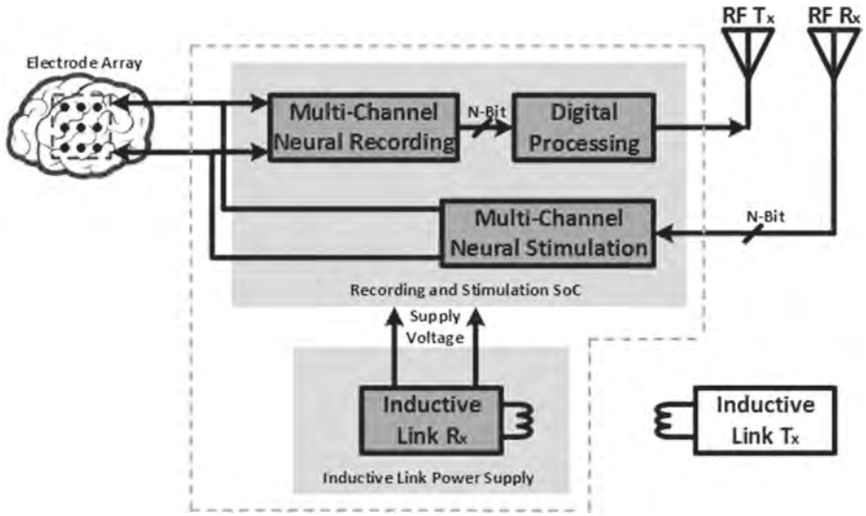


Fig. 1. Fully integrated implantable neural recording and stimulation SoC.

to control the switch timing accurately to obtain the proper forward current conduction and avoid the reverse current conduction. Thus, PCE of the converter is maximized. On the other hand, the need for energy harvesting is driven by the portable electronics market as well as the industrial and automotive applications. Moreover, there is a rising demand for most of the applications to have a low-voltage and low-power designs to maximize the lifetime of the battery.[15]

The rest of the paper is organized as follows. Through the second section, the system design, as well as the circuit implementation, are discussed. Moreover, in the third section, the circuit layout and simulation results are drawn. Finally, some conclusions are presented.

2. SYSTEM ARCHITECTURE AND CIRCUIT DESIGN

In this section, a 13.56 MHz CMOS near-field inductive link power supply (ILPS) for a fully integrated implantable neural recording and stimulation SoC, shown in Figure 2, is proposed with a low-power self-startup bandgap reference (BGR) circuit for biasing both the LDO circuit as well as the implantable neural SoC. The proposed ILPS is divided as follows: (1) active voltage doubler, (2) bandgap reference circuit, and (3) low-dropout voltage regulator.

2.1. Active Voltage Doubler

Initially, a fully integrated CMOS active voltage doubler (AVD) in 0.13 μm using offset-controlled high-speed

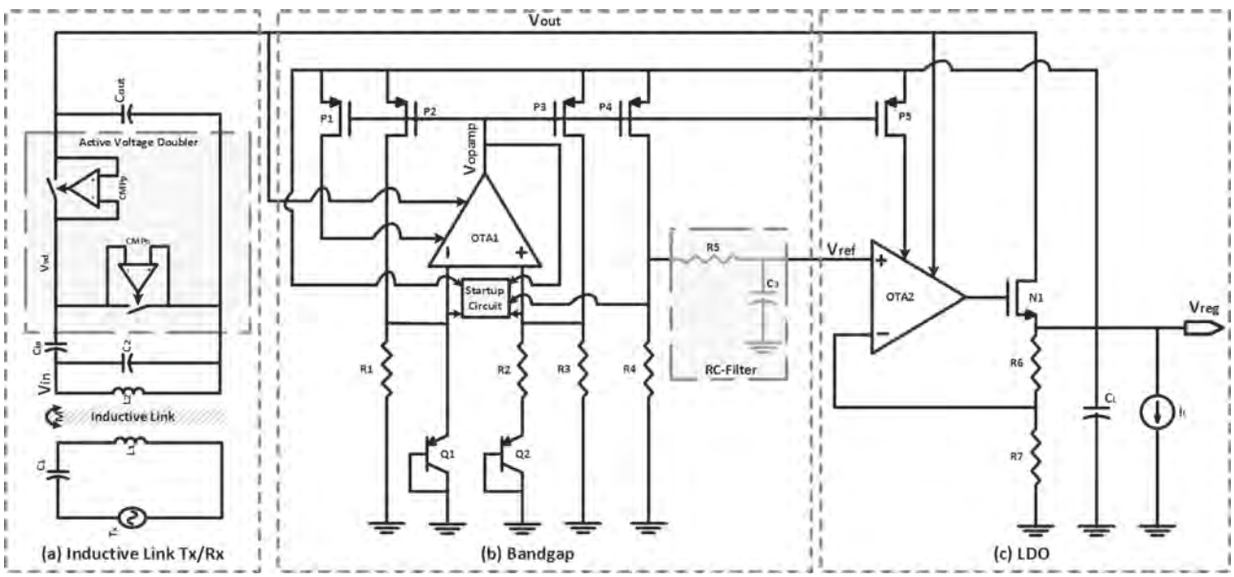


Fig. 2. Block diagram for the proposed near-field inductive link power supply for implantable neural recording and stimulation SoC.

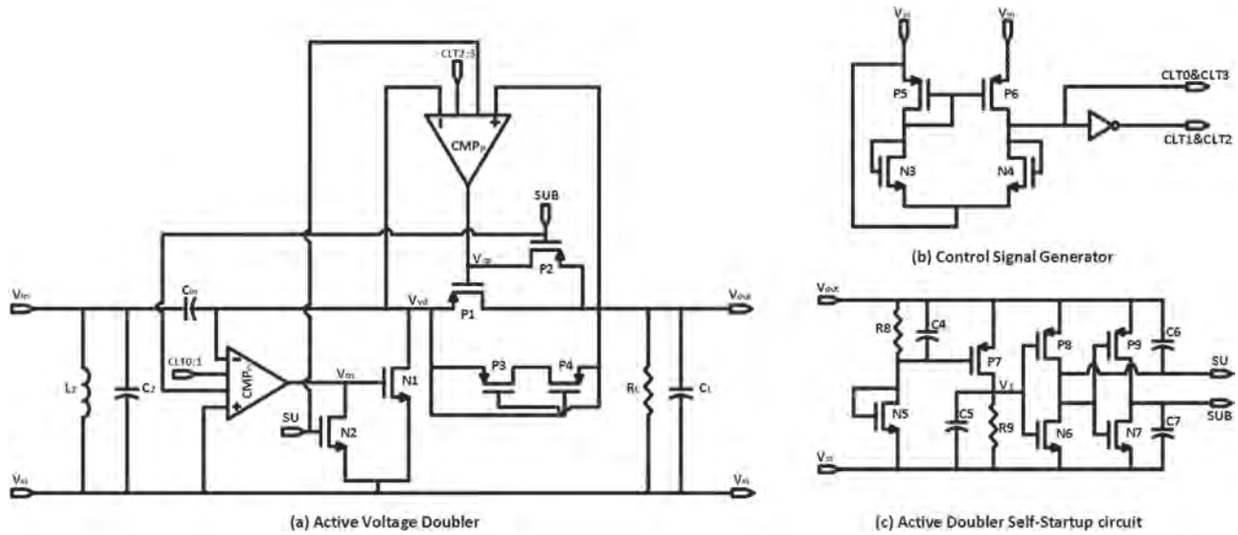


Fig. 3. Active voltage doubler circuit schematic.[4]

comparators for inductive power transmission is presented. This AVD improves PCE with a high load current and lower dropout voltage compared to the passive rectifiers, leading to a reliable and efficient operation with weakly coupled inductive links. Also, it is known that the input voltage range of a full-wave active rectifier has to be larger than its output DC voltage. However, the input voltage range of AVD is lower than that of a full-wave active rectifier, leading to a more reliable operation in the weakly coupled inductive link environment. Moreover, the offset-controlled functions in the comparators are implemented to compensate the turn ON and OFF delays which improve the PCE by maximizing the forward charging current to the load and minimizing the backward current.[14]

Figure 2(a) shows the block diagram of inductive link transmitter (Tx) and receiver (Rx) that consists of three main blocks: power Tx, an inductive link, and Rx (IMD). On the Tx side, the primary coil, L_1, is driven by a power amplifier (PA) at the carrier frequency, f_c. This signal induces power in the secondary coil, L_2, and the active voltage doubler converts the AC voltage in tank L_2C_2 to a DC voltage (V_{out}) at higher levels than the peak input voltage. Usually, both passive rectifiers and voltage doublers using diode-connected transistors suffer from large forward voltage drops and power losses because of their threshold voltages.[14]

Figure 3(a) shows a simplified schematic diagram of the proposed active voltage doubler, in which the pass transistor switches, N_1 and P_1, are driven by two symmetrical common gate high-speed comparators, CMP_N and CMP_P, respectively.[9] When $V_{\text{VD}} < V_{\text{SS}}$, CMP_N output goes high, the transistor N_1 turns on with a low dropout voltage, $V_{\text{DS(N1)}}$, and C_{IN} is charged to $V_{\text{IN, peak}} - V_{\text{DS(N1)}}$.[14] While $V_{\text{VD}} > V_{\text{out}}$, CMP_P output goes low, the transistor P_1 turns ON with a low dropout voltage, $V_{\text{SD(P1)}}$, and current flows through the transistor P_1 to charge R_LC_L. Therefore, after a few cycles, V_{out} is charged up to $2V_{\text{IN, peak}} - V_{\text{DS(N1)}} - V_{\text{SD(P1)}}$ and the total dropout voltage, $V_{\text{Drop}} = V_{\text{DS(N1)}} + V_{\text{SD(P1)}}$. Moreover, this happens due to the instantaneous input current flowing through the on-resistance of the transistors N_1 and P_1, will be much smaller than that of the passive voltage doubler.[14]

To drive N_1 and P_1 at a high frequency of 13.56 MHz, both CMP_N and CMP_P are equipped with the internal offset-control functions and four signals (CLT (0:3)) to reduce the effects of the comparators delay.[14] Additionally, an on-chip calibration comparator, shown in Figure 3(b), is proposed to generate these control signals by comparing V_{IN} with 0 V, where the signals CTL1 and CTL2 are connected to the comparator output and the signals CTL0 and CTL3 are connected to the inverted version of the comparator output. Thus, these built-in offset control functions allow the comparators to turn their pass transistors ON and OFF with a proper delay, leading to higher PCE.

For the startup circuit, shown in Figure 3(c), it generates the startup enable signals, SU and SUB, depending on the V_{out} level to control the startup switches N_2 and P_2, as well as the comparators.[14] When V_{out} is too low to power on the comparators, the startup circuit sets SU = HIGH and SUB = LOW, which turns ON the transistors N_2 and P_2, respectively, while disabling the comparators. In this condition, both transistors N_1 and P_1 are diode-connected to form a passive voltage doubler, which starts charging V_{out} regardless of the comparators status. When V_{out} exceeds a certain threshold that is sufficient to power on the comparators, SU and SUB toggle and turns OFF the transistors N_2 and P_2 while enabling the comparators to run the active voltage doubler normally. Moreover, the startup circuit reconfigures the doubler circuit as a diode-connected passive voltage doubler by generating SU and SUB signals based on V_{out}. When V_{out}

equals zero: the output of the comparators V_{CN} and V_{CP}, shown in Figure 3(a), equal zero, where the transistors N_1 and P_1 are diode-connected and conduct when $V_{VD} > V_{TH(P1)}$ and $V_{VD} < -V_{TH(N1)}$, respectively, then V_{OUT} starts to charge up. Moreover, the control signals, as well as the startup signals with the circuit operation status, are summarized in Table I. In addition, the startup circuit, shown in Figure 3(c) operates as follows: (1) $V_{OUT} < V_{TH(N5)} + V_{TH(P7)}$, the transistor P_7 stays OFF, and V_1 remains 0 V through R_2. SU and SUB follow V_{OUT} and V_{SS} making the transistors N_1 and P_1 act as diode-connected transistors and (2) $V_{OUT} > V_{TH(N5)} + V_{TH(P7)}$, the transistor N_5 turns ON creating sufficient voltage across R_1 to turn ON the transistor P_7 and pull V_1 up. This, SU and SUB become V_{SS} and V_{OUT}, respectively, turning OFF the transistors N_2 and P_2 releasing the comparator outputs, and allowing the transistors N_1 and P_1 operate as switches.[14]

2.2. Bandgap Reference Circuit

Figure 2(b) displays a modified low-power BGR circuit presented in Ref. [16] with a dual supply voltage. The implemented operational amplifier (opamp) is supplied by 3.38 V from AVD, while the rest of BGR core is powered on by 1.2 V from LDO circuit. And the output voltage V_{ref} is the sum of the base-emitter voltage (V_{BE}), and the thermal voltage (V_{TH}) multiplied by a constant ΔV_{BE}. To get a zero-temperature coefficient (TC), V_{ref} is in order of 1.1 V, which is not suitable for low-voltage applications. The BGR circuit[16] adds controlled output currents that are proportional to V_{BE}, and ΔV_{BE}. Thus, this produces V_{ref} with the required value. This circuit operates at low-voltage supply that is given by $V_{SD} + V_{BE}$. Moreover, the implemented opamp in Ref. [16] is self-biased through the BGR circuit. Also, it is connected a high-voltage supply to sustain a high-power supply rejection ratio (PSRR). Also, a low pass RC filter is added at the output of the bandgap circuit to increase the PSRR.[16] Since the AVD ripples have high-frequency components, so the low pass filter keeps only low-frequency ripples reducing V_{ref} variation with the power supply ripples.[16]

Table I. Active voltage doubler control signals.

	Status	
Control signals	High	Low
CLT0	No change	Delay Turn OFF of N1
CLT1	No change	Speed up Turn OFF of N1
CLT2	Delay Turn OFF of P1	No change
CLT3	Speed up Turn OFF of P1	No change
SU	CMPp → OFF and N1 → Act as diode	CMPp → ON and N1 → Act as Pass Tr
SUB	CMPn → ON and N2 → Act as Pass Tr	CMPn → OFF and N2 → Act as diode

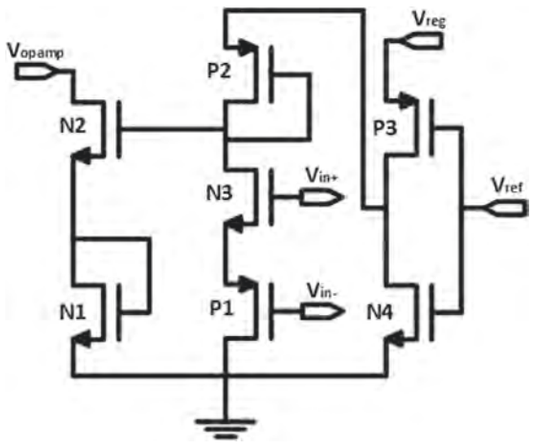


Fig. 4. BGR startup circuit schematic.

Figure 4 shows a zero-power startup circuit proposed in Ref. [16]. The proposed idea depends on adding a switch between the source of transistor N3 and the ground to turn N3 OFF when V_{in+} reaches its normal value. The source of P2 needs to be connected to a low voltage after the startup to turn the transistors N1 and N2 OFF. To achieve this, the output of an inverter, formed by the transistors P3 and N4, is connected to the source of transistor P2, instead of V_{DD}, where the inverter input is connected to V_{ref}. When V_{ref} is low, the inverter output is a high voltage that is converted to the gate of the transistor N2 through V_{SG} of transistor P2 turning it on and injecting current to the circuit. After the circuit starts, the inverter is OFF, and the transistors P2, P1, and N3 are switched OFF too. While V_{ref} at logic high, then the inverter output is low. Since there are no current flows through the transistor P2, and V_{SG4} equals zero, the output of the inverter is transmitted to the gate of transistor N2 turning the transistors N2 and N1 OFF. The cascoded transistors N1 and N2 are used to make sure that they are turned OFF completely after the circuit starts.

2.3. Low-Dropout Regulator

Figure 2(c) displays a conventional linear LDO circuit with a feedback loop that senses the output voltage (V_{reg}), then compares a ratio value of V_{reg} to the V_{ref} until reaching the required value within a specific tolerance due to the error amplifier (EA) regardless of its operating conditions. The relation between V_{reg} and V_{ref} is controlled by the following equation:

$$V_{reg} = \left(1 + \frac{R_6}{R_7}\right) V_{ref} \quad (1)$$

Where R_6 and R_7 denote the feedback sensing resistors. Also, these resistors control the quiescent current through the output branch. On the other hand, the NMOS pass transistor (N1) controls the maximum current for LDO to source the load.[22] The NMOS LDO is utilized since it has a higher mobility with less implementation area, as

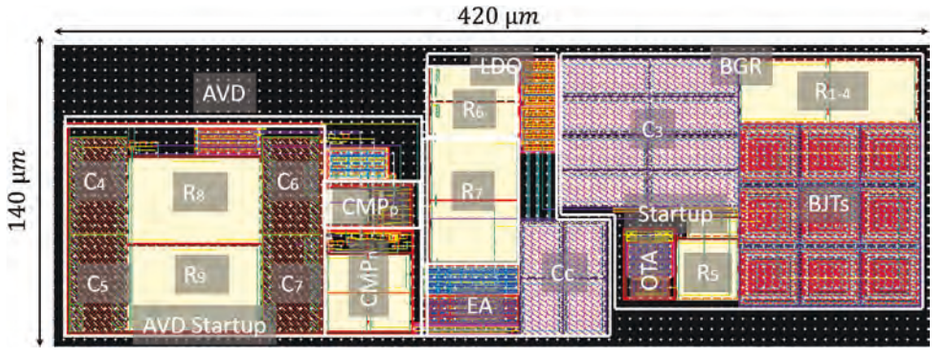


Fig. 5. Chip layout for the proposed near-field ILPS in 0.13 μm technology.

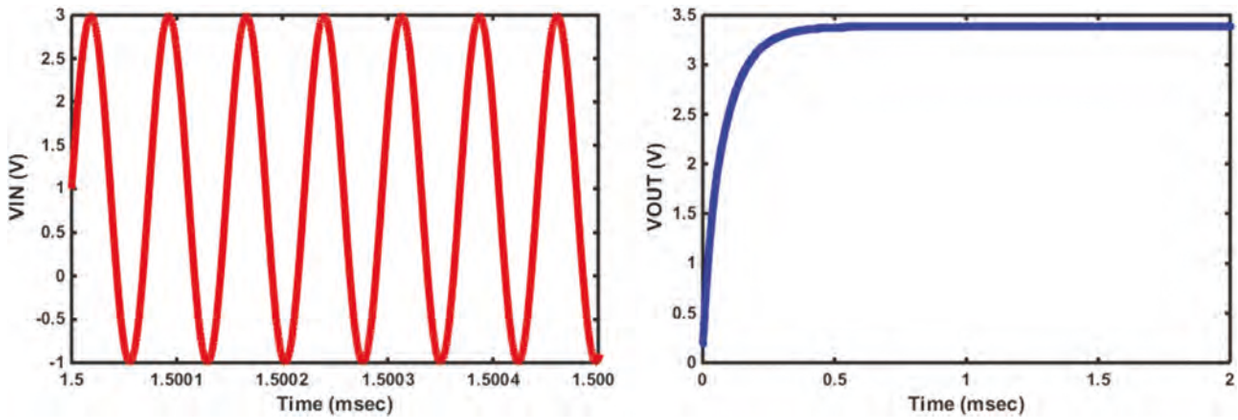


Fig. 6. AVD both input and output voltage waveforms with $R_L = 0.5$ KΩ, $C_{IN} = C_{OUT} = 1$ μF, $V_{IN,\,peak} = 2$ V, and $f_c = 13.56$ MHz.

well as higher intrinsic load regulation characteristics due to the low output impedance. Thus, it improves the load regulation.[22]

3. CHIP LAYOUT AND SIMULATION RESULTS

A prototype of the proposed ILPS is implemented through UMC 0.13 μm technology. The circuit layout is shown in Figure 5 with an overall area of 0.06 mm^2. Also, the main design blocks are highlighted, starting from AVD on the left followed by LDO, then BGR circuit. Finally, the prototype is tested and verified using Cadence Virtuoso.

Figure 6 displays the simulated input and output waveforms of the AVD using $R_L = 160$ Ω, $C_{IN} = C_L = 1$ μF, $V_{IN,\,peak} = 2$ V, and $f_c = 13.56$ MHz. In addition, the PCE is calculated as follows:[14]

$$\mathrm{PCE} = \frac{P_{\mathrm{Load}}}{P_{\mathrm{IN}}} = \frac{P_{\mathrm{Load}}}{P_{\mathrm{Load}} + P_{\mathrm{CMP}} + P_{\mathrm{Tr,\,sw}} + P_{\mathrm{Tr,\,Ron}}} = 75\% \quad (2)$$

Where P_{Load} denotes the power consumption by the load and P_{CMP} denotes the power dissipation by the comparators excluding the power needed to drive the gates of the transistors P1 and N1.[14] $P_{\mathrm{Tr,\,sw}}$ and $P_{\mathrm{Tr,\,Ron}}$ are the power losses in the pass transistors due to gate switching and dissipation in R_{ON}, respectively.[14] Moreover, Figure 7 shows the key node waveforms of the AVD, showing V_{VD}, V_{CP}, V_{CN}, and CLT (0:3), respectively.

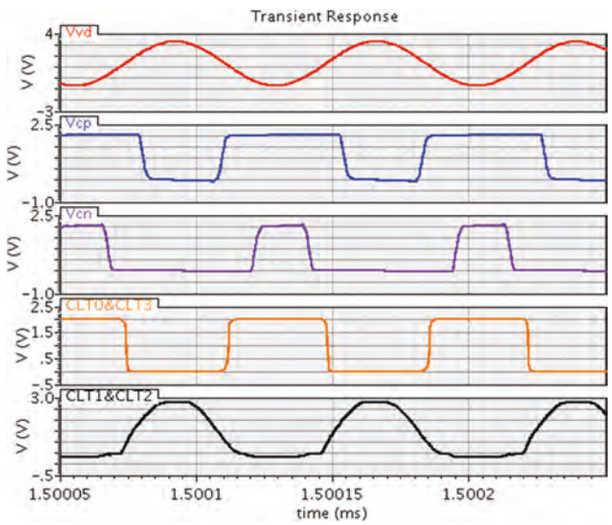


Fig. 7. Control signals of the proposed on-chip calibration circuit for the implemented AVD with achieving the maximum power efficiency.

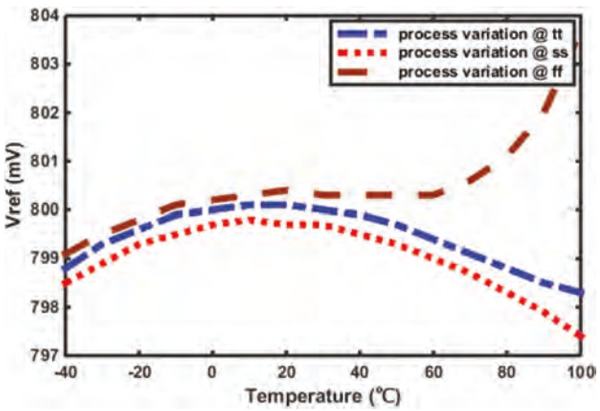
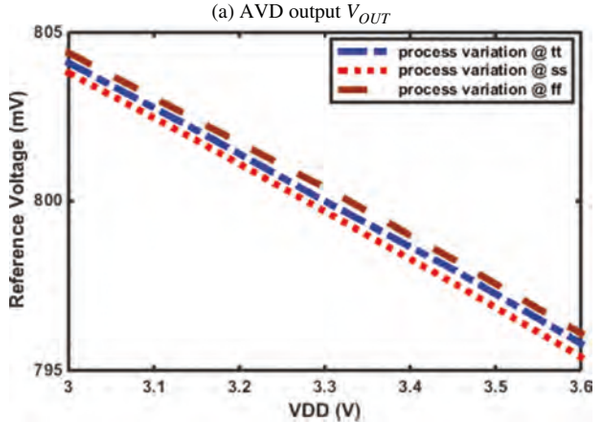


Fig. 8. V_{ref} of the proposed BGR across temperature and process variations.

Figure 8 shows V_{ref} generated by the modified low-power dual-supply BGR circuit across a wide range of temperature variations from −40 °C to 100 °C with varying the technology process, where the maximum temperature variation equals 0.4%. While in Figure 9(a), the V_{ref} variation is shown with sweeping the AVD output supply voltage from 3 to 3.6 V where the maximum change equals 0.3%. In addition, in Figure 9(b) is shown with sweeping the LDO regulated supply voltage from 1.1 to 1.3 V where the maximum deviation equals 0.25%.

(a) AVD output V_{OUT}



(b) LDO output V_{reg}

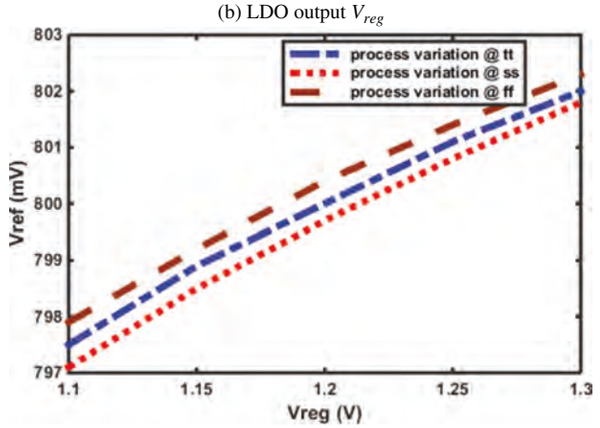


Fig. 9. V_{ref} of the proposed BGR across supply and process variations. (a) Variations due to high V_{OUT}. (b) Variations due to low V_{reg}.

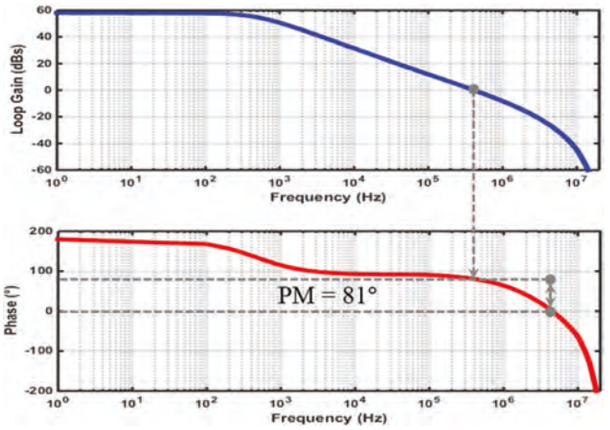


Fig. 10. The proposed BGR stability analysis by calculating both gain margin and phase margin.

The stability test for the modified low-power dual-supply BGR circuit, shown in Figure 10, where the phase margin is designed to be 81° to ensure that there are no hidden oscillations, and to achieve proper settling time. Moreover, the output PSRR with varying the technology process is shown in Figure 11. In addition, the PSRR is calculated through simulations and equals −67.5 dB at 1 KHz. This degradation in PSRR from Ref. [16] is due to using a dual supply for the BGR circuit powering. Finally, the supply ramp up test, shown in Figure 12, is done to measure the settling time of the proposed dual-supply BGR circuit. The supply is ramped from 0 to maximum

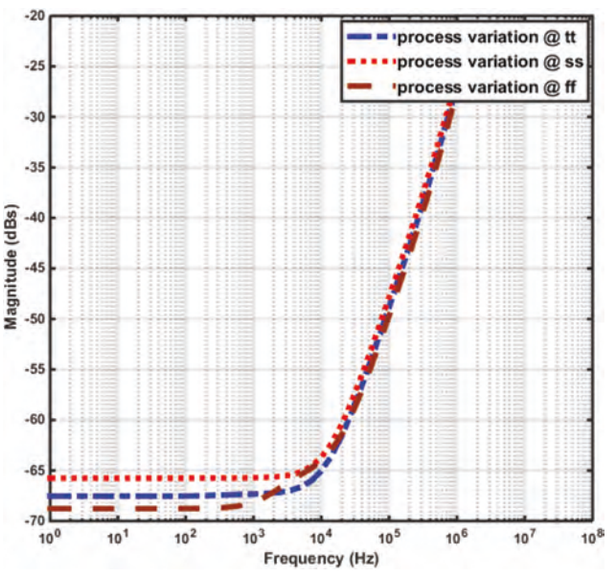


Fig. 11. PSRR of the proposed BGR across process variations.

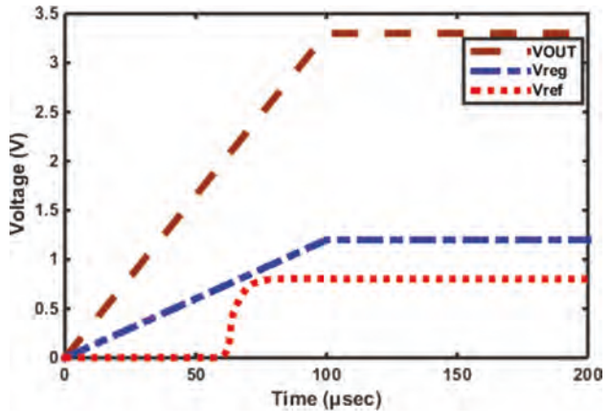


Fig. 12. V_{DD} ramp-up test of the proposed BGR.

and reaches V_{DD} after 100 μsec where V_{ref} reaches its steady-state value after 60 μsec.

For a low-power conventional LDO circuit: Figure 13 shows V_{reg} across the load current variation from 1 mA till 20 mA, where the maximum deviation of the output voltage equals 0.14%. While in Figure 14(a), the V_{reg} variation is shown across the technology process variation with sweeping the supply voltage from 3 V till 3.6 V at minimum load current where the maximum variation equals 0.175%. In addition, in Figure 14(b) shows the V_{reg} variation across the technology process variation with sweeping the supply voltage from 3 V till 3.6 V at maximum load current where the maximum change in the output voltage equals 0.14%.

The stability test for the low-power conventional LDO circuit, shown in Figure 15, where the phase margin is designed to be 65° to ensure that there are no hidden oscillations, and to achieve proper settling time. Moreover, the output PSRR with varying the technology process is shown in Figure 16. Also, the PSRR is calculated through simulations and equals −53 dB at 1 KHz. Finally, both the

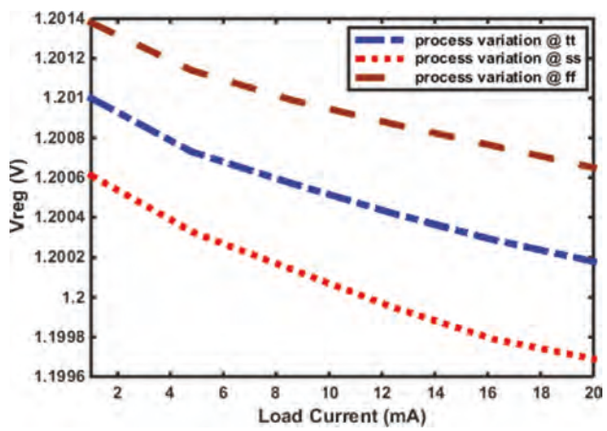


Fig. 13. V_{reg} of the implemented LDO across load current and process variations.

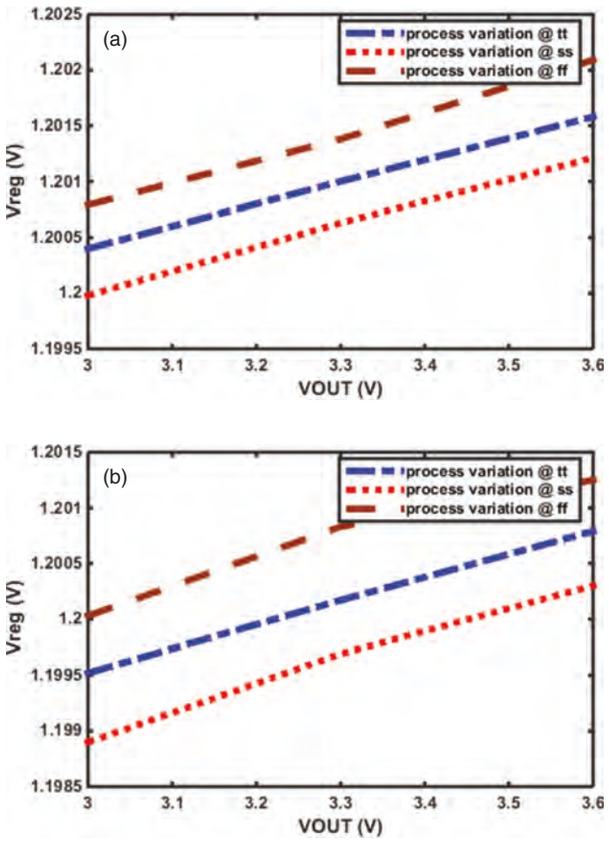


Fig. 14. V_{reg} of the implemented LDO across supply and process variations. (a) Minimum load current. (b) Maximum load current.

load regulation and line regulation are calculated using the following equations:

$$\text{Load regulation} = \frac{\Delta V_{reg}}{\Delta I_{load}} \tag{3}$$

$$\text{Line regulation} = \frac{\Delta V_{reg}}{\Delta V_{in}} \tag{4}$$

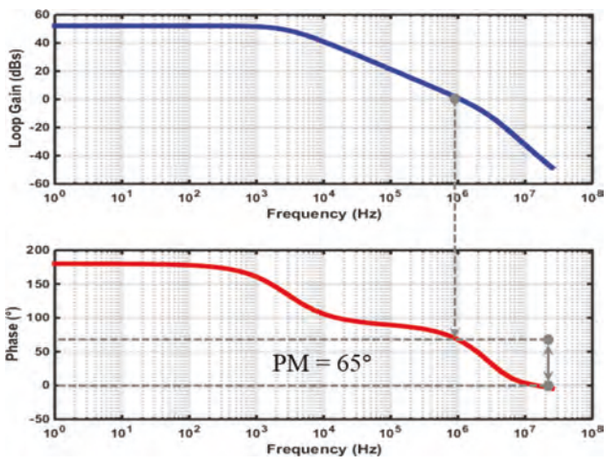


Fig. 15. The implemented LDO stability analysis by calculating both gain margin and phase margin.

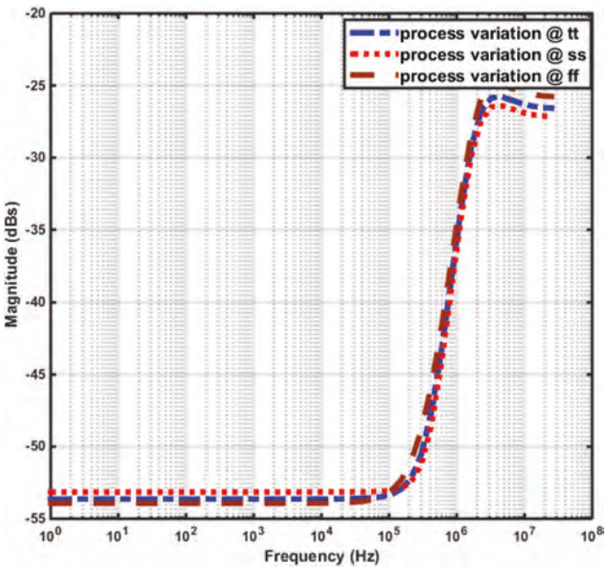


Fig. 16. PSRR of the implemented LDO across process variations.

Where ΔV_{reg} denotes the difference in the output regulated voltage from the nominal value, ΔI_{load} denotes the range of the output load current, and ΔV_{in} denotes the range of the input supply voltage from AVD circuit. Finally, the load transient regulation, shown in Figure 17, is tested for a full load (1 mA–20 mA with 50 ns rise and fall times). The implemented LDO is completely recovered within 400 ns with voltage spikes 260 mV for the undershoot and 295 mV for the overshoot.

Figure 18 portrays the output voltages at the input and output nodes of each block where all the nodes are precharged until the output became stable. The proposed BGR circuit stabilized in less than 3 μs with the LDO circuit. Moreover, the AVD output reaches the steady state after 20 μs since the output capacitor (C_{out}) is already precharged with 3.4 V.

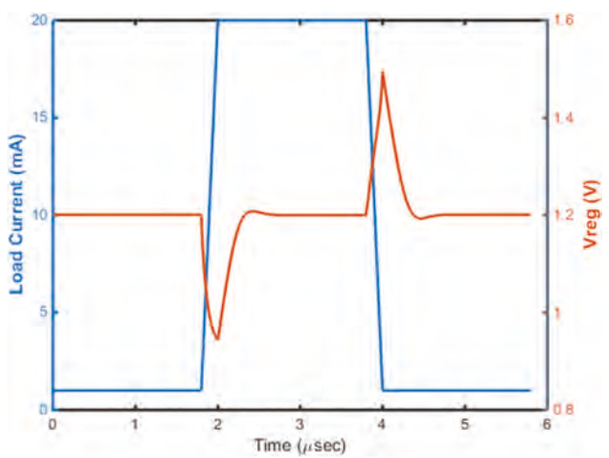


Fig. 17. Load transient regulation of the implemented LDO across the load range from 1 mA till 20 mA.

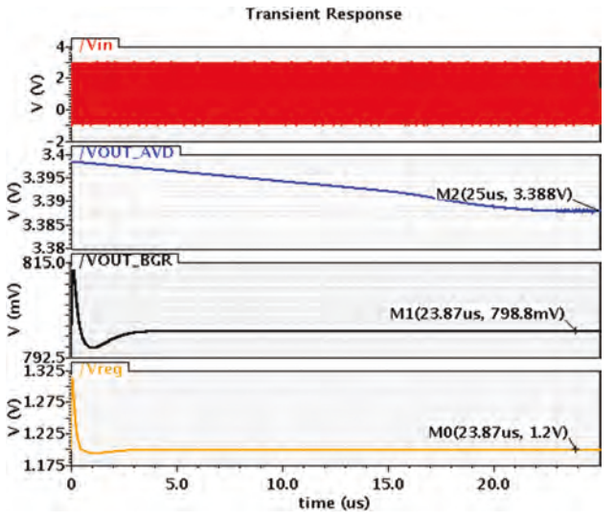


Fig. 18. Transient simulation of the whole loop of the ILPS.

Finally, Table II shows a detailed performance summary of this work and the recently published power converters in Refs. [11–14]. The AVD circuit is optimized on the gate level by setting a more accurate aspect ratio to achieve a lower power consumption with on-chip calibration provides good results compared to other work in the literature. It is obvious from Table II that the load current of the proposed AVD circuit is higher than that in Refs. [11–14] by factors of 3.38X, 3.4X, 8.8X, and 1.1X, respectively. Moreover, Table III shows a detailed performance summary of this work and the recently published BGR circuits in Refs. [17–21]. The modified low-power dual-supply BGR circuit provides good results compared to other work in the literature. It is observable from Table III that the power consumption of the proposed BGR circuit is lower than that in Refs. [16–20] by factors of 2.3X, 3.18X, 5.3X, 1.9X, and 6.18X, and 1.17X, respectively. The low power consumption is the main objective of the proposed bandgap circuit to be suitable for IMDs. Although the proposed BGR circuit achieves significant power reduction, this comes at the expense of higher temperature coefficient compared to that in Refs. [16–20]. Finally, Table IV shows a detailed performance summary of this work and the

Table II. Active voltage doubler performance summary versus the state-of-the-art power converters.

Ref.	[12]	[13]	[14]	[11]	This work
Tech (μm)	0.5	0.5	0.5	0.18	0.13
$V_{IN,\,Peak}$ (V)	3.8	2.2	1.46	1.192	2
F_{IN} (MHz)	13.56	13.56	13.56	13.56	13.56
V_{OUT} (V)	3.12	3.1	2.4	2	3.38
I_L (mA)	6.24	6.2	2.4	20	21.125
PCE	80.2% @500 Ω	70% @500 Ω	80% @1 KΩ	85% @100 Ω	77% @160 Ω 82%@LDO with 20 mA

Table III. BGR circuit performance summary versus the state-of-the-art BGR circuits.

Ref.	[17]	[18]	[19]	[20]	[21]	[16]	This work
Tech (μm)	0.18	0.13	0.13	0.13	0.045	0.13	0.13 μm
V_{DD} (V)	1.2	1.2	1	1.2	0.8	3.3	1.2/3.4
P_{diss} (μW)	43.2	72	26	84	16	31.3	13.6
V_{ref} (V)	0.767	0.602	0.798	0.85	0.475	0.8	0.8
Temp range (°C)	$-40 \rightarrow 120$	$0 \rightarrow 100$	$-50 \rightarrow 160$	$-25 \rightarrow 85$	$-40 \rightarrow 125$	$-40 \rightarrow 85$	$-40 \rightarrow 100$
Temp coeff (ppm/°C)	4.5	2.2	6.64	11	31	20	22
PSRR @ 1 KHz	−80 dB	−58 dB	N/A	−71 dB	−70 dB	−76 dB	−67.5 dB

Table IV. LDO performance summary versus the state-of-the-art LDOs.

Ref.	[23]	[24]	[25]	[26]	This work
Tech (μm)	0.35	0.35	0.35	0.18	0.13
V_{IN} (V)	3	2.5–4	3.7	1.84–3.6	3–3.6
I_Q (μA)	65	7	26	7	6.5
V_{reg} (V)	2.8	2.35	3.25	1.8	1.2
I_L (mA)	50	100	50	50	1–20
C_L (pF)	100	100	100	100	1
Line regulation @ max I_L (mV/V)	∼23	1	N/A	0.00647	2.1
Load regulation (mV/mA)	∼0.56	0.08	∼2.86	0.0024	0.046
PSRR @ 1 KHz	−57 dB	N/A	−40 dB	−53 dB	−53 dB

recently published LDOs in Refs. [23–26]. The conventional LDO is optimized on gate level through setting a more accurate aspect ratio with self-biased through BGR circuit for low-power consumption provides good results compared to other work in the literature. It is cleared from Table IV that the quiescent current (I_Q) of the optimized LDO is lower than that in Refs. [23–26] by factors of 10X, 1.08X, 4X, and 1.08X, respectively.

4. CONCLUSION

In this paper, a low-power high-efficiency CMOS ILPS has been described. The proposed ILPS is easily calibrated through an on-chip comparator for timing control with a self-startup AVD circuit and zero-power self-startup BGR circuit. In addition, a low-power LDO circuit is presented to generate the required DC voltage for the neural recording and stimulation SoC supply. The proposed ILPS harvests 24 mW with 82% PCE and occupies 0.06 mm^2. Also, it utilizes a modified low-power dual-supply BGR circuit for biasing both the ILPS circuits and the overall implantable neural recording and stimulation SoC. Finally, this ILPS is well suited for intractable diseases or disorders, especially neurological types, as it consumes a low quiescent current.

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