Suez Canal University

Faculty of Engineering
Electrical Engineering Department

Performance Enhancement of Emerging Memory Technologies Using Memristor–Based Structures

A Thesis Submitted to the Faculty of Engineering, Suez Canal University in Partial Fulfillment of the Requirements for the

Doctor of Philosophy Degree in
Electrical Engineering

BY

Sherief Fathy Ibrahim Kamel Abou Nafea

M. Sc. in Electrical Engineering 2012 Faculty of Engineering – Port Said University
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English Abstract

Until 1971, the known three fundamental electrical elements were resistor, inductor, and capacitor. In 1971, Professor Leon Chua proposed that there should be a fourth fundamental element to complete the missing link between electric charge and magnetic flux. This element has been denoted by “Memristor." Memristor is a two-terminal passive element whose resistance varies based on the historic profile of the applied voltage/current. The first realization of this element was by HP labs in 2008. After that, a wide area of research on the memristor and its possible applications is opened. The thesis gives an overview of the memristor’s properties, types, and modeling approaches with a special focus on the spintronic memristor type. Then a brief survey on the applications such as memory and neural circuits is provided.

One interesting type of memristors is the spintronic memristor which is based on the spin-transfer torque (STT) effect of magnetic devices. The spintronic memristor combines the advantages of memristors such as the non-volatility and the advantages of spin-transfer torque magnetic devices such as the good scalability and the radiation hardness. Spintronic memristors are promising devices that can be used efficiently in various applications such as memory chips and neuromorphic systems. They can benefit from the maturity of integrating magnetic devices on top of CMOS devices. Thus, the spintronic memristor is a promising candidate for a new generation of universal memory circuits.

In this thesis, two spintronic memristor models are proposed. The first one is a thermal fluctuation aware (TFA) model which accounts for the effect of the temperature variations on the spintronic memristors and studies the read disturbance due to these thermal variations. The model

is useful for the analysis and design of memristive-based memory circuits and it keeps the simplicity of existing models.

The second spintronic memristor model has a higher accuracy, more generality, but also more complicity. Existing models of spintronic memristors represent a similar version of the linear ion drift model of resistive memristors, which offer simplified models, with lower accuracy and without enough linkage to the device's physical parameters. The proposed model provides a general spintronic memristor model in which its dynamical behavior is represented by the Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation. The proposed model provides a more accurate dynamical behavior by using the LLGS equation, and better link to the device's physical parameters. It also gives the required equations to cover different types and geometries of spintronic memristors. The effect of the thermal variations on the memristor's parameters is also included in the model. The model is verified to experimental data and shows a significant enhancement in fitting compared to existing models. For both models, Verilog-A codes are developed and integrated with an integrated circuit CAD tool.

Then, the thesis provides a mathematical analysis of the dynamical behavior of spintronic memristors and their memory circuits using the TFA model. From the mathematical analyses, some useful equations are deduced that can be used in the design of memristor-based memory circuits.

After that, a read/write circuit for spintronic memristor-based memories is proposed. The proposed read/write circuit achieves a significant reduction in the occupied area. The read disturbance of the circuit is investigated to calculate the maximum allowed number of reading cycles before a refreshment operation is needed, and it is compared to some well-known existing read/write circuits.

Finally, the thesis provides a brief comparison between different memristor types for different applications. The comparison helps to recognize the advantages and disadvantages of each memristor type in these applications, which helps in deciding which memristor type can be more efficient in each application.

Key Words	Memristor – Modeling - Spintronic Memristor - Read Disturbance - LLGS Equation - Tunneling Magnetoresistance - Temperature Variations - Verilog-A - MRAM - Nonvolatile Memories – Dynamical Analysis – Read/Write Circuits.

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ABSTRACT

Until 1971, the known three fundamental electrical elements were resistor, inductor, and capacitor. In 1971, Professor Leon Chua proposed that there should be a fourth fundamental element to complete the missing link between electric charge and magnetic flux. This element has been denoted by “Memristor." Memristor is a two-terminal passive element whose resistance varies based on the historic profile of the applied voltage/current. The first realization of this element was by HP labs in 2008. After that, a wide area of research on the memristor and its possible applications is opened. The thesis gives an overview of the memristor properties, types, and modeling approaches with a special focus on the spintronic memristor type. Then a brief survey on the applications such as memory and neural circuits is provided.

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KEYWORDS

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LIST OF PUBLICATIONS

1. S. F. Nafea, A. A. Dessouki, and S. El-Rabaie, "Memristor Overview up to 2015," Menoufia Journal of Electronic Engineering Research (MJEER), Vol.24, No. 1&2, Jan-July 2015.
2. S. F. Nafea, A. A. Dessouki, S. El-Rabaie, K. El-Barbary, and H. Mostafa, "Read disturbance and temperature variation aware spintronic memristor model," in Electrical and Computer Engineering (CCECE), 2016 IEEE Canadian Conference on, 2016, pp. 1-4.
3. S. F. Nafea, A. A. Dessouki, S. El-Rabaie, Basem E. Elnaghi, Yehea Ismail, and H. Mostafa, "Area-Efficient Read/Write Circuit for Spintronic Memristor Based Memories", 60th IEEE International Midwest Symposium on Circuits and Systems, 2017.
4. S. F. Nafea, A. A. Dessouki, S. El-Rabaie, Basem E. Elnaghi, Yehea Ismail, and H. Mostafa, "Accurate LLGS-Based Spintronic Memristor Model". *Submitted to Microelectronics Journal (MEJ), Elsevier "Under Reviewing"*.

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LIST OF SYMBOLS AND ABBREVIATIONS

List of Abbreviations

1D1M	One **D**iode one **M**emristor
1T1M	One **T**ransistor one **M**emristor
AGC	Automatic Gain Control
CAD	**C**omputer **A**ided **D**esign
CAM	**C**ontent **A**ddressable **M**emory
CF	**C**onductive **F**ilament
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
DRAM	**D**ynamic **R**andom **A**ccess **M**emory
EIRP	**E**lectric **P**ulse **I**nduced **R**esistance switching
FeRAM	**F**erroelectric **R**andom **A**ccess **M**emory
FL	**F**ree **L**ayer
FPGA	**F**ield **P**rogrammable **G**ate **A**rray
FTJ	**F**erroelectric **T**unneling **J**unction
HRS	**H**igh **R**esistive **S**tate
IPA	**I**n **P**lane **A**nisotropy
LRS	**L**ow **R**esistive **S**tate
LLG	**L**andau **L**ifshitz **G**ilbert
LLGS	**L**andau **L**ifshitz **G**ilbert **S**lonczewski
MCAM	Memristor-based Content Addressable Memories
MIM	**M**etal **I**nsulator **M**etal
MRAM	**M**agnetoresistive **R**andom **A**ccess **M**emory
MTJ	**M**agnetic **T**unneling **J**unction
PANI	**P**oly**ani**line
PCRAM	**P**hase **C**hange **R**andom **A**ccess **M**emory
PEO	**P**oly**e**thylene **O**xide
PPA	**P**erpendicular **P**lane **A**nisotropy
PL	**P**inned **L**ayer

redox	**red**uction–**ox**idation reaction
RFID	**R**adio-**F**requency **Id**entification
RRAM	**R**esistive **R**andom **A**ccess **M**emory
RTD	**R**esonant **T**unneling **D**iode
SPICE	**S**imulation **P**rogram with **I**ntegrated Circuit **E**mphasis
SRAM	**S**tatic **R**andom **A**ccess **M**emory
STT	**S**pin **T**ransfer **T**orque
TEAM	**T**hr**E**shold **A**daptive **M**emristor Model
TMR	**T**unneling **M**agneto **R**esistance
TFA	**T**hermal-**F**luctuation **A**ware model

List of Symbols

Q	Electric Charge
Φ	Magnetic Flux
R	Resistance
L	Inductance
C	Capacitance
M	Memristance
W	Memductance
I	Current
V	Voltage
W	State Variable position
X	Normalized State Variable position
R_H	Memristor OFF state resistance
R_L	Memristor ON state resistance
J_{cr}	Critical Current Density
J_{eff}	Effective Current Density
R_{DW}	Domain Wall Resistance
P_S	Polarization efficiency
μ_V	Mobility of Oxygen Vacancies
A_{ex}	Exchange parameter
α_g	Gilbert damping parameter
R_P	Parallel resistance of spintronic memristor
R_{AP}	Antiparallel resistance of spintronic memristor
r_L	Resistance per unit length at the low-resistance state
r_H	Resistance per unit length at the high-resistance state
M_S	Saturation Magnetization
Δ	Thermal Stability Factor

$\boldsymbol{M}$	Magnetization Vector
sv	State Variable Position in LLGS-based Memristor model
H_K	Anisotropy field
Γ_v	Domain wall velocity coefficient
η	spin torque efficiency
τ_0	The nominal switching time of spintronic memristor when a current I_{cr} is applied to it.
$\tau_{P\text{-}AP}$	The Neel-Brown relaxation time

Chapter 1: Introduction

The CMOS technology has been the dominant semiconductor integrated circuit technology over the past three decades. However, the continuous CMOS scaling down suffers increasing technological difficulties. Moreover, getting closer to the atomic dimension led to increasing the quantum effect and other second-order effects on the device performance. For example, in the deep submicron, the power consumption due to the subthreshold and gate leakages became a real bottleneck. Thus, many alternative technologies are being investigated in order to replace CMOS technology or to be integrated with it. Among the emerging technologies, memristor-based technologies are very promising ones.

The memristor is a fundamental two terminal device relates the magnetic flux φ with the electric charge q. With its inherent nonvolatile property and its dependence on the historic profile of current/voltage, the memristor offered a strong candidate for many applications. The memristor-based memory and neuromorphic circuits are considered the most important applications that greatly benefit from memristive properties. This thesis proposes two different models of a memristor type called “spintronic memristors”, and investigates memristor-based memory design.

1.1. Problem Statement

The memristor devices with their different types are still immature technologies that need more investigation in device characterization and modeling. Accurate modeling is a crucial part of the memristor-based circuits design. Providing accurate modeling helps in gaining a better understanding of the circuit design and the design trade-offs. Besides,

linking the model of the memristor to its physical parameters helps to estimate the impact of changes in these parameters on the memristor-based circuits. In addition, accurate modeling provides results closer to the real device behavior and shows the limitations of the technology that must be considered during the circuit design.

Memristor-based memories also require investigating the basic-cell design and read/write circuits in order to find the best tradeoffs between higher storage densities, larger noise margins, and higher performance. Proposing different cell designs and read/write circuits help the designer to compare between these designs and choose the best design that suits the design constraints.

1.2. Thesis Objectives

The main objectives of this thesis are to:

- Review the types and the models of memristors and compare existing memristor models to investigate their advantages and disadvantages.
- Survey the applications of the memristor with a special focus on memristor-based memory design.
- Proposing two different spintronic memristor models that overcome some limitations and disadvantages of existing memristor models.
- Provide a mathematical analysis of the dynamical behavior of memristors and the memory design using the proposed thermal fluctuation aware memristor model. This analysis can be effectively used to compromise between different memory design tradeoffs and understanding the design limitations.

- Proposes a read/write circuit that achieves a significant reduction in the circuit area. Compares different read/write circuits and provides design insights that may effectively help in the design of memristive-based memories.
- Compares memristor types for some well-known memristor applications. This comparison can be used in deciding which memristor type is more suitable for each application.

1.3. Thesis Outline

The organization of this thesis is outlined as follows:

Chapter One presents the introduction and the scope of the thesis.

Chapter Two gives an overview of the types and the models of the memristors. The models are reviewed and compared to define points on strengths and weaknesses.

Chapter Three introduces different applications of memristors with a special focus on memristor-based memory design.

Chapter Four introduces two alternative spintronic memristor models. The first model is a thermal fluctuation aware model. The second model is a more accurate more complicated model that links the spintronic memristor model to its physical parameters. The model represents the dynamical behavior of the spintronic memristor using the LLGS equation.

Chapter Five introduces an analysis of the dynamical behavior of memristors and memristor-based memory design. The thermal fluctuation aware model that is provided in chapter 4 is used in this analysis. A read/write circuit with a significant area reduction is proposed. The circuit theory of operation is investigated. The circuit is also compared with two existing well-known read/write circuits of memristive-based memories.

Chapter Six provides a comparison between the performance of different memristor types for some memristor-based applications.

Chapter Seven provides the conclusions of the thesis and gives the suggestions for future work.

Finally, the appendices and the list of references are provided.

Chapter 2: Literature Review of Memristor Types and Modeling

2.1. Introduction

Memristive devices were defined by Professor Leon Chua as devices that have hysteresis zero-crossing current-voltage characteristics [1]. The hysteretic effect decreases when the frequency increases, until reaching a purely resistive system. From this definition, we can conclude that any possible fabrication of a two terminal device that achieves zero-crossing hysteresis current-voltage characteristics represents a memristor. Through this chapter, memristor types from the point of view of the material used in fabrication are discussed. Then, well-known models -up to the author's knowledge- are discussed and compared. Separate sections for the resistive and the spintronic memristors modeling are provided. It should be noted that resistive memristors' models are usually used as general memristor models for different memristor types, but with empirical values that are not linked to physical parameters of these devices.

As shown in Figure 2.1, the memristor is a two-terminal device element that directly relates electric charge (q) with magnetic flux (Φ) [1]. The memristor's parameter is the *memristance* (M) and it is measured in ohms. As the current is the time integration of the electric charge and the voltage is the time integration of the magnetic flux, the memristance value changes depending on the historic profile of the applied voltage on the memristor terminal and the historic profile of the current passed through it. That is why the element is denoted as a memristor, which is a short of *"memory-resistor"*.

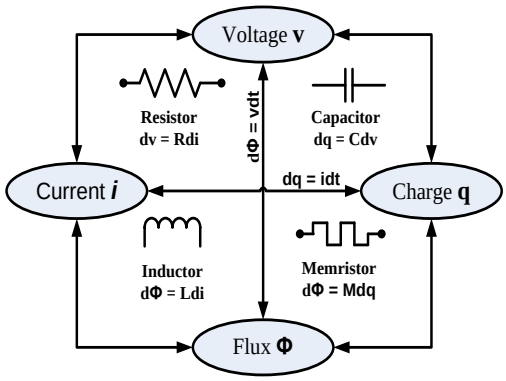


Figure 2.1 Fundamental Electrical Elements Relationships

In 2008, the members of an HP Labs announced a successful realization of a two terminal element that achieves the characterization of the memristor [2]. The HP memristor is a solid-state two terminal device formed of a nanometer scale titanium dioxide (TiO_2) thin film sandwiched between two metal electrodes as shown in Figure 2.2. The device achieved the main memristor properties according to Prof. Chua definition.

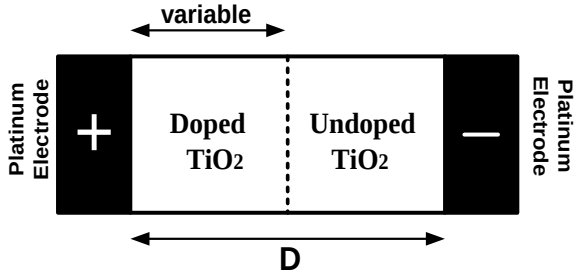


Figure 2.2 HP TiO2 Memristor

After the HP announcement, memristors gained a wide research interest for both modeling and applications. In the field of modeling, many models such as linear and nonlinear ion drift models were proposed. Some models

were implemented using SPICE such as Biolek model [3], and others were implemented using Verilog-A such as TEAM model [4].

Besides the HP memristor, many devices have been submitted as physical realizations of the memristor such as ZnO [5], and TaO_x [6, 7]. Another promising memristor type is the spintronic memristor [8]. The spintronic memristor is the main focus of this thesis.

2.2. Device Properties

As referred in Figure 2.1, the memristor relates the electric charge (*q)* and the magnetic flux (φ). The *q*-φ relation is a nonlinear relationship, and the memristor parameter is called memristance *(M).*

The memristor is said to be a charge-controlled memristor when its memristance is a *q* dependent. Where *M (q)* equals:

$$M(q) = {}^{d\varphi}/_{dq} \tag{2.1}$$

On the other hand, the memristor is said to be a flux-controlled memristor when its memductance *(W)* is a φ dependent. Where *W* (φ) is the inverse of the memristance and it equals:

$$W(\varphi) = {}^{dq}/_{d\varphi} \tag{2.2}$$

For the charge-controlled memristor, the current-voltage relationship is:

$$v = M(q)\,.\,i \tag{2.3}$$

For the flux-controlled memristor, the current-voltage relationship is:

$$i = W(\varphi)\,.\,v \tag{2.4}$$

2.2.1. Current-Voltage (I-V) Characteristic

In order to say that the memristor is a *fundamental* element, it must have a *unique* current-voltage characteristic that cannot be formed by any combination of the other three fundamental elements *R*, *L*, *C*. Figure 2.3 shows the difference between the current-voltage characteristic of the four fundamental elements. As shown in the figure, the memristor has a hysteresis current-voltage characteristic.

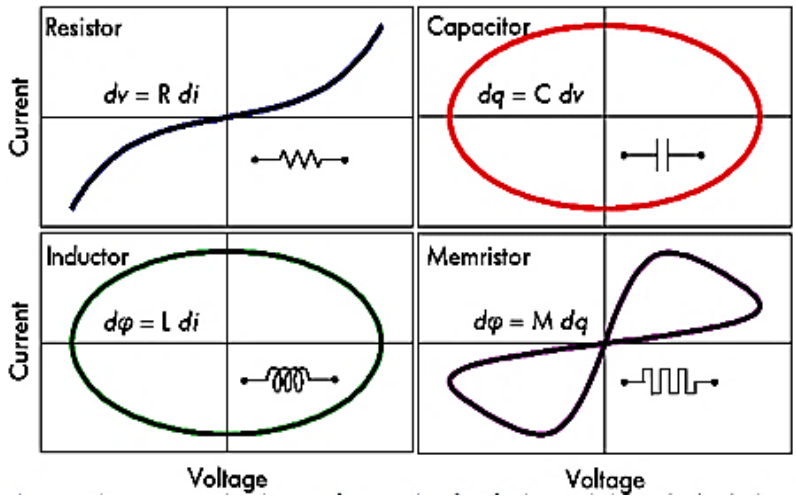


Figure 2.3 Current-voltage characteristics of the resistor, capacitor, inductor, and memristor [9].

Figure 2.4 represents the current-voltage characteristics of the memristor under a sinusoidal voltage signal at different frequencies. As shown in this figure, increasing the frequency of the applied signal reduces the hysteresis of the memristor's current-voltage characteristic. Under very high frequencies, the hysteresis completely vanishes and the memristor gives a resistor-like characteristic. The charge-controlled memristor is taken as an example to explain the reason of hysteresis reduction in higher

frequencies. Being a charge-controlled means that the memristance changes with the amount of the electric charge passed through the memristor in a specific direction. The higher the frequency for the same current amplitude, the less the amount of the charge *'$\Delta Q = I\,\Delta t$'*. Thus, at higher frequencies, the change in the memristance become smaller and the memristance hysteresis vanishes leading to a resistor-like current-voltage characteristic as shown in Figure 2.4.

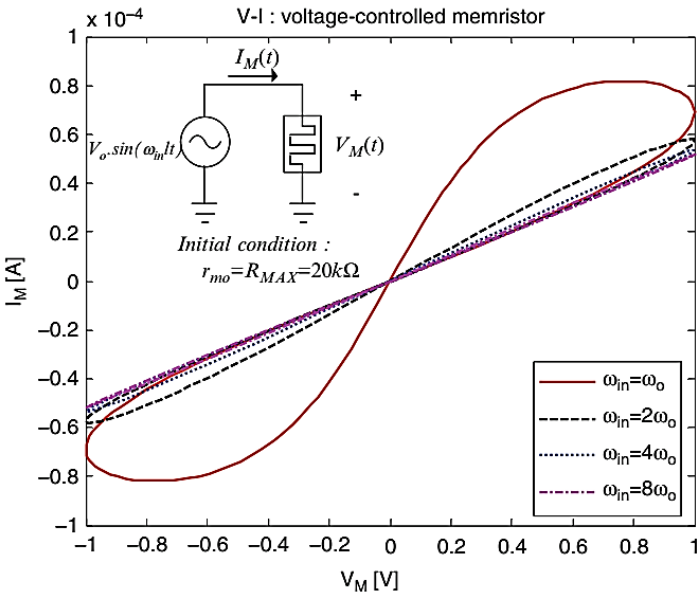


Figure 2.4 Current-voltage characteristics of memristor at different frequencies [10].

2.3. Types of Memristors

This section introduces a quick review of different implementations of memristor according to the type of the material used. The resistive and the spintronic memristors might be the most interesting types of memristor implementations. Thus, a special focus on them is provided here. The

modeling of these two memristor types is discussed in details in later sections.

2.3.1. Resistive Memristors

This type of memristors mainly depends on thin resistive film sandwiched between two metal electrodes in a similar manner to Figure 2.2. In order to consider this device as a memristor, its resistivity must change under the motion of electric current showing the hysteresis current-voltage relationship. Resistive memristors are used in building Resistive Random Access Memory (RRAM) cells. The theory of operation for any RRAM cell is that its resistivity can be switched between two or more resistive states based on inherent physical behavior affected by an external stimulation.

In case of absence of any external stimulation, the memristor device should keep its resistive state, which results in a non-volatile cell. In case of switching between two distinctive resistive states, these two states can represent Logic '1' and Logic '0' for the data storage. Resistive memristors have an additional advantage that they are usually able to take any resistive value between two resistive states, High Resistive States (HRS) and Low Resistive State (LRS), which means that it can be used in multi-bit data storage.

The physical mechanism of the resistive memristor is similar to most devices used as RRAM cells. In case of the device is in the HRS state, the current moves uniformly through the entire device, and the whole device has a high resistivity. On the other hand, the case of LRS is different. In the LRS state, a low resistivity path between the device's two electrodes is established. The current passes only through this limited regime of the

device, which acts as a low resistivity path surrounded by the rest of the device that still has high resistivity.

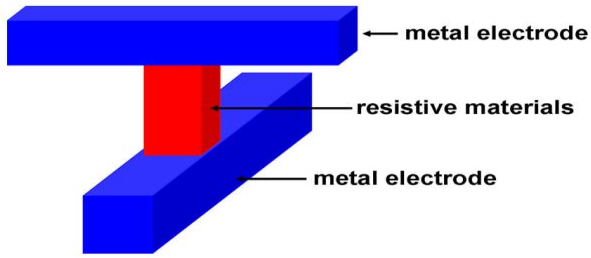


Figure 2.5 Resistive memristor based on MIM architecture [11].

Resistive switching devices can be divided into two groups, unipolar and bipolar devices. The differentiating between the two types depends on the polarity of the voltages needed for the SET and RESET. The SET usually refers to the switching from the HRS state to the LRS state, and the RESET refers to the switching from the LRS state to the HRS state. In the unipolar devices, the voltage needed for the SET 'V_{SET}' and the voltage needed for the RESET 'V_{RESET}' have the same polarity. In the bipolar devices, the V_{SET} and V_{RESET} have opposite polarities. The unipolar and bipolar switching mechanisms are shown in Figure 2.6. The memristive devices are bipolar devices, which means that voltages of both positive and negative polarities are needed for the switching operation.

Resistive memristors can be build using different materials such as TiO_2, ZnO, and TaO_x [5-7]. Despite that these types were built years ago, the physical interpretation of the switching mechanism is still not confirmed. The two most common proposed switching mechanisms are discussed here.

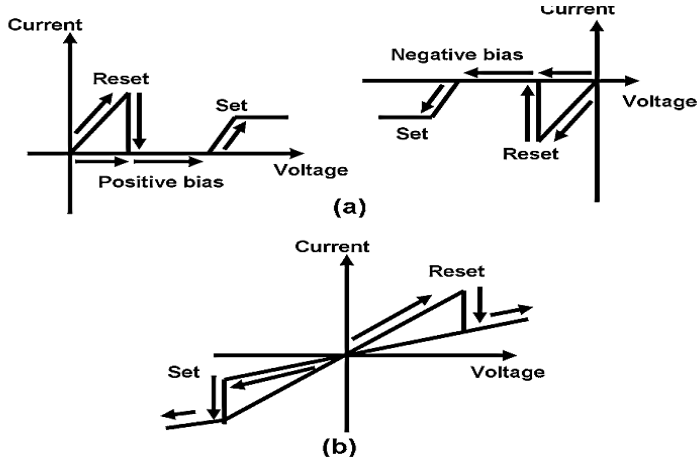


Figure 2.6 Switching of resistive materials (a) Unipolar mode (b) Bipolar mode [11].

The first and the most common interpretation of the switching mechanism is the electric pulse induced resistance switching (EIRP). This mechanism explained the resistance switching as a result of applying a strong directional electric field. That electric field establishes a *conductive filament (CF)* that have less resistivity than the rest of the device material. The CF establishes a low resistivity path between the top and the bottom electrodes of the resistive memristor. Thus, the current flow is concentrated in the CF which causes more heating around the CF. The heating helps in the process of construction of the CF, and the device becomes in an LRS state. That process is considered as a thermochemical process. In the RESET case, a reverse current passes in the memristor. This current induces a large heating at the bottom electrode, as the CF is thin near the bottom electrode, which leads to a thermal rupture of the CF restoring the previous HRS state. Figure 2.7 shows the steps of this mechanism.

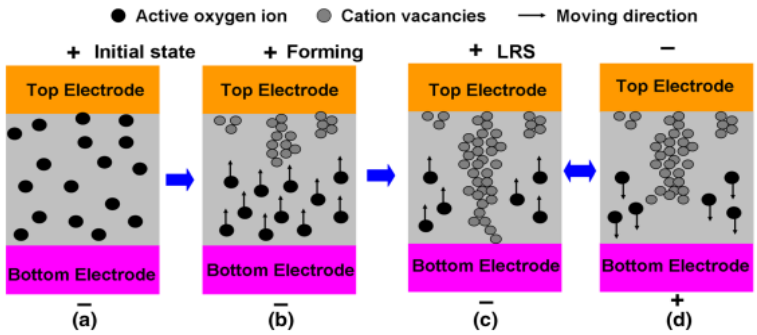


Figure 2.7 Formation of conductive filament (CF) (a) initial state (b) growth start from anode to cathode (c) CF completed (d) Reverse voltage causes CF rupture [12].

The second proposed switching mechanism is that oxygen ions that occur due to crystal defects and oxygen vacancies are the main reason for CF establishment. The applied positive voltage on the top electrode attracts the oxygen ions towards the top electrode. The oxygen ions are accumulated on the top electrode and repel each other toward the bottom electrode forming the CF. The RESET mechanism is similar to the first switching mechanism.

In both switching mechanisms, the CF always begins at the top electrode and then moves toward the bottom electrode. That is why the CF is narrower at the cathode. Thus, the joule heating at the cathode is high which plays the main role in destroying the CF when a voltage of opposite polarity is applied leading to the RESET operation and the HRS state.

The resistive memories gain a wide research interest due to the invention of the titanium-dioxide HP memristor and benefiting from the RRAM research that already existed years before the resistive memristor. In the following subsection, the titanium-dioxide HP memristor is discussed.

2.3.1.1. Titanium Dioxide Memristor

In 2008, HP labs announced a physical realization of a solid-state memristor using TiO_2 [2]. The HP memristor's basic structure is shown in Figure 2.2. It consists of a layer of TiO_2 sandwiched between two Platinum electrodes. The TiO_2 layer is divided into two parts -doped and undoped. The boundary between the doped and undoped TiO_2 is called "domain-wall". Domain-wall position (state) is changed under the effect of the applied voltage or current.

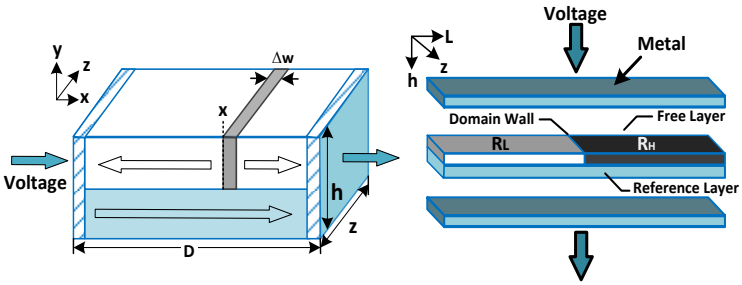
As mentioned, the titanium dioxide memristor was proposed by members of an HP Lab. The device is composed of a thin (*50 nm*) titanium dioxide film between two *5nm* thick electrodes, one is titanium, and the other is platinum. The titanium dioxide film consists of two layers, one of which has a slight depletion of oxygen atoms (undoped). The other is the doped layer with oxygen vacancies, which act as charge carriers. The doped layer has a much lower resistance than the undoped layer.

2.3.2. Spintronic Memristors

Chen et al. [13] described three different possible designs of spin-transfer torque based magnetic memristors. A promising structure is the domain-wall spintronic memristor, in which the device resistance occurs when the spin of electrons in one section of the device points in a different direction from those in another section, creating a boundary between the two sections called a "domain wall". Electrons flowing into the device have a certain spin, which alters the device's magnetization state. Changing the magnetization of the device moves the domain wall and changes its resistance.

Beside the solid-state device, magnetic technology provides an alternative method to implement memristive systems [8, 13]. Figure 2.8 shows two possible realizations of the spintronic memristor. The first device, shown in Figure 2.8.a, is the domain-wall spintronic memristor proposed by Wang and Chen [13].

The device geometry is In-Plane-Anisotropy (IPA), in which the current flow is parallel to the spintronic memristor junction. Another possible realization of the spintronic memristor is shown in Figure 2.8.b. This device has been proposed by Miao Hu in [8], and its geometry is Perpendicular-to-Plane Anisotropy (PPA), in which the current flow is perpendicular to the spintronic memristor junction.



(a) (b)

Figure 2.8 (a) A spintronic memristor with IPA structure. (b) spintronic memristor with PPA structure.

In both structures, the device is divided into two layers: a reference or a pinned layer (PL), and a free layer (FL). The magnetization direction in the reference layer is fixed. The domain-wall position in the free layer changes according to the magnitude and direction of the current passes through the device and on the duration of the applied current pulse. By changing the domain-wall position, the memristance of the device is varied.

Spintronic memristors are promising candidates for many applications Such as memory chips [14, 15], and neuromorphic circuits [16-18]. In the field of memory circuits, spintronic memristors offer excellent scalability, and non-volatility properties, leading them to become one of the main promising candidates for a high-performance and high-density storage technologies. In the field of logic circuits, a new type of implied logic using memristors is presented in [19]. The memristor-based logic has the unique ability to be fabricated with memory cells on the same chip. The memristor is used also in crossbar arrays in switching blocks of Field Programmable Gate Arrays (FPGAs) [20, 21].

The device is divided into two layers as shown in Figure 2.9. A reference or a pinned layer (PL), and a free layer (FL). The magnetization direction in the reference layer is fixed. The position of the domain wall in the free layer can be changed by passing a driving current, and hence the total memristance of the device changes.

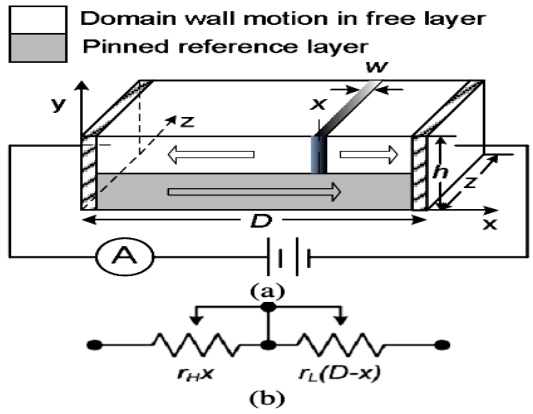


Figure 2.9 A spintronic memristor based on magnetic-domain-wall motion. (a) Structure. (b) Equivalent circuit [7]

The spintronic memristor has the potential to be a non-volatile memory element, since it holds its resistive value, even after it is unplugged from a power source. It also has the advantages of Magnetic random-access memories (MRAM) such as radiation hardness, and mature memory technology. Thus, the spintronic memristor-based memory devices could be the future of the non-volatile memories.

2.3.3. Other Types of Molecular Memristors:

Beside the resistive and the spintronic memristors, other possible realizations of memristors are provided in this section.

2.3.3.1. Polymeric Memristor

From its name, the polymer memristor is a memristor in which a thin polymeric strip and inorganic dielectric-type material are used to achieve a hysteresis current-voltage characteristic. The resistivity of the polymeric strip can be switched between an HRS state called 'reduced state', and an LRS state called 'oxidized state'. The mechanism of switching of the polymeric memristor depends on the well-known redox-reaction, which is a short for '**red**uction–**ox**idation reaction'. Oxidation is the loss of electrons or an increase in oxidation state by a molecule, atom, or ion. The *reduction* is the gain of electrons or a decrease in oxidation state by a molecule, atom, or ion.

As shown in Figure 2.10, the polymeric memristor contains a micro-strip *polyaniline* called 'PANI' deposited on a solid insulating substrate layer and sandwiched between two metal electrodes. Another layer of Lithium perchlorate ($LiClO_4$). Doped polyethylene-oxide (PEO) is

deposited over the PANI strip. The PANI-PEO interface is the place in which the redox-reaction takes place.

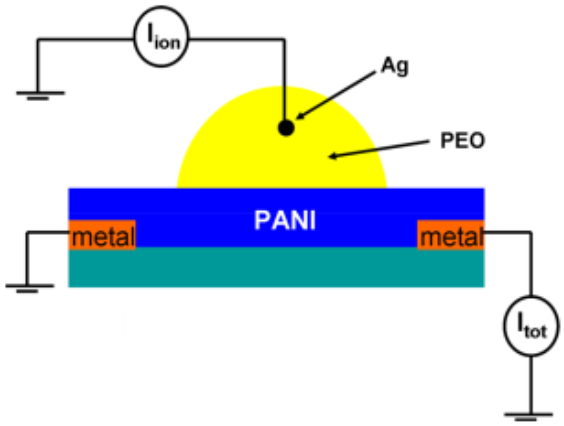


Figure 2.10 The cell structure of the polymeric memristor [11].

The theory of operation of this device is as follows:

- When applying a positive voltage to the top electrode, an active region with a voltage higher than the oxidation potential is established. Thus, the PANI layer switches from the insulating state to an oxidized conducting state only in the limited active region. This is called ‘oxidized state’ and it is corresponding to the LRS state. The oxidized region is ‘gradually formed’ and thus this operation is usually relatively slow and offers the gradual change in resistivity of memristors, which is modeled by a ‘state-variable’ representing the position of the device between the LRS and HRS states.
- When applying a negative voltage to the top electrode, the polymeric memristor faces a reduction potential as shown in

Figure 2.11. Thus, the PANI layer switched back from the oxidized state to the insulating ‘reduction’ state.

The polymeric device memristive function is consequently achieved by changing the applied voltage measured to a reference voltage to add or remove Li^+ ions to the PANI layer.

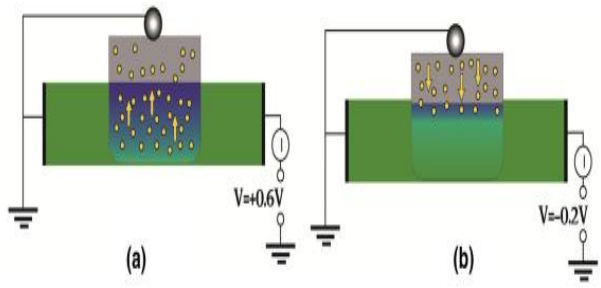


Figure 2.11 The polymeric memristor switching mechanism [22].

2.3.3.2. Ferroelectric Memristor

The ferroelectric memristor [23] uses a thin ferroelectric barrier sandwiched between two metallic electrodes. Switching the polarization of the ferroelectric material is achieved by applying a positive or a negative voltage across the junction, which leads to LRS and HRS resistances. The polarization does not switch abruptly. Those two states are used as Logic ‘0’ and Logic ‘1’ states in the ferroelectric memristor, which can be used in RAM circuits denoted by Ferroelectric RAM (FeRAM). The ferroelectric material has a non-volatile storage ability, which means that it can keep its state after removing the external field, which gives it the ability to achieve the memristive function. This feature is also used in many applications such as smart cards and radio frequency identification (RFID).

If the ferroelectric layer is at a nanoscale, it is denoted by a ferroelectric tunneling junction (FTJ). The ferroelectric memristor consists of an FTJ strip sandwiched between two metal electrodes. As stated, the switching mechanism is based on altering the polarization of the ferroelectric memristor by applying an external electric field. The change in the polarization causes the resistive switching of the device.

The realization of ferroelectric memristors can be done using a $BiTiO_3$ strip deposited onto a $La_xSr_yMnO_3$ layer and they are sandwiched by the two metal electrodes [24].

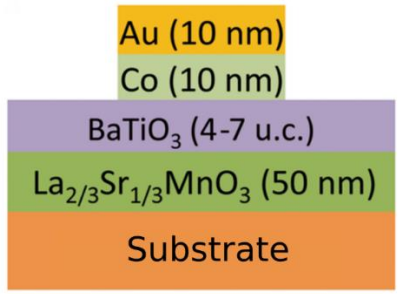


Figure 2.12 A cross-section of the FTJ used in ferroelectric memristors [24].

2.3.4. Comparison of Different Types of Memristor

The previous discussion aimed to give a thorough study of the most common memristor types from the fabrication point of view. It should be noted that the previous types are the most common memristor types up to the author's knowledge, but not *all* possible memristor implementations. There are other memristor types such as manganite memristors and resonant tunneling (RTD) memristors. However, RTD memristors characteristics are still not clear.

Table 2.1 Comparison between different memristor types [11].

Memristor Type	Resistive	Spintronic	Polymeric	Ferroelectric	Manganite
ON/OFF Ratio	2000	5	100	300	100
Access Time (ns)	~10	~10	~25	~10	~100
Retention	Very Long	Very Long	Relatively Long	Relatively Long	Long
Endurance	10^9	10^{16}	10^8	10^{14}	10^{16}
References	[5-7]	[13]	[11]	[23]	[25]

Table 2.1 presents a comparison between different memristor types [11]. From the table, we can see that the resistive memristor has the highest ON/OFF ratio, which increases noise margin and helps in using the memristor cell for a multi-bit storage. On the other hand, the resistive memristor has a lower endurance, which is the main disadvantage and it needs a new technology to be integrated with CMOS. The spintronic memristor has a much better endurance and the technology of integrating magnetic devices with CMOS already exists. However, the spintronic memristor has a low ON/OFF ratio and the fabrication flexibility is difficult. Manganite memristor has a good endurance also and an intermediate ON/OFF ratio, but its access time is very high. From this discussion, we can conclude that the resistive and the spintronic memristor might be the most promising types of memristors which is the reason there modeling are discussed in the following two sections.

2.4. Resistive Memristors Modeling

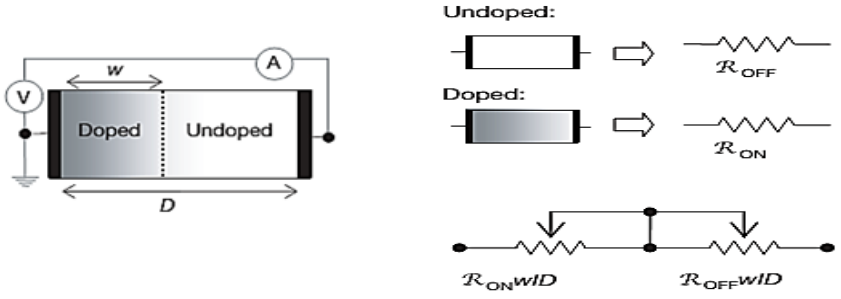
As is the case with any new technology, it is important to learn how the memristor behaves to external stimulus in terms of voltage and current. There are many proposed models of memristors depending on the needed compromise between simplicity and accuracy and on the type of application. In this section, we try to cover the main models of memristors.

2.4.1. Linear Ion Drift Model

The model discussed here is based on the HP memristor shown in Figure 2.2. In Linear Ion Drift model, a uniform electric field across the device is assumed; thus, there is a linear relationship between drift-diffusion velocity and the net electric field.

$$\frac{dw(t)}{dt} = \mu_V \frac{R_L}{D} i(t) \tag{2.5}$$

where D is the total TiO_2 length, $w(t)$ is a state variable defining the length of the doped TiO_2, R_L is the equivalent resistance of the memristor when the whole device is dropped, μ_V is the average ion mobility.



(a) (b)

Figure 2.13 The coupled variable-resistor model for a memristor (a) Memristor Device (b) Equivalent resistor model. [2].

According to the linear ion drift; the memristor can be modeled as a coupled variable-resistor model as shown in Figure 2.13, yielding the following I-V relationship[2]:

$$v(t) = \left(R_L \frac{w(t)}{D} + R_H \left(1 - \frac{w(t)}{D}\right)\right) i(t) \quad (2.6)$$

where R_H is the equivalent resistance of the memristor when the whole device is undoped.

Solving equations (5) and (6) the memristance of the device, for $R_H >> R_L$, simplifies to:

$$M(q) = R_H \left(1 - \frac{\mu_V R_L}{D^2} q(t)\right) \quad (2.7)$$

The coupled equations of motion for the charged dopants and the electrons in this device take the normal form for a current-controlled (or charge-controlled) memristor as in (2.5) and (2.6).

2.4.2. Nonlinear-Ion Drift Model

The nanometer dimensions of memristor cause a high electric field with only applying a few volts. Thus, the electric field can easily exceed 10^6 V/cm, and it is reasonable to expect a high nonlinearity in the ionic drift-diffusion. The linear drift assumption also suffers from a problem in incorporating boundary effects.

A few attempts have been carried out so far to consider this nonlinearity in the state equation[2],[26], [27]. Each paper proposed using a different 'window function *F(w/D)*' multiplied by the right-hand side of (2.5). Thus, the state equation can be modified to be as follows:

$$\frac{dw(t)}{dt} = \mu_V \frac{R_L}{D} i(t) F\left(\frac{w}{D}\right) \quad (2.8)$$

Qualitatively, the boundary between the doped and undoped regions moves with speed v_d in the bulk of the memristor, but that speed is strongly

suppressed when it approached either edge, *w~0* or *w~D*. Thus, the window function should satisfy *F(0)=F(1)=0* to ensure no drift at the boundaries.

2.4.2.1. Window Function

The choice of the suitable nonlinear drift model depends on the proper choice of the window function. Many papers proposed different window functions that attempt to achieve a good agreement with the nonlinear behavior and fewer simulation problems.

The first window function was proposed by Joglekar [28]. The window function equation is:

$$f(w) = 1 - (2(w/D) - 1)^{2p} \tag{2.9}$$

where p is a control parameter that defines the curvature of the window function. Figure 2.14 shows the Joglekar window function for different values of p. As shown in the figure, increasing the value of the parameter p makes the window function more flat with a value of unity, which reduces the effect of the window function in the middle around $w/D = 0.5$. The Joglekar window function is an empirical equation in which the value of p should be optimized to fit the real behavior of the memristor as possible.

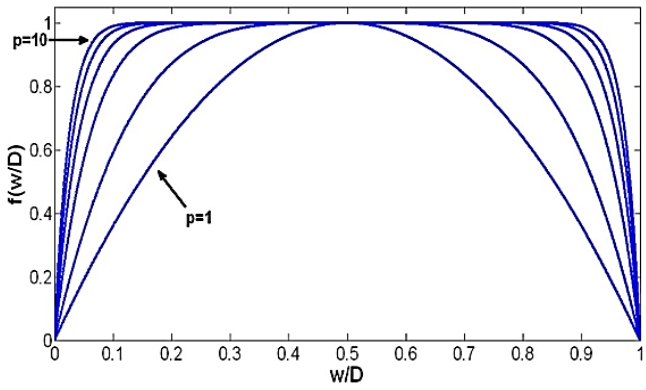


Figure 2.14 Joglekar window function [28].

The advantage of Joglekar window function is that it offers a simple straightforward relationship that achieves the desired boundary condition. On the other hand, The drawback of this window function is that once the state variable *w(t)* reaches one of the boundaries extreme point *w(t)=0 or D*, the rate of change of the state variable "*dw(t)/dt*" equals zero, and thus the state variable *w(t)* is *trapped* at this boundary.

Another window function was proposed by Biolek [29] in order to overcome this problem. The Biolek window function is as follows:

$$f(w) = 1 - ((w/D) - u(i))^{2p} \tag{2.10}$$

where *u(-i)* is the unity function as a function of the current direction. The window function of Biolek is shown in Figure 2.15.

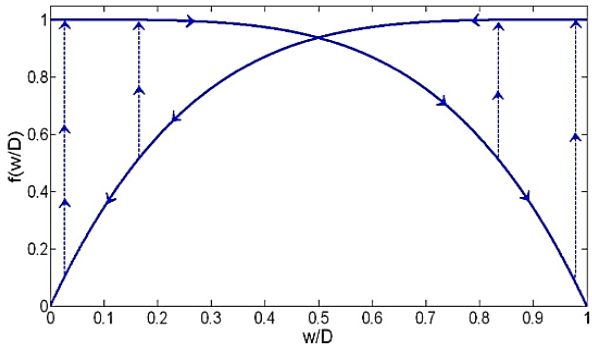


Figure 2.15 Biolek window function [29].

Both Joglekar and Biolek window functions do not have a scale factor and therefore the maximum value of the window function cannot be changed to a value lower or greater than one.

In 2015, a window function is proposed by Prodromakis [30]. This window function modified the Joglekar's window function in order to be able to control the maximum value of the window function to greater or less than unity. Equation (2.11) represents the Prodromakis window

function. Figure 2.16a shows this window function for different values of the parameter *p*, and Figure 2.16b shows the window function under different values of parameter *j*. The two parameters *P* and *j* offer a greater opportunity to fit the Prodromakis window function to the real memristor characteristics compared to Joglekar and Biolek window functions.

$$f(w) = j\left(1 - \left[\left(\frac{w}{D} - 0.5\right) + 0.75\right]^{tanh(P)}\right) \tag{2.11}$$

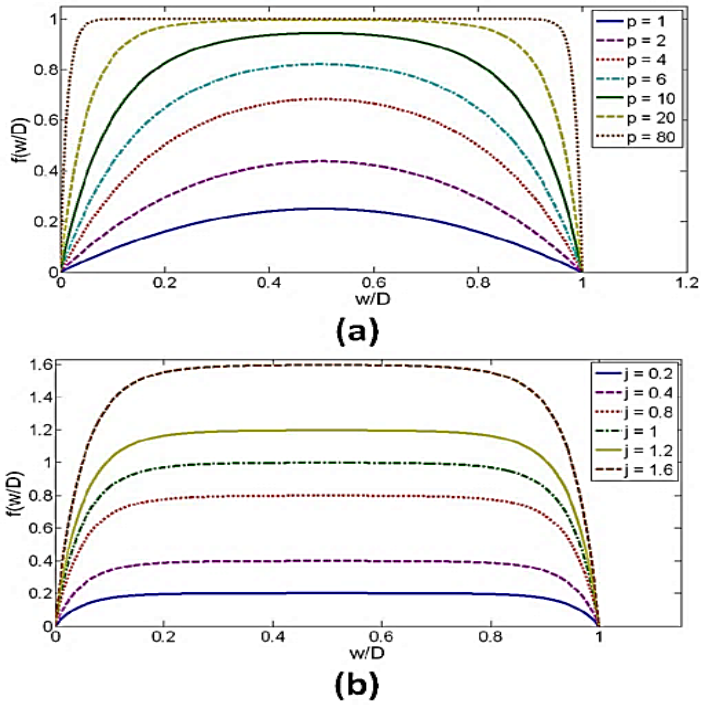


Figure 2.16 Prodromakis window function [30] described by (2.11)

2.4.3. Simmons Tunnel Barrier Model

Previous linear and nonlinear ion-drift models are empirical models that try to *fit* the real behavior of memristor. Both models do not represent physic-based models, and thus they do not give a real representation of a

specific memristor device based on its physical parameters. The Simmons tunnel barrier model was proposed by Pickett et al. who are members of the HP lab team that presented the TiO_2 memristor.

The model represents a physic-based current-voltage relationship model for the TiO_2 memristor, but with an added empirical window function. The theory of this model and the window function are provided in [31]. This model assumes nonlinear and asymmetric switching behavior of the TiO_2 memristor. In this model, rather than two resistors in series as in the linear drift model, there is a resistor in series with a tunnel barrier.

Figure 2.17.a shows the schematic of the device cross-section, and Figure 2.17.b shows the switching I-V curve. The window function of this model is provided in (2.12) and (2.13) [31]. The two equations represent the same window function but using different fitting parameters in order to account for the asymmetry of the memristor's switching mechanism. During the off switching, the current is positive *(i>0)*, and the window function of (2.12) is used. During the on switching, the current is negative *(i<0)*, and the window function of (2.13) is used.

$$\dot{w} = f_{off} \sinh\left(\frac{i}{i_{off}}\right) exp\left[-exp\left(-\frac{w-a_{off}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right] \qquad (2.12)$$

where the values of the fitting parameters are: f_{off} = *3.5±1 μm/s*, i_{off}*=8.9±0.3 μA*, a_{off}*=1.2±0.02 nm*, *b=500±70 μA, and* w_c*=107±4 pm.*

$$\dot{w} = f_{on} \sinh\left(\frac{i}{i_{on}}\right) exp\left[-exp\left(-\frac{w-a_{on}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right] \qquad (2.13)$$

where the values of the fitting parameters are: f_{on} = 40±10 μm/s, i_{on}=115±4 μA, a_{on}=1.8±0.01 nm, b=500±90 μA, and w_c=107±3 pm.

The current-voltage relationship and the SPICE model of the Simmons tunnel barrier are proposed by Hisham Abdalla et al. [32].

Simmons tunnel barrier's model offers high accuracy in modeling TiO_2 memristors and relates the device to its physical parameters. However, the current-voltage relationship of this model is complicated and the overall model is ambiguous. The model shows a very little flexibility during simulations and usually causes convergence issues.

However, this model is still used as the standard model for TiO_2 memristors and all other models accuracy and fitting are measured to this model.

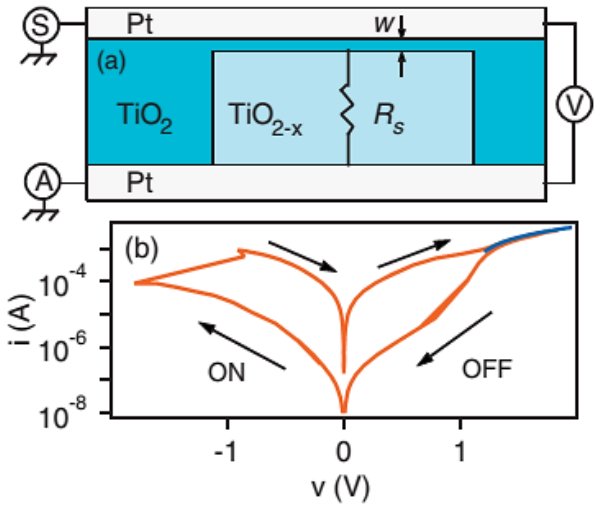


Figure 2.17 Device schematic and characterization protocol. (a) Schematic of the device cross-section (b) Example switching i-v curve for the device [31].

2.4.4. TEAM Model

The TEAM model [4] tries to provide a flexible model that can achieve a compromise between the simplicity of the linear ion-drift model and accuracy of Simmons tunnel barrier model. The model provides two possible current-voltage relationships in linear and exponential forms. The window function of the model is as follows [4]:

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}\left(\frac{i(t)}{i_{off}} - 1\right)^{a_{off}} . f_{off}(w) \; ; & 0 < i_{off} < i \\ 0 \; ; & i_{on} < i < i_{off} \\ k_{on}\left(\frac{i(t)}{i_{on}} - 1\right)^{a_{on}} . f_{on}(w) \; ; & 0 < i_{on} < i \end{cases} \quad (2.14)$$

The model has a large number of fitting parameters that enables the user to achieve better fitting to the desired memristor. The model also provides a current threshold as described in (2.14), as some memristor devices do not respond to external stimulations, which provides currents lower than a specific threshold value. The TEAM model is widely used as it gives a reasonable accuracy with a complexity degree between the linear ion-drift and the Simmons tunnel barrier. The availability of a Verilog-A code of the TEAM model also played an important role in its popularity [33].

2.4.5. Model Comparison

Table 2.2 provides a comparison between different resistive memristor models. It should be noted that the TEAM model is a general model, and it can be used for any memristor. However, this means that the TEAM model parameters do not give any direct relation with the physical parameters of any memristor type. The linear ion drift model is the simplest model and it has parameters that are physically connected to the resistive memristor. However, this model has many drawbacks as it has the lowest accuracy and it does not represent the nonlinearity behavior of the material ions. The nonlinear ion drift model provides a better representation of the resistive memristor. However, it requires fitting its window parameters to different memristors, as they are empirical parameters with no relation to the device material. In addition, the model still does not provide the best accuracy but it is better than the linear ion drift model accuracy. The Simmons tunneling barrier or the Pickett model provides the best accuracy and it is fitted to the

realized HP TiO_2 memristor. On the other hand, this model is highly complex and cannot be used in any mathematical analysis. The Simmons model also has a high probability of convergence issues during simulation and thus it is inefficient for SPICE simulators. The Simmons model is still used as a reference model for the HP memristor for model accuracy measurement.

Table 2.2 Comparison between different resistive memristor models

Model	**Linear Ion-Drift [2]**	**Non-Linear Ion-Drift [34]**	**TEAM [4]**	**Simmons Tunneling Barrier [31]**
State Variable	$0 \leq w \leq D$	$0 \leq w \leq D$	$a_{off} \leq x \leq a_{on}$	$x_{on} \leq x \leq x_{off}$
Memristance Deduction	Explicit	Intermediate	Intermediate	Ambiguous
Accuracy	lowest	Low	Intermediate	Highest
Relation to device physical parameters	No	No	No	Partially
Threshold	No	No	Yes	Partially exist
Probability of convergence	Lowest	Low	Moderate	High
complexity	Simple	Intermediate	Intermediate	Complex

* *w:doped region physical width , x: undoped region width*

Table 2.3 provides a comparison between different window functions used for nonlinear ion drift models. The Joglekar window function was the first proposed window function. This window function has a crucial drawback as its value equals zero at the state variable boundaries *w=0, and w=D,* which means that the state variable will be *trapped* at this boundary. The Biolek model solves this issue by using the current direction index *step(-i).* Prodromakis window function added the ability to scale the window function maximum value. The TEAM window function is

dedicated only to the TEAM model in order to fit it to the Simmons tunneling barrier model. All window types except for the TEAM window are symmetrical, which is not always the real case of the resistive memristors.

Table 2.3 Comparison of Different Window Functions

Window type	**Joglekar [28]**	**Biolek [35]**	**Prodromakis [27]**	**TEAM [4]**
Function	$f(w) = 1 - \left(\frac{2w}{D} - 1\right)^{2P}$	$f(w) = 1 - \left(\frac{w}{D} - stp(-i)\right)^{2P}$	$f(w) = j(1 - ((w - 0.5)^2 + 0.75)^P)$	$f_{on,off} = exp(-exp(\lvert x - x_{on/off}\rvert / w_c))$
Symmetric	Yes	Yes	Yes	Not necessarily
Resolve boundary condition	No	Yes	Partially	Partially
Scale factor	No	No	Yes	No
Fits memristive model	Linear/nonlinear ion drift / TEAM	Linear/nonlinear ion drift / TEAM	Linear/nonlinear ion drift / TEAM	TEAM for Simmons tunneling barrier fitting

2.5. Spintronic Memristors Modeling

In this section, two spintronic memristor models are discussed. The spintronic memristor can be modeled using any empirical memristor model. However, these models are the only available models that use the physical parameters to model the spintronic memristor devices up to author's knowledge. Other general memristor models are not related to the STT effect or the magnetic device material. The first model is proposed by Chen for a CIP GMR-based spintronic memristor [36]. The second model is a CPP TMR-based spintronic memristor model proposed by Miao Hu

[8]. Both models are nearly the same, as the only difference in Wang model is using two series resistors instead of parallel ones

The model of the spintronic memristor that is modified in this work was proposed in [7]. It uses r_L and r_H to denote the values of the resistance per unit length of the spintronic memristor at the low-resistance and the high-resistance states, respectively. The memristance of a spintronic memristor can be calculated as [7]:

$$M(x) = r_H.x + r_L.(D - x) \tag{2.15}$$

where *x* is the position of the domain wall, and *D* is the length of the device. The domain-wall velocity (v) is proportional to the effective current density J_{eff} [7], i.e.

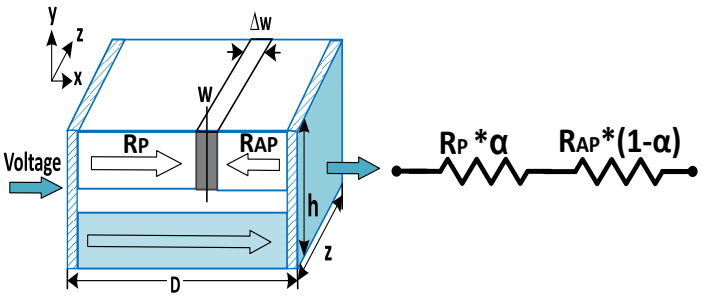
$$v = \frac{dx}{dt} = \Gamma_v.J_{eff} \tag{2.16}$$

where the effective current density J_{eff} only affects the domain-wall position if it is greater than a specific critical value J_{cr}.

$$J_{eff} = \begin{cases} J & J \geq J_{cr} \\ 0 & J < J_{cr} \end{cases} \tag{2.17}$$

2.5.1. Helen & Chen Model

Figure 2.18 shows the structure of the CIP spintronic memristor and the equivalent circuit proposed by Chen [36]. Chen's model assumes that when the FL has a parallel magnetization vector to the PL, the resistance is the lowest and denoted by R_P. On the other hand, when the FL has an antiparallel magnetization vector to the PL, the resistance is the highest and denoted by R_{AP}.



(a) (b)

Figure 2.18 GMR-based spintronic memristor (a) Structure (b) Equivalent Circuit.

Now let us assume that a part of the FL is parallel to the PL and the other part is antiparallel to the PL, and those two parts are separated by the domain wall. This can be represented by two series resistances as shown in Figure 2.18b. The total memristance of the device is given by:

$$M(\alpha) = R_P.\alpha + R_{AP}.(1-\alpha) \tag{2.18}$$

where α is the relative domain-wall position. It represents the "state variable" of this memristor and is equals the ratio of the domain-wall position w over the total length of the free layer D ($\alpha = w/D$, $0 \leq \alpha \leq 1$).

The velocity of the domain-wall v is proportional to the current density J passing through the memristor. It can be calculated as follows:

$$v(t) = \frac{d\alpha(t)}{dt} = \Gamma_v.J_{eff} \tag{2.19}$$

where Γ_v is the domain-wall velocity coefficient, and it is related to the device's structure and the material properties [36]. The value of Γ_v is estimated from a modified form of the LLG equation [37, 38] , and it can be expressed as [36]:

$$\Gamma_v = \frac{P\,\mu_B}{e\,M_S} \tag{2.20}$$

where P is the polarization efficiency, μ_B is Bohr magneton.

The effective current density J_{eff} is equal to J only when $J>J_{cr}$ as the current density only affects the DW position if it is higher than a specific critical value J_{cr}.

$$J_{eff} = \begin{cases} J; & J \geq J_{cr} \\ 0; & J < J_{cr} \end{cases} \tag{2.21}$$

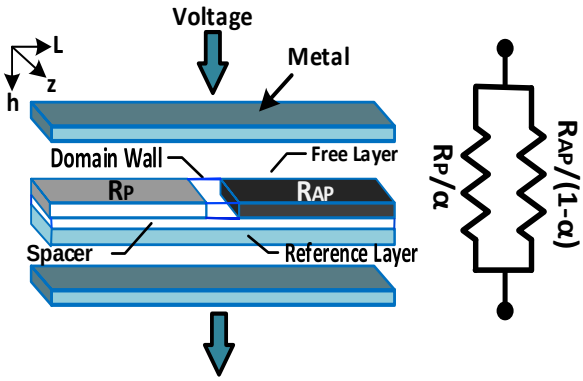
This model offers is similar to the linear ion-drift model of the solid-state memristors, but with a DW motion based on a simplification of a modified form of the LLG equation.

2.5.2. Miao & Chen Model

Figure 2.19a shows the structure of the CPP spintronic memristor proposed by Miao Hu [8]. The equivalent circuit of this spintronic memristor is shown in Figure 2.19b. This model is identical to the Chen model except for using parallel resistors instead of series resistors due to the CPP structure. The domain-wall separates the parallel and the antiparallel parts of the free layer, the model takes them as two parallel connected resistors R_P/α and $R_{AP}/(1-\alpha)$ respectively.

Thus, the overall memristance of the spintronic memristor can be calculated as follows [8]:

$$M(\alpha) = \frac{R_{AP}R_P}{R_{AP}\alpha + R_P(1-\alpha)} \tag{2.22}$$



(a) (b)

Figure 2.19 TMR-based spintronic memristor (a) Structure (b) Equivalent Circuit.

The DW velocity is calculated from (4) similar to the Chen model. The magnetic-based memory devices strongly depend on the temperature [39, 40]. Both Chen and Miao Hu models do not include the thermal fluctuations effect on the device behavior.

Chapter 3: Overview of Memristor Applications

3.1. Introduction

Many memristor applications are proposed including memory chips, neuromorphic systems, logic circuits, and FPGA switching blocks. In the field of memory chips, memristors can be used in Resistive Random Access Memory (RRAM) cell structures, Magnetic Random Access Memory (MRAM) cell structures, and Memristor-based Content Addressable Memories (MCAMs).

Memristors have distinguished properties that permit great opportunities in memory design. The first property is the device's inherent non-volatility. This property greatly helps in the design of memory circuits. Memristors also offer excellent scalability. Thus, the memristor is one of the main promising candidates for a next-generation high-performance high-density universal memory technology that can be used as a replacement for all current memory types. In the field of neuromorphic systems, the inherent "*remembering*" property of the memristor can be used effectively to build circuits with lower area and complicity. The need for a "*learning/training*" property in neuromorphic circuits greatly benefit from the ability of memristor to "memorize" the current pass in it and its direction.

In the field of logic circuits, a new type of IMPLY logic circuits was implemented using memristors. The memristor-based implied logic has a distinguished feature that it can be fabricated with memory cells in the same place on the chip, providing opportunities for novel non-von Neumann computer architectures [41]. Memristors are also used in the design of crossbar-arrays, which are used in the switching blocks of the Field

Programmable Gate Arrays (FPGAs). This chapter provides a brief review of memristors applications with a special focus on the memory design using memristors.

3.2. Memristor-based memory circuits

As mentioned, memristor's nonvolatile, high scalability, and fast switching properties may lead to a new generation of universal memory devices that replaces existing DRAMs, SRAMs, and Flash memories.

DRAM cell in the current technology occupies about $6F^2$, where F is the half-pitch. The one-transistor one capacitor (1T1C) topology is the most common topology used in building DRAM cells. The research field in DRAM includes using capacitors with higher dielectric constants, investigating the 3D-NAND DRAMs, and reducing the cell size to $4F^2$, which is still very challenging.

In the field of non-volatile memories, flash memories serve more than 99% of current nonvolatile memories. The flash memory cell uses one transistor (1T) to work as both an access element and a storage cell.

However, as current memory technology is reaching its scaling limit, other technologies are investigated like FeRAM, MRAM, PCRAM, and RRAM. Spintronic memristors can be used in MRAM, and resistive memristors can be used in RRAM. All these emerging technologies usually used an element that is equivalent to a resistor or a capacitor. The problem here is that both resistors and capacitors are two terminal elements, which means that these elements cannot provide the "gating" function in addition to their main role as a storage element. Thus, current memory cells usually combine 1T1C, 1T1R, or 1D1R, which reduces scalability. On the other hand, if no gating or access element is used, the memory array faces an

important issue known as the “sneak path”. The sneak path issue will be discussed in some details in section 3.2.5.

A final note is that the memristor offers a very interesting feature, which is the ability to be used in multilevel cells (MLC) which allows the cell to store more than one bit and increase the storage capacity dramatically. This advantage may be the main point of strength of memristors against other emerging memory technologies.

3.2.1. Basic Cell

The basic memristor-based memory cell can be built in different topologies. The main three topologies are using memristor only cell (0T1M), one transistor one memristor (1T1M), or one diode-one memristor (1D1M). The three types are discussed briefly in this section.

3.2.1.1. 0T1M Memory Cell

The simplest way of building a memristor-based memory is using only one memristor as a memory cell. Benefiting from its inherent nonvolatility, the stored data in the memristor is kept as long as no current passes through the memristor.

The memory array is built as shown in Figure 3.1, where a *k x m* array of memory cells using one memristor for each cell is built. The row and column decoder are used to select the memory cell on which the read/write operation is done. The main drawback of this topology is that due to the non-gating of each cell, some undesired sneak paths occurs. However, this technique provides the highest possible density which is highly required in memory circuits.

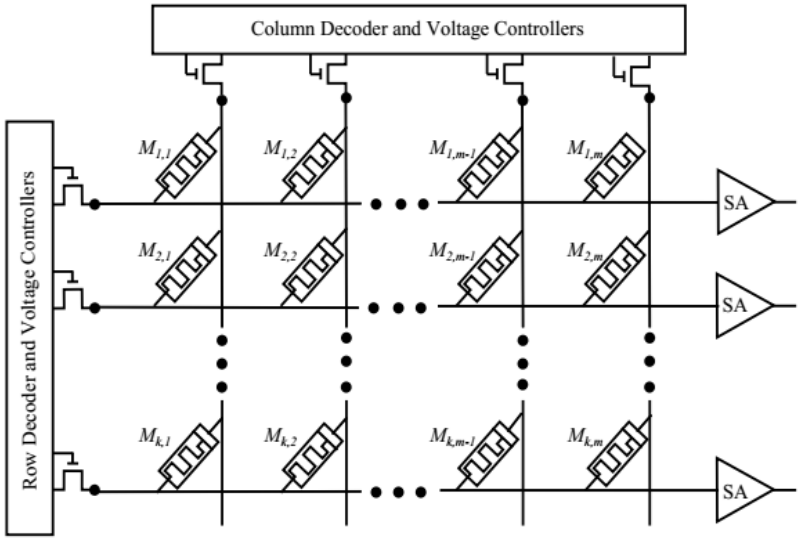


Figure 3.1 Schematic of a conventional *k x m* memristive memory crossbar [42].

3.2.1.2. 1T1M Memory Cell

The 1T1M memory cell is another way to build memristor-based memory arrays. The memory cell is shown in Figure 3.2 in which the memristor memory element is accessed through the access transistor. Although this topology solves the sneak path problem, it will reduce the array density considerably. This topology is still required to guarantee reliability, and it can be beneficial in multi-level memory cells as one transistor only is used for a memory cell that can store two or more bits. The schematic of the 1T1M memristive-memory crossbar is shown in Figure 3.3. The pull-up voltages of the first column and the first row are activated to select the memory element M_{11}.

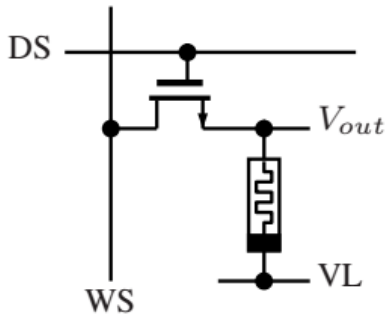


Figure 3.2 Memristor-NMOS (1T1M) storage cell [43]

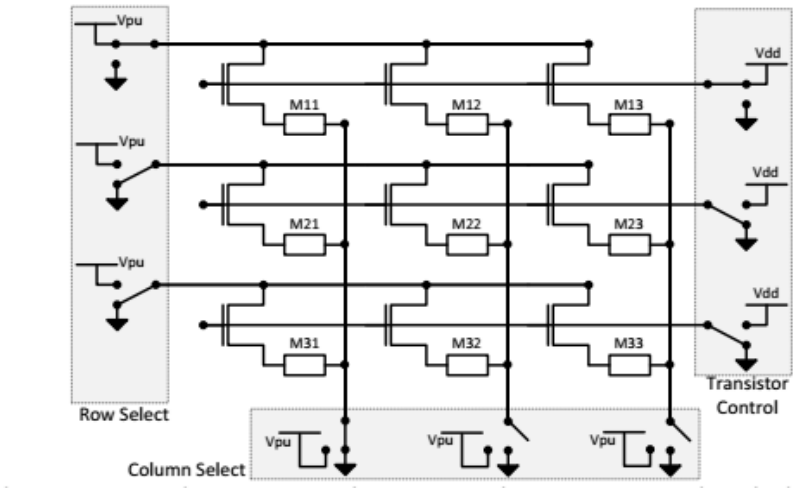


Figure 3.3 Accessing memory element M11 in a 1T-1M memristive memory crossbar [44].

3.2.1.3. 1D1M Memory Cell

The third topology is the 1D1M memory cell. The 1D1M memristive memory crossbar is shown in Figure 3.5. However this memory element is non-gated, but the diode that needs about 0.5 volts to conduct current will reduce the sneak path problem considerably as the sneak path usually requires going through multiple memory cell elements and thus multiple diodes.

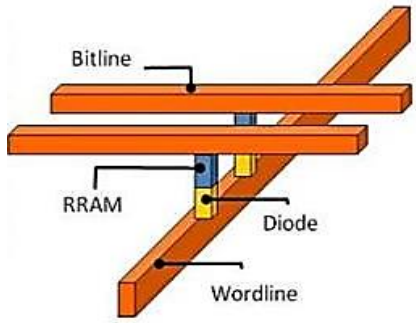


Figure 3.4 1D1M RRAM cross-bar structure[45]

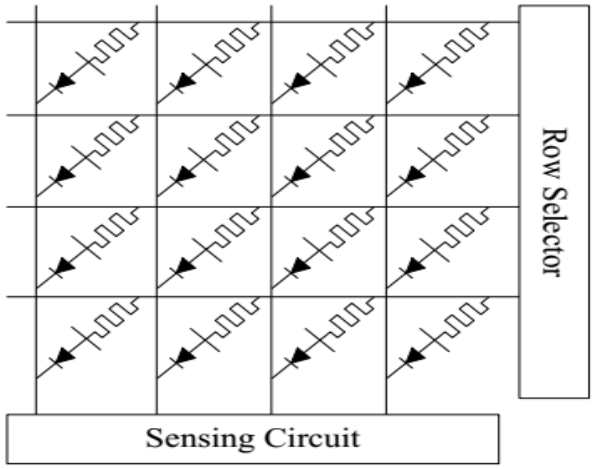


Figure 3.5 Memristor-Diode (1D1M) memory array [46] .

3.2.2. Read/Write Circuits

The read/write circuit of spintronic memristor memories requires a careful design to avoid data disturbance during the read operation. The current that passes through the memristor memory element during the read operation changes the state variable position. After multiple reading operations, the accumulated effect on the state variable eventually leads to alter the stored data. Many read/write circuits were proposed for

memristive memory circuits. The two read/write circuits provided in this discussion covers two main *ideas* that are used in most read/write circuits.

Figure 3.6 shows a read/write circuit proposed by Yenpo et al. [15]. The write operation is achieved by applying a DC write voltage for enough time T_W to ensure full switching. As shown in Figure 3.7a, a write voltage of 1V is applied for 4ns to achieve full switching from Logic 0 to Logic 1. Figure 3.7b shows the calculation of the minimum time required for switching to the minimum level that is interpreted as Logic 1 (*0.6 V*).

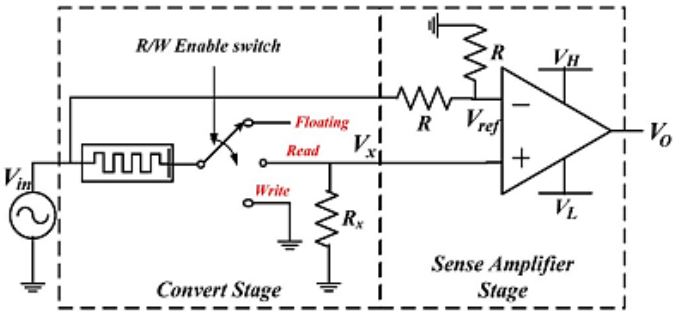


Figure 3.6 Yenpo Read/Write Circuit proposed in [15].

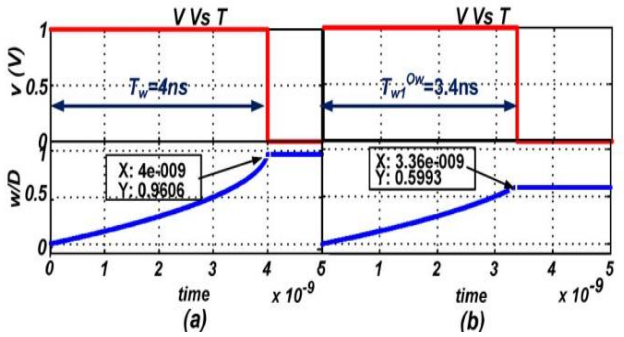


Figure 3.7 Write operation (a) Logic 1 full switch (b) O_H level (O_H=0.6) [15].

The read operation is achieved by applying the read pulse shown in Figure 3.8. The read pulse consists of two pulses of opposite polarities, and

with the same amplitude and width in order to compensate the read disturbance of each other. However, in the case of pulse widths mismatch, a small read disturbance occurs which means that this circuit needs a periodic refreshment after a specific number of reading cycles. The reading operation is achieved by comparing the sensed voltage V_X on the resistor $R_X = (R_H + R_L)/2$ caused by the voltage divider between the memristor and the resistor R_X, with a reference voltage $V_{ref} = V_{read}/2$.

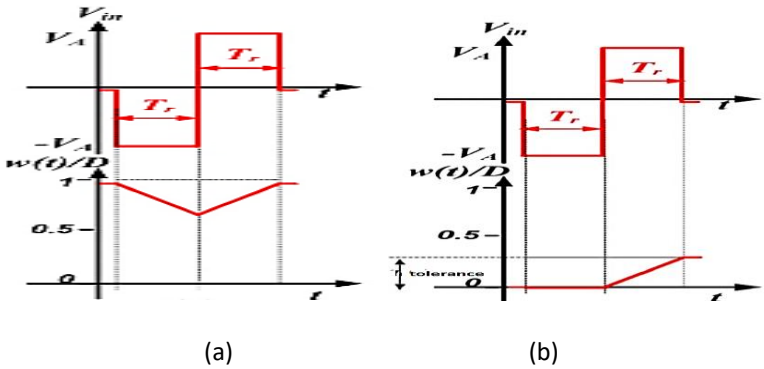


Figure 3.8 Read pulse when reading (a) logic '0'(w=D) (b) logic '1'(w=0) [15]

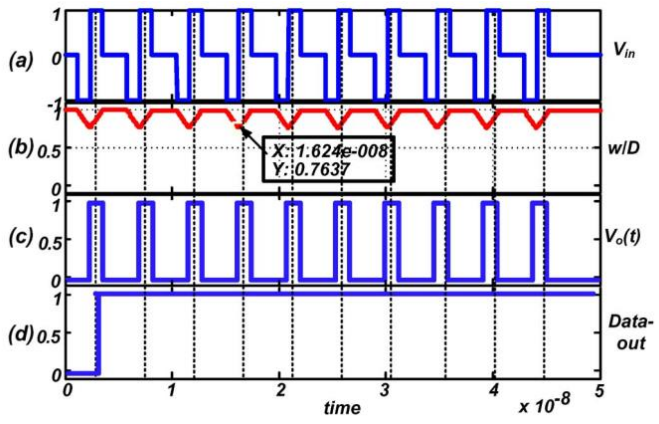


Figure 3.9 Read operation (logic 1) (a) Read pulse waveform (b) Memristor state (c) Output voltage (d) Logic value at data-out buffer [15].

Figure 3.9 shows the waveforms of the read operation of a stored logic 1. Figure 3.9a is the read pulse waveform and Figure 3.9b is the state variable waveform of the memristor. As shown in this figure, the state variable variation for the positive pulse compensates the variation due to the negative pulse for an ideal read pulse. The stored data is then sensed during the positive read pulse as shown in Figure 3.9c, and then the data output is buffered at the sensed logic state as in Figure 3.9d.

There are two main disadvantages of this circuit. The first one is the large area required to fabricate the resistors. The second one is that the circuit suffers from data disturbance during the read operation if the positive and negative read pulses are mismatched. As shown in Figure 3.10, a mismatch of ±*10%* caused a loss of the data after *20* cycles.

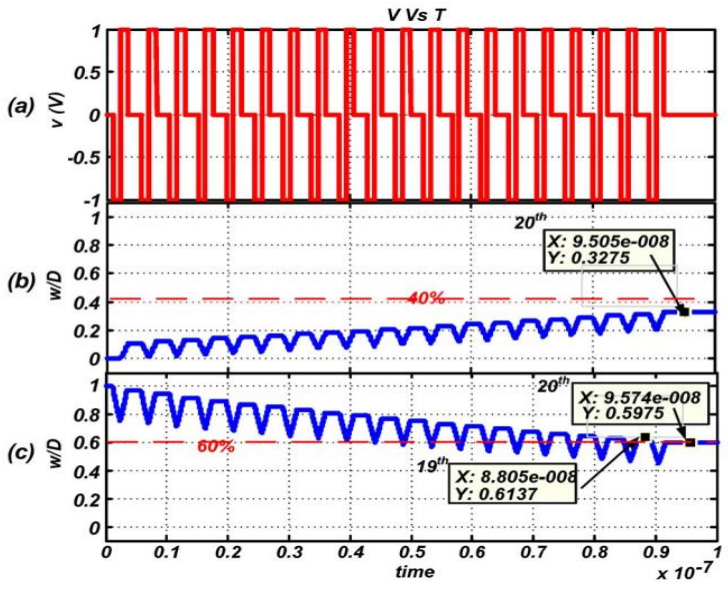


Figure 3.10 (a) Impact of ±10% pulse mismatch for (b) '0' state (c) '1' state [15].

The second R/W circuit is El-Shamy et al. which is shown Figure 3.11 [47]. This circuit was originally proposed for solid-state memristors in

order to avoid the date disturbance of Yenpo R/W circuit. Note that this circuit is equivalent to the convert stage only. However, due to the small R_H of spintronic memristors compared to resistive memristors, this advantage cannot be achieved in case of spintronic memristors as will be discussed in Chapter 5.

The write operation is identical to Yenpo read/write circuit. The read/write equivalent circuit during the reading operation is shown in Figure 3.12.

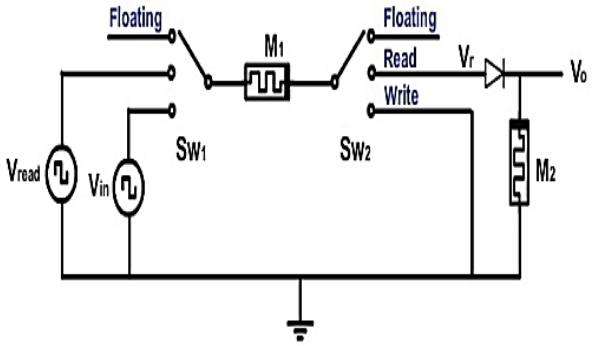


Figure 3.11 El-Shamy Read/Write Circuit proposed in [47].

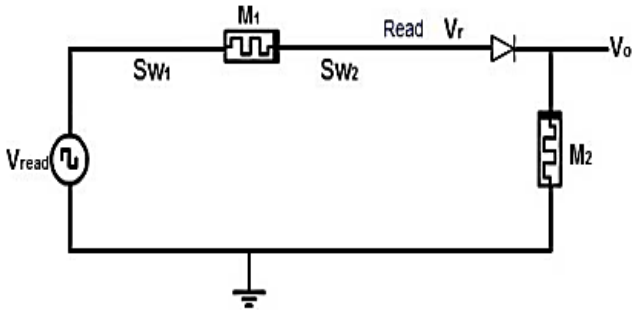


Figure 3.12 El-Shamy Read/Write Circuit during the reading operation [47].

The idea of the reading operation depends on dividing the voltage $(V_{read} - V_D)$ between two memristors M_1 which represents the memory cell and

M_2 which represent a part of the reading circuit. The second memristor M_2 is kept always at the off state benefitting from the diode that prevents current from passing in the reverse direction. For resistive memristors, R_H is usually high and thus the passing current is very low providing a disturbance-free reading operation as shown in Figure 3.13.

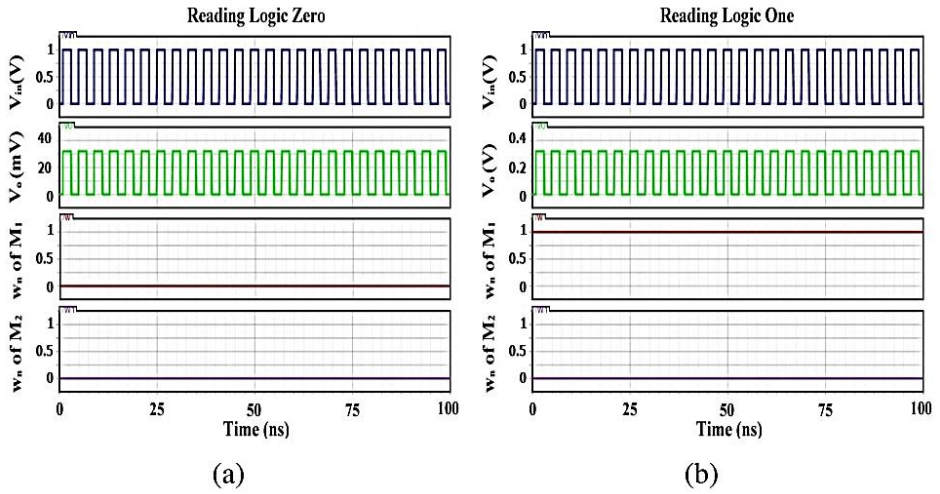


Figure 3.13 Fifty successive reading cycles when reading (a) logic 0 (b) logic 1 [47].

It should be noted that all previous simulations use resistive memristors. Spintronic memristors have a small OFF state resistance R_H and a much lower ON/OFF resistance ratios compared to resistive memristors, which increases the possibility of reading disturbance and reduces the sensed voltage difference. It is required to design a read/write circuit that can achieve larger sensed voltage difference, lower read operation data disturbance, and smaller occupied area.

3.2.3. Sneak Path Problem

One of the most important issues that face memristive memories is the sneak path problem. This problem arises from the fact that the memristor

device has "no gate". Thus, undesired paths of current arise and form an additional resistance R_{SP} in parallel with the main path memristor's resistance R_M.

Figure 3.14a shows the reading operation of a 1M memory array in the ideal case. The second row and second column are selected to read the memristor $M_{2,2}$. Ideally, this memristor is the only element that can conduct current as it is the only element that both of its terminals -column terminal and raw terminal- are selected leading to a potential divider circuit between the load resistance R_L and the memristor resistance R_M. However, as shown in Figure 3.14b, the current can take other indirect sneak paths through multiple memristor elements resulting in an additional undesired resistance R_{SP} in parallel with the sensed resistance R_M.

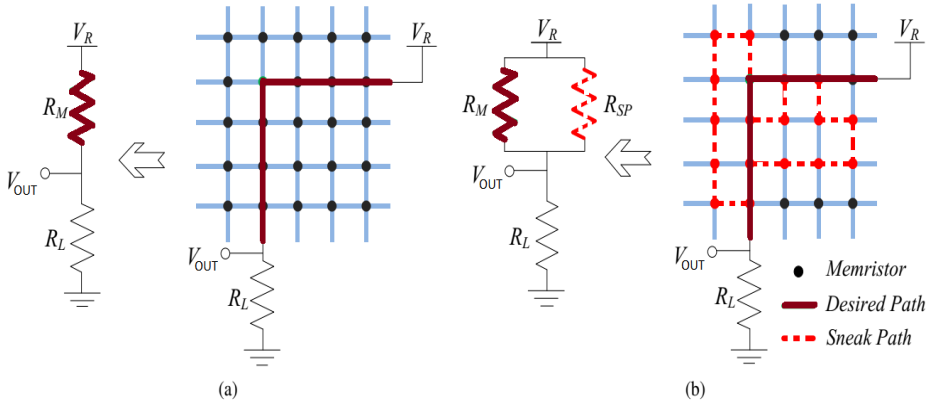


Figure 3.14 Effect of the sneak-path during the reading process (a) ideal case (b) real case [46].

The sneak path problem is an important issue that limits the use of the 1M memristive memory arrays. One straightforward solution is to add a transistor to each cell as discussed in the 1T1M memristive memory arrays. However, this is highly undesirable technique, as it will reduce the array

density substantially. The 1D1M memristive memory arrays reduce the sneak path array problem, but also at the cost of the memory array density.

Another direction in solving the sneak path problem is to keep the 1M memory array and try to change other parameters that affect this problem. HP Labs team introduced a technique of multistage reading to overcome the sneak path problem [48]. The solution is straightforward but has a long algorithm and it will be even worth with larger designs. The reading procedure begins with performing a current measurement of the target cell in its normal state. Then, performing two current measurements to the target cell after putting it into OFF state and ON state. Comparing the three measurements, the cell content is defined. Finally, the data is rewritten to the target cell.

The second solution is the unfolded architecture proposed in [49]. This solution does not use a memristor cell at each cross-point in the memory array. However, this leads to the same problem of reducing the memory density similar to gating techniques.

Mohammed Zidan et al. also studied the effect of the array aspect ratio on the sneak path problem in order to find the best aspect ratio that should be used [46].

3.2.4. Memory Technologies Comparison

Table 3.1 provides a comparison between different memory technologies. The memristor is provided in a separate column for clarification, despite that it should be included in other technologies according to its type. Memristors provide a small cell area (~$4F^2$) which makes it a promising element for high-density memories. It can provide a

nonvolatile element similar to flash memories with a high speed close to SRAMs and DRAMs. It also has a good retention and acceptable endurance. That combination of advantages of different memory technologies is the reason that memristor might replace all these technologies in the future.

Table 3.1 Comparison between different memory technologies [46, 50].

	Mainstream Memories			**Emerging Memories**			**Redox Including Memristor**
	DRAM	SRAM	NAND Flash	FeRAM	STT-MRAM	PCRAM	
Cell element	1T1C	6T	1T	1T1C	1(2)T1R	1T(1D)1R	(1D)(1T)1R
Cell area	6-10 F^2	>100F^2	4F^2	15-35F^2	6-50F^2	4-30F^2	4F^2
Energy/bit (pJ)	0.005	0.0005	0.00002	0.01	0.1-2.5	2-25	0.1-3
Read time (ns)	2-10	0.2	100	45	10-35	10-50	<50
Write time (ns)	2-10	0.2	10^6	65	35	12	<10
Retention	4-64ms	N/A	10 years	10 years	>10 years	>10 years	>10 years
Endurance (cycles)	$>10^{16}$	$>10^{16}$	10^4	10^{10}-10^{14}	10^{15}	10^9	10^{12}

3.3. Memristor-based Neuromorphic circuits

The field of memristor-based neuromorphic applications is a very promising field and gains a wide research interest. Using memristors as synapses in neuromorphic circuits can potentially offer both high connectivity, and high density required for efficient computing.

The brain tissues are generally assumed to be complex networks of neurons that change their functional properties by processing sensed data. This process is called learning and the learned knowledge is stored in the

cortex through modified synaptic connectivity. The learning in the neural tissues has various models like Hebbian correlational learning [51] and spike time dependent plasticity [52], and others. It is conceivable that all these learning effects are in fact manifestations of memristive behavior in the neural tissue.

The neuromorphic hardware community is largely focused on developing massively parallel, subthreshold analog circuits, often combined with memristive or other experimental devices for implementing synaptic memory. Any platform designed to develop intelligent machines must be (1) massively-parallel; (2) low power; (3) algorithmically flexible.

Storing and updating synaptic weights based on synaptic plasticity rules is a computationally very demanding operation in biologically-inspired neural networks [53] using basic operations of addition and multiplication. Memristive hardware holds the promise of greatly reduced power requirements by increasing synaptic memory storage capacity and decreasing wiring length between memory storage and computational modules.

Memristive nano-devices have inspired the neuromorphic community to examine their potential for building low power, intelligent machines. Their dynamics [31] and small size have suggested their use as “synapses” in analog circuits that learn online in real time [54-56]. There are suggestions from many researchers that memristor-based analog memory can be used to build brain-like learning machines with nanoscale memristive synapses.

Digital computers have one significant shortcoming: they are very inefficient at integrating the stiff differential equations found in many cognitive algorithms. Short of an algorithmic breakthrough in nonlinear

dynamics, digital computers will probably never compete with analog in this area. Thus, the analog behavior of memristors can be of a great help in such algorithms.

3.3.1. Synapses Analysis Modeling Using Memristive Devices

Figure 3.15 shows how to model the biological neural network using memristor crossbars. Synapses are emulated using the memristor device, and the synapse weight is analog to the memristor's state variable. Corinto et al. present a rigorous mathematical study concerning the dynamics of different memristor models with a special emphasis on the effect of initial and boundary conditions of the system [57]. The analytical results connecting the initial condition of a memristor with its current-voltage characteristic can be used to devise a new pattern recognition system based on the synchronization of nonlinear dynamical systems. Nathan McDonald analyzed some promising and practical non-quasi-static linear and nonlinear memristor device models for neuromorphic circuit design and computing architecture simulation [58, 59].

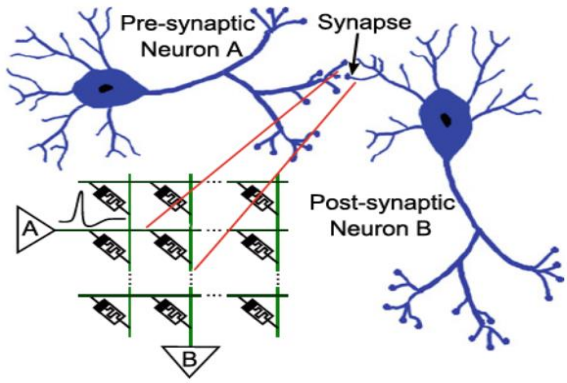


Figure 3.15 Modeling the biological neural network using memristor crossbars [54].

3.4. Memristor-based Logic

An important advantage of memristors is that it can be used in designing a combined memory and logic functions on the same chip. The memristors can be used efficiently in crossbar arrays for both memory and logic functioning.

Memristors can be used to perform implied logic operations. It is important to note that the logic circuits realized by memristor differ than the Boolean logic realized by CMOS technology. The realization of implied logic is explained in [60, 61]. T. Raja and S. Mourad provided a tutorial on how to use memristor crossbars for logic design [62]. Hybrid reconfigurable logic circuits are fabricated by integrating memristor-based crossbars onto a foundry-built CMOS platform using nano-imprint lithography [63].

Another important way of memristor logic design is the memristor ratioed logic (MRL) that was proposed in [65]. This design has the advantage of being more reliable and has fewer design constraints. Figure 3.16 shows the schematic of AND gate and OR gate which have the same design but only the memristors are reversed. This type can only achieve non-inverting functions and uses the static CMOS inverter to achieve any inverting function and to restore logic swing.

For the OR gate, applying a voltage of V_{IN1}='1' and V_{IN2}='0' decreases the resistance of the first memristor (*R1*) and increases the resistance of the second memristor (*R2*). Thus, the output becomes high. Using the same theory for all other cases, it can be shown that the gate in Figure 3.16a work as an OR gate, and the gate in Figure 3.16b work as an AND gate.

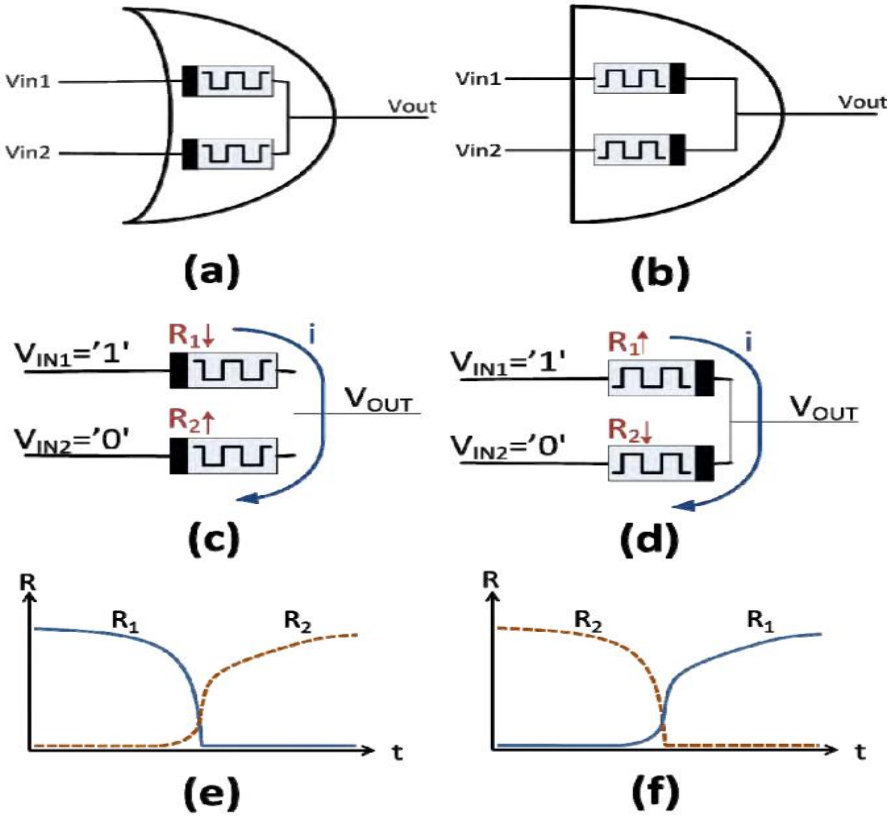


Figure 3.16 Schematic of MRL gates (a) OR gate (b) AND gate . The behavior of (c) an OR gate and (d) AND gate when V_{IN1}='1' and V_{IN2}='0'. The change of the resistance of memristive devices for the (e) OR, and (f) AND gates [65].

3.5. Memristor-based FPGA Switching Blocks

A novel FPGA architecture with memristor-based reconfiguration (mrFPGA) was introduced in [66]. The proposed architecture is based on a CMOS-compatible memristor fabrication process. The programmable interconnects of mrFPGA use only memristors and metal wires. Thus, the interconnections can be fabricated over logic blocks, resulting in significant reduction of overall area and interconnect delay. D. Strukov and A. Mishchenko also introduced novel FPGA circuits based on hybrid

CMOS/resistive switching device (memristor) technology to achieve different logic architectures [67].

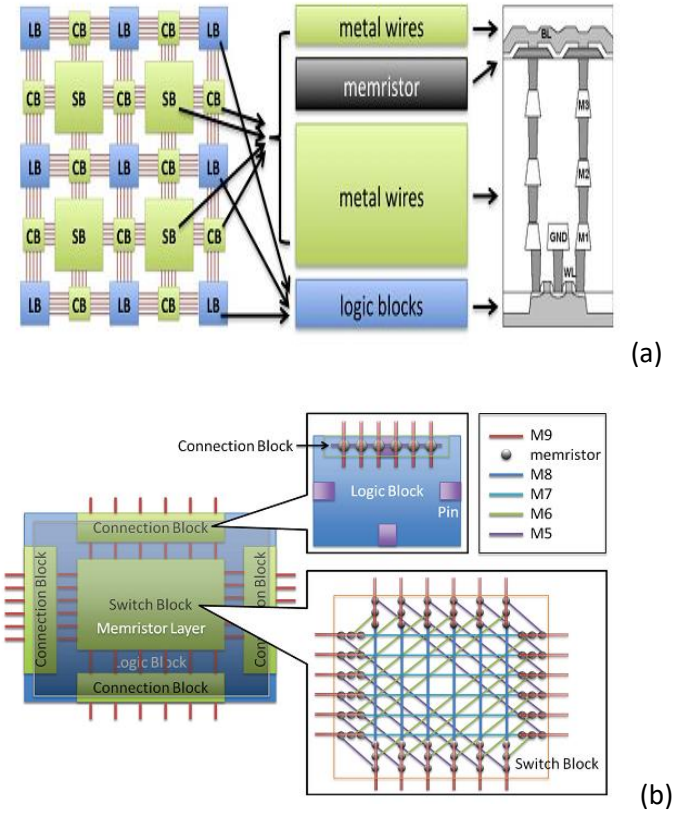


Figure 3.17 mrFPGA (a) architecture (b) Design of connections and switching blocks [66]

3.6. Analog Applications

Memristors can be used to implement programmable analog circuits, Amplifiers, and oscillators. Sangho Shin showed that memristors can be used to implement programmable analog circuits, leveraging memristor's fine-resolution programmable resistance without causing perturbations due to parasitic components [68]. The resistance programming can be achieved

by controlling the input pulse width and its frequency. A Pulse-coded programmable resistor using memristor is shown in Figure 3.18.

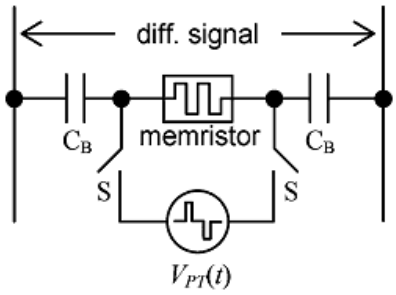


Figure 3.18 Pulse-coded programmable resistor using a memristor [68]

T. Wey and W. Jemison used an automatic gain control (AGC) topology with a variable gain amplifier utilizing a (TiO_2) memristor [69]. Makot O. Itoh derived several memristor-based nonlinear oscillators from Chua's oscillators [70]. M. Affan Zidan presented a memristor-based oscillator without using any capacitors or inductors [71]. The introduced reactance-less oscillator enables an area efficient implementation for low-frequency oscillators. The circuit is shown in Figure 3.19. Despite that this circuit is theoretically suitable for low frequencies, it should be noted that the circuit assumed a very slow switching speed of the memristor which could be impractical for actual circuit realization.

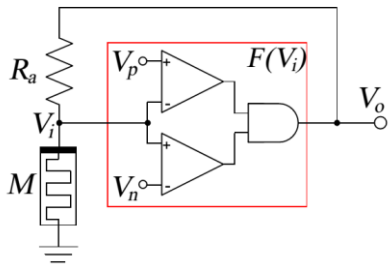


Figure 3.19 Memristor based reactance-less oscillator [71].

The nonlinear dynamics of three memristor based phase shift oscillators are reported in [72]. It is considered that they will be a plausible solution for the realization of parametric oscillation as an autonomous linear time-variant system. A.G. Mosad presented an improved memristor-based relaxation oscillator which offers higher frequency and wider tuning range than the existing reactance-less oscillators [73].

CHAPTER 4: Modeling of Spintronic Memristors

4.1. Introduction

The model of the spintronic memristor that is modified in this work was proposed in [7]. The overview in Sec 2.5 provide a detailed explanation of existing spintronic models. This section focuses on the equations of the GMR-based memristor. It uses r_L and r_H to denote the values of the resistance per unit length of the spintronic memristor at the low-resistance and the high-resistance states, respectively. The memristance of a spintronic memristor can be calculated as [7]:

$$M(x) = r_H.x + r_L.(D - x) \tag{4.1}$$

where x is the position of the domain wall, and D is the length of the device. The domain-wall velocity (v) is proportional to the effective current density J_{eff} [7], i.e.

$$v = \frac{dx}{dt} = \Gamma_v.J_{eff} \tag{4.2}$$

where the effective current density J_{eff} only affects the domain-wall position if it is greater than a specific critical value J_{cr}.

$$J_{eff} = \begin{cases} J & J \geq J_{cr} \\ 0 & J < J_{cr} \end{cases} \tag{4.3}$$

From (4.3), it is obvious that this model did not include some important properties that occurs in all magnetoresistive based structures such as the effect of temperature variations, and the magnetoresistance voltage-dependence. This model needs to be modified to include such important properties. Through this chapter, two spintronic memristor models are

proposed. The first model deals with including the temperature variations effect and keeps model simplicity. The second model is a more complicated model that tries to include all physical parameters and to be suitable for all device geometries forming a *general* model for all spintronic memristors. The proposed models are implemented in Verilog-A, and integrated with an integrated circuit CAD tool to carry out any desired analyses of different circuits that utilize spintronic memristors.

4.2. Thermal Fluctuation Aware Model

4.2.1. Thermal effect on magnetic devices

Experimental studies of MRAM structures show that increasing the temperature of MRAM cells increases the probability of the cell switching between the parallel and the antiparallel states [8]. The thermal fluctuation becomes a disadvantage during the reading process as it can cause an undesirable switching to the data stored in the MRAM cell.

The probability that an MRAM cell switches its state after a duration time (*t)* is calculated by [9]:

$$P(t) = 1 - exp\left(\frac{-t}{\tau_{P\rightarrow AP}}\right) \tag{4.4}$$

where $\tau_{P\rightarrow AP}$ is the Neel-Brown relaxation time of an ensemble in an initial parallel state and can be calculated as [8]:

$$\tau_{P\rightarrow AP} = \tau_0 \, exp\left[\frac{K_U V}{K_B T}\left(1 + \frac{H(t)}{H_K}\right)^2\left(1 - \frac{I(t)}{I_{cr}}\right)\right] \tag{4.5}$$

where *H(t)* is the applied magnetic field, *I(t)* is the applied current, τ_0 is the nominal switching time when a current equals to I_{cr} is applied to the cell, K_U is the anisotropy constant, *V* is the volume of the MRAM cell's

(memristor's) FL, K_B is the Boltzmann constant, and T is the absolute temperature in Kelvin.

Equations (4.4) and (4.5) show that increasing the temperature increases the relaxation time ($\tau_{P\rightarrow AP}$), which increases the probability of the MRAM cell switching. This effect occurs in both writing and reading processes.

4.2.2. Proposed Thermal Fluctuation Aware Model

The spintronic memristor model presented in [7] assumed that when the current density is less than a specific critical value J_{cr}, then no change occurs to the domain wall position. According to this assumption, if the current that is used to read the stored data in a spintronic memristor-based memory cell is smaller than this critical value ($I_{read}<I_{cr}$), then the data stored within the cell is not affected by the reading process. Correspondingly, there exists no read disturbance regardless of the number of successive read cycles or the operating temperature value.

However, as reported in [8], it is shown that even if the applied current is less than the critical current, the data stored in the memory cell is changed due to the thermal fluctuation [8].

From (4.4), the probability of switching the cell state during the read process is [11]:

$$P_{failure} = 1 - \ exp\left(\frac{-t_P}{\tau_{P\rightarrow AP}}\right) \tag{4.6}$$

where t_P is the duration time when I_{read} is applied to the memristor that achieves a full memristor state switching (i.e., switching the memristor from the low-resistance state to the high-resistance state). In case of successive read cycles, t_P becomes the total duration of the successive read pulses required to have a full switching in the memristor state. In absence

of an external applied field ($H(t)=0$), $\tau_{P\rightarrow AP}$ defined in (4.5) is reduced to [11]:

$$\tau_{P\rightarrow AP} = \tau_0 \exp\left[\frac{K_U V}{K_B T}\left(1 - \frac{I_{read}}{I_{cr}}\right)\right] \quad (4.7)$$

Equation (4.6) shows that when the summation of the read pulses durations, and consequently the number of reading cycles, increases, there is a high probability that the domain wall switches its state from parallel to anti-parallel or vice versa. In other words, the memristor switches its state even if the read current (I_{read}) is lower than the critical current value (I_{cr}) especially, for a large number of successive read operations. (4.7) shows that increasing the temperature decreases the duration ($\tau_{P\rightarrow AP}$) and thus increasing the probability of failure. The term ($K_U V/K_B T$) is considered as a "stability factor" to the memory circuit.

Equation (4.7) also shows another important design factor, which is the ratio between the read current (I_{read}) and the critical current (I_{cr}). Decreasing the term (I_{read}/I_{cr}) gives a better stability against thermal fluctuation.

These model modifications have a great significance in the analysis of the memory reading process and can be used to define the maximum allowable successive read cycles before the stored data in the spintronic memristor is disturbed.

Now we need to modify the model in [7] to take into account the effect of thermal fluctuation. Instead of assuming that J_{eff} equals zero for ($J<J_{cr}$) as in [7], the thermal fluctuation effect on J_{eff} is taken into account in the modified model.

From its definition, τ_0 is the switching time when a current of magnitude equal to I_{cr} is applied to the cell. Based on (4.2) we can write that:

$$\int_0^D dx = \int_0^{\tau_0} \Gamma_v . J_{cr}\, dt \tag{4.8}$$

This equation gives that:

$$D = \Gamma_v J_{cr} \tau_0 \tag{4.9}$$

Now we need to define the value of J_{eff} that achieves the same full switching in a duration time equals to t_P. Thus from (4.2), we can write that:

$$\int_0^D dx = \int_0^{t_P} \Gamma_v . J_{eff}\, dt \tag{4.10}$$

This equation gives that:

$$D = \Gamma_v J_{eff}\, t_P \tag{4.11}$$

Equating (4.9) and (4.11) gives that the equivalent effective current density for the thermal fluctuation is:

$$J_{eff} = \frac{J_{cr}\, \tau_0}{t_P} \tag{4.12}$$

Thus, the value of J_{eff} in (4.3) is modified to be:

$$J_{eff} = \begin{cases} J & J \geq J_{cr} \\ \frac{J_{cr}\, \tau_0}{t_P} & J < J_{cr} \end{cases} \tag{4.13}$$

where t_P can be calculated from (4.6) for a given design parameter ($P_{failure}$), as follows:

$$t_P = \tau_{P \to AP}\, ln\left(\frac{1}{1 - P_{failure}}\right) \tag{4.14}$$

4.2.3. Simulation Results

The spintronic memristor's material properties and model parameters are taken from [7]. The Verilog-A code of the proposed model is provided in Appendix A. The nominal switching time calculated from (9) is $\tau_0 = 100nS$. The duration of the read pulse is chosen to be $t_{read}=10nS$ [12]. The thermal factor (K_UV/K_BT) $=50$ at room temperature ($t=27°C$).

Figure 4.1 shows the probability of failure versus the number of cycles that achieves a full switch to the memristor memory cell for different values of (I_{read}/I_{cr}) at room temperature. The figure indicates that decreasing the read current strongly increases the stability of the memory cell during the read process.

However, decreasing the read current has two disadvantages. First, the sensed voltage difference becomes very small, which reduces the cell's noise immunity and makes the design of the supporting read circuit very challenging.

To understand this concern, let us study this issue using the read circuit design proposed in [13]. The critical current is $I_{cr}=35\mu A$, and the two memristance states are $R_P = 5\ K\Omega$ and $R_{AP} = 6\ K\Omega$. Let us consider $I_{read} = 0.9*I_{cr} = 31.5\mu A$. The read circuit is based on comparing the memristance value (R_P or R_{AP}) with the average value of the parallel and antiparallel resistances (5.5 KΩ). Thus the voltage difference sensed at the input of the comparator terminals will be $\Delta V=I_{read}*(R_{AP} - R_{avg}) \approx 16$mV. This sensed voltage is too small compared to the comparator's offset voltage, which is typically larger than 50mV. Accordingly, reducing I_{read} results in very complex, power consuming, and large area read circuits.

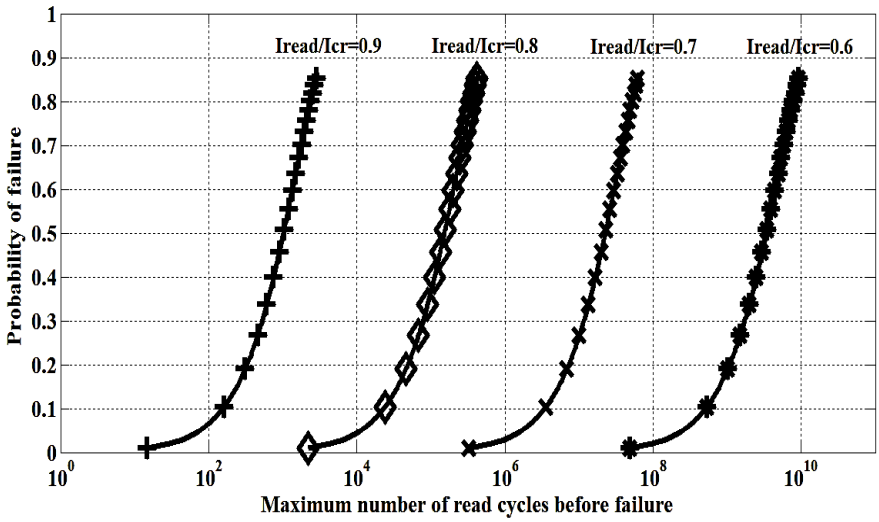


Figure 4.1 Probability of failure versus the number of reading cycles before failure.

Second, decreasing I_{read} decreases the speed of the reading process. Therefore, choosing the read current value (I_{read}) is a trade-off between reducing the thermal fluctuation and achieving a larger sensed voltage difference.

A final remark in Figure 4.1 is that the calculated number of reading cycles represent total cycles before "full switch". The reason for this is that the $P_{failure}$ defined in (6) assumed the probability of failure is the probability of a "full switch" as the phenomenon was studied generally for any Magnetic Tunneling Junction (MTJ) based structure. In case of the domain-wall spintronic memristor, if the memristor state changes from 0% to 50%, then the data stored in the cell is already destroyed. For example, at $P_{failure}=10\%$ & $I_{read}=0.9*I_{cr}$, data will be destroyed after 80 read cycles only as the state variable x exceeds $0.5*D$.

Figure 4.2 shows the relationship between the number of cycles before failure versus the read current ratio (I_{read}/I_{cr}) under different $P_{failure}$ values

at room temperature. As shown in this figure, in order to achieve less probability of failure, the maximum number of reading cycles before failure is reduced. This is a hard limitation on the memory design, which must be taken into consideration. In memory design, if the probability of failure is $P_{failure} \approx 0.1\%$, at $I_{read} = 0.8 * I_{cr}$, the maximum number of reading cycles before failure is *110* cycles.

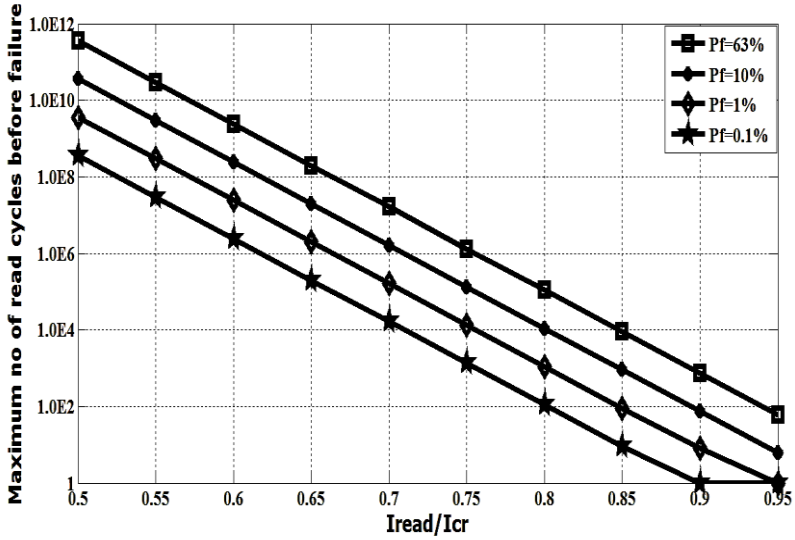


Figure 4.2 Calculated number of reading cycles before failure versus the read current ratio (Iread/Icr) for different probabilities of failure.

Figure 4.3 studies the effect of temperature variation on the maximum allowable successive read cycles versus the read current ratio (I_{read}/I_{cr}). As shown in this figure, the maximum allowable successive read cycles decrease exponentially with temperature increase. For example, at 110°C, and $I_{read}/I_{cr} = 0.75$, it takes only 100 read cycles before the data is altered.

In the design of memory circuits, it is convenient to assume a temperature of around 70°C for commercial applications [74].

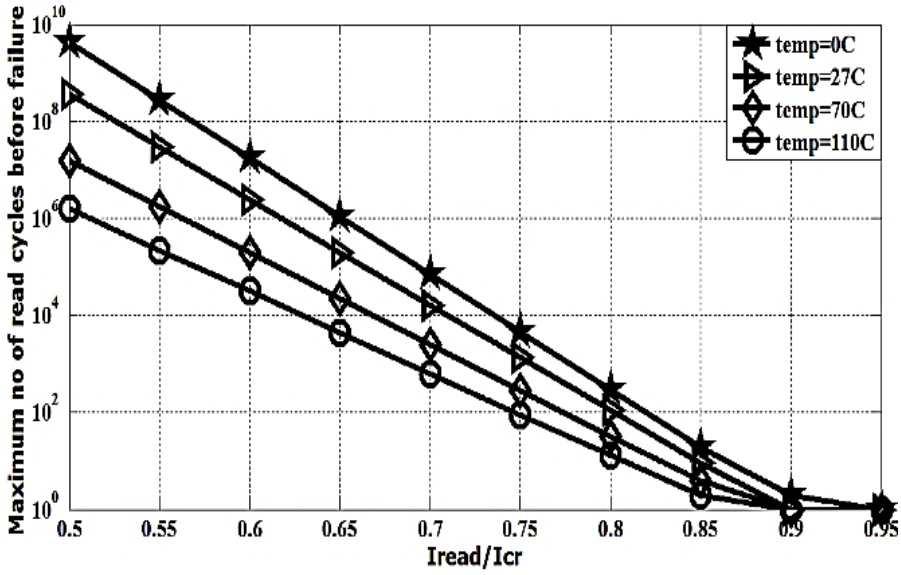


Figure 4.3 Calculated number of reading cycles before failure versus the read current ratio (Iread/Icr) for different temperature values.

4.2.4. Design Insights

From the proposed modified model as well as the presented simulation results, the following design guidelines and insights are extracted to help the spintronic memristor-based memory designers.

1) The read current (I_{read}) should be chosen carefully. Increasing I_{read} reduces the stability of the circuit due to thermal fluctuations, and thus reduces the maximum allowable successive read cycles. On the other hand, reducing I_{read} reduces the sensed voltage difference, the noise immunity, and the speed of the reading process. Therefore, the selection of the I_{read} value is a trade-off between thermal fluctuation impact and the supporting read circuit complexity.

2) Memory circuit design always requires a strict constraint on the allowable probability of failure as it causes a considerable data disturbance. Spintronic memristor-based memory designers should define the accepted

$P_{failure}$, and based on that, the maximum allowed successive read cycles is defined. A refresh scheme is needed to avoid read disturbance. Thus, this model gives the designer an important insight on when the refreshment circuit is required.

3) Temperature variation greatly affects the probability of failure in spintronic memristor based memories. Spintronic memristor-based memory designers should define carefully the expected operating temperature of the memory device.

4.3. LLGS-Based Spintronic Memristor Model

4.3.1. Issues of Previous Models

In this section, three spintronic memristor models are discussed. These models are the available models that are dedicated to spintronic memristor devices up to author's knowledge. Other general memristor models are empirical models with no relation to the STT effect or the magnetic device material. The first model is the spintronic memristor model proposed by Miao Hu [8]. This model represents the memristor as two parallel resistors that are a function of the domain-wall position as will be discussed in the following subsection. There is a similar model proposed by Wang [13], but for IPA spintronic memristor. Both models are nearly the same, as the only difference in Wang model is using two series resistors instead of parallel ones. The Miao Hu model is chosen due to the advantage of using PPA devices over IPA devices as discussed in the previous section. The second model is the proposed thermal fluctuation aware model. From its name, the second model is a modified model of the first one with considering the thermal fluctuation effect.

In the three models, there are some assumptions that limit the model accuracy, and usage.

1) As given in (4.2), the rate of change of the state variable has a "linear" dependence on the effective current density of the memristor. This linear dependence represents the simplest and the lowest accuracy assumption of modeling the dynamical behavior of memristors. Although, that these models are straightforward models that achieve faster simulations, a more accurate model is needed for the estimation of the dynamical behavior of spintronic memristors.

2) The three models do not provide enough linkage to the physical parameters, structure, and dimensions of the spintronic memristor. A model with a direct relation to the magnetic material properties and device structure can be of a great impact on the studying and the manufacturing of the spintronic memristor. In addition, the proposed model will allow the optimization of the spintronic memristor materials' properties and design parameters at early design phases.

3) The three models assumed that the antiparallel resistance R_{AP} has a fixed value. Actually, the antiparallel resistance in magnetic-based devices is strongly dependent on the applied voltage as shown in Figure 4.4. Equation (4.15) provides an acceptable approximation for the tunneling magnetoresistance ratio (TMR) as a function of the applied voltage [75]. Taking the effect of the applied voltage on the TMR and consequently, R_{AP} is essential in the spintronic memristors simulations and strongly affects the design of the spintronic memristor-based memory cells.

$$TMR(V) = TMR_0 \frac{1}{1+\left(\frac{V}{V_h}\right)^2} \tag{4.15}$$

where V_h is the voltage at which the TMR is halved.

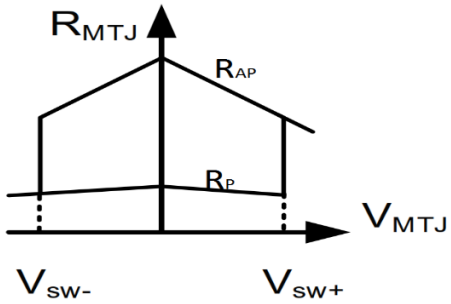


Figure 4.4 MTJ device's resistance vs applied voltage [76].

4) Finally, these models do not consider the thermal dependent parameters in the spintronic memristor. The TFA model considered only one temperature dependent parameter (J_{cr}), and the other two models did not include any thermal dependent factors.

5) Chen and TFA models are only applicable for GMR CIP structures, and Miao Hu model is only applicable for TMR CPP structure. A more generalized model that cover different possible structures of spintronic memristors can offer a standard model for any spintronic memristor.

4.3.2. Dynamical Behavior of Magnetic Devices

The Landau-Lifshitz-Gilbert (LLG) equation [77-79] describes the dynamic behavior of the magnetization vector of magnetic materials according to the following relationship:

$$\frac{\partial \vec{M}}{\partial t} = -\frac{\gamma}{1+{\alpha_g}^2}\vec{M} \times \vec{H}_{eff}(\theta) - \frac{\alpha_g \gamma}{(1+{\alpha_g}^2)M_s}\vec{M} \times (\vec{M} \times \vec{H}_{eff}(\theta)) \quad (4.16)$$

where α_g is the gilbert damping parameter, γ is the gyromagnetic ratio, M_S is the saturation magnetization, Heff is the effective magnetic field, and θ

is the angle between the easy axis of the magnet and the magnetization vector.

The first term of the LLG equation represents the precession of the magnetization vector due to the applied magnetic field. The second term represents a damping phenomenon that tends to counteract any change in the magnetization vector.

Recent research on magnetic nano-structure shows that the current flowing through these devices generates spin waves, layer switching, and a torque on the magnetization vector.

In 1996, Slonczewski stated that spin-polarized electrons in magnetic multilayers experience a change in their angular momentum, resulting in a torque applied to the magnetization vector called spin-transfer torque[80, 81]. A torque term should be added to the right-hand side of the previous equation to include this effect, and this term is given by [82]:

$$\overrightarrow{T_{spin}} = -\frac{\gamma\eta(\theta)\hbar}{2etM_S^2A} I.\left(\vec{M} \times \left(\vec{M} \times \vec{M}_{PL}\right)\right) \quad (4.17)$$

where $\hbar$ is the reduced Planck constant, t is the thickness of the free layer, A is the cross-sectional area, e is the electron charge, MPL is the magnetization vector of the pinned layer, I is the current passing through the spintronic memristor from the pinned layer to the free layer, and η is the spin torque efficiency.

After adding the torque term, the equation is called Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation. This equation is able to model the dynamic behavior of magnetic devices accurately.

The spin-transfer torque effect is exploited in MTJ device forming a device denoted by Spin-Transfer Torque Magnetic Tunneling Junction

(STT-MTJ). Semiconductor spintronic devices are preferable for their maturity and endurance [83].The main advantage of using the spin-transfer torque effect is that it requires lower current densities to achieve MTJ switching between P and AP states than all other existing techniques, which makes this technique preferable in high-density MRAMs [84].

The proposed model aims to overcome the drawbacks of current spintronic memristor models. The proposed model uses the LLGS equation to model the dynamical behavior of the spintronic memristor. Using the LLGS equation offers a more accurate representation of the memristor's dynamical behavior than previous models as they were using a simplified form of only the STT term from the modified LLG equation.

The LLGS equation deals with the free layer of the MTJ-based devices as one part that has a specific normalized magnetization vector m. The magnetization vector makes an angle θ with the easy axis (magnetization vector of the pinned layer). Thus, in the case of modeling spintronic memristors, The LLGS equation is applied to the DW part. In order to use the LLGS equation in modeling the spintronic memristor, the free layer is divided into three parts, a part with a magnetization vector parallel to the magnetization vector of the pinned layer, the domain-wall, and a part of a magnetization vector antiparallel to the magnetization vector of the pinned layer.

The proposed model also uses different equations that can represent all possible structures of spintronic memristors and links them to their physical parameters. The model included all the temperature-dependent parameters up to the author's knowledge. The domain wall width and its resistance value are also included in the model.

4.3.3. The Domain wall width and motion.

The switching between P and AP states in the spintronic memristor is based on the DW motion. The theory of operation is shown in Figure 4.5. The LLGS equation is used to calculate the domain-wall magnetization vector's relative angle to the easy axis of the memristor. If the STT effect exceeds the demagnetization field effect, the magnetization vector starts to rotate from AP to P state.

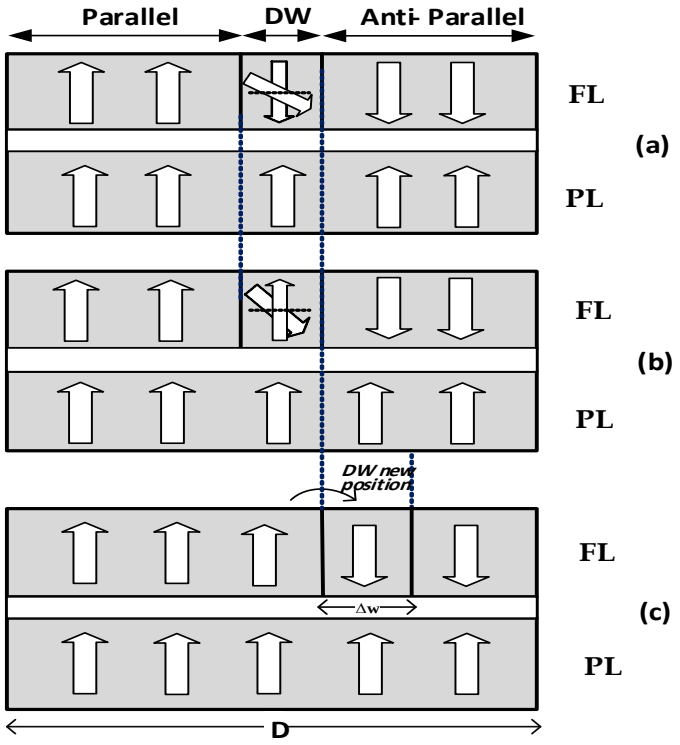


Figure 4.5 Domain-wall motion (a) Begin of rotation (b) DW fully switched (c) DW moved to the new position

When this magnetization vector reaches the parallel state as shown in Figure 4.5b, its width is added to the parallel part of the free layer, and the domain-wall position moves to the next part reducing the antiparallel part width as shown in Figure 4.5c. The LLGS is applied again on the domain-

wall in its new position, and so on. The same theory works for the domain-wall when its magnetization vector rotates from P to AP state, but the motion here is in the reverse direction reducing the parallel part and increasing the antiparallel part.

The DW type of the spintronic memristor is assumed to be a Neel wall in which the magnetization vector rotates in the plane of transition as shown in Figure 4.5. The Neel type DW width can be calculated by [36, 85] :

$$\Delta w = \sqrt{\frac{2A_{ex}}{M_S H_K}} \tag{4.18}$$

where A_{ex} is exchange parameter and H_K is the easy anisotropy. The FL is divided into "*N*" domain-walls. Thus, the number of domain walls *N* in the FL strip equals:

$$\mathrm{N} = \frac{D}{\Delta w} \tag{4.19}$$

4.3.4. The CIP and CPP structures

The spintronic memristor can use either the CIP structure like the spintronic memristor proposed by Chen [13] or CPP structure like the one proposed by Miao Hu [8]. Figure 4.6a shows a spintronic memristor of CIP structure. The CIP spintronic memristor can be divided into three parts, *P*, *DW*, and *AP*. Thus, the CIP spintronic memristor can be considered equivalent to the three parts connected in series as shown in Figure 4.6b. This is the same assumption used by Chen model, except that he only takes the P and AP parts.

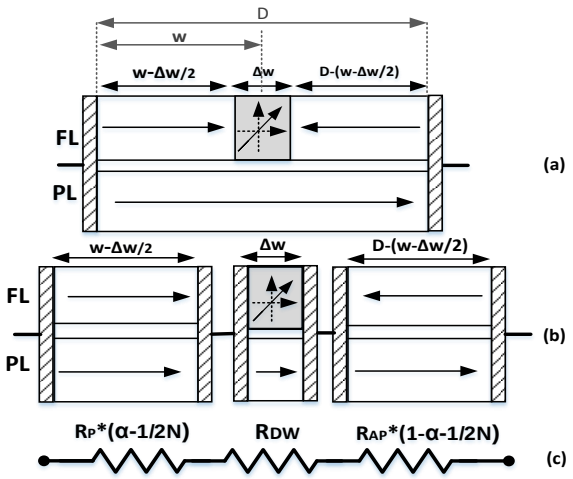


Figure 4.6 CIP Spintronic Memristor (a) Basic cell (b) free layer division (b) equivalent circuit.

Figure 4.6c shows the equivalent circuit that is used by the proposed model for the spintronic memristors with a CIP structure. The first resistor R_P * *(α-1/2N)* is the equivalent resistor of the P part. The DW part has a resistance of R_{DW}, and it will be calculated according to whether the memristor type is GMR or TMR. The AP part is modeled by the resistance R_{AP}*(1-α-1/2N). The resistance R_P is the equivalent resistance of the spintronic memristor when the entire FL is in the P state. The derivation of this model is straightforward, as for a resistor *R*, $R=\rho L/A$, then the ratio of the P part resistance to the total resistance is $R_{p\_part}/R_P=L_{p\text{-}part}/L_{tot}$. Thus, the P part resistance is given by:

$$R_{P\_part} = R_P * \frac{w-\frac{\Delta w}{2}}{D} = R_P * \left(\alpha - \frac{1}{2N}\right) \qquad (4.20)$$

where w is the DW position at the center of the DW which has a width of Δw, and α = w/D.

Similarly, the AP part equivalent resistance is:

$$R_{AP\_part} = R_{AP} * \frac{D-\left(w-\frac{\Delta w}{2}\right)-\Delta w}{D} = R_{AP} * \left(1-\alpha-\frac{1}{2N}\right) \quad (4.21)$$

where the antiparallel resistance R_{AP} is calculated from the following equation:

$$R_{AP}(V) = R_P * (1 + TMR(T,V)) \quad (4.22)$$

where *TMR (T, V)* is the tunneling magnetoresistance ratio as a function of temperature and voltage, and its value is calculated in the next subsection.

The total memristance can be calculated as follows:

$$M(\alpha) = R_P * \left(\alpha-\frac{1}{2N}\right) + R_{DW} + R_{AP} * \left(1-\alpha-\frac{1}{2N}\right) \quad (4.23)$$

Using the same idea, the equivalent parallel resistance of the DW R_{P_DW} is calculated as follows:

$$R_{P\_DW} = R_P * \frac{\Delta w}{D} = \frac{R_P}{N} \quad (4.24)$$

The R_{P_DW} value will be used in the calculation of the DW resistance R_{DW}.

Figure 4.7a shows a spintronic memristor of CPP structure. The CPP memristor can be divided into three parallel parts, P, DW, and AP. In contrast to the CIP structure, the devices area is divided into the three parts instead of the length. Thus, $R_{p\_part}/R_P = A_{tot}/A_{p\_part}$. Thus, the P part resistance equals:

$$R_{P\_part} = R_P * \frac{D}{w-\frac{\Delta w}{2}} = \frac{R_P}{\left(\alpha-\frac{1}{2N}\right)} \quad (4.25)$$

Similarly, the AP part equivalent resistance is:

$$R_{AP\_part} = R_{AP} * \frac{D}{D-\left(w-\frac{\Delta w}{2}\right)-\Delta w} = \frac{R_{AP}}{\left(1-\alpha-\frac{1}{2N}\right)} \quad (4.26)$$

The total memductance $W(\alpha)$ can be calculated as follows:

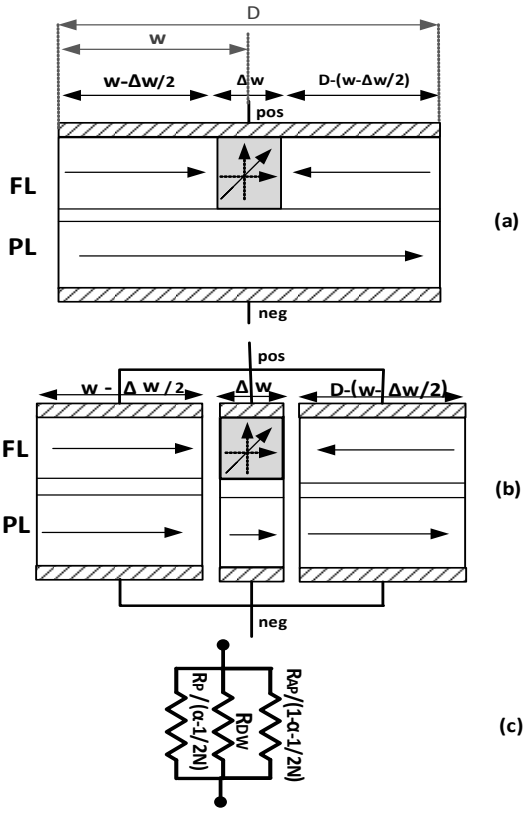


Figure 4.7 CPP Spintronic Memristor (a) Basic cell (b) free layer division (c) the equivalent circuit

$$W(\alpha) = \frac{\left(\alpha - \frac{1}{2N}\right)}{R_P} + 1/R_{DW} + \frac{\left(1 - \alpha - \frac{1}{2N}\right)}{R_{AP}} \tag{4.27}$$

where $W(\alpha) = 1/M(\alpha)$.

The area of the DW is ($1/N$) times of the total FL area. Thus, the R_{P_DW} in the CPP structure is calculated as follows:

$$R_{P\_DW} = R_P * \frac{D}{\Delta w} = N R_P \tag{4.28}$$

4.3.5. Thermal Dependent parameters

The magnetic parameters have a substantial dependence on the temperature. Thus, including the thermal dependence of the magnetic

parameters is of a great importance to study the behavior of spintronic memristors. In the proposed model, the effect of temperature fluctuations on the saturation magnetization, the polarization, and the tunneling magnetoresistance ratio are included.

The temperature dependent magnetization saturation can be calculated as follows:

$$M_s(T) = M_{s0}\left(1 - \frac{T}{T_C}\right)^{\beta} \tag{4.29}$$

where M_{S0} is the magnetization saturation at absolute zero, T_C is the Curie temperature, and β is a material dependent critical exponent.

The zero-voltage temperature dependent spin-polarization can be calculated as follows:

$$P_s(T) = P_0\left(1 - \alpha_{SP} T^{3/2}\right) \tag{4.30}$$

where P_0 is the spin-polarization at absolute zero, and α_{SP} is a material and dependent geometry constant. The zero-voltage *TMR* is related to the spin-polarization as follows:

$$TMR_0(T) = \frac{2\,{P_s}^2(T)}{1-{P_s}^2(T)} \tag{4.31}$$

The voltage-dependent *TMR* is then calculated as follows:

$$TMR(T,V) = \frac{TMR_0(T)}{1+\left(\frac{V}{V_h}\right)^2} \tag{4.32}$$

The voltage-dependent spin-polarization is then calculated as follows:

$$P_S(\mathrm{T},\mathrm{V}) = \sqrt{\frac{TMR(\mathrm{T},V)}{TMR(T,V)+2}} \tag{4.33}$$

4.3.6. In-plane anisotropy and perpendicular-to-plane anisotropy.

The in-plane anisotropy (IPA) and perpendicular-to-plane anisotropy (PPA) describe the direction of the anisotropy compared to the device geometry. In the IPA shown in Figure 4.8a, the anisotropy is parallel to the FL-PL interface. On the other hand, the anisotropy in PPA is perpendicular to the FL-PL interface as shown in Figure 4.8b.

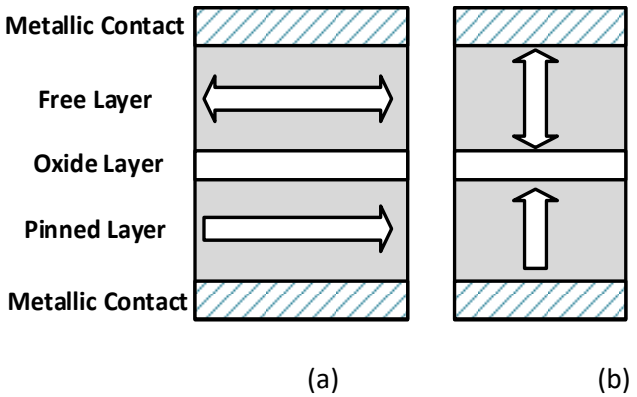


Figure 4.8 Spintronic Memristor (a) IPA structure (b) PPA structure

Comparing IPA and PPA structures shows that the PPA structure requires less critical current than the equivalent IPA structure. The critical current of IPA and PPA structures is given in (4.34), and (4.35), respectively [86]. The ratio between the critical current of the IPA devices to the PPA devices is $(H_K+2\pi M_S)/H_K$. Typically, $M_S>H_K$, and so the PPA devices have lower critical currents than IPA devices which enable PPA devices to be used in more advanced technologies with smaller feature sizes, and thus providing higher densities than IPA devices. On the other hand, the IPA devices can provide higher ratios between the parallel and antiparallel resistances, which give better noise margins. It should be noted that the STT effect is more effective on PPA devices than IPA devices [79].

The proposed model includes the critical currents described in (4.34) and (4.34) based on whether the memristor type is IPA or PPA.

$$I_{C0\,(IPA)} = \frac{2e\alpha_g M_S Vol\,(H_K+2\pi M_S)}{\hbar\eta(\theta)} \tag{4.34}$$

$$I_{C0\,(PPA)} = \frac{2e\alpha_g M_S Vol\,H_K}{\hbar\eta(\theta)} \tag{4.35}$$

where Vol is the FL volume, and $\eta(\theta)$ is the polarization efficiency and it is given by [87]:

$$\eta(\theta) = \frac{P_S}{1+P_S{}^2\cos(\theta)} \tag{4.36}$$

Equations (4.34) and (4.35) show that the critical current of the spintronic memristor depends on $\eta\,(\theta)$ which is a function of the angle θ between the magnetization vectors of the FL and PL. This leads to an important deduction that the critical current of the spintronic memristor in the case of P-AP switching differs than the critical current in case of AP-P switching. In case of the P-AP switching, $\theta=0^o$ and the polarization efficiency becomes $\eta_{P\text{-}AP} = \eta\,(0^o) = P_S / (1+P_S^2)$. Similarly, the AP-P switching has a polarization efficiency of $\eta_{AP\text{-}P} = \eta\,(180^o) = P_S / (1-P_S^2)$. Thus, the switching from AP to P states is easier than switching from P to AP states. This is physically understandable, as the FL magnetization vector tends to align with the easy axis. The ratio between the critical currents of P-AP and AP-P switching is:

$$\frac{I_{co_{P-AP}}}{I_{co_{AP-P}}} = \frac{1-P_S{}^2}{1+P_S{}^2} \tag{4.37}$$

4.3.7. The GMR- and TMR-based spintronic memristors

The proposed model uses the following equation to calculate the parallel resistance of the TMR-based devices [88]:

$$R_P = \frac{t_{ox}}{(F.\varphi^{1/2}.Area)}\, e^{(Coef.t_{ox}.\varphi^{1/2})} \tag{4.38}$$

where φ is the average potential barrier height of the oxide material, *coef* is a fitting parameter, and F is a fitting parameter corresponding to t_{ox} and depends on the material composition of the spintronic memristor layers.

The domain wall resistance as a function of θ is then calculated from the Julliere model [89] as follows:

$$R_{DW}(\theta) = \frac{2\, R_{P\_DW} \parallel R_{AP\_DW}}{1 + P_S^2 \cos(\theta)} \tag{4.39}$$

where R_{P_DW} is calculated from (4.24) for CIP devices and from (4.28) for CPP devices in both GMR- and TMR-based memristors. R_{AP_DW} is calculated from (4.22) as a function of R_{P_DW} and *TMR (T, V).*

In the case of the GMR-based spintronic memristor, the parallel resistance of the device is calculated from the sheet resistance R_{eL} as in Chen model [36]:

$$R_P = R_{eL}\,(D/z) \tag{4.40}$$

where D, z is the device's length and width respectively as in the GMR-based spintronic memristor shown in Figure 2.18.

The DW resistance of the GMR-based memristors is then calculated from the following equation [90]:

$$R_{DW}(\theta) = R_{P\_DW} + \left(R_{AP\_DW} - R_{P\_DW}\right)\left(\frac{1-\cos(\theta)}{2}\right) \tag{4.41}$$

4.3.8. Verilog-A Description

Figure 4.9 shows the flowchart of the flow of the proposed model. The designer should first specify the memristor type whether it is GMR/TMR, CIP/CPP, and IPA/PPA. Then the physical parameters, magnetic device constants, and device dimensions are provided by the designer.

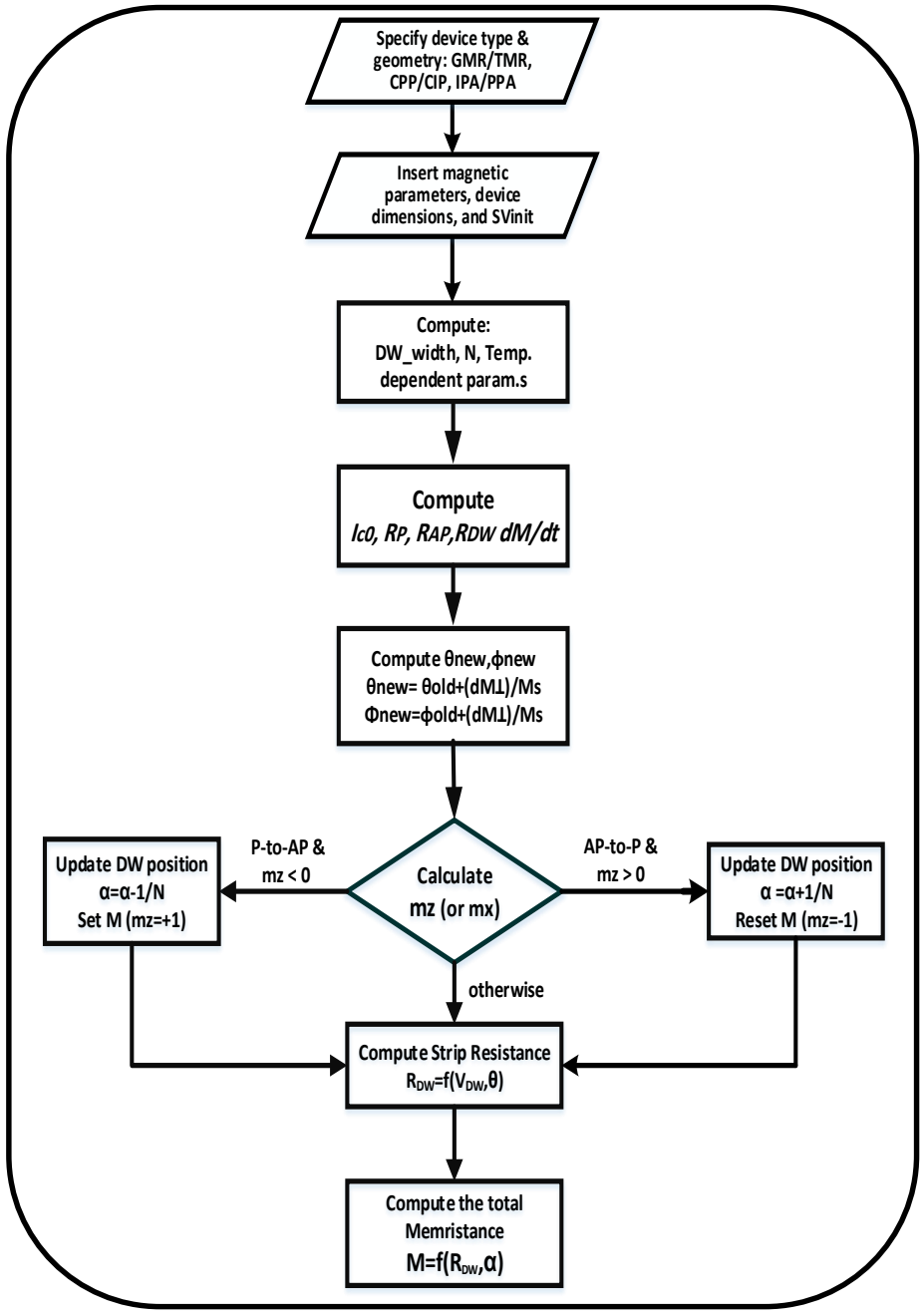


Figure 4.9 Verilog-A Flow Chart of the proposed model

After that, the Verilog-A routine computes temperature dependent parameters, DW width, and the number of DWs N. According to the device type, the values of R_P, R_{AP}, I_{C0}, and initial R_{DW}. The LLGS equation is applied to the DW and the rate of change of the normalized magnetization vector $d\boldsymbol{m}/dt$ and the angle θ are calculated. Then the value of the magnetization vector is updated. If the value of the normalized magnetization-vector component (*mz* for PPA or *mx* for IPA) crosses the switching point between P and AP states, the position of the DW is updated. Otherwise, move to the next step to compute the DW resistance $R_{DW}(\theta)$, and the total memristance $M(\alpha)$.

The switching point is taken as *mz (or mx)=0*, as it is the middle point between P and AP states [91].

4.3.9. Simulation Results

The model is implemented by Verilog-A language and used with a SPECTRE-based CAD tool to study the behavior of the spintronic memristor under different stimulations and to show the main characteristics of the device. The Verilog-A code of the proposed model is provided in Appendix A. Table 4.1 lists the values of the dimensions and the main parameters, used in the simulations. Due to the absence of spintronic memristor's experimental data, these values were taken from implemented STT-MTJ devices as to be the closest to the spintronic memristors [82, 92].

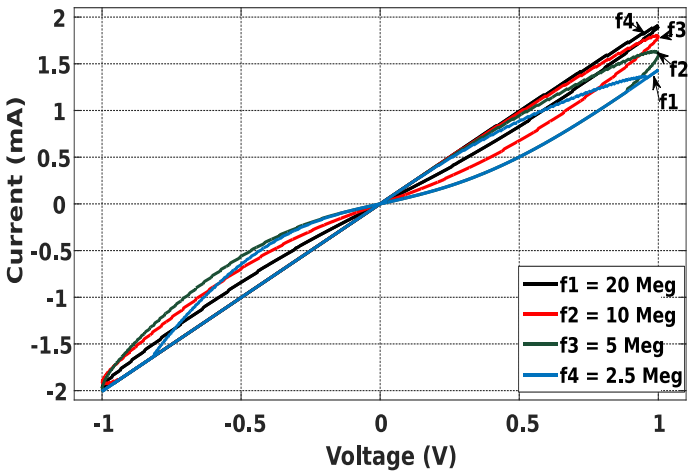
The general behavior of different geometries of spintronic memristors are similar. The TMR-based PPA spintronic memristor is chosen through our simulations because it might be the most promising type of spintronic memristor.

TABLE 4.1 Constant and Parameters in The Proposed Model

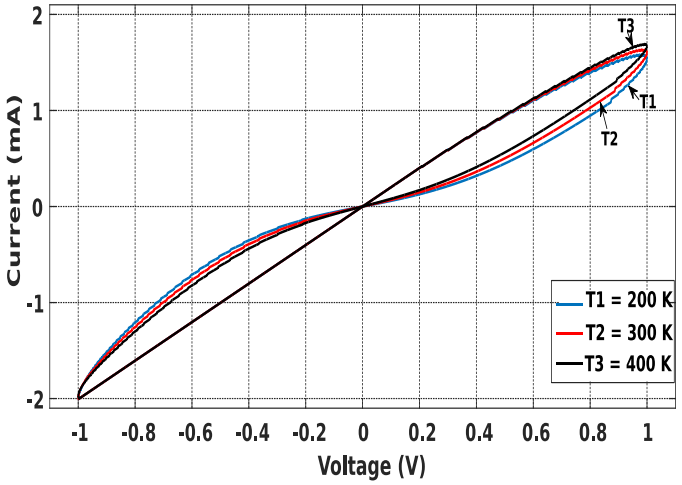
	Physical constants	
e	*Elementary charge (C)*	*1.602x10^{-}*
$\hbar$	*Reduced Planck constant*	*1.054x10^{-}*
	Material parameters	
M_{s_nom}	*Magnetization saturation at room temperature*	*1050*
H_K	*Easy anisotropy (O_e)*	*250*
A_{ex}	*Exchange parameter*	*1.8 x10^{-11}*
α_g	*Gilbert damping*	*0.002*
γ	*Gyromagnetic ratio*	*1.7608x10^{-}*
V_h	*TMR voltage dependence*	*0.5*
T_C	*Curie temperature*	*1420*
α_{sp}	*P_s thermal dependence*	*2x10^{-5}*
β	*M_s thermal dependence*	*0.4*
F	*TMR-based R_P fitting*	*409405*
	Model parameters	
D	*Length (nm)*	*500*
h	*Thickness (nm)*	*1.5*
z	*Width (nm)*	*60*
t_{ox}	*Oxide thickness (nm)*	*0.85*
R_{eL}	*Low sheet resistance*	*50*

Figure 4.10a shows the current-voltage (I-V) characteristics of the spintronic using a 1 V sinusoidal input voltage. The I-V characteristics are studied under different input frequencies 2.5, 5, 10, and 20 MHz. The curve hysteresis reduces when the signal frequency increases as expected for any memristor device.

Figure 4.10b shows the I-V characteristics of the spintronic memristor when applying a sinusoidal input of *1V* under different temperature values, 200^o, 300^o, and 400^o K.



(a)



(b)

Figure 4.10 Proposed model driven by a sinusoidal input of 1 V (a) for different frequencies (b) for different temperatures.

The figure shows that the curve hysteresis reduces when the temperature increases. Thus, we can conclude from this figure that increasing temperature reduces the unique hysteresis feature of the memristor, making it a little closer to the resistor-like behavior.

In Figure 4.11, a biased sinusoidal voltage excitation is applied on the spintronic memristor. A frequency of $f=20MHz$ and amplitude of $V_m = 0.8V$. A negative bias of -0.1V is added for the first three cycles and then a positive bias of +0.3V) is added for the next three cycles. In the first three cycles, the negative bias combined with the sinusoidal voltage causes the gradually increasing ripples. Another reason for the increasing ripples is that the switching from P to AP is slower than the AP to P switching due to the inherent trend of the magnetization vector to be aligned with the easy axis as mentioned. Thus to overcome this effect and force the devices to achieve gradually decreasing ripples, a bias of +0.3 V was needed in the second three cycles compared with only -0.1 V bias in the first three cycles.

The state variable switching between ON and OFF is shown in Figure 4.11. A *1 V* input pulse is used. As shown in Figure 4.12a, the change of the state variable depends on the DW mz switching which is calculated from the LLGS equation. Thus, for a full ON and OFF memristance switching, mz must achieve *N* switches ON or OFF respectively as shown in Figure 4.12b.

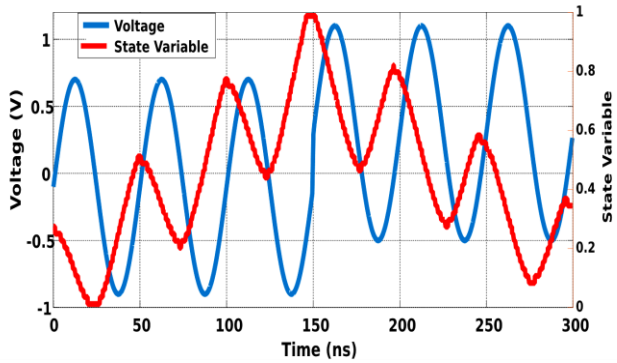


Figure 4.11 State Variable of a spintronic memristor driven by a biased sinusoidal voltage

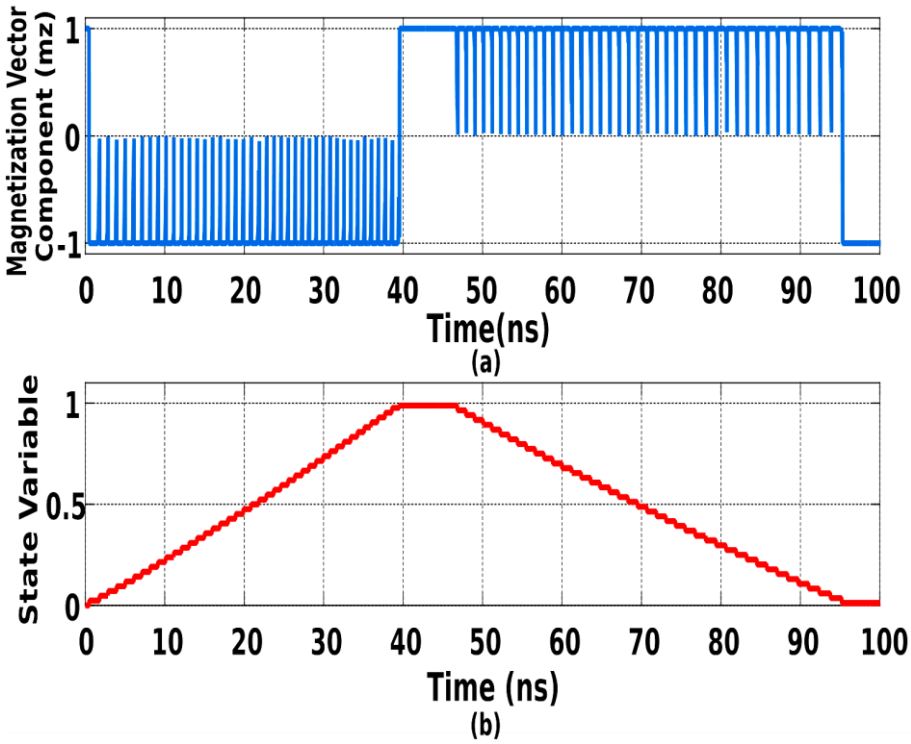


Figure 4.12 (a) Magnetization vector z-component (mz) (b) State Variable.

The value of the antiparallel resistance and thus the total memristance is a function of the applied voltage. The proposed model includes the TMR/GMR voltage dependence effect. Figure 4.13 shows the value of the antiparallel resistance for a sinusoidal applied voltage. As shown in this figure, the antiparallel resistance reaches its maximum value when the input voltage equals zero. Under zero applied voltage, the tunneling magnetoresistance $TMR\ (V=0) = TMR_0$ and the R_{AP} value is maximum. When the applied voltage reaches its positive or negative maximum (±1V), the tunneling magnetoresistance and the antiparallel resistance reach their lowest value: $TMR\ (V=\pm 1) = 0.2 * TMR_0$ and the R_{AP} value is minimum. Thus, reducing the operating voltage in spintronic memristor is preferable

in the design, as it increases the noise margin of the memristor in memory applications.

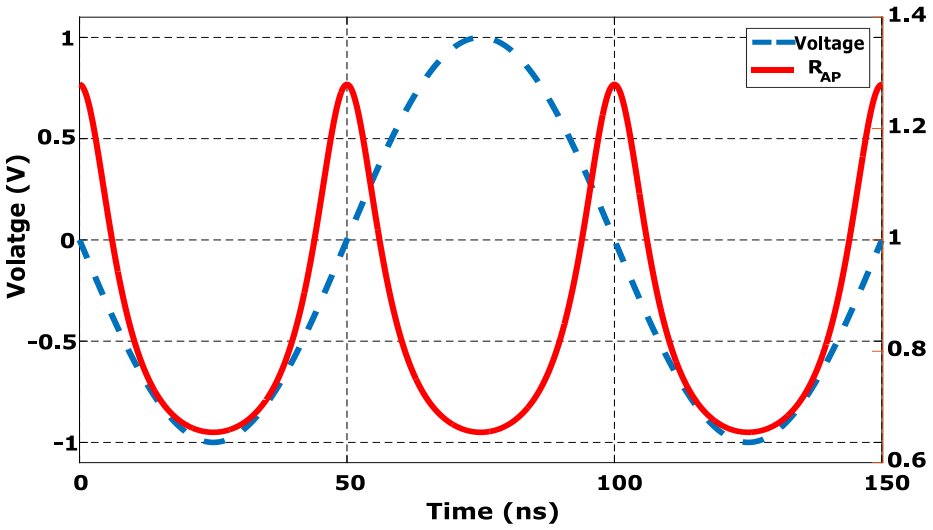
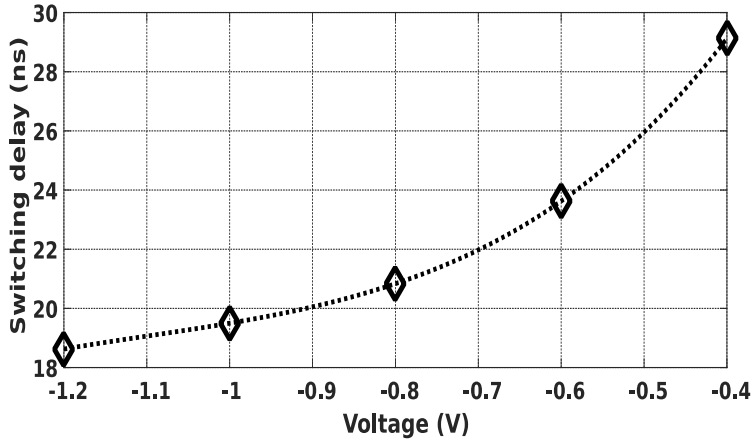
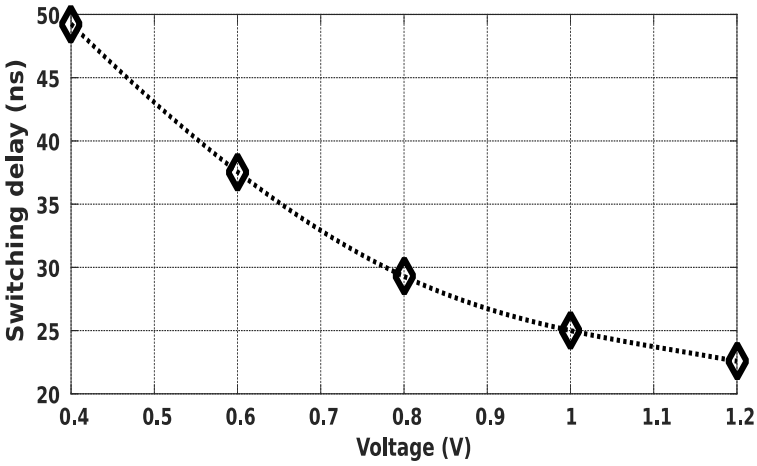


Figure 4.13 Antiparallel resistance for sin wave input (TMR0=2)

Figure 4.14 shows the switching delays of the spintronic memristor versus the applied voltage. The switching delay decreases with voltage increment. The designer needs to achieve a compromise between decreasing the applied voltage to increase *TMR (V)* and increasing it to decrease switching delay. In Figure 4.14a, a negative voltage signal is applied leading to AP-to-P switching. In Figure 4.14b, a positive voltage signal is applied leading to P-to-AP switching. The figure shows the clear asymmetry of the switching delay. At ±0.4V for example, the AP-to-P switching requires only 29.5ns compared to 49.5ns for the P-to-AP switching.



(a)



(b)

Figure 4.14 Switching delay (a) AP to P switching (b) P to AP switching

4.3.10. Model Verification

In 2016, a paper published by Steven Lequeux et al. provided the first realization of a spintronic memristor [93].This is the first experimental achievement of a spintronic memristor up to the author knowledge. Figure 4.15 shows a comparison between Miao Hu model and the proposed model fitting to the current-memristance relationship. The reason for choosing

Miao Hu model for the comparison is that this spintronic memristor is a TMR-based memristor. The proposed model shows better fitting to the experimental data. The first reason behind this is the clear voltage dependency of the TMR and thus the antiparallel resistance. The second reason is the ability to use two different critical currents for the positive and negative voltages in the proposed model. It should be noted that some values in Table 1 do not apply to this fitting. The values that are used in this fitting are $R_P = 37\ \Omega$, and $TMR=0.84$. The device dimensions are (1000*100*2.2 nm3), which fit the provided experimental data.

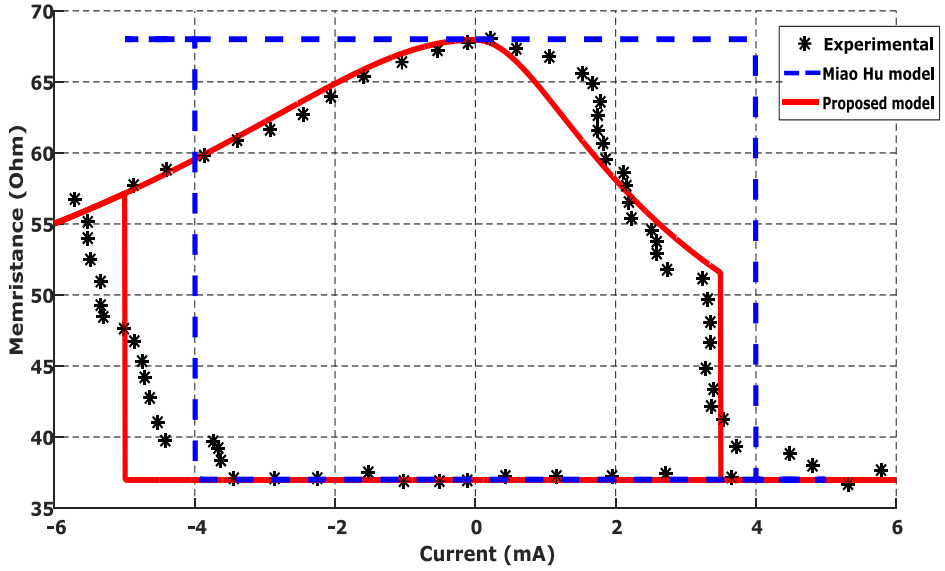


Figure 4.15 Resistance as a function of current for the experimental data, Miao Hu model, and the proposed model

4.3.11. Memristor-based memory cell

The memristor-based memories might be the most promising application for spintronic memristors. The memory read/write operations are discussed here as a case study of the proposed model. The read/write circuit used here is provided in [15], and it is shown in Figure 4.16. The

write operation is simply achieved by applying a positive pulse of 1V to write logic '0', or a pulse of *-1V* to write logic '1'. Figure 4.17 shows the simulation results of the write operation.

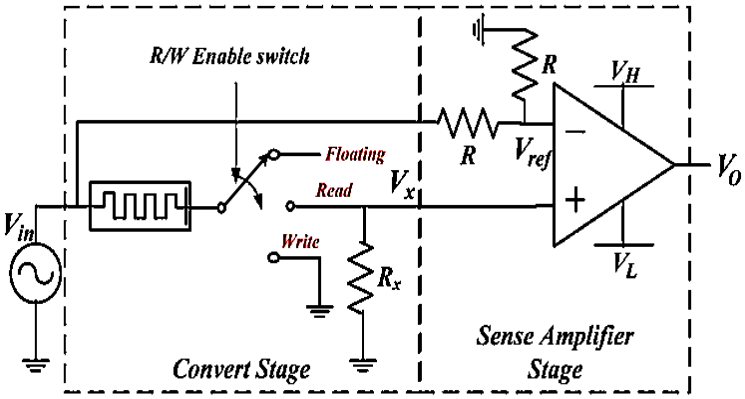


Figure 4.16 Yenpo R/W circuit [15].

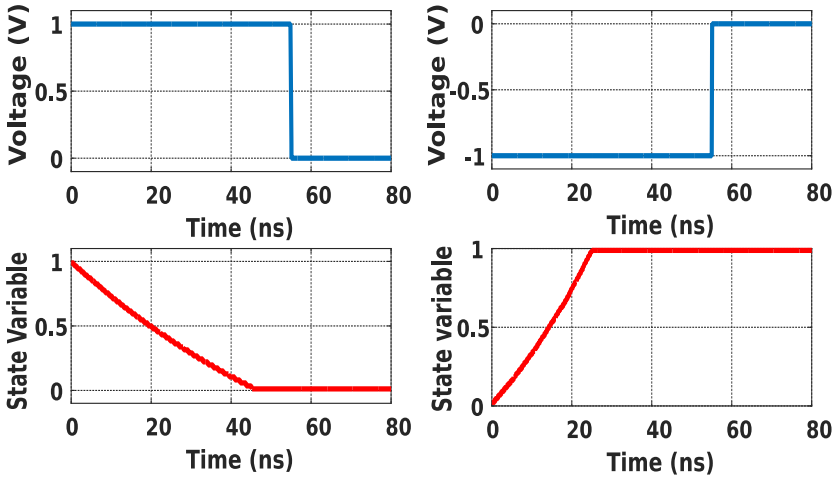
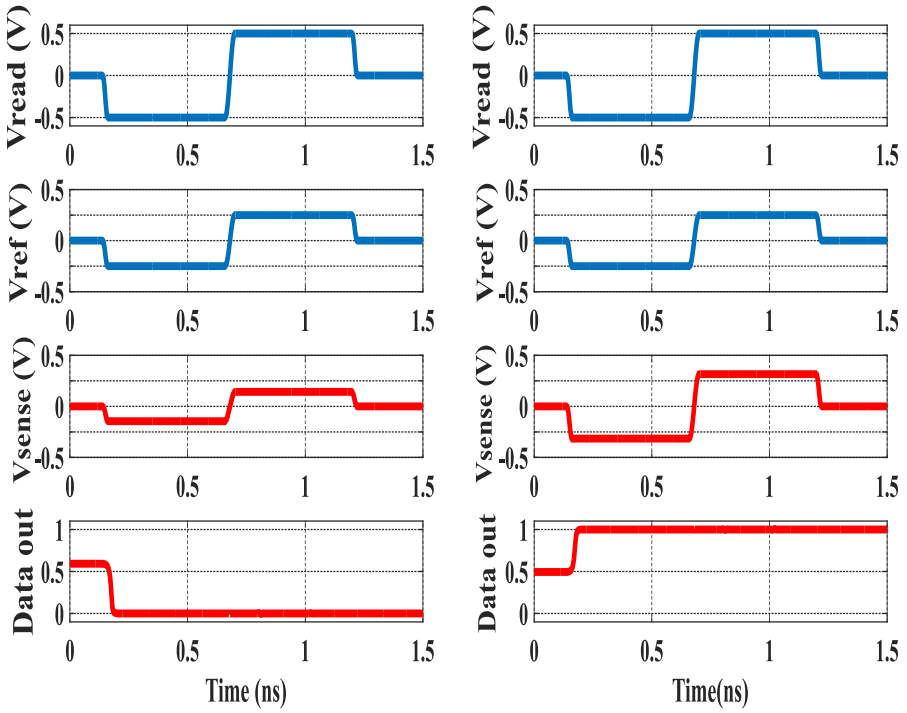


Figure 4.17 Write operation (a) Logic '0'((b) Logic '1'.

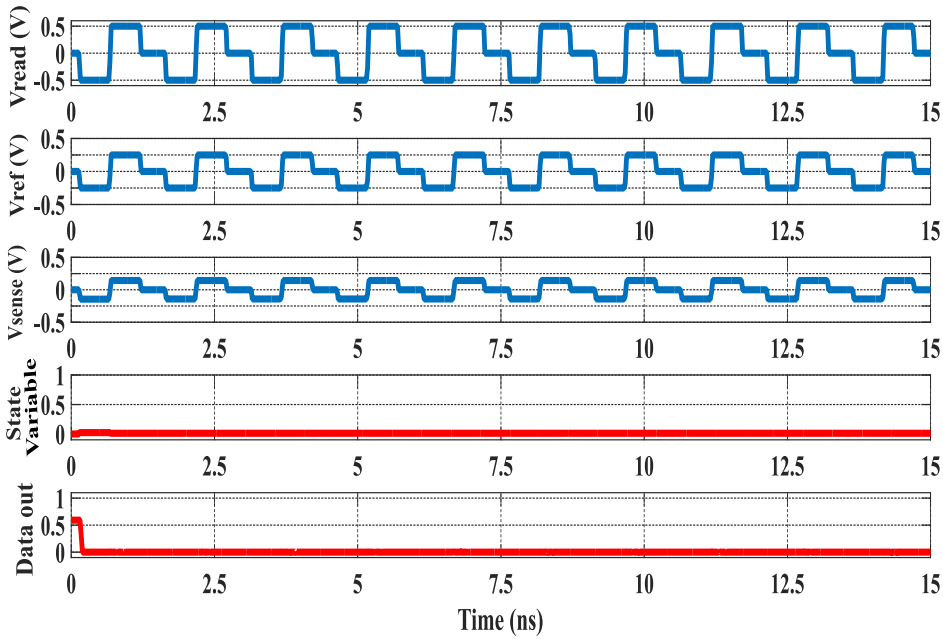
The simulation results of the read operation for one cycle is shown in Figure 4.18. The theory of the circuit depends on applying a read voltage signal of equivalent positive and negative pulses to cancel the effect of each

other. The output data is sensed during the positive reading pulse and latched at the output until the next cycle. Figure 4.19 shows the memristor's state and the data out for successive reading pulses. As shown in the figure, there is no disturbance of the stored data. The reason is that the reading pulse is chosen to be narrower than the lowest pulse width that could produce a change in the memristor state. The amplitude of the reading pulse is $V_m=0.5V$ at which the memristor need about $52ns$ for a full AP-to-P switching. The no. of DWs is $N=43$. Thus, for only one DW switch, a pulse duration of 1.21ns is needed which is clearly larger than the reading pulse duration. Thus, there is no data disturbance for multiple reading cycles.

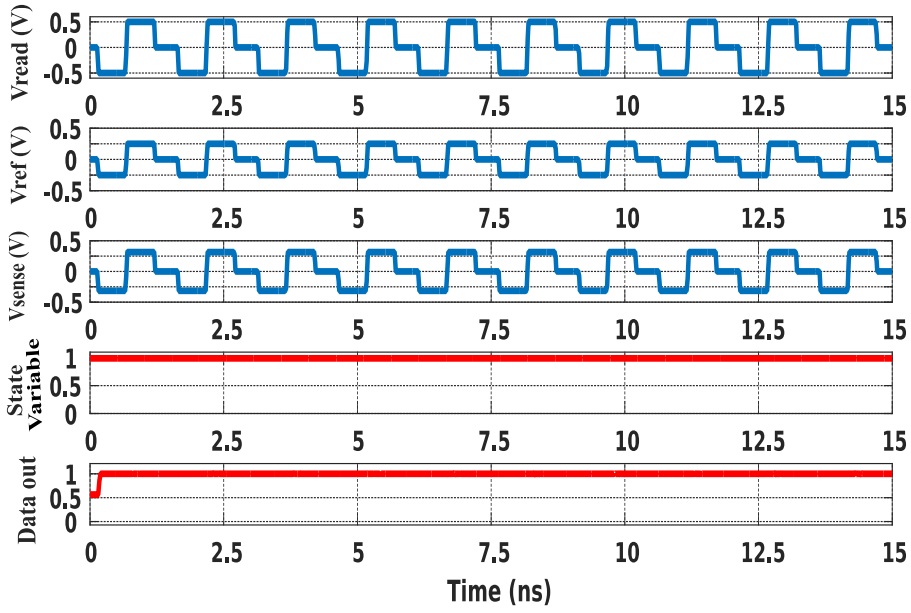


(a) (b)

Figure 4.18 Read operation one cycle (a) Logic '0' (b) Logic '1'.



(a)



(b)

Figure 4.19 Read operation successive cycles (a) Logic '0' (b) Logic '1'.

4.3.12. LLGS Model Summary

The LLGS model is the first model that represents the dynamical behavior of the spintronic memristor using the LLGS equation. Chen, Miao Hu, and TFA models only take one term of a modified LLG equation and deduced approximate DW speed from it. The proposed model uses suitable equations to model different types of spintronic memristors like GMR/TMR, CPP/CIP, and PPA/IPA as a function of their physical parameters. The proposed model is also the first model that includes the TMR/GMR voltage dependence in spintronic memristor modeling. The model includes thermal dependent parameters to model the effect of thermal fluctuations on the device's behavior. Both voltage-dependent and thermal-dependent effects are of a great importance in studying the actual behavior of spintronic memristors in circuit design. The model is verified to an experimental data of a spintronic memristor, and it showed much better fitting compared to existing models. A case study memristor-based read/write memory circuit is used to verify the model. The model is written using Verilog-A, and it is integrated with SPECTRE-based CAD tool.

4.4. Comparison of Spintronic Memristor Models

Table 4.2 provides a comparison between previous models and the proposed model. Unlike previous models, which partially depends on a modified LLG equation, the proposed uses the LLGS equation to model the dynamical behavior of the spintronic memristor. The proposed model uses physic equations to model different types of spintronic memristors as a function of its physical parameters. The proposed voltage and thermal dependent parameters. This can be used efficiently to study the effect of thermal fluctuations of spintronic memristors. However, the proposed model needs a longer simulation time, as it requires smaller time step to

keep up with the fast changes in the magnetization vector when it is modeled by the LLGS equation.

TABLE 4.2 Comparison Between Previous Models and The Proposed Models.

Model	Chen Model [36]	Miao Hu Model [8]	TFA Model	LLGS Model
LLGS-based	partially	partially	partially	Yes
Valid for different geometries	No	No	No	Yes
Material parameters' dependence	partially	partially	partially	Yes
Thermal dependence	No	No	partially	Yes
TMR/GMR voltage dependence	No	No	No	Yes
Simulation time	Shorter	Shorter	Shorter	Longer

Chapter 5: Memory Design Using Memristors

The memory applications might be the most important memristor applications. The inherent non-volatility of the memristor combined with its high scalability make the memristor technology a strong candidate for the future of memory circuit design. In this chapter, an analysis of spintronic memristor properties using the TFA model is provided. The memory design is also investigated using this model. Then, a read/write circuit that offers a sensational area reduction is proposed and compared with existing read/write circuits.

5.1. Properties of Memristors Using (TFA) Model

The memristance of the spintronic memristor can be written as a function of q by solving equations (2.15), (2.16), and (2.17) for a driving DC current large enough that $J>J_{cr}$ to be as follows:

$$M(q) = R_L + (R_H - R_L)\left(\frac{w_0}{D} + \frac{\Gamma_v}{h\,z\,D}q\right) \tag{5.1}$$

where $R_L=r_L.D$, $R_H=r_H.D$ are the memristor's overall ON and OFF resistances, w_0 is the initial value of the state variable.

Thus, the state variable can also be written as a function of q as follows:

$$w(q) = w_0 + \frac{\Gamma_v}{h\,z}q \tag{5.2}$$

Assume that the charge required to increase w to its upper limit ($w=D$) equals Q_{UP}, and the charge required to decrease w to its lower limit ($w=0$) equals Q_{LOW}. Then Q_{UP} and Q_{LOW} can be calculated as follows:

$$Q_{UP} = \frac{h\,z}{\Gamma_v} * (D - w_0) \tag{5.3}$$

$$Q_{LOW} = -\frac{h\,z}{\Gamma_v} w_0 \tag{5.4}$$

Thus, the normalized state variable $x=w/D$ can be written as follows:

$$x(q) = \frac{w(q)}{D} = \begin{cases} 1 & ; q \geq Q_{UP} \\ \left(\frac{w_0}{D} + \frac{\Gamma_v\, q}{h\, z\, D}\right) & ; Q_{LOW} < q < Q_{UP} \\ 0 & ; q \leq Q_{LOW} \end{cases} \tag{5.5}$$

5.1.1. Write Operation:

During the writing process, the designer ensures that $J>J_{cr}$. The charge needed to write a logic "0" starting from initial state $w_0=0$, or logic '1' starting from $w_0=D$ (Full Switch) is:

$$Q_{write\,0} = \frac{\Gamma_v D}{h\, z} \tag{5.6}$$

$$Q_{write\,1} = -\frac{\Gamma_v D}{h\, z} \tag{5.7}$$

Equations (5.6) and (5.7) are used to calculate the minimum time duration needed for the writing process under a specific driving DC current I_A by substituting with $Q_{write}= I_A.T_{WRITE}$.

$$T_{WRITE} = \frac{\Gamma_v}{h\, z}.D.I_A \tag{5.8}$$

5.1.2. Read Operation ($J < J_{cr}$)

The read operation is a quite difficult operation in memristor-based memory cells, as we need to apply read voltage or current without *disturbing* the stored data. This problem is even more difficult in case of spintronic memristor than solid-state memristor because the latter one has a much higher ON/OFF ratio and thus much higher R_H also. In case of the spintronic memristor, the designer wants to make a compromise between avoiding data disturbance and gaining enough voltage difference to be used

with the sense amplifier state. Thus, this operation might be done using current densities higher or lower than the critical value J_{cr}. In case of using $J>J_{cr}$, equations derived so far can be used to estimate the data disturbance *(Δw)*.

The second method is to use $J<J_{cr}$ which is the case discussed here. For the Wang model, this case does not cause any disturbance in the stored data. However, using TFA model shows that there is a disturbance caused by thermal fluctuation should be taken into consideration.

In spintronic memristors, there is no external applied field $(H(t)=0)$, and $\tau_{P\rightarrow AP}$ is reduced to :

$$\tau_{P\rightarrow AP} = \tau_0 \exp\left[\Delta\left(1-\frac{I_{read}}{I_{cr}}\right)\right] \qquad (5.9)$$

where $\Delta=(K_UV/K_BT)$ is considered as a *stability factor* to the memory circuit.

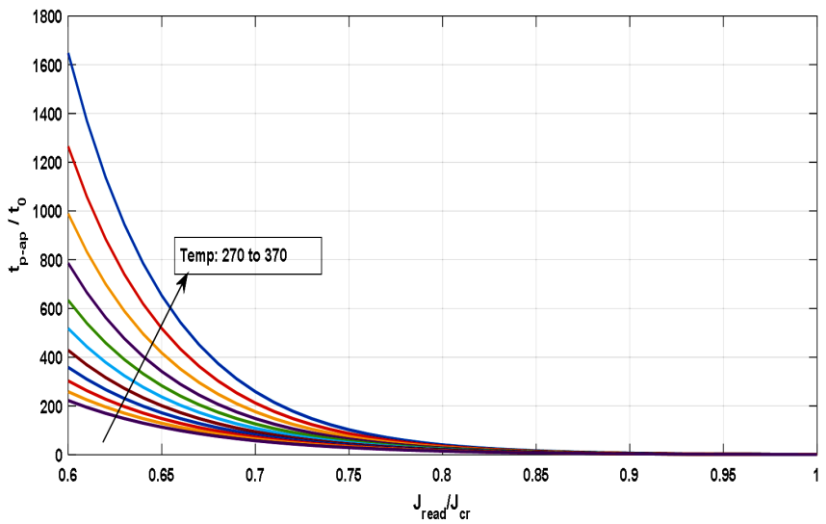


Figure 5.1 Normalized Neel-Brown relaxation time vs current density of reading pulses normalized to Jcr.

Figure 5.1 shows the normalized Neel-Brown relaxation time $\tau_{P\to AP}$ as a fuction of the reading pulses current density normalized to J_{cr}.

For a given design factor $P_{failure}$, let that:

$$f_P = ln\left(\frac{1}{1-P_{failure}}\right) \tag{5.10}$$

then

$$t_P = f_P\,\tau_{P\to AP} = f_P\,\tau_0 \exp\left[\Delta\left(1-\frac{J_{read}}{J_{cr}}\right)\right] \tag{5.11}$$

and

$$J_{eff} = \frac{J_{cr}\tau_0}{t_P} = \frac{J_{cr}}{f_P \exp\left[\Delta\left(1-\frac{J_{read}}{J_{cr}}\right)\right]} \tag{5.12}$$

The read disturbance Δw can be calculated by integrating (2.13):

$$\int_{w0}^{w} dw = \int_0^{T_{read}} \Gamma_v\, J_{eff}\, dt \tag{5.13}$$

$$\Delta w = (w - w0) = \frac{\Gamma_v\, J_{cr}}{f_P} \int_0^{T_{read}} \mathrm{e}^{\left(-\Delta\left(1-\frac{J_{read}}{J_{cr}}\right)\right)}\, dt \tag{5.14}$$

Thus, for a given factor $\frac{J_{read}}{J_{cr}}$, read disturbance equals:

$$\Delta w = \frac{\Gamma_v\, J_{cr}}{f_P}\, \mathrm{e}^{\left(-\Delta\left(1-\frac{J_{read}}{J_{cr}}\right)\right)}.T_{read} \tag{5.15}$$

Equation (5.15) shows an important design consideration; the read disturbance increases exponentially with the reading current for $J<J_{cr}$.

Using the previous equation to plot the relation between the read time and the read disturbance for different $\frac{J_{read}}{J_{cr}}$ gives Figure 5.2 and Figure 5.3.

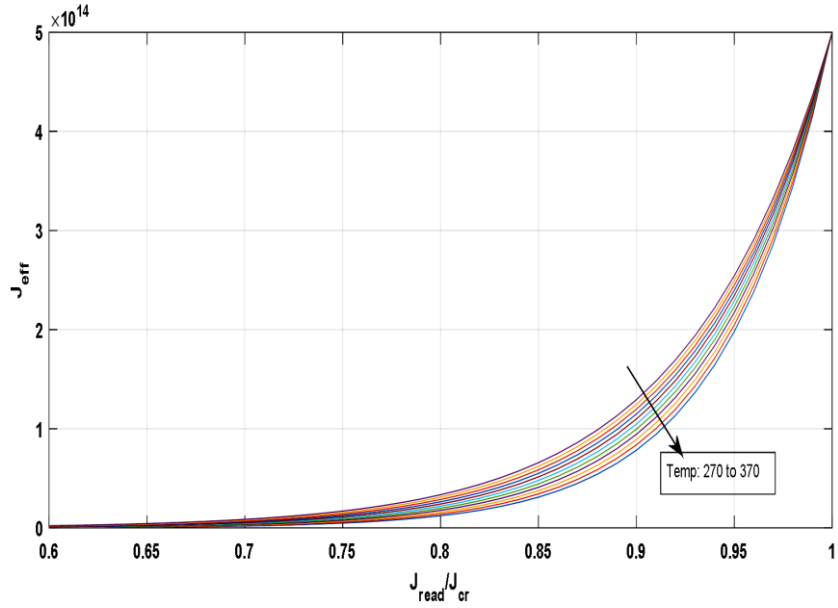


Figure 5.2 Effective current density (Jeff) versus normalized read current density to Jcr for different temperature values.

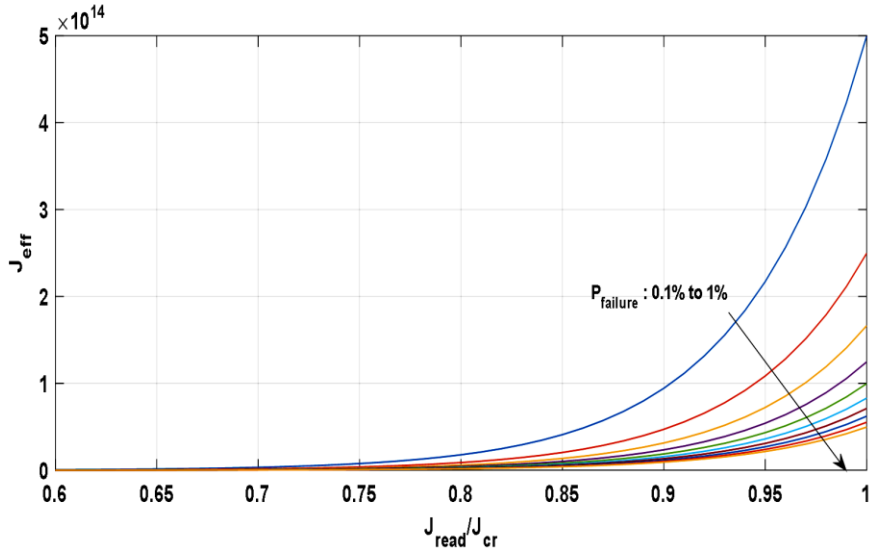
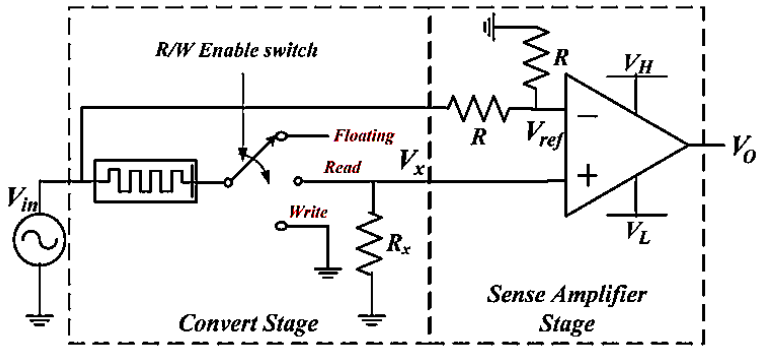


Figure 5.3 Effective current density (Jeff) versus normalized read current density to Jcr for different Pfailure values.

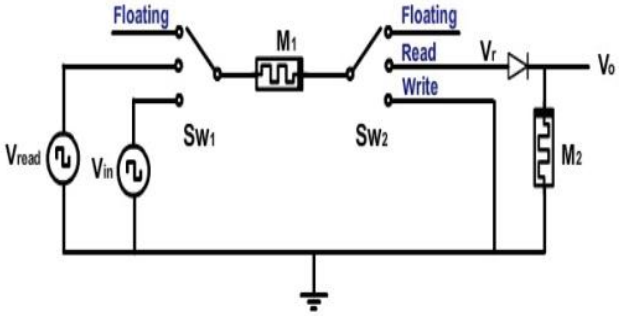
5.2. Proposed R/W Circuit

The Read/Write circuit in spintronic memristor memories needs a careful design to achieve larger sensed voltage difference, lower data disturbance, and smaller area as possible.

Figure 5.4 shows two realizations of Read/Write circuits proposed by Yenpo et al. [15] and El-Shamy et al. [47]. For both R/W circuits, the writing process is achieved simply by applying a DC write voltage for enough time T_{WRITE} to ensure full switching.



(a)



(b)

Figure 5.4 Two possible Read/Write circuits realizations (a) Yenpo R/W circuit[15] (b) El-Shamy R/W circuit [47].

For the R/W circuits shown in Figure 5.4a, the read process is achieved by applying the read pulse shown in Figure 5.5. The read pulse consists of two opposite polarities pulses with the same amplitude and width in order to compensate the read disturbance of each other. However, in case of pulse widths mismatch, a small read disturbance occurs which means that this circuit needs a periodic refreshment after a specific number of reading cycles. The reading process is achieved by comparing the voltage V_X which is a voltage divider between the memristor's resistance and a resistor $R_X = (R_H + R_L)/2$, with a reference voltage $V_{ref} = V_{read}/2$. The main disadvantage of this circuit is the large area required to fabricate the resistors.

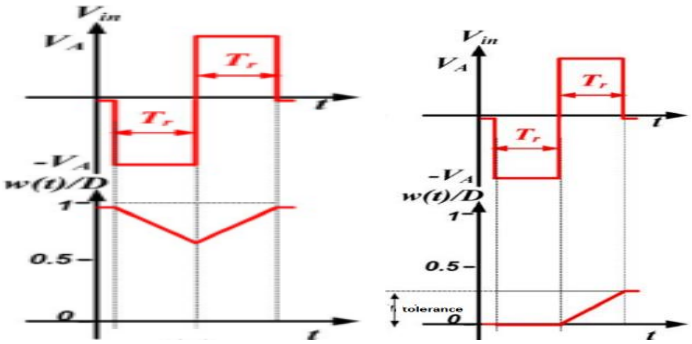


Figure 5.5 Read pulse when reading (a) logic '0' (w=D) (b) logic '1' (w=0) [15]

The second R/W circuit is shown in Figure 5.4b. This circuit was originally proposed for solid-state memristor in order to avoid the date disturbance of Yenpo R/W circuit. Note that this circuit is equivalent to the convert stage only. However, due to the small R_H of spintronic memristors compared to solid-state memristors, this advantage cannot be achieved in case of spintronic memristors as will be shown in the simulation results.

Figure 5.6 shows the proposed R/W circuit. In this circuit, the resistor R_X of Yenpo circuit is replaced by two parallel memristors (M_2, M_3) and they are kept in the OFF state. Thus, the equivalent resistance of M_2 and M_3 equals ($R_H/2$). Despite that, this value is slightly lower than R_X, it can give similar operation without any problems. Similarly, the two resistors of the sense stage are also replaced by two memristors (M_4 and M_5). This circuit works in the same manner of Yenpo R/W circuit. During floating and write operation, memristors (M_2, M_3, M_4, and M_5) are connected to a voltage (V_{DD}) to prevent accumulated mismatches that occur in the read operation. Memristor M_1 represents the memory cell, and it still affected by the read pulse mismatch like in Yenpo R/W circuit. The main advantage of this circuit is the great reduction in the circuit's area, as the memristor's area is much smaller than its equivalent resistor.

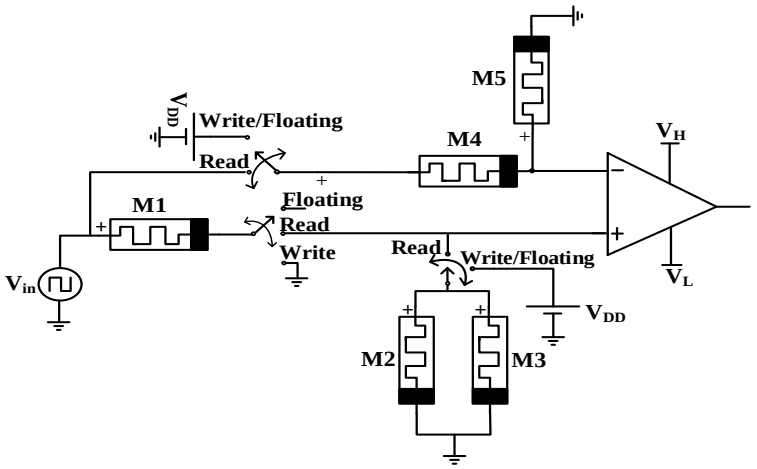


Figure 5.6 Proposed Read/Write Circuit.

5.2.1. Simulation Results

Memristor parameters are taken from [36]. The ON/OFF ratio is adjusted to 5, which is the largest ratio achieved in spintronic memristors

up to the author's knowledge [11]. The memristor dimensions are *(D=200nm, z=10nm, h=70A°).* The thermal stability factor $\Delta=50$.

Figure 5.7 shows the equivalent circuit of the R/W circuit during the write operation. The write operation is simply achieved by applying a positive pulse of *1V* to write logic '0', or a pulse of *-1V* to write logic '1'. Figure 5.8 shows the simulation results of the write operation.

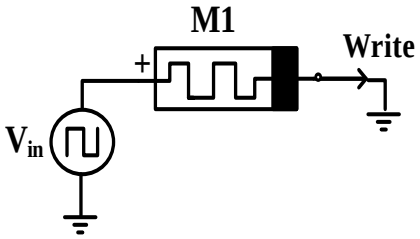


Figure 5.7 Equivalent R/W Circuit during the write operation.

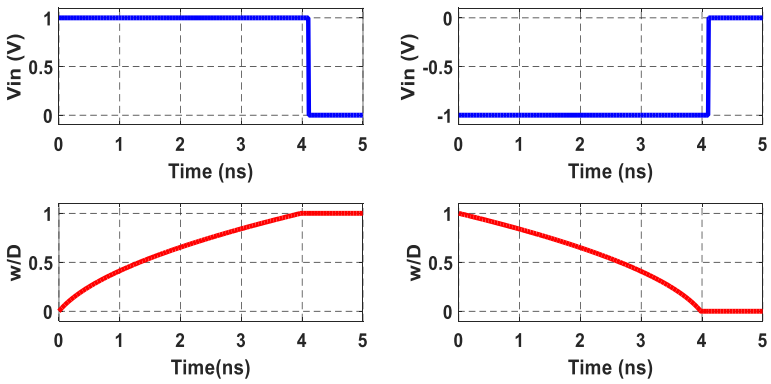


Figure 5.8 Write operation (a) Logic '0' (w/D=1) (b) Logic '1' (w/D=0).

Figure 5.9 shows the equivalent R/W circuit during the read operation. The simulation results of the read operation for one cycle is shown in Figure 5.10. In the case of *w/D=1*, the negative pulse compensates the positive pulse disturbance. If *w/D=0*, the first negative pulse cannot reduce

w/D as it is at minimum limit. However, this disturbance is not accumulative as the next read cycle $(w/D) > 0$ and thus next negative and positive pulses compensate each other. The data out is sensed during the positive reading pulse, thus the output is valid after the rising edge of the reading pulse as shown in Figure 5.10b. Figure 5.11 shows the memristor's state and the data out for successive reading pulses. As shown in the figure, there is no data disturbance as long as there is no pulse match in the reading voltage signal.

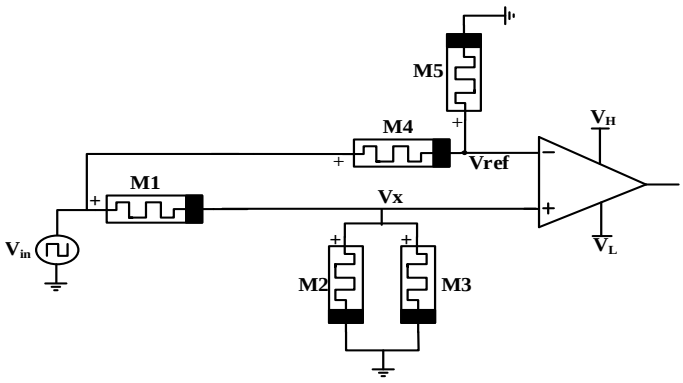
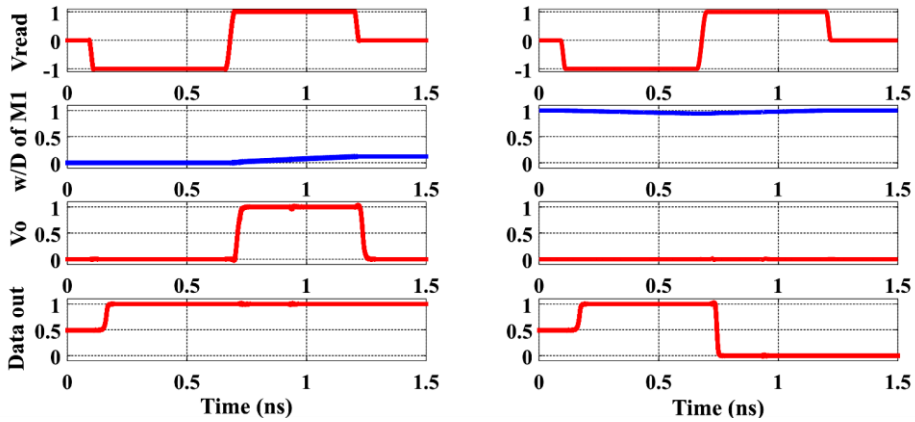
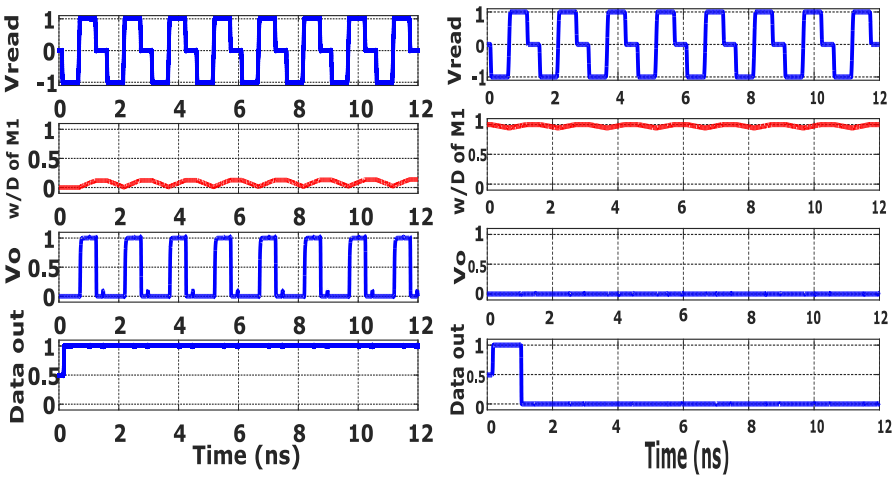


Figure 5.9 Equivalent R/W circuit during Reading operation.



(a) (b)

Figure 5.10 Read operation one cycle (a) Logic '0' (w/D=1) (b) Logic '1' (w/D=0).



(a) (b)

Figure 5.11 Read operation successive cycles (a) Logic '0' (b) Logic '1'.

5.2.2. Read Disturbance

The read disturbance is an important concern, as it defines the maximum allowed successive read cycles after which the data must be refreshed. Assume that the allowable margin for logic '1' is *w/D: 0 to 0.4*, and for logic '0' is *w/D: 0.6 to 1*. The effect of the reading pulse mismatch is similar in the Yenpo and the proposed R/W circuits.

Figure 5.12 shows the simulation results of successive reading cycles using El-Shamy R/W circuit and reading a logic '1'. In contrast with the results of this circuit using solid-state memristors, the stored data is disturbed after only 40 cycles. The high resistance state R_H of solid-state memristors is about 200 KΩ, and the voltage drop of the forward biased diode is about 0.7 V. The read current I_{READ} passes through memristors M_1 and M_2, where M_2 is kept always at R_H. In the worst case, if *M1* resistance equals R_L=*100*Ω, the current I_{READ} becomes:

$$I_{READ} = \frac{V_{READ} - V_D}{R_H} \approx \frac{0.3}{200 * 10^3} = 1.5\ \mu A \qquad (5.16)$$

This is a small value and thus no disturbance occurs in solid-state memristor. On the other hand, for the spintronic memristor; R_L=1KΩ, and R_H = 5 KΩ. I_{READ} ≈0.3/6K = 50 μA. This current is more than 30 times of the equivalent one in the solid-state memristor, which causes the significant read disturbance as shown in Figure 5.12. Note that this technique uses a positive read pulse only, which means that there is no disturbance in logic '0' successive reading.

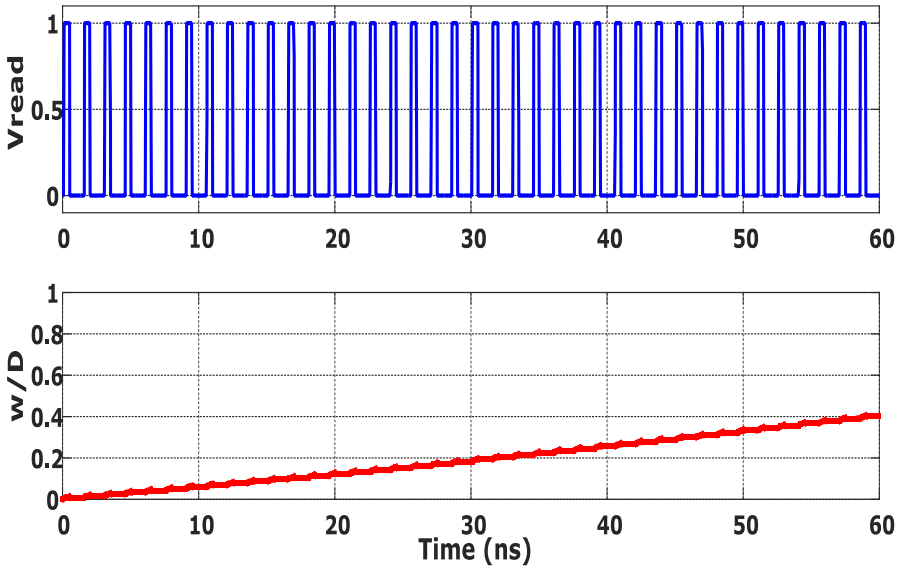


Figure 5.12 Read disturbance in El-Shamy R/W Circuit.

Figure 5.13 shows the read disturbance in the proposed circuit for a 10% pulse mismatch. The data is lost after 60 cycles. The logic '0' is not shown here also because the memristor becomes in the higher resistance state, which reduces the read disturbance. Thus, reading logic '1' is the worst-case condition.

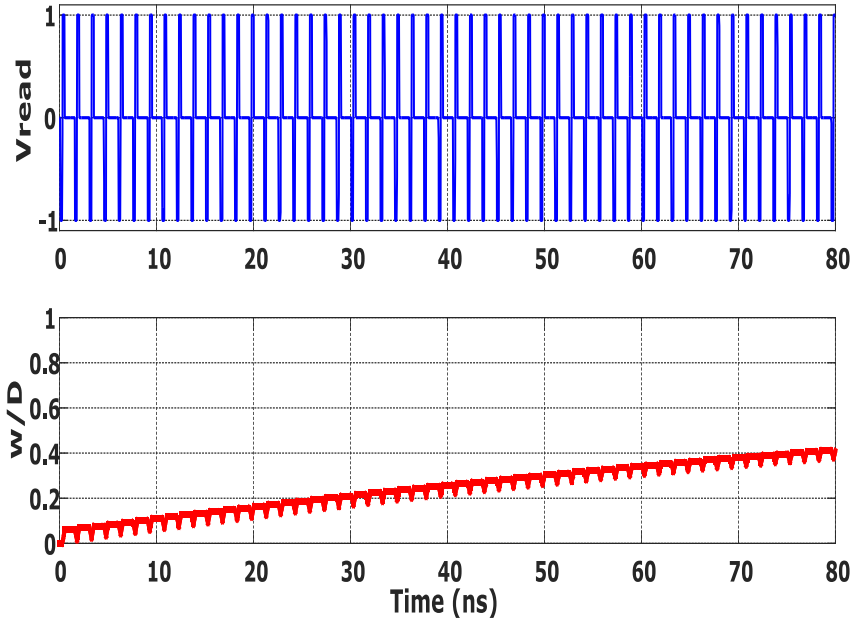


Figure 5.13 Read disturbance in the proposed R/W circuit for a 10% pulse mismatch.

Table 5.1 concludes the comparison between the three R/W techniques. The sense amplifier stage for El-Shamy is assumed the same as in Yenpo R/W circuit. The write power is the same in the three R/W because they are identical in the write operation. The comparator used in El-Shamy R/W circuit is twice the area of the compactor used in the other two techniques because the sensed voltage difference in El-Shamy is small. The small ON/OFF ratio provided a voltage difference of 60 mV (175 mV for Logic '1', and 115 mV for logic '0'). The resistors used in the sense stage should be reduced as possible to reduce their area. However, the tolerance of the N-diffusion resistor should be observed. For this design, $R=0.5\ K\Omega$ is chosen. The convert stage area of the proposed circuit is $1:10^5$ of Yenpo R/W and *1:500* of El-Shamy R/W circuits.

TABLE 5.1 Read/Write circuits comparison

Comparison Aspect	Dynamical [15]	El-Shamy [47]	Proposed
Power write '1'(µW)	270	270	270
Power write '0'(µW)	290	290	290
Power read '1'(µW)	56	260	52
Power read '0'(µW)	88	290	90
Convert stage area (µm^2)	800	4	0.008*
SA stage area (µm^2)	277	294	13
Sensed ΔV (mV)	370	60	355
***N* cycles before refreshment**	60	40	60

**The Memristor area is estimated as (Area=Length*Width)*

5.3. Design Insights

These are some design insights that can help the designer of memristive based memory circuits:

- The memristor can replace the resistor if we can make sure that the current moves in one direction or will compensate itself in two directions. This idea can reduce the area significantly.
- The circuit that works fine for a specific type of memristors does not necessarily give the same advantages to other memristor types as proved in El-Shamy read/write circuit. Thus, a separate analysis for each type is always required and this also shows the importance of having dedicated models for each type.
- The read process is a very challenging process in memristors especially for those of small ON/OFF ratios such as spintronic

memristors. Spintronic memristors with higher ON/OFF would be of a great benefit in memristive based memory design.

Chapter 6: Performance Comparison of Memristor types for main applications

6.1. Introduction

In this chapter, a comparative study of different memristor types for some well-known circuits/topologies is provided. The aim of this chapter is to study the effect of memristor's fabrication and properties on its performance and circuit design. Thus, this can help us to choose between different memristor types based on the application and the required design criteria.

The memristor types were discussed in Chapter 2. Table 2.1 provided an important comparison between memristor types for their main parameters and specifications. This chapter tries to answer the question of how could these specifications affect the design of memristor-based circuits and main topologies, which provides the designer some important design insights that help him to choose the best memristor type that can give the best performance and meets the main design requirements. It is important to note that there are a wide variety of memristor fabrication types which makes it difficult to accurately define the exact parameter values of each type. However, the values that are used in this study provides acceptable average values of each fabrication type and can be a good reference for this comparison.

Table 6.1 repeat important properties mentioned in Table 2.1, add the model parameters' values that are used for different memristor types

through the simulations of this study and refers to some references with experimental data that justify the choice of these values.

The model that is used in this comparative study is the non-linear ion-drift model using Biolek window function [29]. The reason for not using the proposed models in Chapter 4 for this comparison is that these models are dedicated for spintronic memristor only. Biolek model is suitable for all memristor types with an acceptable degree of accuracy. The window function parameter *P=40* for all memristor types. The rest of the model parameters are provided in Table 6.1. For all memristor types, we assumed that they have the same area. Thus, the area of each compared circuit/topology is the same and not included in the comparison.

Table 6.1 Comparison of main parameters for different memristor types using Biolek Model.

Memristor Type	**Resistive**	**Spintronic**	**Polymeric**	**Ferroelectric**	**Manganite**
ON/OFF Ratio	2000	5	100	300	100
Access Time (ns)	~10	~10	~25	~10	~100
R_{on}	100Ω	1KΩ	10KΩ	150KΩ	50
R_{OFF}	200KΩ	5KΩ	1MΩ	46MΩ	5kΩ
μ_v	1.00E-05	3.00E-08	2.00E-07	1.50E-07	5.00E-08
References	[2, 94]	[93]	[95, 96]	[24, 97]	[25, 98]

The circuits/topologies discussed in this chapter are not divided into categories such as analog, memory, and neuromorphic applications. Many memristor-based circuits/topologies can be used in different applications. For example, the crossbar memristor topologies 1T1M, 1D1M, and 0T1M

are used in almost all memristor applications. That is why these circuits/topologies are not categorized.

6.2. Memristor-based Oscillators

Figure 6.1 shows an example of a relaxation oscillator proposed in [99]. The memristor in this circuit substitutes the capacitor as it keeps increasing and decreasing its state variable to provide the required sustained oscillation. The input voltage moves between the two limiting values V_p and V_n , and their corresponding memristances are R_{mn}, and R_{mp}. The values of R_{mn}, and R_{mp} must lie between the lowest and highest memristance values R_{ON}, and R_{OFF}. For equal absolute values of V_{OH} and V_{OL}, the cycle time (T) equals [99]:

$$T = \frac{(R_{mp}^2 - R_{mn}^2) + 2\,R_a(R_{mp} - R_{mn})}{2\,K' V_{OL}} \tag{6.1}$$

where K' equals:

$$K' = \mu_V R_{ON} \frac{(R_{OFF} - R_{ON})}{D^2} \tag{6.2}$$

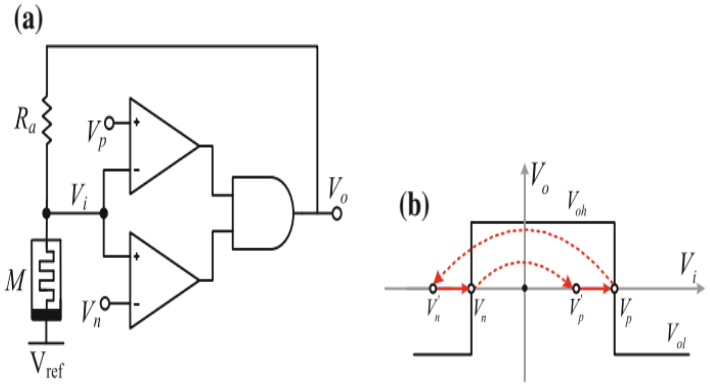


Figure 6.1 Memristor-based reactance-less oscillator (a) Circuit (b) transition between different operating points [99].

From (6.1) and (6.2), it is clear that the operating frequency of this oscillator is inversely proportional to R_{ON}, the ON/OFF ratio of the memristor, and the mobility μ_V.

Figure 6.2 shows the simulation results of the oscillator using the reference values provided in **[99]** (R_{ON}=100 **Ω**, and R_{OFF}=38 K**Ω**, μ_V =1x10^{-10} cm^{2}s^{-1}V^{-1}). The resultant frequency of this circuit equals *3.51 Hz.*

However, when using the approximate parameter values of different memristor types, they give much higher frequencies, which means that the practical applications of this oscillator should be changed or the design must be modified to achieve such low frequencies. Figure 6.3 shows the simulation results of the oscillator using the resistive memristor. The operating frequency is about 149 MHz which is in a completely different scale than the example provided in [99].

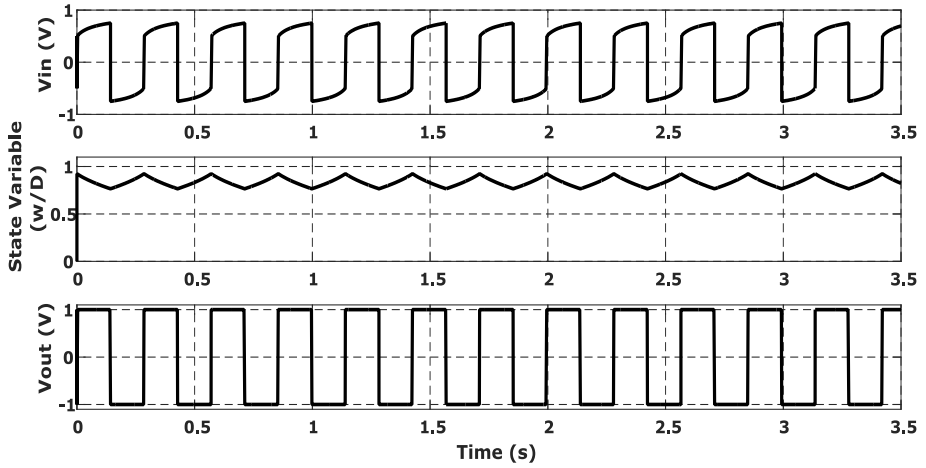


Figure 6.2 The simulation results of the memristor-based reactance-less oscillator (R_{ON}=100 **Ω**, and R_{OFF}=38 K**Ω**, μ_V =1x10-10 cm2s-1V-1).

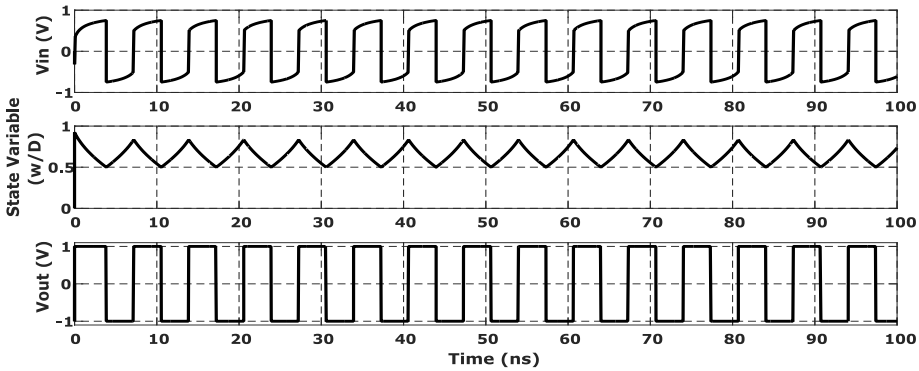


Figure 6.3 Memristor-based reactance-less oscillator using the resistive memristor.

Table 6.2 provides a comparison between memristor types when used in the reactance-less oscillator of Figure 6.1. The table shows that the resistive memristor can provide a wide range of frequencies up to *16.67 THz* benefiting from its high ON/OFF ratio which gives a high K' value and thus a high frequency as given in (6.1), and (6.2). The lowest possible frequency is f_{min}*=3.65 MHz* using the ferroelectric memristor due to its high R_{OFF} value. The oscillating frequency f_{osc} is calculated at the average R_a value between $R_{a,max}$, and $R_{a,min}$ as given in the table. All these values are calculated based on the mathematical derivation provided in [73].

Table 6.2 Comparison between different memristor types for the parameters of Affan reactance-less oscillator.

Memristor Type	**Resistive**	**Spintronic**	**Polymeric**	**Ferroelectric**	**Manganite**
f_{osc} (Hz)	149.6M	56.5M	56.4M	14.5M	14.1M
f_{max} (Hz)	16.667T	100M	16.5G	38.15G	4.16G
f_{min} (Hz)	37.5M	36M	14.85M	3.65M	3.75M
R_a (Ω)	33.38K	1.33K	171K	7.7M	860
$R_{a,max}$(Ω)	66.67K	1.67K	333K	15.33M	1.67K
$R_{a,min}$(Ω)	100	1K	10K	150K	50

A.G. Mosad presented an improved memristor-based relaxation oscillator which offers higher frequency and wider tuning range than the previous reactance-less oscillator [73]. The circuit is shown in Figure 6.4 and the tracing that describes its behavior.

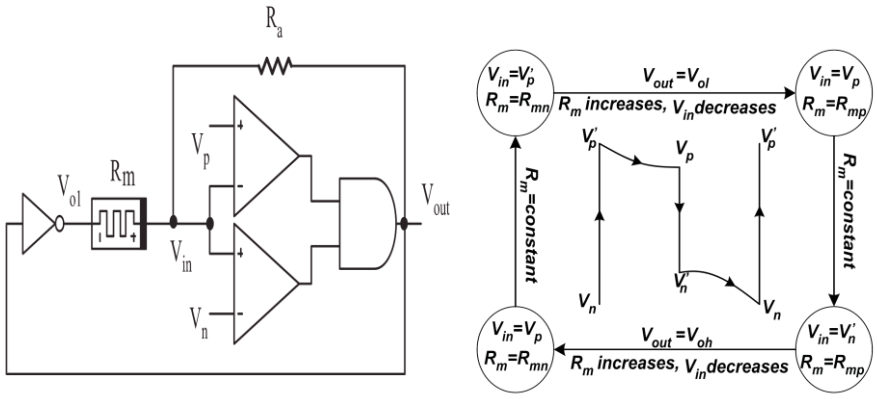


Figure 6.4 Memristor-based improved reactance-less oscillator (a) Circuit. (b) tracing of the circuit [73].

The idea of the circuit is connecting the negative terminal of the memristor to inverted output instead of to ground. This allows using a single supply voltage V_{DD} with the ground instead of two supply voltages of $\pm V_{DD}$.

Figure 6.5 shows the output of the circuit using the basic values provided in [73]. The same note that was mentioned in the previous circuit also exists here as the operating frequency is much lower than the achieve values when applying different memristor types. Thus, these circuits cannot be used for very low-frequency applications such as biomedical applications. Figure 6.6 shows the simulation results of the improved reactance-less oscillator using the manganite memristor. In this circuit, we used an initial state variable far from the desired value to achieve oscillation

to prove that the oscillation can still be achieved regardless the initial state of the memristor. The operating frequency is about 700 MHz which as mentioned much higher than the proposed values in [73].

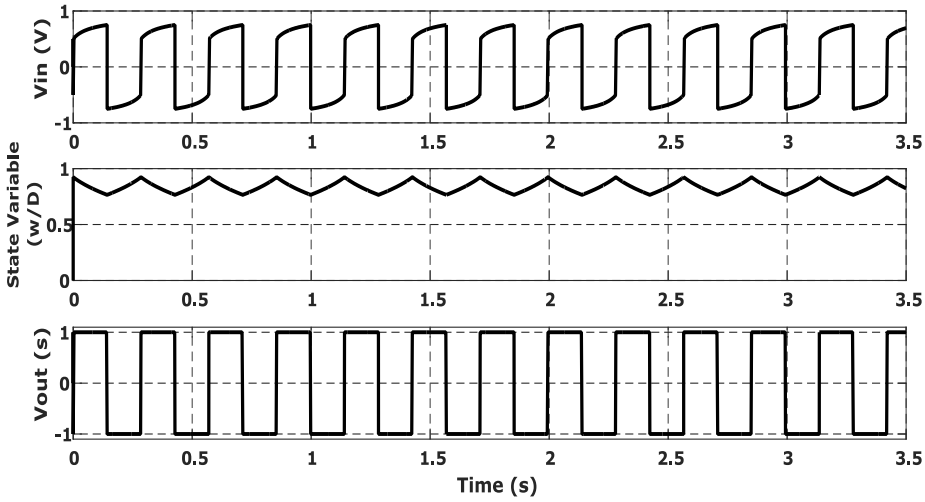


Figure 6.5 Memristor-based reactance-less oscillator

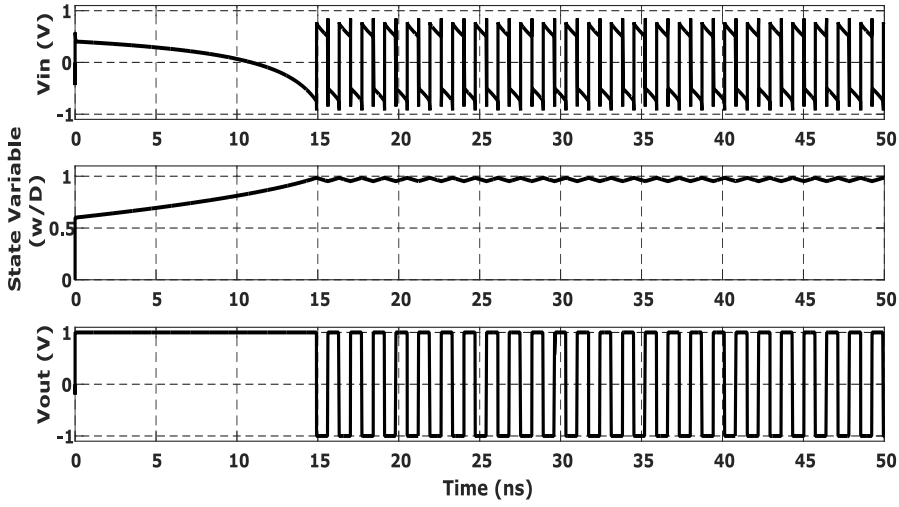


Figure 6.6 Simulation results (a) Vi (b) Memristor state variable (c) Vout.

Table 6.3 provides a comparison between different memristor types for the improved oscillator circuit. The improved circuit provides a wider frequency ranges with a minimum value of f_{min} = 2.3 MHz using the ferroelectric memristor and a maximum value of f_{max} = 17.31 THz for the resistive memristor.

Table 6.3 Comparison between different memristor types for Affan Improved Oscillator Circuit.

Memristor Type	**Resistive**	**Spintronic**	**Polymeric**	**Ferroelectric**	**Manganite**
f_{osc} (Hz)	7.6G	2.87G	2.87G	737.8M	717.4M
f_{max} (Hz)	17.31T	103.8M	17.13G	39.62G	4.32G
f_{min} (Hz)	23.56M	22.62M	9.33M	2.3M	2.36M
R_a (Ω)	33.38K	1.33K	171K	7.7M	860
$R_{a,max}$(Ω)	600K	15K	3M	138M	15K
$R_{a,min}$(Ω)	100	1K	10K	150K	50

6.3. Memristor-based Ratioed Logic (MRL) Circuits

The memristor ratioed logic (MRL) was proposed in [65]. The concept of this logic type depends on the idea that the memristor resistivity increases when a current pass in a specific direction and decreases when current passes in the reverse direction. Thus, if enough time is allowed the memristor eventually becomes in the ON state or the OFF state depending on the current direction. After that, the output value is calculated depending on the potential divider between different memristors. Figure 6.7 shows the schematic of AND gate and OR gate. Those circuits are the basic circuit for all MRL logic. A static inverter must be used to achieve any inverting

function. It should be noted that there are other types of memristor-based logic such as memristor-aided logic (MAGIC) [41] and Memristor-based material implication (IMPLY) logic [61]. However, the MRL type is more reliable with acceptable noise margins and fewer design constraints.

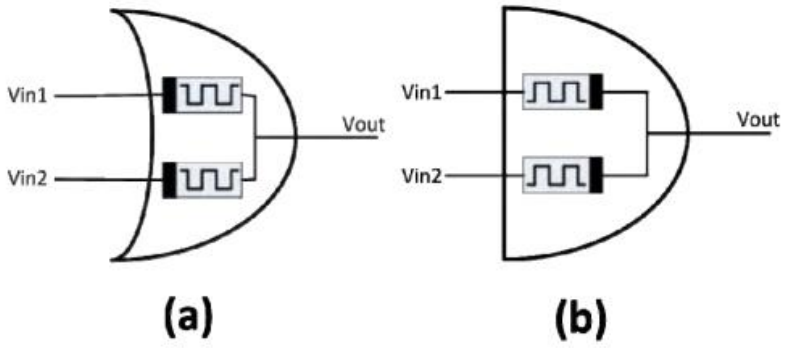


Figure 6.7 Schematic of MRL gates (a) OR gate (b) AND gate [65].

Figure 6.8 and Figure 6.9 show the simulation results of both the 2-input NAND and 5-input OR gate respectively. The performance of these gates depends on the speed of the memristor. Also, memristors with higher resistance values can provide lower currents and power consumptions at the cost of the device speed. The 2-input NAND gate uses the and gate shown in Figure 6.7 followed by a static CMOS inverter. The *0.13 µm* CMOS technology is used and a supply voltage of *1.2 V*. The 5-input OR gate is used to show the effect of the number of inputs on the performance. As will be shown, memristors with high ON/OFF ratio does not suffer any problems due to a large number of inputs. However, memristor with low ON/OFF ratio cannot function properly under a large number of inputs.

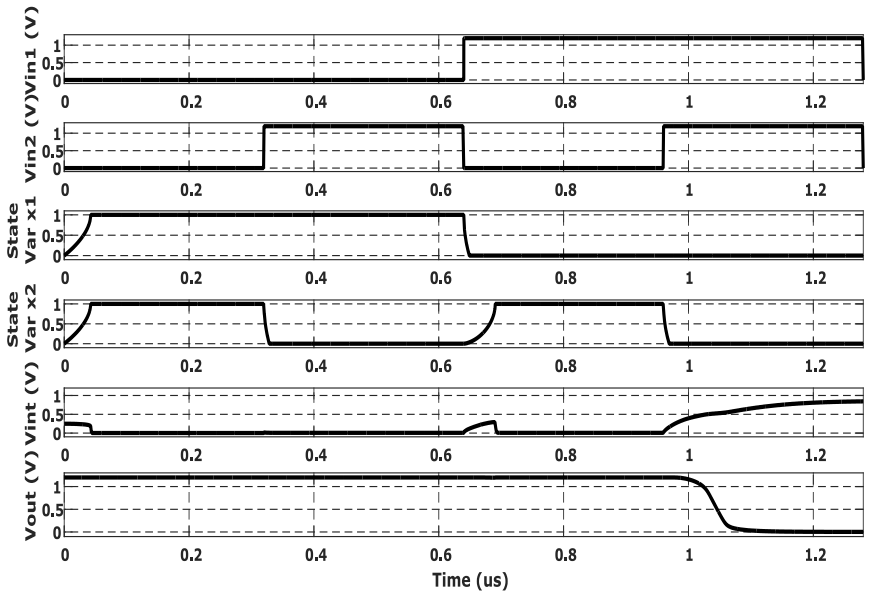


Figure 6.8 Simulation results of inputs, output, and state variables for a 2-input NAND gate using ferroelectric memristor.

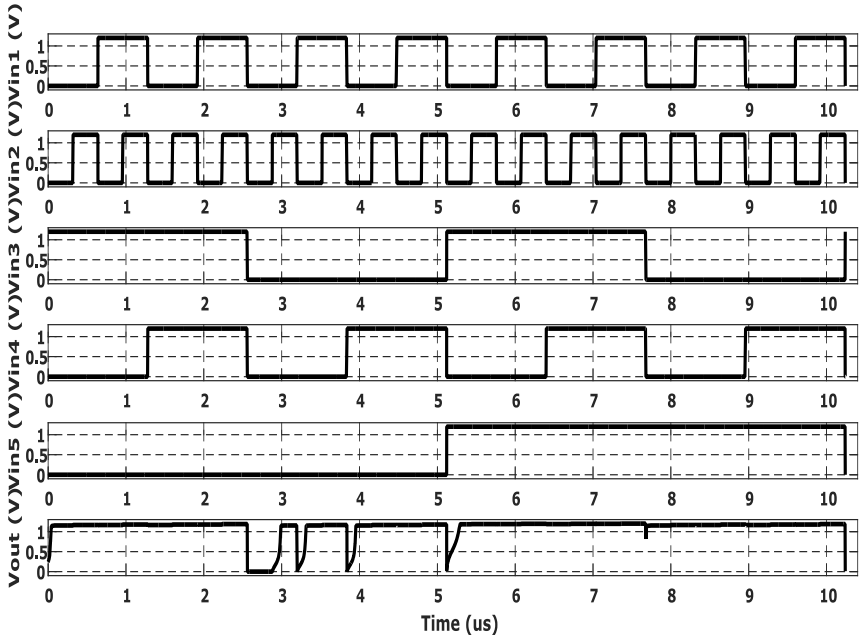


Figure 6.9 Simulation results of inputs, and output, for a 5-input OR gate using the manganite memristor.

Another important design issue is to cascade stages of MRL logic without separating it with static CMOS inverter. To study the effect of cascading MRL logic, the full adder shown in Figure 6.10 is investigated. The circuit uses two cascaded stages of MRL to the *SUM* output and four cascaded stages for the C_{OUT} output.

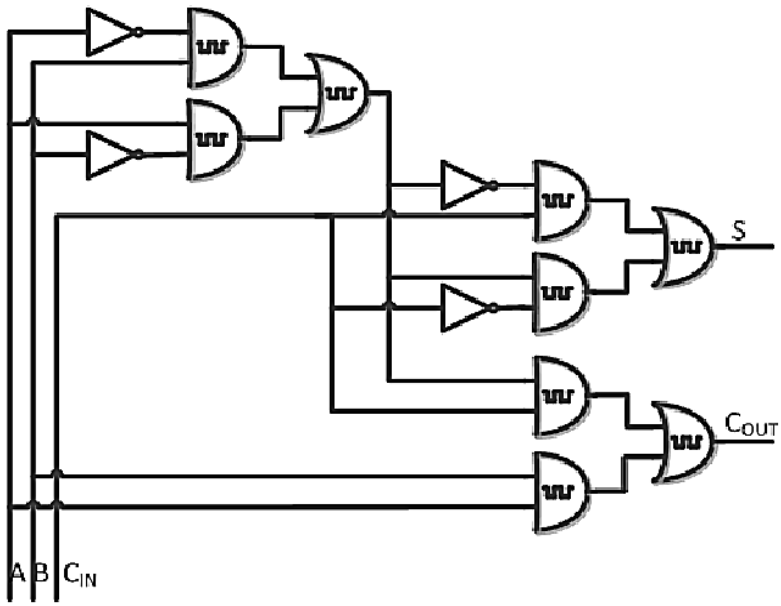


Figure 6.10 Simulation results of inputs, and outputs, for a full adder using the resistive memristor [65].

Figure 6.11 shows the simulation results of the full adder using resistive memristor. Cascading logic stages reduces the logic swing from the full swing (0,V_{DD}) to (0.2 V_{DD}, 0.5 V_{DD}).

The logic swing in the MRL is not constant, and the provided values are the worst case values. This problem can be solved by using static inverters at the end of MRL logic.

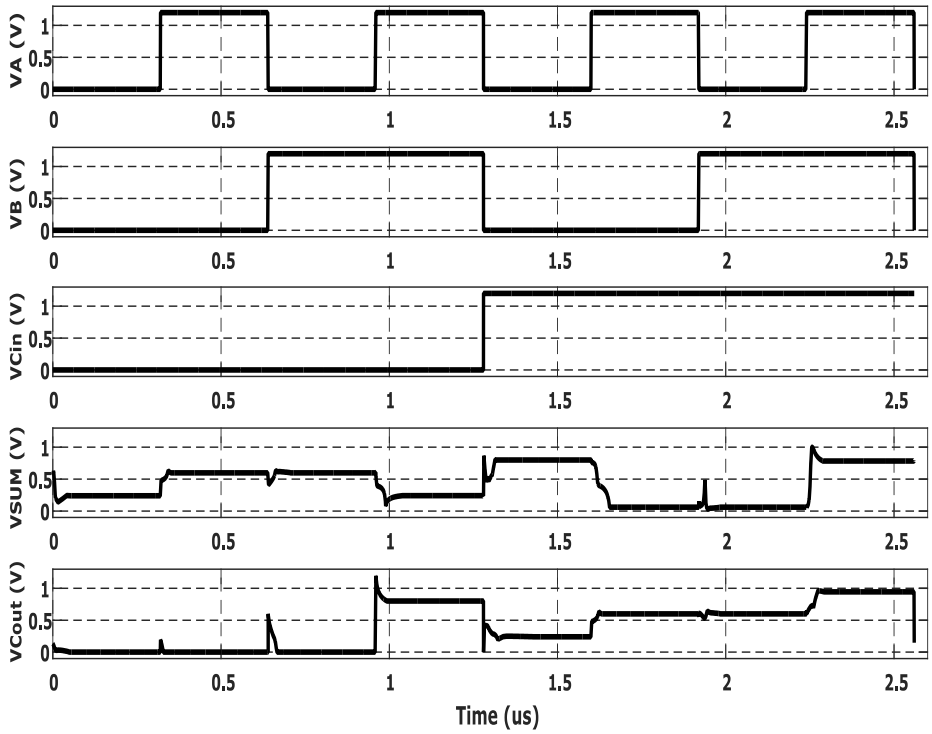


Figure 6.11 Simulation results of inputs, and outputs, for a full adder using the resistive memristor.

However, as long as the number of cascaded stages increases, the logic swing keeps reducing until a point at which the circuit fails to provide distinguished output levels for logic 1 from logic 0 states. Thus, for the MRL logic, the maximum allowable number of cascaded stages must be calculated to ensure proper operation. Figure 6.12 shows another example of a full adder circuit using polymeric memristors. The circuit gives nearly the same logic swing, but it has a slower response.

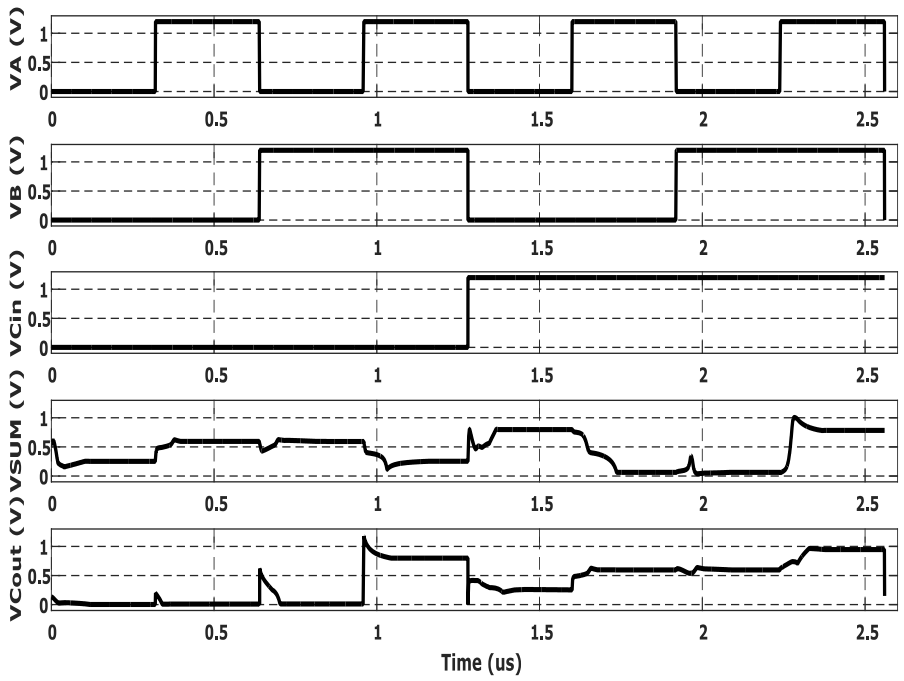


Figure 6.12 Simulation results of inputs, and outputs, for a full adder using the polymeric memristor.

Table 6.4 summaries the comparison between different memristor types for MRL Logic from the propagation delay point of view. It should be noted that for the full adder circuit, the propagation delay is measured to the middle point between the worst case values of logic 1 and logic 0. For the spintronic memristor, the 5-input OR and the 5-input AND gates failed to provide two distinguished levels for logic 0 and logic 1. The reason for this is the low ON/OFF ratio of spintronic memristors which greatly limits the use of this type in MRL logic and even all other types of memristor-based logic circuits. An interesting note in the ferroelectric memristor-based MRL logic is the great difference between the propagation delay of the

AND/OR gates and the NAND/NOR gates. The simulation shows a very narrow overshoot current tunnel through the inverter input (MOS gates), and this overshoot diminish slower when the memristors have higher resistances. Thus, for the ferroelectric memristor which have the highest ON and OFF resistances, this current delays switching from high to low. This effect exists in other memristor types, but its effect is considerably smaller. The MRL using manganite memristor is slower than other types due to the slower switching of the manganite memristor as provided in Table 6.1.

Table 6.4 Comparison between different memristor types for MRL Logic (Speed).

Memristor Type	Resistive	Spintronic	Polymeric	Ferroelectric	Manganite
2-in AND	8.4 ns	8.3 ns	21 ns	18.4 ns	82 ns
2-in OR	8.4 ns	8.34 ns	21 ns	8.4 ns	85 ns
2-in NAND	10 ns	10 ns	27.9 ns	82 ns	95 ns
2-in NOR	8 ns	6.6 ns	20 ns	119 ns	72 ns
5-in AND	8.76 ns	failed	22 ns	18.87 ns	100 ns
5-in OR	8.77 ns	failed	22 ns	10 ns	100 ns
Full Adder	23 ns	7.6 ns	57 ns	240 ns	failed

Table 6.5 provides a comparison between different memristor types for MRL Logic from the power consumption point of view. For memristor types with low memristances, the power consumption is higher. For memristors with higher memristances, the power consumption of the MRL gates is much lower and the static CMOS inverter's power consumption is dominant like in the ferroelectric memristor case.

Table 6.5 Comparison between different memristor types for MRL Logic (Power Consumption).

Memristor Type	Resistive	Spintronic	Polymeric	Ferroelectric	Manganite
2-in AND	3.6 µW	120 µW	0.69 µW	15.57 nW	124.2 µW
2-in OR	3.6 µW	76.76 µW	0.69 µW	15.4 nW	124.2 µW
2-in NAND	11.34 µW	127.3 µW	4.28 µW	21.5 µW	142.6 µW
2-in NOR	13 µW	78.22 µW	4.05 µW	12.71 µW	136.2 µW
5-in AND	16.9 µW	failed	3.25 µW	73.25 nW	540.9 µW
5-in OR	16.4 µW	failed	3.19 µW	72.5 nW	594.1 µW
Full Adder	65 µW	450 µW	46.38 µW	53.32 µW	failed

Table 6.6 provides a comparison between different memristor types for MRL worst case logic swing. The logic swing of MRL logic is not only important for noise margins, but also for ensuring proper operation as the logic swing keeps reducing with direct cascading of logic stages. For memristor types with high ON/OFF ratio, the one stage logic can achieve a full swing. The spintronic memristor is the only type that could not achieve a full swing in the one-stage logic as it has a very small ON/OFF ratio compared to other types. On the other hand, for the full adder which has cascaded logic gates of two and four stages, all memristor types suffer from logic swing reduction. The manganite memristor has the lowest R_{ON}, and thus it failed to provide two distinguished voltage levels for logic 1 and logic 0 states. As a conclusion, both the spintronic and the manganite memristors need careful design to ensure proper operation. The resistive memristor has the best characteristics of acceptable logic swing, higher speed, and intermediate power consumption.

Table 6.6 Comparison between different memristor types for MRL Logic worst case (V_{LOW} ,V_{HIGH}) where V_{DD}= 1.2 V.

Memristor Type	Resistive	Spintronic	Polymeric	Ferroelectric	Manganite
1 Stage (ex: 5-in OR)	Full Swing (0 V, 1.2 V)	(0.2 V, 1.2 V) AND (0 V, 1 V) OR	Full Swing (0 V, 1.2 V)	Full Swing (0 V, 1.2 V)	Full Swing (0 V, 1.2 V)
2&4 Stages (ex: Full Adder)	(0.24V, 0.6 V)	(0.41 V, 0.5 V)	(0.25 V, 0.6 V)	(0.25 V, 0.6 V)	failed

6.4. Memristor Crossbar Arrays

For most applications, memristors need to be connected in array form. Thus, studying the crossbar memristor arrays is an essential step for applications such as memories, and neuromorphic systems. The crossbar arrays can be formed using only a memristor at each cross-point which is called (0T1M) crossbar array, or one diode and one memristor (1D1M), or one transistor and one memristor (1T1M). The first type – 0T1M- provides the highest density which is an essential requirement for any application and especially for memristor-based memory circuits. However, as the memristor is a two-terminal device, undesired paths called *sneak paths* can occur besides the selected path, and it is unavoidable in this crossbar array type. The aim of this section is to study the effect of sneak paths on the crossbar arrays of each memristor type. One solution to avoid the problem of sneak paths is to use the 1D1M crossbar arrays. In this type, if there are N diodes in one sneak path, then this path needs a voltage of $N.V_{D,ON}$ to turn these diodes ON. Achieving this voltage level is usually difficult, which prevent the sneak path from affecting the circuit operation. The second solution is to use the 1T1M crossbar array which completely prevents the

sneak paths by turning off MOSFETs in undesired paths. However that these solutions avoid the effect of sneak paths, the price in density reduction is high. The 0T1M crossbar can achieve up to 93% less area than the 1T1M crossbar arrays [100]. Thus, the study of sneak paths effect in 0T1M crossbars is important to see if the circuit can operate properly with the sneak paths or not.

6.4.1. The 0T1M Crossbar Arrays

Figure 6.13 shows a simple example of a *5x5* memristor crossbar. The reading operation is performed by applying a reading pulse V_R and sensing the output voltage V_{OUT} that comes from the potential divider between the selected memristor and a load resistance R_L. Figure 6.13a shows the ideal case where there is only the selected current path. In this case, the output voltage is calculated as follows:

$$V_{OUT,ideal} = V_R \frac{R_L}{R_L+R_M} \tag{6.3}$$

However, as shown in Figure 6.13b, some undesired current paths might occur if the all the memristors in each of these current paths are in the ON state. These current paths are called sneak paths and they add parallel paths with an equivalent parallel resistance R_{SP} to the main memristance of the selected memristor. Thus, the real equation of the output voltage becomes:

$$V_{OUT,sneak} = V_R \frac{R_L}{R_L+(R_M \,//\, R_{SP})} \tag{6.4}$$

The effect of the sneak paths can be considerably large, especially if the memristor is in the OFF state and the ON/OFF ratio is large. In this case, the sneak path resistance R_{SP} becomes the dominant resistance as it is much smaller than the memristance of the selected memristor R_M.

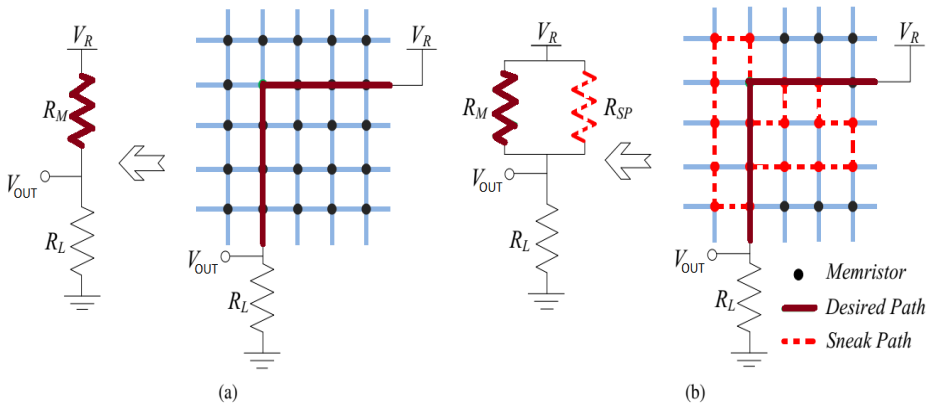


Figure 6.13 The reading current path through 0T1M memristor crossbar (a) Ideal case without sneak paths (b) Real case example with the dashed lines are undesired current paths (sneak paths) [46].

The design of the 0T1M memristor crossbars requires a smart choice of the reading pulse V_R and the load resistance R_L. The reading pulse should use an identical positive and negative pulses with narrow pulse widths as shown in Figure 6.14. The narrow pulse width ensures a small disturbance to the state variable ($x = w/D;\ 0 \leq x \leq 1$) of the selected memristor, and the negative pulse prevents accumulated drifts to the state variable by compensating the effect of the positive pulse. The output voltage is sensed during the positive reading pulse. The proper choice of the load resistance R_L can help in reducing the sneak path effect. Let's take an example of the resistive memristor where $R_{ON} = 100\ \Omega$, and $R_{OFF} = 200\ K\Omega$. Assuming that the positive reading pulse V_R=1 V, and the equivalent sneak paths resistance is $R_{SP}=5*R_{ON}=500\ \Omega$. The first choice is to make the load resistance $R_L=R_{OFF}$. From (6.3) and (6.4), the output voltages with and without the sneak path effect are as follows:

$$\text{Logic 0 } (x=0,\ R_M=R_{OFF}):\ V_{OUT,ideal} = 0.5\ V\ ,\ V_{OUT,sneak} = 0.9975\ V \quad (6.5.a)$$

$$\text{Logic 1 } (x=1,\ R_M=R_{ON}):\ V_{OUT,ideal} = 1\ V\ ,\ V_{OUT,sneak} = 1\ V \quad (6.5.b)$$

It is clear from (6.5) that this choice is a bad choice as the difference between the sensed voltage at logic 0 and logic 1 reduces from $\Delta V_{OUT,ideal}=0.5\ V$, to $\Delta V_{OUT,sneak} = 0.0025\ V$. The second choice is to choose the load resistance as the average of R_{ON}, and R_{OFF} which also highly reduces ΔV_{OUT} . Thus, the third and best choice is to take the load resistance as low as possible $R_M=R_{ON}$. The output voltages with and without the sneak path effect, in this case, are as follows:

$$\text{Logic 0 } (x=0,\ R_M=R_{OFF}):\ V_{OUT,ideal} = 0\ V\ ,\ V_{OUT,sneak}= 0.1667\ V \qquad (6.6.a)$$

$$\text{Logic 1 } (x=1,\ R_M=R_{ON}):\ V_{OUT,ideal} = 0.5\ V\ ,\ V_{OUT,sneak}= 0.5454\ V \qquad (6.6.b)$$

In this case, the difference between the sensed voltage at logic 0 and logic 1 reduces from $\Delta V_{OUT,ideal}=0.5\ V$, to $\Delta V_{OUT,sneak} = 0.3787\ V$, which is much better than the first and second choices.

The 0T1M memristor crossbar that is used in our comparison is an *8x8* memristor crossbar with three sneak paths. The load resistance is chosen to be $R_L=R_{ON}$ to reduce the sneak path effect. The total width of the reading signal is *0.25 ns* with ± *1 V* identical pulses. It is assumed that there is no pulse mismatch for simplicity.

Figure 6.14 shows the simulation results of reading a logic 0 polymeric memristor without sneak path effect. The output voltage is $V_{OUT,ideal} = 40\ mV$. The simulation is repeated with the sneak path effect, and the output is shown in Figure 6.15 . The output voltage increased to $V_{OUT,sneak}= 0.43\ V$. The positive pulse increases the state variable by a very small drift and it is compensated by the negative pulse. Thus, for reading logic 0, there is no disturbance in the state variable for all memristor types ($\Delta x=0$).

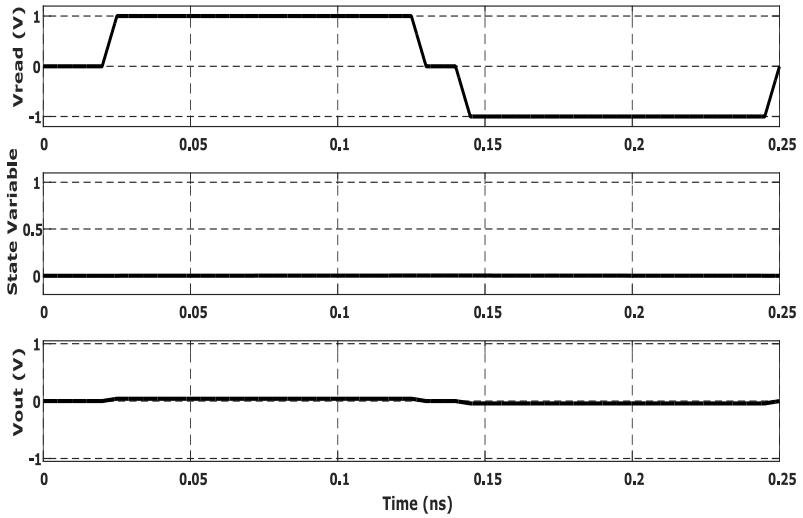


Figure 6.14 Reading Logic 0 of polymeric memristor without the sneak path effect.

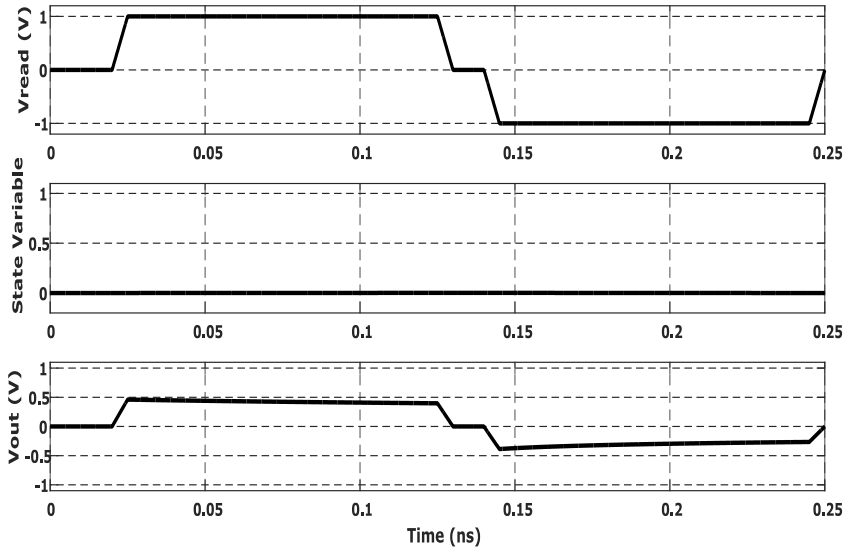


Figure 6.15 Reading Logic 0 of polymeric memristor with the sneak path effect

Figure 6.16 shows the simulation results of reading logic 1 for a ferroelectric memristor in the ideal case. The output voltage is

$V_{OUT,ideal}$ = *0.51 V*. As the initial state variable is *x=1*, the positive pulse cannot increase the state variable. In the negative reading pulse, the state variable decreases causing a drift with Δx = *20m*. However, this drift is compensated with the next reading pulse, and thus the drift in the state variable is not accumulative. Another reason for the noticeable drift in the state variable when reading logic 1 is the high current flow as the memristor is in the ON state (R_{ON}). In Figure 6.17, the sneak paths are added. The output increased to $V_{OUT,sneak}$ = *0.58 V* and the state variable drift increased to Δx_{sneak} =*90m*. Despite that the drift is not accumulative, it is based on the assumption that there is no pulse mismatch in the reading signal. In the practical application, this increase in the state variable drift due to the sneak path effect reduces the allowable number of successive reading operations before a refreshment is required.

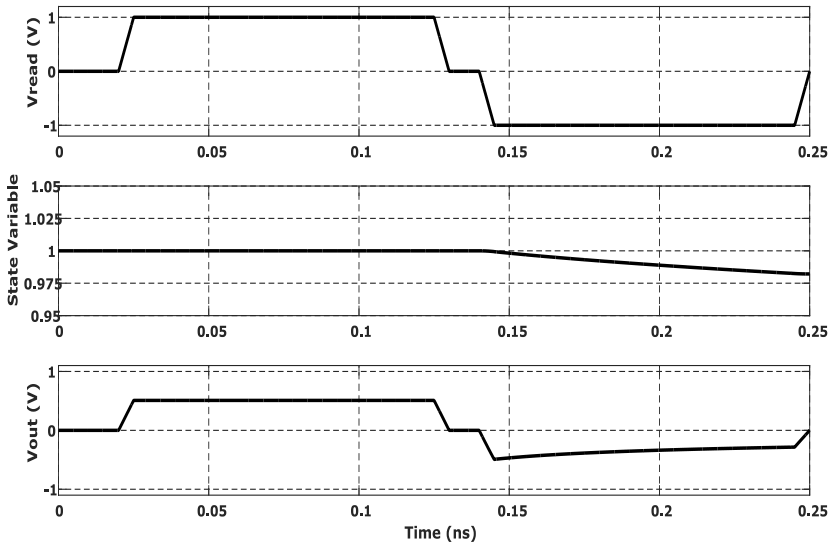


Figure 6.16 Reading Logic 1 of ferroelectric memristor without the sneak path effect.

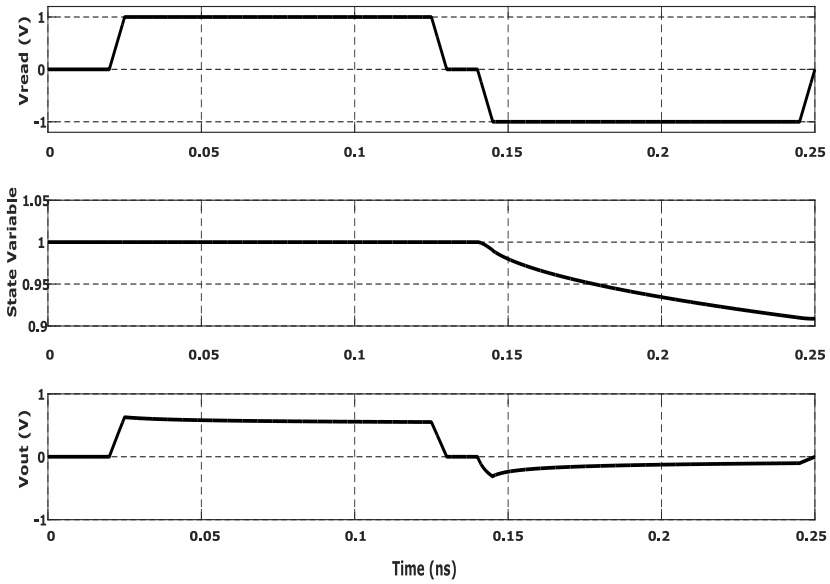


Figure 6.17 Reading Logic 1 of ferroelectric memristor with the sneak path effect

Table 6.7 summarize the comparison between different memristor types for the 0T1M 8x8 Crossbar array. The table shows the great effect of sneak paths. For spintronic memristors, the output voltages of logic 1 and logic 0 differ by only 80 mV. The matter is even worse as the sneak paths are not determinant, and thus all these calculations are valid only for this particular example.

6.4.2. The 1D1M Crossbar Arrays

The use of the 1D1M memristor crossbar arrays is one of the main solutions to the sneak paths on the price of reducing density. The same 8x8 memristor crossbar is used here but with adding one diode to each cross-point. Also, there is no need to use a positive and negative reading signal in this case as the diode only conducts in one direction and its voltage drop takes most of the read signal voltage. Thus, a reading signal of +1 V is directly applied here to read the data stored in any memristor.

Table 6.7 Comparison between different memristor types for 0T1M Crossbar.

Memristor Type			**Resistive**	**Spintronic**	**Polymeric**	**Ferroelectric**	**Manganite**
Reading Logic 0	**Without Sneak paths**	**V_{OUT}**	0 V	0.46 V	40 mV	13 mV	40 mV
		Δx	0	0	0	0	0
	With Sneak paths	**$V_{OUT(avg)}$**	72 mV	0.64 V	0.43 V	0.27 V	0.45 V
		Δx	0	0	0	0	0
Reading Logic 1	**Without Sneak paths**	**V_{OUT}**	0.5 V	0.62 V	0.5 V	0.51 V	0.51 V
		Δx	100 m	12 m	50 m	20 m	18 m
	With Sneak paths	**$V_{OUT(avg)}$**	0.54 V	0.72 V	0.64 V	0.58 V	0.65 V
		Δx	100 m	9 m	40 m	90 m	14 m
ΔV_{OUT} (logic 1 – logic0)	**Without Sneak paths**		0.5 V	0.16 V	0.46 V	0.5 V	0.47 V
	With Sneak paths		0.47 V	0.08 V	0.21 V	0.31 V	0.2 V

Figure 6.18 shows the simulation results of reading logic 0 of resistive memristor without the sneak path effect. The output voltage is $V_{OUT} = 0.63$ *V*. Figure 6.19 shows the simulation results of reading logic 0 of resistive memristor including the sneak path effect. It gives exactly the same results. Regardless the type of memristor and whether reading logic 0 or logic 1, the 1D1M memristor crossbar arrays were able to completely cancel the sneak path effect.

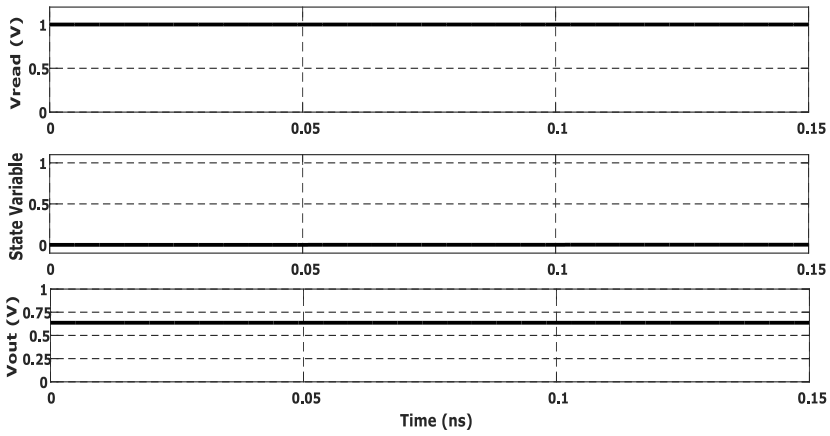


Figure 6.18 Reading Logic 0 of resistive memristor without the sneak path effect.

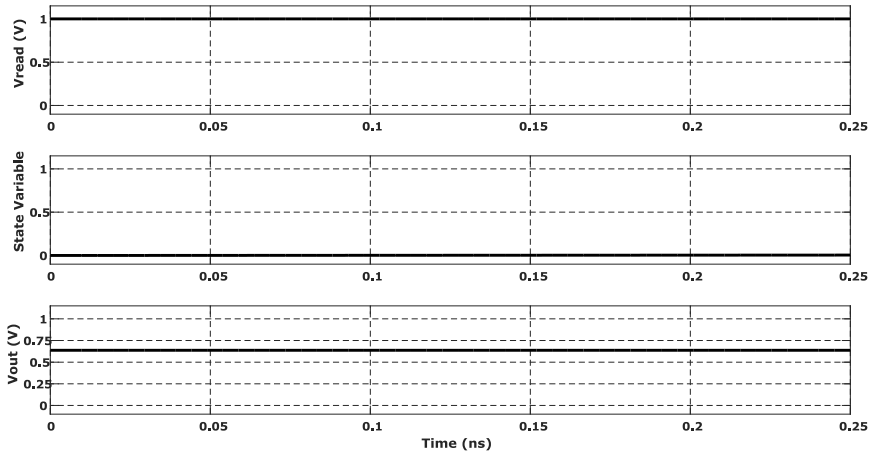


Figure 6.19 Reading Logic 0 of resistive memristor with the sneak path effect

6.5. Memristor Training

Another important application is memristor training/programming. Memristor programming means the ability to adjust its memristance and hence its state variable to any desired value. Memristor programming is required in many applications such as neuromorphic systems, multi-level memories, and using memristors as a programmable resistor which can be used in variable gain amplifiers. The word *training* is usually used with the neural applications. Figure 6.20 shows an example of a circuit used in training memristors [101]. The concept of the circuit is to use a simple inverting operational amplifier with the memristor that is required to be trained and a fixed resistance. The required memristance value is translated to its equivalent output voltage and inserted to the two comparators with a small precision value subtracted for the 1st comparator input and added to the 2nd comparator input.

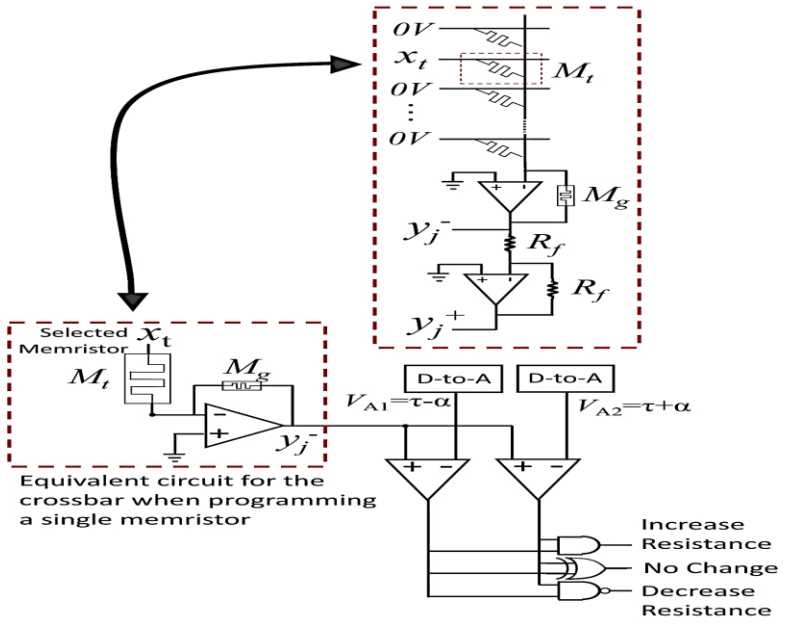


Figure 6.20 Circuit used to program a single memristor to a target resistance [101].

When the memristance is smaller than the required value the AND gate is high indicating the need to increase its resistance. When the memristance is higher than the required value the NAND gate is high indicating the need to increase its resistance. Both increasing and decreasing are achieved through a feedback voltage pulses until reaching the target resistance. The XOR gate becomes high when reaching the target resistance indicating the end of the training process.

The first training test initialize the memristor at x_{init}= 0.875. The target state variable is assumed to be x_{final} = 0.75. This test is performed for all memristor types to study their response. The implementation of the circuit and the simulation using Virtuoso are provided in Appendix B.

Figure 6.21 shows the training of the ferroelectric memristor. As the initial state variable is larger than the target state variable, then the initial memristance is smaller than the target memristance. The first control output is zero which means that the target memristance is not larger than the initial memristance. The second control output initially equal 1 V which activate the feedback loop to increase the memristance (decrease state variable). When the memristance reaches the target value the second control output (Increase R_M) switched to 0 V and stop the feedback loop. The third control output (No Change) switches to 1 V at the same time which indicates that the target memristance is achieved. Figure 6.22 shows the training of manganite memristor for the same conditions. The time required to train the manganite memristor is larger than the time required to train the ferroelectric memristor, because the manganite memristor switching speed is slower than the ferroelectric memristor.

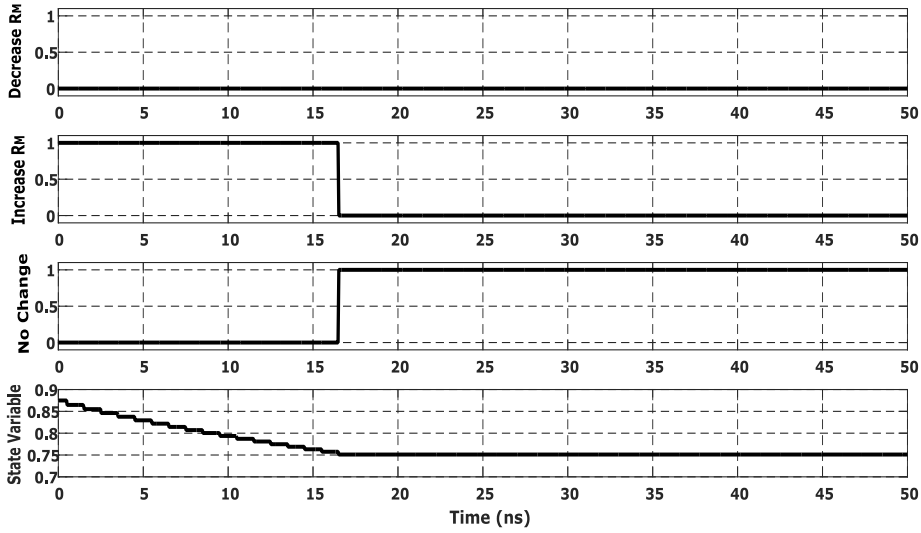


Figure 6.21 Training ferroelectric memristor with initial memristance smaller than the target memristance.

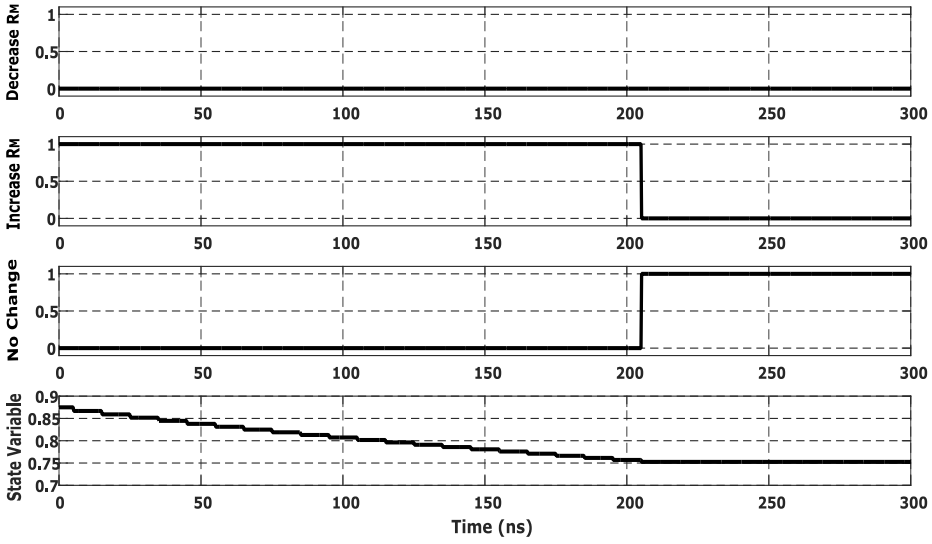


Figure 6.22 Training Manganite memristor with initial memristance smaller than the target memristance.

Table 6.8 provide a comparison of the time required to train each memristor type for the given example (x_{init} = 0.875, x_{final} = 0.75). The

manganite and polymeric memristors are the slowest in switching, so they are also the slowest in training. However, the switching speed of memristors can't explain the difference between resistive, spintronic, and ferroelectric memristors which have the same switching delay. The other factors that affect the training time are the values of μ_V , R_{ON}. Equation (2.5) shows that the rate of change of the state variable is proportional to μ_V , R_{ON}. Thus, the memristor which have higher μ_V, or higher R_{ON} can achieve faster training. The dependence on R_{ON} is not directly proportional as the increasing of R_{ON} reduces the current pass though the memristor. As a conclusion, the simulation results shows that training speed has a direct proportionality to μ_V, and it also increases with R_{ON} but at a slower rate.

Table 6.8 Comparison between different memristor types for training time (x_{init}=0.875 , x_{final} = 0.75).

Memristor Type	**Resistive**	**Spintronic**	**Polymeric**	**Ferroelectric**	**Manganite**
Training time	14.5 ns	25.5 ns	51.5 ns	16.5 ns	205 ns

Figure 6.23 shows the reverse situation when the initial memristance is higher than the final memristance. In this case, the initial state variable is set to x_{init} = 0.5 and the same target state variable of x_{final} = 0.75. The (Decrease R_M) control signal starts at 1 V which means that the memristance needs to be decreased. When the target value corresponding to x_{final} =0.75 is achieved, the control signal (Decrease R_M) switched to 0 V and the (No Change) control signal switched to 1V.

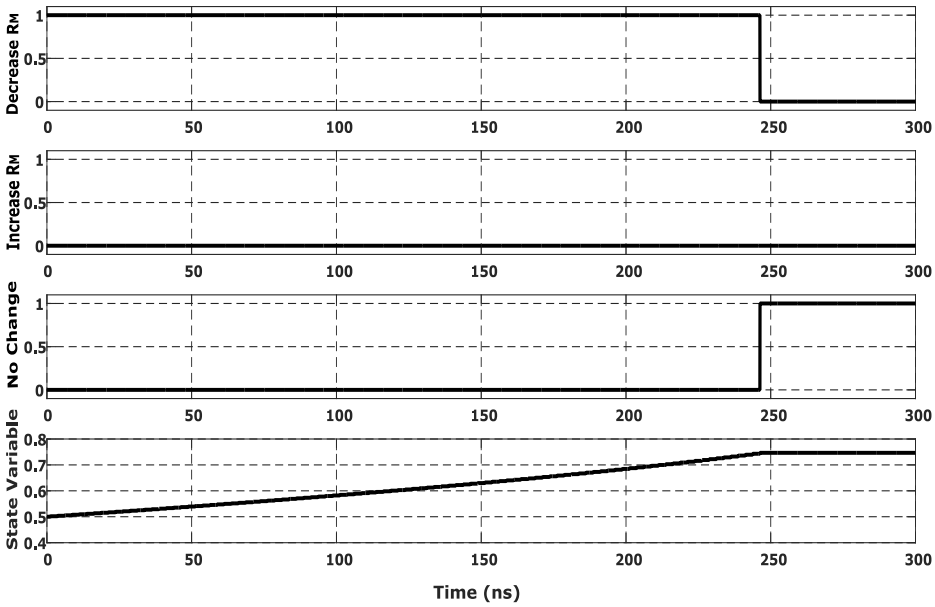


Figure 6.23 Training polymeric memristor with initial memristance higher than the target memristance.

Chapter 7: Conclusions and Future Work

In this chapter, some important conclusions about this thesis, and also the suggested topics for future work are introduced.

7.1. Conclusions

Recently, memristors have gained a wide research interest and found many applications. In this paper, an overview of memristor's basic operation, fabrication, and modeling are presented. Also, a survey on the various applications of memristors, which include nonvolatile memories, neuromorphic computer architectures, logic circuits, and analog applications is provided. This survey aims to give the reader a general overview of the device operation, main models, and recent research achievements in the field of memristor technology. Besides the overview, a future perspective is given for many possible improvements in memristors' modeling and applications, which can be useful for the upcoming researchs and helps in finding new ideas in the memristor field.

In this work, we have proposed a modified spintronic memristor model. The proposed model is used to study the read disturbance in spintronic memristor-based memory cells due to the thermal fluctuation. The simulation results show that, for a specific probability of failure during the reading process, there is a maximum allowable number of successive read cycles before failure. These results can be used to define the needed frequency of a data refreshment scheme. It is shown that increasing the read current increases the probability of data disturbance. Also, increasing the

operating temperature reduces the maximum allowable successive read cycles before failure.

The thesis also proposed an LLGS-based spintronic memristor model. The proposed model is the first model that represents the dynamical behavior of the spintronic memristor using the LLGS equation. This equation provides a physic based method to calculate the change in the magnetization vector of the free layer, providing an accurate model with a direct relation to the physical parameters of the memristor. Thus, the model takes into account the physical behavior of spin-transfer-torque effect of the MTJ-based spintronic memristor. The model also takes into account two important effects, the TMR voltage dependence, and the thermal fluctuation. Both effects are of great importance in studying the actual behavior of spintronic memristors in circuit design. The model is verified to an experimental data of a spintronic memristor, and it showed much better fitting compared to existing models. The model is written using Verilog-A and integrated with SPECTRE-based CAD tool to study the dynamical behavior of the memristor in various electronic circuits with CMOS designs.

The dynamical behavior of spintronic memristors is investigated using the proposed TFA model in order to gain better knowledge about the effect of temperature variations on their behavior. The write and read processes are also investigated using the TFA model. Some useful relations between the probability of failure and critical current density are calculated and plotted.

A read/write circuit is proposed. The proposed circuit achieved a great reduction in the required area for the read/write circuits compared to

existing techniques. The read disturbance of the proposed circuit is also investigated and compared with existing techniques to estimate the maximum allowable successive reading cycles before a refreshment is needed.

7.2. Suggestions for Future Work

From what is discussed in the thesis, it is clear that more enhancement in memristor fabrication and modeling is still needed.

In the field of fabrication, it is strongly recommended to investigate various available compounds that can enhance the ON/OFF ratio and the switching speed of spintronic memristors. Spintronic memristors have many great potentials, but the ON/OFF ratio can be a bottleneck if not increased than current values. The same thing goes for resistive memristors, which needs more investigation of enhancing the endurance.

In order to benefit from the high scalability of memristive-based crossbar arrays, the problem of the sneak path must have reliable solutions without reducing scalability. Despite all of the current solution, the sneak path problem is still a major block that will probably delay this technology from finding its place in the market.

Specific model for each type of memristor with a focus on relating the model to the devices' physical parameters is highly required. The proposed model of spintronic memristor shows how different might be the behavior from memristor type to another one. Thus, investigating other types of memristors such as the manganite memristors will give us a better view of the advantages and limitations of each type.

The comparison of memristor types for different application excluded talking about the neuromorphic application. The neuromorphic application is –of course- an important memristor application. However, it was excluded as it needs a lot of simulations and to be well-covered, which is out of the scope of the thesis. Such comparison can be greatly beneficial for memristor-based neural networks.

Appendices

Appendix A

1. Thermal Fluctuation Aware Memristor Model:

```
// VerilogA for Thermal Fluctuation Aware Spintronic Memristor Model
// Parameter values are in SI units
`include "constants.vams"
`include "disciplines.vams"
module spintronic_memristor_Sherief(pos, neg, x_norm);
inout pos,neg, x_norm;
electrical pos,neg;
electrical x_norm;
branch (pos,neg) memristor;
real jeff;
real memristance;
real current_density;
real rL;
real rH;
real x;
real x_last;
real dxdt;
real first_iteration;
// Physical Constants
parameter real e=1.602e-19;
parameter real uB=9.274e-24;        // Bohr magneton (J/T)
// Matrial Parameters
parameter real Hp=5000*1e3/(4*3.1415);  // Hard Anisotroby "Converted from Oe to A/m"
parameter real Hk=100*1e3/(4*3.1415);   // Easy Anisotroby "Converted from Oe to A/m"
```

```
parameter real Ms=1010*1e3;        // Magnetization Saturation "Converted from emu/cm3 to A/m"
parameter real A=1.8e-11;          // Exchange Parameter (J/m)
parameter real Alpha=0.02155;      // Range from [0.002-0.1]
parameter real P=0.35;             // Polarization Efficiency
parameter real Gama=1.75e7;        // Gyromagnetic Ratio
parameter real Jcr=5e11;           // Critical current Density (A/m2)
// Model Parameters
parameter real D=1000e-9;          // Length
parameter real h=70e-10;           // Thickness
parameter real z=10e-9;            // Width
parameter real ReL=50;             // Low Sheet resistance (Ohm/m2) "at h=70A"
parameter real GMR=0.2;            // Giant Magnetoresistance ratio
//  time step
parameter real dt=200e-12;         // user must specify dt same as max step
 // size in transient analysis & must be at least 3 orders smaller than T period of the source  (Must be as small as 1e-3*Tsource)
parameter real init_state=0.2; // Initial value of the normalized state variable
parameter real Del=15000;   // dimensionless
parameter real Temp=300;
analog begin
  if(first_iteration==0) begin
  x_last=init_state*D; // if this is the first iteration, start with x_init
  memristance = rH*x_last + rL*(D-x_last);
  end
rL = ReL/z;
rH = rL*(1+GMR);
current_density = V(memristor)/(memristance*h*z);
   if(abs(current_density) > Jcr) begin
   jeff = current_density;
   end
```

```
  else if ((current_density < Jcr) && (current_density>0)) begin
  jeff = 1*Jcr/exp((Del/Temp)*(1-(current_density/Jcr)));
  end
  else if ((current_density > -Jcr) && (current_density<0)) begin
  jeff = -1*Jcr/exp((Del/Temp)*(1-(abs(current_density)/Jcr)));
  end
dxdt= P*uB*jeff/(e*Ms);
x=x_last+dxdt*dt;
  if(x > D ) begin
  x = D;
  end
  else if( x < 0 ) begin
  x = 0;
  end
memristance = rH*x + rL*(D-x);
x_last=x;
V(memristor) <+ I(memristor)*(memristance);
V(x_norm) <+ x/D;
first_iteration=1;
end
endmodule
```

2. LLGS-based Memristor Model:

```
// VerilogA for Memristor, LLGS-based spintronic memristor model
`include "constants.vams"
`include "disciplines.vams"
module LLGS_Memristor (pos, neg);
//terminal definitions
inout pos,neg;
electrical pos, neg;
branch (pos, neg) memr;
// variables
real  res, net_torque, efficiency, volume, rpar, RandomGaussian, Hfluctuation;
integer seed, Ni, sv_multiple;
real DW_width,DW_volume, RandomTheta, std_dev,N, Memres, Memduc;
// LLG equation coefficients
real h1, h2, h3, k1, k2, k3, s1, s2, s3;
real dmx_dt, dmy_dt, dmz_dt;
real mx, my, mz,sv,Icr,Ieff;
real V_dx, I_dx;
real Ms0,Ms,tmr0, Jc,Rp,Rap, Rp_DW,Rap_DW;
real Ps_nom, Ps0, Ps0_T, Ps_V_T,tmr0_T,
TMR_V_T,eff_AP_to_P,eff_P_to_AP;
// model parameters
parameter real plank_constant = 1.054e-27 from (-inf:inf);
parameter real electron_charge = 1.602e-19 from (-inf:inf);
parameter real gyromagnetic_ratio =  1.7608e7 from (-inf:inf);
parameter real alpha = 0.002 from (0:inf); // Range from [0.002-0.1]
parameter real Ms0_nom = 1050 from (0:inf);  // Magnetization Saturation
"emu/cm3 ": Ms0_nom(Vmemr=0) at room temperature
```

parameter real Hk = 250 from (0:inf);

parameter real Vh = 0.5 from (0:inf);

parameter real Aex= 1.8e-7; *// Exchange parameter converted from (J/m) to cgs by (*10^4)*

parameter real g=2; // G-Factor

parameter real ReL=50; // GMR low sheet resistance (Ohm/cm2)

parameter real Tc=1420; // Curie temperature (Kelvin)

parameter real alpha_sp=2e-5; // Material & Geometry dependent factor

parameter real beta=0.4; // material dependent

parameter real modifier=1; // modifier to adapt for Jcr if given (def=1)

parameter integer GMR_TMR= 1 from [0:1]; *// set this value = 0 for GMR or =1 for TMR*

parameter integer CIP_CPP= 1 from [0:1]; *// set this value = 0 for "current-in-plane" CIP or =1 for "current perpendicalr to plane" CPP "TMR is always CPP"*

parameter integer IPA_PPA= 1 from [0:1]; *// set this value = 0 for In plane Anisotropy (IPA) or =1 for Perpendicular to plane anisotropy (PPA)*

// Difference between IPA & PPA is in the critical current. To keep model generality, assume that in IPA, coordinatdes are rotated so that mz is the easy axis.

parameter real sv_init=0.51 from [0:1]; *// between [0,1], it will be approximated to nearest DW position.*

parameter real tmr0_nom = 2 from (0:inf); *// tmr0_nom = TMR(Vmem=0) at room temperature*

parameter real length = 500e-7 from (0:inf);

parameter real width = 60e-7 from (0:inf);

parameter real thickness = 1.5e-7 from (0:inf);

parameter real tox = 0.85e-7 from (0:inf);

parameter real F = 409405; // Fitting parameter of tunneling resistance (Fitted nominal size to Rp=1500)

parameter real Coef = 1.025;

parameter real Phi = 0.4; // Phi in eV

parameter real kb=1.38e-16; //Boltzman constant

parameter real T=300; //Temperature (Kelvin)

parameter real dt=2e-12; *// dt must be defined in cadence with the same value*

*// take dt <= (1/(10000*fmax))*

// model analog block

analog begin

volume = length*width*thickness; // FL volume

Ms0 = Ms0_nom / pow((1-300/Tc),beta);

Ms=Ms0*pow((1-T/Tc),beta);

DW_width=sqrt(2*Aex/(Ms*Hk)); // Neel DW width

Ni=length/DW_width;

N=Ni;

DW_volume=volume/N;

std_dev=sqrt(kb*T/(Ms*DW_volume*Hk)); *//standard deviation of theta "initialization"*

k1 = -1*gyromagnetic_ratio/(1 + pow(alpha,2));

k2 = -1*gyromagnetic_ratio*alpha/(1 + pow(alpha,2));

k3 = gyromagnetic_ratio*plank_constant/(2*electron_charge*Ms*DW_volume);

//conventional STT source (PL with easy axis parallel to FL)

s1 = 0;

s2 = 0;

s3 = 1;

// Polarization and TMR as a function of voltage and temperature

Ps_nom = sqrt(tmr0_nom/(tmr0_nom+2)); *// polarization at room temperature*

Ps0 = Ps_nom / (1-alpha_sp*pow(300,1.5)); // polarization at zero Kelvin

Ps0_T = Ps0*(1-alpha_sp*pow(T,1.5)); // Ps(0,T)

```
tmr0_T = 2*pow(Ps0_T,2)/(1-pow(Ps0_T,2)); // TMR(0,T)
TMR_V_T = tmr0_T / (1+pow((V(memr)/Vh),2)); // TMR(V,T)
Ps_V_T = sqrt(TMR_V_T/(TMR_V_T+2));
// IPA and PPA critical currents
eff_AP_to_P=Ps_V_T/(2*(1-pow(Ps_V_T,2)));
eff_P_to_AP=Ps_V_T/(2*(1+pow(Ps_V_T,2)));
if (IPA_PPA==0) begin
  if (V(memr) <= 0) begin // AP to P switching
    Icr = modifier* (g*electron_charge* alpha/(plank_constant*eff_AP_to_P))
*(Ms*volume)*(Hk+2*`M_PI*Ms);
  end
  else if (V(memr) > 0) begin // P to AP switching
    Icr = modifier*(g*electron_charge*alpha/(plank_constant*eff_P_to_AP))
*(Ms*volume)*(Hk+2*`M_PI*Ms);
  end
end
else if (IPA_PPA==1) begin
  if (V(memr) <= 0) begin // AP to P switching
    Icr = modifier*(g*electron_charge*alpha/(plank_constant*eff_AP_to_P))
*(Ms*volume)*Hk;
  end
  else if (V(memr) > 0) begin // P to AP switching
    Icr = modifier*(g*electron_charge*alpha/(plank_constant*eff_P_to_AP))
*(Ms*volume)*Hk;
  end
end
// CIP CPP Geometry
if (CIP_CPP==0) begin   // CIP & GMR
V_dx = res*V(memr)/(res+Rp*(sv-1/(2*N))+Rap*(1-sv-1/(2*N)));
```

```
I_dx=I(memr); // V_dx is the equiv memr voltage that achieves same switching delay as Aynaz model (V_dx=N*Vdw_dx)
// GMR resistance calculations
Rp = ReL*length/width;
Rp_DW = Rp/N;
Rap_DW = Rp_DW*(1+TMR_V_T);
res = Rp_DW + (Rap_DW-Rp_DW)*(1-mz)/2;
end
else if (CIP_CPP==1) begin // CPP
V_dx=V(memr);
I_dx= I(memr)/(1+res*((sv-1/(2*N))/Rp+(1-sv-1/(2*N))/Rap));
 if (GMR_TMR==0) begin  // GMR
   Rp = (ReL*length/width);
   Rp_DW = Rp*N;
   Rap_DW = Rp_DW*(1+TMR_V_T);
   res = Rp_DW + (Rap_DW-Rp_DW)*(1-mz)/2;
 end
 else if (GMR_TMR==1) begin //TMR Julliere Model
   Rp = (tox/(F*length*width*sqrt(Phi*electron_charge*1e7)))*exp(-Coef*tox*1e7*sqrt(Phi)); // Brinkman tunn barrier res model
   Rp_DW = Rp*N;
   res = 2*Rp_DW*(1+TMR_V_T)/(2 + TMR_V_T*(1+mz)); // Julliere Model
 end
end
// Net Tourqe calculation
if (abs(I(memr)) >= abs(Icr)) begin
Ieff=I_dx;
end
```

```
    else if (abs(I(memr)) < abs(Icr)) begin
    Ieff = 0;
    end
    efficiency = Ps_V_T/(2*(1 + pow(Ps_V_T,2)*mz));
    net_torque =  Ieff*efficiency;
    //Heff=Heff+Hfluctuation
    seed=25;
    RandomGaussian=$rdist_normal(seed, 0, 1);
    Hfluctuation=sqrt(2*alpha*kb*T/(gyromagnetic_ratio*Ms*volume))*Rando
mGaussian;
    h1= -4*`M_PI*Ms*mx+Hfluctuation;
    h2 = 0+Hfluctuation;
      h3 = Hk*mz+Hfluctuation;
if(analysis("ic")) begin
    //This defines the initial conditions for the   magnetization vector
    //fixed
    /*V(x) <+ 0;
    V(y) <+ 0.3;
    V(z) <+ sqrt(1 - 0.3*0.3);*/
    // random
    // seed=4;
    // RandomTheta=$rdist_normal(seed, 0, std_dev);
    mx= 0;
    my= sin(RandomTheta);
    mz= cos(RandomTheta);
    sv_multiple = sv_init*N;
    sv = sv_init;// sv_multiple/N+1/(2*N);
    if (sv >= 1) begin
```

```
    sv = 1-1/(2*N);
    end
end

else if(analysis ("tran")) begin
    dmx_dt = k1*(h3*my-h2*mz)+ k2*(-h1*my*my-h1*mz*mz+ h2*mx*my +h3*mx*mz) + k3*net_torque*(-s1*my*my-s1*mz*mz+ s2*mx*my+ s3*mx*mz);
    mx=mx+dt*dmx_dt;

    dmy_dt = k1*(h1*mz-h3*mx)+ k2*(h1*mx*my-h2*mx*mx-h2*mz*mz+ h3*my*mz) + k3*net_torque*(s1*mx*my-s2*mx*mx-s2*mz*mz+s3*my*mz);
    my= my+dt*dmy_dt;

    dmz_dt=  k1*(h2*mx-h1*my)+ k2*(h1*mx*mz+h2*my*mz-h3*mx*mx-h3*my*my) + k3*net_torque*(s1*mx*mz+s2*my*mz-s3*mx*mx-s3*my*my);
      mz= mz+dt*dmz_dt;

    if (V(memr)<0) begin
      if (mz>0) begin
        sv=  sv+1/N ;
        if (sv <= (1-1/(2*N)) ) begin
        mx = 0;
        my = 0;
        mz = -1;
        end
        else if (sv >= 1) begin
        sv= 1-1/(2*N);
        mx = 0;
        my = 0;
```

```
        mz = +1;
            end
      end
    end

    else if (V(memr)>0) begin
        if (mz<=0) begin
          sv= sv-1/N ;
         if (sv >= 1/(2*N)) begin
            mx = 0;
            my = 0;
            mz = +1;
         end
         else if (sv <= 0) begin
           sv = 1/(2*N);
          mx = 0;
          my = 0;
          mz = -1;
        end
      end
    end
end

Rap = Rp*(1+TMR_V_T);
if (CIP_CPP==0) begin
Memres=(res+Rp*(sv-1/(2*N))+Rap*(1-sv-1/(2*N)));
V(memr) <+ I(memr)*Memres;
end
```

```
else if (CIP_CPP==1) begin
Memduc=((1/res)+((sv-1/(2*N))/Rp)+((1-sv-1/(2*N))/Rap));
I(memr) <+ V(memr)*Memduc;
end
end
endmodule
```

Appendix B

Cadence Simulation Example:

Circuit: Memristor Training

PC Specs: Core i7 2.7 GHz , 8 GB RAM

Simualtion time : 12.5 Seconds

Transient simulation : Total time : 300 ns, time step : 1 ps.

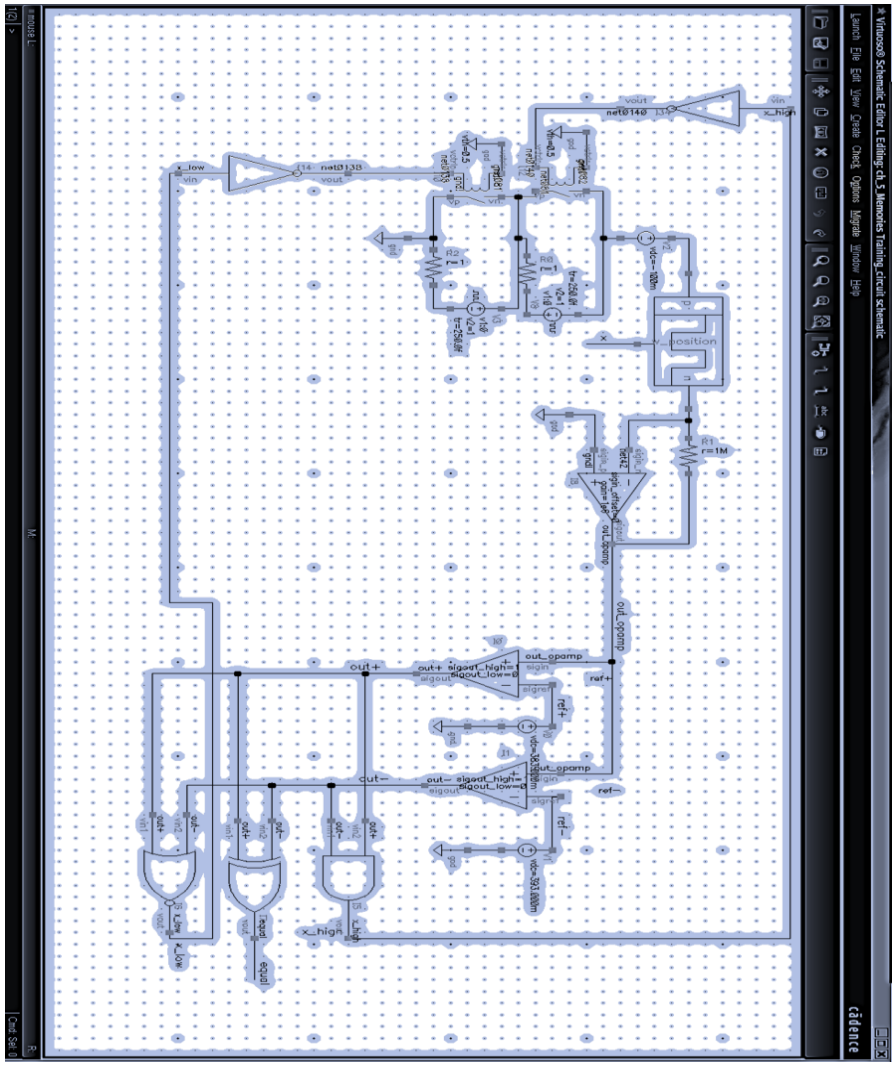


Figure B-1 Cadence schematic of the memristor training circuit.

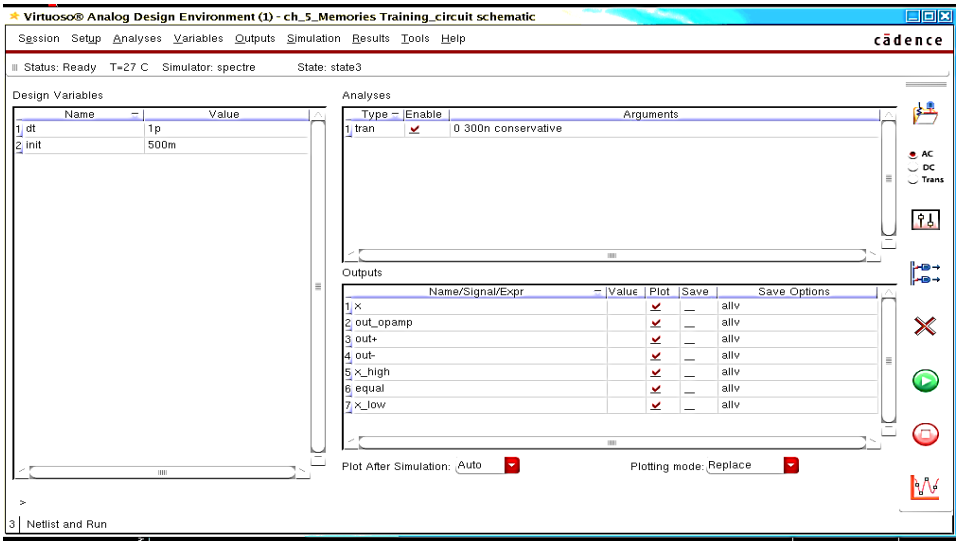


Figure B-2 The Analog Design Environment of the training circuit

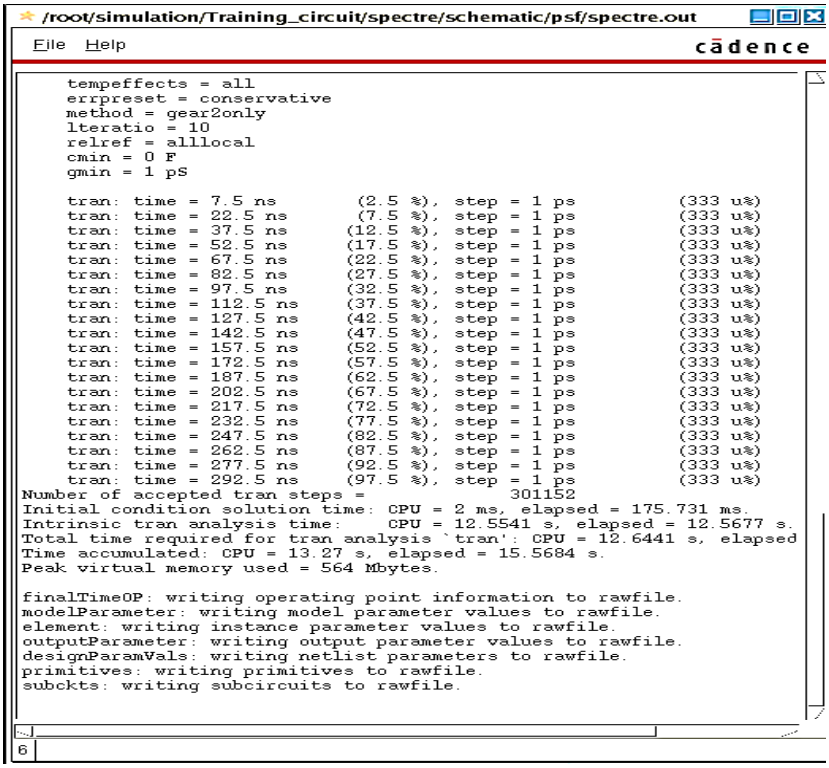


Figure B-3 The simulation output file of the training circuit.

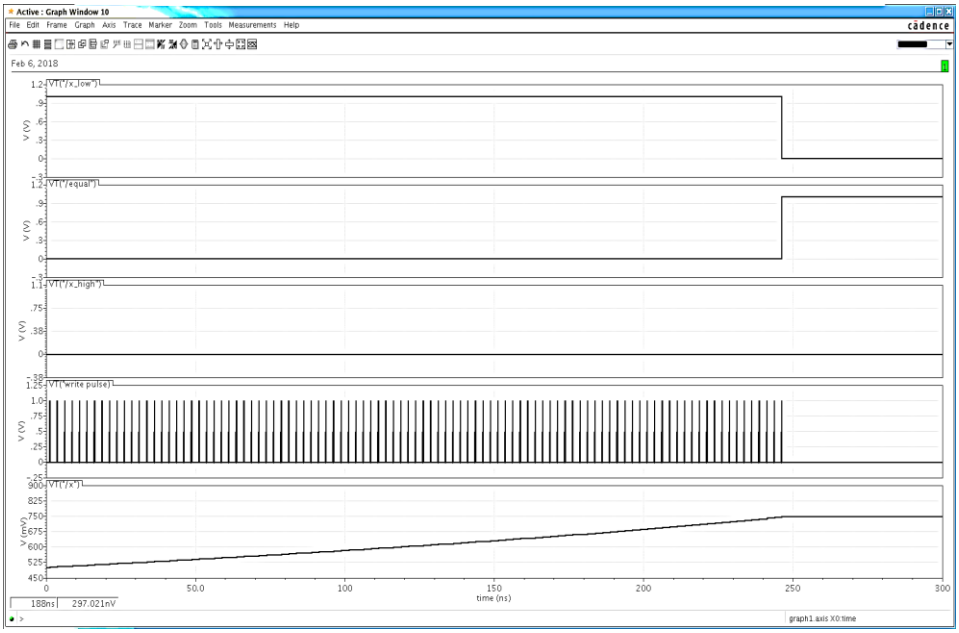


Figure B-4 The simulation results of the training circuit.

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