DESIGN OF FREQUENCY BASED ANALOG TO DIGITAL CONVERTER (FADC): NEW DESIGN METHODOLOGY FOR VOLTAGE-TO-FREQUENCY-CONVERTER (VFC) CIRCUITS

By

Mohammed Ahmed Ahmed Mahmoud ElGabry

A Thesis Submitted to the Faculty of Engineering at Cairo University in Partial Fulfillment of the Requirements for the Degree of MASTER OF SCIENCE in Electronics and Communications Engineering
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FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
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(Associate professor in the National Research Center)

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GIZA, EGYPT
2017
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**Title of Thesis:**

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**Key Words:**
Voltage to Time Converter (VTC); Voltage to Frequency Converter (VFC); Time to Digital Converter (TDC); Analog to Digital Converter (ADC); Software Defined Radio (SDR)

**Summary:**
In this thesis we introduce a new design methodology for Voltage-to-Frequency Converters (VFCs) circuits suitable for Time-Based Analog-to-Digital Converters (T-ADCs) circuits. This new methodology is tested using the parasitic after post layout using Cadence based on TSMC 65nm CMOS technology.
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I want to take the opportunity to show my deep appreciation, thanks and gratitude to my advisors Prof. Ahmed M. Soliman and Dr. Hassan Mostafa for their support, encouragement, patience, and guidance. As I learned too many things under their supervision and it was a great honor to work under their supervision.

Finally, I want to thank all my friends who supported me and helped me during the period of this work.
Dedication

I am dedicating this work to my family for their support, encouragement, attention, and providing me a good working environment. I want to thank them for their support, love and care. I owe them every achievement done in my life. Special thanks to my dear father and my caring mother for always giving me the guidance, support and love I always needed.
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List of Abbreviations

ADC  Analog to Digital Converter
VFC  Voltage to Frequency Converter
VTC  Voltage to Time Converter
CMOS Complementary Metal Oxide Semiconductor
DAC  Digital to Analog Converter
dB   Decibel
DNL  Differential Non Linearity
DR   Dynamic Range
DSP  Digital Signal Processing
ENOB Effective Number Of Bits
FDC  Frequency to Digital Converter
FS   Full Scale signal
INL  Integral Non Linearity
LSB  Least Significant Bit
MSB  Most Significant Bit
Op-amp Operational Amplifier
OSR  Oversampling Ratio
RF   Radio Frequency
S/H  Sample and Hold
SAR  Successive Approximation Register
SNR  Signal to Noise Ratio
SNDR Signal to Noise and Distortion Ratio
TADC Time based Analog to Digital Converter
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<td>VCO</td>
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<td>VDL</td>
<td>Vernier Delay Line</td>
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<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
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<td>LPF</td>
<td>Low Pass Filter</td>
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Abstract

Analog to digital converter (ADC) is a very important part in the mixed analog/digital systems since it acts as the interface between the external world (analog world) and the computer world (digital world). Designers are now trying to move towards the digital world where they make use of technology scaling in terms of area and gate delay, to be able to implement more complex applications; this approach leads to what is called software defined radio (SDR).

Software defined radio (SDR) concept is very important nowadays; where it is a radio communication system where components that are typically implemented in hardware (i.e. filters, amplifiers, modulators / demodulators, detectors, etc.) are implemented in software instead. A basic SDR system consists of a digital processing module equipped with analog to digital converter (ADC) proceeded by some of RF front end. The ultimate objective receiver design would be to connect an ADC to an antenna directly. A digital signal processing (DSP) module reads the converter, and then the software converts the obtained data stream from the ADC to the suitable format that will be used by the application.

According to the application requirements, designers can choose which type of ADCs is suitable for their application. Flash ADC, successive approximation ADC, Sigma delta ADC, pipelined ADC, and dual slope ADC are some types of conventional ADCs.

This ideal scheme is not reachable due to the actual technology limits, because the decrease in the voltage supply as a result of technology scaling results in difficulty in designing the conventional ADCs. With technology scaling; the decrease in the supply voltage is much higher than the CMOS threshold voltage. This makes the transistors cascading more difficult; therefore if we can convert the voltage to an intermediate form (time or frequency) and then convert it to digital, we use the benefits of the technology scaling to design the time-based ADC.

In this thesis; a comparative study between the two circuits (i.e., voltage to time converter (VTC) circuit and voltage to frequency converter (VFC) circuit) is introduced with respect to the sensitivity, linearity error, dynamic range, ENOB, SNDR, and maximum input frequency. It shows that VFC is better than VTC with respect to maximum input frequency, ENOB, SNDR, sensitivity and linearity error; however it consumes more power than VTC. A new design methodology is introduced for voltage to frequency converter circuit enhancing the sensitivity, linearity error, maximum input frequency, dynamic range, ENOB, and SNDR at the expense of area and power.
Chapter 1: Introduction

Analog to digital converter is a fundamental block in the mixed analog/digital systems. For example, in automotive sensor applications, ADC performs an important role in interfacing between the external world (analog world) and the digital world; where the sensors in vehicles sense the distance between it and another object and send this to the embedded system (computing system) that gives an alert to the driver to avoid accidents. Another example for ADC applications is in the medical applications, e.g. heart pacemaker. In addition, it is utilized in cellular phones, communication systems, etc. ADC becomes the system bottle neck as a result of technology scaling and the focus on digital systems, which results in decreasing the analog part in the system [1, 2, 3, 4, 5, and 6].

ADCs are divided into two types according to the method of conversion. The first type converts the analog input directly to digital output. The second type converts the analog input in an indirect way; first converts the analog signal to a transitional form like time or frequency, and then converts this transitional form to digital output. This thesis targets the second method. As VFC is better than VTC with respect to the maximum input frequency that can be introduced to the circuit without the need of sample and hold circuits, SNDR, ENOB and circuit sensitivity; it can be used in the RF applications.

The main challenge is to have an ADC that converts the analog signals and digital at a high rate and high accuracy.

1.1. Motivation

The improvement in the analog portion is small in comparison to the improvement in the digital portion; this is due to the technology scaling and the rapid increase of using SDR which is the reason of the rise of more complex applications [7, 8, 9, and 10].

Nowadays applications require having more complex processing methods that give the results with less power consumption and high accuracy. These applications lead to the decrease of the analog portion in the system; this results in putting the ADC in the front-end and using the digital signal processing (DSP) module to carry out the function.

Due to technology scaling the voltage supply decreases resulting in difficulty of implementing conventional ADCs using the new technologies. The decrease in the voltage supply leads to two problems. The first problem is that the signal to noise ratio becomes small as the noise level is not decreasing by the same rate as the voltage supply. The second problem is that the transistor threshold voltage is not decreasing by the same ratio as the voltage supply; this makes the transistors cascading more difficult.

A new avenue is introduced to take the benefit of technology scaling, high speed and low power consumption. This approach is to transform the analog signal to a transitional form such as time or frequency using VTC or VFC and then converting the resulted output to digital using time to digital converter (TDC) or frequency to digital converter (FDC).

1.2. Proposed work

In this thesis, a comparative study between Voltage-to-Time Converters (VTC) and Voltage-to-Frequency Converters (VFC) is introduced; both circuits are based on the current
starved inverter circuit. In addition, a new design methodology is introduced for the VFC circuits to enhance the sensitivity, linearity error, ENOB, SNDR, and maximum input frequency.

Current starved inverter circuit introduces an inherited sample and hold (S/H) to sample the input analog signal instead of using an external sample and hold. The prevalence of the inherent S/H is that it does not need an external hardware to build the TADC. It also assists the TADC to overcome some of the normal S/H disadvantages, such as introducing delay to the circuit input as each circuit introduces delay, and avoid adding noise to the VTC input voltage. However, the inherent S/H has some limitations and problems.

1.3. Organization of the thesis

This thesis is arranged as follows: Chapter 2 presents a review of ADC types and ADC characteristics used to judge the ADC whether this kind of ADC is suitable for the application requirement or not.

Chapter 3 presents time based analog to digital converter circuits that are proposed in other publications.

Chapter 4 presents a comparative study between voltage to time converter (VTC) and voltage to frequency converter (VFC). In this chapter we introduce the two circuits used for the voltage-to-time converter circuit and voltage-to-frequency converter circuit, the aspects that are used in the comparison between the two circuits, design recommendation and finally summarize the comparison between both circuits.

Chapter 5 introduces a new design for voltage-to-frequency converter circuit and a comparison between the proposed circuit and equivalent circuits that convert the voltage-to-frequency.

Finally, chapter 6 introduces a summary for the work done in the thesis, future work and the publications.
2.1. Analog to digital converter

ADC is the device used to convert continuous physical quantity (usually voltage) into a digital number that expresses the amplitude of the quantity. The conversion operates periodically (Samples). The conversion engages quantization of the input, so it necessarily originates a small amount of error. Figure 2.1 demonstrates a 3-bit ADC output. The result is converted from continuous time and amplitude analog signal into a discrete time and amplitude digital signal. ADC is usually characterized by its bandwidth and its signal to noise ratio.

The ADC performs four functions: Continuous time anti-aliasing filtering, Sampling, Quantization, Data coding.

2.1.1. Anti-aliasing filter

Anti-aliasing filter is a filter that acts prior to a signal sampler, to reduce the signal’s bandwidth to nearly meet the sampling theorem. The theorem declares that unambiguous interpretation of the signal from its samples is possible when the frequencies power above the Nyquist frequency is zero. A real anti-aliasing filter will commonly allow some aliasing to occur; the aliasing amount that appears depends on how good the filter is.

Anti-aliasing filter is mostly a low-pass filter. Figure 2.2 demonstrates an example of the anti-aliasing filter (low-pass filter). Figure 2.3 demonstrates the properties of the anti-aliasing filter.
2.1.2. Sampling

Sampling is the conversion of a continuous signal to a discrete signal. In the ADCs, Sample and Hold (S/H) [8] is used, where it samples the voltage of a regularly changing analog signal and freezes its value to a certain level for a specific minimum time period. S/H circuits are the fundamental analog memory devices; they are mainly used to discard variations in input signal that can corrupt the conversion process.

Sampling is performed with a persistent rate known as the sampling frequency $f_s$ as illustrated in Figure 2.4. The sampling must follow the Nyquist criterion which states that the frequency of the sampling has to be at least twice the maximum frequency of the input signal $f_{in}$.

$$f_s \geq f_{in} \quad (2.1)$$
If the system does not satisfy the Nyquist criterion, aliasing occurs, and it will not reconstruct the original signals from the samples taken. Figure 2.5 illustrates an example of wrong sampling and how the aliasing affects the reconstructed signal.

As a result of the wrong sampling, the constructed signal is not the same as the prime signal that was sampled. So to overcome the wrong sampling and to apply Nyquist criterion an anti-aliasing filter is used before the S/H. The anti-aliasing filter reduces the input signal frequency to half the sampling frequency.

### 2.1.3. Quantization

Quantization is the operation of limiting signal from a continuous set of values to a relatively small discrete set. Quantization is a displeasing incident as it introduces some non-linearity errors. The error introduced is called quantization error where it is the difference between the truly existing analog value and the quantized digital value. This error occurs because of the truncation of the analog value to the closest digital value.

The resolution of ADC is the minimal change in the input that results in change in the output digital value. Therefore, as the resolution of the ADC becomes smaller it results in small quantization error.

The resolution of ADC can be demonstrated as
\[ \text{LSB} = \frac{FS}{2^N} \]  

(2.2)

Where \( FS \) is the input full scale and \( N \) is the ADC bits number that can be generated to give the digital output value. Therefore, to decrease the quantization error of ADC the ADC resolution must be increased by increasing the number of bits. Figure 2.6 demonstrates an example of the quantization error.

Figure 2.6: Quantization error [11]

2.1.4. Data coding

Data coding is the conversion of the quantized values generated to digital value; i.e. the representation of the ADC output in bits. The bits number in which the output is represented is determined by the ADC resolution. Figure 2.7 demonstrates an example of the data coding for a 3-bit ADC, where \( E_{FSR} \) is the full scale of the signal.

Figure 2.7: Example for 3-bit ADC coding [12]
2.2. ADC characteristics

There are many types of ADCs, we have to judge which type of them is suitable for the application we are going to utilize the ADC in. ADC characteristics are the aspects that help in choosing the suitable type of ADC to a specific application.

ADC characteristics are detached into two parts; static characteristics and dynamic characteristics.

2.2.1. Static characteristic

ADC implementation introduces other errors rather than the quantization error; these additional errors are a result of the circuit. In this part we are reviewing the errors that are time independent.

2.2.1.1. Offset error

The offset error is the divergence of the ADC from the ideal ADC at input equals to zero. i.e., it can be demonstrated as the difference between the nominal and actual offset points. For ADC, the offset point is the mid-step value when the digital input is zero. Figure 2.8 demonstrates the offset error for ADC [1, 13, 14, and 15].

The offset error is introduced due to the offset voltage in the operational amplifier. This error acts on the digital output of the ADC; calibration can be done to eliminate the offset error.

![Figure 2.8: ADC offset error [1]](image-url)
2.2.1.2. Gain error

The gain error can be demonstrated as the diversity between the nominal and actual gain points on the transfer function after the offset error has been eliminated. For an ADC, the gain point is the mid-step value when the digital output is full scale. Figure 2.9 demonstrates the gain error for ADC [15, 16, 17, and 18].

![Figure 2.9: ADC gain error](image)

2.2.1.3. Differential non-linearity

The differential non-linearity error is the diversity between an actual step width (for an ADC) and the ideal value of 1 LSB. Therefore, if the width of the step is 1 LSB, then the differential non-linearity error is zero. If the DNL becomes more than 1 LSB, it is likely that the converter can become non-monotonic. This means that the magnitude of the output gets smaller with the increase in the magnitude of the input. Figure 2.10 demonstrates the DNL for ADC [19].

![Figure 2.10: ADC DNL](image)
2.2.1.4. Integral non-linearity

The integral non-linearity error is the divergence of the values on the actual transfer function from a straight line. For an ADC the divergence is calculated at the transition from one step to the following step. The name integral non-linearity is developed from the summation of the differential non-linearity from the bottom up to a specific step. Figure 2.11 demonstrates the INL for ADC [19].

![Figure 2.11: ADC INL [1]](image)

2.2.1.5. Missing code

The ADC is known to have a missing code when it misses one of the digital output codes. An ADC is guaranteed not to have a missing code if the maximum DNL is lower than 1 LSB or if the maximum INL error is less than 0.5 LSB. Figure 2.12 demonstrates the ADC missing code [20].

![Figure 2.12: ADC missing code [12]](image)
2.2.2. Dynamic characteristics

In this part we will discuss the errors that are time dependent.

2.2.2.1. ADC sampling rate

As the ADC is utilized to transform the signal from the analog form (continuous input) to the digital form (digital value), so it is mandatory to define a rate by which the analog input is sampled and converted to digital value, this rate is known as the sampling rate.

Sampling rate is a function of the time of the conversion of the ADC as it is the inverse of the time required by the ADC to complete the conversion from analog value to its equivalent digital value. Figure 2.13 demonstrates a sample of the sampling rate [21, 22, 23, and 24].

![Diagram of sampling rate](image)

**Figure 2.13: Example for sampling rate [12]**

2.2.2.2. Signal to noise ratio

Signal to Noise Ratio (SNR) is a way of measurement used to compare the level of wanted signal to the level of background noise. It is presented as the ratio of signal power to the noise power in dB; also it is usually used to refer to the ratio of useful information to awkward data in a conversation [25, 26, 27, and 28].

\[
SNR = 10 \log \left( \frac{Input \ power}{Noise \ power} \right) \ dB \tag{2-3}
\]

Noise power can be a result of the circuit noise and quantization noise. In case of quantization error only SNR can be given as

\[
SNR = 6.02N + 1.76 \ dB \ [1] \tag{2-4}
\]

This means that the SNR increases as the number of bits increase. Figure 2.14 shows an example of SNR.
2.2.2.3. Signal to noise and distortion ratio

Signal to Noise and Distortion Ratio (SNDR) is illustrated as the ratio between the signal power to the noise power and the distortion power. SNDR can be derived from

\[
SNDR = 10 \log \left( \frac{\text{Input power}}{\text{noise power} + \text{distortion power}} \right) \text{ dB}
\]  

(2-5)

Figure 2.15 shows an example of the Signal that has harmonic distortion [25, 26, 27, and 28].

Figure 2.14: SNR [1]

Figure 2.15: Signal with harmonics [1]
2.2.2.4. Effective number of bits

ADC circuits introduce distortion and noise because of the circuit and quantization noise. Effective number of bits (ENOB) \cite{25, 26, 27, 28} is the resolution of an ideal ADC circuit that would have the same resolution as the circuit under application. ENOB can be demonstrated as a function of SNDR as

\[
ENOB = \frac{SNDR_{dB} - 1.76}{6.02}
\]  

(2-6)

2.3. ADC types

As illustrated in Figure 2.16, ADCs are divided into direct conversion ADCs and indirect conversion ADCs.

Direct conversion ADCs converts the analog signal directly to digital code. However, an indirect conversion ADCs performs the conversion in an indirect way; first converting the analog signal into an intermediate representation, and then this intermediate representation is transformed into digital code.

According to the sample frequency rate, both direct and indirect conversion ADCs are divided into Nyquist rate ADCs and oversampling ADCs.

For Nyquist rate ADCs, the sampling frequency is equal to twice the maximum input frequency (the Nyquist frequency). For oversampling ADCs, the sampling frequency is very big in comparison to the input frequency.

Nyquist rate ADCs if compared with oversampling ADCs are usually good for applications requiring high frequency input signal. Oversample ADCs are usually good for applications calling for low frequency input signal but also require high resolution.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{Figure2.16.png}
\caption{ADC Classification \cite{1}}
\end{figure}
Flash ADC, successive approximation ADC are examples of Nyquist rate-direct conversion ADCs. Sigma-delta modulator (also known as a delta-sigma modulator) is a sample of oversampling-direct conversion ADCs. Dual slope ADC is a sample of Nyquist rate-indirect conversion ADCs. Voltage controlled oscillator time based analog to digital converter is a sample of oversampling-indirect conversion ADCs.

2.3.1. Nyquist rate ADCs

In this part, we will review some examples of the Nyquist rate direct conversion ADCs.

2.3.1.1. Flash ADC

Flash ADC is the fastest kind of ADCs. In this kind the input is compared with a \( 2^N - 1 \) reference values using \( 2^N - 1 \) comparators.

Figure 2.17 illustrates the implementation of flash ADC. In this figure it is demonstrated that each reference voltage differs from the reference voltage below it by 1 LSB. Each reference voltage is coupled to one of the comparator inputs while the other comparator input is connected to the analog voltage input. The comparator produces a ‘1’ when the analog input is larger than the reference voltage connected to the other comparator input, and it produces ‘0’ if the input analog voltage is less than reference voltage connected to the other input of the comparator. The comparators produce a thermometer code. The thermometer code is then decoded to the suitable digital output code [29, 30, 31, and 32].

![Figure 2.17: Flash ADC [4]](image-url)
The drawback of this kind of ADCs is that it needs a huge number of comparators compared to other kinds of ADCs, i.e. the comparators number is doubled with the increase of one bit resolution, resulting in consuming large area and more power. Therefore it becomes impractical for resolution more than 8 bits (255 comparators).

### 2.3.1.2. Successive approximation ADC

Successive approximation ADC is a widely spreading type in the ADC market for medium to high resolution ADCs [29, 30, 31, and 32].

Figure 2.18: SAR [1]

Figure 2.18 demonstrates the block diagram of successive approximation ADC. Successive approximation ADC includes a comparator, DAC, and successive approximation register (SAR).

A flow chart illustrating how the successive approximation works is portrayed in Figure 2.19 [29, 30, 31, and 32]. The SAR is first set to midscale (the most significant bit (MSB) is set to ‘1’). Thus, the output of the DAC is manipulated to be half the reference voltage. The output of the DAC is compared to the analog input sample, if the input voltage is greater than the DAC output, the comparator produces ‘1’ and the MSB of the SAR remains at ‘1’. Otherwise, the comparator produces ‘0’ and the MSB of the SAR is set to ‘0’. The SAR repeats the same process to the next lower bit and continues all the way down to the LSB. Once this is performed, the conversion is complete, and the N-bits digital word is accessible in the SAR.

The drawback of this kind of ADC is the linearly increase in the area with increase in resolution and Limited sampling rate.
Figure 2.19: SAR algorithm [1]
2.3.1.3. Pipelined ADC

Pipelined ADC has become the most popular ADC type utilized in high speed applications as its speed is almost the same as the Flash ADC, however it consumes less area and power, and its resolution is almost the same like the resolution of successive approximation ADC.

![Diagram of 12-bit pipelined ADC](image)

**Figure 2.20: 12-bit pipelined ADC [11]**

Figure 2.20 demonstrates a 12-bit pipelined ADC, where the ADC consists of five stages; each stage except for the last stage includes a 3-bits flash ADC, a S/H, a 3-bits DAC, a summer, and a gain block, while the last stage is 4-bits flash ADC. The S/H samples the output of the previous stage except for the first stage which samples the input voltage.

As demonstrated in Figure 2.20, the analog input, $V_{IN}$, is first sampled using a sample-and-hold (S/H), while the flash ADC in stage one converts the input into 3-bits. The 3-bits output are then propagated to 3-bits DAC, and the analog output generated from the DAC is subtracted from the input stage. The residue is then collected and supplied to the following stage (Stage 2). This collected residue progresses through the pipeline to provide 3-bits per stage until it reaches the 4-bits flash ADC.

As the bits from each stage are identified at various points in time, all the bits corresponding to the same sample are time aligned with shift registers before being supplied to the digital error correction logic. When a stage ends processing a sample, identifying the bits, and passing the residue to the following stage, it can then begin processing the following sample acquired from the sample and hold planted within each stage. This pipelining action is the reason for the high throughput.

The drawback of the pipelined ADC is that its area increases linearly with increasing the ADC resolution.

2.3.2. Oversampling ADCs

The oversampling conversion technique has recently become popular because it avoids many of the difficulties encountered with the conventional method for analog to digital conversion for example the use of anti-aliasing filters [11].

In this part we review one kind of oversampling ADCs, sigma-delta modulator.
2.3.2.1. **Sigma-delta ADC**

The basic concept of the sigma-delta ADC is the usage of high sampling rate and feedback to improve the effective resolution of the quantizer [11].

Sigma-delta ADC modulates the analog signal converting it into a simple code, usually single bit word at a frequency much higher than the Nyquist rate. The usage of high frequency modulation terminates the commitment for sharp cutoffs in the analog anti-aliasing filter at the ADC input [1].

The most important sigma-delta ADC characteristics is the oversampling ratio (OSR) which is described as the ratio of sampling frequency $f_s$ to the Nyquist frequency.

### 2.3.2.1.1. **First order sigma-delta ADC**

Figure 2.21 demonstrates the simplest sigma-delta ADC, the first order sigma-delta modulator. The circuit’s input is supplied to the quantizer through an integrator, and the quantized output is fed back to be subtracted from the input signal [1, 33, 34].

![Figure 2.21: First order sigma-delta ADC](image)

To simplify the analysis of the first order sigma delta ADC, let’s assume that the equivalent circuit portrayed in Figure 2.22 (i.e. the nonlinear operation of the ADC) is replaced with a linear one through the addition of signal $e[n]$ which represents the quantization error. Also it is assumed that the gain of the ADC and DAC are unity. The integrator is represented as the accumulation with unity gain.

![Figure 2.22: First order sigma-delta ADC model circuit](image)
The accumulator output can be written as

\[ w[n] = (x[n - 1] - y[n - 1]) + w[n - 1] \]  \hspace{1cm} (2-7)

and \( y[n] \) can be expressed as

\[ y[n] = w[n] + e[n] \]  \hspace{1cm} (2-8)

By substituting equation (2-8) in equation (2-7)

\[ w[n] = x[n - 1] - e[n - 1] \]  \hspace{1cm} (2-9)

Therefore, \( y[n] \) can be expressed as

\[ y[n] = x[n - 1] + (e[n] - e[n - 1]) \]  \hspace{1cm} (2-10)

As it is shown from equation (2-10), the output differentiates the quantization error, while leaving the input signal unchanged, except there is a delay.

2.3.2.1.2. Second order sigma-delta ADC

Figure 2.23 illustrates the second order sigma delta ADC. As it is demonstrated from the Figure the divergence between the first order sigma delta ADC and second order sigma delta ADC is the existence of another integral part and an extra feedback from the output [33, 34].

Applying the same analysis performed for the first order sigma delta ADC, the output can be written as

\[ y[n] = x[n - 1] + (e[n] - 2e[n - 1] + e[n - 2]) \]  \hspace{1cm} (2-11)

As it is shown from equation (2-11), the output differentiates the quantization error, but this time it makes the modulation error the second difference of the quantization error, while leaving the input signal unchanged, except there is a delay.
2.4. **Summary**

In this chapter, we introduced the ADCs’ characteristics and showed how these characteristics are measured and how they affect the judgment on the ADC used; these characteristics are classified into static characteristics which are time independent and dynamic characteristics which are time dependent.

ADCs are classified into four categories depending on the sampling method used in the conversion (oversampling or Nyquist sampling) and whether the conversion is direct (convention ADCs) or indirect (Time based ADCs). Examples for these direct ADCs including oversampling ADCs and Nyquist ADCs are introduced; showing the strength and weakness of each ADC.
Chapter 3 : Time based Analog to Digital Converter

Time based Analog to Digital Converter (TADC) circuits are the second type of ADCs that perform the analog to digital conversion on two steps, first it transforms the analog input to an intermediate form e.g. time or frequency, and then converting this intermediate form to the digital output. Therefore, TADC is a type of indirect conversion ADCs.

The decrease in the supply voltage because of the technology scaling leads to two problems. The first problem is the signal to noise ratio becomes small as the noise level is not decreasing by the same ratio as the supply voltage. The second problem is the transistor’s threshold voltage is not decreasing by the same ratio as the supply voltage leading to difficulty in implementing cascade transistors. TADC is a solution that overcomes these problems and can make benefit from the technology scaling and achieving an ADC with high SNR and low power consumption. There are a lot of researches and publications discussing the function of TADC and the design of TADC.

3.1. Nyquist rate TADCs

In this part, we are reviewing a sample of the Nyquist rate indirect conversion ADCs (TADCs).

3.1.1. Dual slope TADC

Dual slope ADC is a sample of the ADC that follows the Nyquist rate in the conversion. It is also defined as integrating converter. Its advantage is that it can be employed in high resolution applications, consumes less power, and less area as its area is not affected by increasing the resolution of the ADC. Dual slope ADC involves comparator, integrator, counter, and control logic as portrayed in Figure 3.1.

The input signal $V_{\text{in}}$, is supplied to an integrator to get the output voltage $V_{\text{out}}$; concurrently a counter is started, counting clock pulses. The correlation between the input voltage and the output voltage is demonstrated in equation (3-2). After a pre-determined amount of time $T_1$; a reference voltage $V_{\text{ref}}$ having a reverse polarity to $V_{\text{in}}$ is supplied to the integrator and the discharge starts until $V_{\text{out}}$ reaches zero, the discharge relies upon $V_{\text{out}}$ which relies upon $V_{\text{in}}$. The time required to discharge is proportional to $V_{\text{in}}$ according to equation (3-4) [35].

\[
V_{\text{out}} = \int_0^t -\frac{V_{\text{in}}}{RC} \, dt = \frac{V_{\text{in}} t}{RC} \quad (3-1)
\]

\[
V_{\text{out}}|_{T_1} = \frac{V_{\text{in}} T_1}{RC} \quad (3-2)
\]

\[
V_{\text{out}} = -\int_{T_1}^t \frac{V_{\text{ref}}}{RC} \, dt + \frac{V_{\text{in}} T_1}{RC} \quad (3-3)
\]

\[
V_{\text{out}} = \frac{V_{\text{in}} T_1}{RC} + \frac{V_{\text{in}} (T_1 - t)}{RC} \quad (3-4)
\]
By substituting \( V_{\text{out}} \) by zero in equation (3-4) it will result in the equation (3-5), where
\[
T_2 = T_1 - t
\]

\[
T_2 = \frac{V_{\text{in}}}{V_{\text{ref}}} T_1 \tag{3-5}
\]

As demonstrated in equation (3-5) the input voltage \( V_{\text{in}} \) is correlated to the pulse width, after that \( T_2 \) is converted to digital code using any ordinary method as used in other TADC types. The main advantage is that the dual slope ADC is independent of the RC; however, its drawback is its low sampling rate.

![Figure 3.1: Dual slope ADC](image)

3.2. Oversampling TADCs

Oversampling TADCs depend mainly on angular modulation like frequency or pulse position or pulse width modulation. In this part we are introducing some examples of oversampling TADCs [4].

3.2.1. Pulse Width Modulation ADC

Pulse Width Modulation (PWM) ADC is one of the eldest time based ADC. Its circuit is portrayed in Figure 3.2. The input signal is first pulse-width-modulated and then quantized with a counter. Pulse width modulation transfers amplitude domain signal information to the time domain (pulse width). Generally PWM creates signal distortion due to its nonlinear behavior; therefore, to avoid these nonlinearities, the modulation frequency is required to be at least 8 times larger than the bandwidth of the input signal leading to large power consumption.
3.2.2. Time based ADC

In this type the conversion is performed into two steps. The first step is converting the input voltage to time using either pulse width modulation or pulse position modulation; this is performed using Voltage-to-Time Converter (VTC) circuit. The second step is to convert the time representation generated from VTC to digital code; which is done using Time-to-Digital Converter (TDC) circuit. Figure 3.3 demonstrates the overall block diagram of the TADC [15].

3.2.2.1. Voltage to time converter

In this part a circuit is introduced that uses pulse width modulation. The signal is first pulse width modulated where the signal is converted to time using ramp generator and comparator. Figure 3.4 demonstrates the circuit utilized to transform the analog input to time representation.
The input is compared with a constant ramp; the comparator generates a pulse when the ramp and input intersects. The ramp is constant so the comparator pulse output is proportional to the input value (i.e., the time between the start of the ramp to the comparator pulse output is proportional to the input voltage). Figure 3.5 illustrates the waveform of the TADC.

![Figure 3.5: Waveform showing VTC operation](image)

### 3.2.2.2. Time to digital converter

For time to digital converter there are many circuits addressed in many publications trying to find a suitable TDC that satisfies high resolution, high dynamic range and consumes less power. In this part two examples of TDCs are introduced [36-44].

#### 3.2.2.2.1. Counter based TDC

Counter based TDC is one of the basic TDCs. It contains a simple counter which counts the number of complete cycles of a reference clock between the start and stop signal. One of its advantages is that it consumes small area; however, its major disadvantage is the need of a high speed counter to avoid errors as demonstrated in Figure 3.6. To achieve this high speed counter, we need a high frequency clock which consumes large power.

![Figure 3.6: Counter TDC error](image)
3.2.2.2. Two level Vernier delayed line

Vernier Delayed Line (VDL) demonstrated in Figure 3.7 is one of the most used Time-to-Digital Converters (TDC); however, its drawback is that it takes a long time in the conversion and requires a huge number of elements. To overcome these drawbacks a two level Vernier delayed line (VDL) is introduced [45, 46, 47, and 48], this proposed circuit reduces the time of conversion and decreases the delay elements number. Figure 3.8 demonstrates the block diagram of the proposed two level VDL.

The two level VDL consists of two levels; the first level performs coarse quantization with resolution $T_{CLK}/N$ and the second level performs fine quantization with resolution $T_{CLK}/N^2$, where $T_{CLK}$ and $N$ are the circuit clock and the delay elements number respectively.

The VTC output consists of two parts; integral part which is propagated to the counter and non-integral part which is propagated to the two level VDL. Figure 3.9 demonstrates the timing diagram of the integral and non-integral parts of the VTC. Where $T_{12}$ is the integral part while $T_1$ and $T_2$ are the non-integral parts.
The circuit uses the time interval between two rising edges (P_start and P_end). The control circuit portrayed in Figure 3.10 generates a step waveform to the VDL. The DLL controls the bias voltage for the delay elements. Figure 3.11 and 3.12 demonstrate the coarse and fine VDL respectively. for the coarse VDL the upper delay is $3T_{df}$ while the lower delay is $2T_{df}$; this results in a resolution of

$$T_{res} = 3T_{df} - 2T_{df} = T_{df} = \frac{T_{CLK}}{N} \quad (3-6)$$

for the fine VDL the upper delay is $T_{df}$ while the lower delay is $T_{ds}$ leading to a resolution of

$$T_{res} = T_{ds} - T_{df} = \frac{T_{CLK}(N+1)}{N^2} - \frac{T_{CLK}}{N} = \frac{T_{CLK}}{N^2} \quad (3-7)$$

The readout circuit uses the two level VDL circuit thermal code output and converts it into a digital code.

![Figure 3.9: Timing diagram [45]](image-url)
Figure 3.10: Control circuit [45]

Figure 3.11: Level one VDL (coarse quantization) [46]

Figure 3.12: Level two VDL (fine quantization) [45]
3.2.3. Frequency based ADC

In this type the conversion is performed into two steps. The first step is converting the input voltage to frequency by using frequency modulation; this is performed using Voltage-to-Frequency Converter (VFC) circuit. The second step is to convert the frequency representation generated from VFC to digital code which is done using Frequency-to-Digital Converter (FDC) circuit. Figure 3.13 demonstrates the overall block diagram of the frequency based ADC (FADC).

![FADC block diagram](image)

**Figure 3.13: FADC block diagram**

3.2.3.1. Voltage to frequency converter

Voltage controlled oscillator (VCO) is one of the circuits that is utilized to transform the analog input to frequency as it is considered a method of oscillation. Many circuits can be employed to implement the VCO like LC and ring oscillator which is preferred as it is simple in integration.

![VCO diagram](image)

**Figure 3.14: VCO diagram [1]**

As demonstrated in Figure 3.14, ring oscillator consists of a series of delay cells (inverter) which are linked together, and the ring is established by connecting the last delay cell output to the input of the first delay cell. To implement the ring oscillator it must be composed of odd number of delay cells (N must be odd).

To show the operation of the ring oscillator, let’s assume that the output of the first delay cell is zero. The first delay cell output is propagated to the second delay cell giving one at the output, following the same process at each stage; the output is an inverted version of the stage input till reaching the last delay cell giving its output zero. The last delay cell output is propagated to the first delay cell leading to one at its output, this output starts to propagate via the whole delay cells until the first delay cell output becomes zero and so on. It is demonstrated that it takes two loops to complete one period. Thus the period of oscillation T can be written as a function of the delay of the delay cell $t_d$ and the stages number N as

\[ T = 2Nt_d \]  

(3-8)
and the VCO frequency can be written as

\[ F = \frac{1}{T} = \frac{1}{2Nt_d} \quad (3-9) \]

The circuit described uses a multi-phase VCO, the usage of multi-phase VCO helps in increasing the resolution of the ADC.

Another example is the circuit proposed in [16] is based on ring oscillator which converts the input voltage to phase information as demonstrated in Figure 3.15. The frequency is controlled by the input voltage. The output phase of the VCO is the average input during the sampling period and is shown as

\[ \Delta \phi_{out} = 2\pi \int_{T_{s1}}^{T_{s2}} (K_{VCO}V_{in}(t) + F_{fr}) dt \quad (3-10) \]

Where \( K_{VCO} \) is the voltage-to-frequency gain, \( T_{s1}, T_{s2} \) are the sampling times and \( F_{fr} \) is the free running frequency of VCO when \( V_{in} = 0 \).

![Figure 3.15: VFC circuit [16]](image)

### 3.2.3.2. Frequency to digital converter

The frequency to digital converter is utilized to convert the modulated frequency generated from VFC to digital code. To perform this we can use a counter counting the rising and falling edges of the VCO, the counter’s output is the digital code of \( \Delta \phi_{out} \), the counter’s output feeds a digital code generator. However, the counter produces some quantization error; to defeat this quantization error a fine quantization is used.

The VCO output (\( \Delta \phi_{out} \)) is supplied to a phase detector with resolution \( \pi/N_{dcell} \), where \( N_{dcell} \) is the delay cells number in the ring VCO. The phase detector output feeds a digital code generator. The digital code generator combines the data from the counter (coarse quantization) and phase detector (fine quantization) and generates the digital code. Figure 3.16 demonstrates the block diagram of the whole ADC.
3.3. Summary

In this chapter we have introduced the time based ADCs, where the T-ADC consists of two main parts: the first part is converting the voltage signal to an intermediate form using VTC, and then converting this transient form to digital using TDC.

The intermediate form can be either time this is done using VTC or frequency using VFC. While converting the transient form to digital depends on the representation of the intermediate form; if the intermediate form is time TDC is used to convert the time to digital, while if the intermediate form is frequency, then FDC is used to convert the frequency to digital.

Examples for both circuits (i.e. VTC and VFC) are illustrated in this chapter showing the operation of the conversion and showing the circuits used in the conversion.
Chapter 4: A COMPARATIVE STUDY BETWEEN TIME BASED ADC AND FREQUENCY BASED ADC

As discussed in chapter 3 that the Time-based ADC (TADC) is a kind of the indirect ADC converter as it transforms the analog input to an intermediate representation and then converts this intermediate representation to digital code.

Also it was demonstrated that Time-based ADC (TADC) consists of two parts: the first part is transforming the voltage to time using Voltage-to-Time Converter (VTC) circuit and the second part is transforming the time obtained from VTC to digital using Time-to-Digital Converter (TDC) circuit. For VTC there are two ways to represent the voltage either by converting the Voltage-to-Time (VT) or Frequency (VF). The main supplement in this chapter is to demonstrate a comparative study between the two methods (i.e., the VTC circuit and the VFC circuit).

The aspects used in the comparison between the two circuits are dynamic range, maximum input frequency, linearity error, Effective Number Of Bits (ENOB), sensitivity, power consumption, and Signal to Noise and Distortion Ratio (SNDR) [48, 49, 50].

4.1. Circuit description

Several Voltage-to-Time Converter (VTC) circuits and Voltage-to-Frequency Converter (VFC) circuits are introduced. Most of these circuits depend on the simple current starved inverter portrayed in Figure 4.1. The simple current starved inverter utilizes an inherited sample-and-hold employed in the circuit. VFC is an inverter based ring oscillator [51], where the clock (CLK) of the circuit is the output feedback as portrayed in Figure 4.2. VTC uses the current starved inverter followed by two stage inverters to assure almost the same load of the circuit output similar to the VFC circuit for fair comparison as portrayed in Figure 4.3 [1, 48, 52, 53, and 54].

![Figure 4.1: Current starved inverter circuit [1]](image)
The simulations are performed using Cadence Virtuoso where industrial hardware-calibrated TSMC 65nm CMOS technology is used, with 1.2V as the supply voltage and through assigning the same design parameters for both circuits.

The CLK of the VTC circuit is 51 ns as the maximum pulse width that can be achieved within the dynamic range we are running on (0.12 V) is 50 ns. At the rising edge of the CLK, the current starved inverter output $V_{out}$ starts to decrease gradually relying upon the input voltage value ($V_{IN}$), then as $V_{out}$ crosses $V_{threshold}$ of the inverter which is $V_{DD}/2$ the output of the inverter will be $V_{DD}$ and will not be affected by any variation of $V_{IN}$ value till the subsequent rising edge of the CLK. This illustrates how the sample-and-hold operates inherently, where the sampling starts at the rising edge of the CLK and ends when $V_{out}$ crosses $V_{threshold}$ of the inverter, by crossing $V_{threshold}$ of the inverter the hold state begins and lasts till the next rising edge of the CLK [1, 55, 56].

4.2. Simulation results and comparative study

In this part we are viewing the simulation results and the comparison between Voltage-to-Time Converter (VTC) circuit and Voltage-to-Frequency Converter (VFC) circuit.
4.2.1. Dynamic range

Dynamic range is chosen to specify a linearity error less than 1% for both circuits as demonstrated in Figure 4.4 and Figure 4.5. The Dynamic range for both circuits equals to 0.12 V ranging from 0.68 V to 0.8 V.

![Figure 4.4: VFC linearity error is 0.66%](image1)

![Figure 4.5: VTC linearity error is 0.95%](image2)

4.2.2. Sensitivity (Linearity)

Most of the Analog to Digital converters suffer from non-linearity error, causing their output to go away from the linear functionality of their input. Sensitivity is measured for both circuits by performing a parametric sweep analysis for the input voltage within the desired dynamic range 0.12 V; the sweep analysis is operated by varying the input voltage between
0.68 V and 0.8 V. It is demonstrated that the VFC circuit enhances the sensitivity because of using the $CLK$ as the feedback from the output, resulting in high sampling frequency which leads to capturing more samples. The CLK is correlated to the input voltage which differs from the VTC circuit. It is demonstrated that VFC circuit is more sensitive to the input variations than the VTC circuit as demonstrated in Figure 4.6 and Figure 4.7. Sensitivity is the slope of the linear range, from the graph it is proven that the simulated results for VFC circuit is much linear than that of VTC circuit.

![Simulated results vs Ideal fitting line](image)

**Figure 4.6: VFC linearity error is 11.71 GHz/V**

![Simulated results vs Ideal fitting line](image)

**Figure 4.7: VTC linearity error is 0.2 ns/V**

### 4.2.3. Power

The consumption power is calculated at an input frequency ($F_{in}$) equals to 0.195 MHz (the maximum input frequency for VTC at 5-bits resolution) for both circuits. Since VFC uses its output as its $CLK$ leading to a better sampling frequency, it consumes more power than VTC. It is observed that the VTC circuit consumes less power than the VFC circuit, (i.e., VTC dissipates 418.5 $nW$, while VFC dissipates 171 $\mu W$).
4.2.4. Signal to Noise and Distortion Ratio (SNDR)

Signal to noise and distortion ratio (SNDR) is the measure used to compare the level of the desired signal to the level of the noise. It is also used on determining the ratio of the desired information to awkward data. It is determined as the signal power to the noise power and distortion in dB, the SNDR can be written as

\[
SNDR = 10 \log \left( \frac{\text{Input power}}{\text{noise power} + \text{distortion power}} \right) \text{ dB}
\]  

(4-1)

It is demonstrated that the VFC circuit is better than the VTC circuit with respect to the SNDR, (i.e., VTC introduces more noise as shown in Figure 4.9 than VTC does as shown in Figure 4.8.) This is due to the \(CLK\) in VFC being the feedback from the output leading to the increase in the current supplying the circuit resulting in enhancing the SNDR as explained in [57]. VFC consumes more current than what VTC consumes due to the feedback.

![Figure 4.8: VFC SNDR is 22.9 dB](image1)

![Figure 4.9: VTC SNDR is 16.1 dB](image2)
4.2.5. Effective Number Of Bits

Resolution of Analog to Digital converters (ADC) is the variety of discrete values that can be produced within the range of the analog values. The resolution of ADC is specified by the number of bits; these bits represent the number of levels that can be used to represent the analog values. The number of levels is a power of two; i.e., for \( N \) bits resolution we have \( 2^N \) levels to represent the analog values. However, ADC circuits generate noise and distortion.

ENOB is the resolution of an ideal ADC circuit that might have the same resolution as the circuit under consideration. ENOB can be expressed as function of SNDR as

\[
ENOB = \frac{SNDR - 1.76}{6.02}
\]  

(4-2)

VFC circuit shows better results than VTC circuit as a result of the feedback of the \( CLK \) in the VFC circuit leading to a higher sampling frequency. It is demonstrated that the ENOB value for VFC circuit is better than VTC circuit, (i.e., VFC ENOB is 3.8 bits, while VTC ENOB is 2.7 bits).

4.2.6. Maximum input frequency

The maximum input frequency is the frequency that may be used within the circuit while not having a significant error when the circuit is used without sample-and-hold. The maximum input frequency of VFC and VTC is evaluated via using sinusoidal input signals at multiples of the clock frequency (i.e., \( (4/3) * f_{CLK}, 2 * f_{CLK}, \) and \( 4 * f_{CLK} \)) as performed in [49]. The simulated results are portrayed in Figure 4.10 and Figure 4.11 where the delay and frequency error is plotted versus the input frequency.

The error for VFC is calculated as the deviation between the output frequency compared to the output frequency with DC input voltage equal to the sinusoidal input voltage at the sampling instant, while VTC is calculated as the deviation between the output pulse width compared to the output pulse width with DC input voltage equal to the sinusoidal input voltage at the sampling instant. The maximum tolerable error because of an input signal varying quickly all through the time when that signal is correctly being sampled is equal to one Least Significant Bit (LSB) of the ADC resolution [49]. For example, for 5-bits ADC resolution with an input dynamic range of 120 mV and a sensitivity of 0.2 ns/V for VTC and 11.71 GHz/V for VFC, one LSB corresponds to 3.75 mV (= 120 mV / 2^5) or 0.75 ps (= 3.75 mV * 0.2 ns/V) pulse width for VTC and 44.39 MHz (3.75 mV * 11.71 GHz/V) for VFC. Numerous traces indicating the maximum delay and frequency error for 5-bits, 6-bits, 7-bits, and 8-bits ADC resolutions are demonstrated in Figure 4.10 and Figure 4.11.
Figure 4.10: VFC max input frequency curve

Figure 4.11: VTC max input frequency curve
4.2.7. Design recommendation

By applying the comparative study between both circuits (i.e. VFC and VTC) taking into consideration the same design parameters to guarantee fair comparison, the results demonstrate that the VFC circuit shows better performance than the VTC circuit; however, the VTC circuit consumes less power than the VFC circuit. VTC circuit is preferred to be utilized in the applications which consume less power such as medical applications. While S/H circuit is required when using VTC circuits in applications requiring high input frequency. VFC circuit is preferable to be utilized in RF applications where it requires high input frequency; however, the drawback is consuming large power compared to VTC.

4.3. Summary

From Table 4.1 it is obvious that VFC circuit shows better performance than VTC circuit with respect to SNDR, the maximum input frequency, sensitivity, linearity error and ENOB at $F_{in}$ is 0.195 MHz. However, VTC circuit consumes less power compared to VFC circuit.

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>VFC</th>
<th>VTC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic range (DR)</td>
<td>0.12V</td>
<td>0.12V</td>
</tr>
<tr>
<td>Power</td>
<td>171 $\mu W$</td>
<td>418.5 $nW$</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>11.71 $GHz/V$</td>
<td>0.2 $ns/V$</td>
</tr>
<tr>
<td>Linearity error</td>
<td>0.66 %</td>
<td>0.95 %</td>
</tr>
<tr>
<td>Signal to noise and distortion ratio (SNDR)</td>
<td>22.9 $dB$</td>
<td>16.1 $dB$</td>
</tr>
<tr>
<td>Effective number of bits (ENOB) at $F_{in}$ = 0.195 MHz</td>
<td>3.8 $bits$</td>
<td>2.7 $bits$</td>
</tr>
<tr>
<td>Maximum input frequency at 5-bits resolution</td>
<td>100.4 $MHz$</td>
<td>0.195 $MHz$</td>
</tr>
</tbody>
</table>
Chapter 5: NEW DESIGN METHODOLOGY FOR VFC CIRCUIT

Many publications proposed many circuits trying to convert voltage to time, and according to chapter 4 it was illustrated that VFC circuit performance is better than VTC circuit. Therefore, in this chapter we are introducing a new design for voltage to frequency converter.

The proposed methodology is based on VFC as VFC is better than VTC with respect to the maximum input frequency that can be introduced to the circuit without the need of sample and hold circuits, SNDR, ENOB and circuit sensitivity as explained in [58]. The circuit introduced in [58, 59] depends on ring oscillator, where the output frequency is inversely proportional to the applied voltage input. The proposed methodology improves the sensitivity, ENOB, SNDR and maximum input frequency.

5.1. Motivation

A new methodology is introduced based on converting the voltage to time, the concept is to make use of the reciprocity between the NMOS based VTC known as falling circuit and PMOS based VTC known as rising circuit, both circuits are portrayed in Figures 5.1 and 5.2, the transistor Na1 in the falling circuit is used to limit the maximum discharge time in case Na2 threshold voltage is higher than $V_{IN}$. The clock of the reciprocal circuit (i.e. rising circuit) is a delayed and inverted version of the clock used with the falling circuit [60]; similarly Pb3 is used for the same reason as Na1. Figure 5.3 demonstrates the block diagram of the methodology, and the timing diagram is portrayed in Figure 5.4 [48].

![Figure 5.1: Falling Circuit](image)
Figure 5.2: Rising Circuit [4]

Inverter Delay Line

Figure 5.3: VTC methodology block diagram [4]
Figure 5.4: VTC timing diagram [48]

Where $T_{f_{th}}$, $T_{r_{th}}$, and $\Delta$ are the falling circuit delay, rising circuit delay, and the inverted clock version circuit delay respectively.

Simulation is performed comparing the three circuits (i.e. falling circuit, rising circuit, and the methodology) showing that the methodology is better than the other two circuits. Tables 5.1,
5.2, and 5.3 demonstrate the comparison results between the three circuits taking into consideration fixed dynamic range, fixed THD, and fixed linearity error.

### Table 5.1: Comparison results at Dynamic Range 0.55V

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>Falling</th>
<th>Rising</th>
<th>VTC methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linearity error</td>
<td>33.87%</td>
<td>5.85%</td>
<td>3%</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>$-4.77 \text{ dB}$</td>
<td>$-11.87 \text{ dB}$</td>
<td>$-20 \text{ dB}$</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>$0.64 \text{ mV/ps}$</td>
<td>$2.45 \text{ mV/ps}$</td>
<td>$2.13 \text{ mV/ps}$</td>
</tr>
</tbody>
</table>

### Table 5.2: Comparison results at THD -20dB

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>Falling</th>
<th>Rising</th>
<th>VTC methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linearity error</td>
<td>10.14%</td>
<td>3.6%</td>
<td>3%</td>
</tr>
<tr>
<td>THD</td>
<td>80mV</td>
<td>140mV</td>
<td>550mV</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>$0.64 \text{ mV/ps}$</td>
<td>$2.45 \text{ mV/ps}$</td>
<td>$2.13 \text{ mV/ps}$</td>
</tr>
</tbody>
</table>

### Table 5.3: Comparison results at linearity error 3%

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>Falling</th>
<th>Rising</th>
<th>VTC methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD</td>
<td>$-9.9 \text{ dB}$</td>
<td>$-12.45 \text{ dB}$</td>
<td>$-20 \text{ dB}$</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>240mV</td>
<td>400mV</td>
<td>550mV</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>$0.64 \text{ mV/ps}$</td>
<td>$2.45 \text{ mV/ps}$</td>
<td>$2.13 \text{ mV/ps}$</td>
</tr>
</tbody>
</table>

### 5.2. Circuit description

A new methodology based on VFC is introduced. The NMOS based Voltage-to-Frequency Converter (NVFC) is based on ring oscillator with NMOS transistor as the input stage to the circuit as portrayed in Figure 5.5. The input voltage is propagated to the gate of transistor MN2, the value of $V_{IN}$ controls the frequency of the output; the needed frequency to discharge the output capacitor is denoted by $F_N$, where the frequency of the output is directly proportional to the input voltage. PMOS based Voltage-to-Frequency Converter (PVFC) is introduced where the input voltage is propagated to the gate of MP1 as portrayed in Figure 5.6. The required frequency to charge the output capacitor is denoted by $F_P$, where the frequency of the output is inversely proportional to the applied input voltage. The new methodology relies upon the reciprocity between both circuits; where the output frequency is the difference between $F_N$ and $F_P$. The new methodology increases the ENOB, SNDR, sensitivity at the expense of power and area.
Figure 5.5: NMOS based VFC

Figure 5.6: PMOS based VFC

The methodology proposed can be practiced to any current starved inverter based VFC circuit found in the literature. To apply the methodology proposed, a reciprocal VFC circuit is
introduced (i.e., if the original VFC relies upon discharging the output capacitor, the reciprocal circuit should be introduced so that the output capacitor is charging, and vice versa). The outputs of the NVFC circuit and the PVFC circuit are propagated as inputs to a frequency mixer which is a NMOS transistor, where the output of the NVFC is linked to the drain of the transistor, and the PVFC output is linked to the gate of the transistor. The frequency mixer output frequencies are $F_N - F_P$ and $F_N + F_P$. To get the difference only, the output of the frequency mixer is propagated to a Low-Pass-Filter (LPF) as demonstrated in Figures 5.7.

![New methodology block diagram](image)

Figure 5.5 demonstrates the original VFC circuit denoted by the NMOS based VFC. Figure 5.6 displays the reciprocal VFC circuit of the original circuit portrayed in Figure 5.5, this reciprocal circuit is denoted by the PMOS based VFC. For a given input voltage, the output signal is $F_N - F_P$, where $F_N$ is the NMOS based circuit Frequency and $F_P$ is the PMOS based circuit frequency.

The sizing of the transistors is modeled to increase the term $F_N - F_P$. Accordingly, the design objective is to minimize the PMOS frequency ($F_P$); the effective transistor (MP1) in the PVFC circuit is modeled to be of minimum size. To increase the NMOS frequency ($F_N$); the NVFC circuit is modeled so that the load capacitor is discharged rapidly; this is achieved by increasing the input transistor (MN2) width.

### 5.3. Mathematical Analysis

The methodology proposed shows its strength by applying a complete analysis and comparison with the VFC circuits portrayed in Figure 5.5 and Figure 5.6. In the NMOS based VFC circuit, when the clock signal is zero, the load capacitor is charged to $V_{DD}$, transistors MN2 and MP1 are in the deep triode region, and transistor MN1 is in the cut-off region. When the clock rises, transistor MN1 turns on and the capacitor discharges through transistors MN2 and MN1 based on equation (5-1). The aim is to evaluate the delay needed to discharge the capacitor to the threshold voltage (i.e., $0.5 V_{DD}$) as demonstrated in the following equations.
\[ I_N = -C_L \left( \frac{dV_{out}}{dt} \right) \quad (5-1) \]

\[ I_N = I_{MN2} \quad (5-2) \]

\[ I_N = \frac{1}{2} \mu_n C_{ox} \frac{W_{MN2}}{L} [V_{IN} - V_{th}]^2 \quad (5-3) \]

\[-C_L \left( \frac{dV_{out}}{dt} \right) = \frac{1}{2} \mu_n C_{ox} \frac{W_{MN2}}{L} [V_{IN} - V_{th}]^2 \quad (5-4) \]

\[ \int_{V_{DD}}^{0.5V_{DD}} -C_L \, dV_{out} = \int_0^{T_{NMOS}} I_N \, dt \quad (5-5) \]

\[ T_{NMOS} = \frac{V_{DD} \cdot C_L}{2 \cdot I_N} \quad (5-6) \]

The same evaluation is performed for the PMOS based VFC circuit to evaluate the delay time; this is demonstrated in (5-12).

\[ I_P = -C_L \left( \frac{dV_{out}}{dt} \right) \quad (5-7) \]

\[ I_P = I_{MP1} \quad (5-8) \]

\[ I_P = \frac{1}{2} \mu_p C_{ox} \frac{W_{MP1}}{L} [V_{DD} - V_{IN} - V_{th}]^2 \quad (5-9) \]

\[-C_L \left( \frac{dV_{out}}{dt} \right) = \frac{1}{2} \mu_p C_{ox} \frac{W_{MP1}}{L} [V_{DD} - V_{IN} - V_{th}]^2 \quad (5-10) \]

\[ \int_{V_{DD}}^{V_{DD}} -C_L \, dV_{out} = \int_0^{T_{PMOS}} I_N \, dt \quad (5-11) \]

\[ T_{PMOS} = \frac{V_{DD} \cdot C_L}{2 \cdot I_P} \quad (5-12) \]

The inverter delay is given as

\[ T_{inverter} = \frac{1}{2} \left( \frac{V_{DD} \cdot C_L}{\mu_p C_{ox} \left( \frac{W}{L} \right)_p [V_{DD} - V_{th}]^2} + \frac{V_{DD} \cdot C_L}{\mu_n C_{ox} \left( \frac{W}{L} \right)_n [V_{DD} - V_{th}]^2} \right) \quad (5-13) \]

the delay for the NMOS based VFC circuit is shown in (5-14) while the delay of the PMOS based VFC circuit is shown in (5-15)

\[ T_N = T_{NMOS} + 2 \cdot T_{inverter} \quad (5-14) \]

\[ T_P = T_{PMOS} + 2 \cdot T_{inverter} \quad (5-15) \]
where $C_L$, $\mu C_{ox}$, $T_{NMOS}$, $T_{PMOS}$, $T_{\text{inverter}}$, $T_N$, and $T_P$ are the input capacitance of the following stage, the electrons mobility multiplied by the oxide capacitance, the time delay for NMOS based current starved inverter, the time delay PMOS based current starved inverter, the time delay for inverter, the time delay for NMOS based VFC circuit and the time delay for the PMOS based VFC circuit respectively. The frequencies of the circuits are expressed as

\[ F_N = \frac{1}{T_N} \]  
\[ F_P = \frac{1}{T_P} \]  
\[ F_{\text{meth}} = F_N - F_P \]

where $I_N$, $I_P$, $I_{MN2}$, and $I_{MP1}$ are the current of the capacitor in the NMOS based VFC circuit, the current of the capacitor in the PMOS based VFC circuit, the current of transistor MN2 and the current of transistor MP1 respectively; and $F_N$, $F_P$, and $F_{\text{meth}}$ are the frequency of the NMOS based VFC circuit, frequency of the PMOS based VFC circuit, and the frequency of the proposed methodology respectively. Taylor series expansions for $F_N$, $F_P$, and $F_{\text{meth}}$ are expressed in the coming equations. They aid in evaluating the linearity error effective parameters.

\[ F_N = a_0 + a_1 (V_{IN} - V_{\text{const}}) + a_2 (V_{IN} - V_{\text{const}})^2 + \cdots + a_n (V_{IN} - V_{\text{const}})^n \]  
\[ F_P = b_0 + b_1 (V_{IN} - V_{\text{const}}) + b_2 (V_{IN} - V_{\text{const}})^2 + \cdots + b_n (V_{IN} - V_{\text{const}})^n \]  
\[ F_{\text{meth}} = c_0 + c_1 (V_{IN} - V_{\text{const}}) + c_2 (V_{IN} - V_{\text{const}})^2 + \cdots + c_n (V_{IN} - V_{\text{const}})^n \]

where $a_i$, $b_i$, and $c_i$ are the ith terms of the Taylor coefficients for $F_N$, $F_P$, and $F_{\text{meth}}$ respectively and $V_{\text{const}}$ is the center point of Taylor expansion. The coefficients introduced in (5-19), (5-20), and (5-21) are used to evaluate their corresponding dynamic ranges and the total harmonic distortion (THD) as in [13].

5.4. Simulation results and discussions

VFC characteristics such as linearity, sensitivity, maximum input frequency, power consumption, ENOB and SNDR are evaluated by sweeping the input voltage. The simulations are performed using Cadence Virtuoso where industrial hardware-calibrated TSMC 65nm CMOS technology is used, with 1.2V as the supply voltage. The output of the NVFC circuit and PVFC circuit is demonstrated in Figures 5.8 and 5.9 respectively. Figure 5.10 demonstrates the output of all the mixer and LPF in the methodology, where the first curve demonstrates the output of the frequency mixer; the second curve demonstrates the LPF output. It is shown from the following tables that the new methodology provides better sensitivity than the other two circuits NVFC and PVFC.
Figure 5.8: PVFC output

Figure 5.9: NVFC output
Several simulations are performed to show the strength and the effectiveness of the new proposed methodology, Tables 5.4, 5.5 and Figures 5.11, 5.12 show the results of the simulations performed taking in consideration same linearity error showing that the new proposed methodology is better than the NVFC and PVFC circuits in the sensitivity, the maximum input frequency, SNDR, and ENOB. However, it dissipates much power than the other two circuits, more area than both circuits and less dynamic range (DR) than PVFC but better than NVFC. The methodology proposed enhances the sensitivity, the maximum input frequency, the dynamic range, the ENOB and the SNDR by factors of 1.97X, 1.1X, 1.6X, 1.5X and 1.4dB, compared to the original VFC circuit for the same linearity error.
Table 5.4: Comparison results at linearity error 3%

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>PVFC</th>
<th>NVFC</th>
<th>New methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic range (DR)</td>
<td>615 mV</td>
<td>205 mV</td>
<td>320 mV</td>
</tr>
<tr>
<td>Power</td>
<td>145.4 µW</td>
<td>331.7 µW</td>
<td>477.1 µW</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>11.88 GHz/V</td>
<td>21.9 GHz/V</td>
<td>43.24 GHz/V</td>
</tr>
<tr>
<td>SNDR</td>
<td>3.9 dB</td>
<td>9.96 dB</td>
<td>13.8 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>0.356 bits</td>
<td>1.34 bits</td>
<td>2 bits</td>
</tr>
<tr>
<td>Maximum input frequency</td>
<td>15.92 MHz</td>
<td>70.04 MHz</td>
<td>74.82 MHz</td>
</tr>
</tbody>
</table>

Table 5.5: Comparison results at linearity error 5%

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>PVFC</th>
<th>NVFC</th>
<th>New methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic range (DR)</td>
<td>660 mV</td>
<td>255 mV</td>
<td>430 mV</td>
</tr>
<tr>
<td>Power</td>
<td>140.1 µW</td>
<td>344.4 µW</td>
<td>484.5 µW</td>
</tr>
<tr>
<td>Linearity error</td>
<td>11.55 GHz/V</td>
<td>18.6 GHz/V</td>
<td>52.6 GHz/V</td>
</tr>
<tr>
<td>SNDR</td>
<td>4.4 dB</td>
<td>7.4 dB</td>
<td>7 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>0.44 bits</td>
<td>0.9 bits</td>
<td>0.88 bits</td>
</tr>
<tr>
<td>Maximum input frequency</td>
<td>11.94 MHz</td>
<td>70.04 MHz</td>
<td>53.03 MHz</td>
</tr>
</tbody>
</table>

59
Figure 5.11: SNDR at linearity error 3%, where (a) PVFC, (b) NVFC, (c) new methodology
Figure 5.12: SNDR at linearity error 5%, where (a) PVFC, (b) NVFC, (c) new methodology
Tables 5.6, 5.7 and Figures 5.13, 5.14 show the simulation performed taking into considerations the same dynamic range (DR), it also shows that the new proposed methodology is better than the other two circuits (NVFC and PVFC) in the sensitivity, maximum input frequency, ENOB and SNDR. However, it shows less linearity error than the PVFC but better than the NVFC; the new methodology results in improving the linearity error by 2.8X. The layouts for the three circuits are portrayed in Figure 5.15, 5.16 and 5.17.

Table 5.6: Comparison results at DR 0.3v

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>PVFC</th>
<th>NVFC</th>
<th>New methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linearity error</td>
<td>1.3 %</td>
<td>7.25 %</td>
<td>2.6 %</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>10.97 GHz/V</td>
<td>16 GHz/V</td>
<td>41.7 GHz/V</td>
</tr>
<tr>
<td>Power</td>
<td>140.1 µW</td>
<td>344.4 µW</td>
<td>484.5 µW</td>
</tr>
<tr>
<td>SNDR</td>
<td>10.1 dB</td>
<td>6.45 dB</td>
<td>13.8 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>1.4 bits</td>
<td>0.78 bits</td>
<td>2 bits</td>
</tr>
<tr>
<td>Maximum input frequency</td>
<td>189.5 MHz</td>
<td>353.1 MHz</td>
<td>551.6 MHz</td>
</tr>
</tbody>
</table>

Table 5.7: Comparison results at DR 0.13v

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>PVFC</th>
<th>NVFC</th>
<th>New methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linearity error</td>
<td>0.3 %</td>
<td>1 %</td>
<td>0.79 %</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>9.3 GHz/V</td>
<td>38.67 GHz/V</td>
<td>49.5 GHz/V</td>
</tr>
<tr>
<td>Power</td>
<td>226.6 µW</td>
<td>304.4 µW</td>
<td>668.2 µW</td>
</tr>
<tr>
<td>SNDR</td>
<td>1.77 dB</td>
<td>15.35 dB</td>
<td>9.24 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>0.0017 bits</td>
<td>2.26 bits</td>
<td>1.24 bits</td>
</tr>
<tr>
<td>Maximum input frequency</td>
<td>57.26 MHz</td>
<td>70.05 MHz</td>
<td>51 MHz</td>
</tr>
</tbody>
</table>
Figure 5.13: SNDR at linearity DR 0.3v where (a) PVFC, (b) NVFC, (c) new methodology
Figure 5.14: SNDR at linearity DR 0.13v where (a) PVFC, (b) NVFC, (c) new methodology
Figure 5.15: PVFC Layout

Figure 5.16: NVFC Layout
Figure 5.17: New methodology Layout

Figure 5.18 shows the output frequency from the proposed VFC circuit across different process corners, where the output frequency is maximum at FF-corner. Moreover, the minimum frequency is calculated at SS-corner. Figure 5.19 implies the effect of varying the temperature from -25 °C to 85 °C on the proposed VFC circuit. However, Figure 5.20 shows the circuit dependency on the supply variations that affects the main circuit functionality.

Figure 5.18: Process variation Frequency VS VIN
Figure 5.19: Temperature variation Frequency VS $V_{IN}$

Figure 5.20: Supply voltage variation Frequency VS $V_{IN}$
5.5. Summary

The methodology proposed enhances the linearity, the sensitivity, the maximum input frequency, the effective number of bits and the signal to noise and distortion ratio for VFC circuits. The methodology proposed relies upon increasing the slope of the frequency-input voltage curve that correlates the output frequency to the input voltage. This is achieved by using a VFC circuit reciprocal to the original VFC circuit and connecting both of them as demonstrated in Figure 5.7. The methodology proposed enhances the sensitivity, the maximum input frequency, the dynamic range, the ENOB and the SNDR by factors of 1.97X, 1.1X, 1.6X, 1.5X and 1.4dB, compared to the original VFC circuit at the same linearity error. Moreover, the methodology proposed enhances the linearity error by factor of 2.8X. However, the methodology proposed is under research to decrease the power and area overheads. The new circuit with the aspects in Table 5.8 is a result of applying the methodology proposed on the basic VFC circuit.

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic range (DR)</td>
<td>320 mV</td>
</tr>
<tr>
<td>Power</td>
<td>477.1 µW</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>43.24 GHz/V</td>
</tr>
<tr>
<td>Linearity error</td>
<td>3 %</td>
</tr>
<tr>
<td>SNDR</td>
<td>13.8 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>2 bits</td>
</tr>
<tr>
<td>Maximum input frequency</td>
<td>74.82 MHz</td>
</tr>
</tbody>
</table>
Chapter 6 : Conclusion and Proposed future work

In this chapter we are summarizing all what have been achieved in the thesis; the importance of the TADC is introduced and why it is nowadays one of the most important topics, a summary of the comparison performed between VFC and VTC, and the advantages of the new methodology introduced in this work.

6.1. TADC review

Time based analog to digital converter (TADC) is the type of ADCs that performs the analog to digital conversion on two stages, which is indirect conversion, first it transforms the analog input to an intermediate form e.g. time or frequency, and then converting this intermediate form to the digital output. Therefore, TADC is a type of indirect conversion ADCs.

Because of the technology scaling leading to the decrease in the supply voltage results in two problems: the first problem is that the signal to noise ratio becomes small since the noise level is not decreasing by the same rate as the supply voltage, the second problem is that the transistor’s threshold voltage is not decreasing by the same rate as the supply voltage; this makes the transistors cascading more difficult. Also nowadays all the researches performed are trying to reduce the analog part in the applications and increase the digital part so as to be capable of applying more complicated applications with less power consumption and less area.

TADC is a solution that overcomes these problems and can makes benefit from the technology scaling and achieving an ADC with high SNR and low power consumption. There are a lot of researches and publications discussing the function and the design of TADC.

TADC is detached into two parts; the first part is the translation of the signal to the intermediate form (time or frequency) either using Pulse Width Modulation (PWM) or frequency modulation, the second part is the translation of the output from the first part to digital form. The first part of the TADC can be done in two ways; either transforming the signal to time using Voltage-to-Time Converter (VTC) circuit or transforming the signal to frequency using Voltage-to-Frequency Converter (VFC) circuit, while the second part is done using Time-to-Digital Converter (TDC) circuit.

6.2. Comparison between VTC and VFC

A comparative study is performed between both circuits (i.e. VTC and VFC) to determine which circuit is better to be used according to the required applications. The main part in the two circuits is the current starved inverter which is considered the main part in most of the TADC circuits introduced.

The comparison is performed according to the main aspects of the ADCs; these aspects help designers to choose the correct kind of ADC for the required application. These aspects are sensitivity, dynamic range, linearity error, SNDR, ENOB, power consumption, and maximum input frequency. Table 6.1 demonstrates the comparison results between VFC and VTC.
Table 6.1: Comparison results between VTC and VFC

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>VTC</th>
<th>VFC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic range (DR)</td>
<td>0.12V</td>
<td>0.12V</td>
</tr>
<tr>
<td>Power</td>
<td>418.5 nW</td>
<td>171 μW</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>0.2 ns/V</td>
<td>11.71 GHz/V</td>
</tr>
<tr>
<td>Linearity error</td>
<td>0.95 %</td>
<td>0.66 %</td>
</tr>
<tr>
<td>Signal to noise and distortion ratio (SNDR)</td>
<td>16.1 dB</td>
<td>22.9 dB</td>
</tr>
<tr>
<td>Effective number of bits (ENOB) at $F_{in} = 0.195 \text{MHz}$</td>
<td>2.7 bits</td>
<td>3.8 bits</td>
</tr>
<tr>
<td>Maximum input frequency at 5-bits resolution</td>
<td>0.195 MHz</td>
<td>100.4 MHz</td>
</tr>
</tbody>
</table>

From the table it is obvious that VFC is better than VTC with respect to SNDR, ENOB, maximum input frequency, sensitivity, and linearity error. However, VTC shows better results than VFC with respect to consumption power. VTC is preferred in the applications that require less consumption power like the medical applications while in the RF applications it is preferred to use VFC as it requires high input frequency.

6.3. New methodology results

A new methodology has been introduced relying upon the VFC since VFC is proved to be better than the VTC in most of the aspects used in the comparison. The new methodology depends on the current starved inverter as it utilizes the inherited sample-and-hold in the circuit.

A comparison is performed between three circuits; the first circuit is NMOS based VFC (NVFC) where the input is applied to a NMOS transistor, the second circuit is PMOS based VFC (PVFC) where the input is applied to a PMOS transistor, and the third circuit is the new methodology which is a combination of the two circuits (i.e. NVFC and PVFC); the new methodology utilizes the reciprocity between the two circuits demonstrating results better than both circuits.

Several simulations are performed illustrating the power of the new methodology; where simulations are done taking into consideration fixed dynamic range and fixed linearity error. In these simulations it is illustrated that the new methodology is better than both circuits. However, the PVFC circuit is better than the new methodology with respect to the linearity error and dynamic range, but the new methodology shows better results in the other aspects compared to PVFC circuit. Tables 6.2 and 6.3 illustrate the simulation results between the three circuits.
Table 6.2: Comparison results at linearity error 3%

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>PVFC</th>
<th>NVFC</th>
<th>New methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic range (DR)</td>
<td>615 mV</td>
<td>205 mV</td>
<td>320 mV</td>
</tr>
<tr>
<td>Power</td>
<td>145.4 µW</td>
<td>331.7 µW</td>
<td>477.1 µW</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>11.88 GHz/V</td>
<td>21.9 GHz/V</td>
<td>43.24 GHz/V</td>
</tr>
<tr>
<td>SNDR</td>
<td>3.9 dB</td>
<td>9.96 dB</td>
<td>13.8 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>0.356 bits</td>
<td>1.34 bits</td>
<td>2 bits</td>
</tr>
<tr>
<td>Maximum input frequency</td>
<td>15.92 MHz</td>
<td>70.04 MHz</td>
<td>74.82 MHz</td>
</tr>
</tbody>
</table>

Table 6.3: Comparison results at DR 0.3v

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>PVFC</th>
<th>NVFC</th>
<th>New methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linearity error</td>
<td>1.3 %</td>
<td>7.25 %</td>
<td>2.6 %</td>
</tr>
<tr>
<td>Sensitivity (linearity)</td>
<td>10.97 GHz/V</td>
<td>16 GHz/V</td>
<td>41.7 GHz/V</td>
</tr>
<tr>
<td>Power</td>
<td>140.1 µW</td>
<td>344.4 µW</td>
<td>484.5 µW</td>
</tr>
<tr>
<td>SNDR</td>
<td>10.1 dB</td>
<td>6.45 dB</td>
<td>13.8 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>1.4 bits</td>
<td>0.78 bits</td>
<td>2 bits</td>
</tr>
<tr>
<td>Maximum input frequency</td>
<td>189.5 MHz</td>
<td>353.1 MHz</td>
<td>551.6 MHz</td>
</tr>
</tbody>
</table>

Table 6.4: Area calculations

<table>
<thead>
<tr>
<th>Comparison aspects</th>
<th>PVFC</th>
<th>NVFC</th>
<th>New methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>49.7 µm²</td>
<td>55.44 µm²</td>
<td>1325.34 µm²</td>
</tr>
</tbody>
</table>

From the tables it is illustrated that the new methodology is better than both circuits with respect to sensitivity, SNDR, ENOB, and maximum input frequency; however, its dynamic range and linearity error is less than the PVFC circuit but better than NVFC circuit. The new methodology consumes more power and area than both circuits as illustrated in Table 6.4.

6.4. Future Work

The drawback of the new methodology is that it consumes larger area and more power; the next step is trying to reduce the area of the new methodology and reduce the power consumption as much as possible.

Also as illustrated in chapter 5 the new methodology consists of a frequency mixer followed by a R-C low pass filter (LPF); the drawback is that the amplitude of the frequency mixer output and LPF output is decreased, also the capacitor uses large area (the main cause of the large area); the next step is to implement a frequency mixer and a LPF that have a gain to increase the amplitude of the output and reduce the capacitor value so decreasing the area but taking into consideration minimizing the consumption power.
6.5. List of Publications

Published


Submitted

References


Appendix A: Calculation of Sensitivity and Linearity error

1- From cadence open the ADEL.
2- Choose the analysis (time transient).
3- Enter the time you want to simulate.
4- Run the parametric simulation by varying the input (VIN) all over your dynamic range (e.g. 0.25V-1.2V), graphs for the different VIN will appear, Tools → Parametric Analysis.
5- Use the calculator tab to write a function that draws the pulse width or the frequency vs VIN as illustrated in Figures A.1 and A.2 respectively.

Figure A.1: Calculating the pulse width for the circuit output
Figure A.2: Calculating the Frequency for the circuit output

6- After getting the Delay or Frequency graph choose the graph from the tool bar menu choose Trace→save and choose the path where you want to save the file as illustrated in Figure A.3, you will have three options to save the graph

.VCV → this is related to cadence as when you close the graph and opens a new graph window instead of running the simulation from the beginning just load this VCV file.

.CSV → this will save the graph as an excel file where you can open it and apply any excel formulas on the data extracted; also you can use it in the matlab (importing it using the import wizard).

.matlab → this saves the graph as a matlab file where you can use it in matlab by using import function in the matlab.

Now we got the graph and saved it as a CSV or matlab file now we will use matlab to get the other results
7- Calculating the linearity error and sensitivity use the following code in matlab

```matlab
function [ Error,Linearity ] = lin_error( Filename)
    data = importdata(Filename);
    X = data.data(:,1);
    Y = data.data(:,2);
    Slope = polyfit(X,Y,1);
    new_y = polyval(Slope,X);
    error = abs((new_y - Y) / Slope(1))*100;
    Error = max(error);
    Linearity = abs(Slope(1));
    figure(1);
    plot(X,error);
    title(['Error Graph', 'ERROR = ', num2str(Error)]);
    xlabel('VIN v');
    ylabel('ERROR %')
    figure(2);
    plot(X,Y);
```
hold on;
plot(X,new_y,'g');
title('delay and linear')
xlabel('VIN v');
ylabel('Period sec');
end
Appendix B: Calculating ENOB and SNDR

1- Use the output extracted from Appendix A (i.e. delay or frequency) and enter it in matlab
2- Use the following Matlab code to calculate the ENOB and SNDR

function [ENOB , SQNR , freq_db ] = enob(samples ,Nbits )
% calculating the FFT
% the mean is subtracted to remove the DC component from the FFT output
% the "fftshift" function centers the FFT around Fs/2
freq = fftshift(abs(fft( samples - mean(samples) ,Nbits)));
freq_db = 20*log10(freq);
%figure; h =plot(freq_db);
% The signal is assumed to be presented in one peak ( one peak)
Spwr = max(freq)^2;
% Spwr is multiplied by 2 because there is 2 peaks centered around Fs /2
Npwr = sum(freq.^2) - Spwr *2;
SQNR = 10*log10(Spwr / Npwr);
% roughly, each 6db increase in the signal power means 1 bit increase in
% the ENOB value
ENOB = (SQNR-1.76) /6.02;
end
Appendix C: Layout and parasitic analysis

1- Launch the layout xl, a window will appear configure it as shown in Figures C.1 and C.2.

![Image](image.png)

**Figure C.1: Creating new layout**

![Image](image.png)

**Figure C.2: Write the same name of your circuit**
2- From the tool bar choose connectivity \(\rightarrow\) generate \(\rightarrow\) All from source. This will generate the layouts for all the components in the schematic, as shown in Figure C.3.

3- Connect the layouts as connected in the schematic.
4- After finishing the layout, run a DRC from Calibre “in the tool bar” \(\rightarrow\) Run DRC to check that there is no conflict with the technology spacing.
5- A window will open as shown in Figure C.4.
6- Navigate to your technology file used in your work (i.e. TSMC 65nm), as shown in Figure C.5.
7- Run the DRC and solve the errors that appear.
8- Run LVS check, this check guarantees that all the components in the schematic exists in the layout and are connected to each other correctly. Calibre → Run LVS.
9- A window will open to navigate to your technology file, as shown in Figure C.6.

Figure C.5: The path of the technology file DRC

Figure C.6: LVS technology file window
10- Navigate to your technology file, as shown in Figure C.7.

![Figure C.7: The paths of the technology file LVS](image)

11- After passing the LVS successfully, extract the parasitic via Calibre → Run PEX.
12- A window will open to navigate to your technology file, as shown in Figure C.8.

![Figure C.8: PEX technology file window](image)

13- Navigate to your technology file, as shown in Figure C.9.
After running the PEX a window will open, choose your technology cell map, as shown in Figure C.10.
Figure C.10: Choosing the technology cellmap file

15- Then click ok.
16- Two new views will appear to you (Layout and Calibre), as shown in Figure C.11
Figure C.11: Library manager showing the new views created

17- To use the parasitic in the library manager choose file \(\rightarrow\) new \(\rightarrow\) cell view, in the type choose config, as shown in Figure C.12.

Figure C.12: Creating new configuration

18- A window will open, in this window at the bottom press “Use template” button a window will appear as shown in Figure C.13.
Figure C.13: Use template window

19- In the name field choose “spectre”, as shown in Figure C.14, then press ok.
In the View tab choose “schematic” as shown in Figure C.15, then press ok.
21- A window will appear, in the “Tree View tap”, you will find your circuit, press R.Click and then you can choose between simulating without parasitic by choosing schematic or with parasitic by choosing caliber, as shown in Figure C.16.
Figure C.16: Navigation between the schematic and parasitic extraction
ملخص الرسالة

تعتبر محولات البيانات واحدة من أهم الأجزاء في الدوائر التي تجمع بين الإلكترونيات التناظرية والإلكترونيات الرقمية. حيث أنها الواجهة ما بين العالم الخارجي (العالم التناظري) وعالم الحاسب (العالم الرقمي)، يحاول المصممون الآن من التقليل من الإلكترونيات التناظرية واتجاه الى الإلكترونيات الرقمية حيث يمكن الاستفادة بقدر الإمكان من عملية التصغير المستمر للترانزستور. الإتجاه إلى إنشاء تطبيقات معقدة أدى إلى ظهور ما يسمى بدوار نظم الراديو المعرفة برمجيا. أصبح مفهوم دوائر نظم الراديو المعرفة برمجيا من أهم المفاهيم، والأبحاث في وقتنا هذا حيث يتم استبدال الأجزاء الإلكترونية التناظرية بأخرى رقمية.

الهدف الأساسي من استخدام نظم دوائر الراديو المعرفة برمجيا هو أن تتواجد محولات البيانات في المقدمة (متصلة مباشرة بالهوائي) لإستقبال الإشارات وتحويلها من تناظرية إلى رقمية. تقوم وحدة المعالجة الرقمية بإستقبال النتائج الناتجة من محول البيانات حيث تقوم بتحويلها إلى الشكل الذي يتطلبه التطبيق.

يعتبر الوصول للمخاطر المثالى صعباً نتيجة لحدود التكنولوجيا. أصبح من الصعب تصميم محولات البيانات التقليدية نتيجة التصغير المستمر لتكنولوجيا الترانزستور مما يؤدي إلى تقلص جهد المصدر، حيث أن جهد المصدر يتقلص بنسبة أكثر من نسبة تقليص الجهد المطلوب لتشغيل الترانزستور، مما يؤدي إلى صعوبة وضع الترانزستورات بشكل متتالي. ولذلك فإن امكان تحويل الإشارات التناظرية إلى شكل وسيط (مثل وقت أو تردد) من ثم تقوم بتحويلها الى إشارة رقمية فيمكننا الاستفادة من التصغير في تكنولوجيا الترانزستور.

في هذه الرسالة، نقوم بتقديم مقارنة ما بين محولات البيانات التي تقوم بتحويل الإشارات التناظرية إلى وقت ومحولات البيانات التي تقوم بتحويل الإشارات التناظرية إلى تردد، من حيث الحساسية للتغيير، الخطأ الخطي، نسبة الإشارة للضوضاء و التشويهات، أكبر تردد تتحمله الدائرة، و الطاقة؛ يتضح من هذه الدراسة أن محولات البيانات التي تقوم بتحويل الإشارات التناظرية إلى تردد أفضل من محولات البيانات التي تقوم بتحويل الإشارات التناظرية إلى وقت من حيث الحساسية للتغيير، الخطأ الخطي، نسبة الإشارة للضوضاء و التشويهات، أكبر تردد تتحمله الدائرة بينما أقل من حيث الطاقة.
أيضاً نقوم بعرض تصميماً جديداً لمحولات البيانات التي تقوم بتحويل الإشارات التناظرية إلى تردد حيث تقوم بتحسين النتائج من حيث الحساسية للتغير، الخطأ الخطي، نسبة الإشارة للضوضاء و التشويهات، أكبر تردد تتحمله الدائرة على حساب المساحة و الطاقة.
مهندسة:
محمد أحمد أحمد محمود الجبري
تاريخ الميلاد:
۹/۰۵/۹۸
 الجنسية:
مصري
تاريخ التسجيل:
۲۰۱۷/۱۰/۰۱
تاريخ المنح:
۲۰۱۷
القسم:
الإلكترونيات والاتصالات الكهربية
الدرجة:
ماجستير العلوم
المشرفون:
أ.د. أحمد سليمان
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عنوان الرسالة:
تصميم محول تناظري رقمي معتمد على صيغة التردد: طريقة تصميم جديدة لدوائر تحويل الجهد إلى تردد
الكلمات الدالة:
محول الجهد للوقت، محول الجهد لتردد، محول تناظري رقمي، نظم الراديو المعرفة برمجيا.
ملخص الرسالة:
في هذه الرسالة، نقوم بتقديم مقارنة ما بين محولات البيانات التي تقوم بتحويل الإشارات التناظرية إلى وقت ومحولات البيانات التي تقوم بتحويل الإشارات التناظرية إلى تردد، من حيث الحساسية للإختلاف، الخطأ الخطي، نسبة الإشارة للضوضاء والتشويهات، أكبر تردد تتحمله الدائرة، و الطاقة؛ يتضح من هذه الدراسة أن محولات البيانات التي تقوم بتحويل الإشارات التناظرية إلى وقت من حيث الحساسية للإختلاف، الخطأ الخطي، نسبة الإشارة للضوضاء والتشويهات، أكبر تردد تتقبله الدائرة بينما أقل من حيث الطاقة. أيضا نقوم بعرض تصميم جديد لمحولات البيانات التي تقوم بتحويل الإشارات التناظرية إلى تردد حيث تقوم بتحسين النتائج من حيث الحساسية للإختلاف، الخطأ الخطي، نسبة الإشارة للضوضاء والتشويهات، أكبر تردد تتحمله الدائرة على حساب المساحة و الطاقة.
تصميم محول تناظري رقمي معتمد على صيغة التردد: طريقة تصميم جديدة
لدوان تحويل الجهد إلى تردد

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رسالة مقدمة إلى كلية الهندسة - جامعة القاهرة
كجزء من متطلبات الحصول على درجة
ماجستير العلوم
في
هندسة الإلكترونيات و الإتصالات الكهربائية

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كلية الهندسة - جامعة القاهرة
الجيزة - جمهورية مصر العربية
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