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An accurate model of domain-wall-based spintronic memristor

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ABSTRACT

Spintronic memristors are promising devices that can be used in various applications such as memory chips and neuromorphic systems. The spintronic memristor combines the non-volatility advantage of resistive memristors, and the good scalability, and radiation hardness of spin-transfer torque magnetic devices. In addition, spintronic memristors can benefit from the maturity of integrating magnetic devices on top of CMOS devices. Current models of spintronic memristor only provide a similar version of the linear ion drift model of resistive memristors, which offers a simplified model, but with low accuracy and without enough linking to the device's physical parameters. In this paper, an accurate model of domain-wall- based spintronic memristor based on Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation is proposed. The proposed model provides a more accurate dynamical behavior by using the LLGS equation, and better relation to the device's physical parameters. It also uses the required equations that cover different types and geometries of spintronic memristors. The effect of the thermal fluctuations on device's parameters is also included into the model. The model uses the theory of domain-wall motion to explain the behavior of the device. Furthermore, a Verilog-A model is developed in order be compatible with IC CAD tools.

1. Introduction

In 1971, Professor Leon Chua reasoned from symmetry that there should be a fourth fundamental two terminal element completing the missing link between the electric charge (q), and the magnetic flux (Φ) as shown in Fig. 1 [1].

He denoted this element by “memristor” as a short term for “memory resistor”. Memristor's resistance changes based on the historical profile of the applied current or voltage. The memristor provides a distinguished pinched hysteresis current-voltage characteristic. In 2008, HP Labs announced a physical realization of a solid-state memristor using TiO_2 [2]. Since then, memristor devices gained a wide research interest for their unique properties such as their inherent nonvolatile property, which can be used effectively in the design of memory circuits.

1.1. Spintronic Memristor

Beside the resistive memristors, magnetic technology provides an alternative method to implement memristive systems [3,4]. Fig. 2 shows two possible realizations of the domain-wall (DW) based spintronic memristors.

The spintronic memristor shown in Fig. 2(a) was proposed by Wang et al. [3]. The device consists of two ferromagnetic layers separated by a strip of antiferromagnetic metal. The device geometry is current in-plane (CIP) in which the current flow is parallel to the memristor's interface between different layers. Another possible realization is the spintronic memristor shown in Fig. 2(b). It consists of two ferromagnetic layers separated by a thin insulator strip. This device was proposed by Miao Hu et al. in Ref. [4], and its geometry is a current perpendicular-to-plane (CPP) in which the current flow is perpendicular to memristor's

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interface between different layers.

In both structures, the ferromagnetic layers are denoted by the pinned layer (PL), and the free layer (FL). The magnetization direction in the PL is fixed. In the FL, the magnetization direction changes when the current passes through it.

The FL can be divided into three parts, a part with a parallel magnetization direction to the PL (P), a part with an antiparallel magnetization direction to the PL (AP), and a domain-wall (DW) part separating the parallel and the antiparallel parts. By changing the DW position, the memristance of the device is varied.

Spintronic devices are preferable for magnetic memories mature technology and good endurance [5]. However, resistive memristors such as TiO_2 memristors can provide higher ON/OFF ratios. Thus, the designer decision to choose between them depends on the design requirements of the ON/OFF ratio and the endurance.

Spintronic memristors are promising candidates for many applications such as neuromorphic circuits [6,7], memory chips [8–10], and temperature sensors [11]. In the field of memory circuits, spintronic memristors offer excellent scalability, and non-volatility properties, leading them to become one of the promising candidates for high-performance and high-density storage technologies. They can also be used in the field of logic circuits [12] and field programmable gate arrays (FPGAs) [13,14].

1.2. Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation

The Landau-Lifshitz-Gilbert (LLG) equation describes the dynamical behavior of the magnetization vector of magnetic materials according to the following relationship [15–17]:

$$\frac{\partial \vec{m}}{\partial t} = \frac{\gamma}{1+\alpha_g^2}\vec{H}_{eff} \times \vec{m} + \frac{\alpha_g \gamma}{\left(1+\alpha_g^2\right)}\vec{m} \times \left(\vec{H}_{eff} \times \vec{m}\right) \quad (1)$$

where $\vec{m}$ is the normalized magnetization vector, γ is the gyromagnetic ratio, α_g is the Gilbert damping parameter, $\vec{H}_{eff}$ is the effective magnetic field which includes the external field, the anisotropy field, and the thermal equivalent field.

The first term of the LLG equation represents the precession of the magnetization vector due to the applied magnetic field. The second term represents the damping phenomenon that tends to align the magnetization with the effective field.

In 1996, Slonczewski [18,19] indicated that spin-polarized electrons in magnetic devices experience a change in their angular momentum, resulting in a torque applied to the magnetization vector known as spin-transfer torque (STT). Therefore, a torque term should be added to the right-hand side of the previous equation to include this effect.

In this work, two types of STT are used, one for CIP devices as given in Eq. (2) [20–22] and the other for CPP devices as given in Eq. (3) [20,22,23]. One of these STT terms is added to the right-hand side of the LLG equation depending on whether the device is CIP or CPP.

$$\vec{T}_{CIP} = -\left(\vec{u}\cdot\vec{\nabla}\right)\vec{m} + \beta\vec{m} \times \left[\left(\vec{u}\cdot\vec{\nabla}\right)\vec{m}\right] \quad (2)$$

where $\vec{u}$ is the velocity of DW in the direction of electron motion; $u = Jg\mu_B P/(2eM_S)$ where J is the current density, g is the g-factor, μ_B is Bohr magneton, P is the polarization of the ferromagnetic material, e is the electron charge, and M_S is the saturation magnetization. The second term is denoted by the *beta term* which refers to the damping associated with the first term. The parameter β is much smaller than unity.

$$\vec{T}_{CPP} = -\frac{Jg\mu_B}{2eM_S\, t}\eta(\theta)(\vec{m} \times (\vec{m} \times \vec{m}_{PL})) \quad (3)$$

where t is the thickness of the free layer, η is the spin torque efficiency, θ is the angle between the easy axis of the magnet and the magnetization vector, and $\vec{m}_{PL}$ is the normalized magnetization vector of the pinned layer.

After adding the torque term, the equation is denoted by the Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation. This equation is able to model the dynamic behavior of magnetic devices accurately.

The spin-transfer torque effect is exploited in MTJ device forming a device denoted by spin-transfer torque magnetic tunneling junction

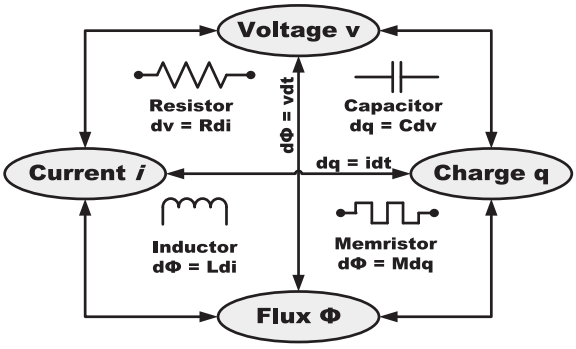

Fig. 1. Fundamental circuit variable relationships [1].

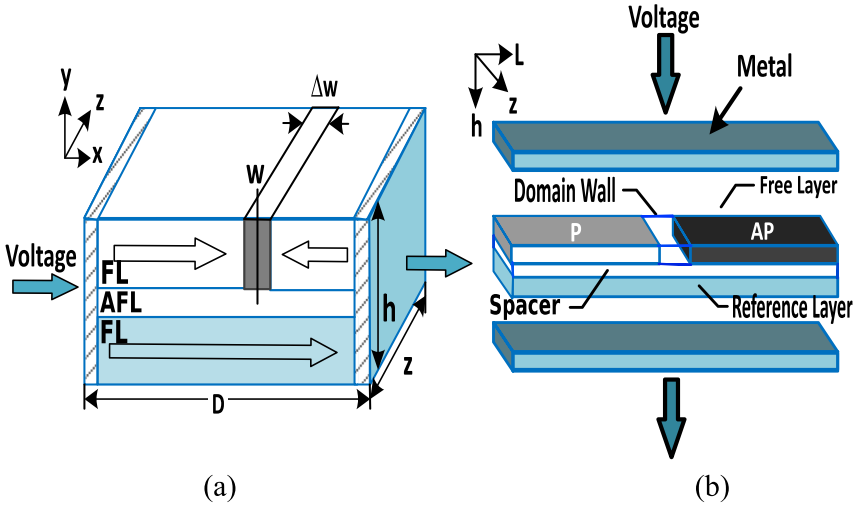

Fig. 2. (a) A spintronic memristor with CIP structure [3]. (b) Spintronic memristor with CPP structure [4].

(STT-MTJ). The main advantage of using the spin-transfer torque effect is that it requires lower current densities to achieve MTJ switching between P and AP states than other existing techniques, which makes this technique preferable in high-density MRAMs [24].

In this paper, a compact model of the DW-based spintronic memristor using LLGS equation is proposed. This model is implemented using Verilog-A, and is used with SPECTRE-based CAD tool to study its capabilities to investigate the dynamic behavior of the spintronic memristors.

The rest of the paper is organized as follows. Section 2 introduces a short survey on the previous models related to this work. Section 3 presents the proposed spintronic memristor model. Section 4 provides simulation results of the model and the model verification. Section 5 concludes the paper.

2. Previous spintronic memristor modeling

The spintronic memristor can be modeled using any empirical memristor model. However, there are only two available models - up to author's knowledge that use physical parameters related to the spintronic memristor devices.

The first model was proposed by Chen et al. [25] for the CIP spintronic memristors.

The second model is a CPP spintronic memristor model proposed by Miao Hu et al. [4]. Both models are similar, as the only difference is that Chen model uses two series resistors to model the spintronic memristor while Miao Hu model uses two parallel resistors.

2.1. Chen spintronic memristor model

Fig. 3 shows the structure of the CIP spintronic memristor (Fig. 3(a)) and its equivalent circuit (Fig. 3(b)) proposed by Chen et al. [25].

When the whole FL has a parallel magnetization vector to the PL, the resistance becomes lowest and is denoted by R_P. On the other hand, when the whole FL has an antiparallel magnetization vector to the PL, the resistance is the highest and it is denoted by R_{AP}.

When a part of the FL is in parallel state and the other part is in antiparallel state, the memristor can be modeled by two series resistors as shown in Fig. 3(b). The total memristance of the device is given by:

$$M(\alpha) = R_P\,\alpha + R_{AP}\,(1-\alpha) \tag{4}$$

where α is the relative DW position. It represents the "*state variable*" of this memristor and is equal to the ratio of the DW position (w) to the total length of the free layer (D) ($\alpha = w/D,\ 0 \le \alpha \le 1$).

The velocity of the DW motion (v) is proportional to the current density (J) passing through the memristor. It can be calculated as follows [25]:

$$v(t) = \frac{d\alpha(t)}{dt} = \Gamma_v\, J_{eff} \tag{5}$$

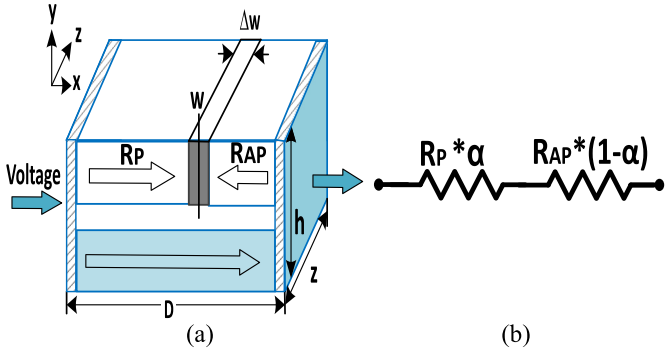

Fig. 3. CIP-based spintronic memristor (a) Structure (b) Equivalent Circuit [25].

where Γ_v is the DW velocity coefficient, and it is related to the device's structure and the material properties [25]. The value of Γ_v is estimated from the torque term of the LLGS equation for the CIP structure, and it can be expressed as [25]:

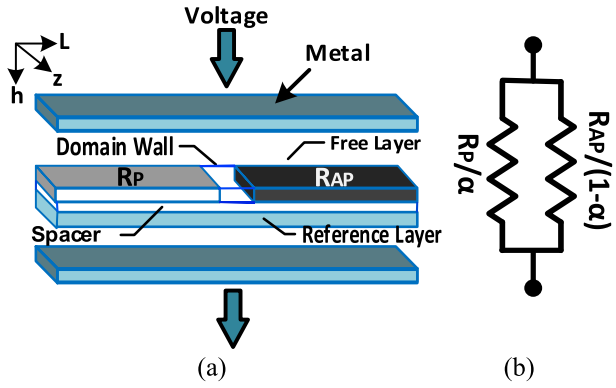

Fig. 4. CPP- based spintronic memristor (a) Structure. (b) Equivalent circuit.

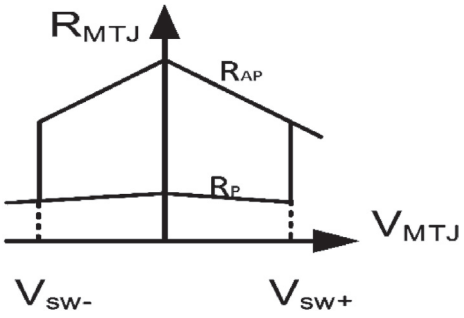

Fig. 5. MTJ device's resistance vs applied voltage [26].

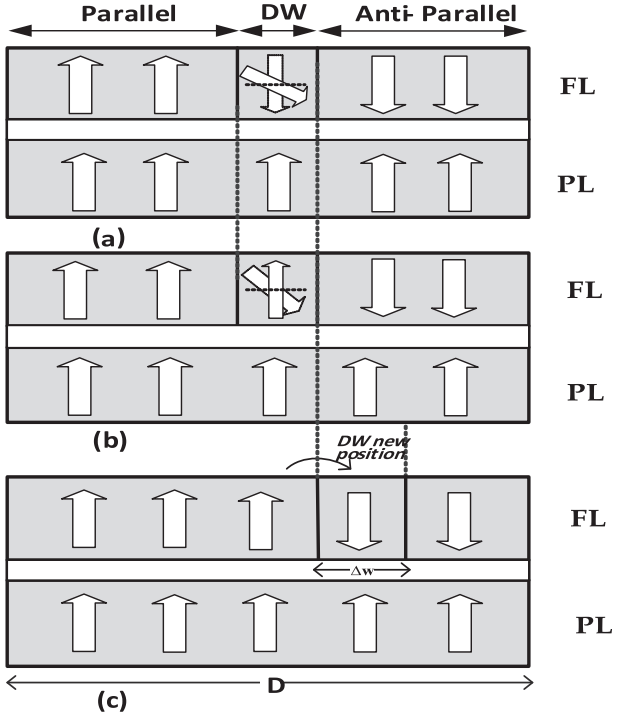

Fig. 6. Domain-wall motion at (a) the beginning of rotation. (b) DW fully switched. (c) DW moved to the new position.

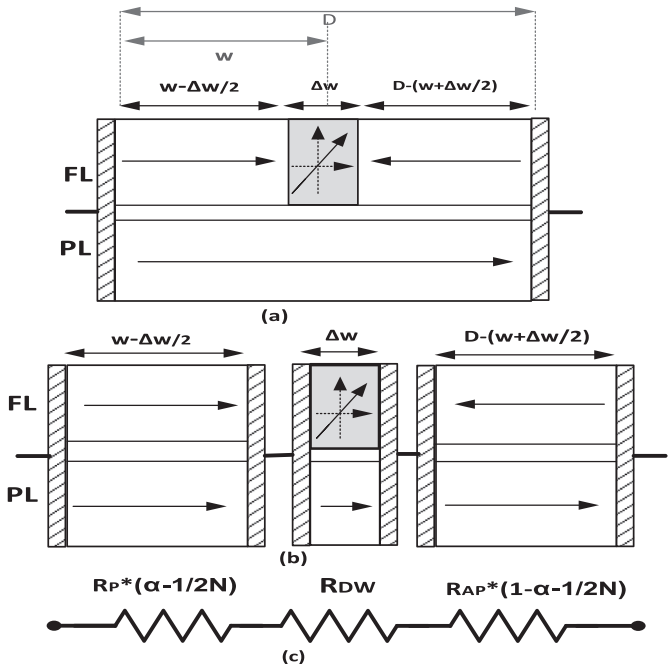

Fig. 7. CIP Spintronic Memristor. (a) Basic cell, (b) free layer division, and (c) equivalent circuit.

$$\Gamma_v = \frac{P\,\mu_B}{e\,M_S} \tag{6}$$

The effective current density (J_{eff}) is equal to J only when $J > J_{cr}$ as the current density only affects the DW position if it is higher than a specific critical value J_{cr}.

$$J_{eff} = \begin{cases} J\,; & J \geq J_{cr} \\ 0\,; & J < J_{cr} \end{cases} \tag{7}$$

This model is similar to the linear ion-drift model of the resistive memristors, but with a DW motion based on a simplification of the LLGS equation.

2.2. Miao Hu spintronic memristor model

Fig. 4(a) shows the structure of the CPP spintronic memristor proposed by Miao Hu et al. [4]. The equivalent circuit of this spintronic memristor is shown in Fig. 4(b). This model is similar to the Chen model except for using parallel resistors instead of series resistors as the structure is CPP. The DW separates the P and the AP parts of the free layer, and the model represents them as two parallel resistors R_P/α and $R_{AP}/(1-\alpha)$.

Thus, the overall memristance of the spintronic memristor can be calculated as follows [4]:

$$M(\alpha) = \frac{R_{AP}\,R_P}{R_{AP}\,\alpha + R_P\,(1-\alpha)} \tag{8}$$

The velocity of the DW motion (v) is calculated from Eq. (5) similar to the Chen model.

In both models, there are some assumptions that limit the model accuracy, and usage.

(1) As given in Eq. (5) and Eq. (6), the DW speed is derived from the LLGS equation of the CIP structure. Thus, it can predict the dynamic behavior of CIP memristors efficiently. On the other hand, the torque term of the CPP structure differs than the CIP torque and it can't provide accurate estimation of the dynamic behavior for the CPP spintronic memristors.

(2) Both models did not provide enough linkage to the physical parameters, structure, and dimensions of the spintronic memristor. A model with a direct relation to the magnetic material properties and device structure can be of a great impact on the studying and the manufacturing of the spintronic memristor. In addition, the proposed model allows the optimization of the spintronic memristor materials' properties and the design parameters at early design phases.

(3) Both models assumed that the antiparallel resistance R_{AP} has a fixed value. Actually, the antiparallel resistance in magnetic-based devices is strongly dependent on the applied voltage as shown in Fig. 5.

Eq. (9) provides an acceptable approximation for the tunneling magnetoresistance ratio (TMR) as a function of the applied voltage [27]. Taking the effect of the applied voltage on the TMR and R_{AP} is essential in spintronic memristors' modeling and it strongly affects the design of the spintronic memristor-based applications.

$$TMR(V) = TMR_0 \frac{1}{1 + \left(\frac{V}{V_h}\right)^2} \tag{9}$$

where TMR_0 is the tunneling magnetoresistance at zero volt, and V_h is the voltage at which the TMR is halved.

(4) The two models also did not consider the thermal dependent parameters of the spintronic memristor.

(5) Chen model is only applicable for CIP structures, and Miao Hu model is only applicable for CPP structures. A more generalized model that covers different possible structures of spintronic memristors is required to offer a standard model for the domain-wall spintronic memristors.

3. Proposed LLGS-based spintronic memristor model

The proposed model uses the LLGS equation to offer a more accurate representation of the memristor's dynamical behavior, especially for CPP structure, compared to the existing models that utilize a simplified form of the STT term from the LLGS equation.

The LLGS equation deals with the free layer of MTJ-based devices as one part that has a specific normalized magnetization vector **m**. The magnetization vector makes an angle θ with the easy axis (magnetization vector of the pinned layer). In case of modeling spintronic memristors, the LLGS equation is applied to the DW part only based on the theory of DW motion in nanostructures [28–30]. In order to use the LLGS equation in the modeling of spintronic memristors, the free layer is divided into three parts, a part with a magnetization vector parallel to the magnetization vector of the pinned layer, the DW, and a part of a magnetization vector antiparallel to the magnetization vector of the pinned layer.

The proposed model also uses the required equations that can represent all possible structures of spintronic memristors and link them to their physical parameters. The model included all the temperature dependent parameters up to the author's knowledge. The model also includes the voltage dependence of the TMR value.

3.1. The domain wall width and motion

The switching between P and AP states in spintronic memristors is based on the DW motion. The theory of operation is shown in Fig. 6. The LLGS equation is used to calculate the DW magnetization vector's relative angle to the easy axis of the memristor. If the STT effect exceeds the demagnetization field effect, the magnetization vector starts to rotate from AP to P state. When this magnetization vector reaches the parallel state as shown in Fig. 6(b), it is added to the parallel part of the free layer, and the DW position moves to the next position reducing the antiparallel

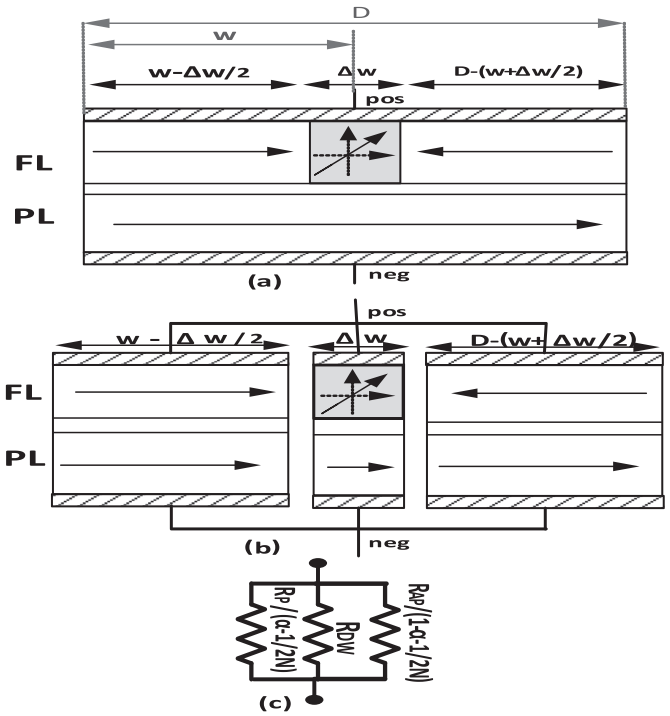

Fig. 8. CPP Spintronic Memristor. (a) Basic cell, (b) free layer division, and (c) equivalent circuit.

part width as shown in Fig. 6(c). The LLGS is applied again on the DW in its new position, and so on.

The same theory works for the DW when its magnetization vector rotates from P to AP state, but the motion is in the reverse direction reducing the parallel part and increasing the antiparallel part.

The DW type of the spintronic memristor is assumed to be a Néel type DW similar to Chen model [25]. In Néel DW type, the magnetization vector rotates in the plane of transition as shown in Fig. 6. The Néel DW width can be calculated as follows [21,25]:

$$\Delta w = \sqrt{\frac{2A_{ex}}{M_S H_K}} \tag{10}$$

where A_{ex} is the exchange parameter and H_K is the anisotropy field.

Thus, the FL has '*N*' DW positions. The number of DW positions (*N*) considered in our approach equals:

$$N = \frac{D}{\Delta w} \tag{11}$$

It should be noted that the DW of narrow-width spintronic devices is usually a mix between the Néel and Bloch DW types [31], and thus estimating the DW width from (10) is an approximation. If an experimental data is offered, it is better to use the value of the DW width from the experimental results.

3.2. The CIP and CPP structures

The spintronic memristor can be a CIP structure like the spintronic memristor proposed by Chen et al. [3] or CPP structure like the one proposed by Miao Hu et al. [4]. Fig. 7(a) shows a spintronic memristor of a CIP structure. The CIP spintronic memristor is equivalent to three resistors connected in series representing the P, AP, and DW parts, as shown in Fig. 7(b). This is the same assumption used by the Chen model, except that the DW resistance is included as a standalone part. In Chen model, the DW part is assumed to be divided equally between the P and AP parts [25].

Fig. 7(c) shows the equivalent circuit that is used by the proposed model for the spintronic memristors with a CIP structure. The first resistor R_P *(α-1/2 N)* is the equivalent resistor of the P part. The DW part has a resistance of R_{DW}, and it is calculated depending on whether the memristor type is GMR or TMR. The AP part is modeled by the resistance R_{AP} *(1-α-1/2 N)*. The derivation of this model is straightforward, as for a resistor *R*, $R = \rho\, L/A$.

Thus, the ratio of the P part resistance to the total resistance is $R_{P\text{-}part}/R_P = L_{p\text{-}part}/L_{tot}$. Thus, the P part resistance is given by:

$$R_{P\_part} = R_P \frac{w - \frac{\Delta w}{2}}{D} = R_P\left(\alpha - \frac{1}{2N}\right) \tag{12}$$

where *w* is the DW position at the center of the DW which has a width of *Δw*.

Similarly, the AP part equivalent resistance is:

$$R_{AP\_part} = R_{AP}\left(\frac{D - \left(w - \frac{\Delta w}{2}\right) - \Delta w}{D}\right) = R_{AP}\left(1 - \alpha - \frac{1}{2N}\right) \tag{13}$$

The antiparallel resistance R_{AP} is calculated from the following equation:

$$R_{AP}(V) = R_P(1 + TMR(T, V)) \tag{14}$$

where *TMR (T, V)* is the tunneling magnetoresistance ratio as a function of temperature and voltage.

Thus, the total memristance can be calculated as follows:

$$M(\alpha) = R_P\left(\alpha - \frac{1}{2N}\right) + R_{DW} + R_{AP}\left(1 - \alpha - \frac{1}{2N}\right) \tag{15}$$

Similarly, the equivalent parallel resistance of the DW R_{P_DW} is calculated as follows:

$$R_{P\_DW} = R_P\left(\frac{\Delta w}{D}\right) = \frac{R_P}{N} \tag{16}$$

The R_{P_DW} value is to be used in the calculation of the DW resistance R_{DW}.

Fig. 8(a) shows a spintronic memristor of a CPP structure. In contrast to the CIP structure, the device area is divided into the three parts instead of the length.

Thus, $R_{P\_part}/R_P = A_{tot}/A_{p\_part}$. Thus, the P part resistance equals:

$$R_{P\_part} = R_P\left(\frac{D}{w - \frac{\Delta w}{2}}\right) = \frac{R_P}{\left(\alpha - \frac{1}{2N}\right)} \tag{17}$$

Similarly, the AP part equivalent resistance is:

$$R_{AP\_part} = R_{AP} \times \frac{D}{D - \left(w - \frac{\Delta w}{2}\right) - \Delta w} = \frac{R_{AP}}{\left(1 - \alpha - \frac{1}{2N}\right)} \tag{18}$$

The total memductance *W(α)* can be calculated as follows:

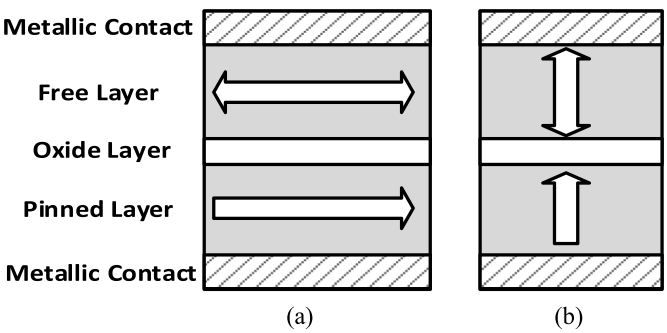

Fig. 9. Spintronic Memristor (a) IMA structure. (b) PMA structure.

$$W(\alpha) = \frac{\left(\alpha - \frac{1}{2N}\right)}{R_P} + 1/R_{DW} + \frac{\left(1 - \alpha - \frac{1}{2N}\right)}{R_{AP}} \tag{19}$$

where $W(\alpha) = 1/M(\alpha)$.

The area of the DW is $(1/N)$ times of the total FL area. Thus, the R_{P_DW} in the CPP structure is calculated as follows:

$$R_{P\_DW} = R_P\left(\frac{D}{\Delta w}\right) = N\,R_P \tag{20}$$

3.3. Thermal dependent parameters

Some magnetic parameters are affected by thermal fluctuations. Thus, including the temperature dependence to the magnetic parameters is important to study the thermal fluctuations effect on spintronic memristors. In the proposed model, the effect of the temperature variations on the magnetization saturation M_S, the spin-polarization P_S, and the magnetoresistance ratio (TMR/GMR) are included.

The temperature dependent magnetization saturation can be calculated as follows [32,33]:

$$M_s(T) = M_{s0}\left(1 - \frac{T}{T_C}\right)^{\beta_{TMR}} \tag{21}$$

where M_{S0} is the magnetization saturation at absolute zero, T_C is the Curie temperature, and β_{TMR} is a material dependent critical exponent.

The zero-voltage temperature dependent spin-polarization can be calculated as follows [34]:

$$P_s(T) = P_0\left(1 - \alpha_{SP}T^{3/2}\right) \tag{22}$$

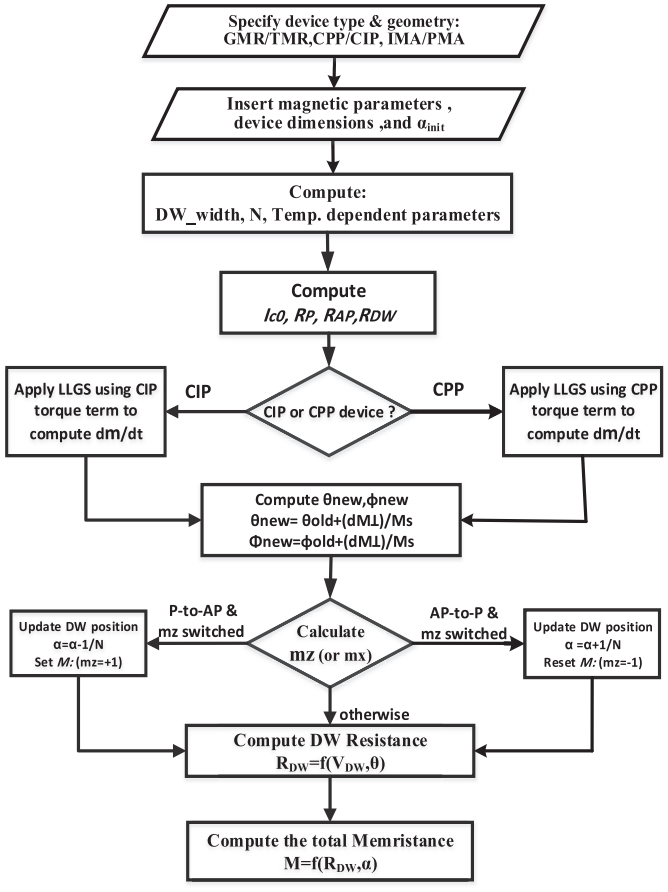

Fig. 10. Verilog-A Flow Chart of the proposed model.

where P_0 is the spin-polarization at absolute zero, and α_{SP} is a material- and geometry-dependent constant. The zero-voltage magnetoresistance $TMR_0\ (T)$ is related to the spin-polarization as follows [35]:

$$TMR_0(T) = \frac{2\,P_s^2(T)}{1 - P_s^2(T)} \tag{23}$$

The voltage-dependent TMR is then calculated as follows:

$$TMR(T,V) = \frac{TMR_0(T)}{1 + \left(\frac{V}{V_h}\right)^2} \tag{24}$$

The TMR voltage dependency is usually asymmetric for positive and negative voltages [36]. Thus, two fitting parameters V_{hp} *and* V_{hn} can be used for positive and negative voltage dependent equations. Then, the voltage-dependent spin-polarization is calculated as follows:

$$P_S(\mathrm{T,V}) = \sqrt{\frac{TMR(T,V)}{TMR(T,V)+2}} \tag{25}$$

It should be noted that Chen et al. [37] referred to the existence of the TMR voltage dependency in spintronic memristors, but it was not included in any memristor model before.

Finally, the fluctuating thermal field that is added to the effective field is given by Ref. [20]:

$$\vec{H}_{th}(T) = \vec{\eta}(t)\sqrt{\frac{2\alpha K_B T}{(1+\alpha^2)\,\gamma\,\mu\,M_S\,Vol\,dt}} \tag{26}$$

where $\vec{\eta}(t)$ is a stochastic vector with zero mean and standard normal distribution, and dt is the time step. It is important to note that $\vec{H}_{th}$ has a random behavior depending on both the temperature and the simulation time step.

3.4. In-plane magnetic anisotropy (IMA) and perpendicular magnetic anisotropy (PMA)

The IMA and PMA describe the direction of the anisotropy compared to the device geometry. In the IMA shown in Fig. 9(a), the anisotropy is parallel to the FL-PL interface. On the other hand, the anisotropy in PMA is perpendicular to the FL-PL interface as shown in Fig. 9(b).

The critical currents of IMA and PMA structures are given in Eq. (27), and Eq. (28), respectively [38]. The ratio between the critical current of

Table 1
Constant and parameters in the proposed model.

Physical constants		
e	Elementary charge (C)	1.602×10^{-19}
$\hbar$	Reduced Planck constant (erg s)	1.054×10^{-27}
Material parameters		
$\mathbf{TMR_0}$	TMR at 0 V & room temperature	2
$\mathbf{M_{s\_nom}}$	Magnetization saturation at room temperature (emu/cc)	1050
$\mathbf{H_K}$	Easy anisotropy (O_e)	250
$\mathbf{A_{ex}}$	Exchange parameter (J/m)	1.8×10^{-11}
$\boldsymbol{\alpha_g}$, $\boldsymbol{\beta}$	Two damping parameters	0.002
$\boldsymbol{\gamma}$	Gyromagnetic ratio ($s^{-1}O_e^{-1}$)	1.7608×10^{-7}
$\mathbf{V_h}$	TMR voltage dependence parameter (V)	0.5
$\mathbf{T_C}$	Curie temperature (K)	1420
$\boldsymbol{\alpha_{sp}}$	P_s thermal dependence parameter	2×10^{-5}
$\boldsymbol{\beta_{TMR}}$	M_s thermal dependence exponent	0.4
F	TMR-based R_P 1st fitting parameter ($nm^{-1}eV^{-1/2}$)	5.39×10^{-7}
Coef	TMR-based R_P 2nd fitting parameter ($nm^{-1}eV^{-1/2}$)	1.025
Model parameters		
D	Length (nm)	500
h	Thickness (nm)	1.5
z	Width (nm)	60
$\mathbf{t_{ox}}$	Oxide thickness (nm)	0.85
$\mathbf{R_{eL}}$	Low sheet resistance (Ω/□)	50

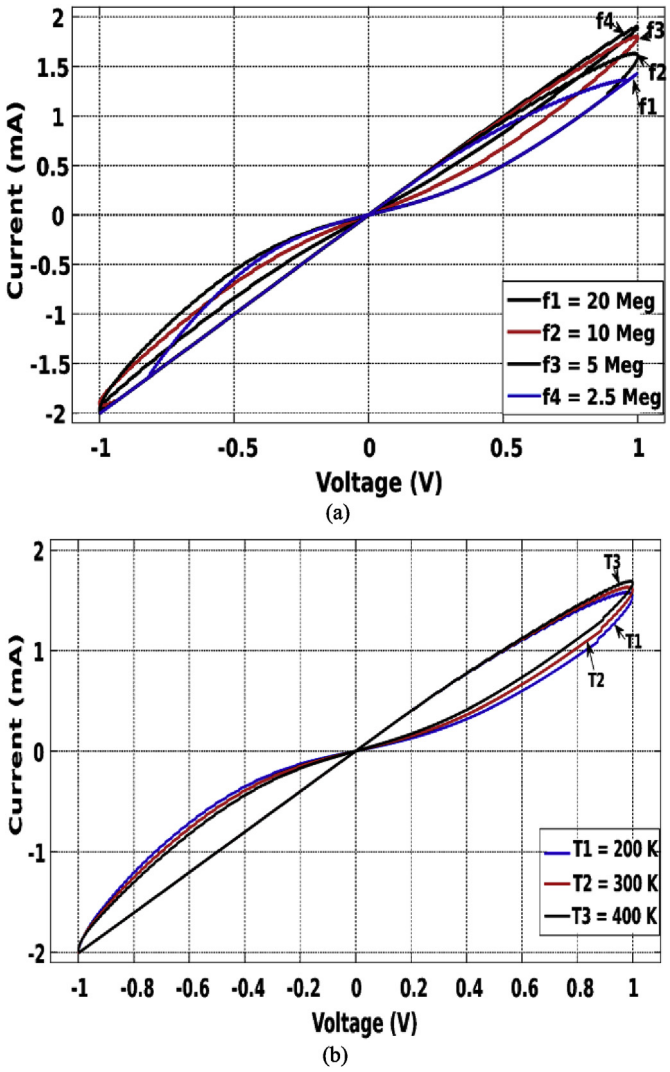

Fig. 11. The current-voltage (I-V) characteristics of a given spintronic memristor driven by sinusoidal input of 1 V using the proposed model (a) for different frequencies (b) for different temperatures.

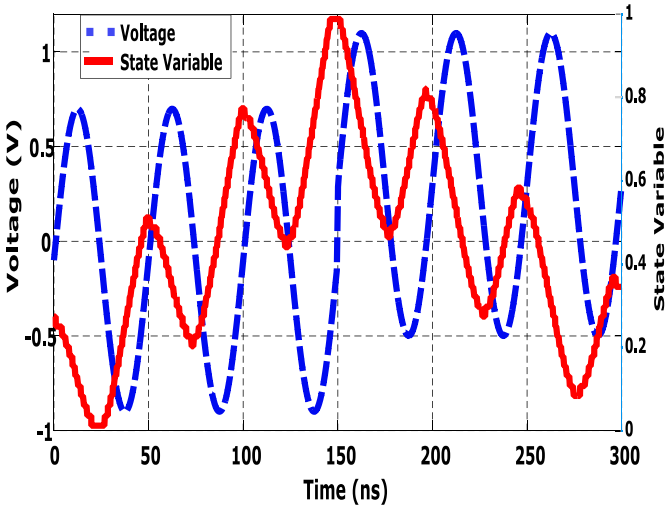

Fig. 12. State variable of a spintronic memristor driven by a biased sinusoidal voltage.

the IMA devices to the PMA devices is $(H_K + 2\pi M_S)/H_K$. Thus, PMA devices have lower critical currents than IMA counterparts. PMA materials can lead to higher density because the DW is narrower. However, PMA devices are more difficult to be fabricated and rely on more complicated stack. The proposed model includes the critical currents described in Eq. (27) and Eq. (28) based on whether the memristor type is IMA or PMA, respectively.

$$I_{C0\ (IMA)} = \frac{2e\alpha_g M_S Vol\ (H_K + 2\pi M_S)}{\hbar\eta(\theta)} \tag{27}$$

$$I_{C0\ (PMA)} = \frac{2e\alpha_g M_S Vol\ H_K}{\hbar\eta(\theta)} \tag{28}$$

where *Vol* is the FL volume, and $\eta(\theta)$ is the polarization efficiency and it is given by Ref. [39]:

$$\eta(\theta) = \frac{P_S}{1 + P_s^2 \cos(\theta)} \tag{29}$$

Eqs. (27) and (28) show that the critical current of the spintronic memristor depends on $\eta\ (\theta)$ which is a function of the angle θ between the magnetization vectors of the FL and PL. Thus, the critical current of the spintronic memristor in the case of P-AP switching differs from the critical current in case of AP-P switching. In case of the P-AP switching, $\theta = 0^\circ$ and the polarization efficiency equals $\eta_{P\text{-}AP} = \eta\ (0^\circ) = P_S/(1 + P_S^2)$. Similarly, the AP-P switching has a polarization efficiency of $\eta_{AP\text{-}P} = \eta\ (180^\circ) = P_S/(1\text{-}P_S^2)$. Thus, the switching from AP to P states is easier than switching from P to AP states. This is physically understandable, as the FL magnetization vector tends to align with the easy axis. The ratio between the critical currents of P-AP and AP-P switching is:

$$\frac{I_{C0P-AP}}{I_{C0AP-P}} = \frac{1 - P_s^2}{1 + P_s^2} \tag{30}$$

3.5. The GMR- and TMR-based spintronic memristors

The proposed model uses the following equation to calculate the parallel resistance of the TMR-based devices [40]:

$$R_P = \frac{t_{ox}}{(F\ \varphi^{1/2} \cdot Area)}\ e^{(Coef \cdot t_{ox} \cdot \varphi^{1/2})} \tag{31}$$

where φ is the average potential barrier height of the oxide material, *coef* is a fitting parameter, and *F* is a fitting parameter corresponding to t_{ox} and depends on the material composition of the spintronic memristor layers.

The DW resistance as a function of θ is then calculated from the Julliere model [41] as follows:

$$R_{DW}(\theta) = \frac{2\ R_{P\_DW}\ \|\ R_{AP\_DW}}{1 + P_S^2 \cos(\theta)} \tag{32}$$

where R_{P_DW} is calculated from Eq. (16) for CIP devices and from Eq. (20) for CPP devices in both GMR- and TMR-based memristors. R_{AP_DW} is calculated from Eq. (14) as a function of R_{P_DW} and *TMR (T, V)*.

In the case of the GMR-based spintronic memristor, the parallel resistance of the device is calculated from the sheet resistance R_{eL} as in Chen et al. model [25]:

$$R_P = R_{eL}\ (D/z) \tag{33}$$

where *D, z* are the device's length and width respectively as in the CIP-based spintronic memristor shown in Fig. 3.

The DW resistance of the CIP-based memristors is then calculated from the following equation [42]:

$$R_{DW}(\theta) = R_{P\_DW} + (R_{AP\_DW} - R_{P\_DW})\left(\frac{1 - \cos(\theta)}{2}\right) \tag{34}$$

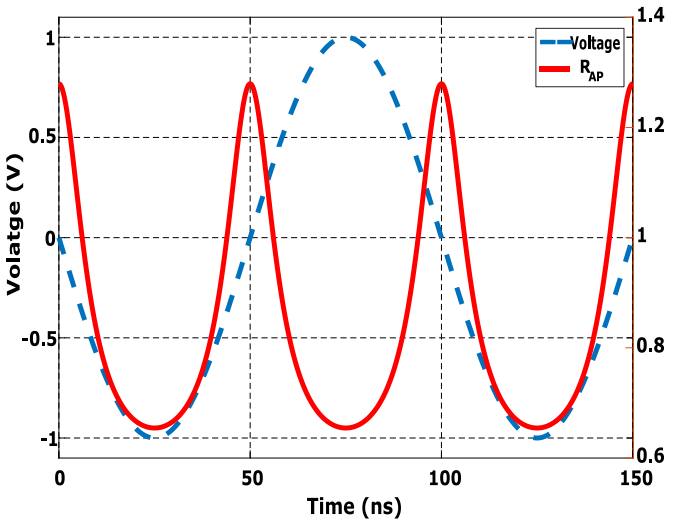

Fig. 13. Antiparallel resistance for sin wave input ($TMR_0 = 2$).

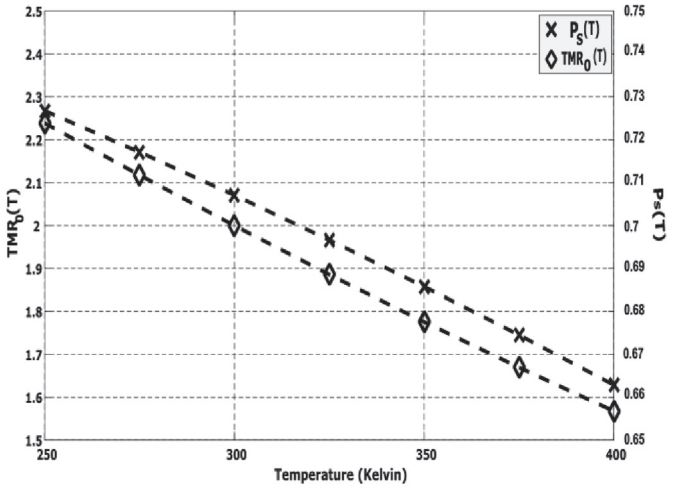

Fig. 14. Effect of temperature on zero-bias *TMR* and P_S.

3.6. Verilog-A Description

Fig. 10 shows the flowchart of the proposed model. According to this flowchart, the designer should first specify the memristor type whether it is GMR/TMR, CIP/CPP, and IMA/PMA. Then the physical parameters, magnetic device constants, and device dimensions are provided by the designer. After that, the Verilog-A routine computes temperature dependent parameters, DW width, and the number of DW positions *N*. According to the device type, the values of R_P, R_{AP}, I_{C0}, and initial R_{DW} are computed. The LLGS equation is applied to the DW and the rate of change of the normalized magnetization vector dm/dt and the angle θ are calculated.

Then the value of the magnetization vector is updated. If the magnetization-vector switched from P to AP or AP to P states, the position of the DW is updated. Finally, the DW resistance R_{DW} (θ), and the total memristance M (α) are calculated.

4. Simulation results

The model is implemented using Verilog-A language and used with a SPECTRE-based CAD tool to study the behavior of the spintronic memristor for different stimulations and to show the main characteristics of the device. Table 1 provides the values of the dimensions and the main parameters used in the simulations [43,44].

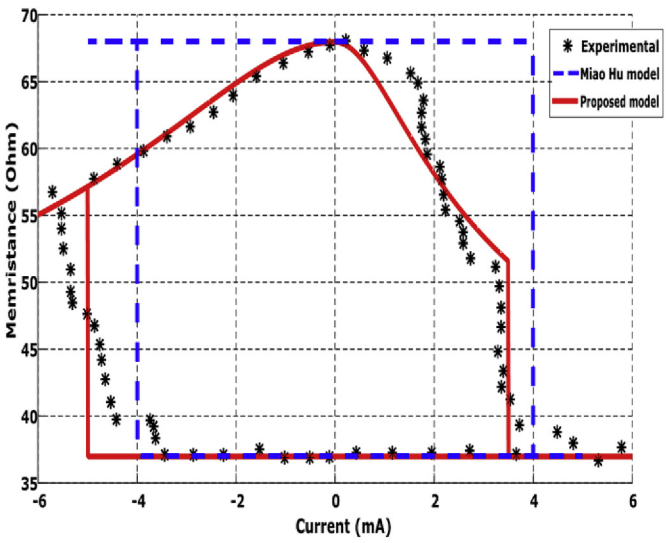

Fig. 15. Resistance as a function of current for the experimental data, Miao Hu model, and the proposed model.

4.1. Model properties

The TMR-based PMA spintronic memristor is chosen through our simulations because it might be the most promising type of spintronic memristors.

Fig. 11(a) shows the current-voltage (I-V) characteristics of the spintronic memristor using a *1 V* sinusoidal input voltage. The I-V characteristics are studied under different input frequencies *2.5, 5, 10, and* 20 MHz. The hysteresis curve reduces when the signal frequency

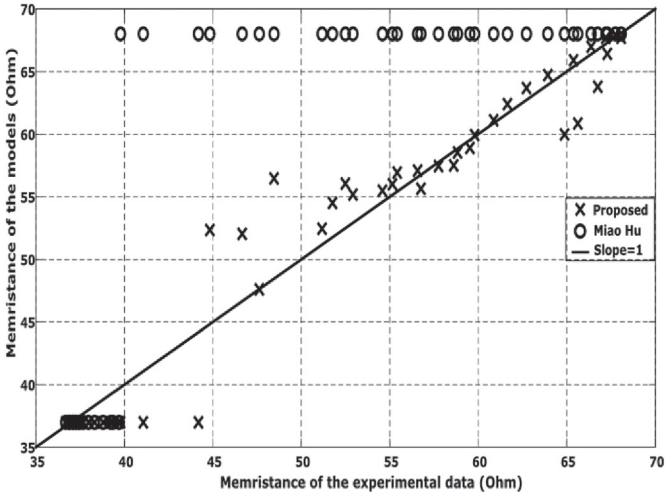

Fig. 16. Memristance of the experimental data versus Miao Hu model and the proposed model.

Table 2
Percentage error fitting comparison.

	Miao Hu model [4]	Proposed model
Root-mean-square %error	22.98%	5.32%
Maximum %error	71%	16.7%

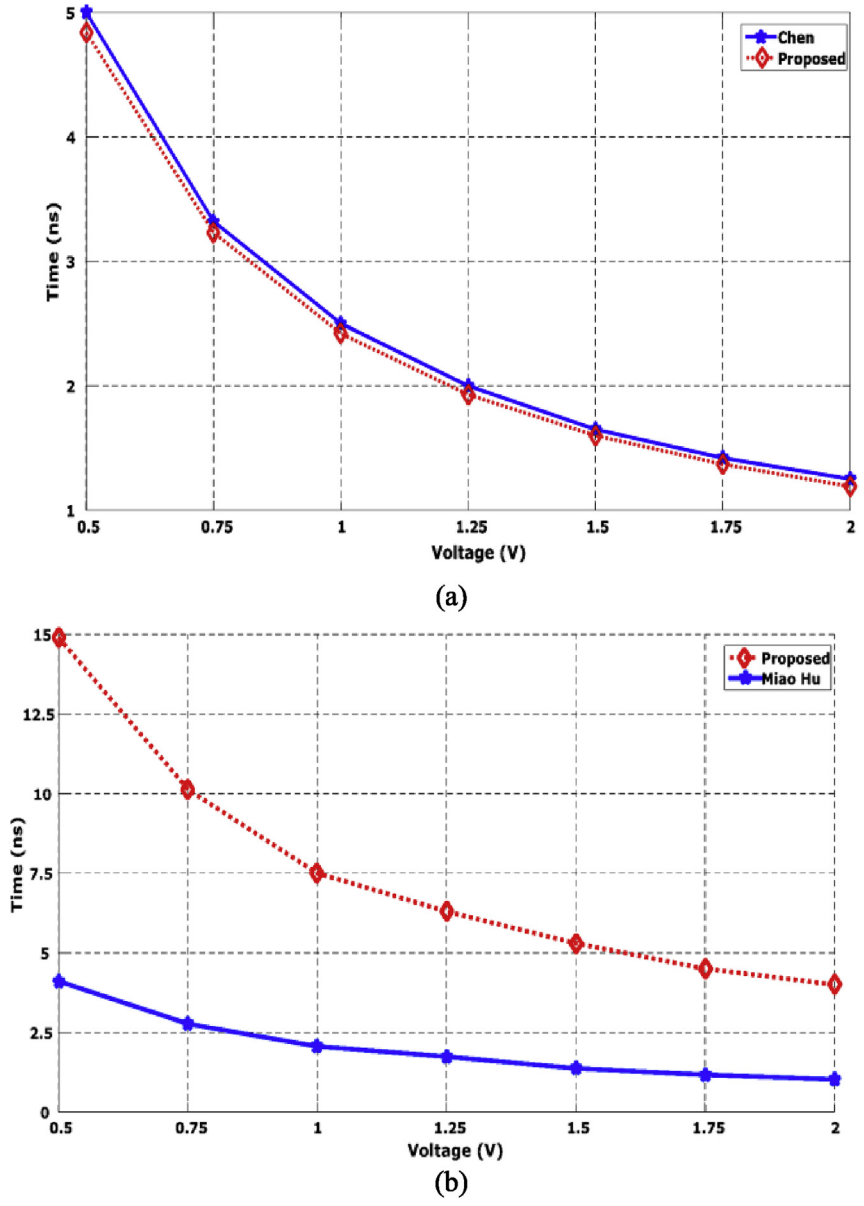

Fig. 17. Switching delay versus applied voltage for (a) CIP structure Chen et al. model [25] and the proposed model (b) CPP structure Miao Hu et al. model [4] and the proposed model.

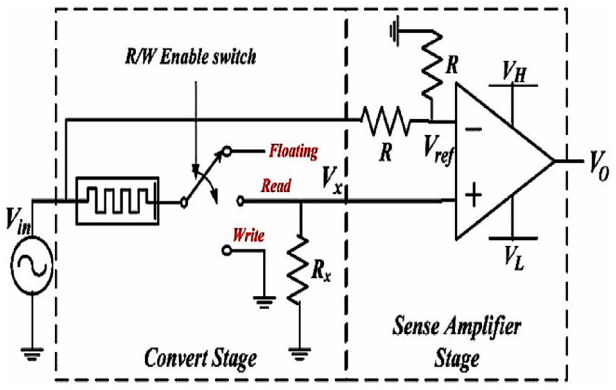

Fig. 18. Yenpo R/W circuit [9].

increases as expected for any memristor device. Fig. 11(b) shows the I-V characteristics of the spintronic memristor when applying a sinusoidal input of *1 V* under different temperature values, *200°, 300°, and 400° K*.

The figure shows that the hysteresis curve reduces when the temperature increases. Thus, we can conclude that increasing temperature reduces the unique hysteresis feature of the memristor, making it slightly closer to the resistor-like behavior.

In Fig. 12, a biased sinusoidal voltage excitation is applied to the spintronic memristor with a frequency of $f = 20$ MHz and amplitude of $V_m = 0.8V$. A negative bias of *-0.1V* is added to the first three cycles and then a positive bias of $+0.3V$ is added for the next three cycles. In the first three cycles, the negative bias combined with the sinusoidal voltage causes the gradually increasing of the state variable α. Another reason for the increasing ripples is that the switching from P to AP is slower than the AP to P switching due to the inherent tendency of the magnetization vector to be aligned with the easy axis as mentioned.

The value of the antiparallel resistance and thus the total memristance are functions of the applied voltage. The proposed model includes the TMR/GMR voltage dependence effect. Fig. 13 shows the value of the antiparallel resistance for a sinusoidal applied voltage. As shown in this figure, the antiparallel resistance reaches its maximum value when the input voltage equals zero. Under zero applied voltage, the tunneling magnetoresistance $TMR\ (V=0) = TMR_0$ and the R_{AP} value is maximum.

When the applied voltage reaches its positive or negative peak $\pm 1V$, the tunneling magnetoresistance and the antiparallel resistance reach their lowest value: $TMR\ (V=\pm 1) = 0.2\ TMR_0$, and thus R_{AP} value is minimum. Thus, reducing the operating voltage in spintronic memristor is preferable in the design, as it increases the magnetoresistance and thus increases the noise margin of the memristor when it is used in memory applications.

Fig. 14 shows the temperature effect on the zero-bias *TMR* and P_S. The spin polarization P_S decreases with temperature as expected from (22). From (23), the *TMR* and consequently R_{AP} also decrease with temperature. The $TMR_0(400^oK) = 1.567$ which is *22%* lower than the *TMR* at room temperature. $P_S(400^oK)$ is *6.3%* lower than the P_S at room temperature. Combining both the voltage and temperature effects on TMR may lead to a significant reduction in its value, which is an important design factor that should be considered during the design of any spintronic memristor-based circuit.

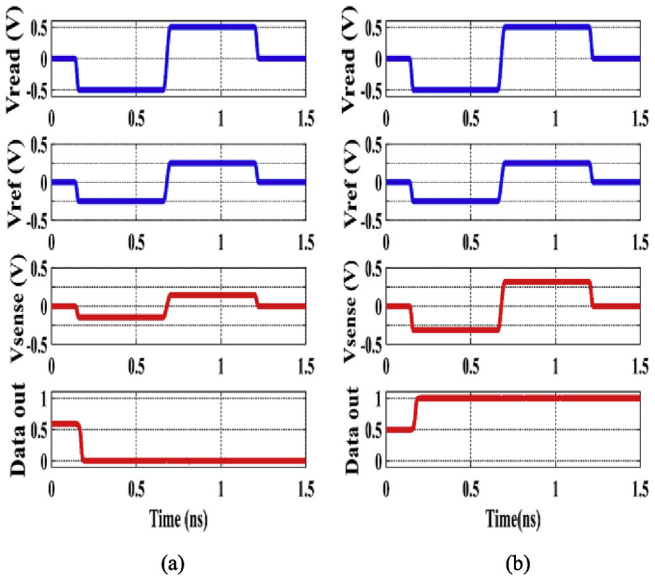

Fig. 19. Write operation (a) Logic '0'((b) Logic '1'.

4.2. Model verification

4.2.1. Fitting to an experimental data

In 2016, a paper published by Steven Lequeux et al. [36] provided the first realization of a spintronic memristor. This is the first experimental achievement of a spintronic memristor up to the author knowledge. Fig. 15 shows a comparison between Miao Hu model and the proposed model fitting to the current-memristance relationship. The reason of choosing Miao Hu model for the comparison is that this spintronic memristor is a CPP spintronic memristors which is compatible with Miao

Table 3
Comparison between previous Models and the Proposed Model.

Model	Chen Model [25]	Miao Hu Model [4]	Proposed Model
LLGS-based	partially	partially	Yes
Valid for different geometries	No	No	Yes
Material and geometry parameters' dependence	partially	partially	Yes
Thermal dependence	No	No	Yes
TMR/GMR voltage dependence	No	No	Yes
Simulation time	Shorter	Shorter	Longer

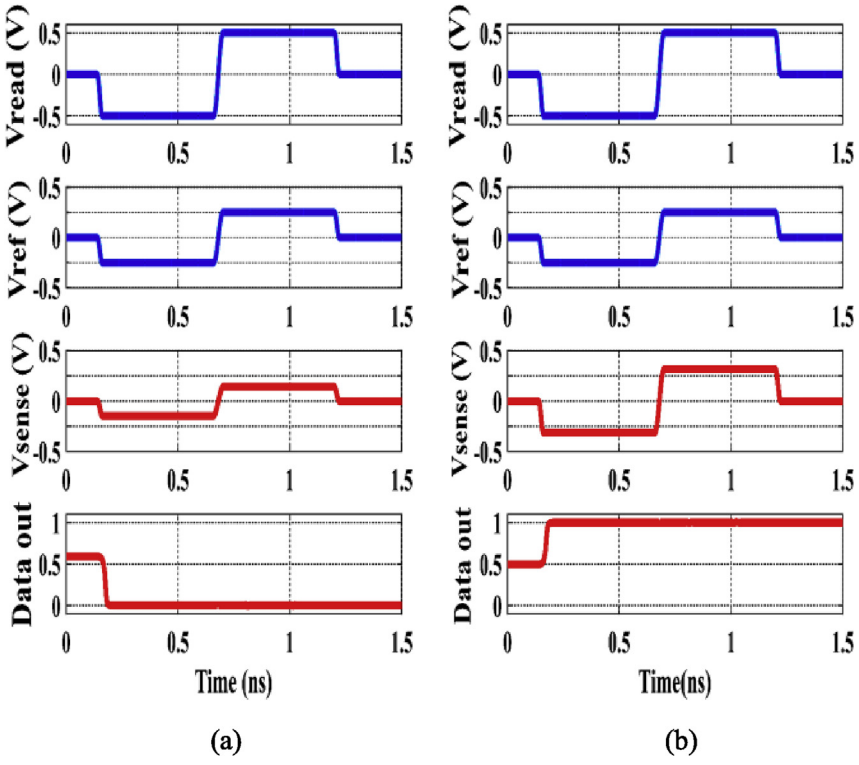

Fig. 20. Read operation one cycle (a) Logic '0' (b) Logic '1'.

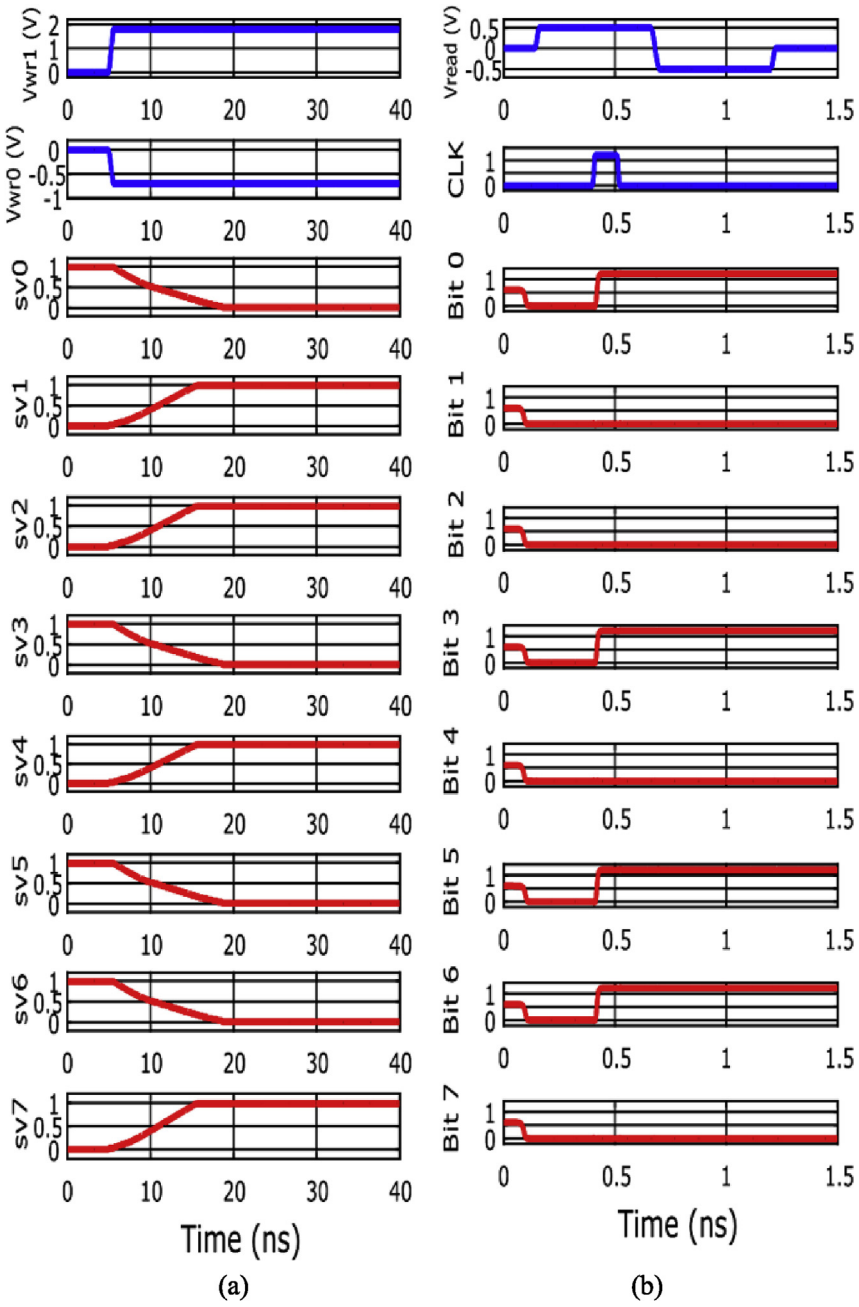

Fig. 21. Read/Write operation of one word from a 1 Kb 1T1M memory circuit (a) Writing the word (10010110), (b) Reading the word (01101001).

Hu model. The proposed model shows better fitting to the experimental data. The first reason behind this is the clear voltage dependency of the TMR and thus the antiparallel resistance. The second reason is the ability of using two different critical currents for the positive and negative voltages in the proposed model. The values that are used in this fitting are $R_P = 37\,\Omega$, $TMR_0 = 0.84$, $V_h = 0.22\,V$, $J_{cr(P\text{-}AP)} = 4.9 \times 10^6\ A/m^2$, and $J_{cr(AP\text{-}P)} = 3.4 \times 10^6\ A/m^2$. The device dimensions are ($1000 \times 100 \times 2.2\,nm^3$), which fit the provided experimental data.

Fig. 16 shows memristance values of experimental data that derived from Fig. 15 versus the memristance values that derived from simulation using both Miao Hu and the proposed models under the same current values stimulations used with the experimental data that shown in Fig. 15. The comparison used the outer *R-I* curve at which the applied dc current pulse has a density larger than J_{cr} for enough duration to make the memristor switches from R_P to R_{AP} or from R_P to R_{AP} states. Thus, Miao Hu model in this case reaches the minimum and maximum values R_P and R_{AP} which are fixed for his model. On the other hand, the proposed model gives a better fitting to the experimental data under the same stimulation. It should be noted that the internal states of the experimental data which represents the memristance levels between R_P and R_{AP} is not provided in this comparison as the experimental data for them was not clear enough and to make the comparison more readable.

Table 2 provides a comparison of the percentage error of the Miao Hu and the proposed models. The root mean square error of the proposed model is only 5.32% compared to 22.98% for Miao Hu model. Also, due to the high voltage dependence of the R_{AP}, the maximum percentage

error of Miao Hu model reaches 71% compared to 16.7% for the proposed model.

4.2.2. Dynamical behavior of the proposed model

Due to the absence of a transient analysis of an experimental spintronic memristor, the proposed model is compared to the Chen et al. model [25] and Miao Hu et al. model [4].Fig. 17(a) shows the switching delay versus the applied voltage of a spintronic memristor using both Chen et al. model [25] and the proposed model for the CIP structure. The used parameters are $R_P = 1.25\,K\Omega$, $TMR_0 = 2$, $M_s = 1010$, $H_K = 100$, $DW\ width = 10\,nm$, and device dimensions of $100 \times 20 \times 10\,nm$. The simulation results show that switching delay of the proposed model is very close to the Chen model (3% lower) which is logical because the DW velocity of the Chen model is derived from the LLGS equation with the CIP STT term like the proposed model for CIP structures. This result shows the validity of the proposed model dynamical equations.

Fig. 17(b) shows the switching delay versus the applied voltage of a spintronic memristor using both Miao Hu et al. model [4] and the proposed model for the CPP structure. The proposed model shows that the expected delay should be about 3.5 times of the delay of Miao model. The reason of this result is that Miao Hu model used the approximation of the CIP torque term instead of the CPP term. The torque of the CPP structure strongly depends on θ which reduces the DW speed noticeably.

4.3. Case study: memristor-based memory cell

The memristor-based memories might be the most promising application for spintronic memristors. The memory read/write operations are discussed here as a case study of the proposed model. The read/write circuit used here is provided in Ref. [9], and it is shown in Fig. 18. The write operation is simply achieved by applying a positive pulse of 1 V to write logic '0', or a pulse of -1 V to write logic '1'. Fig. 19 shows the simulation results of the write operation.

The simulation results of the read operation for one cycle are shown in Fig. 20. The theory of the circuit depends on applying a read voltage signal of equivalent positive and negative pulses to cancel the effect of each other. The output data is sensed during the positive reading pulse and latched at the output until the next cycle.

Another case study is the 1024-bit memory circuit using the 1T1M crossbar array. The circuit is assumed to be consisted of 128-word x 8-bits for each word. Fig. 21(a) shows the write process of the word (10010110), where sv7 is the state variable of the memristor that represents the most significant bit. Fig. 21(b) shows the read process of the word (01101001). The output of the read process is valid after the CLK rising edge. This circuit is used to validate the model ability to be used in large circuits without any convergence problems.

4.4. Comparison between the models

Table 3 provides a comparison between previous models and the proposed model. Unlike previous models, which partially depend on a modified LLG equation, the proposed uses the LLGS equation to model the dynamical behavior of the spintronic memristor. The proposed device uses physical equations to model different types of spintronic memristors as a function of its physical parameters. For example, the proposed voltage and thermal dependent parameters can be used efficiently to investigate the effect of voltage and thermal fluctuations on the spintronic memristors dynamic behavior. However, the proposed model needs a longer simulation time, as it requires smaller time step to keep up with the fast changes in the magnetization vector when it is modeled by the LLGS equation.

5. Conclusion

In this paper, an accurate model of the domain-wall spintronic memristor is proposed. Previous models utilized a simplified form of the CIP torque term to represent the dynamic behavior of the spintronic memristor. The proposed model uses the accurate LLGS equation. For CIP structures, the proposed model showed a very close dynamic behavior to the Chen model (3% lower) because the DW velocity of Chen model is derived from the proper LLGS CIP torque term. However, for the CPP structures, Miao Hu model uses the same CIP torque term instead of the CPP torque term that should be used in this case. The proposed model showed that the expected switching delay should be about 3.5 times of that of Miao Hu model.

The proposed model uses the required equations to model different types of spintronic memristors like GMR/TMR, CPP/CIP, and PMA/IMA as a function of their physical parameters. Also, the proposed model is the first model that includes the TMR/GMR voltage dependence in spintronic memristor modeling. The model includes thermal dependent parameters to model the effect of thermal fluctuations on the device's behavior. Both voltage-dependent and thermal-dependent effects are of a great importance in studying the actual behavior of spintronic memristors in circuit design. Also, the fluctuating thermal field is added to the effective field to model the fluctuating thermal effects and the stochastic behavior of the spintronic memristors. The model is verified to an experimental data of a spintronic memristor, and it showed much better fitting compared to existing models. Two case studies of a memristor-based read/write memory circuit and a 1024 bit 1T1M memory circuit are used to verify the model. The model is written using Verilog-A, and it is integrated with SPECTRE-based CAD tool.

In brief, this work makes important contributions to the accurate characterization and modeling of domain-wall spintronic memristors, analyzing, and designing its based memory circuits by addressing the problems of the existing models which utilize a simplified form of the CIP STT term from the modified LLG equation.

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