

Design of Microscale Piezoelectric Energy Harvesting System

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Abstract—This paper presents a design of microscale piezoelectric energy harvesting system, AC/DC converter is used to convert the AC power generated from piezoelectric to DC power, then DC/DC is used to convert the DC voltage to suitable voltage, Analog to digital converter is used to convert the analog signal produced from AC/DC to 8 bits digital signal then feeds to digital control oscillator that produced the clock for DC/DC and hence guarantees maximum point power tracking of all system based on the input signal.

Index Terms—Energy harvesting, AC/DC, DC/DC, ADC SAR DCO, and MPPT.

I. INTRODUCTION

Energy harvesting system aims to eliminate the need to replace batteries, by converting ambient energy mechanical, optical, thermal and RF into electrical energy and charging a battery. Ambient energy of thermoelectric generators (TEG), silicon-based micro-fuel and single junction photovoltaic (PV) cells produce a dc power [1] without the need of AC/DC converter. Ambient energy of piezoelectric, electromagnet and RF produce ac power, AC/DC converter must be employed to convert the ac power harvested from piezoelectric to dc power, DC/DC converter is used to convert DC power to suitable DC power for storing at supercapacitor, the clock frequency needed for DC/DC will be generated by digitalize the analog signal from AC/DC to 8 bits digital signal using analog to digital converter, 8 bits will feed to the digital control oscillator that produced the clock for DC/DC and hence guarantee maximum point power tracking based on the input signal. The energy harvesting system block diagram is shown in Figure 1.

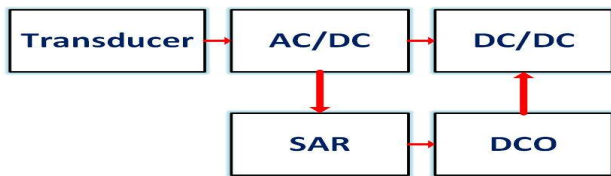


Fig. 1. System block diagram

This paper is organized as follows. In Section II, the AC/DC and DC/DC are introduced. In Section III, Successive approximately register SAR and digital control oscillator DCO

are presented. Simulation results are given in Section IV, followed by conclusions in Section V.

II. AC/DC CONVERTER AND DC/DC CONVERTER

The AC/DC converter is used to convert AC power harvested using piezoelectric to DC power as shown in Figure 2, AC source V_{in} is used instead of using transducer for easy understanding. AC/DC converter consists of two stages, At the first stage during the negative cycle of the AC input signal, the capacitor C_1 is charging by the AC peak voltage $V_{C1}=2V_{in}-V_{th(M1)}$, as the transistor M_1 acts as a diode clamp conducts, During the positive cycle of the AC input signal, the capacitor C_1 discharge very little as the transistor M_1 is OFF, the AC peak voltage will be $2V_{in}-V_{th(M1)}$ at terminal A. When the voltage of point (B) is smaller than the voltage of point (A), the transistor M_2 ON that allow charging of the capacitor C_3 to DC voltage $V_{C3}=2V_{in}-V_{th(M1)}-V_{th(M2)}$. When the voltage of point (A) is smaller than the voltage of point (B), the transistor M_2 OFF disconnected the path of conduction. At point (C) the capacitor C_2 voltage is shifted by a DC value $(2V_{in}-V_{th(M1)}-V_{th(M2)}-V_{th(M3)})$ plus the AC peak voltage $2V_{in}-V_{th(M1)}$ from the second path. At the second stage if the voltage of point (D) is smaller than the voltage of point (C), the switch M_4 ON allowing a capacitor C_4 charging by a DC value $4V_{in}-2V_{th(M1)}-V_{th(M2)}-V_{th(M3)}-V_{th(M4)}$. When the voltage of point (C) is smaller than the voltage of point (D), the switch M_4 OFF, and discharge a capacitor C_4 by R_L . An ACTIVE diode is used to control the current direction and to work nearly as an ideal diode. The active diode is a comparator-controlled PMOS switch.

The active diode schematic is shown in figure 3. Transistors M_4 - M_9 work as a comparator to control the gate voltage of PMOS switch M_1 . Transistors M_{10} - M_{12} are two current mirrors to supply a current needed to power on the comparator. M_1 should turn on and turn off completely to reduce the voltage drop. Transistors M_2 - M_3 work as a dynamic bulk regulator, connecting the substrate of transistors M_1 , M_4 , and M_6 to the highest potentials which prevent the chance of latch-up. In addition, the body effect on M_1 is reduced and therefore, the voltage drop and power dissipation will be reducing.

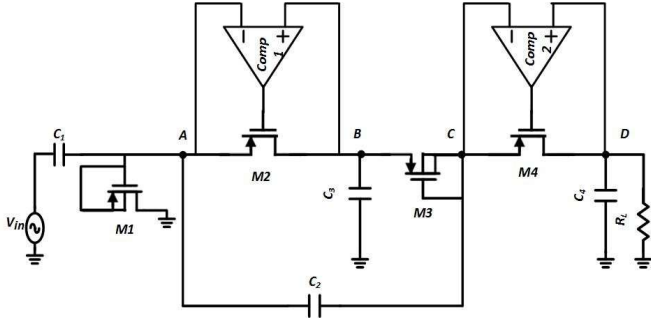


Fig. 2. The proposed AC/DC converter

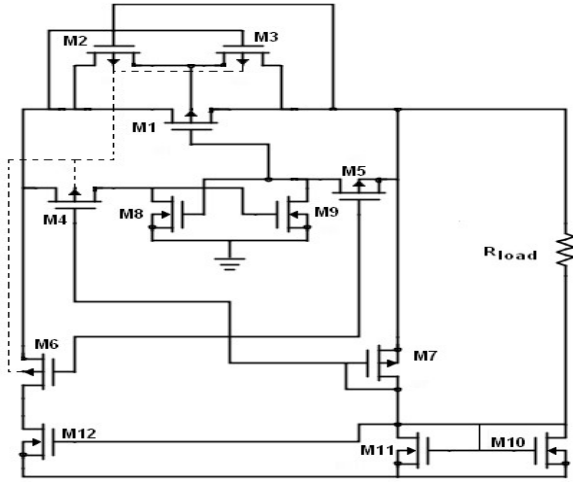


Fig. 3. The proposed active diode

The DC/DC converter tree topology used to provide the electronics circuit with DC power needed through the output capacitor without the need of replacing the battery as shown in Figure 4. The operation of this topology working as a following the output voltage of the AC/DC converter will charge the capacitor C_1 at Q_B is high, the charge is transferred from C_1 to C_3 when another phase Q is high the same script occurs at the capacitor C_3 If $(V_x > V_{out})$, and if it $(V_x < V_{out})$ will be transferred.

The output current for DC/DC can be modeled as:

$$I_{out} = f_{clk} Q_{avg} = \frac{1}{3} f_{clk} C (4V_{in} - V_{out}) \quad (1)$$

Where, f_{clk} is the switching frequency, C is the flying capacitor used in each stage, the output voltage of AC/DC converter V_{in} and the converter output voltage is V_{out} . The DC/DC input impedance will be a very important key to get the maximum point power tracking MPPT of the designed circuit. The DC/DC input impedance will be as:

$$R_{in} = \frac{1}{f_{clk} \left[\left(4 - \frac{V_{out}}{V_{in}} \right) \frac{4C}{3} + \frac{\beta}{V_{in}} \right]} \quad (2)$$

Where f_{clk} is the switching frequency, C is the flying capacitor used in each stage, the output voltage of the AC/DC converter V_{in} , the converter output voltage is V_{out} and β is the power converter losses. As shown in 1.2 the input impedance is inverse proportional to the switching frequency of DC/DC, by setting switching frequency =0 Hz, we will get high input impedance of DC/DC converter and by increasing switching frequency the input impedance will be decreased.

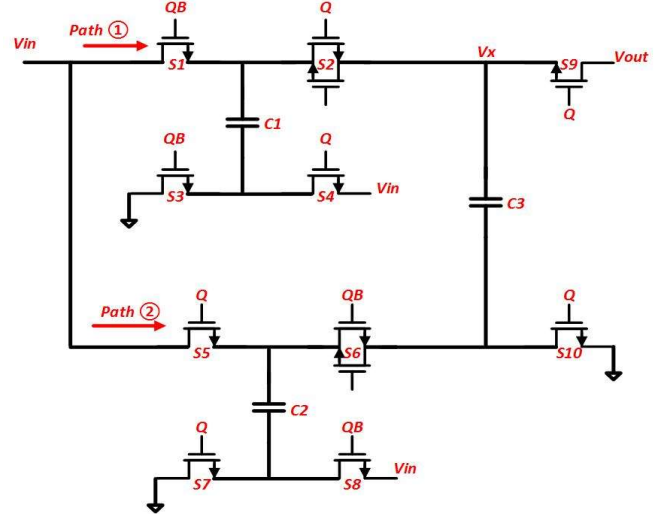


Fig. 4. The DC/DC converter

III. SAR AND DCO

This section is presenting a detailed explanation for the maximum point power tracking for piezoelectric energy harvesting systems. The idea of this technique depended on studying the piezoelectric characteristics. This study is based on connecting the piezoelectric to AC/DC converter then to the DC/DC, and getting a relationship between the frequency of DC/DC and the voltage of piezoelectric transducer and finding the maximum power of the piezoelectric. The target of the MPPT circuit is getting the frequency of the switching desired for DC/DC charge pump to find the MPPT relationship.

The MPPT circuit is consists of a successive approximation register (SAR) 8-bit converter that converts the analog voltage of AC/DC to digital bits which will control a digital control oscillator (DCO) to generate the switching frequency needed to DC/DC topology to get the MPPT of our transducer.

The analog to digital converters Successive Approximation Register (SAR) used based on its low power and area in comparison with many different analog to digital converters ADC [2] as shown in Figure 5. Sample and hold samples the analog output signal of the AC/DC converter and holds it until the conversion period finishing. The comparator compares the output of the digital to analog circuit with the output of the sample and hold and its output will be fed to the successive approximation register, By the end of conversion, we will have a digital output of the analog AC/DC signal. By using the charge redistribution circuit we implement the sample and hold circuit and DAC as shown in Figure 6. SAR is implemented using the VerilogA code.

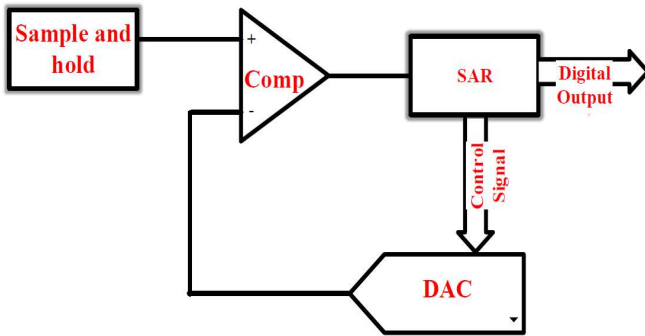


Fig. 5. SAR

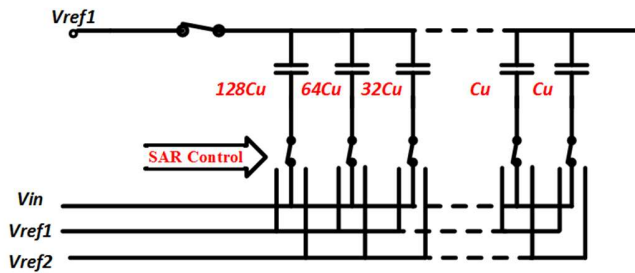


Fig. 6. Implementation of charge redistribution circuit

The digital output of the SAR ADC converter is then fed to DCO that is responsible to generate the desired clock for DC/DC converter to get the MPPT for our transducer. The DCO is implemented using the VerilogA coding.

IV. SIMULATION

By using Cadence Spectre the voltage multiplier AC/DC converter is simulated using 130nm CMOS technology UMC provider. Figure 7 shows the transient behavior of AC/DC

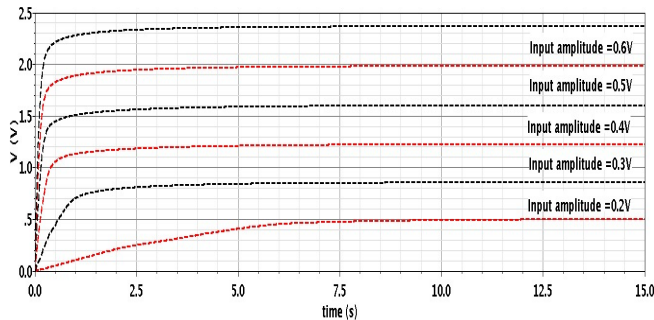


Fig. 7. The voltage multiplier proposed AC/DC transient behavior

The different input voltage amplitude versus voltage efficiency with 100kΩ load and without load is shown at Figure 8, the efficiency for input voltage 0.6 V will be larger than 300% without load and for input 0.7V the voltage efficiency will be 270% with 100kΩ load.

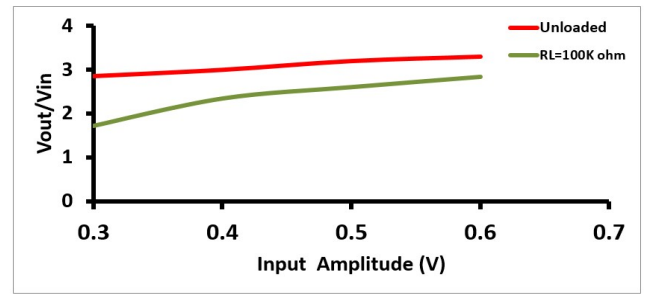


Fig. 8. Voltage efficiency versus input voltage amplitude unloaded and with ohmic load 100KΩ.

Figure 9 shows that by adjusting the size of the transistor of active diode there will be no delay time so the power efficiency enhancement.

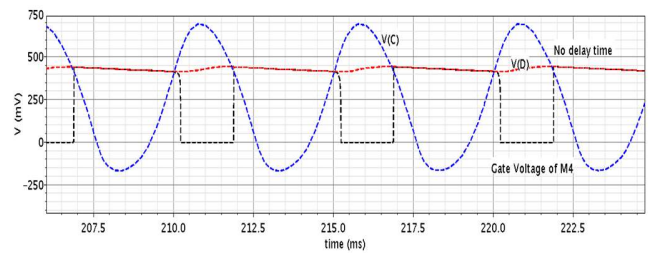


Fig. 9. show no delay time of active diode

Figure 10 shows the AC/DC converter maximum power versus output voltage of the AC/DC converter.

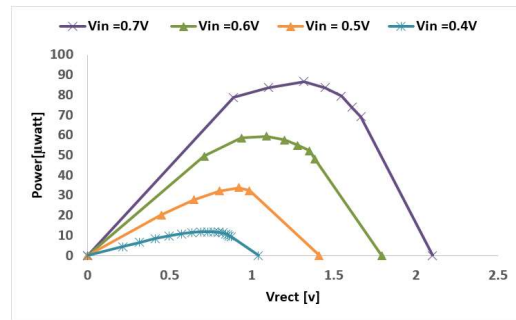


Fig. 10. The Vrect versus the maximum power

Table I presents a comparison between the proposed AC/DC converter with the latest papers. The minimum input voltage will be 0.2 and 83% is the maximum power efficiency of the proposed circuit. The voltage efficiency will be 270% with 100KΩ load and its ripples lower than 5% compared to the other AC/DC converters.

Figure 11 shows the relation between the output voltage of the AC/DC converter and the switching frequency of the DC/DC converter for different input values. It can be shown that at $f = 0$ Hz, the AC/DC voltage is equal to open circuit voltage. When the clock frequency of DC/DC increases, the input impedance starts to decrease, the output of AC/DC starts to decrease as well. It can be concluded that there is a point on each curve that corresponds to the maximum power out.

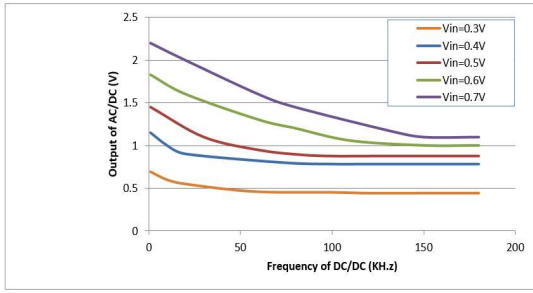


Fig. 11. The relation between output voltage of AC/DC converter and the frequency of DC/DC charge pump

Table I shows the different input signal samples, the corresponding F_{clk} that will get the MPPT of the input signal and V_{oc} when $F_{clk}=0\text{Hz}$.

TABLE I
PERFORMANCE COMPARISON

| Reference | TPEL 2011 [3] | ICEAC 2012 [4] | Transducers 2013 [5] | CSENS 2014 [6] | This work |
|----------------------|---------------|----------------|----------------------|----------------|-----------|
| V_{in} | 0.1-1.2 | 0.1V-1V | 0.1V-0.8V | 0.15V-1V | 0.2V-0.7V |
| V_{out} | N/A | 0.2V-1.7V | 0.2V-1.4V | 0.2V-2V | 0.5-2.2 V |
| Ripples | 10% | N/A | N/A | N/A | <5% |
| Frequency | 1Hz-500Hz | 1Hz-10kHz | 10H.z | 8H.z | 20Hz-1KHz |
| Max power efficiency | >80% | 92% | 67% | 86% | 83% |

TABLE II
THE DIFFERENT INPUT SAMPLES AND THE FREQUENCY TO GET MPPT

| V_{in} (V) | 0.3 | 0.4 | 0.5 | 0.6 | 0.7 |
|-----------------|-------|-------|-------|--------|------|
| V_{MPP} (V) | 0.46 | 0.796 | 0.895 | 1.0557 | 1.17 |
| F_{clk} (KHz) | 57 | 74 | 83 | 110 | 132 |
| V_{oc} (V) | 0.696 | 1.115 | 1.446 | 1.825 | 2.21 |

Figure 12 shows that the analog input voltage 0.6V will be digitalized using SAR by the end of conversion the output will be 11011010. Figure 13 shows that the simulation of digital control oscillator DCO when the input signal is (11011010), the clock frequency is 109.703 KHz.

Table III shows the performance metrics of two designs. It can be illustrated that the proposed approach achieves promising results

TABLE III
PERFORMANCE METRICS OF THE PROPOSED DESIGN

| Design Metric | [8-9] | Proposed Design |
|--------------------------|--------------------|------------------------|
| Transducer | Solar | Piezo |
| Control Frequency | 1.06MHz:6.11MHz | 57KHz:132KHz |
| Input voltage range | 613mV:714mV | 300mV:700mV |
| Maximum Input power | 276 μ W:3.13mW | 12 μ W:108 μ W |
| Maximum Power Efficiency | 58% | 70% |
| Energy Buffer Voltage | 1.8V | 1.8V |
| Size | N/A | 0.249mm ² |

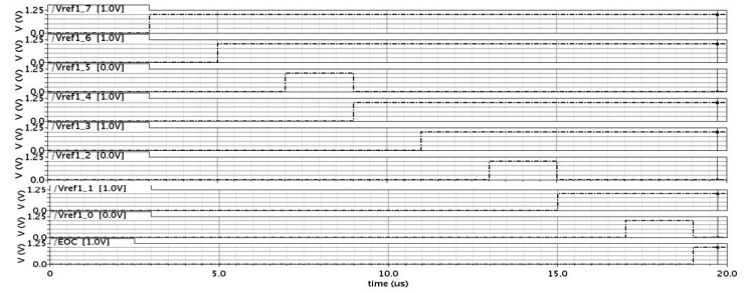


Fig. 12. The digital output 11011010 for 0.6 analog input

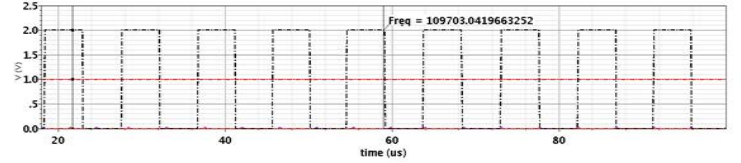


Fig. 13. The output frequency 109.7 KHz for 11011010 digital input

V. CONCLUSION

The proposed Energy harvesting system using Piezoelectric has input ac voltages in the range of 0.2-0.7 V, then DC/DC converter with energy buffer voltage 1.8 and frequency of DC/DC will be generated by using DCO then generated clock based on the digital input using SAR and the total size circuit is 0.249mm²

VI. ACKNOWLEDGEMENT

This work was partially funded by ONE Lab at Zewail City of Science and Technology and Cairo University, NTRA, ITIDA, ASRT, Mentor Graphics ,NSERC.

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