Design Optimization Methodology for High-Efficiency RF-to-DC Converters

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***Abstract*—This paper proposes a new optimization methodology for RF-to-DC converters. The proposed methodology optimizes the power conversion efficiency (PCE) at low RF input power. In addition, it improves the sensitivity and extends the dynamic range. An LC-circuit is embedded with any RF-to-DC converter circuit architecture. Since it reduces the matching constraints at different frequency bands and boosts up the low RF input power. The proposed methodology is applied to four different circuit topologies where the performance results are improved significantly compared to the original architectures. All designs are simulated and verified at dual frequency bands (1.9GHz and 2.4 GHz) with fixed load impedance $50K\Omega$. Finally, a prototype is implemented using two different CMOS technology nodes (130nm and 65nm) to emphasize the technology process effect on the circuit performance.**

***Index Terms*—energy harvesting, wireless powering, RF-to-DC converter, CMOS rectifier, voltage multiplier, low RF power.**

I. Introduction

Recently, the whole world seeks for wireless power transfer (WPT) to power up micro-scale electronic systems (i.e., smart sensors platforms, bio-medical implants, and wireless sensor networks)[1]. With the wide range of applications that are located in remote or inaccessible areas. Therefore, WPT is rising solution for such applications. Moreover, RF-to-DC power converter is the core of any wireless power systems which supplies usable dc power from the RF input power coming from the antenna. The main performance metrics of any RF-to-DC converters are sensitivity which defines the minimum RF input power required to generate certain output voltage , and power conversion efficiency (PCE) which defines the output dc power relative to input RF power. The performance of any RF-to-DC converter is improved if sensitivity increased and PCE increased at low input power so the low power wireless powering electronic devices have been the goal for many researches.

RF-to-DC Rectifiers has started with diode-based architectures as full-wave bridge rectifier and voltage multiplier which magnifies output voltage. Voltage multipliers can be cascaded to enhance the rectifier performance. It can be cascaded in series to form Villard circuit or parallel to form Dickson circuit .The main disadvantages is the low sensitivity and the threshold voltage (V_{th}) which affects output DC so they achieve high PCE values which then drops as input power increases due to the high drop voltage. Generally, the performance of Dickson is better than that of Villard concerning PCE and sensitivity. The problem of V_{th} can be decreased by replacing diode connected transistor with Schottky diodes but it requires additional fabrication steps so it is avoided. The used rectifier can be followed by a Dickson charge pump to increase output voltage as in [2]. Several architectures are based on decreasing V_{th} of voltage multiplier either by external V_{th} cancellation scheme , internal V_{th} cancellation scheme as in [3], [4], [5], [6] or self V_{th} cancellation Scheme .A rectifier that employs diode-connected input transistors with self-bootstrapping and bulk biasing can be used to overcome threshold drop. The differential fully cross-coupled (FX) rectifier has improved sensitivity and high PCE peak. In this paper a modification is tested on four designs which are Villard Rectifier, Dickson Rectifier [7], Self-Biased Rectifier based on feedback resistors [8] and Self-Biased Rectifier based on feedback diode-connected transistors [9].

ISM is the Industrial, Scientific and Medical frequency band that is reserved and designated for their devices which use RF signal. This is license free band of radio and microwave frequencies. Some consumer and commercial devices also work in this band around 2.4 GHZ such that WIFI, WLAN, Radio Frequency Identification (RFID) [8], [9], [10] wireless router, Bluetooth and microwave ovens. Eventually, allocation of ISM radio frequencies is stipulated by the International Telecommunication Union (ITU). ITU has documented a worldwide ISM allocation table that varied slightly depending on the region. ISM users must accept laid down terms and regulations to ensure safety and avoid interference. Therefore, the proposed modified architecture is applied at two different frequencies which is 1.9GHz and 2.4GHz to get an advantage of the free ISM-band.

II. Proposed RF-to-DC Converter Circuit Architecture

The proposed methodology is to add LC-filter as a matching circuit between the RF input signal and the rectifier circuit. Since the power conversion efficiency is the main function on impedance matching. In addition, this LC-filter is boosting the input voltage fed to the rectifier to improve the rectifier sensitivity. This filter acts as DC-to-DC boost converter which

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stores energy from the input source then injects it into the load. The inductor used to store the magnetic energy during the negative half cycle and returns it during the positive half cycle. While the capacitor is used to store electric energy during the positive half cycle and returns it during the negative half cycle. The inductor voltage is proportional to the variation rate of the inductor current, as the alternating current is changing constantly so the inductor creates a certain voltage polarity across itself in half cycle and during the next half-cycle creates an opposite voltage which limits the variation in the current. This voltage potential is used for charging capacitors to the strength output voltage. Aims to increase the output voltage, At the resonant frequency, the current through the circuit is at a maximum value so the reactive voltages across L and C are equal and each is greater than the circuit supply voltage, this effect is called Voltage magnification. This can be a very useful property in the antenna stages of radio receivers where a series circuit resonates at the frequency of the transmission being received, is used to magnify the voltage amplitude of the received signal voltage, before it is fed to any transistor amplifiers in the circuit [7].

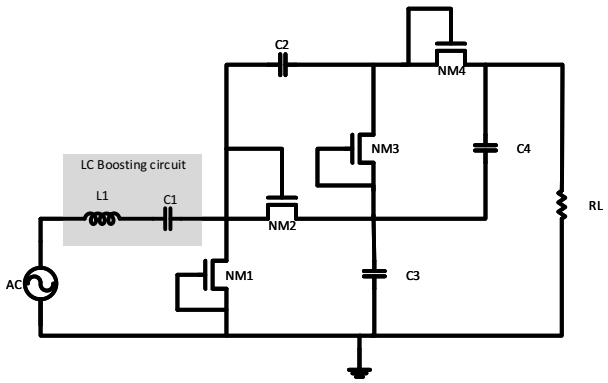

Fig. 1. Modified-Villard

A. Proposed Modified-Villard

The proposed voltage multiplier shown in Fig. 1 increases output voltage by the use of capacitors and diodes, during first half of the cycle the pumping capacitor charges, in the second half of cycle the pumping capacitor acts as a second source added to original source to double output voltage. Therefore , consecutive stages in cascade for multiplier circuit can provide more voltage than the basic circuit so that rectifier can have n stages from voltage multiplier producing higher output voltage , the rectifier output voltage V_{out} is given by the equation (1). But in practice there are restrictions which limit the number of stages, due to increasing number of stages lead to increase parasitic capacitor and power losses [7].

$$V_{out} = \frac{nV_oR_L}{nR_o + R_L} \quad (1)$$

Where n number of stages, V_o one stage open circuit voltage, $R_L$load resistance, $R_o$internal resistance.

Villard shown in Fig. 1, is a circuit of multiple connected series voltage multipliers, it can be considered as batteries connected in series to each other, where each stage adds an offset to the output.

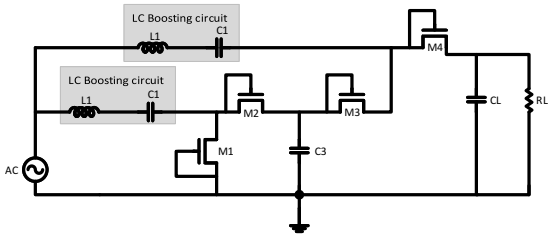

Fig. 2. Modified-Dickson

B. Proposed Modified-Dickson

Dickson rectifier is multiple stages of voltage multiplier circuit connected in parallel shown in Fig. 2. It has a parallel capacitors configuration in order to reduce stages losses. Dickson rectifier achieves PCE approximately 80% but at high input power. It has high peak efficiency than other rectifiers but at high input power. Using this rectifier, the input RF power converts into DC power which multiplies input voltage providing the continuous offset voltage from the previous stage to the next stage [7].

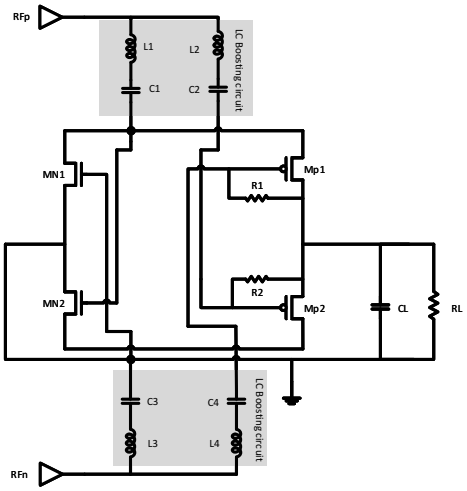

Fig. 3. Modified-Resistive Based Self-Biased

C. Proposed Modified-Resistive

The differential cross coupled rectifier is used due to its improved sensitivity and high peak efficiency shown in Fig. 3. FX rectifier is biased using MOSFETs by charge stored

in capacitors - a way of threshold compensation, Low ON resistance due to high overdrive voltage, Both half cycles of input charges the output capacitor. However, it suffers from leakage current that conducts in opposite direction. This is caused due to the bidirectional characteristics of the transistor where current begins to flow in reverse direction whenever output voltage becomes higher than instantaneous RF input unlike diodes which supports current flow in one direction. Self-biased rectifier was developed to overcome this burden [11], [5].

Self-biased rectifier shown in Fig. 3, is based on FX design to use its merits of high sensitivity at low input power and low drop out voltage. Self-biased is characterized by a low drop out voltage equals to or less than the overdrive voltage so it passes high output .It is based on decreasing the leakage reversible current by increasing effective turn on voltage of the rectifying transistors at high RF input power by connecting output voltage to the gates of the rectifying transistors through high value resistors to act as an RF chock coil (short circuit for Dc and open circuit for Ac).This leads to decreasing the biasing voltage so $V_{SG} = \frac{V_{RF}}{2}$ so leakage current decreases, while having forward turn on voltage= $\frac{V_{DD}}{2} + V_{th}$ which is greater than that of FX. This rectifier has an enhanced efficiency across various input power with a moderate sensitivity [8].

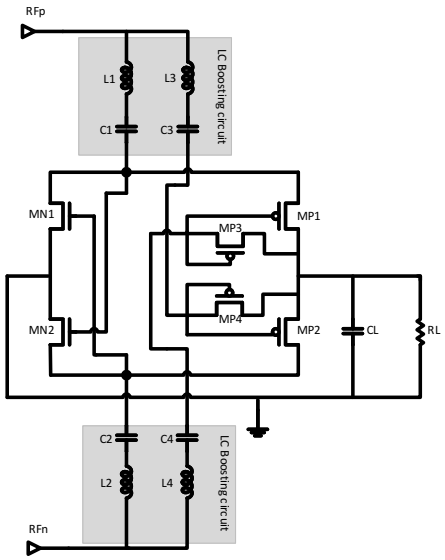

Fig. 4. Modified-Diode-Connected Based Self-Biased

D. Proposed Modified-Diode-Connected

Self-Biased based on feedback resistors shown in Fig. 4 it has high sensitivity , high dynamic range but it decreases the efficiency peak at low input power by decreasing forward current .Therefore ,it has poor performance at low input power than FX [8]. So the most recent architecture is Self-Biased single side design shown in Fig. 4. It is efficient, high peak efficiency at low input power, high sensitivity, less dependent on the load resistance and has an extended dynamic range. This design is based on the self –Biased concept by replacing feedback resistors by diode connected transistors. The main advantages of these diodes are concentrated to provide a variable resistance. It has high peak efficiency like FX as at low input RF power the diode is off R_{off}~∞ so this design acts as FX design thus achieve high peak while at high input RF power diode is on R_{on}~0 so design acts like self-biased based on resistance puts V_{DD} on the gate of PMOS to increase turn on voltage at high input power to decrease leakage current so it has extended dynamic range [9].

III. Simulation Results and Discussions

This part discusses results of the performance of the original rectifier and the modification on the rectifier with LC-filter. The circuits are simulated at two different frequencies 1.9GHz and 2.4GHz and simulated from -20dbm up to -5 dbm. The modification circuit is matched using LC-filter and Rin but the original circuit is matched using only resistance RIN. Simulations were carried out using both 130nm and 65nm technology at two different frequencies. IN both cases PCE of the rectifier has improved specifically at low input power after adding the filter boosting circuit.

A. PCE

The PCE of the proposed RF-to-DC converter circuits is evaluated at two different frequencies 1.9GHz and 2.4GHz as shown in Fig. 5 and Fig. 6, respectively. In each subfigure, the circuit performance is simulated and verified using TSMC 130nm and 65nm, respectively. Using 130nm technology process, the PCE of both modified-Villard and modified-Dickson at 1.9GHz is improved compared to their original architectures by 2.1X and 2.14X at -10dBm, respectively. Moreover, it is improved for modified-Resistive and modified-Diode-Connected by 1.3X and 1.14X at -20dBm, respectively. While the PCE of both modified-Villard and modified-Dickson at 2.4GHz is improved compared to their original architectures by 2.46X and 2.92X at -10dBm, respectively. In addition, it is improved for modified-Resistive and modified-Diode-Connected by 1.7X and 1.3X at -20dBm, respectively. While using 65nm technology process, the PCE of both modified-Villard and modified-Dickson at 1.9GHz is improved compared to their original architectures by 1.37X and 1.32X at -10dBm, respectively. Moreover, it is improved for modified-Resistive and modified-Diode-Connected by 1.1X and 1.04X at -20dBm, respectively. While the PCE of both modified-Villard and modified-Dickson at 2.4GHz is improved compared to their original architectures by 2.56X and 1.73X at -10dBm, respectively. In addition, it is improved for modified-Resistive and modified-Diode-Connected by 1.24X and 1.1X at -20dBm, respectively.

B. Sensitivity

The circuit sensitivity at $V_{out} = 1V$ for the proposed RF-to-DC converter circuits is determined at two different frequencies 1.9GHz and 2.4GHz as shown in Fig. 7 and Fig. 8, respectively. Using 130nm technology process, the PCE

TABLE I
A COMPARISON TABLE BETWEEN THIS WORK AND THE STATE-OF-THE-ART RD-TO-DC CONVERTERS

Architecture	Freq.(HZ)	Tech (nm)	n-stages/load	Peak PCE (%)	Sensitivity(dbm)
Proposed Modified-Villard	1.9G/2.4G	65	1 @ $50K\Omega$	54.95/55.3	-5.535/-5.834
Proposed Modified-Dickson	1.9G/2.4G	65	1 @ $50K\Omega$	53.5/52.6	-5.24/-5.03
Proposed Modified-Resistive	1.9G/2.4G	65	1 @ $50K\Omega$	75.08/77.11	-11.35/-10.74
Proposed Modified-Diode-Connected	1.9G/2.4G	65	1 @ $50K\Omega$	77.9/86.4	-10.62/-9.92
Fully cross-coupled[11]	433M/953M	180	1 @ $100K\Omega$	73/82.6	-14.5/-12.9
Single_Sided self biased[9]	1.9G/2.4G	65	1 @ $50K\Omega$	75.2/74.9	-9.892/-9.204
Double_Sided self biased[9]	433M/953M	180	1 @ $100K\Omega$	86/66	-19.2/-18.2
Res Self-Biased[8]	1.9G/2.4G	65	1 @ $50K\Omega$	65.91/65.49	-10.39/-9.698
Adaptive[12]	900M	180	1 @ $100K\Omega$	65	-18
DC-Boosted Biasing Technique[13]	2.45G	65	2 @ $29K\Omega$	59.6	-17
Dickson Based on Gate Bias Method[14]	2.45G	65	4 @ $13K\Omega$	31	-19
controlled cross coupled rectifier[15]	2.4G	130nm	1 @ $13K\Omega$	55	-5

of the modified-Villard, the modified-Dickson, the modified-Resistive, and the modified-Diode-Connected at 1.9GHz is enhanced compared to their original architectures by 1.5dBm, 2.8dBm, 1.5dBm, and 1.05dBm, respectively. While their senstivity at 2.4GHz is improved by 0.2dBm, 4dBm, 0.2dBm, and 0.8dBm, respectively. And using 65nm technology process, the circuit sensitivity of the modified-Villard, the modified-Dickson, the modified-Resistive, and the modified-Diode-Connected at 1.9GHz is improved compared to their original architectures by 1.5dBm, 1.1dBm, -1dBm, and 0.7dBm, respectively. Moreover, their senstivity at 2.4GHz is improved by 4.6dBm, 2dBm, -1dBm, and 0.7dBm, respectively.

Finally, Table I shows a detailed comparison between this work and the recently published work presented in [11], [8], [9], [12], [13], [14], [15]. The proposed architecture modification improves significantly both PCE and the circuit sentivity. Moreover, the technology process affects the circuit perfromance clearly by improving PCE for all designs. While the circuit sentivity is enhanced based on the architecutre dependency on the leakage current.

IV. CONCLUSIONS

In this paper, an optimization methodology for RF-to-DC converter circuit architecture is discussed. The proposed methodology is investigated through four different RF-to-DC converters. Moreover, a prototype for the modified architectures is presented using TSMC 130nm and 65nm to highlight on the technology process effect on the circuit performance. Finally, the proposed methodology is advantageous in deep sub-micron technologies for low-input-power RF energy harvesting.

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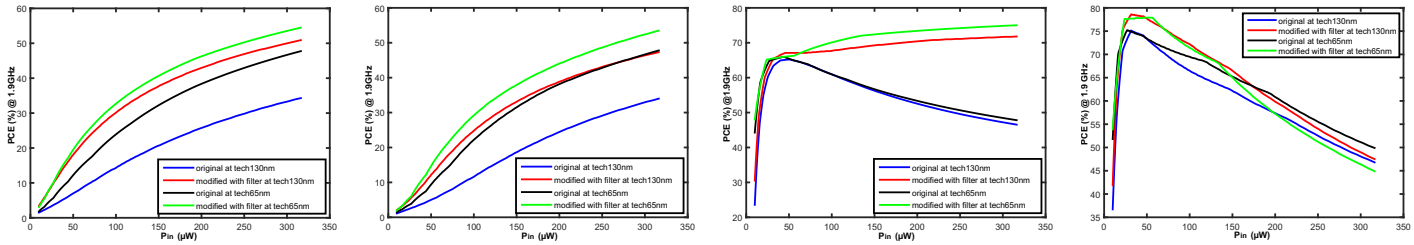
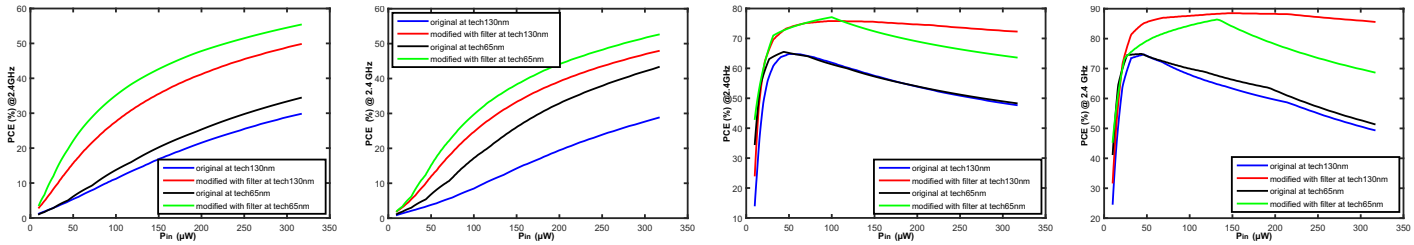


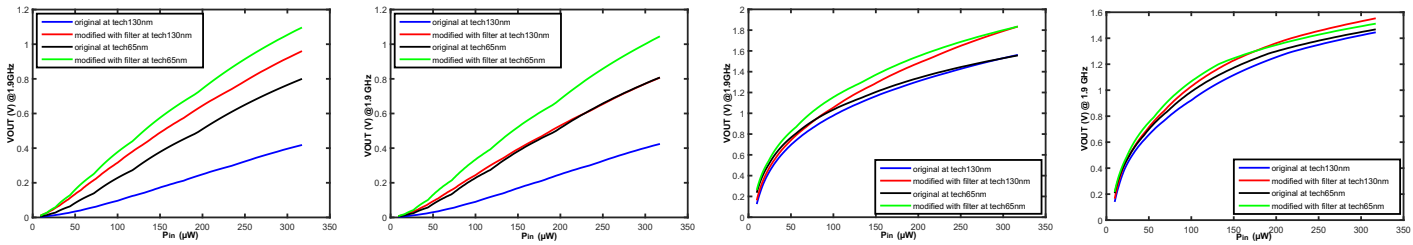
(a) Modified-Villard (b) Modified-Dickson (c) Modified-Resistive (d) Modified-Diode-Connected

Fig. 5. PCE RF-to-DC Converters @ 1.9GHz



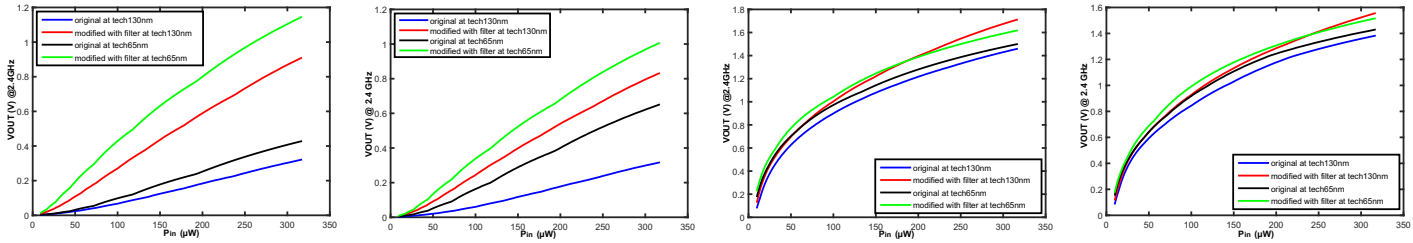
(a) Modified-Villard (b) Modified-Dickson (c) Modified-Resistive (d) Modified-Diode-Connected

Fig. 6. PCE RF-to-DC Converters @ 2.4GHz



(a) Modified-Villard (b) Modified-Dickson (c) Modified-Resistive (d) Modified-Diode-Connected

Fig. 7. Sensitivity RF-to-DC Converters @ 1.9GHz



(a) Modified-Villard (b) Modified-Dickson (c) Modified-Resistive (d) Modified-Diode-Connected

Fig. 8. Sensitivity RF-to-DC Converters @ 2.4GHz