Comparative Study for Some Memristor models in Different Circuit Applications

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***Abstract*—Memristors modeling and applications are a hot topic in research nowadays, mostly because of their unique hysteresis behavior, nanoscale properties and non-volatility. However, there is a scarcity in comparisons between different models on circuit based work. In this paper, four models are examined: two of resistive memristors (TEAM/VTEAM model and ZC modification) and the other two of spintronic memristors (CHEN model and Domain-Wall (DW) based model). Functions and operations of these four models are compared in three applications ranging from memory, analog and logic circuits. Lastly it is concluded that the choice of the model may rely on the type of circuit used.**

Keywords—Resistive memristor, Spintronic memristor, Domain-wall, window function, Read time, Write time, Saturation time, Relaxation based oscillator, Delay.

I. Introduction

Memristor was firstly introduced in 1971 by Leon Chua as the fourth fundamental circuit element [1]. The uniqueness of the memristor stems from its I-V characteristics as it has a hysteresis behavior that gives it the ability to remember its resistance, hence its name: memory-resistance [1]. According to Chua the equations govern the memristor are (1, 2)

$$v(t) = R(w,i) * i(t) \quad (1)$$

$$\frac{dw}{dt} = f(w,i) \quad (2)$$

Where w is defined as the state variable which is different from model to model, $R(w,i)$ is the resistance of the memristor or memristance. It was until 2008 that a team at HP fabricated the first memristor [2]. Since then, different models were introduced to explain the behavior of memristors. The models differ according to the type of memristor, as there are resistive (thin films memristors) such as TiO_x [2] and IMEC HfO_x-based memristor [3], and spintronic memristors that depend on the magnetization vector such as CHEN model [4] and domain-wall model [5]. In this paper, the resistive models used are TEAM model [6], VTEAM [7] and ZC modification model [8], while spintronic models are CHEN [4] and domain-wall (DW) based model (SHERIF) [5].

A. Resistive Memristors

TEAM model is a simplification of the Simmons Tunnel Barrier model [6], as Simmons model is quite complex, however, it is the most accurate model based on the physics of the memristor. Simmons model defines the state variable as the width of an electron tunnel barrier which is modeled in series with a resistor to represent the memristor's active layer. TEAM model uses the same physics in Simmons model, yet with polynomial dependence rather than exponential dependence of the rate of change of the state variable. It has a current threshold for the switching mechanism to take place as well as the flexibility to use either linear or nonlinear I-V relation. It can be modeled to any resistive memristor unlike Simmons model.

VTEAM is another version of TEAM model with the same physics, however, it has a voltage threshold rather than TEAM's current threshold and its importance lies in its applicability in memory circuits [7].

ZC model [8] is a modification with a new window function (Butterworth) on Stanford model which models the switching mechanisms of bipolar memristive devices especially in RRAM applications [9]. The state variable is represented by the gap size and its physics is described as the growth of conductive filament. The advantage of ZC is that the new window function diminishes the ability of the state variable to overcome the assigned lower and upper boundaries while limiting the state variable by the oxide thickness. This results in introducing resistive bands instead of the use of R_{OFF} and R_{ON} as single values which is more accurate to the experimental results.

B. Spintronic Memristors

The idea of spintronic memristor is that the current flux entering the memristor with certain electron spin that changes the spin and magnetization state of the device. This change moves what is called domain wall which separates the free layer FL which has a changing magnetization direction, and pinned layer PL which has fixed magnetization direction. In addition, the domain wall is the state variable. This movement changes the

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resistance of the device. Two spintronic models are chosen, CHEN and Domain Wall-based models which are explained briefly below.

CHEN model uses a current in plane (CIP) structure where two series resistors are connected that represent the resistances in both the parallel and antiparallel regions. It ignores the resistance of domain wall and uses simplified LLG (Landau Lifshitz Gilbert) equation [4]. Whereas domain wall model is a generalized model that can model both CIP and CPP (current perpendicular to plane) structures. It takes into account the domain wall resistance, thermal effect on magnetization vectors and resistances and also models the full LLGS (Landau Lifshitz Gilbert Slonczewski) equation, which adds a torque term- spin transfer torque (STT) which results from the change of angular momentum of spin-polarized electrons. In addition of having voltage dependence on giant magnetoresistance to tunneling magnetoresistance ratio (GMR/TMR), respectively [5]

This work is divided into three sections covering the circuit applications: section II. Memory circuit, section III. Memristor based relaxation oscillator, section IV. Logic circuit and the last section is the conclusion. The parameters for memristors used in the circuit applications differ from model to model and they are extracted as follows: VTEAM and ZC models are obtained from [8] where the parameters are fitted to the experimental data of the IMEC HfOx-based memristor. While the parameters of TEAM model are extracted from [6]. The parameters of the Chen model is obtained from [4], while DW-based model is obtained from [5] using CPP structure TMR based memristor. The circuits used for comparison and simulation are explained in their distinct sections. They were simulated on Cadence Virtuoso using Verilog-A models

II. MEMORY CIRCUIT

In this section, the performance of the four memristor models, previously introduced, is compared in a single memory cell based on 1-memristor (1M) memory. The memory cell circuitry is obtained from [10,11] and shown in Fig. 1. The circuit's R/W enable switch moves between three states: write-where a logic value "1" or "0" is being written to the memristor, read-where the state of the memristor is sensed to read the logic stored in it, and floating-where no operation is being done to the memristor and, hence, no change in its state occurs.

For the write mechanism, a voltage pulse is applied to the memristor. The pulse width must be long enough to ensure the injected flux is sufficient for full switching of the state function to the desired logic value. The read mechanism is more complicated as it requires performing the operation without affecting the memristor's state. The read operation is divided into two stages. First is the convert stage where a read pulse (V_{in}) is applied to sense the memristor's state then a signal is produced (V_x), which is the output of a voltage divider between the memristance R(w) and R_x. V_x is calculated through:

$$V_x = V_{in} * \frac{R_x}{R_x + R(w)} \quad (3)$$

, where

$$Rx = \frac{R_{on} + R_{off}}{2} \quad (4)$$

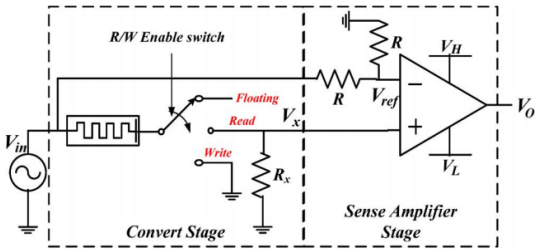


Fig. 1 Memory circuit based on 1M adopted from [10]

Second is the sense amplifier stage where the logic value is read from the output of a comparator that compares V_x with a reference voltage V_{ref}, which is half V_{in}.

The applied read pulse (V_{in}) consists of two pulses of the same magnitude and width but opposite polarities to ensure the net injected flux is zero, which in turn won't affect the memristor's state. For the integrity of the read/write data, a safety margin should be introduced while defining logic values. Therefore, a logic one is defined to be when the memristor's normalized state variable *w/D* is between 0 and 0.4, and a logic zero is defined to be when *w/D* is between 0.6 and 1, or vice versa depending on the model. The region from 0.4 to 0.6 in all the models is treated as undefined logic and should be avoided to account for noise and for data integrity.

For the write operations, the models are subjected to an applied pulse with an amplitude of |2.3| volts with the polarity changing depending on the required logic value. The reason for choosing this specific magnitude is that ZC model won't write for smaller magnitudes which is mentioned in the simulation results. Due to differences between the Verilog-A models, the significance of *w/D* differs from one model to the other as well as the significance of the polarity of the pulse on the logic value being written. For DW-based model, w/D = 1 means that R(w) = R_{on} (logic "1") while in chen model w/D = 1 means R(w) = R_{off} (logic "0"), both of the spintronic models need a negative applied voltage to write "1" and a positive voltage to write "0". For the ZC and VTEAM models, when w/D = 1, R(w) = R_{off} . Both models require a positive pulse to write "1" and a negative pulse to write "0". The write time is calculated when *w/D* reaches 1 from 0 or 0 from 1. For ZC model the state variable was normalized to the gapmax parameter. Since the gap is not limited to the assigned upper and lower limits, during write 0, w/D exceeds the value of 1, however, the write time is measured at the time the upper boundary is reached.

For the read operation, circuit parameters used are shown in Table. 1. An ideal comparator from Cadence's ahdLib library was used in the sense amplifier stage. The only parameter that

differs from one model to the other is R_x. Calculating R_x for models with defined R_{on} and R_{off} (VTEAM, Chen, DW) is straightforward. Nonetheless, for ZC model the determination of R_x took an experimental approach since R_{on} and R_{off} exist as narrow bands. During simulation, the true logic value is read through the second half of the pulse V_o to get the right result. The read time is calculated when the 90 % of the maximum value of V_o is reached in case of reading "1", and at 10% of the maximum value of V_o is reached in case of reading "0".

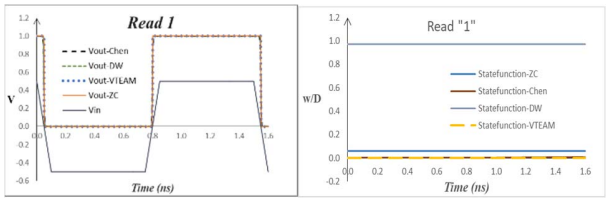
Table.1
Read Circuit Parameters

Read circuit parameters	Vin amplitude	Period of Vin	Rise and Fall time	Rx (Ω)
VTEAM	+-500 mV	1.5 ns	100 ps	625K
ZC-Modification				199K
Chen				5.5K
DW-based				1.795K

Fig. 2 shows the transient analysis simulation. It is noted in the read simulations that the read pulse does not inject enough flux to perturb the memristors' states in either halves of the pulse. However, Chen model is the only exception due to its high sensitivity which makes it prone to read disturbance more than the other models. Table. II concludes the simulation results. For the two spintronic models; Chen exhibited lower power consumption and faster read time while the DW-based model performed better in the read operations and proved less prone to read disturbance. During write "1" and "0" ZC model's gap was very slightly affected by pulse amplitudes less than |2.3| volts yet at |2.3| volts the model shows an abrupt transition after a certain amount of flux is injected. The VTEAM model exhibited a highly asymmetric behavior in the write time as well as the power which exhibited the greediest operation of all during writing "1". Although the VTEAM simulation is fast, it dissipates huge power when compared by the relatively slow and less power greedy ZC. During read ZC consumes more power but in the order of 10^-6 watt which is almost insignificant.

TABLE. II
Simulation Results

Results Table	DW-based	Chen	VTEAM	ZC
Write 1 time (ns)	29.55	8.876	4.136	11.53
Write 1 Power (W)	3.044E-03	6.320E-04	1.466E-02	3.451E-3
Write 0 time (ns)	29.41	8.85	0.9127	10.57
Write 0 Power (W)	3.001E-03	5.781E-04	1.247E-04	2.366E-4
Read 1 time (ns)	0.8025	0.8047	0.8008	0.8008
Read 1 Power (W)	2.86E-04	2.58E-04	2.34E-04	2.37E-04
Read 0 time (ns)	0.80024	0.80584	0.8001	0.8002
Read 0 Power (W)	2.636E-04	2.539E-04	2.351E-04	2.344E-4



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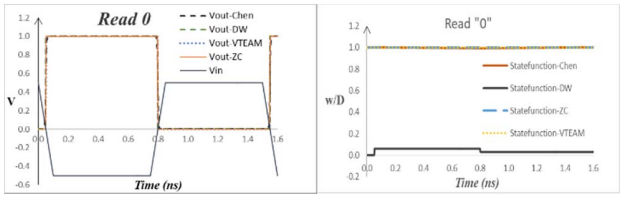

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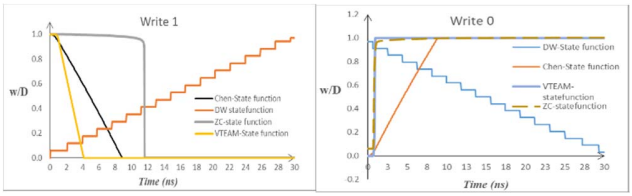


2.c

Fig. 2 Transient analysis simulation. (a) Read 1 scheme and the state variable behavior, (b) Read 0 scheme and the state variable behavior, (c) State variable behavior for write 1 and write 0 operations.

III. MEMRISTOR BASED RELAXATION OSCILLATOR

The memristor was introduced in many oscillator circuits as a substitute for resistors and capacitors [12-15]. The use of memristor in oscillator circuits differs according to the nature and the design of the circuit, so memristors work as substitute to resistances in wein oscillators family as in [13]. In [12] the memristor was used as a substitute to the capacitor in low frequency applications in relaxation oscillator circuits. The behavior of increasing and decreasing memristor resistance due to the direction of current passing the memristor, works as the energy storing property of capacitor so the capacitor can be replaced with memristor. In this paper we used a memristor based relaxation circuit [16]. This circuit is shown in Fig. 3. It consists of a memristor, two comparators, AND gate, inverter and a resistor. The comparators and AND gate act as a Schmitt trigger circuit to fixate the memristor resistance R_m between R_{off}, R_{on} and ensure an oscillation with the mechanism of positive feedback using the resistance R_a that acts as a voltage divider. The inverter works as a substitute to the ground and ensures an extreme voltages between 0,1 applying at the end of the memristor. The comparators and logic gates were ideal components from the ahdlLib library in Cadence with AND gate Vlow = -1, Vhigh = 1, inverter Vlow = 0, Vhigh = 1 and comparator sigout_high = 1, sigout_low = 0 and sigout_offset =0

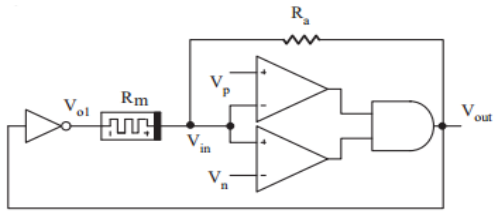


Fig. 3 Memristor-based relaxation circuit adopted from [16]

In [15] the oscillation frequency is given by $f = \frac{k'}{R_a^2} V_{oh} F$ Where V_{oh} is the output high voltage = 1, F is a coefficient depending on the voltage ratios of $\frac{V_P}{V_{oh}}, \frac{V_n}{V_{oh}}$, k' is a memristor model coefficient depends on the dopant mobility, R_{off}, R_{on} and the memristor length. So it depends on the model used.

The parameters of the circuit were the same except only V_P which changed in resistive modeling to spintronic modeling as presented in Table. III. This change was accustomed after iterations on the simulation environment to get the best oscillation.

TABLE III
PARAMETERS OF MEMRISTOR-BASED RELAXATION CIRCUIT

R_a	5.5 KΩ
V_P for Spintronic Memristors	500m V
V_p for Resistive Memristors	600 mV
V_n	-600 mV

The transient analysis as shown in Fig. 4 of the four models give comparable frequency with changes in 0.02 % in spintronic models and 0.04 % in resistive models due to the fact that frequency is dependent on the circuit parameters which are constant among the four models and the memristor coefficient which is comparable to the four models due to fitting the four models to each other. Fig. 4 shows that the four models not on the same phase, that due to the fact that time required to reach oscillation is different from model to another, as it is depending on the way that the model works. In addition, same frequency is observed in the models as anticipated.

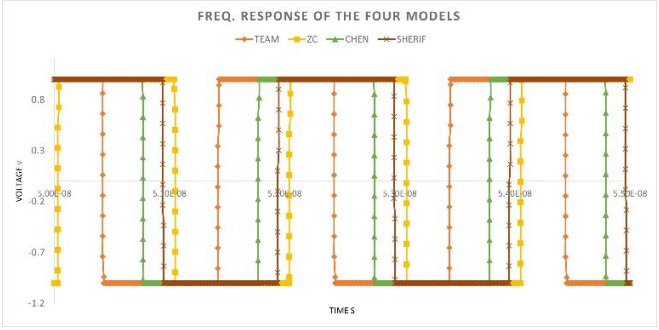
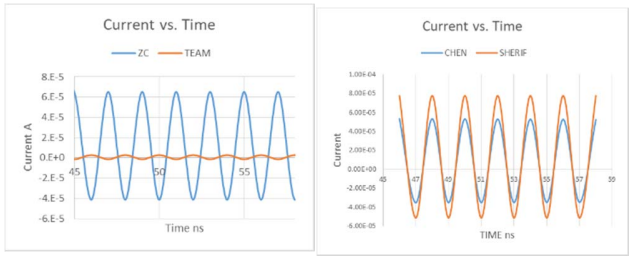


Fig. 4 Transient analysis of the models

As the power = $\frac{V_{out}^2}{R}$ where $R = R_m + R_a$, R_a in the circuit is constant for all models, so power is inversely proportional to R_m - memristor's resistance. The change in R_m is related to the model and how the state function behaves for every model, Table IV clarifies that ZC modification and Domain wall model consume more power than TEAM model and CHEN model respectively as their R_{mn}, R_{mp} is smaller as shown in Fig .5.

TABLE IV.
RESULTS OF FOUR MODELS OF THE SIMULATION OF THE CIRCUIT

	TEAM	ZC	CHEN	DOMAIN WALL
Frequency (HZ)	4.975E+08	4.973E+08	4.975E+08	4.974E+08
saturation Time (sec)	5.185E-09	7.528E-09	5.550E-09	9.726E-09
R_{mp} (Ω)	8.333E+05	3.296E+04	2.448E+04	1.514E+04
R_{mn} (Ω)	3.378E+05	9.513E+03	5.704E+03	2.265E+03
Power (Watt)	1.823E-06	3.166E-05	3.817E-05	4.841E-05



(a) (b)

Fig .5 Current Behavior with Time (a) ZC and TEAM models current behaviors (b) Chen and Domain Wall Current behaviors.

IV. MEMRISTOR RATIOED LOGIC

The logic operations are at the heart of any computational device. For long, the CMOS logic operation was the most logic family used due to its great properties. The advent of memristors allows integrating memristors with CMOS which saves physical layers and increase logic density [17]. The MRL or memristor ratioed logic is a proposed logic to integrate CMOS with memristor. The integration is performed as the memristors do the logic operation with a CMOS inverter to provide the negation of the logic operation. NOR gate is simulated using the four models. The power, delay and the behavior of such circuit are studied.

The NOR gate is shown in Fig. 6 below. The principle of operation depends on the property of memristor changing resistance according to the direction of current passing it, as shown in Fig. 7, the opposite operation happens at $V_{in2} = 1$, $V_{in1} = 0$. The two memristors work as voltage divider, and give an output voltage depending on the memristances values: R_{off}, R_{on}. This output voltage is then inverted using CMOS inverter. We simulate the four models in a Cadence virtuoso with TSMC 130 nm CMOS technology file. The CMOS has

130 nm length and 2 um width. The avg. power and delay are summarized in Table V. The results show substantial improvements in delay in ZC over TEAM; this can be attributed to more current being drawn in ZC as observed in oscillator circuit. It is worthy to mention that power in ZC did not increase as it did in oscillator circuit, this may be attributed to the way ZC model deals with transitions from high to low in digital logic. For CHEN and DW models, they are comparable with slightly improvement for DW model as it incorporates GMR voltages.

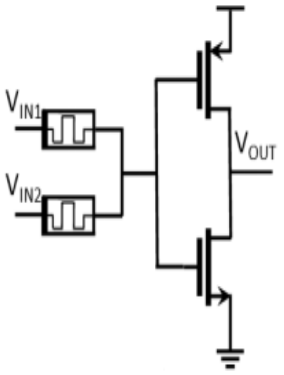


Fig .6 NOR MRL gate adopted from [17]

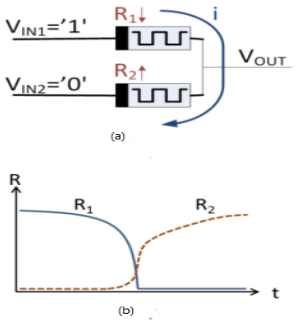


Fig .7 adopted from [17] (a) explains the direction of current at V_{in2} = 1, V_{in1} =0 and its effect on resistance of the memristor. (b) shows the behavior of resistance of the memristances

TABLE V
RESULTS OF FOUR MODELS OF THE SIMULATION OF THE CIRCUIT

	TEAM	ZC	CHEN	DOMAIN WALL (DW)
Avg. power (Watt)	1.015E-05	9.507E-06	9.747E-06	9.127E-06
Delay (sec)	2.394E-09	2.963E-10	3.89E-11	2.84E-11

V. CONCLUSION

The application-based comparison between the four models shows that some models behave more efficiently in some applications while they are surpassed by other models in other applications. In memory, CHEN model exhibited better write performance while the DW model was better during read, VTEAM showed greediness for power while performing faster during write operations. While in analog applications such as oscillators, TEAM and CHEN models behave very well in power consumption and saturation time. This is due to the way these models behave to changes in voltage and current which is more compact and well defined than ZC and Domain wall models. On the other hand, in logic applications as we deal with extremities in voltage, ZC and Domain wall surpass other applications due to the window function that is more compact in the extremes in ZC and GMR voltage dependences that is covered by Domain Wall model.

VI. ACKNOWLEDGEMENT

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