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A high precision write/read circuits for memristors using digital input/output interfaces

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ABSTRACT

In this paper, high precision write and read circuits for memristors are proposed. The proposed write circuit utilizes a DC voltage provided by a Digital-to-Analog Converter (DAC) to tune the memristor to a specific memristance. A feedback link is connected to read the final memristance, and determine the required decision of switching the memristance to a lower or a higher memristance value. An Analog-to-Digital Converter (ADC) is used in the read circuit to convert the read voltage to a digital word. Simulations are carried out to test the proposed write and read circuits. Industrial hardware-calibrated TSMC 130 nm CMOS technology models are used in Cadence Spectre environment simulation tool throughout all the simulations.

1. Introduction

The memristor is the fourth passive element that exhibits different current-voltage characteristics depending on its configurations. Several mathematical models are provided in the literature to describe the memristor behaviors. The memristor is theorized by Leon Chua [1,2], and the first memristor device is realized by HP Labs [1,3]. It is mainly characterized by its resistance (called memristance) which relates the applied flux with the flowing charge. The memristor is a contraction for memory resistor because it remembers its resistance. It has a minimum and a maximum memristances, and its memristance is bounded between these two values. In order for the memristor to have a specific memristance state, special tuning (programming) circuits are required to tune it. Consequently, the memristor is used in single-bit (having one of two memristances) and multi-bit (having one of multiple memristances) memory cells to implement high-density resistive random access memory (RRAM) arrays [4–11].

Memristors are promising devices, and accordingly many circuit applications use them due to their unique characteristics such as non-volatility, fast switching times, high packing density and compatibility with CMOS logic. The memristors can be used in content addressable memory (CAM) [12,13], fast reading and writing for memory circuits with low power consumption using CMOS interfaces [4], and multi-bit memristor based circuits [14–17]. In addition, circuits like relaxation oscillators [18–21] and chaotic oscillators [22–25] use memristors. The memristors also are used recently in neural networks [8,26–28]. These applications may require fine or high precision write circuit for their memristances. Many write circuits have been presented to achieve such high precision target [7,11,29–33], and these write circuits use different techniques to program the memristors.

The idea of a write circuit is to apply positive or negative voltage on the memristor's terminals to change its state from higher to lower value, or vice versa. The memristor is then read by applying a low voltage so that the change of its state is minimal. A refresh is required after successive read operations if the deviation of the final state from the initial state is high enough such that the refresh/reprogram is required, or the memristor will flip its value from '0′ to '1′ or from '1′ to '0'.

Many write circuits are presented in the literature. In Refs. [30–32], the authors use pulses with specific width and amplitude to write, read and refresh a memristor to a specific memristance state. These pulses-based write circuits need to compute the pulse width required for the memristor to reach a specific memristance state. In Refs. [11,34],

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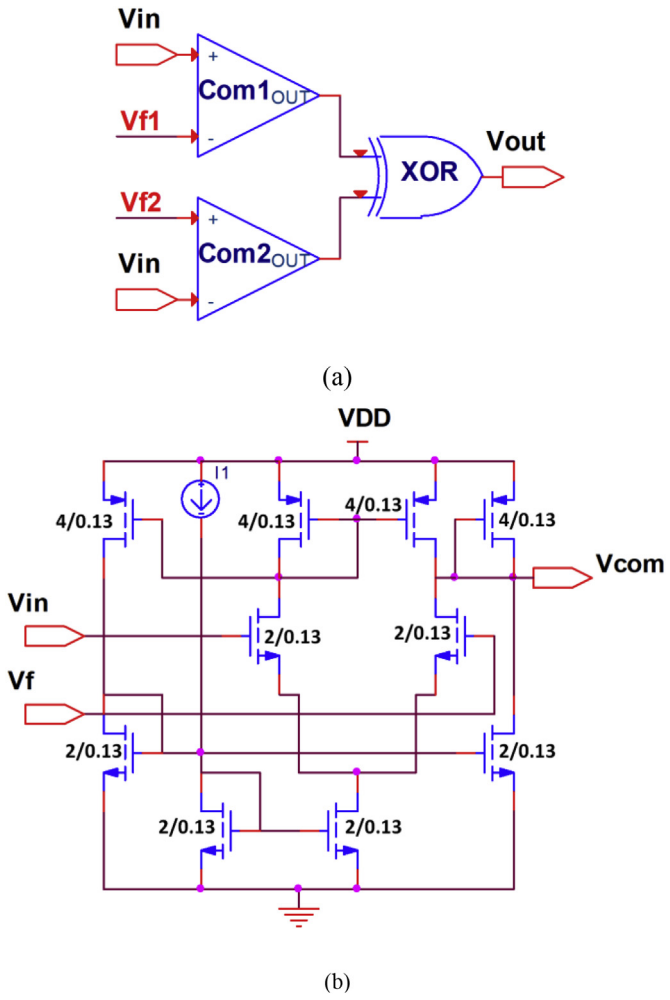

Fig. 1. (a) The presented write circuit with two feedback voltages V_{f1} and V_{f2}. (b) the circuit schematic of the comparators.

authors utilize reference resistors with many selective switches left undiscussed so that the memristance can 'latch' onto them. The use of the reference resistors is poor in terms of area since many reference resistors are needed in both write and read circuits. However, the reference resistors can be replaced by one voltage controlled resistor, or implemented by a group of series or parallel non-switching memristors. In Ref. [17], the current charged by input capacitors are used to tune the memristor, however, the write delay is long due to the used of capacitive part. The authors in Ref. [29] use a read signal of an AC source which alters the memristance during read operation, especially in case of highly asymmetric memristors (i.e., asymmetric ON and OFF switching characteristics) as the memristor tends to change faster for one type of switching.

The rest of the paper is organized as follows. In Section 2, the memristor model used in simulation and the high precision write circuit are presented. Simulation results are given in Section 3. The conclusion is provided in Section 4.

2. Proposed write circuit

A write circuit is proposed in this work to implement high precision write circuit without the need for external AC source, reference resistors and additional processes to calculate the applied pulse width.

The model utilized in the simulation is provided in Refs. [35,36]. This model is selected for simulation as it mimics highly asymmetric I–V characteristics, and it provides specific definitions of the extreme memristances R_{ON} and R_{OFF}, and an explicit definition of the memristance

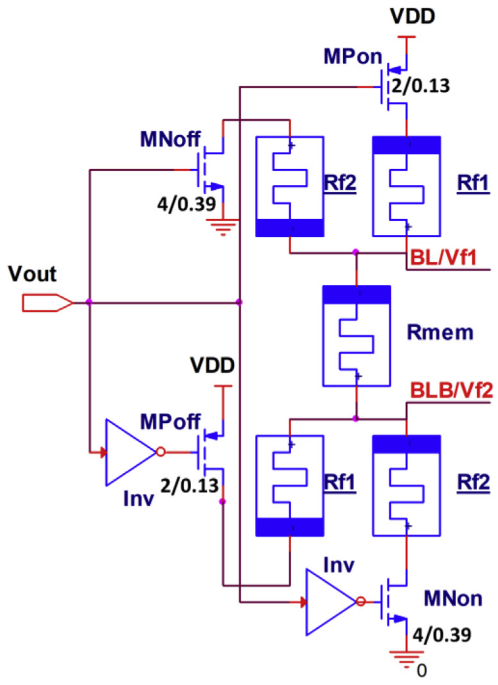

Fig. 2. The presented write circuit providing two feedback voltages V_{f1} and V_{f2} on two bit-lines BL and BLB.

R_{MEM}. In addition, the model-defined memristance varies between the very low ON memristance and the very high OFF memristance as the model does not use a conventional threshold. The model equations are provided in (1) through (5), where the memristance $R_{MEM}(x, v(t))$ is defined by (1) and (2), the state variable derivative dx/dt is defined in (3), the window function $f(x)$ is defined in (4) for both the ON and OFF switching operations respectively. The memristive state depends on the voltage $v_{mem}(t)$ as in (5).

$$R_{MEM}(x, v(t)) = (R_{OFF}(1 - x(t)) + R_{ON}x(t))\times \cosh\left(b_p v_{mem}(t)\right), v_{mem}(t) \geq 0 \tag{1}$$

$$R_{MEM}(x, v(t)) = \frac{(R_{OFF}(1 - x(t)) + R_{ON}x(t))}{\cosh(b_n v_{mem}(t))}, v_{mem}(t) < 0 \tag{2}$$

where $x(t)$ ranges from 0 to 1 to represent the memristive state at time t, b_p and b_n are fitting parameters, and they are similar to non-traditional threshold voltages. The memristive voltage $v_{mem}(t)$ along with the fitting parameters c_p and c_n control the excitation dependent function g in (5). Parameters A_n and A_p are scaling factors, while α_p, S_p and α_n control the shape of the window function. A small constant ε is used to prevent $f(x)$ from holding at either $x = 0$ or $x = 1$.

$$\frac{dx}{dt} = g(v_{mem}(t)) \cdot f(x(t)) + \varepsilon \tag{3}$$

$$f(x) = \begin{cases} \left(1 - x^2\right)^{\alpha_p} \cdot (1 - (2x - 1)^{s_p}), v_{mem}(t) \geq 0 \\ x(1 - x)\exp(-\alpha_n x), v_{mem}(t) < 0 \end{cases} \tag{4}$$

$$g(v_{mem}(t)) = \begin{cases} A_p \sinh\left(c_p v_{mem}(t)\right), v_{mem}(t) \geq 0 \\ A_n \sinh(c_n v_{mem}(t)), v_{mem}(t) \geq 0 \end{cases} \tag{5}$$

Furthermore, the circuits are tested using the TEAM model [37], however there is a limitation in the TEAM model. For low voltages and high memristances (low memristive currents), the change in memristance is stopped by the relatively high ON and OFF threshold currents which are required to be very low for non-zero dx/dt. In addition, the low threshold currents result in convergence problems in the simulations.

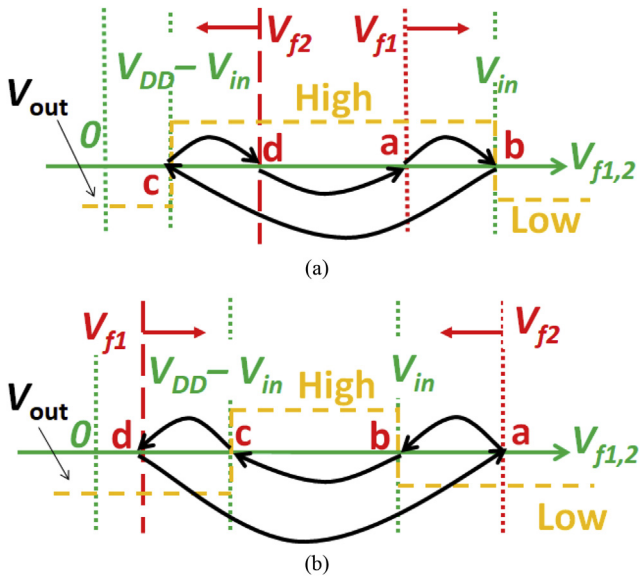

Fig. 3. The transition between different states under high and low output voltage in the write circuit.

An analog programming write circuit is proposed as shown in Figs. 1 and 2. The main idea of the proposed circuit is to avoid the need for inverting the input voltage and hence the extra negative power supply used in the literature [7,11,30,32,33,38]. This circuit uses an XOR gate with W/L ratio of 4/0.13 and 2/0.13 for NMOS and PMOS transistors respectively, and the XOR output controls the switching of a memristor R_{mem} by selecting the ON or OFF switching paths.

The write circuit modulates the memristance of R_{mem} using a constant positive DC signal V_{in} (the input voltage). Two feedback voltages V_{f1} and V_{f2} are taken from a voltage divider of two feedback resistors R_{f1} and R_{f2}, and the memristor R_{mem}, and then compared to V_{in}. Each of these resistors is implemented using parallel memristors acting like a single memristor connected under the OFF switching and having their maximum memristances R_{OFF}. The comparators used for are differential-based OTA. The circuit schematic of these comparators is shown in Fig. 1.

In Fig. 2, two memristors entitled R_{f1} are connected such that their negative terminals are linked to the supply voltage V_{DD} (2 V throughout the design), while two memristors entitled R_{f2} are connected such that their positive terminals are linked to the ground. The other terminals of the four memristors are linked to the memristor under programming as shown in Fig. 2. This configuration guarantees that the four feedback memristors are not programmed by inverting the XOR gate output V_{out}. Another implementation for each of the feedback memristors is to use series memristors having their minimum memristances R_{ON} and acting like a single memristor connected under the ON switching.

Fig. 3a shows how the write circuit works for the OFF switching. The write is performed by applying a certain value of V_{in}, while V_{in} is higher or lower than the feedback voltages V_{f1} and V_{f2} respectively. If V_{f1} falls below V_{in}; at point 'a', the XOR gate provides logic high output that raises the value of V_{f1} toward V_{in}. Thus, the memristor experiences high output voltage and switches towards the OFF state. When V_{f1} exceeds V_{in} at point "b", V_{out} becomes low which makes V_{f1} and V_{f2} exchange their values and V_{f1} reaches point "c" at which V_{f1} is lower than V_{DD}–V_{in}. At this point, V_{out} is high again, and V_{f1} rises again until it exceeds V_{DD}–V_{in} at point 'd', and then V_{out} inverts to high again and raises V_{f1} toward V_{in} as V_{f1} must be higher than V_{f2}.

Similarly, Fig. 3b shows how the write works for the ON switching. The write is performed by applying a specific value of V_{in}, where V_{in} lies between V_{f1} and V_{f2}. At point 'a', the XOR gate provides logic low output that lowers the value of V_{f2} toward V_{in}. Thus, the memristor experiences low output voltage and switches towards the ON state. When V_{f2} falls

Table 1
Relation between the Input and the feedback voltages for $V_{f1} > V_{f2}$.

Case NO.	Input and feedback voltages relation	Comparators outputs (V_{com1}, V_{com2})	Output voltage (V_{out})
1	$V_{in} > V_{f1}$, $V_{in} > V_{f2}$	$V_{com1} = 1$, $V_{com2} = 0$	$V_{out} = 1$
2	$V_{in} < V_{f1}$, $V_{in} > V_{f2}$	$V_{com1} = 0$, $V_{com2} = 0$	$V_{out} = 0$
3	$V_{in} < V_{f1}$, $V_{in} < V_{f2}$	$V_{com1} = 0$, $V_{com2} = 1$	$V_{out} = 1$

Table 2
Relation between Input and feedback voltages for $V_{f1} < V_{f2}$.

Case NO.	Input and feedback voltages relation	Comparators outputs (V_{com1}, V_{com2})	Output voltage (V_{out})
4	$V_{in} > V_{f1}$, $V_{in} > V_{f2}$	$V_{com1} = 1$, $V_{com2} = 0$	$V_{out} = 1$
5	$V_{in} > V_{f1}$, $V_{in} < V_{f2}$	$V_{com1} = 1$, $V_{com2} = 1$	$V_{out} = 0$
6	$V_{in} < V_{f1}$, $V_{in} < V_{f2}$	$V_{com1} = 0$, $V_{com2} = 1$	$V_{out} = 1$

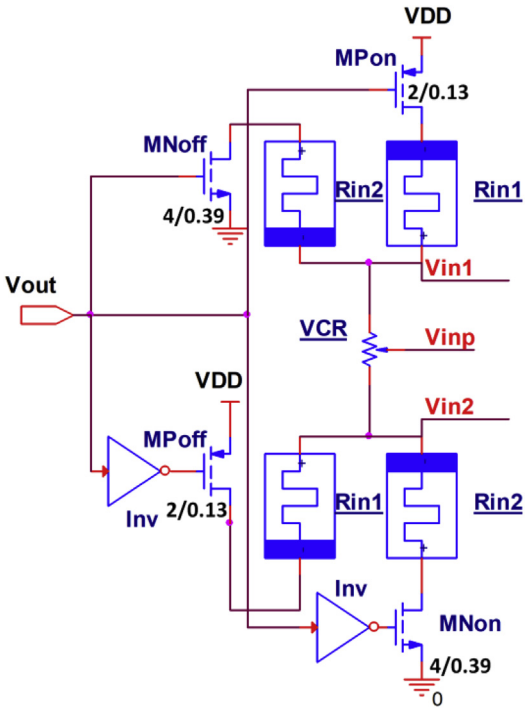

Fig. 4. A Circuit providing two complementary input voltages V_{in1} and V_{in2}.

below V_{in} at point "b", V_{out} becomes high which makes V_{f1} and V_{f2} exchange their values and V_{f2} reaches point "c" at which V_{f2} is higher than V_{DD}–V_{in}. At this point, V_{out} is high again, and V_{f2} decrease again until it falls below V_{DD}–V_{in} at point 'd', and then V_{out} inverts to low again and lowers V_{f2} towards V_{in} as V_{f2} must be higher than V_{f2}.

The output of the XOR gate V_{out} starts to oscillate announcing the end of programming phase and the start of latching phase in which the memristance is almost fixed at a certain value. If V_{in} varies, the relations between V_{in} and the feedback voltages changes and therefore V_{out} changes.

Tables 1 and 2 show the relations between the input voltage and the two feedback voltages and how they control the output of the XOR gate for the ON switching and the OFF switching respectively. In case of the OFF switching, the XOR output voltage (V_{out}) is high, and V_{f1} is higher than V_{f2}. While, in case of the ON switching, V_{out} is low, and V_{f1} is lower than V_{f2}. The circuit switches the memristor to different states according to the relation among V_{in}, V_{f1} and V_{f2}.

The input voltage V_{in} is one of two complementary input levels V_{in1} and V_{in2} (e.g., V_{in} is replaced by V_{in2} in Fig. 1) generated by the circuit

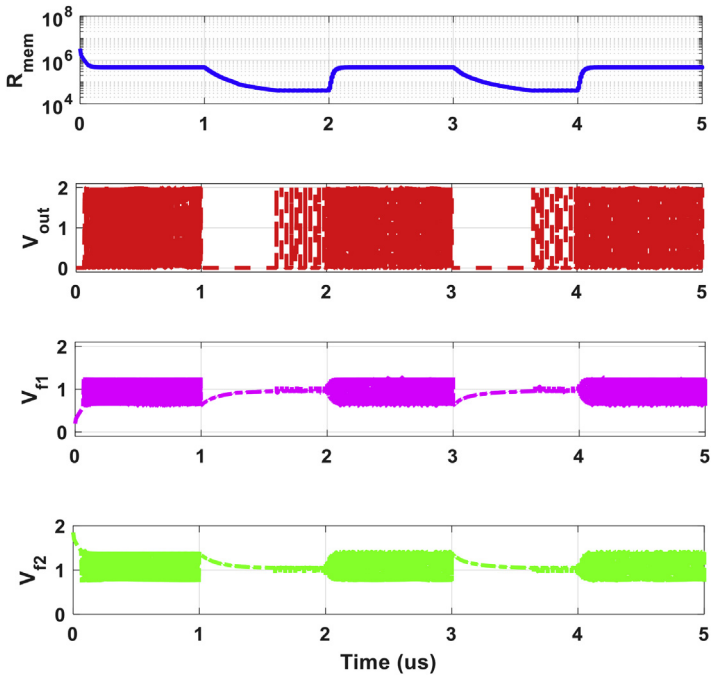

Fig. 5. The variation of the memristance, feedback and output signals of the write circuit.

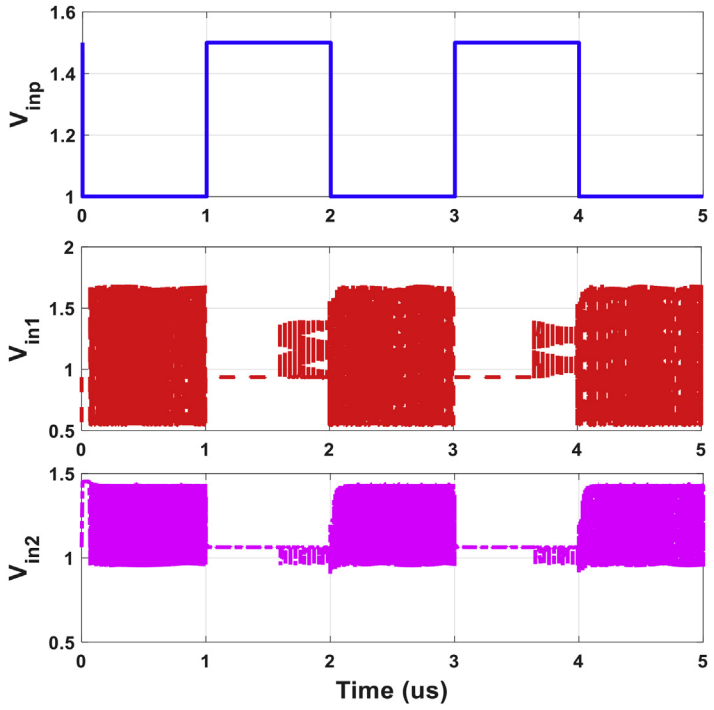

Fig. 6. The input signals V_{inp}, V_{in1} and V_{in2} of the write circuit.

shown in Fig. 4. The complementary input level V_{in2} is applied to twice the parasitic capacitance as seen by each feedback voltage at the inputs of the two comparators. A voltage-controlled resistor (*VCR*) is used to implement such complementary inputs. *VCR* is important to map from an input voltage V_{inp} to the input levels V_{in1} and V_{in2}, and it is implemented using an NMOS device.

Like the feedback resistors, and as shown in Fig. 4, two memristors entitled R_{in1} are connected such that their negative terminals are linked to the supply voltage V_{DD}, while two memristors entitled R_{in2} are connected such that their positive terminals are linked to the ground. The other terminals of R_{in1} and R_{in2} are linked to the VCR. Another implementation for each of the input memristors R_{in1} and R_{in2} is to use series memristors having their minimum memristance R_{ON} and acting like a single memristor connected under the ON switching.

The use of the complementary input enhances the circuit performance affected by the parasitic capacitances which prevent the fast charging and discharging of the feedback voltages and hence the crossing between the input voltage and the feedback voltages.

The circuit in Fig. 4 allows the input level to closely follow the change of the feedback voltages giving an opportunity for crossing. In addition,

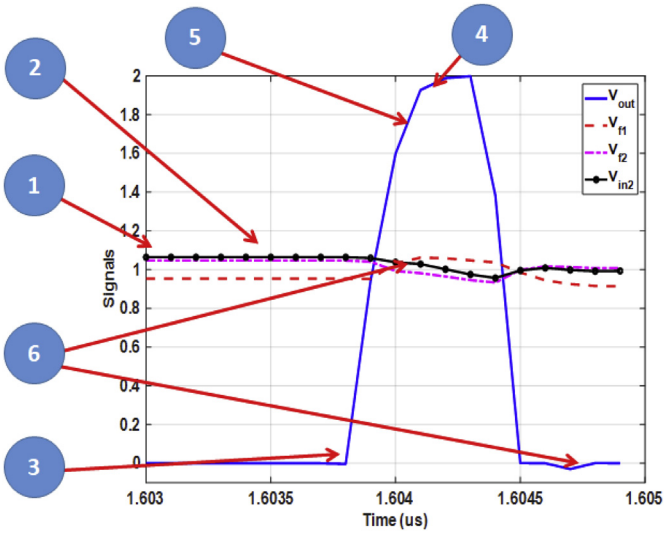

Fig. 7. The signals of the write circuit before and during the first V_{out} inversion at the end of the ON switching, where (1) end of far-away crossing between falling V_{f2} and V_{in2}, (2) ON switching occurs, (3) rising delay of V_{out}, (4) V_{out} is high, V_{f2} falls, (5) OFF switching occurs, (6) early crossing to RESET V_{out} (Low).

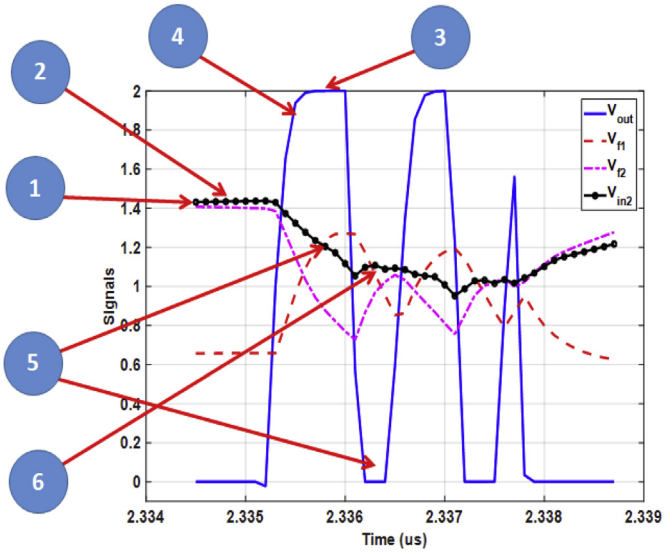

Fig. 8. The signals of the write circuit under a dominant OFF switching, where (1) end of far-away crossing between falling V_{f2} and V_{in2}, (2) ON switching occurs due to Initial Cond. (3) V_{out} is high, V_{f2} falls, (4) OFF switching occurs, (5) late crossing to RESET V_{out} (Low), (6) early crossing to SET V_{out} again.

the input levels V_{in1} and V_{in2} should change faster than V_{f1} and V_{f2} and settle at their extreme values so as to be crossed properly by V_{f1} and V_{f2}. Therefore, the feedback and input resistors and the parameters of the PMOS and NMOS are selected to achieve slower charging/discharging for V_{f1} and V_{f2} and faster charging/discharging for V_{in2} and V_{in1}.

The resistances R_{in1} and R_{in2} are selected to be lower than the half of R_{f1} and R_{f2}, so that the input voltages are faster in charging and discharging than the feedback voltages which are meant to cross the input levels only by the effect of memristive switching.

3. Simulation results

Figs. 5 and 6 show the simulation results for the write circuit using TSMC-130nm CMOS models. Comparing the feedback voltages against V_{in2} drives the memristance to about 460 KΩ for 41 kΩ at V_{inp} of 1 and 1.5 V respectively.

In order to understand how the memristance holds at a certain value, the oscillations observed in Figs. 5 and 6 at about 1.6 μs and 2.3 μs are explained. From Fig. 1, if V_{in2} lies between V_{f1} and V_{f2}, the memristor experiences low V_{out} and makes ON switching. During the ON switching, V_{out} is low, V_{f1} is lower than V_{f2}, and V_{f1} rises and V_{f2} falls toward V_{in2}. Since V_{f2} is closer to V_{in2} than V_{f1} due to the complementary structure, V_{f2} crosses V_{in2}, therefore V_{in2} becomes higher than V_{f2} as shown in Fig. 7 at t = 1.603 μs. Fig. 7 shows the end of the ON switching operation as V_{out} changes its state to high at t = 1.6037 μs and retain its low state again at 1.6045 μs At t = 1.603 μs, V_{in2} is higher than both V_{f1} and V_{f2} pushing the OFF switching to occur, however no OFF switching occurs until V_{f1} becomes higher than V_{f2}. At t = 1.6037 μs, V_{out} tends to make a transition from low to high, V_{f1} rises with V_{out}, and V_{f2} and V_{in2} fall as shown in Fig. 7 at t = 1.6038 μs

In order to revert V_{out} again to logic zero and mitigate the effect of the OFF switching made by high V_{out}, V_{in2} should be crossed by either V_{f1} or V_{f2} and then crossed again by any one of them. As V_{f1} rises and it is lower than V_{in2}, it crosses V_{in2} at t = 1.6039 μsas shown in Fig. 7, then V_{out} tends to go low. Since V_{out} does not make abrupt change, V_{out} starts to go low lately at t = 1.6044 μs, and V_{in2} and V_{f2} continue to fall. Since V_{in2} is faster and higher than V_{f2}, V_{f2} crosses V_{in2} at t = 1.6044 μs Consequently, V_{out} tends to go high again (not shown in Fig. 7).

The input level V_{in2} is constant at an extreme value during the ON switching (before any crossing occurs), then oscillation occurs as a repeating of the waveform shown in Fig. 7. The waveform under the ON switching can be like that shown in Fig. 8 with the signals inverted, if the difference between V_{in2} and V_{f1} is high enough (i.e., the difference between V_{in2} and V_{f2} is low enough) for V_{f2} to make multiple crossings with V_{in2} before a crossing between V_{in2} and V_{f1} takes place. In Fig. 8, V_{f1} makes multiple crossings with V_{in2} before a crossing between V_{in2} and V_{f2} takes place as it demonstrates the OFF switching.

The OFF switching starts when V_{in2} goes higher or lower than both V_{f1} and V_{f2} as shown in Fig. 8. Assuming V_{in2} is driven to be higher than both V_{f1} and V_{f2} at time of 2.335 μs, and an initial condition of V_{f2} being higher than V_{f1}, and V_{out} is low; therefore, V_{out} goes high, and V_{f1} rises and V_{f2} falls until one of them crosses V_{in2}. At 2.3352 μs, the difference between V_{f1} and V_{in2} is large, this gives an opportunity for V_{f1} to exceed V_{f2} and drive the memristance towards the OFF state until the crossings between V_{f1} and V_{f2} at 2.3363 μs takes place. Since V_{f1} is compared to V_{in2} not V_{in1}, the circuit flips V_{out} again to logic zero after their crossing at 2.3357 μs Consequently, oscillation occurs before reaching the required memristance. The triplet shown in Fig. 8 is repeated until the memristance holds a certain state at which the difference between V_{in2} and V_{f2} is minimal and V_{f1} and V_{f2} makes two close crossing with V_{in2}.

The faster charging and discharging speed designed for V_{in2} and the larger values selected for the VCR under OFF switching (low charge sharing between the input levels) helps the input level V_{in2} approach its extreme values faster and to cross both V_{f1} and V_{f2} while it is inverting its states. Nevertheless, this is not the case if the memristance is low enough for the feedback voltages to change faster than the input voltages. For instance, for the case represented in Fig. 8, V_{in2} crosses V_{f1} at 2.3357 μs, and V_{out} makes a transitions before V_{in2} crosses V_{f2}. Since V_{in2} does not reach its extreme value (1.41 V), it crosses V_{f1} at 2.3362 μs after V_{out} goes

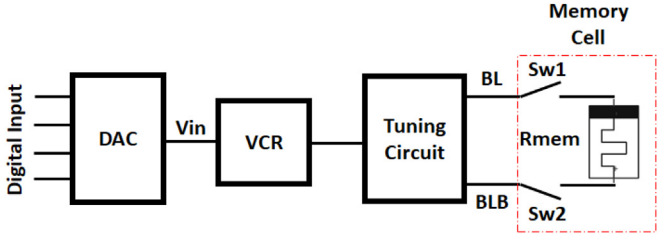

Fig. 9. The full write system.

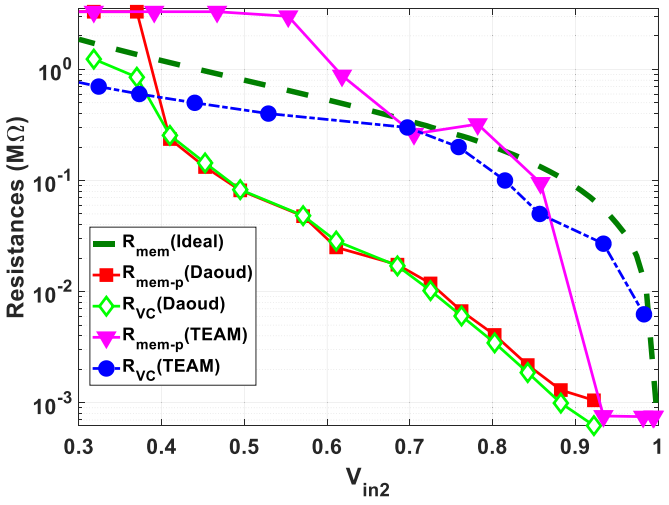

Fig. 10. R_{mem} vs V_{in2} under the effect of bit-lines parasitic capacitances, $R_{in1,2}$ = 200 KΩ, where $R_{mem\text{-}p}$ is the programmed memristance.

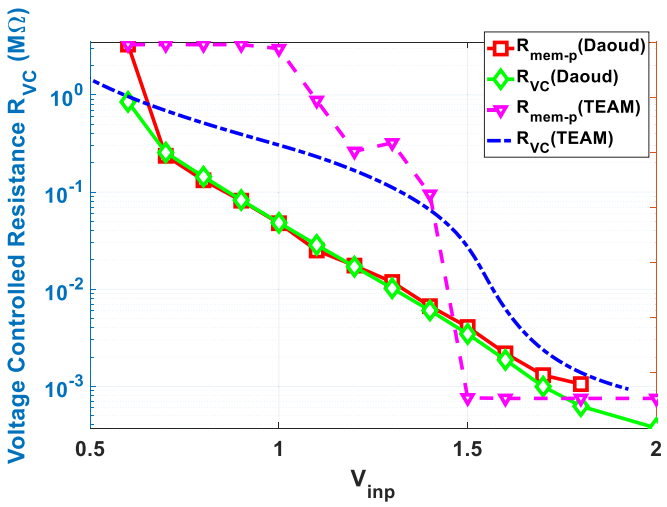

Fig. 11. The Voltage-controlled resistance *VCR* and the programmed memristance $R_{mem\text{-}p}$ vs. V_{inp}.

low. Consequently, the ON switching period is relatively short and this helps for allowing for the OFF switching.

In case of that V_{in2} starts lower than both V_{f1} and V_{f2}, and V_{out} is high, then V_{f2} evolves until it falls below V_{in2}, and a waveform like that shown in Fig. 7, but with inverted signals, and a switching to the OFF state takes place.

The full write system includes using of a digital to analog converter (DAC) to control the VCR as shown in Fig. 9. The DAC is a summing operational amplifier (OPAMP) with 0 and 2 V supply rails. According to the number of inputs, the precision of V_{inp} is determined. In Fig. 9, BL and BLB are the bit-lines that are considered to be V_{f1} and V_{f2} while write the memristor.

The main idea of the paper is to show and focus on the precision of the tuning, hence a simply designed DAC and VCR are used. However, any other type of DAC and/or VCR can be used as an enhancement of the proposed circuit, e.g., capacitive DAC [39,40] can be used instead of the resistive one.

3.1. Effect of bit-lines parasitic capacitances

In the write circuit, the input level V_{in2} charges after V_{out} becomes low and discharges after V_{out} becomes high as shown in Figs. 7 and 8. For the input levels V_{in1} and V_{in2} to be easily tracked by V_{f1} and V_{f2}, the input nodes should be connected to capacitances to neutralize the effect of the parasitic bit-lines capacitances accumulated at the feedback nodes. Consequently, the charging and discharging are affected by the added capacitances that add to the parasitic capacitances of the input ports of the comparators Com 1 and Com 2. In order to analyse the effect of the parasitic capacitances, four pairs of equations; (6) through (13) are extracted from Figs. 2 and 4, where V_{DD}' and V_{gnd}' are the drain voltages of the access PMOS and NMOS transistors respectively. These equations represent the charging and discharging of the signal nodes at V_{in2}, V_{in1}, V_{f2} and V_{f1} respectively.

Equation (6) through (13) along with the derivative of state variable dx/dt in (14) and (15) form a system of linear differential equations. Some simplifications are made in order to solve this system. First, V_{DD}' and V_{gnd}' are considered V_{DD} and zero respectively. Second, the complementary feedback voltages through consecutive charging and discharging meet at the mid-way of V_{DD}, i.e., $V_{DD}/2$. Therefore, their initial values are 1 V. Third, dx/dt is considered zero at its final rest value (target value).

The ten equations (i.e., (6)–(15)) should be solved several times starting from a selected initial value of x with non-zero derivative and the solution is stopped when zero (so small) derivative is achieved. For the best of our knowledge, and after these simplifications, these equations are so difficult to be solved, and the solving procedure is similar to a transient solution. Equations (6)–(15) neglect the parasitic wire resistances of the memory array, however wire resistors are modeled using the distributed RC model in the transient simulation. So that transient simulations are useful, however time consuming. Fig. 10 shows R_{mem} vs. V_{in2} under the effect of 16 fF parasitic bit-line capacitances per column which correspond to 256 fF per column in a single-bit cell memory system. The written memristances is shown for V_{in2} range of 0.3–1.0 V.

$$c_{BLB}\frac{dV_{in2}}{dt}=\frac{V_{in1}-V_{in2}}{R_{VC}}+\frac{V'_{DD}-V_{in2}}{R_{in2}}=+ve \tag{6}$$

$$c_{BLB}\frac{dV_{in2}}{dt}=\frac{V_{in1}-V_{in2}}{R_{VC}}+\frac{V'_{gnd}-V_{in2}}{R_{in2}}=-ve \tag{7}$$

$$c_{BL}\frac{dV_{in1}}{dt}=\frac{V_{in2}-V_{in1}}{R_{VC}}+\frac{V'_{DD}-V_{in1}}{R_{in1}}=+ve \tag{8}$$

$$c_{BL}\frac{dV_{in1}}{dt}=\frac{V_{in2}-V_{in1}}{R_{VC}}+\frac{V'_{gnd}-V_{in1}}{R_{in1}}=-ve \tag{9}$$

$$c_{BLB}\frac{dV_{f2}}{dt}=\frac{V_{f1}-V_{f2}}{R_{mem}}+\frac{V'_{DD}-V_{f2}}{R_{f2}}=\pm ve \tag{10}$$

$$c_{BLB}\frac{dV_{f2}}{dt}=\frac{V_{f1}-V_{f2}}{R_{mem}}+\frac{V'_{gnd}-V_{f2}}{R_{f2}}=-ve \tag{11}$$

$$c_{BL}\frac{dV_{f1}}{dt}=\frac{V_{f2}-V_{f1}}{R_{mem}}+\frac{V'_{DD}-V_{f1}}{R_{f1}}=+ve \tag{12}$$

$$c_{BL}\frac{dV_{f1}}{dt}=\frac{V_{f2}-V_{f1}}{R_{mem}}+\frac{V'_{gnd}-V_{f1}}{R_{f1}}=\pm ve \tag{13}$$

$$\frac{dx}{dt}=\left(1-x^2\right)^{\alpha_p}\cdot\left(1-(2x-1)^{s_p}\right)\times \sinh\left(c_p\left(V_{f2}-V_{f1}\right)\right)=+ve \tag{14}$$

$$\frac{dt}{dt}=x(1-x)\exp(-\alpha_n x)\cdot\sinh\left(c_n\left(V_{f2}-V_{f1}\right)\right)=-ve \tag{15}$$

Moreover, Fig. 11 shows the relation-curves between the voltage-

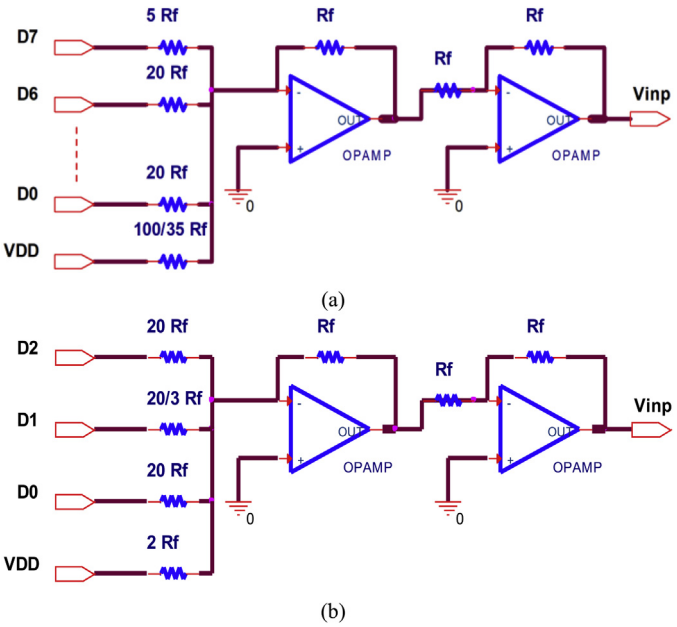

Fig. 12. The summing amplifier (second stage of DAC) for V_{DD} of 2 V (a) for the model in Ref. [36] (b) for the TEAM model [37]. W/L ratio for the PMOS is 4/0.13, and it is 2/0.13 for the NMOS transistors.

controlled resistance *VCR* and the programmed memristance $R_{mem\text{-}p}$ against the applied input V_{inp} which controls *VCR*. From Figs. 10 and 11, non-overlapping states should be selected to program the memristor.

In Fig. 11, the programmed states is corresponding to an input voltage range of 0.6–2.0 V with a space of 0.1 V to facilitate the design of the DAC. Smaller values of V_{inp} is used to program larger memristance, and hence the difference between the complementary voltage V_{in1} and V_{in2} is large and they need more time to be twisted giving the memristor a chance to change with a larger tolerance. Consequently, for V_{inp} lower than 1.00 V, the margin of 0.1 V may be not enough to provide non-overlapping states, therefore V_{inp} of lower than 1.00 V should not be used to program a state.

The DAC uses two stages of operations, the first one is to convert N input digits to 2^N states in a digital form, and hence N to $2^N{-}1$ decoder is required. Then, the 2^N states is then converted to the required values of V_{inp} using a summing amplifier as shown in Fig. 12 for both memristor models in Refs. [36,37].

3.2. A readout scheme

To test the proposed write system, it is utilized in a ReRAM system, a 4 × 4 memory system is proposed as shown in Fig. 13. Write or read circuit is selected by Tune or Read Select signals. The selected circuit is connected to the two bit-lines which then are connected to the memristor memory element selected by Read Access (RA) signal.

Many read circuits are provided in literature [17,35,41], and any one of them is useful, however the one provided in Ref. [35] is utilized to test the circuit.

Figs. 14 and 15 show the pre-read circuit schematic and the readout block diagram respectively. The memory cell is connected to the bit-lines and two reading memristors R_{r1} and R_{r2}. This connection provides a voltage divider which allows the stored memristance state to assign the bit-lines' voltages. An analog to digital converter is used to convert the voltage of BL or BLB to a digital output. The read access voltage V_{ra} is applied to start the read process. V_r is selected to be V_{DD}, and BLB is connected to an ADC's input.

The memristors (R_{f1}, R_{f2}, R_{in1}, R_{in2}, R_{r1} and R_{r2}) are implemented using on-chip memristors to be fabricated along with the memristors stack.

The values of reading memristances R_{r1} and R_{r2} are selected to be equal to R_{f1} and R_{f2} respectively, then BL and BLB lines attain same voltages as V_{f1} and V_{f2} nodes. The ADC consists of two stages; the

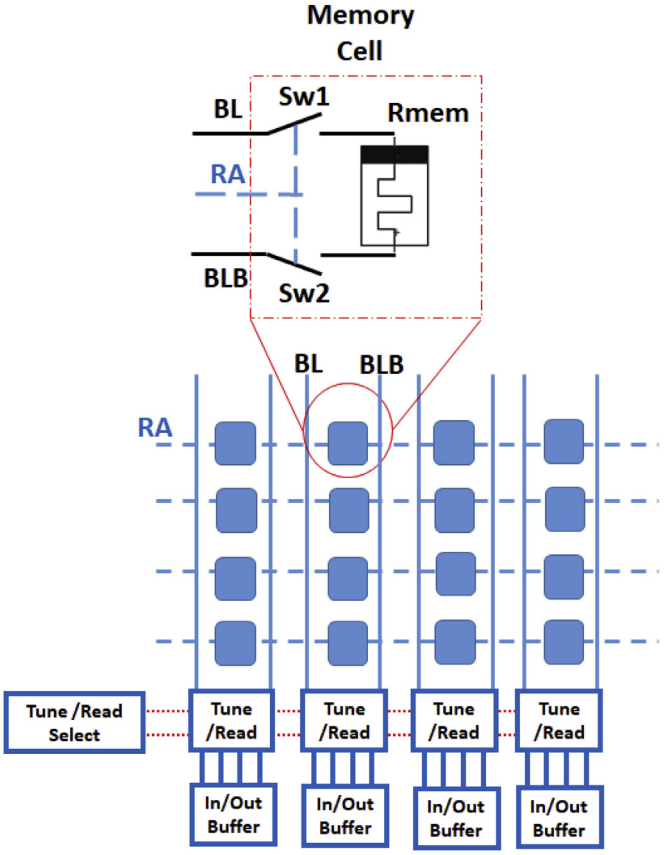

Fig. 13. ReRAM read/write System.

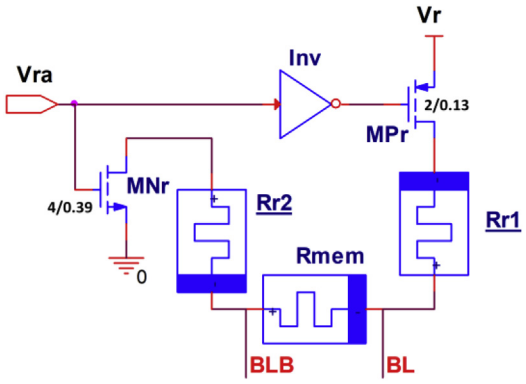

Fig. 14. The pre-read circuit schemtic

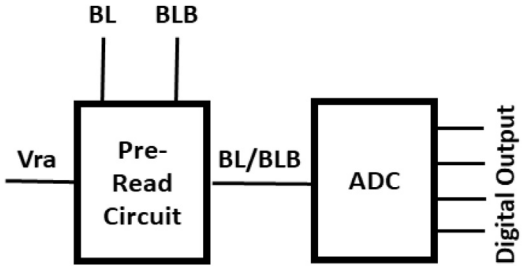

Fig. 15. The readout block diagram.

Table 3
Representation of stored states.

NO.	V_{inp}	Inputs of DAC or Outputs of ADC (Q_0 …. Q_{N-1})		Input of Priority Encoder or Output of Comparing Stage (D_0 …. D_M)		VCR (KΩ)	VCR (KΩ)	$R_{mem\text{-}p}$ (KΩ)	$R_{mem\text{-}p}$ (KΩ)
Model		[36]	[37]	[36]	[37]	[36]	[37]	[36]	[37]
1	2.0					0.371	0.800	00.750	00.750
2	1.8	111		1111111		0.623	1.380	*1.0520*	00.750
3	1.7					0.993	2.293	1.3012	00.750
4	1.6					1.869	6.250	2.1831	00.750
5	1.5	110	11	1111110	111	3.456	017.0	*4.0739*	*00.760*
6	1.4	101	10	1111100	110	6.033	040.0	*6.6810*	*0095.0*
7	1.3	100		1111000		10.2	115.0	*11.850*	321.27
8	1.2	011		1110000		17.04	163.0	*17.479*	262.64
9	1.1	010	01	1100000	100	28.53	231.0	*25.011*	*0878.7*
10	1.0		00		000	48.25	302.0	47.749	*3000.0*
11	0.9	001		1000000		82.69	395.0	*81.522*	3300.0
12	0.8					143.9	740.4	132.22	3300.0
13	0.7	000		0000000		254.8	668.9	*236.23*	3300.0
14	0.6					849.4	968.4	3300.0	3300.0

Table 4
Memristor Model Parameters and the Values of the feedback and input memristances.

The Model in Ref. [36]	$R_{on} = 750$	$R_{off} = 3.3e6$	$\varepsilon = 1e{-}9$
	$A_p = 8$	$A_n = 9.2864e3{-}7$	$\alpha_p = 1$
	$\alpha_n = -16.3$	$b_p = 0.35$	$b_n = 5.4$
	$c_p = 1$	$c_n = 1.5$	$s_p = 250$
TEAM Model [37]	$R_{on} = 750$	$R_{off} = 3.3e6$	
	$A_{on} = -2e{-}6$	$A_{off} = 2e{-}8$	$\alpha_{on} = 2$
	$\alpha_{off} = 2$	$x_{on} = 0.0$	$x_{off} = 3e{-}9$
	$i_{on} = 20e\text{-}9$	$i_{off} = 20e{-}9$	$a_{on} = 1.8e{-}9$
	$a_{off} = 1.2e{-}9$	$x_c = 1.07e{-}9$	
Feedback and Input Memristances	$R_{f1} = R_f = 3e5$	$R_{in1} = R_{in} = 2e5$	$R_{r1} = 3e5$
	$R_{f2} = R_f = 3e5$	$R_{in2} = R_{in} = 2e5$	$R_{r2} = 3e5$

comparator stage and a priority encoder part. The comparing stage is implemented as this used in Ref. [35].

Maximum of four different memristive states (2 bits) are distinguished by the provided readout scheme using TEAM while a maximum of eight states (3 bits) are distinguished using the model in Ref. [36] and they are selected according to Table 3. Finally, the logic functions of N to ($M = 2^N - 1$) decoder and those of the priority encoder are represented by (16) and (17) respectively, where D_{in0} through D_{in2} are the digital inputs of 3–8 decoder (DAC), and D_{0_out} through D_{6_out} are the analog outputs of the decoder, while D_{0_out} through D_{6_in} are the analog inputs of 8 to 3 priority encoder (a part of the ADC) and D_{out0} through D_{out2} are the digital output of the priority encoder (ADC).

$$D_{0\_out} = D_{in0} + D_{in1} + D_{in2}, D_{1\_out} = D_{in0} + D_{in1}, \tag{16}$$

$$D_{out0} = \overline{D_{6\_in}}(\overline{D_{4\_in}D_{2\_in}}D_{1\_in} + \overline{D_{4\_in}}D_{3\_in} + D_{5\_in}) + D_{7\_in}, \tag{17}$$

The circuit works fine using the model in Ref. [36] and the TEAM model with parameters provided below in Table 4. The two utilized models have two completely different window function formulas. The first model is easily configured to be highly asymmetric unlike the TEAM model which has two similar window function formulas which make it hard for the TEAM model to mimic the same state derivative provided by the first model. Therefore, using of TEAM model shows more deviations in the values of the memristance $R_{mem\text{-}p}$ from the corresponding VCR than the first model as shown in Figs. 10 and 11. The states selected to be programmed using the model in Ref. [36] and the TEAM model are shown in Table 3 with a maximum tolerance of −107.83 kΩ at a memristance of 236.2 KΩ using the model in Ref. [36] and −60 kΩ at 321 KΩ using the TEAM model. Furthermore, using the model in Ref. [36], an overlap is observed between the states at V_{inp} of 0.8 and 0.9 V, i.e., one of them should not be selected as a state.

It is worth noting that the feedback and the input memristors shown in Figs. 2 and 4 are connected in order to mitigate their switching while the main memristor device is being programmed. Using the model in Ref. [36] and if the parameters b_p and b_n have non-zero values, those memristors are connected to be under ON switching operation, whereas if b_p and b_n have zero values, those memristors are connected to be under OFF switching operation. Furthermore, using the TEAM model, the memristors are connected to be under OFF switching operation so that their memristances are lightly deviated from their initial values.

A comparison is carried out among the proposed circuit and other circuits provided in the literature [7,29] in terms of multi-bit states that

Table 5
Comparison among different write/read circuits.

Terms of Comparison	[29]	[7]	Proposed Circuit
Multi-bit support by original paper	Yes (up to 2 bits)	No (1 bit)	Yes (up to 3 bits)
Area determined by number of used transistors, diodes, capacitors and resistors for one cell	1 Memristor, 3 Resistors, 1 Capacitor, 1 Diode, 24 MOSFETs	2 Memristors, 1 Diode, 6 MOSFETs	9 Memristors, 16 MOSFETs, 2 Capacitors
Sources for write	DC signal	DC signal	DC signal
Sources for read	No read scheme is provided	DC signal	DC signal
Average Write/Read Delay per bit (for eight selected states)	6.64 s/No read scheme is provided	27.5 s/29 ns	266.5 ms (245 ms for the best case, 319 ms for the worst case)/ 9.5 ns (7.26 ns for the best case, 11.64 ns for the worst case)
Average Write/Read Power per bit (for eight selected states)	17 mW/No read scheme is provided	84.62 mW/2.94 μW	1.88 mW (1.86 mW for the best case, 1.89 mW for the worst case)/0.916 μW (0.9 μW for the best case, 0.949 μW for the worst case)
Power-Delay Product per bit	112.8 mJ	2.33 mJ/85.3 fJ	0.501 mJ/ 8.7 fJ
Used in a memory stack by original paper	No (Neither access transistors are used nor read scheme is provided)	Yes	Yes

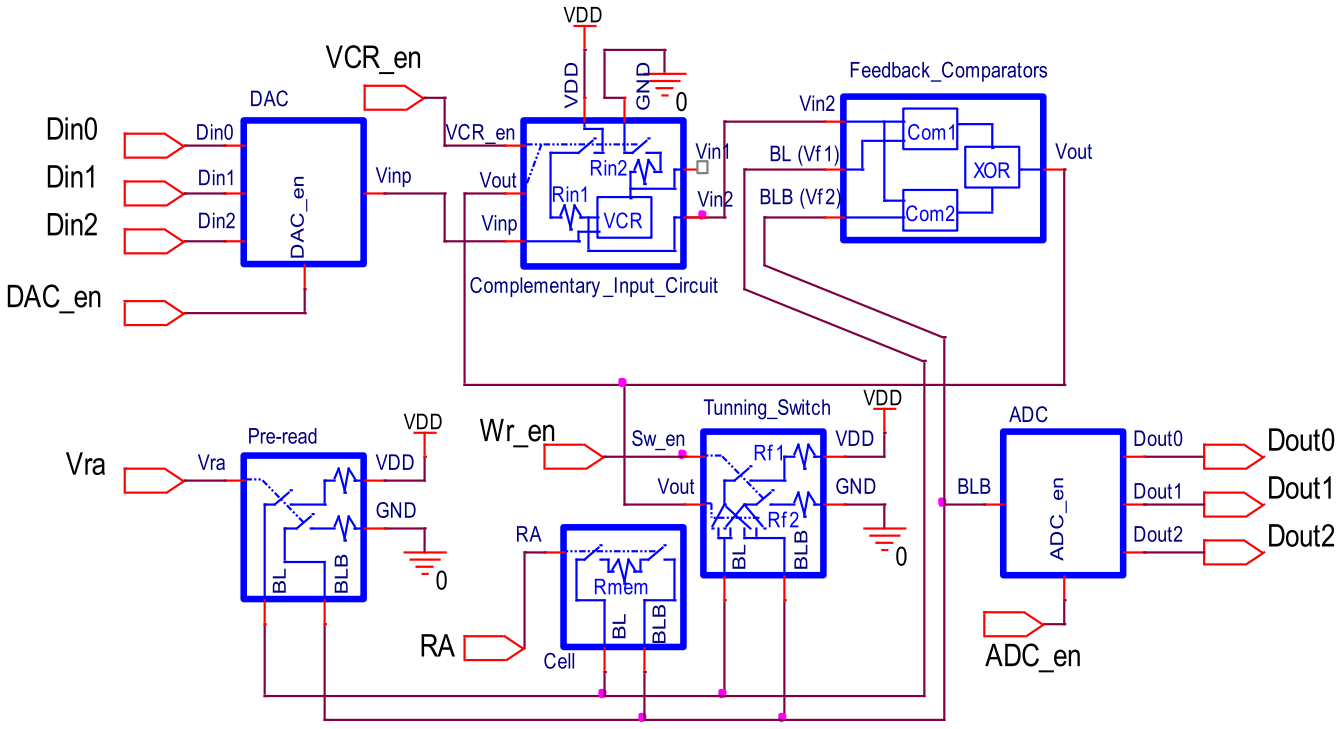

Fig. 16. The complete design of the provided write/read system with a total of seven building blocks (DAC, Complementary Input Circuit, Feedback Comparators, Tuning Switch, Pre-read, ADC and Memristor Cell), and 29 analog and digital signals (DAC_en, SW_en, VCR_en, Din0, Din1, Din2, D0_ out, D1_ out, D2_ out, D3_ out, D4_ out, D5_in, D6_ out, Vinp, Vout, Vcom1, Vcom2, Vf1 (BL), Vf2 (BLB), Vin1, Vin2, Vra, ADC_en, D0_in, D1_ in, D2_ in, D3_ in, D4_ in, D5_ in, D6_ in, Dout0, Dout1 and Dout2; some signals not shown) and four resistance parameters (Rf, Rin, VCR, Rmem0). The first block is a DAC with 3 digital inputs of a prefix Din and an enable signal DAC_en. The DAC provides V_{inp} as an input to the next block; Complementary Input Circuit, which is more illustrated in Fig. 4. This circuit sets the value of the VCR with the help of two extra signals; VCR_en and V_{out}. The third stage provides V_{out} according to comparisons between the feedback voltages Vf1 and Vf2 and one of the complementary input voltages (V_{in2}) provided by the former stage. A tuning switch circuit with a write-enable signal (Wr_en) connects the feedback resistors R_{f1} and R_{f2} according to the provided V_{out} to provide the values of V_{f1} (BL) and V_{f2} (BLB). The schematic of this stage is illustrated in Fig. 2.The pre-read circuit in Fig. 14 and the ADC comprise two other blocks for which V_{ra} and ADC_en are the enable signals for them respectively. The last block is the memristor cell with row access signal (RA). Switches in all blocks are shown as ideal switches for simplicity, and they are implemented using MOSFETs in the simulated schematics. The drawings inside the blocks are just to clarify the role of each block. and it gives a quick note to its internal components.

can be supported, area, average power, delay and power-delay product. The proposed circuit shows good results as compared to others as shown in Table 5.

If the feedback voltages V_{f1} and V_{f2} are deviated from the input voltages V_{in1} and V_{in2}, longer time is spent or more power is consumed to tune the memristor to a specific state, and there are two corner cases. The tolerances of the feedback and the input resistors are the cause of such cases, therefore their effect should be considered. The first corner case has average errors of 2.63%, −0.54% and 2.75% in the write memristances, power and delay for 20% change in the feedback resistances R_{f1} and R_{f2} along with a −20% change in the input resistances R_{in1} and R_{in2}. The second corner case has average errors of 1.21%, −2.1% and 30.4% in the write memristances, power and delay respectively for −20% change in the feedback resistances R_{f1} and R_{f2} along with a 20% change in the input resistances R_{in1} and R_{in2}. Both cases lead to higher power-delay products.

For the read process, +20% tolerance of the read memristances lead to −24.37 to −3.31 mV change in the read bit-line voltage, −0.01 to −0.016 μW change in the average read power, and 0.73–2.139 ns change in the read delay. Furthermore, −20% tolerance of the read memristances lead to 0.9–30.08 mV change in the read bit-line voltage, 0.013–0.033 μW change in the average read power, and 0.07 to −2.24 ns change in the read delay.

At the first tolerance case, two overlaps occur in the input voltage range of 0.7–0.9 V (three states), and only two non-overlapping states should be selected. For the second tolerance case, two overlaps in the input voltage range of 0.7–1 V (four states) takes place, and only two non-overlapping states should be selected. Thus, the tolerance issue excludes one more state.

Regarding the data converters, or course more power is consumed and longer delay time are spent. The DAC adds an average write power of 0.74 mW/bit and an average write delay (conversion time) of 33.7 ps/bit with a resolution of 50 mV, whereas the ADC adds an average read power of 4.67 mW/bit and an average read delay of 6.34 ns/bit.

3.3. Timing analysis

The write operation should be subject to constraints on time duration during which the write signals are applied. Specific time duration should be provided such that the write circuit adopts full switching between the extreme memristances R_{ON} and R_{OFF}. Since the OFF switching is slower than the ON switching, the OFF switching determines the time length of the input voltage V_{inp} during the write process. Starting from (3), (18) is obtained, where T is the maximum time duration require for proper writing, and since $v(t)$ equals the difference between V_{f1} and V_{f2}, (18) is modified to (19). In order to evaluate the value of T, the left hand integral of (19) is numerically calculated at the worst case-value of $R_{MEM} = . R_{ON}$, and it gives a range from 1.3 s to 2.4 h under 2 V and 10 mV of memristive voltage respectively. The states reached using very low memristive voltages $v(t)$ should not be selected since they need longer tuning times.

$$\int_1^0 \frac{1}{f(x)} dx = \int_0^T g(v(t))dt \tag{18}$$

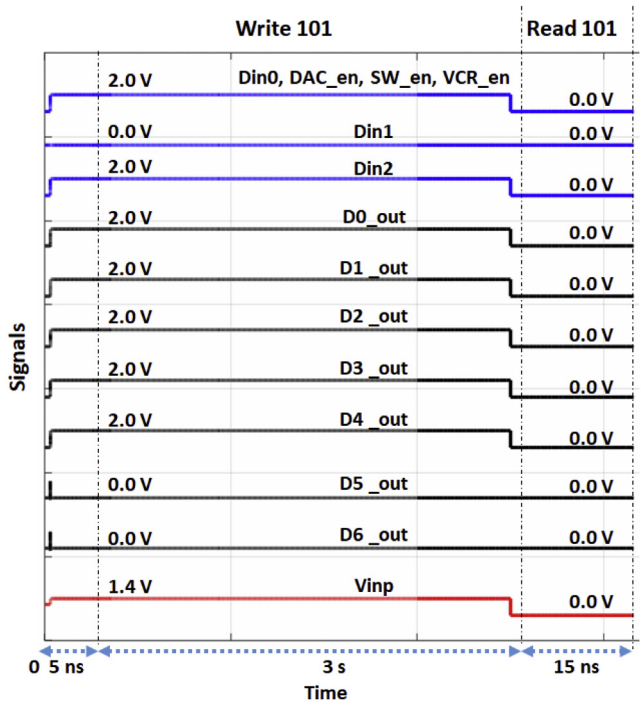

Fig. 17. The enable, input and output signals of the DAC (DAC_en, Din0, Din1, Din2, D0_out, D1_ out, D2_ out, D3_ out, D4_ out, D5_ out, D6_ out and Vinp respectively), and the enable signals of the Tuning Switch and VCR blocks (SW_en and VCR_en respectively).

$$\int_{1}^{0} \frac{1}{f(x)} dx = A_n \sinh\left(c_n \left| V_{f1} - V_{f2} \right|\right) T \tag{19}$$

All of the simulations are carried out using Cadence Virtuoso. The parameters of the used memristor's models and the values of the feedback and input memristances are represented in Table 4.

Fig. 16 shows the complete design of the provided write/read system

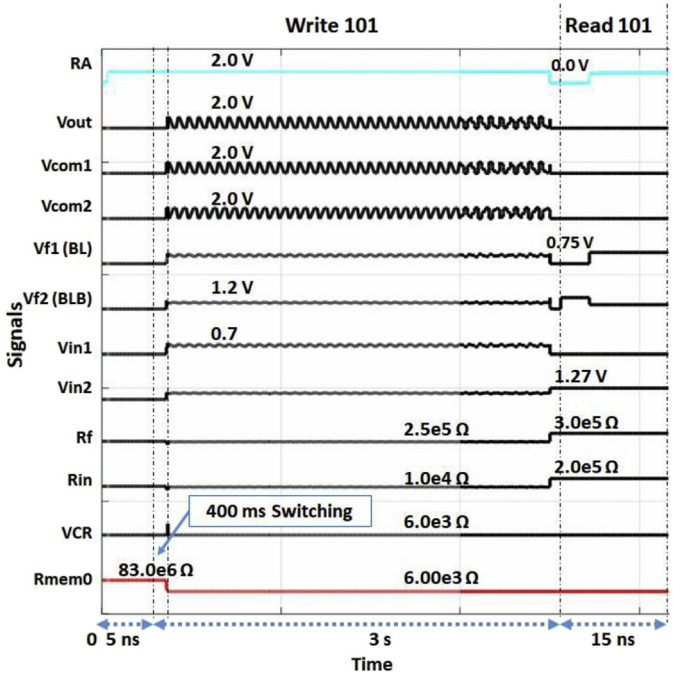

Fig. 18. The memory row-access signal (RA), the values of voltage nodes in the complementary-input circuit and the feedback comparing stage (Vout, Vin1, Vin2, Vcom1, Vcom2, Vf1, Vf2), and the values of four resistance parameters (Rf, Rin, VCR and Rmem0 = $Roff \cdot (1-x) - x \cdot Ron$).

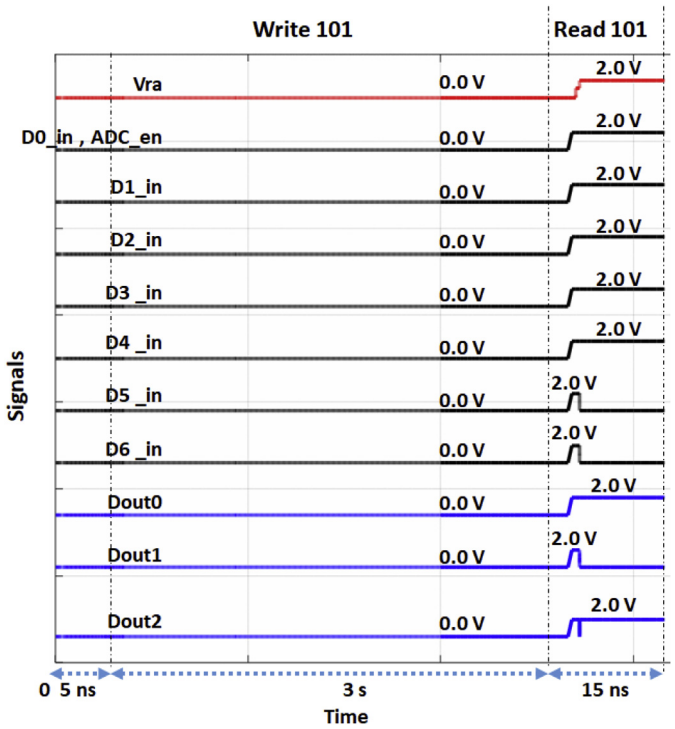

Fig. 19. The enable, input and output signals of the ADC (ADC_en, D0_in, D1_ in, D2_ in, D3_ in, D4_ in, D5_ in, D6_ in, Dout0, Dout1 and Dout2 respectively), and the enable signal of the Pre-read block (Vra).

to write and read three bits (101), with a total of 29 analog and digital signals and four resistance parameters.

The whole system comprises seven building blocks (stages). The first block is a DAC with three digital inputs of a prefix Din and an enable signal DAC_en. For illustration, the DAC inputs (Din0, Din1 and Din2) are set as 101, and it provides V_{inp} of 1.4 V as an input to the Complementary Input Circuit which is illustrated in Fig. 4. The analog outputs of the DAC (D0_out, D1_out, D2_out, D3_out, D4_out, D5_out, D6_out) are driven to be 1111100. The Complementary Input Circuit sets the value of the VCR as 6 KΩ with the help of VCR_en and V_{out}.

The third stage provides V_{out} which alternates between 0 V and 2 V according to comparisons between the feedback voltages V_{f1} and V_{f2} and one of the complementary input voltages ($V_{in2} = 1.27$ V) provided by the former stage. A tuning switch circuit with a write-enable signal (Wr_en) connects the feedback memristors R_{f1} and R_{f2}; which varies between 250 and 300 KΩ, according to the provided V_{out} to set V_{f1} (BL) and V_{f2} (BLB) as 1.2 V and 0.75 V respectively, and hence the memristor takes about 400 ms to be programmed to 6.8 KΩ.

The schematic of this stage is illustrated in Fig. 2. The pre-read circuit in Fig. 14 and the ADC comprise two other blocks for which V_{ra} and ADC_en are the enable signals for them respectively. The last block is the memristor cell with row access signal (RA). The enable signals connects the corresponding block to V_{DD} and the ground or connect the to the bit-lines. The DAC inputs and the ADC outputs comprises the digital interfaces of the circuit.

The curves of all signals and resistances vs. time t are shown in Figs. 17–19. The write process takes place from 0 to 3 s, and then the read process takes place in 15 ns In the first 5 ns, the values of V_{inp} and VCR are prepared by enabling DAC_en, SW_en and VCR_en and setting the digital inputs (3 bits) to 101 before the switching takes place. For the read phase, Vra and RA are activated forcing V_{f2} to be higher than V_{f1} as 0.75 V and 1.2 V respectively. The feedback voltages drive the analog inputs of the ADC (D0_in, D1_in, D2_in, D3_in, D4_in, D5_in, D6_in) to be 1111100, and the digital output of the complete circuit/ADC (Dout0, Dout1 and Dout2) to 101.

Endurance of the memristor is an important physical property that indicates the shift in the memristance levels after many times of switching cycles [42,43]. In order to address the device endurance, experimental tests were performed using experimental tests for TiO_2 and many different memristors [42–46]. The TiO_2 memristor shows endurance of about 10^{10} [42], and still needs to be tested for other variability issues like mechanical endurance [47] as the research about this aspect is under development.

4. Conclusion

A write and read circuits for memristors with digital input and output interfaces have been presented. These circuits have been simulated using the industrial hardware-calibrated TSMC 130 nm CMOS technology models.

The presented write circuit has the ability to tune the memristor to any state starting from any initial state using only positive DC input voltage. Parasitic capacitances are associated to the different nodes of the write circuit giving rise to the delay of the signals during the switching operations. The write circuit compares the feedback voltages against closely chargeable and dischargeable input levels. The effect of the bit-line parasitic capacitances in the memory system has been analysed using different memristor models. The final memristance states are drawn against the input voltage.

A readout schematic has been presented and simulation results have shown that the maximum number of states which are programmed into the presented highly asymmetric memristor device is four. These states have been selected carefully in order for the read circuit to distinguish among them. Furthermore, the effect of the tolerances of the feedback, the input, and the read resistors are tested with the proposed circuit. The results showed low errors in the values of the written memristances.

A comparison was conducted against some circuits found in literature and the proposed circuits showed good results in terms of power and delay values.

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