DESIGN OF MICROSCALE PIEZOELECTRIC ENERGY HARVESTING SYSTEM

By

Ehab Belal Abd El Hamid Ibrahim

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2019

DESIGN OF MICROSCALE PIEZOELECTRIC ENERGY HARVESTING SYSTEM

By

Ehab Belal Abd El Hamid Ibrahim

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

Under the Supervision of

Prof. Amin Nassar
Professor of Electronics

.....

Department of Electronics
Faculty of Engineering, Cairo University

Prof. Mohamed Sameh Said
Professor of Electronics

.....

Department of Electronics
Faculty of Engineering, Cairo University

Dr. Hassan Mostafa Hassan
Associate Professor of Electronics

.....

Department of Electronics
Faculty of Engineering, Cairo University

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2019

DESIGN OF MICROSCALE PIEZOELECTRIC ENERGY HARVESTING SYSTEM

By

Ehab Belal Abd El Hamid Ibrahim

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

Approved by the
Examining Committee

Prof. Amin Mohammed Nassar **Thesis Main Advisor**
Professor of Electronics, Faculty of Engineering, Cairo University

_____
Dr. Hassan Mostafa Hassan **Advisor**
Associate Professor of Electronics, Faculty of Engineering, Cairo University

_____
Prof. Ahmed Nader Mohieldin **Internal Examiner**
Professor of Electronics, Faculty of Engineering, Cairo University

_____
Prof. Elsayed Mostafa Saad **External Examiner**
Professor of Electronics, Faculty of Engineering, Helwan University

_____

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2019

Engineer's Name:	Ehab Belal Abd El Hamed Ibrahim
Date of Birth:	8/4/1987
Nationality:	Egyptian
E-mail:	ehab.belal@gmail.com
Phone:	+2001118715278
Address:	Giza
Registration Date:	1/3/2013
Awarding Date:	.. /../2019
Degree:	Master of Science
Department:	Electronics and Communications Engineering
	.
Supervisors:	
	Prof. Amin Mohammed Nassar
	Dr. Hassan Mostafa Hassan
Examiners:	
	Prof. Amin Mohammed Nassar Thesis Main Advisor
	Professor of Electronics, Faculty of Engineering, Cairo University
	Dr. Hassan Mostafa Hassan Advisor
	Associate Professor of Electronics, Faculty of Engineering, Cairo University
	Prof. Ahmed Nader Internal Examiner
	Professor of Electronics, Faculty of Engineering, Cairo University
	Prof. Elsayed Mostafa Saad External Examiner
	Professor of Electronics, Faculty of Engineering, Helwan University

Title of Thesis:

Design of Microscale piezoelectric Energy Harvesting System

Key Words:

AC/DC converter; Charge pump DC/DC; Digital Control Oscillator DCO; The maximum power point tracing MPPT.

Summary:

Using the energy harvested from the piezoelectric transducer to power on the electronic circuits in biomedical applications. The energy harvested is rectified by using the AC/DC converter with power efficiency 83% and the voltage conversion ratio reaches 300%. The DC/DC converter is used to match the output voltage of the AC/DC converter with the voltage of super capacitor 1.8V. The desired switching frequency range from 57KHz to 132KHz is generated using the voltage control oscillator that used a lookup table to guarantee that the frequency generated corresponding to the maximum power point. The output voltage of the AC/DC is digitalized to N-bits by using the successive approximation register analog to digital converter to build the lookup table.

Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute.
I further declare that I have appropriately acknowledged all sources used and have cited them in the references Section.

Name: Ehab Belal Abd El Hamed Ibrahim Date:

Dedicated

Dedicated to My Family.
For their endless love, support, and encouragement.

Acknowledgements

First, I would like to thank sincerely my thesis advisors Prof.Amin Mohammed Nassar and Dr. Hassan Mostafa for guiding me throughout the research work. They supported me with their great research experience. They are always eager to discuss any design problems. Their design decisions are very effective to deliver this quality of work. I would like to thank them also for discussing issues related to research directions, job decisions, and paper submission. This work would not have been possible without their assistance.

I wish to thank my parents for their endless support and patience. They spent a lot of effort to support me in finishing this work. I would like to thank my mother for her continuous praying for me and my sister for their massive support during the critical part of my life. Special thanks to my wife and my two sons for providing a perfectly stable environment and support at the most critical period of my life.

Table of Contents

List of Tables

List of Figures

Abbreviations

AC	Alternating Current
ADC	Analog-to-digital converters
DC	Direct current
DCO	Digital control oscillator
EOC	End of conversion
FGCCR	Fully gate cross-coupled rectifier
LDO	Low-dropout regulators
MPPT	Maximum Power Point Tracking
OV	Open Voltage
PGCCR	Partially gate cross-coupled rectifier
PV	Photovoltaic
RF	Radio Frequency
SAR	Successive approximation register
SC DC-DC	Switched-capacitor DC-DC
TEG	Thermoelectric generators

Symbols

C	Capacitance Farad
C_M	Mechanical stiffness Pascal
I	Current Ampere
K	Boltzmann constant
R	Resistance Ohm (Ω)
S	Seebeck coefficient V/K
T	Temperature Kelvin/Celsius (◦K/◦C)
V	Voltage Volt
η	Efficiency dimensionless

LIST OF PUBLICATIONS

1- Ehab Belal, Hassan Mostafa, and M. Sameh Said, "Comparison between active AC-DC converters for low power energy harvesting systems", International Conference on Microelectronics *(I*CM*)*, pp. 253-256, Dec. 2015.

2-EhabBelal, Hassan Mostafa, Yehea Ismail, and M. Sameh Said, "A voltage multiplying AC/DC converter for energy harvesting applications", International Conference on Microelectronics (ICM), pp. 229-232, 2016.

3-Ehab Belal, A. Nassar, and H. Mostafa, "Design of Microscale Piezoelectric Energy Harvesting System", IEEE International Mid-West Symposium on Circuits and Systems (MWSCAS 2019), pp.750-753 ,2019.

Abstract

The energy harvesting system aims to convert ambient energy, for example, mechanical, photovoltaic solar, thermal or radio frequency into electrical energy which can be stored in batteries. Ambient energy of thermoelectric generators (TEG), silicon-based micro-fuel and a single junction photovoltaic (PV) cells produces a dc power that can easily charge batteries without the need for AC/DC converter. Ambient energy of piezoelectric, electromagnet and RF produces AC power which needs AC/DC converter to be converted from ac power to dc power that can be easily stored by charging batteries.

The AC/DC converter used is based on active diode due to its efficiency of converting if compared with traditional diode. The AC/DC converter based on active diode has a low threshold voltage than the threshold voltage of the traditional diode. Therefore it has lower power losses and higher efficiency.

The DC/DC converter used to match the rectifying voltage with the voltage of super capacitor and the desired switching frequency is generated by the voltage control oscillator that used a lookup table to guarantee that the generated frequency corresponding to the maximum power point. The used DC/DC converter is the DC/DC charge pump because of its easy implementation, low electromagnetic induction and inductor less.

The control unit provides the desired switching frequency with enough capability to drive the charge pump power. The control unit consists of analog to digital converter and digital control oscillator. The analog to digital converter is used to convert the analog signal which is produced from the AC/DC converter to digital signal, this signal is converted by the digital control oscillator into the desired switching frequency needed for the switched capacitor charge pump. The analog to digital converter used is the successive approximately register because of its low latency, low power consumption, and small area. The input impedance of the DC/DC charge pump acts as a variable resistance that changes its value by changing the desired frequency, finding the relation between the dc input voltage and the frequency enables us to get the maximum power point tracking between the energy harvesting by piezoelectric that changes due to the vibration of piezoelectric transducer and voltage of batteries.

The contribution to this work is shown in several search domains. The first research is a comparison between different Active AC/DC converters, the comparison parameters are lower input voltage used, efficiency and area. The second research is the design of a new active AC/DC converter compared with recent researches. The third research is a design of an energy harvesting system using piezoelectric transducer and subcircuits compared with the recent researches using the same technique.

Chapter 1: Introduction

We will use the piezoelectric transducer for our energy harvesting system, AC/DC converter is used to convert AC power produced from the piezoelectric transducer to DC power. The charge pump DC/DC converter matches the output voltage of the AC/DC converter and batteries' voltage by reducing the higher voltage DC output from AC/DC converter to the lower voltage which needed to charge batteries. The analog signal produced by AC/DC is digitalized to a digital signal using successive approximation register SAR and the digital bits used as a control signal for the digital control oscillator that generates a clock with a specified frequency for each input signals. The DC/DC charge pump acts as variable resistance that changes its value by changing the desired frequency, finding the relation between the dc input voltage and the frequency enables us to get the maximum power point tracking between the energy harvesting by piezoelectric and batteries' voltage.

1.1System block overview

The energy harvesting system is shown in Figure 1.1. The piezoelectric transducer used as a transducer for our energy harvesting system. AC/DC converter is used to convert the ambient energy from piezoelectric to DC power. Successive approximation register analog to digital SAR ADC circuit is used to digitalize the analog signal to a digital signal. The digital control oscillator converts the digital signal to the desired switching frequency needed for the maximum power point tracker switched capacitor charge pump.

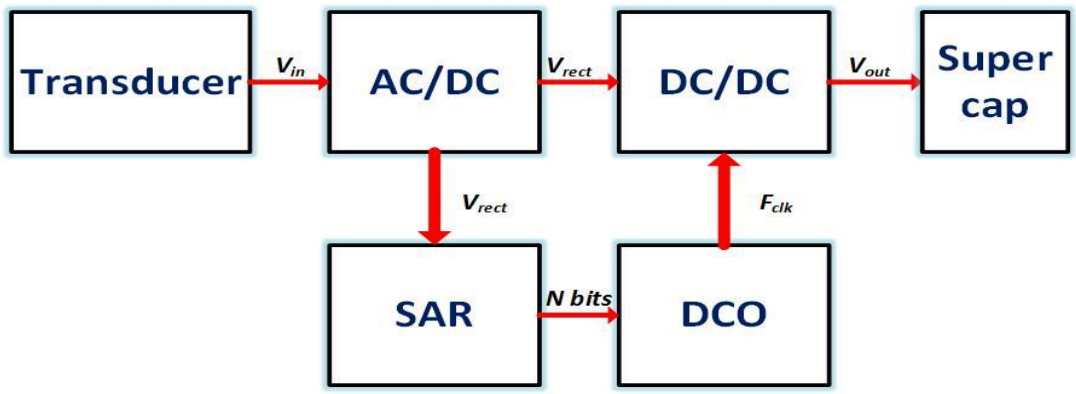

Figure 1.1: System block overview.

1.2 Thesis content

This thesis organized as follows: A detailed survey for the previous studies in Chapter 2. Chapter 3 provides a detailed explanation for the proposed circuit for the energy harvesting system. In conclusion, the main achievements are highlighted together with the future lines of this work in Chapter 4.

Chapter 2: Background and Literature Review

This chapter includes a detailed survey for the previous studying. Different transducer types can be classified based on their output. The transducer types generate AC power and DC power. Various AC/DC converter types will be presented using traditional diodes and types based on the active diode. The maximum power point tracking (MPPT) techniques will be presented. Various types of analog to digital converters and comparisons between them in terms of area, cost, and power.

2.1 Transducers

Different transducer types are used to gather ambient energy, for example, vibration, light, and heat. Table 2.1 shows different energy transducer power density. The power density is the ratio of the power over the volume W/cm^3. The highest power density is the solar transducer with 15mW/cm^3 while the lowest power density is a thermoelectric transducer with 40µW/cm$^{3.}$

Table 2.1: Transducers power density [1]

Transducer	**Power Density**
Solar (Outdoors)	15mW/cm^3
Solar (Indoor)	1mW/cm^3
Piezoelectric	300µW/cm^3
Vibration	116µW/cm^3
Thermoelectric	40µW/cm^3

1.1.1 Solar transducer

Solar Transducer (Photo-Voltaic (PV) cells) is the highest power density compared to other different transducers[2]. Figure 2.1 shows the solar transducer equivalent circuit and the characteristics of the solar transducer which shown in (current-voltage) curve and (power-voltage) curve. The solar transducer is represented as a current source in parallel with a diode and shunt resistor (R_p) the series resistor (R_s) is the silicon ohmic contacts. As the series resistor increased, the I_{sc} curve as shown will be at a constant voltage region. Conversely decreasing the series resistance will lead to being at the constant current region.

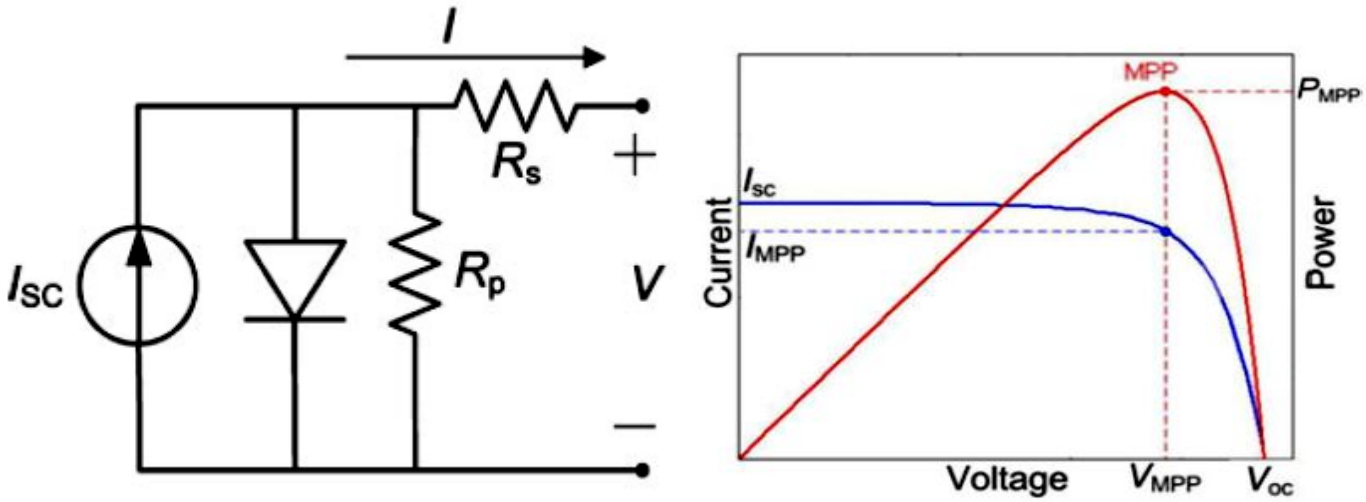

Figure 2.1: The solar transducer equivalent circuit. [2]

The solar Transducer relationship between current and voltage

$$I = I_{ph} - I_o\left(e^{\frac{q(V+IR_S)}{KTn_d}} - 1\right) - \frac{V + IR_S}{R_P} \qquad (2.1)$$

Where (I_{ph}) is the photo generated current, the saturation current (I_0) and the charge of the electron q and factor of the diode n_d that ranges from 1.2 to 1.8, the Boltzmann constant (K) and temperature in Kelvin (T).

1.1.2 Thermoelectric transducer

The thermoelectric transducer is also known as TEG (thermoelectric generator). TEG composed of multiple slices of p-type and n-type junctions connected as parallel in thermal and as series in electrical connection. Saving the surface area, the structure of TEG is aligned. The Seebeck effect will produce thermal energy [3] across the parallel slices, the free carriers moved from a high-temperature side to a low-temperature side, this motion will produce the current. The TEG is used at human-powered biomedical implants; as the thermal variance between a human body and air can easily generate electrical power.

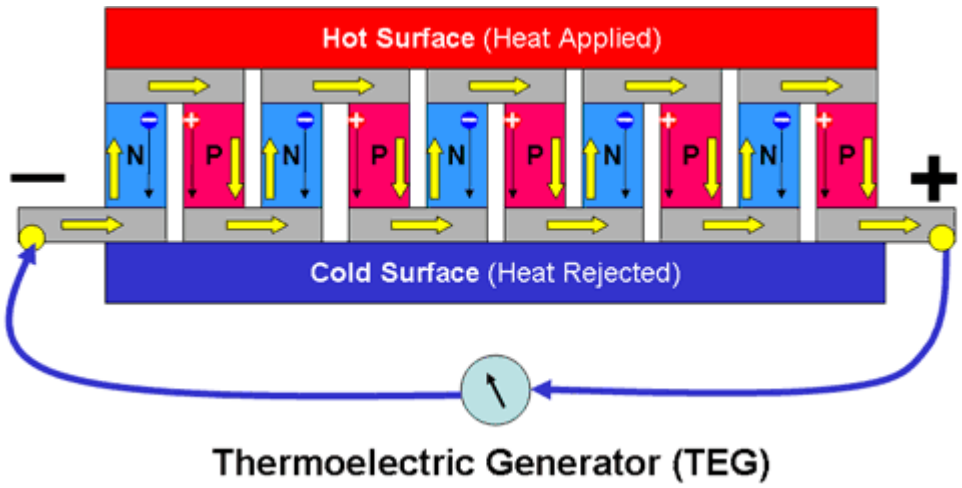

Figure 2.2 Thermoelectric transducer. [4].

The thermoelectric transducer model consists of a dc voltage source and a resistance in series [5- 6] as shown in Figure 2.3. Equation 2.2 shows the relation between V_T the open-circuit voltage and Seebeck coefficient S and ΔT is the temperature difference between the cold and hot sides of the thermoelectric transducer.

$$V_T = S\,\Delta T \qquad (2.2)$$

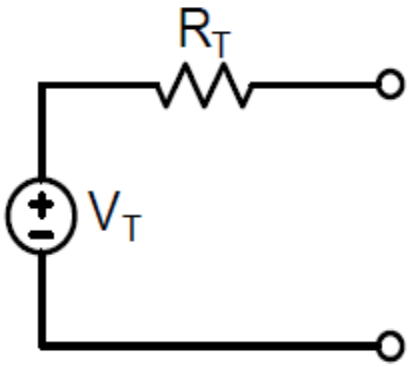

Figure 2.3 Thermoelectric transducer model. [5]

1.1.3 Piezoelectric transducer

The vibration of piezoelectric material made deformations that generate a strain and stress on it. A voltage change will be generated on the piezoelectric material terminals, Figure 2.4 presents the design of a piezoelectric transducer where a piezoelectric layer is attached to a cantilever beam and one side of it is fixed on a base. A voltage difference is generated when we apply an external vibration that leads to bending the piezoelectric layers. The mass is used to get the resonance frequency of the piezoelectric.

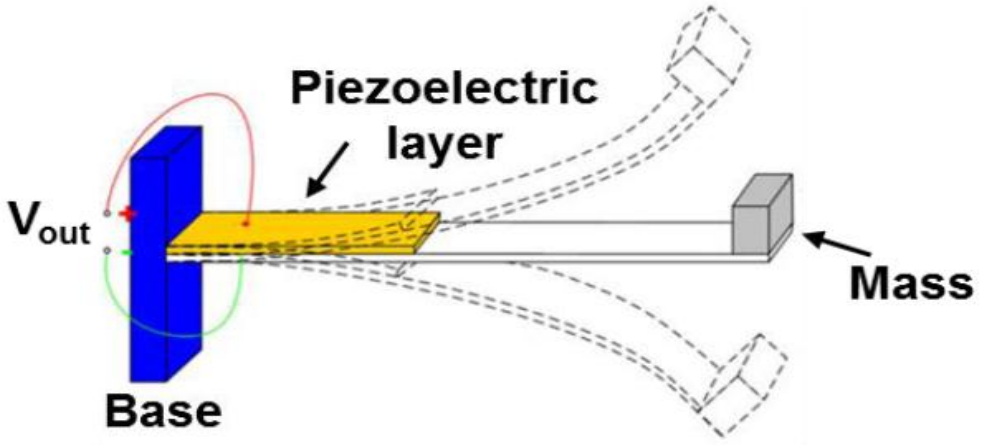

Figure 2.4 The piezoelectric transducer. [7]

The piezoelectric transducer equivalent circuit [8] can be modeled as a mechanical system besides an electrical system as shown in Figure 2.5 where L_M is the mechanical mass, C_M is the mechanical stiffness, R_M is the mechanical losses and C_P is the capacitance of the piezoelectric material. A transformer is used to convert the strain from the mechanical system to the current for the electrical system. Figure 2.6 shows the equivalent circuit of a piezoelectric transducer, where C_P is the capacitance of the piezoelectric material in parallel with a sinusoidal current source I_p and R_P is the resistance.

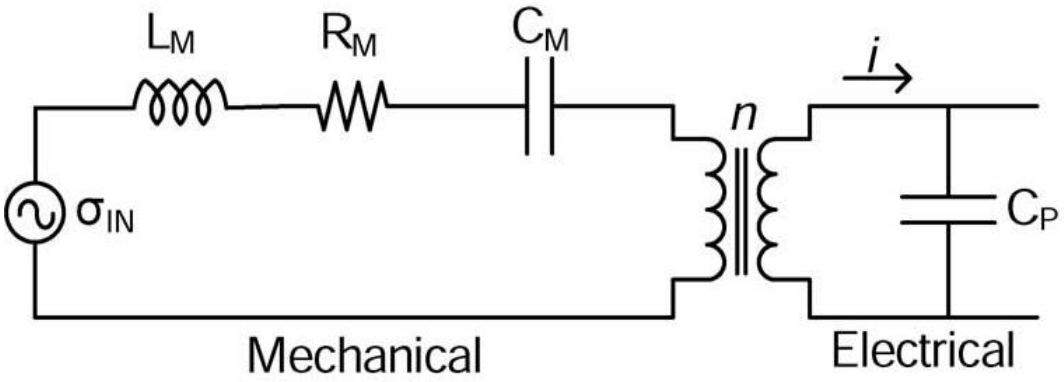

Figure 2.5 The piezoelectric transducer equivalent circuit. [8]

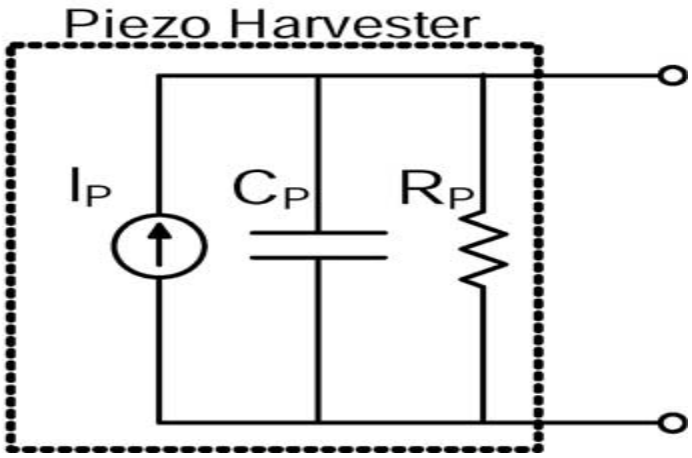

Figure 2.6 The piezoelectric transducer equivalent circuit. [8]

2.2 AC/DC rectifiers

The rectifiers play an important role in electrical energy. It is used to convert the AC power to DC power. Conventional bridge and gate cross-coupled rectifier topologies suffer from low power efficiency, especially when we use low AC input voltage due to the diode threshold voltage. Threshold cancellation techniques are used with the advanced passive rectifiers effectively reducing the MOS diode's threshold voltage.

2.2.1 AC/DC Conventional rectifier

2.2.1.1 AC/DC Half-wave

AC/DC half-wave rectifier passes half of the input AC signal towards the output, in either the negative or the positive cycles and blocks the other half. The conduction path depends on the rectification element polarity. The AC/DC half-wave rectifier used at biomedical implant designs by implemented a substrate or off-chip diodes [9]. The power efficiency of the AC/DC half-wave rectifier is not high due to the conduction path every half of the input cycle.

2.2.1.2 AC/DC full-wave

AC/DC full-wave rectifier as shown in Figure 2.7 converts the full wave cycle of AC input signal to a fixed DC output. In AC/DC full-wave [10], when the input voltage is higher than the output voltage, a conduction path delivers power to output through a diode while the other diode provides a return path to the ground. AC/DC full-wave rectifier compared to AC/DC half-wave rectifier has smaller output ripples, higher power efficiency, and higher reverse breakdown voltage. AC/DC full-wave, however, suffers from having two forward-bias voltage drops of cascaded diodes in each voltage cycle.

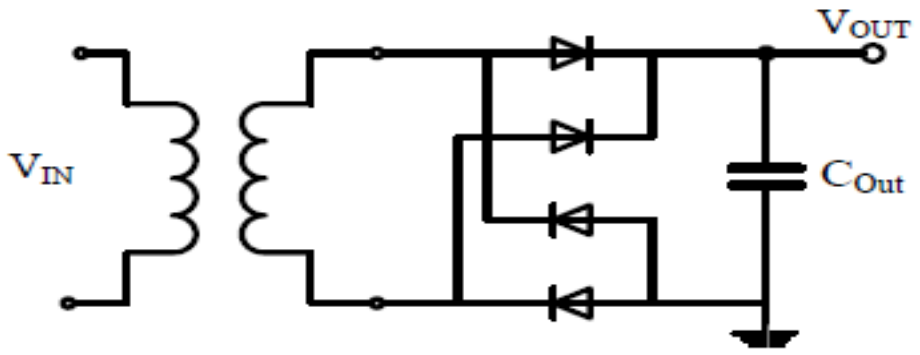

Figure 2.7 AC/DC full-wave. [10]

2.2.1.3 AC/DC switch only

AC/DC switch only [11] as shown in Figure 2.8, consists of a switch M_1 connected across the piezoelectric transducer, M1 switch is connected to AC/DC full-wave rectifier. When the switch is ON, the capacitor discharges immediately to the ground. Once the capacitor has been discharged, M_1 is turned OFF and AC/DC rectifier starts to conduct at

both half-cycles of the input signal. The waveform of the voltage and current related to the AC/DC Switch only is shown in Fig. 2.9. At every half-cycle, the switch is turned ON the capacitor discharges immediately. The current of the piezoelectric transducer charges up the capacitor from ground to the rectifier voltage plus twice the threshold voltage of diodes.

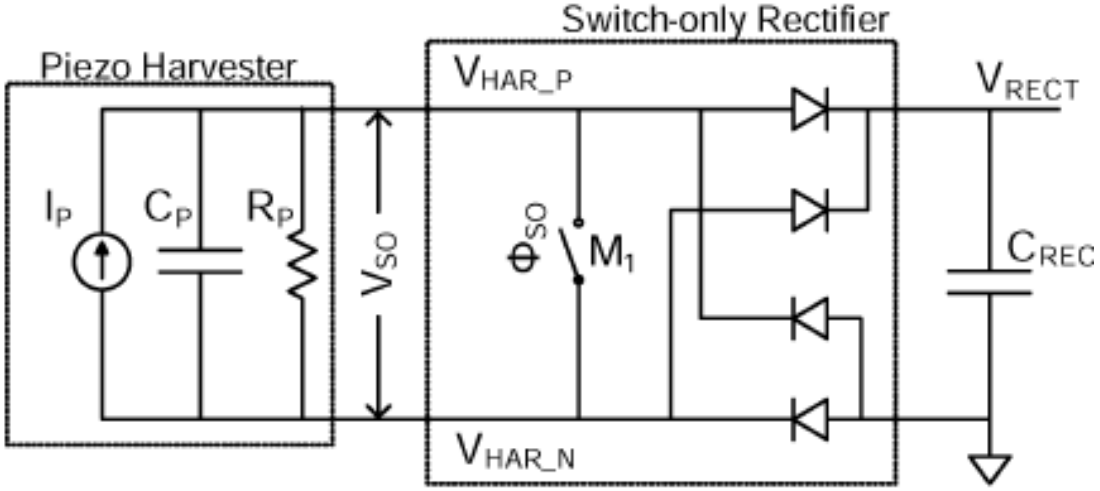

Figure 2.8 Switch only rectifier. [11]

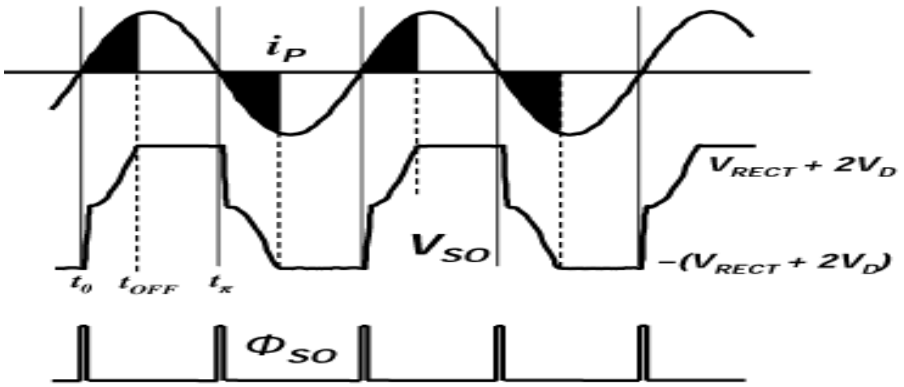

Figure 2.9 switch only rectifier waveform. [11]

2.2.1.4 AC/DC Bias-Flip

AC/DC switch only rectifier rectifies both half-cycles of the input voltage, but there is amount of charge lost due to charging the capacitor from ground to the rectifier voltage plus twice the threshold voltage of the diodes every half-cycle. The improvement of output power can be obtained if we minimize the charge lost. The AC/DC bias-flip rectifier [12] can improve the output power by using an inductor in series with the switch as shown in Figure 2.10. The waveform of voltage and current related to AC/DC bias-flip rectifier is shown in Fig. 2.11. At every half-cycle, the switch is turned ON making the inductor flip the voltage across the capacitor. When the inductor current reaches zero the switch is turned OFF.

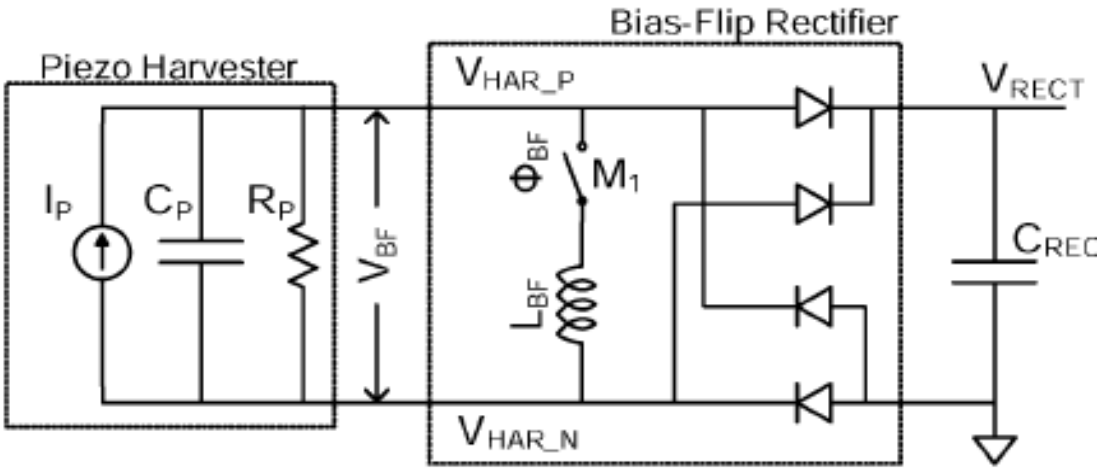

Figure 2.10 AC/DC bias-flip rectifier. [12]

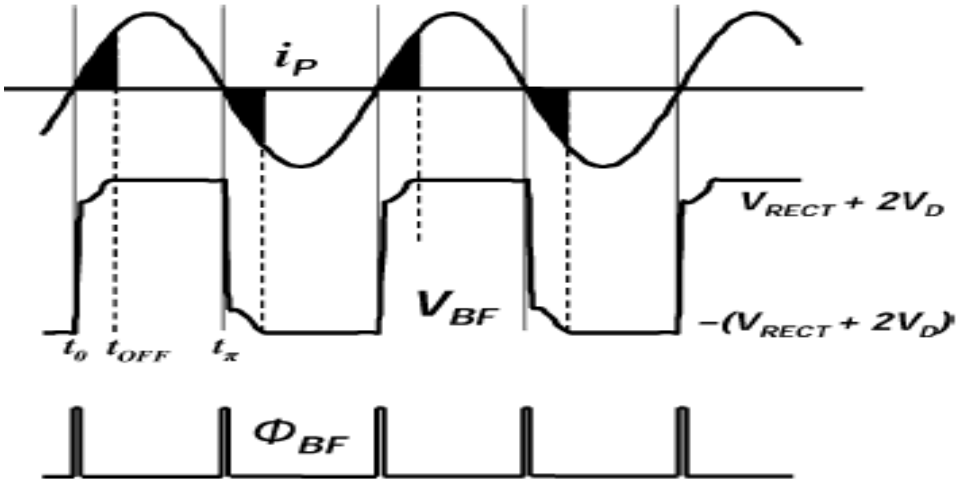

Figure 2.11 Waveform of bias flip rectifier. [12]

2.2.2 Advanced passive bridge rectifier

2.2.2.1 Partially gate cross-coupled

The partially gate cross-coupled rectifier (PGCCR) [13] consists of two gates cross-coupled rectifiers instead of the two diodes of the AC/DC full-wave as shown in Figure 2.12. To ensure that the positive side of the AC input will be connected to the output, the negative side will be connected to the ground. The PGCCR can provide us with voltage drop lower than the threshold voltage of traditional diode if there is sufficient flowing current and the size of transistors is properly designed. The overdrive voltage of pMOS in the bridge topology is much lower than nMOS in the gate cross-coupled topology. Moreover, nMOS devices have higher electron mobility than the pMOS counterparts. With these reasons, the gate cross-coupled circuit is smaller in size, has a lower turn-on voltage, and a smaller voltage drop over the standard bridge structure.

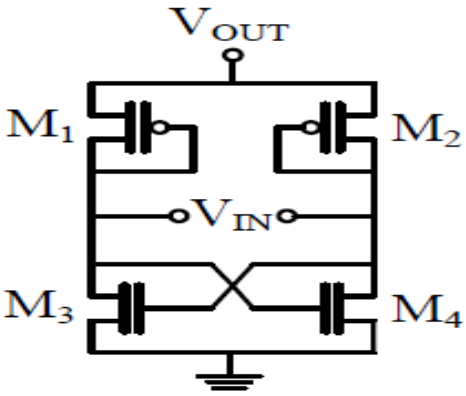

Figure 2.12 Gate cross coupled rectifier. [13]

2.2.2.2 Fully gate cross-coupled

In fully gate cross-coupled rectifier (FGCCR) the problem of threshold diode-connected is overcome [14] by cross-connected each pair of MOS switch as shown in Figure 2.13. There is no voltage drop as there is no diode-connected MOS transistor, only the voltage drop of the switches. The benefit of switches is the provision of the lowest resistance to enable high voltage swing and the higher output voltages and can work with low input voltage compared to the PGCCR, the on-resistance of the switch is changing by changing the transistor size that will effect on the circuit performance

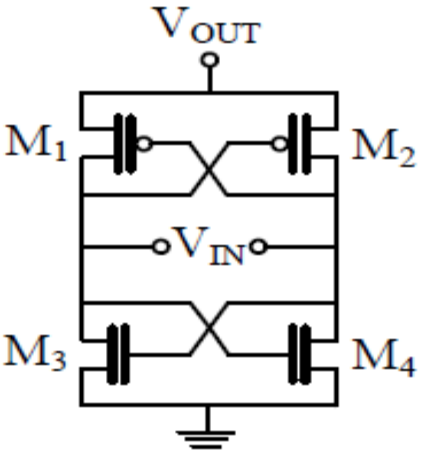

Figure 2.13 Fully gate cross-coupled. [14]

2.2.3 Active power AC/DC rectifier

Active AC/DC rectifiers control the conduction path by using switches, comparators, and possibly feedback to control the conduction path with little power loss and small voltage drop. Figure 2.14 shows an active power AC/DC rectifier. When the output voltage is smaller than the input voltage, the comparator output will be high and the main switch will turn on charging of the output load. Conversely, when the output voltage is higher than the input voltage, the comparator output will be low and the switch will turn OFF, disconnecting the

forward conduction path. Generally, active rectifier has high power efficiency and high output voltage compared to passive rectifiers [15].

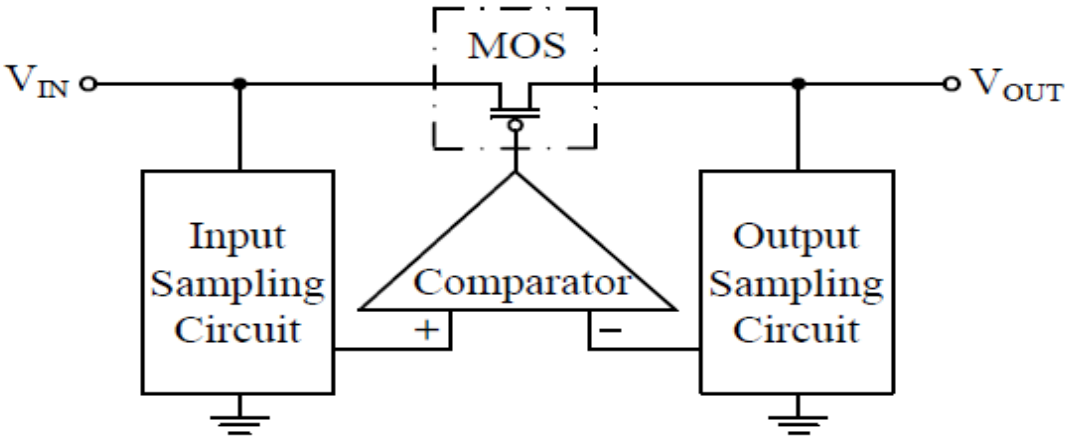

Figure 2.14 An active power AC/DC rectifier. [15]

The main building block of the active rectifier is the active diode that is used to achieve high performance. The active diode works as an ideal diode with negligible voltage drop and no reverse current in forwarding conduction path and due to quiescent current, there are static power losses. If this static power is high, it can overcome its benefits in reducing the voltage drop of the diode. An active diode consists of a switch and a comparator control conduction path. No additional start-up circuit is required due to the use of PMOS transistors as the main switch، as the PMOS turns on when the voltage gate is low

2.2.3.1 Negative voltage converter with active diode

The proposed active rectifier [16-17] is provided using the two stages as shown in Figure 2.15. The first stage Negative Voltage Converter "NVC" is used to convert the negative half-wave of input alternating signal to positive by using two PMOS and two NMOS connected as shown in Figure 2.16. During the positive half-wave of the input ($V_{in1}>V_{in2}$), MP_1 and MN_1 will be conductive when the input voltage becomes greater than V_{thn} and V_{thp}, then terminal 1 becomes high "v_{in1}" and terminal 2 becomes low "v_{in2}". During the negative half-wave ($V_{in2}>V_{in1}$), MP_2 and MN_2 will be conductive then terminal 1 becomes high "v_{in2}" and terminal 1 becomes low"vin1". Therefore terminal 1 is always high. The voltage drop across NMOS and PMOS reaches to V_{thn} and V_{thp}. A further increase of the transistor width would decrease the resistance to get a smaller voltage drop, but also very large area consumption.

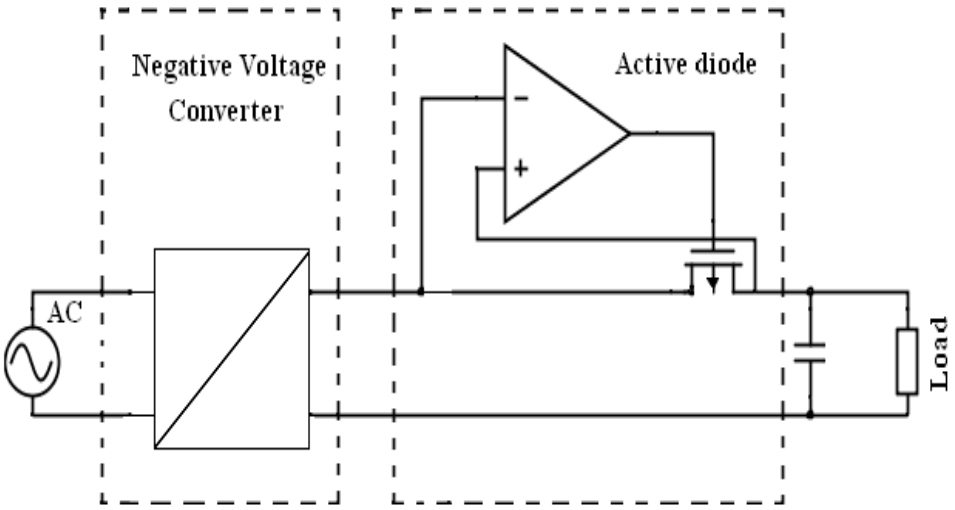

Figure 2.15 Negative voltage converter with active diode. [17]

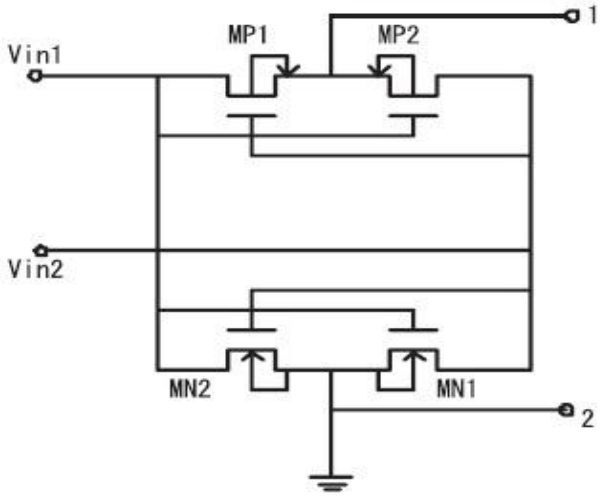

Figure 2.16 Negative voltage converter schematic. [17]

2.2.3.2 Cross-coupled active full bridge

The proposed cross-coupled active full bridge [18-19], displayed in Figure 2.17, consists of two cross-coupled inverters and two active diodes. During the positive wave of the input AC signal ($V_{in1}>V_{in2}$), MP_1 will be active when the input voltage becomes greater than V_{thp}, While the voltage at the negative input port of the left comparator becomes low " V_{in2}". Correspondingly, the output of the left comparator becomes high which turns the transistor MN2 ON. Thus, the current flowing through (MP_1-MN_2) charges the loading capacitor C_L. During the negative wave of the input AC signal ($V_{in2}> V_{in1}$) MP_2 will be active when the input voltage becomes greater than V_{thp}, While the voltage at the negative input port of the right comparator becomes low "V_{in1}". Correspondingly, the output of the comparator is high which turns the transistor MN_1 ON. Thus, the current flowing through (MP_2-MN_1) charges the loading capacitor C_L.

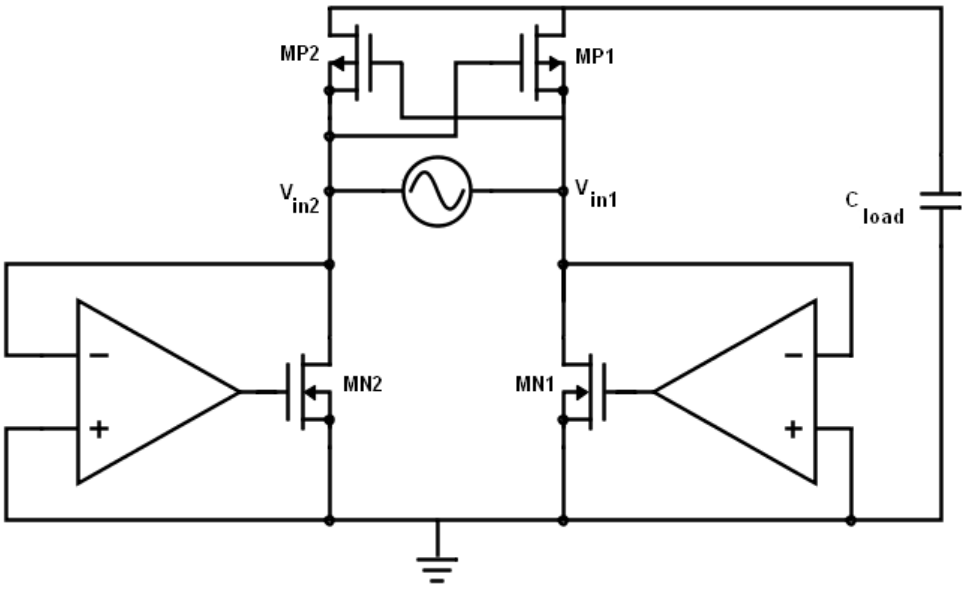

Figure 2.17 Cross coupled active diode. [17]

2.2.3.3 Active bridge voltage doubler

The active bridge voltage doubler [20-21], shown in Figure 2.18, consists of positive and negative peak detectors, that generate DC voltages that track the positive and the negative voltage of the input AC signal. During the positive wave of the input AC signal, the voltage at the negative input port of the comparators is greater than 0V. Correspondingly, the comparator output is low which turns the PMOS switch ON and turns the NMOS switch OFF. Thus, the current flowing through the PMOS switch charges the loading capacitor C_{load}. During the negative wave of the input AC signal, the voltage at the negative input port of the comparator is lower than 0V. Correspondingly, the comparator output becomes high which turns the NMOS switch ON and turns the PMOS switch OFF. Therefore, the current flowing through the NMOS switch charges the loading capacitor C_{load}. The total voltage drop of the active bridge doubler is $V_{th\ switch.}$ The main advantage of that it provides two positive and negative DC output voltages.

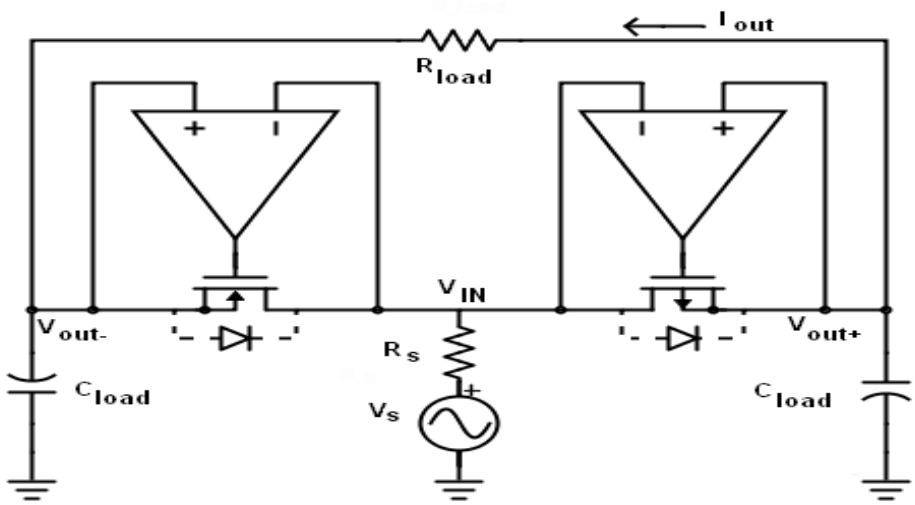

Figure 2.18 Active bridge voltage doubler. [17]

2.3 Switched capacitor DC/DC

Switched-capacitor DC/DC converter (SC DC/DC converter) is a type of voltage converters which provides “a DC voltage level to DC voltage level” conversion using only capacitors without using inductor that used at the conventional DC/DC make SC DC/DC have no EMI emission, smaller size, and easy system integration. SC DC/DC can generate a higher output voltage than the supplying voltage and higher area occupation when compare with the low-dropout regulators (LDO) which provide conversion with step-down only and low area occupation. However, SC DC/DC has a poorer power conversion efficiency than conventional inductor DC/DC.

2.3.1 Linear SC DC/DC

For the linear switched-capacitor DC-DC (Dickson charge pump) as shown in Fig. 2.19[22], the capacitor voltage in each stage is charged to a supply voltage V_{DD}, during the phase clock $\Phi_1$or other phase clockΦ_2. Therefore, by cascading n repeating stages, the output voltage will be $(n+1)V_{DD}$ in the ideal case, i.e. the conversion ratio is $(n+1)$.

2.3.2 Fibonacci SC DC/DC

For the Fibonacci switched-capacitor DC-DC topology as shown in Fig. 2.20[23], the capacitor voltage is charged to $F(n+1)V_{DD}$ during phase clock Φ_1 or other phase clock Φ_2. Therefore, by cascading n repeating stages, the output voltage will be $F(n+1)V_{DD}$ in the ideal case, i.e. the conversion ratio is $F(n+2)$.

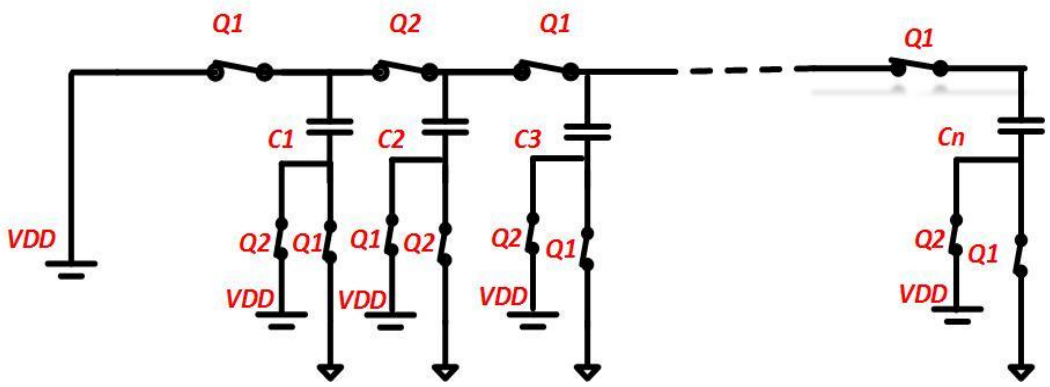

Figure 2.19 Linear switched-capacitor DC-DC. [22]

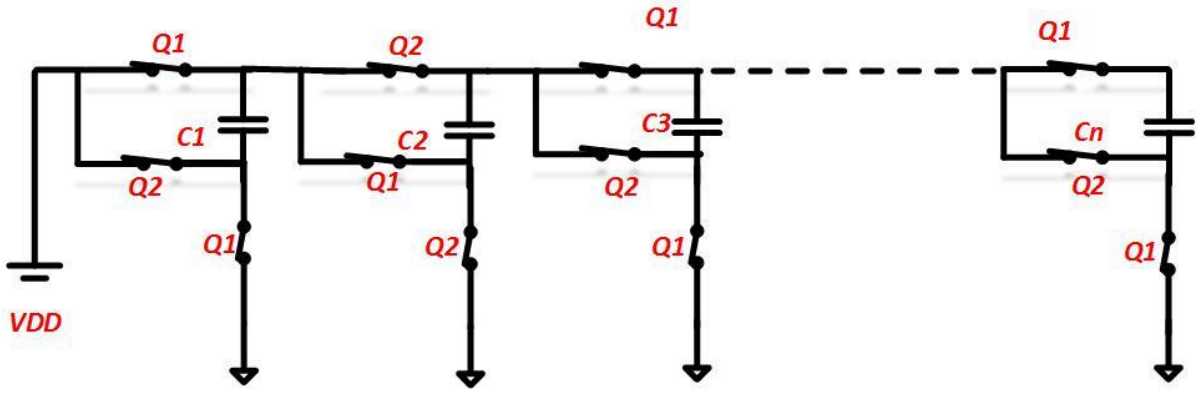

Figure 2.20 Fibonacci switched-capacitor DC-DC. [23]

2.3.3 The exponential SC DC/DC

For the exponential switched-capacitor as shown in Fig. 2.21 [23], the step-up voltage at the output stage will be used as an input voltage of the next stage. Hence the conversion ratio of an *n*-stage exponential switched-capacitor is $2^n V_{DD}$.

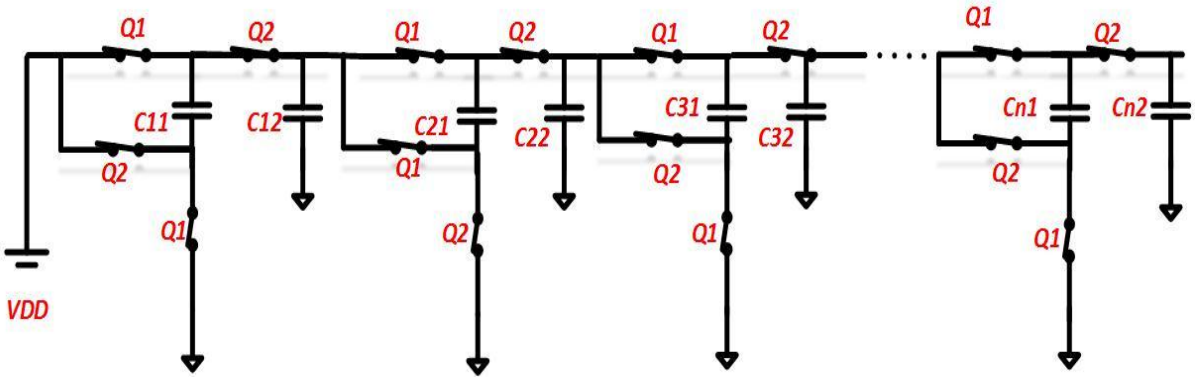

Figure 2.21 An exponential SC DC-DC converter. [23]

2.4 Maximum power point tracking (MPPT)

The maximum output power for a microscale energy transducer depends on the strength of the environment of the energy sources. It is used to ensure that energy harvesting systems operate at the maximum power point of energy transducers at any time, to maximize the amount of energy extracted.

2.4.1 Perturb and Observe Method

The P&O algorithms [24] operate by periodically perturbing (i.e. incrementing or decrementing). The array terminal voltage or current of the transducer changed then compared with the output power of the previous perturbation cycle. The ambient source operating voltage changing and increasing the output power, then the control system moves in the same direction otherwise if the output power decreasing then moving the operating point in the opposite direction and soon in the next perturbation cycle.

A P&O common problem is that the array terminal voltage of transducer is perturbed every MPPT cycle; therefore the output power oscillates around the maximum, resulting in power loss in the ambient source system. There are many different P&O methods available in the literature. The classic P&O method (P&Oa), the perturbations is done with a fixed magnitude. In the optimized P&O method (P&Ob), the magnitude of perturbations is dynamically adjusted by the average of several samples of the array power. In the three-point weight comparison method (P&Oc), the perturbation direction is decided by comparing the output power on three points.

2.4.2 Open voltage method

The open voltage (OV) [25] method is based on the relation between the maximum power point and open voltage with a fixed percentage of the open voltage. The linear relationship between the maximum power point voltage (V_{MPPT}) and the open-circuit voltage (V_{oc}) under different environmental conditions.

$$V_{MPPT} = KV_{oc} \tag{2.3}$$

Where K is the constant voltage factor

2.4.3 Short circuit current method

The short circuit current method is the same as the open-circuit voltage. There is a linear relationship between the current of maximum power point tracking IMPPT and the short circuit current,

$$I_{MPPT} = KI_{sc} \tag{2.4}$$

Where K is the constant current factor and Isc is short circuit current [26]. It is a higher implementation cost but more accurate and efficient.

2.4.4 Look – up table method

In this method, there is stored data for the ambient source under different environmental conditions. The output power is calculated and compared with stored data to track the maximum power point. This method requires a larger capacity to store the data under different atmospheric conditions [27] and requires many sensors, it is not very accurate and its speed is not so good.

2.5 Analog to Digital converter

Analog-to-digital converters (ADCs) play an important role to convert the analog signal to a digital signal. We can find ADC in many applications that we used today from tiny electronics circuits to huge rockets. The parameters that distinguish any ADC are sample rate, resolution, and power dissipation. The following section explains the different ADC.

2.5.1 Flash ADC

Flash analog to digital converter "parallel converter" as it depends on parallel architecture. It is the fastest conversion rate and a high sampling frequency. It consumes much power.

2.5.2 Sigma delta ADC

Sigma delta analog to digital converter has low power consumption and a higher resolution.

2.5.3 Successive approximation ADC

Successive approximation SAR analog to digital converter is the optimum solution for application required medium to high resolution. It has low power consumption so it is used for portable and powered systems.

2.5.4 Folding interpolating ADC

Folding analog to digital converters, has high speed and high conversion rate and it's simpler compared to flash analog to digital converter.

2.5.5 Pipeline ADC

The pipelined analog to digital converter is used at a wide range of applications due to its high-resolution rate up to sixteen bits and the sampling rate up to 100 samples per second.

Table 2.2 shows the different analog to digital converters. The folding interpolating has the highest conversion while sigma delta has the highest resolution. SAR, Pipeline, and flash have the lowest latency. Table 2.3 shows the comparison between the mentioned analog to digital converters in power, area, and cost. The SAR has the lowest power, cost, and area while flash has the highest power, cost, and area

Table 2.2 Comparison between different ADCs (latency, conversion and resolution)

Architecture	**Latency**	**Conversion**	**Resolution**
SAR	Low	Slow	Moderate
Sigma –Delta	High	Slow	High
Pipeline	High	Fast	Moderate
Flash	Low	Moderate	Low
Folding-Interpolating	Low	Fast	Medium

Table 2.3Comparison between different types of ADC [28]

Architecture	**Power**	**Cost**	**Area**
SAR	Low	Low	Low
Sigma -Delta	Moderate	Moderate	Moderate
Pipeline	High	Expensive	Medium
Flash	High	Expensive	Large
Folding-Interpolating	Low	Moderate	Medium

Chapter 3 Energy harvesting system

The energy harvesting system aims to convert ambient energy, for example, mechanical, photovoltaic solar, thermal or radio frequency into electrical energy which can be stored in batteries. Ambient energy of thermoelectric generators (TEG), silicon-based micro-fuel and a single junction photovoltaic (PV) cells produces a dc power that can easily charge batteries without the need for AC/DC converter. Ambient energy of piezoelectric, electromagnet and RF produces AC power which needs AC/DC converter to be converted from ac power to dc power that can be easily stored by charging batteries.

The maximum power point tracker is an electronic DC/DC converter that optimizes the match between the output voltage of the AC/DC converter and batteries' voltage by reducing the higher voltage DC output from AC/DC converter to the lower voltage which is needed to charge batteries.

The control unit provides the desired switching frequency with enough capability to drive the charge pump power. The control unit consists of analog to digital converter and digital control oscillator. The analog to digital converter is used to convert the analog signal which is produced from the AC/DC converter to digital signal; this signal is converted by the digital control oscillator into the desired switching frequency needed for the switched capacitor charge pump. The energy harvesting system block diagram is shown in Figure 3.1.

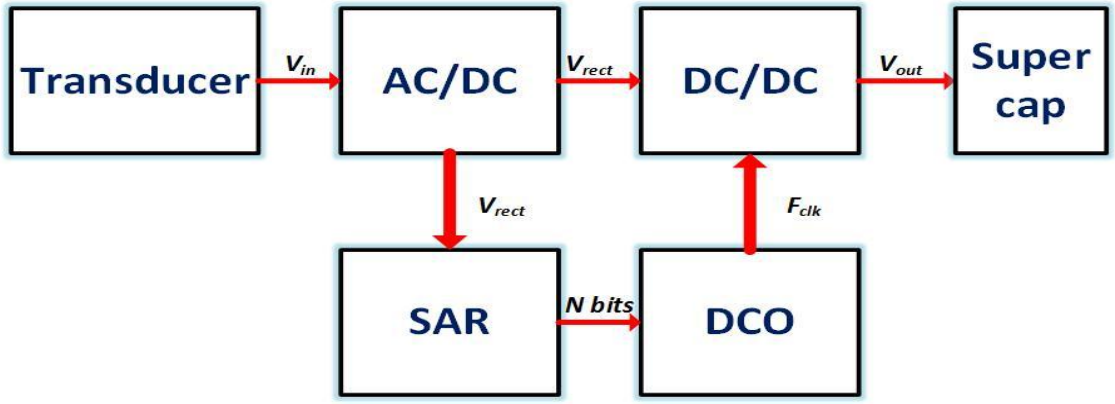

Figure 3.1 Energy harvesting system.

3.1 The AC/DC converter

The AC/DC converter is used to convert AC power harvested using a piezoelectric transducer to DC power as shown in Figure 3.2, AC source V_{in} is used instead of using a piezoelectric transducer for easy understanding. AC/DC converter consists of two stages, At the first stage during the negative cycle of AC input signal, the capacitor C_1 is charging by the AC peak voltage $V_{C1}=2V_{in}-V_{th(M1)}$, as the transistor M_1 acts as a diode clamp, During the positive cycle of the AC input signal, the capacitor C_1 discharged very little as the transistor M1 is OFF, the AC peak voltage will be $(2V_{in}- V_{th\ (M1)})$ at terminal A. When the voltage at point (B) is smaller than the voltage at point (A), the transistor M_2 is ON that allows charging of the capacitor C3 to DC voltage $V_{C3}=2V_{in}-V_{th(M1)}-V_{th(M2)}$.

When the voltage of point (A) is smaller than the voltage of point (B), the transistor M_2 is OFF, disconnected the forward path of conduction. At point (C) the capacitor C_2 voltage is shifted by a DC value ($2V_{in}$-$V_{th(M1)}$-$V_{th(M2)}$-$V_{th(M3)}$) plus the AC peak voltage ($2V_{in} - V_{th(M1)}$) from the second path.

At the second stage if the voltage of point (D) is smaller than the voltage of point (C), the switch M_4 ON allows a capacitor C_4 charging by a DC value ($4V_{in}$-$V_{th(M1)}$-$V_{th(M2)}$-$V_{th(M3)}$-$V_{th(M4)}$). When the voltage of point (C) is smaller than the voltage of point (D), the switch M4 OFF, and discharges the capacitor C_4 by R_L.

The active diode is a comparator-controlled PMOS switch as shown in Figure 3.3 .The comparator controls the gates of the switch M1 by using transistor M4-M9. The transistors M10-M12 are current mirrors used to supply the circuit with the current needed to power on the comparator. To reduce the voltage drop, the transistor M1 should turn ON and OFF completely. The bulk regulator is used by the transistors M2-M3 to prevent the chance of latch-up, the substrate of transistors M1, M4 and M6 will be connected to the highest potentials. If the switch M1 PMOS is still ON while V_{out} is higher than V_{in}, the reverse current appeared from V_{out} to V_{in}, and the power efficiency of the AC/DC converter will be reduced. As the gate voltage of PMOS switch M1 takes time to change to high voltage. The reverse current should be minimized to enhance the power efficiency by adjusting the size of transistor M11 and M12. The transistor size of M11 ought to be smaller than the transistor size M12, to eliminate the reverse current and minimize the delay. By setting R_{load} =30KΩ, the current passes through the current mirror is very small, So V_{GS}=V_{th}. The gate voltage of transistors M7 and M4is around Vin_+-V_{th}.M4 turns ON when $V_{in-} > V_{in+}$ .Meanwhile, M5 turns OFF and the gate of M1 is pulled high to connect the gate of M1 to the ground. Then M1 turns on to charge the capacitor C3 .

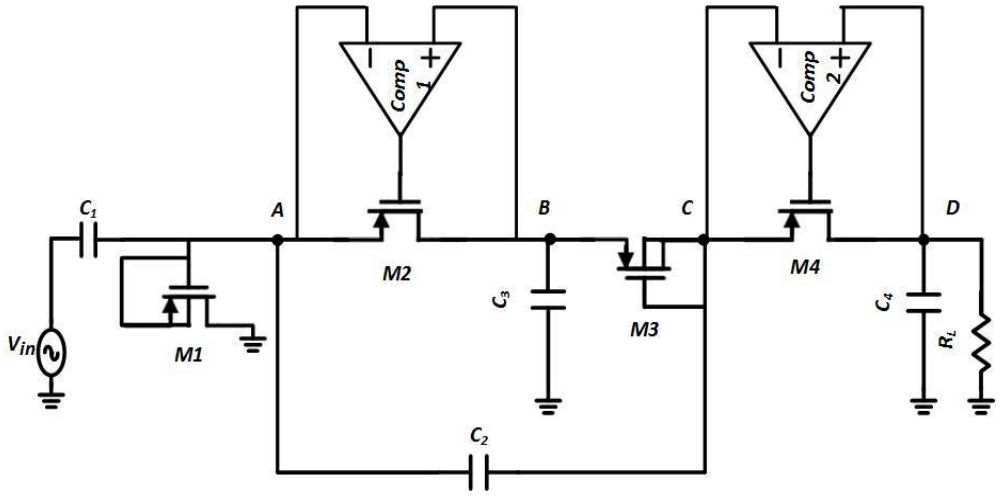

Figure 3.2 The proposed voltage multiplier AC/DC converter. [29]

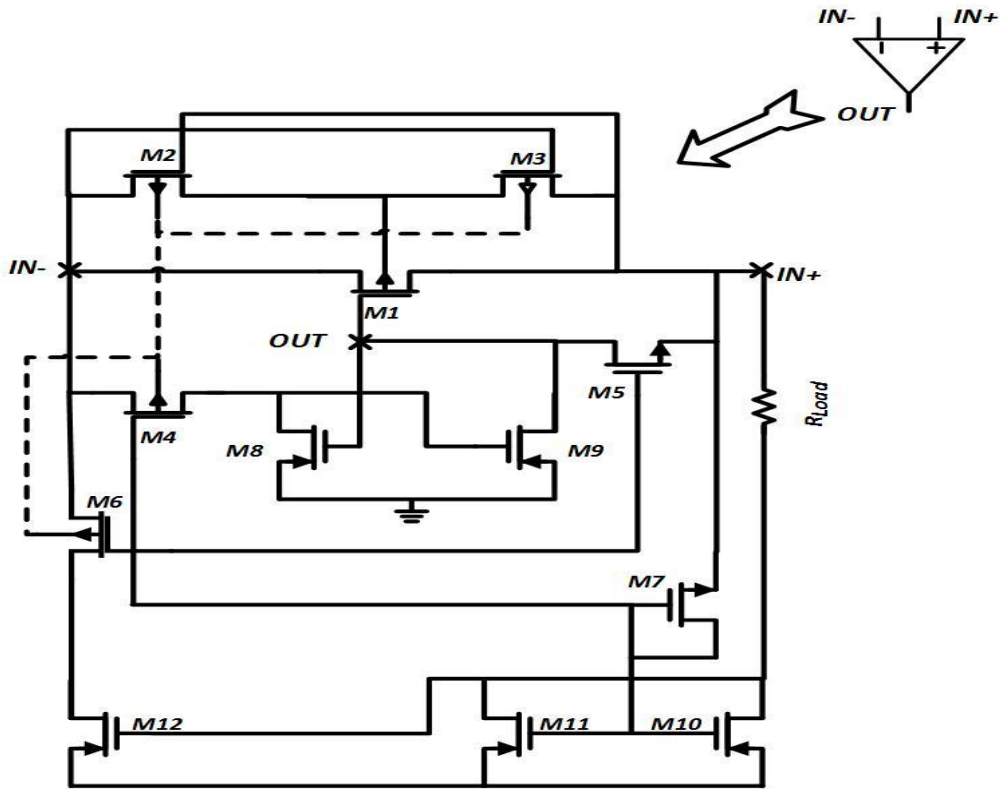

Figure 3.3 The proposed active diode circuit. [29]

The sizes of all devices used in this rectifier and active diode are shown in Table 3.1 and Table 3.2.

Table 3.1: Size of devices in the proposed rectifier

Device	size
M1	1300 µm/0.3 µm
M3	100 µm/3 µm
M2,M4	13 µ/0.3 µm

Table 3.2: Size of devices in the proposed active diode

Device	size
M1	1300 µm/0.3 µm
M2,M3	13 µm/0.3 µm
M4,M5	1 µm/130 nm
M6	1 µm/0.3 µm
M7,M8,M9	1 µm/0.13 µm
M10	10 µm/0.3 µm
M11	20 µm/0.3 µm
M12	40 µm/0.3 µm

3.2 Simulation results

By using cadence spectre the voltage multiplier AC/DC converter is simulated using 130nm CMOS technology TSMC provider. Figure 3.4 shows the proposed voltage multiplier AC/DC transient behavior at different input values. Figure 3.5 shows the proposed voltage multiplier AC/DC transient behavior at sample input values.

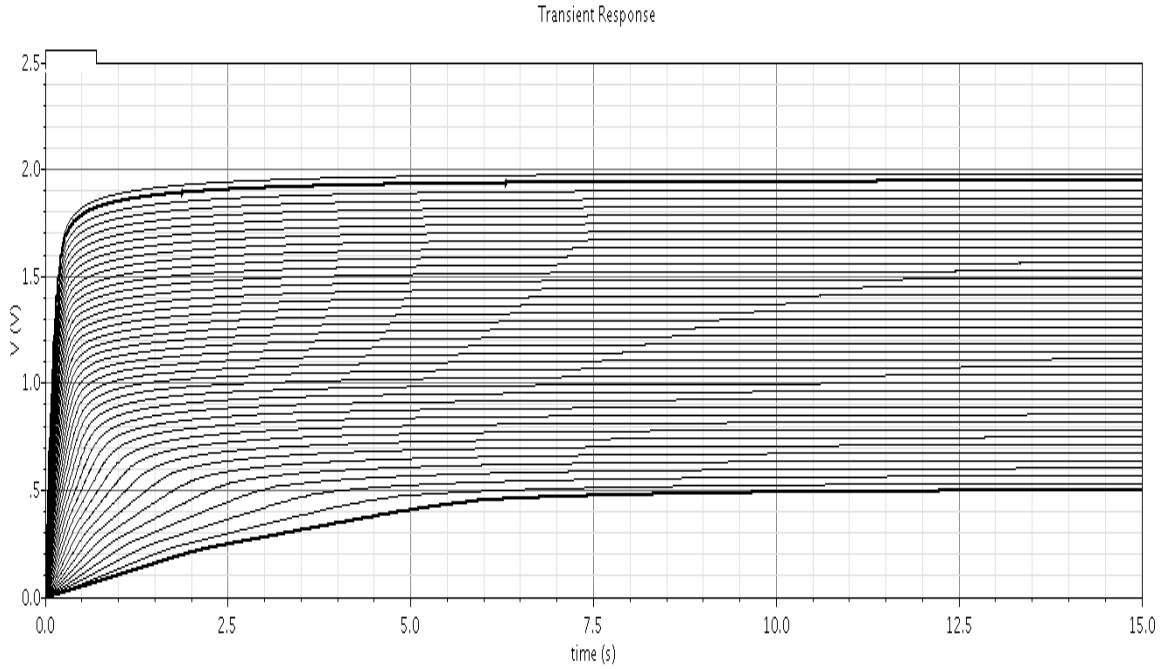

Figure 3.4 The proposed voltage multiplier AC/DC transient behavior.

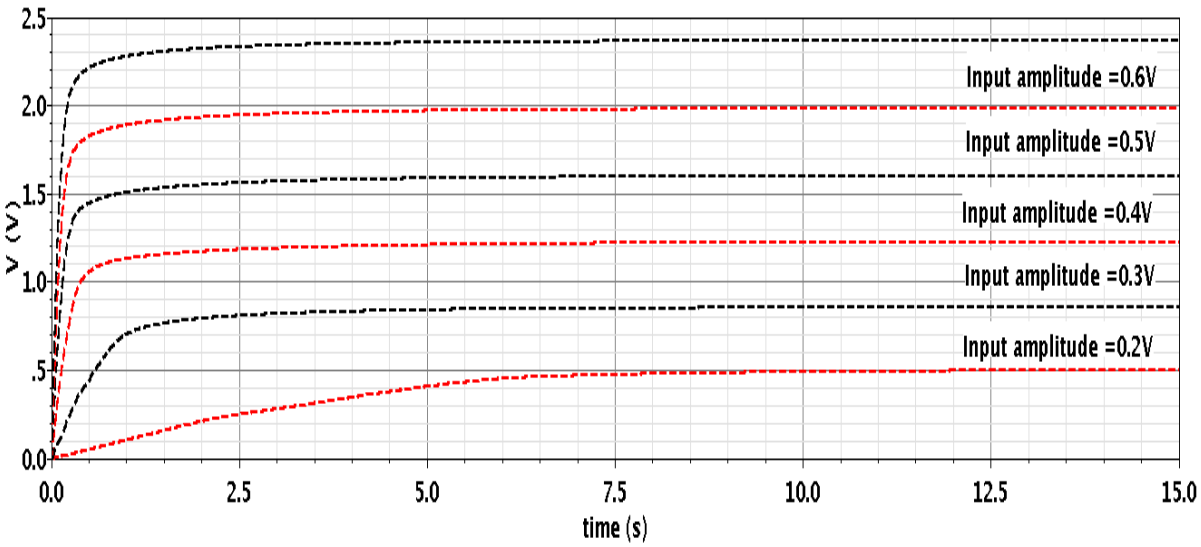

Figure 3.5 The proposed voltage multiplier AC/DC transient behavior.

Figure 3.6 shows the simulation result of the voltage value at point (A) at the proposed voltage multiplier AC/DC for voltage peak 500m, VA $=2V_p-V_{th(M1)}$. Figure 3.7 shows that the voltage value at point (B) that equals to $2(V_p-V_{th})$. The voltage value at point (C) is shown in Figure 3.8 that composed of a DC level equals to $2V_p-3V_{th}$ and an AC level equals to $2(V_p-V_{th})$ through the capacitor C_2. The output voltage at point (D) will be $4(V_p-V_{th})$ as shown in Figure 3.9.

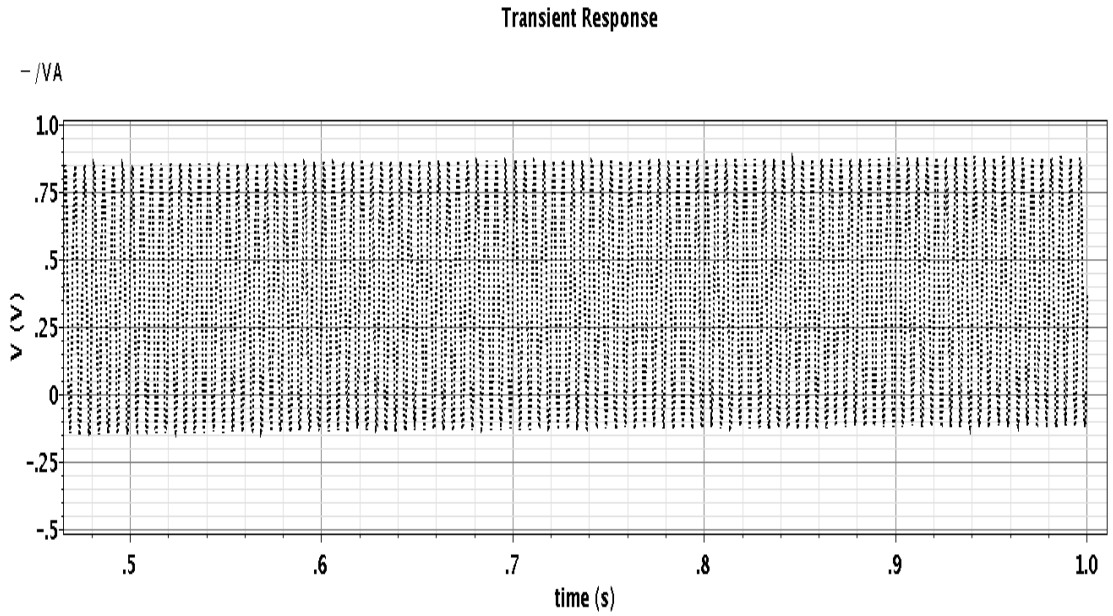

Figure 3.6 The voltage Value at point (A) at the proposed voltage multiplier AC/DC.

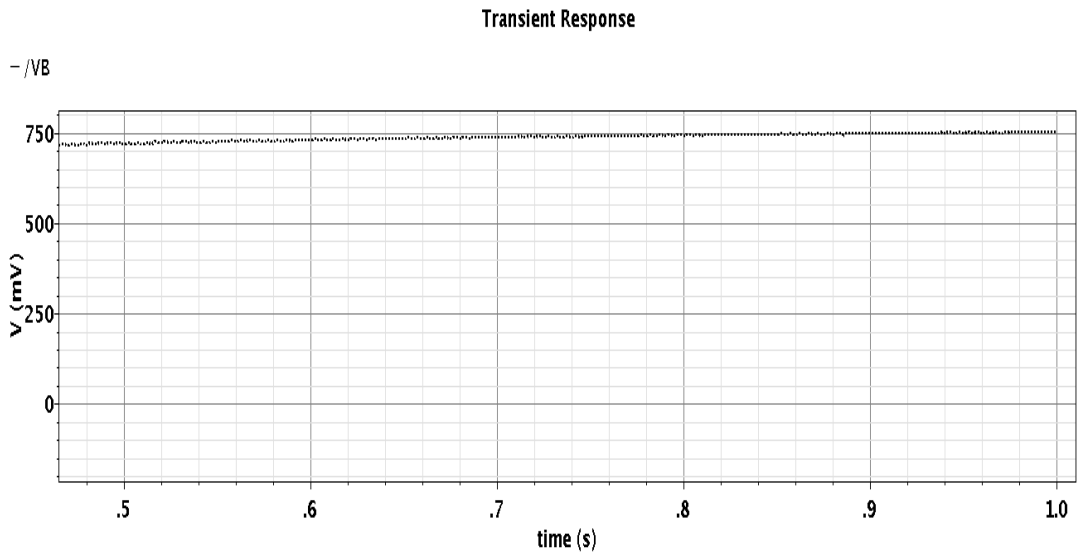

Figure 3.7 The voltage Value at point (B) at the proposed voltage multiplier AC/DC.

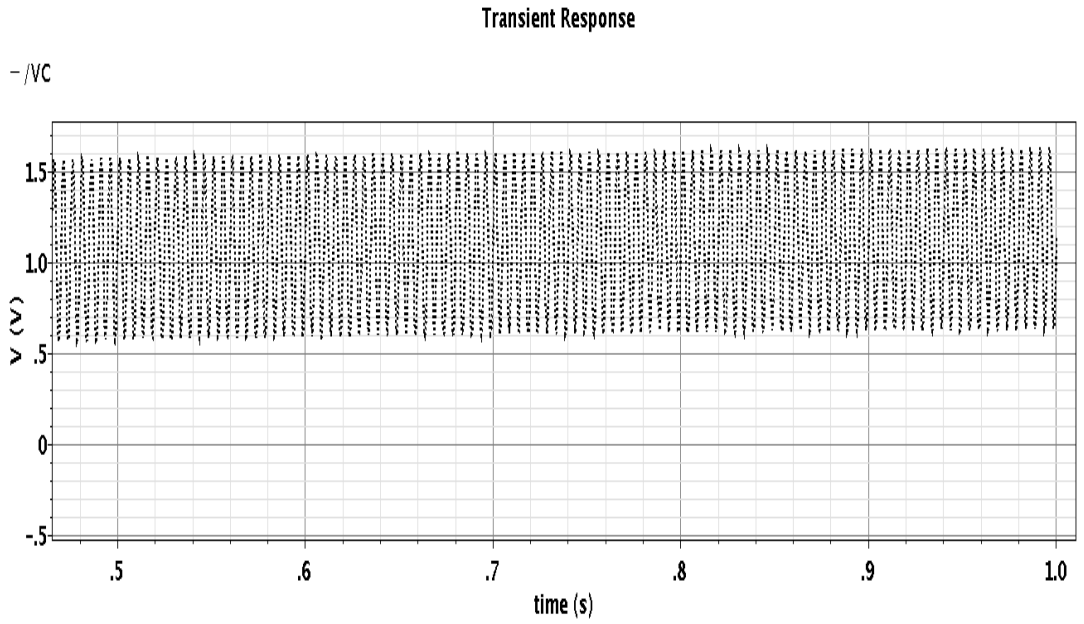

Figure 3.8 The voltage Value at point (C) at the proposed voltage multiplier AC/DC.

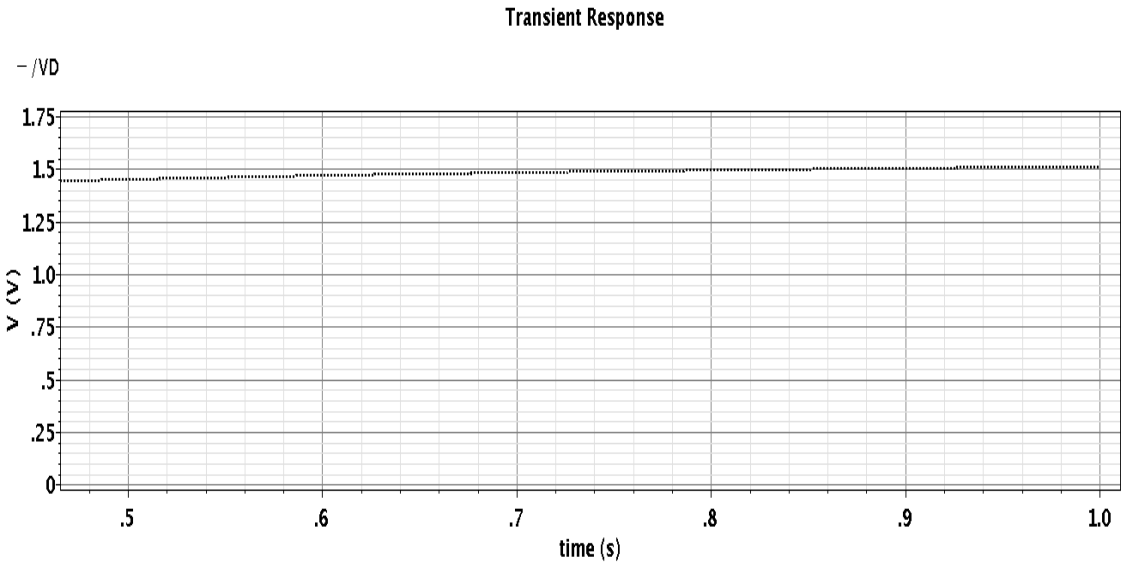

Figure 3.9 The voltage Value at point (D) at the proposed voltage multiplier AC/DC.

Figure 3.10 shows the simulation result of the voltage value at point (A) at the proposed voltage multiplier AC/DC for voltage peak 400m, VA $=2V_p-V_{th(M1)}$. Figure 3.11 shows that the voltage value at point (B) that equals to $2(V_p-V_{th})$. The voltage value at point (C) is shown in Figure 3.12 that composed of a DC level equals to $2V_p-3V_{th}$ and an AC level equals to $2(V_p-V_{th})$ through the capacitor C_2. The output voltage at point (D) will be $4(V_p-V_{th})$ as shown in Figure 3.13.

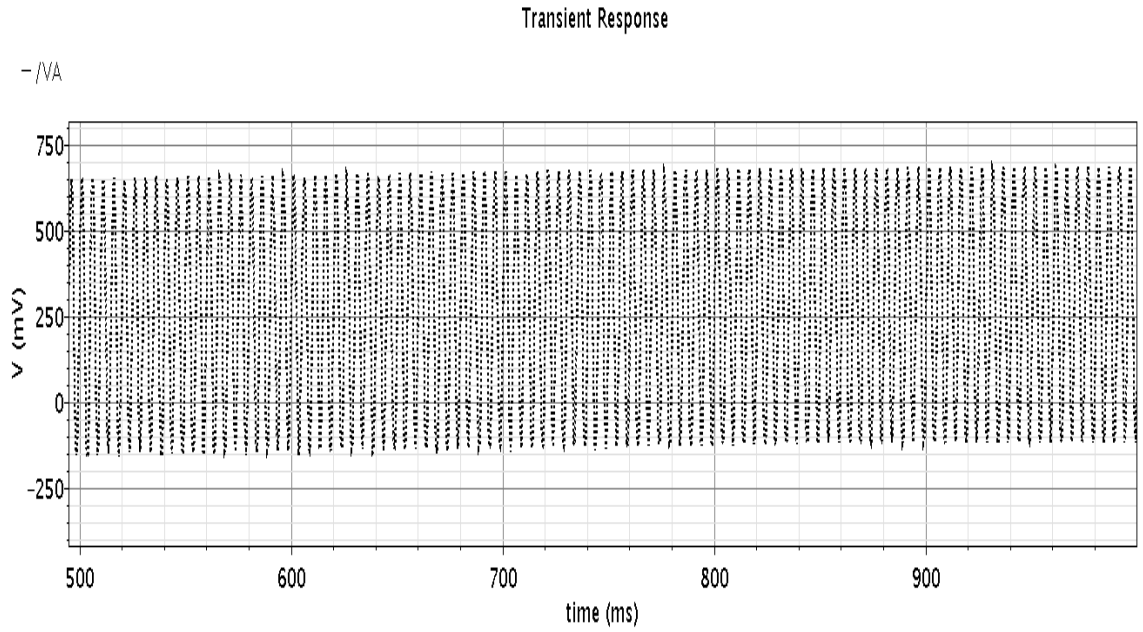

Figure 3.10 The voltage Value at point (A) at the proposed voltage multiplier AC/DC.

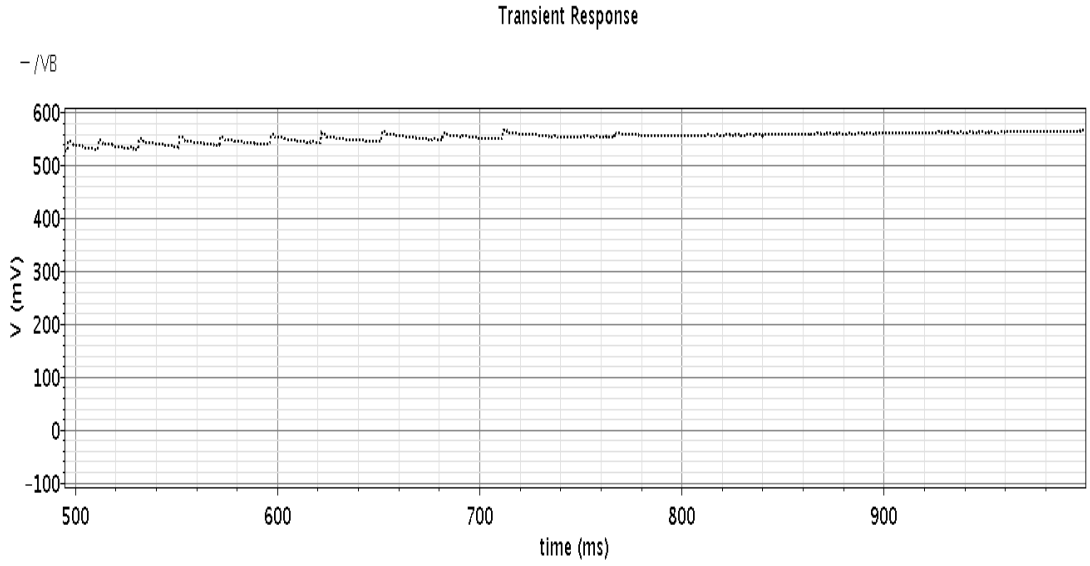

Figure 3.11 The voltage Value at point (B) at the proposed voltage multiplier AC/DC.

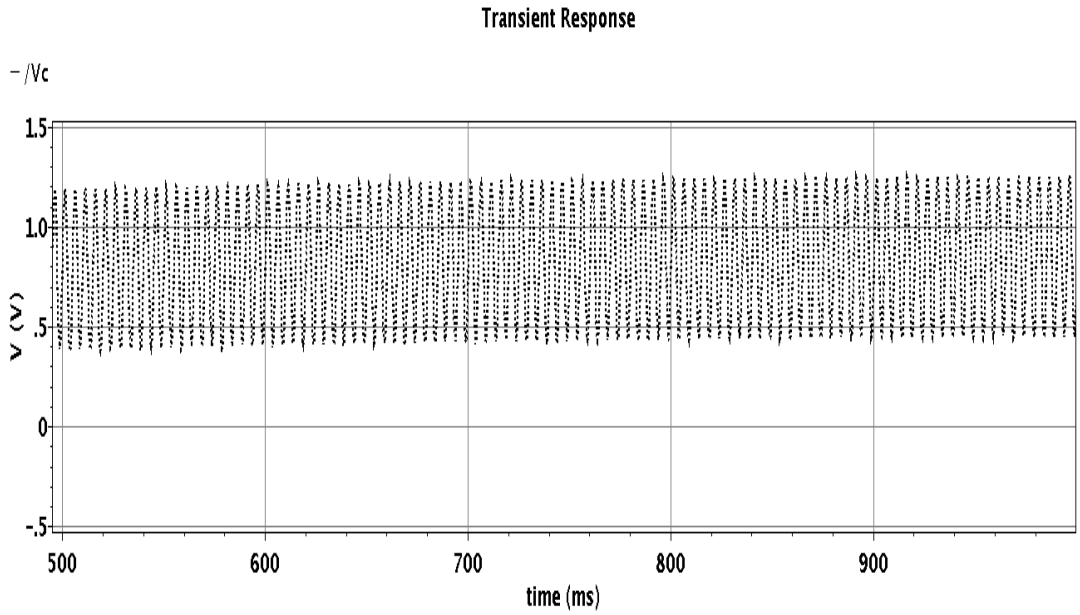

Figure 3.12 The voltage Value at point (C) at the proposed voltage multiplier AC/DC.

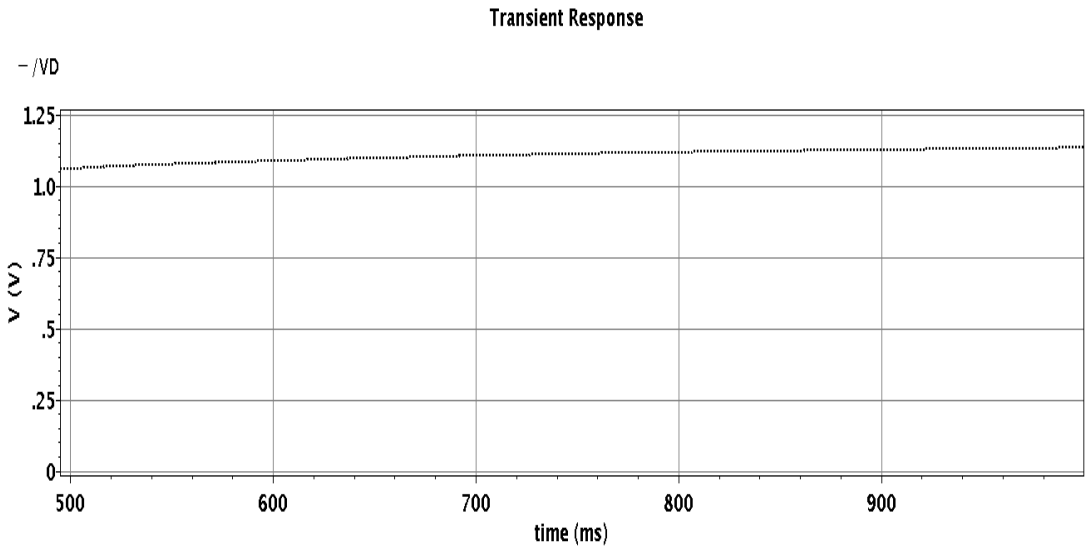

Figure 3.13 The voltage Value at point (D) at the proposed voltage multiplier AC/DC.

Figure 3.14 shows that the transient response of the active diode with propagation delay 30ns, AC analysis for the active diode is shown in Figure 3.15, we can find the gain and bandwidth 600MHz.

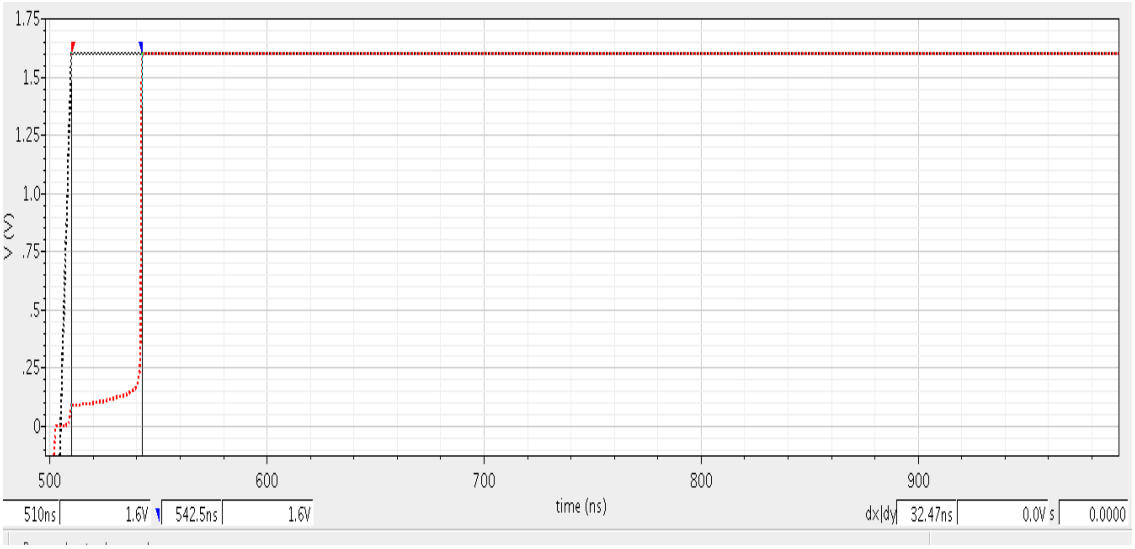

Figure 3.14 Transient response of the active diode

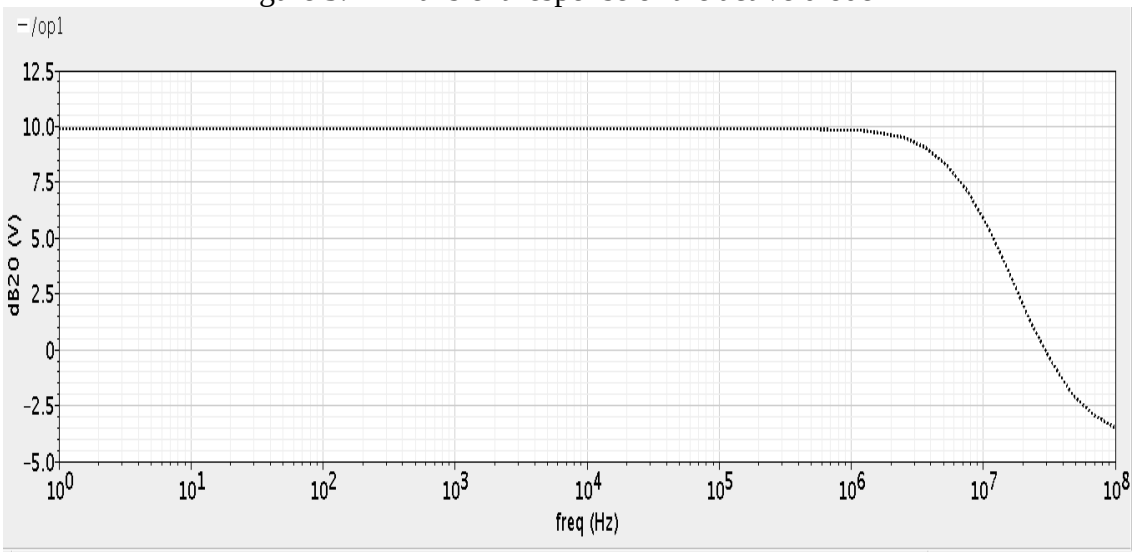

Figure 3.15 AC response of the active diode.

The different input voltage amplitude versus voltage efficiency with 100kΩ load and without load the proposed circuit is shown in Figure 3.16, the voltage conversion efficiency for input voltage 0.6 V will be larger than 300% without load and for input 0.7V the voltage conversion efficiency will be 270% with 100kΩ load.

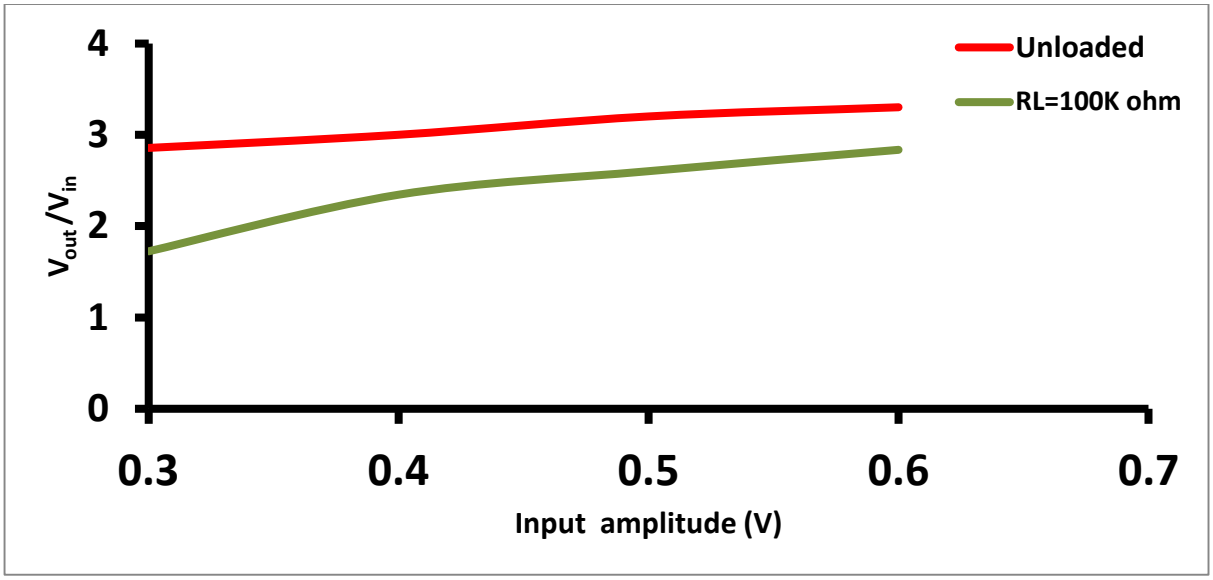

Figure 3.16 The different input voltage amplitude versus voltage efficiency with 100K Ω load and without load.

The power efficiency is calculated using

$$\frac{\int_0^T Vout(t)Iout(t)dt}{\int_0^T Vin(t)Iin(t)dt}100\% \qquad (3.1)$$

Where T is one period. Figure 3.17 shows the power efficiency for the proposed voltage multiplier AC/DC for different input voltage amplitude and the maximum power efficiency is 83%.

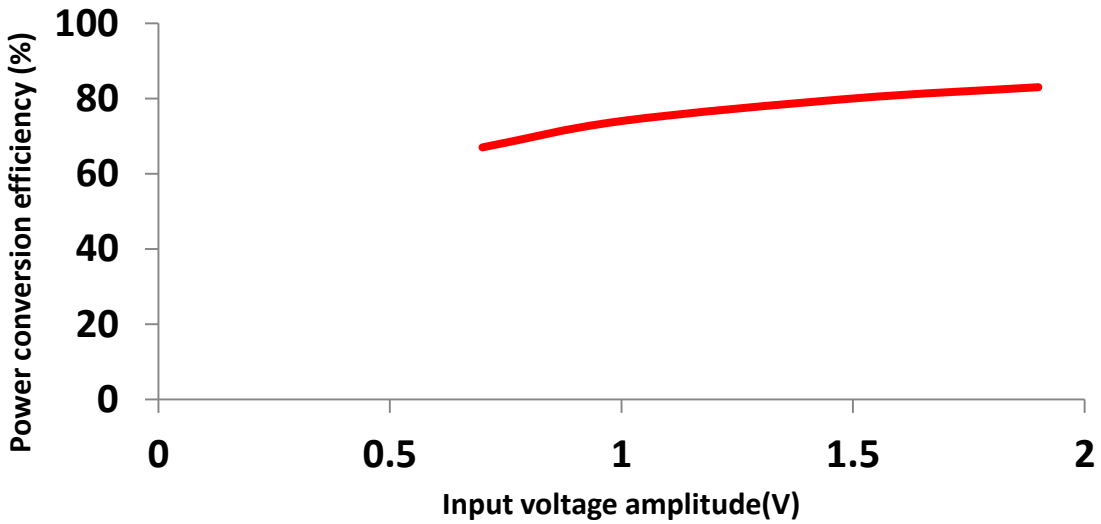

Figure3.17 Input voltage amplitude versus power efficiency.

Table 3.1 presents a comparison with the latest papers. The minimum input voltage will be 0.2 and 83% is the maximum power efficiency of the proposed circuit. The voltage conversion ratio will be 270% with 100KΩ load and its ripples lower than 5% compared to the other AC/DC circuits.

Table 3.3A comparison with latest papers

Ref.	TPEL 2011 [30]	ICEAC 2012 [31]	Transducers 2013 [32]	CSENS 2014 [33]	**This work [29]**
Tech.	External supplies	TSMC 90nm	TSMC 90nm	UMC 180 nm	TSMC 130nm
Input	0.1V-1.2V	0.1V-1V	0.1V-0.8V	0.15V-1V	0.2V-0.7V
Output	N/A	≃ 0.2V-1.7V	≃ 0.2V-1.4V	≃ 0.2V-2V	≃0.5-2.2V
Ripples	10%	N/A	N/A	N/A	<5%
Frequency	1Hz-500Hz	1Hz-10kHz	10H.z	8H.z	20Hz-1KHz
Max power efficiency	>80%	92%	67%	86%	83%

Figure 3.18 shows that by adjusting the size of the transistor there will be no delay time of active diode so the power efficiency will be enhanced.

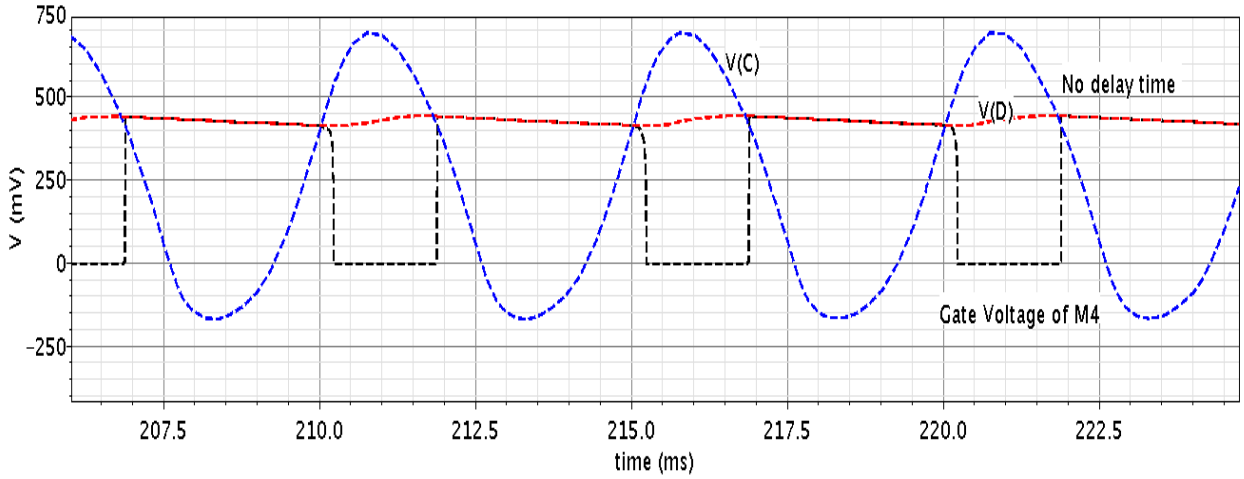

Figure 3.18 No delay time of active diode

Figure 3.19 shows the output dc voltage for the proposed AC/DC converter versus the maximum power that we can get by changing the R_L for the different input values. Figure 3.20 shows the output dc voltage for the proposed AC/DC converter versus the maximum power for the sample input value.

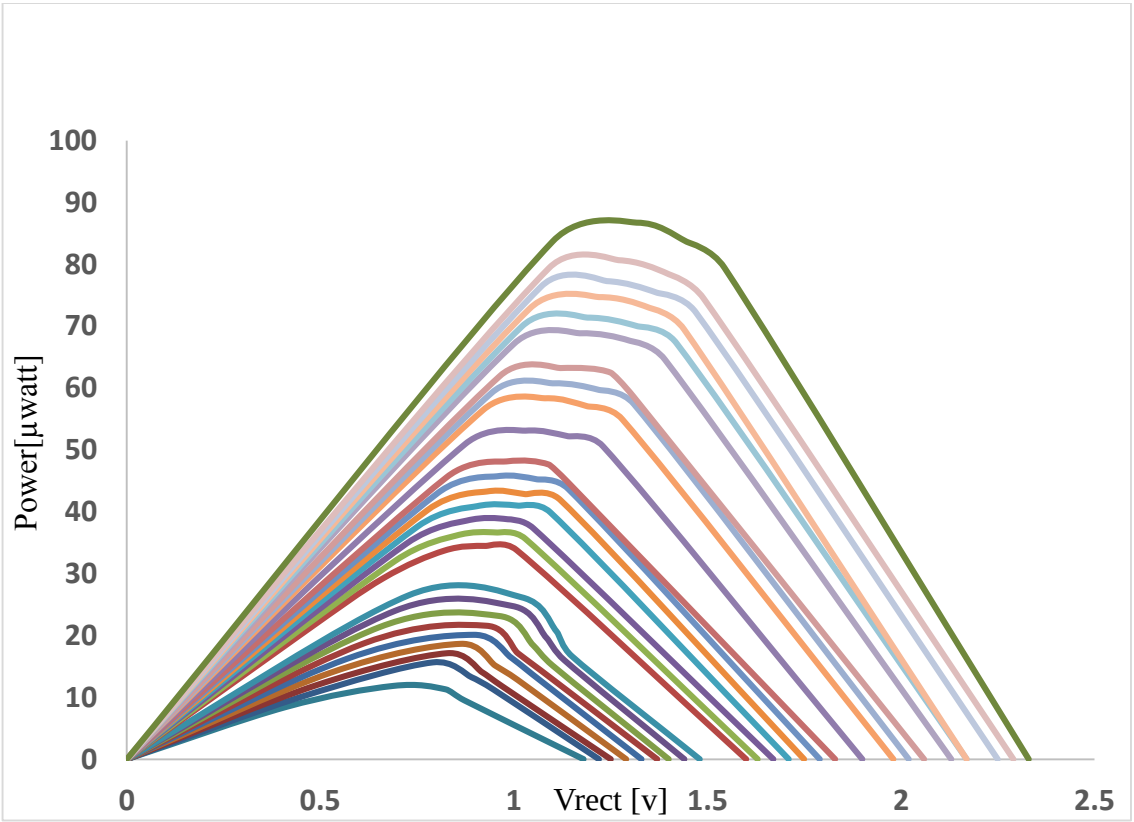

Figure 3.19 The Vrect versus the maximum power.

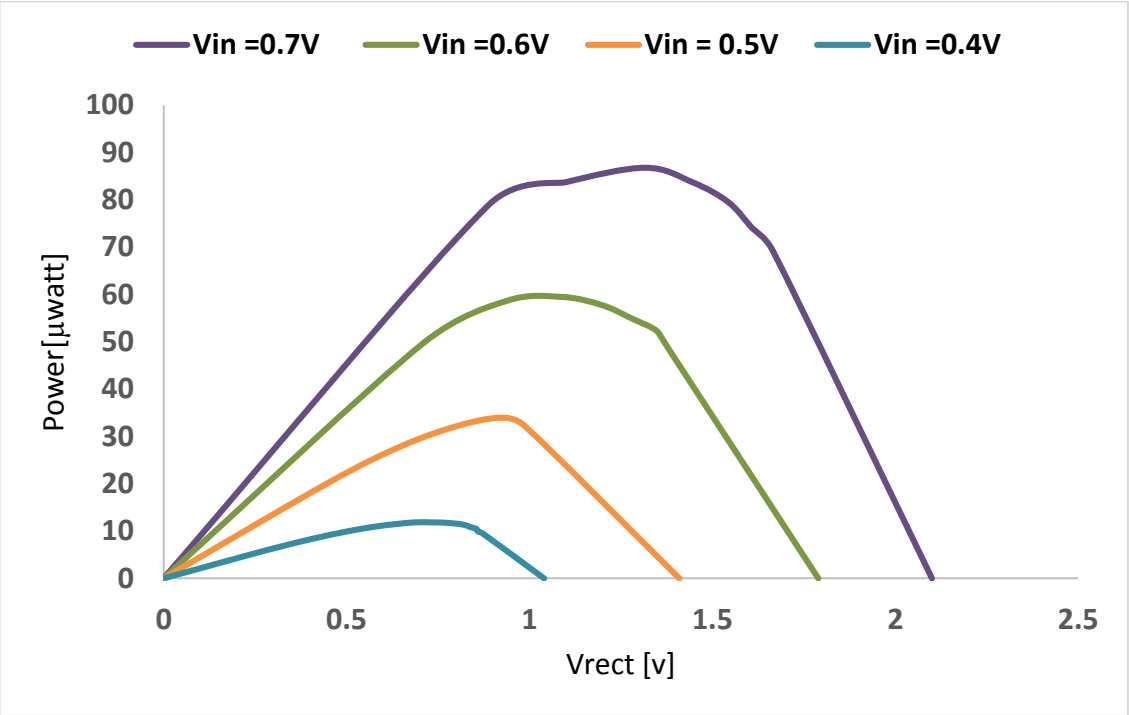

Figure 3.20 The Vrect versus the maximum power for sample of input.

3.3 The DC/DC converter charge pump

The maximum power point tracker is an electronic DC/DC converter that optimizes the match between the output voltage of the AC/DC converter and batteries' voltage by reducing the higher voltage DC output from AC/DC converter to the lower voltage which needed to charge batteries.

The charge pump is used to transfer the harvesting energy from ambient sources to provide the electronics circuit with the needed power through the output capacitor without the need of replacing the battery as shown in Figure 3.21. The operation of this topology working as a following, When Q is high, C3 top plat $V_x=V_1$ and the bottom plate connected to the ground. When Q is low, path 1 is disconnected, and V_3 is charged up by path 2 so if $V_x>V_{out}$ the charge stored at C3 and if $V_x<V_{out}$ the charge moved to supercapacitor.

The amount of charge transfer through path 1 to last stage

$$Q_1=C_1V_{rect}-C_1(V_1-V_{rect}) =C(2V_{rect}-V_1) \quad (3.2)$$

The amount of charge transfer through path 2 to last stage

$$Q_2=C_2V_{rect} -C_2(V_2-V_{rect}) =C(2V_{rect}-V_2) \quad (3.3)$$

The amount of charge transfer from last stage to C_{out}

$Q_3=C_3V_1 - C_3(V_{out}-V_x) = C(V_1 + V_x - V_{out})$ (3.4)

$Q_1=Q_2=Q_3$ from which we can obtain that

From $Q_1=Q_2$, We get $V_1=V_2$

From $Q_1=Q_{3,}$ We get $2V1-V_{out}=2V_{rect}-V_1$

$V_1=1/3\ (2V_{rect}+V_{out})$ (3.5)

$Q3=C\ (4V_{rect}-V_{out})\ /3$ (3.6)

The output current for DC/DC can be modeled as:

$$I_{out} = f_{clk} Q_{avg} = \frac{1}{3} f_{clk}\, C\ (4V_{rect} - V_{out}) \quad (3.7)$$

Where, f_{clk} is the switching frequency, C is the capacitance; V_{rect} is the output voltage of AC/DC converter V_{out} is the output voltage of DC/DC. The DC/DC input impedance will be a very important key to get the MPPT of the designed circuit. The DC/DC input impedance will be as:

$$R_{in} = \frac{1}{f_{clk}\left[\left(4 - \frac{Vout}{Vrect}\right)\frac{4C}{3} + \frac{\beta}{Vrect}\right.} \quad (3.8)$$

The input impedance is inverse proportional to the switching frequency of DC/DC. The DC/DC charge pump acts as a variable resistance changing its value by changing the desired frequency, finding the relation between the dc input voltage and the frequency enables us to get the maximum power point tracking.

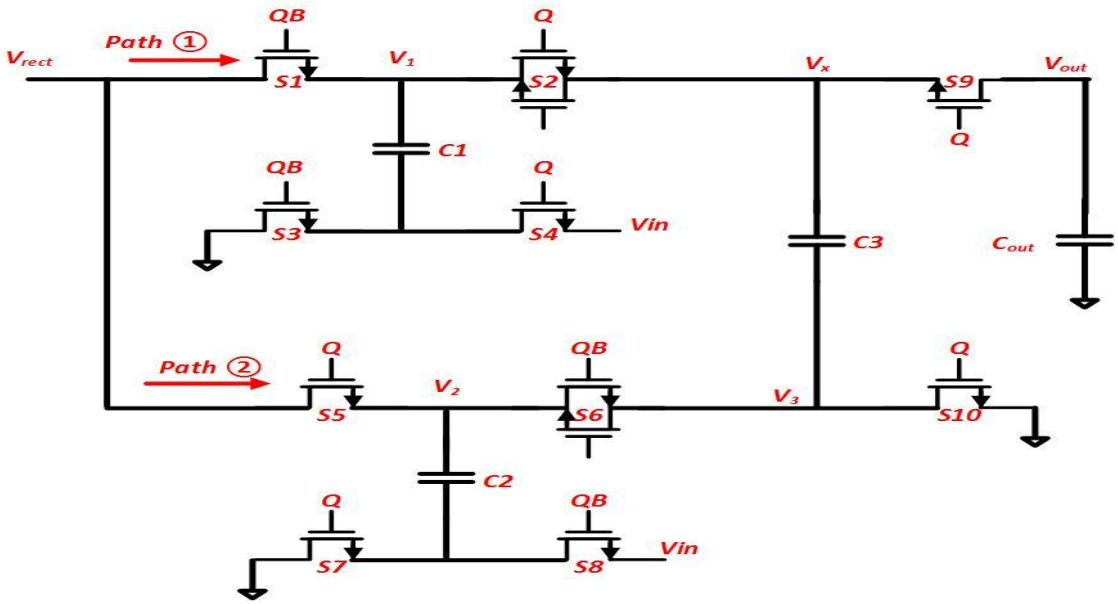

Figure 3.21 The DC/DC circuit. [34]

The sizes of all devices used in the DC/DC converter is shown in Table 3.4

Table 3.4: Size of devices in the DC/DC

Device	size
S1,S3,S4,S5,S7,S8.S10	0.45 µm/0.13 µm
S2,S6,S10	0.90 µm/0.13 µm
C1,C2,C3	300pF

3.4 Simulation results

The AC/DC converter and DC/DC converter is simulated by using cadence spectre with 130nm CMOS technology. Table 3.5 shows that for different input signals at the switching frequency of the DC/DC =0 Hz, the input of DC/DC is equal to the open-circuit voltage of AC/DC; changing F_{clk} will get the MPPT of the input signal. Figure 3.22 shows the relation between V_{oc} and V_{MPPT} for the different input values.

Table 3.5 The relation of different input samples value and V_{MPPT} with F_{clk}

V_{in}(V)	0.3	0.4	0.5	0.6	0.7
V_{oc}(V) at F_{clk}=0	0.696	1.115	1.446	1.825	2.21
V_{MPPT}(V)	0.46	0.796	0.895	1.0557	1.17
F_{clk}(KHz)	57	74	83	110	132

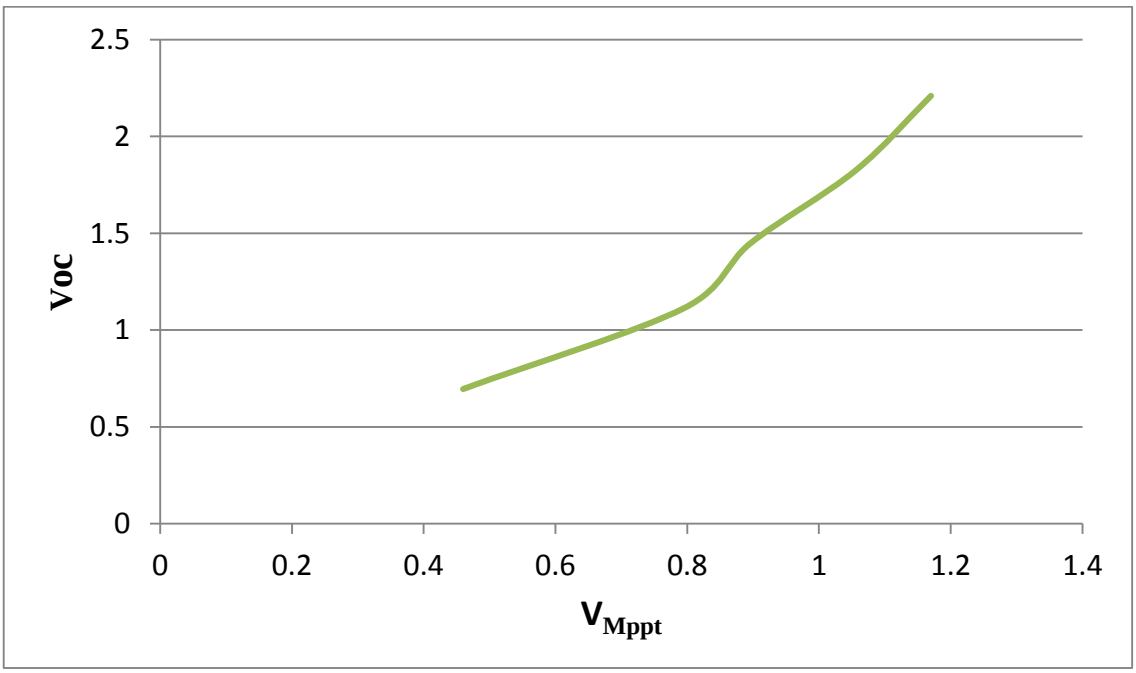

Figure 3.22 The relation of Voc and VMPPT for different input samples value.

Figure 3.23 shows the relation between V_{rect} and V_{out} for the input peak value 500mV the rectifying voltage will be 800mv and the output of the DC/DC converter will be 1.8V

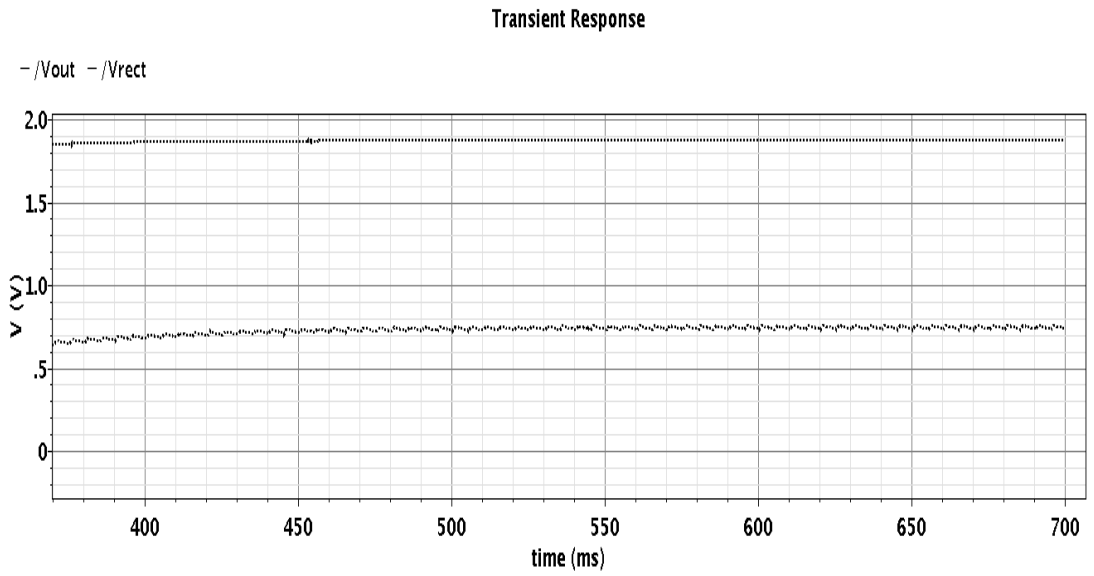

Figure 3.23 The relation of V_{rect} and V_{out}.

Figure 3.24 shows the relation between the output voltage of the AC/DC converter and the switching frequency of the DC/DC converter for different input samples value.

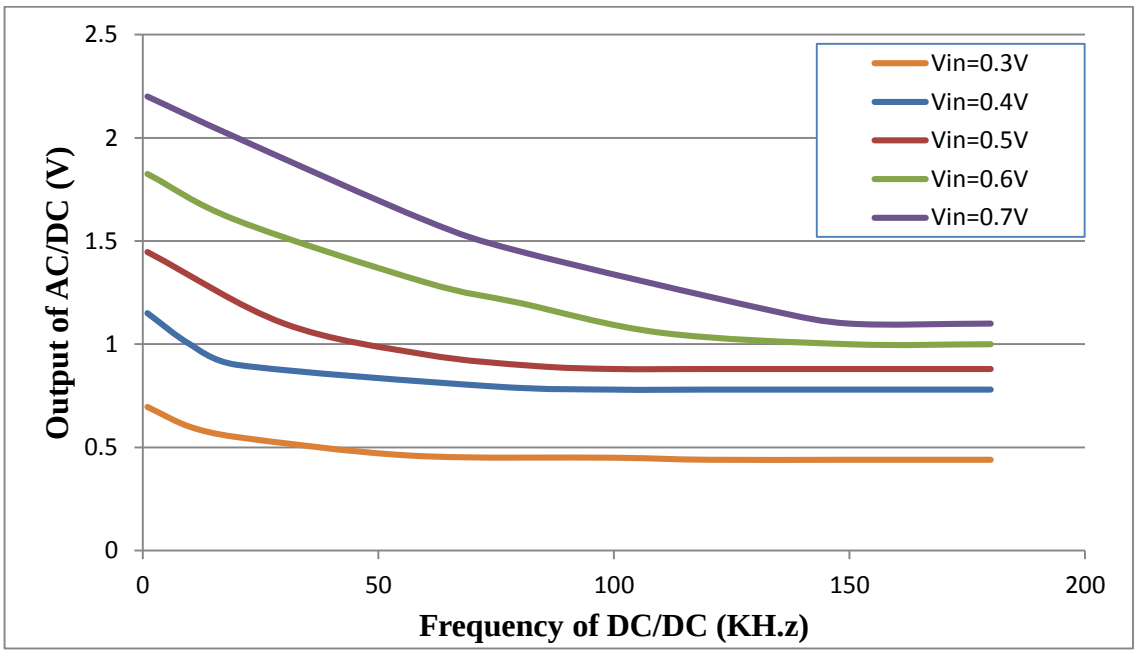

Figure 3.24 The relation between output voltage of AC/DC converter and the frequency of the DC/DC charge pump

The DC/DC charge pump chip layout occupies an active area of 8.80µm*8.90µm as shown at Figure 3.25.

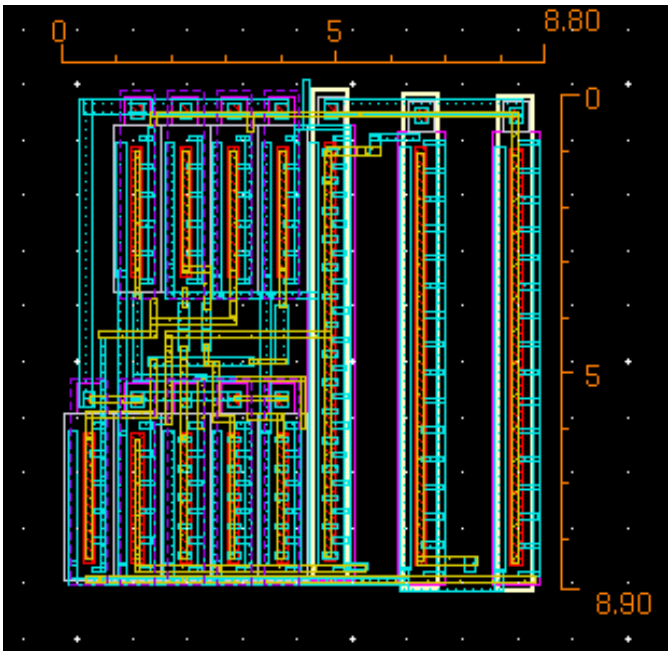

Figure 3.25 Charge pump layout

3.5 A MPPT digital circuit

In recent years, a large number of techniques have been presented for the maximum power point tracking (MPPT), such as the perturb and observe method (P&O) [35-36], the incremental conductance method (IncCond) [37], artificial neural networks (ANN) [38], or fuzzy logic (FL) [39-40].

In P&O strategy, in this method an increase in voltage or current is done then the power is measured, if there is an improvement in measured power over the last state the next step of increasing would be perturbed, otherwise, the converter starts decreasing the voltage/current. The disadvantages of this strategy makes that the system oscillate around the MPP, by using the incremental conductance strategy this situation is corrected, This method tracks the MPP by changing the voltage and current supplied to the load and measuring the instantaneous and incremental conductance periodically to reach the minimum value of the two parameters but it maintains the fixed-step.

In the case of systems based on ANN and FL, the performance of the algorithms depend on the ability of the designer to work well, besides Neural Networks must be adapted when there are changes in the system. The use of a variable-step to calculate the increment in the MPPT control shows a good performance, but in this type of algorithm is necessary to correctly determine the size of the increment or decrement of current, high complexity is the major drawback for such strategies. The fundamental principle of predictive control is to use the actual inputs of the system to pre-calculate the optimal

action for the next state. The major advantage of predictive control is its simple and comprehensive design procedure.

The comparison of MPPT algorithm in case of using the piezoelectric transducer shows in table 3.6

Table 3.6 Comparison of different MPPT algorithms.

Ref.	[41] 2019	[42] 2014	[43] 2013	[44] 2012	[45] 2013
Technology	0.13µm	0.35µm	0.25µm	Off-chip	0.25µm
Harvester	Piezoelectric	Piezoelectric	Piezoelectric	Piezoelectric	Piezoelectric
MPPT Algorithm	P&O	Fraction V_{oc}	Variable step - P&O	P&O	Variable step - P&O

This section is presenting a detailed explanation for the maximum point power tracking for piezoelectric energy harvesting systems. The idea of this technique depended on studying the piezoelectric characteristics. This study is based on connecting the piezoelectric to the AC/DC converter that converts the AC power to DC power.

The DC/DC optimizes the match between the output voltage of the AC/DC converter and voltage of batteries by converting a higher voltage DC output from AC/DC converter down to the lower voltage needed to charge batteries. The DC/DC charge pump acts as a variable resistance changing its value by changing the desired frequency, finding the relation between the dc input voltage and the frequency enables us to get the maximum power point tracking between the piezoelectric transducer that changes due to the vibration of piezoelectric transducer and voltage of batteries.

The control unit provides the desired switching frequency with enough capability to drive the charge pump power that will change its resistance based on this switching frequency consists of analog to digital converter and digital control oscillator.

3.5.1 Analog to digital converter

Analog to Digital Converter (ADC) helps us to communicate between analog signals to digital signals. The resolution, conversion rate, power dissipation, the die area, and the input impedance are some of the common parameters to evaluate ADCs. A figure of merit (FOM) is a useful tool for comparing the conversion efficiency of A/D converters. We will only consider the three primary metrics, which are the resolution, the conversion rate, and power dissipation to construct a useable figure of merit. The popular FOMs that is used to find a good relationship that describes the trade-off between resolution and power dissipation, and conversion rate and power dissipation.

Walden FOM [46] is widely used, which is defined as

$$FOM_w = \frac{P}{F_s.2^{ENOB}} \tag{3.9}$$

Where P is the power dissipation, fs is Nyquist sampling rate, and ENOB is the effective number of bits defined by the signal to noise and distortion ratio (SNDR) as

$$ENOB = \frac{SNDR-176}{6.02} \quad (3.10)$$

Schreier FOM [47] is given as;

$$FOM_{S.DR} = DR + 10\log(\frac{BW}{P}) \quad (3.11)$$

According to Schreier FOM, energy increases 4x per bit (DR). It also ignores the distortion.

Schreier FOM includes distortion [48] is given as;

$$FOM_s = SNDR + 10\log(\frac{fs/2}{P}) \quad (3.12)$$

There are many surveys of ADC are presented to provide a clear perspective on various aspects of ADCs [49-50]. In this section, five types [51] of ADCs architectures have been compared. These five types ADCs are flash ADC, Sigma-Delta ADC, Successive approximation ADC, Pipeline ADC and Folding –Interpolation ADC. SAR is used due to lower power consumption and small size in compared with others, it also has medium to high resolution while Flash has the highest power consumption and sigma-Delta has the highest resolution .The disadvantage of SAR its limited speed. SAR ADC ideal for wide variety of applications, such as portable/battery –powered instruments. The Encoding method of SAR is the successive approximation register.

The Successive-approximation-register (SAR) as shown in Figure 3.26 based on a binary search. Sample and hold circuit samples the analog input signal of the AC/DC converter, and holds it until the conversion period finishing. While the comparator compares the output of the digital to the analog circuit with the output of the sample and hold circuit and its output will feed to successive approximation register, by using the charge redistribution circuit as shown in Figure 3.27, we can apply the sample and hold circuit and DAC, while the SAR control circuit imposes by the Verilog A code as mentioned in Appendix A. By the end of conversion, we will have a digital output of the AC/DC converter.

The principle of operation is shown in Figure 3.28 as the following: at the initial clock cycle Q_0 the input is sampled. While at the next clock cycle Q_1 the voltage of digital to analog converter $V_{DAC}= V_{ref}-V_{in} +V_{ref}/2$ with V_{ref} and the comparator output is high, and so on. The voltage of digital to analog converter $V_{DAC}= V_{ref}-V_{in} +V_{ref}/2 +V_{ref}/4$ compared with V_{ref} at clock cycle Q_2 and therefore the comparator output is still high. While at the third clock cycle Q_3 V_{ref} compared with $V_{DAC}=V_{ref}-V_{in}+V_{ref}/2+V_{ref}/4-V_{ref}/8$ and the comparator output is low.

The voltage $V_{DAC}= V_{DAC}=V_{ref}-V_{in}+V_{ref}/2+V_{ref}/4-V_{ref}/8+V_{ref}/16$ compared with V_{ref} and the comparator output is high at Q_4, at the fifth clock cycle Q_5 $V_{DAC}= V_{ref}-V_{in}+V_{ref}/2+V_{ref}/4-V_{ref}/8+V_{ref}/16 +\underline{V_{ref}}/32$ compared with V_{ref} and therefore the output of the comparator is high. The comparator output is low at Q_6 as the result of the comparison between $V_{DAC}= V_{ref}-V_{in}+V_{ref}/2+V_{ref}/4-V_{ref}/8+V_{ref}/16+V_{ref}/32-V_{ref}/64$ and $V_{ref.}$

At the next clock cycle Q_7, the voltage of digital to analog converter $V_{DAC}= V_{ref}-V_{in}+V_{ref}/2+V_{ref}/4-V_{ref}/8+V_{ref}/16+V_{ref}/32-V_{ref}/64+V_{ref}/128$ compared with V_{ref} and therefore the comparator output is high. The comparator output is low at Q_8 as the result of the comparison between V_{ref} and V_{DAC}.

The digital output will be (10110110) for the analog input voltage 0.5V, as shown in Figure 3.29. Figure 3.30 shows that for the analog input voltage 200mV, the digital output will be (010010011). The resolution of SAR will be 2^8 that can resolve 256 levels. The least significant bit in case of an 8 bit is 1/256. To convert the least significant bit into a voltage we take the input range of ADC and divide by the resolution. Table 3.7 shows the least significant bit for a one volt for different input resolution of 3 to 8 bits.

Table 3.7 Steps and resolution

Resolution	The least significant bit	Minimum Voltage step
3 Bit	1/8	125 mV
4 Bit	1/16	62.5 mV
5 Bit	1/32	31.25 mV
6 Bit	1/64	15.625 mV
7 Bit	1/128	7.812 mV
8 Bit	1/256	3.906 mV

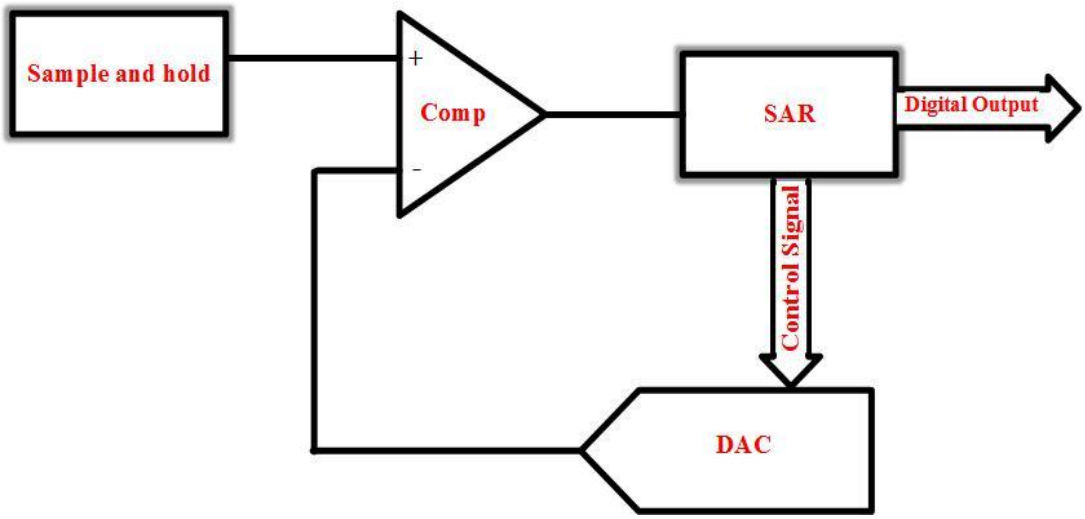

Figure 3.26 The successive approximation register (SAR).

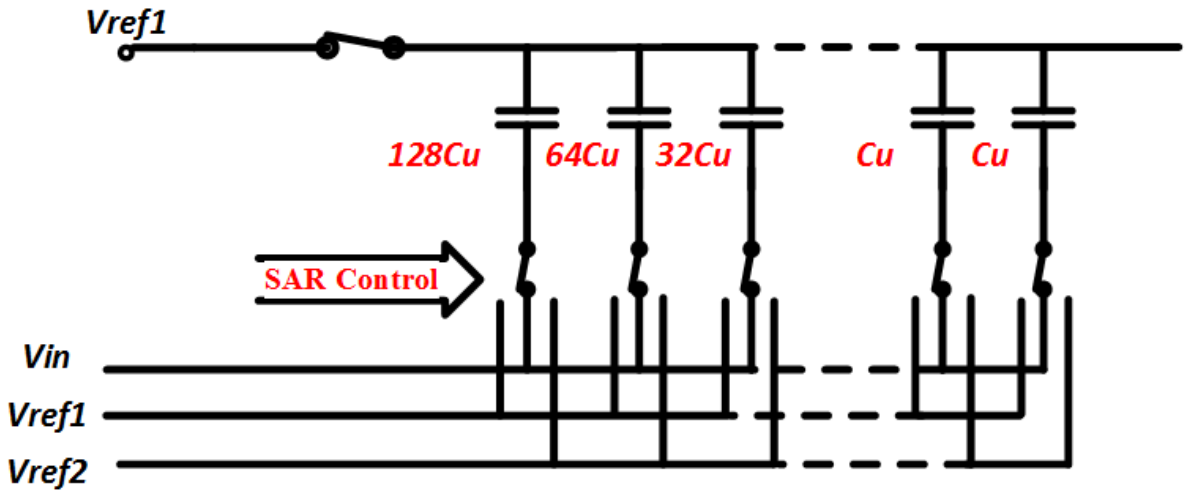

Figure 3.27 Implementation of charge redistribution circuit.

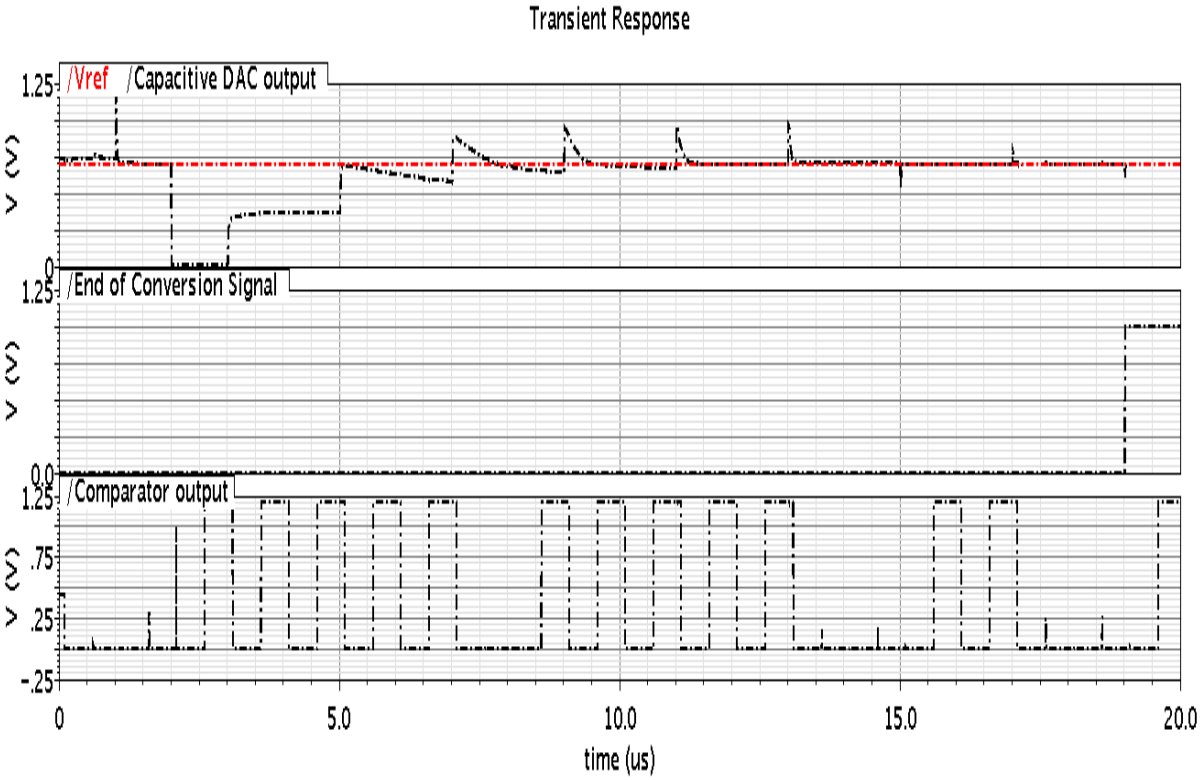

Figure 3.28 The operation of SAR.

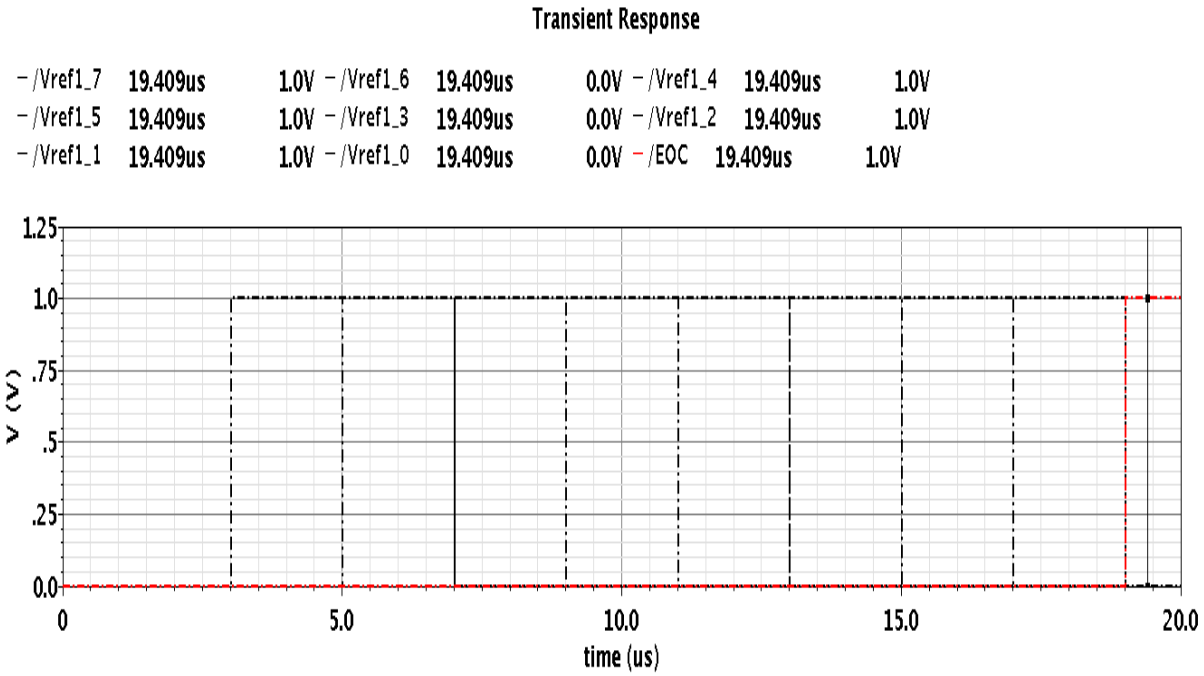

Figure 3.29 Binary search of ADC for 0.5V.

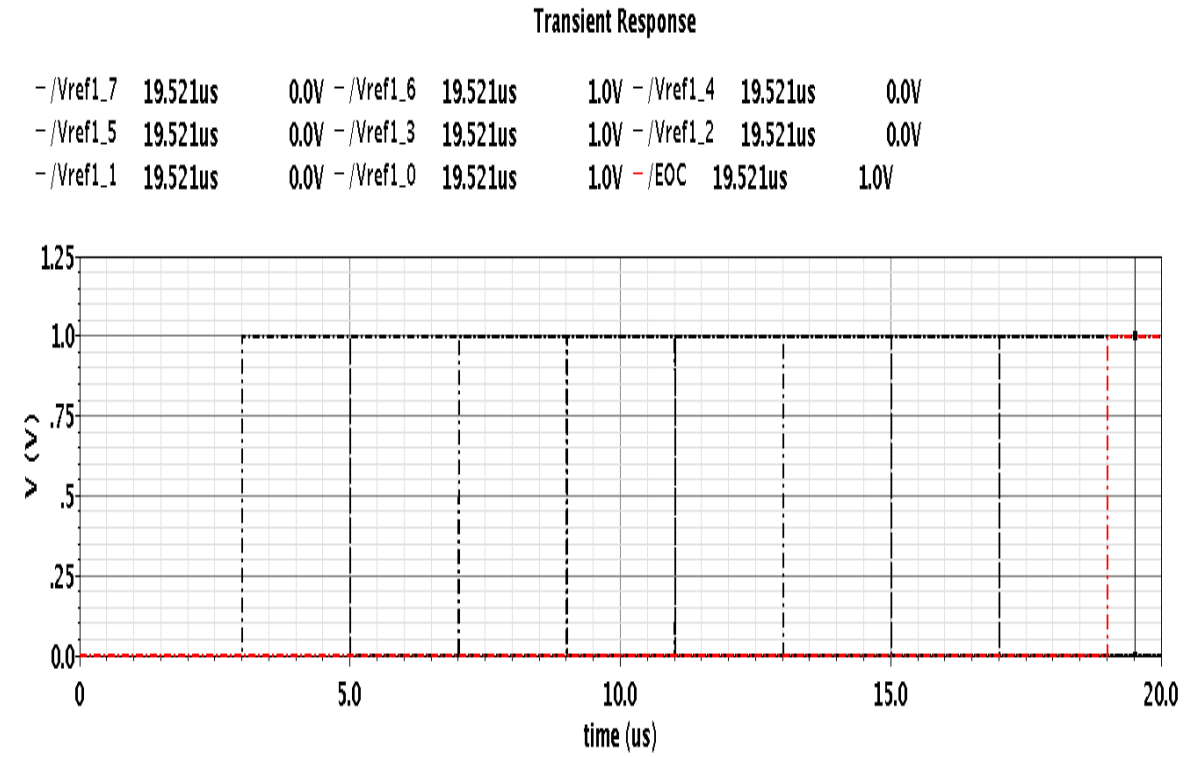

Figure 3.30 Binary search of ADC for 200mV.

Table 3.8 shows the analog signal samples and corresponding digital signal and the error of SAR ADC circuit for analog signal 0V the digital signal (00000000) while for analog signal 200mV the digital signal (01001001) and the actual signal should be (1/2+1/16+ 1/128) around 199.60mv and the error will be 0.001.

Table 3.8 The analog signal samples, digital signal corresponding and the error

Analog Signal	Digital signal	Actual signal	The error
0	00000000	0	0
100mV	00100101	99.998mV	0.001
200mV	01001001	199.60mV	0.0004
300mV	01101101	298.04mV	0.0019
400mV	10010010	399.218mV	0.0007
500mV	10110110	497.65mV	0.002
600mV	11011010	596.09mV	0.003
700mV	11111110	694.53mV	0.005

Table 3.9 compares the designed SAR ADC performance with state of the art realizations ADCs. The power can be decreased by the use of a smaller unit capacitance. Figure 3.31 shows that active area layout for SAR ADC.

Table 3.9 Performance comparison with State of the art implementations

	Vijay [52] 2013	**Liu [53] 2016**	**ISSCC [54] 2015**	**This work 2019**
Technology	90nm	28nm	65nm	130nm
supply	1.2 V	0.9 V	1.2 V	1.2 V
Input range	-	1.6	2.4	2.4
Sampling rate	250Ms/s	100Ms/s	50Ms/s	1Ms/s
Unit cap.	-	0.9pF	2pF	5fF
Power Cons.	1.49mW	0.35mW	1mW	18µW
Area	-	0.0047mm^2	0.054mm^2	0.0124mm^2
architecture	Single ended	SAR – assisted digital slope	SAR-assisted Pipeline	Single ended

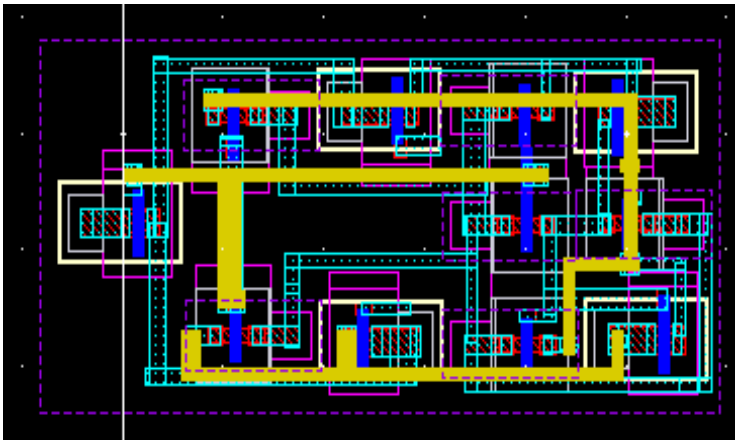

Figure 3.31 SAR ADC active area layout

3.5.2 Digital control oscillator

Traditionally, phase locked loops (PLLs) [55] are considered analog circuit, thus inherently are susceptible to process vibration and noise. We need to redesign when we moved from certain technology to another. To overcome the mention problems the digitalization phase looked loops took place. All digital phase looked loops (ADPLL) [56] promises less noise, fast locking control algorithms, easy to reuse when technology changed. The efforts of current research are focused on lowering supply voltage, power dissipation and occupied area. Table 3.10 shows the improvement in power consumption in the last decade. As the power consumption is very important key in portable devices.

A straightforward implementation of digitally controlled oscillator (DCO) can be implemented by combining a digital to analog converter (DAC) and a voltage controlled oscillator (VCO) .The DAC takes a binary control word and converts it into a voltage, which in turn drives the VCO to generate the needed oscillation frequency. Table 3.11 compares low voltage VCOs and DCOs in terms of their performance.

Table 3.10 Comparisons of power consumption in DCO implementation

Ref.	**Algorithms**	**Achievements mW**
[57] 2004	Shunt capacitor technique	1
[58] 2003	Uses a bank of tri-state inverter buffers	164
[59] 2003	Uses inverter ring	100
[60] 2005	Uses digitally controlled varactor (DCV)	18
[61] 2008	Base on a ring oscillator implemented with Schmitt trigger based inverters	2.3
[62] 2012	Driving strength controlled delay with two NAND gates as inverters	0.7
[63] 2011	Low power Schmitt trigger inverters	0.56

Table 3.11 Comparisons of power consumption and frequency range

Ref.	Technology	VDD	Frequency range	Power
[64] 2015	130nm	0.7V	382-412 MHz	840µW
[65] 2011	90nm	0.5V	0.16-1.5 GHz	1157µW
[66] 2013	180nm	1.2V	3.6-3.9 GHz	570 µW
[67] 2018	180nm	1.8V	0.09-3.7 MHz	105 µW
[68] 2017	65nm	0.6V	46.2-147 MHz	77.3µW
[69] 2013	90nm	0.5V	176-480 MHz	400µW

The DCO implemented using Verilog coding (Appendix B). Figure 3.32 shows that the simulation of the DCO when the input signal is (11011010), the clock frequency is 109.700 kHz. Another simulation is shown in Figure 3.33 for the input (01101101), and the clock frequency is 57.6 kHz.

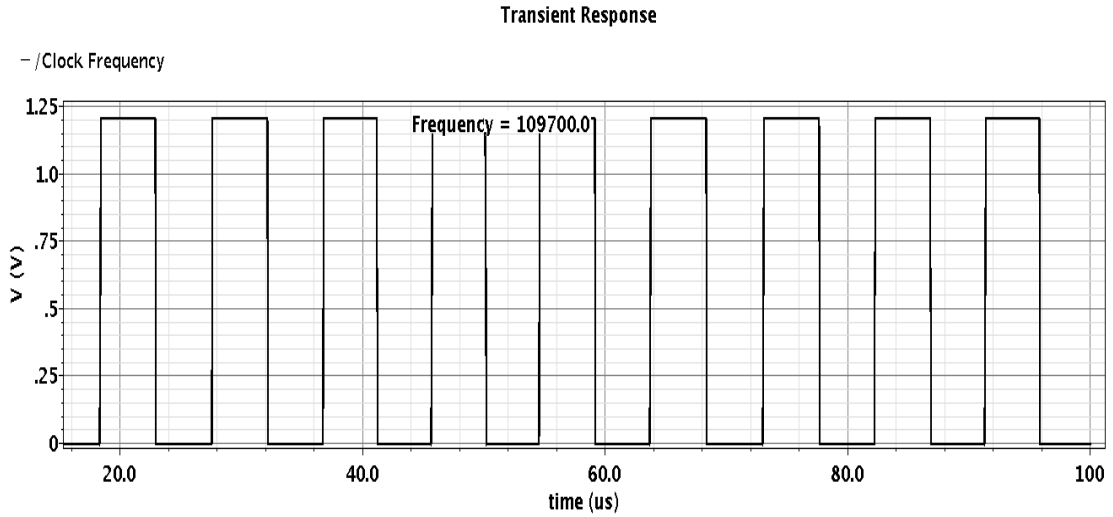

Figure 3.32 Simulation of DCO when the input signal is (11011010), the clock frequency is 109.700 KHz.

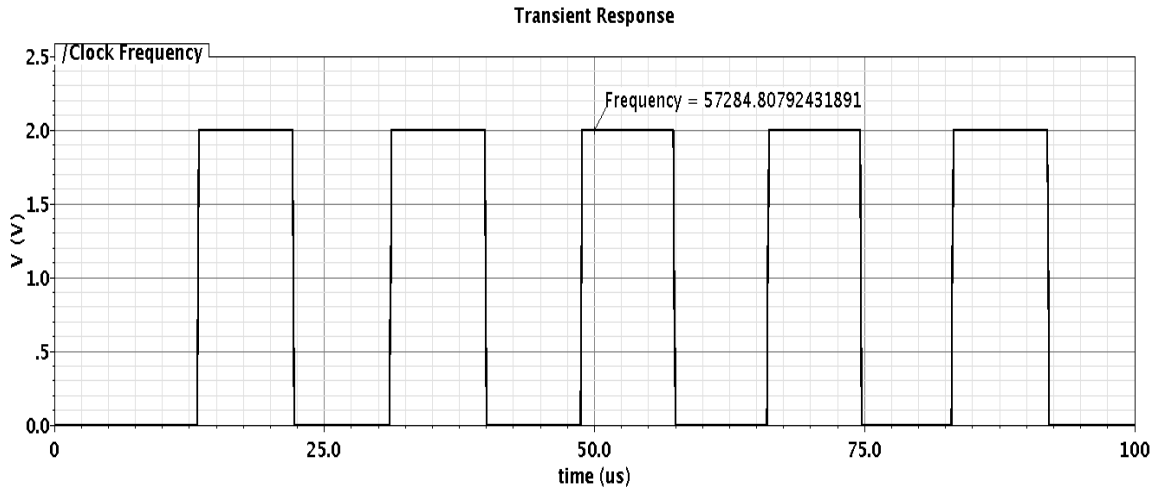

Figure 3.33 Simulation II for DCO for the input (01101101),
The clock frequency is 57.6 KHz.

The digital output of the SAR ADC converter which in turn drives the DCO to generate the desired clock based on the values of the input signal to get the MPPT for our transducer. Table 3.12 shows the analog input samples of AC/DC and the corresponding MPPT value by changing the input resistance of DC/DC circuit, the digital signal generated by the SAR ADC circuit, and the frequency of DCO that controls the DC/DC.

Table 3.12 Summary samples value of each sub-blocks of the system

Input(V)	MPPT(V)	SAR ADC	Frequency of DCO(KHz)
0.3	0.46	01101101	57
0.4	0.796	10010010	74
0.5	0.895	10110110	83
0.6	1.0557	11011010	110
0.7	1.17	11111110	132

The contribution of this work "a design of an energy harvesting system using the piezoelectric transducer and sub-circuits," compared with the recent researches using the same technique. Table 3.12 shows the performance metrics of our proposed design and other designs that used solar transducer. It can be illustrated that the proposed approach achieves promising results with maximum power efficiency reach to 70% with minimum input range between 300:700mV.

Table 3.12 Performance metrics of the proposed design

Design Metric	**VLSID [70] 2012**	**NEWCAS [71] 2015**	**Proposed Design[72]**
Transducer	Solar	Solar	Piezo
Control Frequency	8.8MHz:21.9MHz	1.06MHz:6.11MHz	57KHz:132KHz
Input voltage range	632mV:742mV	613mV:714mV	300mV:700mV
Maximum Input power	424µW:2.138mw	276µW:3.13mW	12µW:108µW
Maximum Power Efficiency	51%	58%	70%
Energy Buffer Voltage	1.8V	1.8V	1.8V
Size	-	-	0.249mm^2

Chapter 4

4.1Conclusion

A survey about several active AC-DC converter circuits that used active diodes such as negative voltage converter with active diode, cross-coupled active full-bridge, and active bridge voltage doubler to perform signal rectification is done. Our study shows that the active AC-DC converter is the most efficient and can work at minimum input voltage. The proposed AC/DC converter works with an input voltage range from 0.2V to 0.7V with a frequency range 20- 1K Hz and its output DC voltage range from 0.5V to 2.2V. The maximum power efficiency achieved is 83% and the circuit layout 0.2mm^2.

The maximum power point tracker is an electronic DC/DC converter that optimizes the match between the output voltage of the AC/DC converter and batteries' voltage by reducing the higher voltage DC output from AC/DC converter to the lower voltage which needed to charge batteries. At the switching frequency of the DC/DC converter equals 0 Hz, the input of the DC/DC converter is very high, so the output of the AC/DC converter equal to the open-circuit voltage, changing F_{clk} by using an external clock. We found the corresponding frequency that enables us to will get the MPPT of the input signal. The DC/DC charge pump acts as a variable resistance changing its value by changing the desired frequency, finding the relation between the dc input voltage and the frequency enables us to get the maximum power point tracking between the energy harvesting by piezoelectric that changes due to the vibration of piezoelectric transducer and voltage of batteries.

The control unit provides the desired switching frequency consists of analog to digital converter and digital control oscillator. The analog to digital converter used is the successive approximately register due to low latency, low power consumption, and small area. Sample and hold circuit samples the analog input signal of the AC/DC converter from 0V to 700mV, and holds it until the conversion period finishing. By the end of conversion, we will have a digital output for the AC/DC converter from 00000000 to 1111111. The DCO implemented using synthesized Verilog coding generates the desired clock to get the MPPT for our transducer.

The proposed energy harvesting system using piezoelectric transducer with input ac voltage range from 0.2 to 0.7 V, with energy buffer voltage 1.8V and frequency of DC/DC will generate by using DCO and the total size circuit is 0.249mm^2.

4.2 Recommendation for the future work

Recommendation for the future work of this study can be categorized for different scopes. We plan to use triboelectric nanogenerators (TENGs) [73] instead of piezoelectric transducer as the triboelectric nanogenerators (TENGs) are considered a very promising technique for harvesting mechanical energy due to its ease of fabrication, relatively cheap materials, large output power and high conversion efficiency compared to other techniques such as those relying on piezoelectric and electromagnetic effects.

AC/DC converter should be redesigned to work with the high voltage provided by TENGs as shown in Figure 4.1 by using different material we have high output voltage and current. We need to design a DC/DC circuit with improved power efficiency as the charge pumps switched capacitor its power efficiency cannot reach 100% due to the structure of the converter itself.

The DCO should design at the circuit level instead of DCO verilogA code to be more realistic and compare with the recent research. The area layout should be resized for fitting the chip into the human body for future use. Besides, the new design technique will lead to improving the power efficiency of the energy harvesting system. The MPPT of circuit can design depending on the relation between the V_{MPPT} and the open circuit voltage $V_{oc,}$ V_{MPPT}=0.5Voc

Conventional TENGs are withheld due to the requirements of a rectifier circuit. Direct current triboelectric nanogenerator [74-75] is designed for harvesting energy without the need of AC/DC rectifier This DC-TENG may open up new avenues for further fundamental research and experimental development of DC energy harvesting systems used in various scenes including large-scale energy harvesting and flexible electronics.

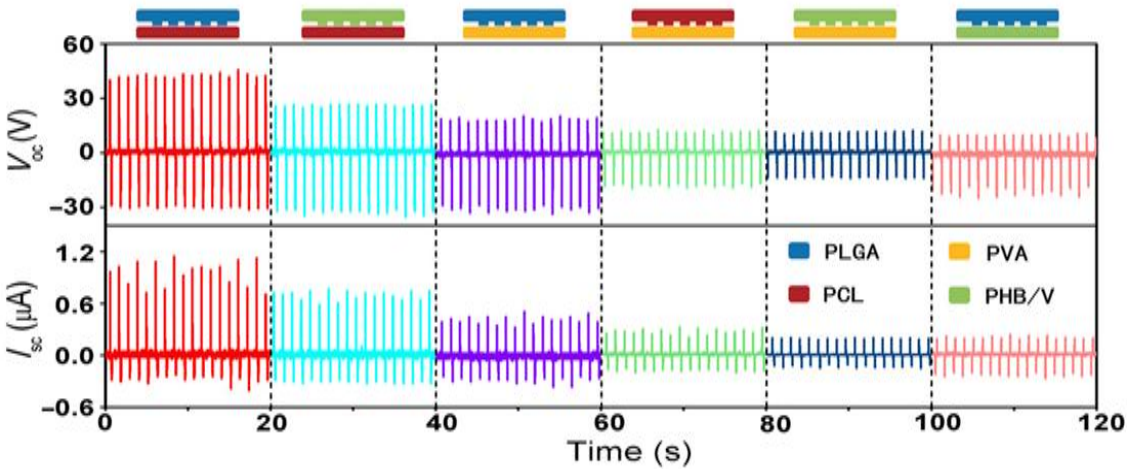

Figure 4.1 The output voltage and current of TENG by changing the materials of friction layers [76]

References

[1]Vijay Raghunathan, AmanKansal, Jason Hsu, Jonathan Friedman, and Mani B. Srivastava, "Design considerations for solar energy harvesting wireless embedded systems", in Proceedings of 4th International Symposium on Information Processing in Sensor Networks (IPSN 2005), pp. 457-462,2005.

[2]M. Penella-Lopez and M.Gasulla-Forner, "Powering Autonomous Sensors", Springer, 2011.

[3] A. Boyer and E. Cisse, "Properties of thin _lm thermoelectric materials:Application to sensors using the seebeck effect", Materials Science and Engineering B, vol. 13, no. 2, pp. 103-111, March 1992.

[4] Chao Lu, "Efficient Design for Micro-Scale Energy Harvesting Systems", PhD thesis, Electrical and Computer Engineering, Purdue University, West lafayette, Indiana, USA, 2012.

[5] J. Damaschke, "Design of a low-input-voltage converter for thermoelectric generator", IEEE Transactions on Industry Applications, vol. 33, no. 5, pp. 1203–1207, September 1997.

[6] S. Lineykin and S. Ben-Yaakov, "Modeling and Analysis of Thermoelectric Modules", IEEE Transactions on Industry Applications, vol. 43, no. 2, pp. 505–512, March-April 2007.

[7] Chao Lu, "Efficient Design for Micro-Scale Energy Harvesting Systems", PhD thesis, Electrical and Computer Engineering, Purdue University, West lafayette, Indiana, USA, 2012.

[8] M. Renaud, T. Sterken, A. Schmitz, P. Fiorini, C. Van Hoof, and R. Puers, "Piezoelectric harvesters and MEMS technology: Fabrication, modeling and measurements,", Int. Solid-State Sensors, Actuators and Microsystems Conf., pp. 891–894,2007.

[9] Bashirullah R., et al., "A Smart Bi-Directional Telemetry Unit for Retinal Prosthetic Device," Proc. Int'l Symp Circuits and Systems (ISCAS), vol. 5, pp. V-5-V-8, 2003.

[10] Y. Jeon, R. Sood, J. H. Jeong, and S.-G. Kim, "MEMS power generator with transverse mode thin film PZT," *Sensors and Actuators A: Physical*, vol. 122, no. 1, pp. 16–22, 2005.

[11] Ramadass, Y.K., and A.P. Chandrakasan. "An EfficientPiezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor." Solid-State Circuits, IEEE Journal, pp. 189-204, 2010.

[12] L. Chao, C.-Y. Tsui, and W.-H. Ki, “A batteryless vibration-based energy harvesting system for ultra-low power ubiquitous applications,” Microelectronics and Electronics (PRIME), pp. 1349–1352, May 2007.

[13] Fu Q., et al., “Optimization for the NMOS and PMOS Gate Cross-Connected Rectifier for RF Power Extraction in RFID Applications,” Asia-Pacific Microwave Conf. (APMC), pp. 1-4, China, 2008.

[14] Facen A., and Boni A., “Power Supply Generation in CMOS Passive UHF RFID Tags,” Research in Microelectronics and Electronics, pp. 33-36 ,2006.

[15] Lehmann T., and Moghe Y., “On-Chip Active Power Rectifiers for Biomedical Applications,” Circuits and Systems (ISCAS), vol. 1, pp. 732-735, 2005.

[16] Niu, D.; Zhangcai Huang; Minglu Jiang; Inoue, Y. “Asub-0.3VCMOS rectifier for energy harvesting application,” Circuits and Systems (MWSCAS), pp.1-4, Aug. 2011.

[17] Ehab Belal, Hassan Mostafa, and M. Sameh Said, "Comparison between active AC-DC converters for low power energy harvesting systems", International Conference on Microelectronics *(*ICM*)*, pp. 253-256, Dec. 2015.

[18] Yang Sun, In-young Lee, Chang-jinJeong, Seok-kyun Han, Sang-gug Lee “An Comparator Based Active Rectifier for Vibration Energy Harvesting Systems." Advanced Communication Technology (ICACT) 13th International Conference, pp. 1404 – 1408, Feb 2011.

[19] Hashemi, S.S.; Sawan, M.; Savaria, Y. “A High-Efficiency Low Voltage CMOS Rectifier for Harvesting Energy in Implantable Devices"Biomedical Circuits and Systems, IEEE Transactions Vol.6, NO. 4, pp. 326 – 335, Aug. 2012.

[20] Rao, Yuan; Arnold, David P “An AC/DC voltage doubler with configurable power supply schemes for vibrational energy harvesting" Applied Power Electronics Conference and Exposition (APEC), pp. 2844 – 2851, March 2013.

[21] Rahimi, A.; Zorlu, O.; Muhtaroglu, A.; Kulah, H“Fully Self-Powered Electromagnetic Energy Harvesting System with Highly Efficient Dual Rail Output "IEEE SENSORS JOURNAL VOL. 12, NO. 6, pp. 2287 – 2298, June 2012.

[22] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier techniques", *IEEE J. Solid-State Circuit*, vol. 11, pp. 374-378, 1976.

[23] F. Ueno, T. Inoue, I. Oota and I. Harada, "Emergency power supply for small computer systems", *IEEE Int. Symp. Circuits and Syst.*, pp. 1065-1068, 1991.

[24] Hui Shao, Chi Y. Tsui, and Wing H. Ki, “A micro power management and maximum output power control for solar energy harvesting applications", International Symposium on Low Power Electronics and Design, pp. 298-303, 2007.

[25] Lee Sanghoey CH,"Design and implementation of photovoltaic power conditioning system using a current based maximum power point tracking", ICSET,pp. 295–300, 2008.

[26] Yuvarajan S, XuS,"Photovoltaic power converter with a simple maximum power point tracker", Circuits System, pp. 399-402, 2003.

[27] Bhatnagar P, Nema RK," Maximum power point tracking control techniques: State of the art in photovoltaic applications", Renewable and Sustainable Energy Reviews Sci Verse Science Direct, pp. 224–241, 2013.

[28] NisaNacarÇikan , Murat Aksoy, " Anolog to Digital Converters Performance Evaluation using Figure of Merits In Industrial Applications," IEEE European Modelling Symposium (EMS),2017.

[29] Ehab Belal, Hassan Mostafa, Yehea Ismail, and M. Sameh Said, "A voltage multiplying AC/DC converter for energy harvesting applications", International Conference on Microelectronics (ICM), pp. 229-232, 2016.

[30]Shuo Cheng, Ying Jin, Yuan Rao, and David P.Arnold, "An Active Voltage Doubling AC/DC Converter for Low-Voltage Energy Harvesting Applications," IEEE Transactions on Power Electronics, vol.26, no.8, pp. 2258-2265,2011.

[31] HasanUlusan, KavehGharehbaghi, OzgeZorlu, and Ali Muhtaroglu, "A Self-powered rectifier circuit for low-voltage energy harvesting applications," International Conference on Energy Aware Computing, pp. 1-5, Dec.2012.

[32] HasanUlusan, KavehGharehbaghi, OzgeZorlu, Ali Muhtaroglu Yang, and HalukKulah, "An efficient integrated interface electronics for electromagnetic energy harvesting from low voltage sources," International Conference on Solid-State Sensors, Actuators and Microsystems, pp.450-453, 2013.

[33] HasanUlusan, OzgeZorlu, Ali Muhtaroglu, and HalukKulah, "A self-powered and efficient rectifier for electromagnetic energy harvesters," IEEE Sensors Proceedings, pp. 182-185, 2014.

[34] Eltaliawy, A., H. Mostafa, and Y. Ismail, "A New Digital Locking MPPT control for Ultra Low Power Energy Harvesting Systems", IEEE International Conference on NEW Circuits and Systems (NEWCAS 2015), Grenoble, France, pp. 1-4, 2015.

[35] Boualem Bendib, Hocine Belmili, Fateh Krim, "A survey of the most used MPPT methods: Conventional and advanced algorithms applied for photovoltaic systems", Renewable and Sustainable Energy Reviews, Vol 45, pp. 637–648, May 2015.

[36] R. Khanaki, M. A. M. Radzi, M. H. Marhaban "Comparison of ANN and P&O MPPT methods for PV applications under changing solar irradiation" in Clean Energy and Technology (CEAT), IEEE Conference, pp. 287 – 292, 2013.

[37] S. Zahra Mirbagheri, S Mekhilef, S. M. Mirhassani, “MPPT with Inc.Cond method using conventional interleaved boost converter”, Proceedings of an International Conference MGEF-13, vol 42, pp. 24–32, 2013 .

[38] R. Khanaki, M. A. M. Radzi, M. H. Marhaban, “Comparison of ANN and P&O MPPT methods for PV applications under changing solar irradiation”, in Clean Energy and Technology (CEAT), pp. 287 – 292, 2013.

[39] A. Kargarnejad, M. Taherbaneh, and A. H. Kashefi, “A New Fuzzy-Based Maximum Power Point Tracker for a Solar Panel Based on Datasheet Values” ,International Journal of Photoenergy, 2013.

[40] M. Z. Alabedin, E. F. El-Saadany, and M. M. A. Salama, “Maximum power point tracking for Photovoltaic systems using fuzzy logic and artificial neural networks,” in Power and Energy Society General Meeting, pp. 1 –9. July 2011.

[41] Shuo Li ; Abhishek Roy ; Benton H. Calhoun, “A Piezoelectric Energy-Harvesting System with Parallel-SSHI Rectifier and Integrated MPPT Achieving 417% Energy-Extraction Improvement and 97% Tracking Efficiency”, Symposium on VLSI Circuits ,2019.

[42] Minseob Shim ; Jungmoon Kim ; Junwon Jung ; Chulwoo Kim, “23.7 Self-powered 30μW-to-10mW Piezoelectric energy-harvesting system with 9.09ms/V maximum power point tracking time”, International Solid-State Circuits Conference Digest of Technical Papers (ISSCC),2014.

[43] Chris van Liempd ; Stefano Stanzione ; Younis Allasasmeh ; Chris van Hoof, “ A 1μW-to-1mW energy-aware interface IC for piezoelectric harvesting with 40nA quiescent current and zero-bias active rectifiers”, IEEE International Solid-State Circuits Conference Digest of Technical Papers, 2013.

[44] N. Kong and D.S. Ha, “Low-Power Design of a Self-Powered Piezoelectric Energy Harvesting System with Maximum Power Point Tracking,” IEEE Trans. Power Electronics, vol. 27, no. 5, pp. 2298-2308, May 2012.

[45] S. Stanzione, C. van Liempd, R. van Schaijk, et al., “A Self-Biased 5-to-60V Input Voltage and 25-to-1600μW Integrated DC-DC Buck Converter with Fully Analog MPPT Algorithm Reaching up to 88% End-to-End Efficiency,” ISSCC Dig.Tech. Papers, pp. 74-75, Feb. 2013.

[46] R. H. Walden, “Analog-to-digital converter survey and analysis,” IEEE J. Selected Areas in Communications, no. 4, pp. 539–550, Apr. 1999.

[47] R. Schreier and G. C. Temes.” Understanding Delta-Sigma Data Converters”, New York, Wiley, 2005.

[48] A.M.A. Ali, et al., "A 16-bit 250-MS/s IF Sampling Pipelined ADC With Background Calibration," IEEE Journal of Solid-State Circuits, pp. 2602 – 2612,2010.

[49]https://web.stanford.edu/~murmann/adcsurvey.html , 1997-2015.

[50] Bin Le ; T.W. Rondeau ; J.H. Reed ; C.W. Bostian, "Analog-to-digital converters," IEEE Signal Processing Magazine, vol.22, no.6, pp. 67-77,2005.

[51]https://www.maximintegrated.com/en/design/technicaldocuments/tutorials/2/2094.html,2016.

[52] Vijay Pratap Singh, Gaurav Kumar Sharma, and Aasheesh Shukla, "Power efficient SAR ADC designed in 90 nm CMOS technology," 2nd International Conference on Telecommunication and Networks (TEL-NET), 2017.

[53] Chun-Cheng Liu, Mu-Chen Huang, and Yu-Hsuan Tu, "A 12 bit 100 MS/s SAR-Assisted Digital-Slope ADC " , IEEE Journal of Solid-State Circuits, pp. 2941-2950,2016.

[54] Y. Lim and M. P. Flynn, "A 1 mW 71.5 dB SNDR 50MS/S 13 b fully differential ring-amplifier-based SAR-assisted pipeline ADC," in ISSCC Dig. Tech. Papers, pp. 1–3, 2015.

[55] K. SHU and E. SANCHEZ-SINENCIO, "CMOS PLL Synthesizers: Analysis and Design", 1st ed. Springer Publishing Company, Incorporated, 2010.

[56] R. B. STASZEWSKI and P. T. BALSARA, "Phase-domain all-digital phase-locked loop", IEEE Transactions on Circuits and Systems II ,pp. 159–163, 2005.

[57] Olsson, T.; Nilsson, P, "A digitally controlled PLL for SoC application," IEEE journal of solid-state circuits, pp. 751-760,2004.

[58] Roth, E.; Thalmann, M.; Felber, N.; Fichtner, W, " A delay-line based DCO for multimedia applications using digital standards cells only", Proceedings of IEEE International Solid-State Circuits Conference (ISSCC), pp. 432-505, February 2003.

[59] Chung, C.; Lee, C, "An all-digital phase-locked loop for high-speed clock generation", IEEE Journal of Solid-State Circuits, pp. 347-351. 2003.

[60] Chen, P.-L.; Chung, C.-C.; Lee, C.-Y, "A portable digitally controlled oscillator using novel varactors.", IEEE transaction on circuits and systems, pp. 233-237,2005.

[61] Zhao, J.; Kim, Y, "A 12-bit digitally controlled oscillator with low power consumption", Proceedings of 51st Midwest Symposium on Circuits and Systems, pp. 370-373, 2008.

[62] Sheng, D.; Chung, C.-C.; Lan, J.-C.; Lai; H.-F., "Monotonic and low-power digitally controlled oscillator with portability for SoC applications" Electronics letters, pp. 321-323, 2012.

[63] Majd, N. E.; Lotfizad, M, "A novel low power digitally controlled oscillator with improved linear operating range", International journal of electrical and electronics engineering, pp. 129-134, 2011.

[64] J. BAE, S. RADHAPURAM, I. JO, T. KIHARA, and T. MATSUOKA, " A low-voltage design of digitally-controlled oscillator based on the gm/id methodology", IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), pp. 187–189, 2015.

[65] K. H. CHENG, Y. C. TSAI, Y. L. LO, and J. S. HUANG, "A 0.5-v 0.4-2.24-ghz inductorless phase locked loop in a system-on-chip", IEEE Transactions on Circuits and Systems I: Regular Papers, pp. 849–859, 2011.

[66] Y. CAO, P. LEROUX, W. D. COCK, and M. STEYAERT, "A 63,000 q-factor relaxation oscillator with switched-capacitor integrated error feedback", IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 186–187, 2013.

[67] R. Groza, I. A. Potarniche, B. S. Kirei, and M. D. Topa, "Digitally controlled oscillator for all-digital frequency locked loops", The Journal of Information Science and Technology (JIST),Vol 21,pp.3-17,2018.

[68] Yudong Zhang ; Xiaofeng Liu ; Woogeun Rhee ; Hanjun Jiang ; Zhihua Wang, "A 0.6V 50-to-145MHz PVT tolerant digital PLL with DCO-dedicated ΔΣ LDO and temperature compensation circuits in 65nm CMOS", IEEE International Symposium on Circuits and Systems (ISCAS), 2017.

[69] Y. Ho, Y. Yang, C. Chang et al., "A Near-Threshold 480 MHz 78 W All Digital PLL With a Bootstrapped DCO," IEEE J. Solid-State Circuits, vol. 48, no. 11, pp. 2805–2814, Nov 2013.

[70] C.Lu,S.P.Park,V.Raghunathan,K.Roy, "Low-overhead maximum power point tracking for micro-scale solar energy harvesting systems," International Conference on VLSI Design(VLSID), pp.215–220,2012.

[71] Eltaliawy, A., Mostafa, H., and Ismail, Y, "A new digital locking MPPT control for ultra-low power energy harvesting systems", IEEE 13th International New Circuits and Systems Conference (NEWCAS), 2015.

[72]Ehab Belal, A. Nassar, and H. Mostafa, "Design of Microscale Piezoelectric Energy Harvesting System", IEEE International Mid-West Symposium on Circuits and Systems (MWSCAS 2019), pp.750-753 ,2019.

[73] Ahmed Zaki; Mohamed Shehata; Yehea Ismail; Hassan Mostafa, "Characterization and model validation of triboelectric nanogenerators using Verilog-A", IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS 2017), Boston, MA, USA, 2017.

[74] Jianjun Luo;Liang Xu ;Wei Tang ;Tao Jiang ;Feng Ru Fan ;Yaokun Pang ;Libo Chen ;Yan Zhang ;Zhong Lin Wang, "Direct-Current Triboelectric Nanogenerator Realized by Air Breakdown Induced Ionized Air Channel," Advanced Energy Material , Sep.2018.

[75] J. Liu, A. Goswami, K. Jiang, F. Khan, S. Kim, R. McGee, Z. Li, Z. Hu, J. Lee, T. Thundat, "Direct-current triboelectricity generation by a sliding Schottky nanocontact on MoS2 multilayers", Nat. Nanotechnol, pp.112–116, 2018.

[76] Qiang Zheng, Yang Zou, Yalan Zhang, Zhuo Liu, Bojing Shi, and Xinxin Wang "Biodegradable triboelectric nanogenerator as a life-time designed implantable power source," ,Science Advances ,Vol. 2, no. 3, 04 Mar 2016.

Appendix A
SAR control-VerilogA

```
// VerilogA for SAR, control_logic, veriloga

`include "constants.vams"
`include "disciplines.vams"

Module
control_logic(Vref1_7,Vref1_6,Vref1_5,Vref1_4,Vref1_3,Vref1_2,Vref1_1,Vref1_0,V
ref2_7,Vref2_6,Vref2_5,Vref2_4,Vref2_3,Vref2_2,Vref2_1,Vref2_0,Vef1_n,Vref2_n,
Vin_7,Vin_6,Vin_5,Vin_4,Vin_3,Vin_2,Vin_1,Vin_n,En_vin,Vin_0,comp_out,clk,EO
C);
electrical
Vref1_7,Vref1_6,Vref1_5,Vref1_4,Vref1_3,Vref1_2,Vref1_1,Vref1_0,Vref2_7,Vref2_
6,Vref2_5,Vref2_4,Vref2_3,Vref2_2,Vref2_1,Vref2_0,Vef1_n,Vref2_n,Vin_7,Vin_6,
Vin_5,Vin_4,Vin_3,Vin_2,Vin_1,Vin_0,Vin_n,En_vin,comp_out,clk,EOC;
parameter real trise = 0 from [0:inf);
parameter real tfall = 0 from [0:inf);
parameter real tdel = 0 from [0:inf);
parameter real vtrans_clk= 0.6;



real Vref1[0:8];
real Vref2[0:8];
real Vin[0:8];
real comp_sig;
real En_vin_sig,EOC_s;
parameter real V_high=0.9;
integer i;
integer j;
```

```
analog begin
@ (initial_step) begin
for (i=8;i>=0;i=i-1) begin
Vref1[i]=0;
Vref2[i]=0;
Vin[i]=0;
j=0;
EOC_s=0;
end
end
@(cross(V(clk)-vtrans_clk,1)) begin
comp_sig=V(comp_out);
if (j==0) begin
En_vin_sig=1.4;
EOC_s=0;
for (i=8;i>=0;i=i-1) begin
Vref1[i]=0;
Vref2[i]=0;
Vin[i]=1;
end
j=j+1;
end else begin
if (j==1) begin
Vref1[7]=1;
Vref2[8]=1;
Vref1[8]=0;
Vref2[7]=0;
Vin[0]=0;
Vin[1]=0;
Vin[2]=0;
Vin[3]=0;
```

```
Vin[4]=0;
Vin[5]=0;
Vin[6]=0;
Vin[7]=0;
Vin[8]=0;
En_vin_sig=0;
j=j+1;
end else begin
if (j==2 && (comp_sig>V_high)) begin
Vref1[6]=1;
Vref2[6]=0; //
Vin[8]=0.8; // delete this line
j=j+1;
end else begin
if (j==2 && (comp_sig<V_high)) begin
Vref1[7]=0;
Vref2[7]=1;
Vref1[6]=1;
Vref2[6]=0;//
j=j+1;
end else begin
if (j==3 && (comp_sig>V_high)) begin
Vref1[5]=1;
Vref2[5]=0;//
j=j+1;
end else begin
if (j==3 && (comp_sig<V_high)) begin
Vref1[6]=0;
Vref2[6]=1;
Vref1[5]=1;
Vref2[5]=0;//
```

```
j=j+1;
end else begin
if (j==4 && (comp_sig>V_high)) begin
Vref1[4]=1;
Vref2[4]=0;//
j=j+1;
end else begin
if (j==4 && (comp_sig<V_high)) begin
Vref1[5]=0;
Vref2[5]=1;
Vref1[4]=1;
Vref2[4]=0;//
j=j+1;
end else begin
if (j==5 && (comp_sig>V_high)) begin
Vref1[3]=1;
Vref2[3]=0;//
j=j+1;
end else begin
if (j==5 && (comp_sig<V_high)) begin

        Vref1[4]=0;

        Vref2[4]=1;

        Vref1[3]=1;

        Vref2[3]=0;//
j=j+1;
end else begin
if (j==6 && (comp_sig>V_high))begin
```

```
        Vref1[2]=1;
        Vref2[2]=0;//
        j=j+1;
end else begin
        if (j==6 && (comp_sig<V_high)) begin
        Vref1[3]=0;
        Vref2[3]=1;
        Vref1[2]=1;
        Vref2[2]=0;//
        j=j+1;
        end else begin
                if (j==7 && (comp_sig>V_high)) begin
                        Vref1[1]=1;
                        Vref2[1]=0;//
                        j=j+1;
                end else begin
                        if (j==7 && (comp_sig<V_high)) begin
                                Vref1[2]=0;
                                Vref2[2]=1;
                                Vref1[1]=1;
                                Vref2[1]=0;//
                                j=j+1;
                        end else begin
                                if (j==8 && (comp_sig>V_high)) begin
                                        Vref1[0]=1;
                                        Vref2[0]=0;//
                                        j=j+1;
                                end else begin
                                        if (j==8 && (comp_sig<V_high)) begin
                                                Vref1[1]=0;
                                                Vref2[1]=1;
```

```
                    Vref1[0]=1;
                    Vref2[0]=0;//
                    j=j+1;
                end else begin
                    EOC_s=1;
                    if (j==9 && (comp_sig<V_high)) begin
                        Vref1[0]=0;
Vref2[0]=1;
end
j=0;
end
end
end
end
end
end
end
end
end
end
end
end
end
end
end
end
end
end

@(cross(V(clk) - vtrans_clk,-1)) begin
            if(j==1) begin
                Vin[0]=0;
```

```
                Vin[1]=0;
                Vin[2]=0;
                Vin[3]=0;
                Vin[4]=0;
                Vin[5]=0;
                Vin[6]=0;
                Vin[7]=0;
                Vin[8]=0;
                En_vin_sig=0;
                Vref2[0]=1;
                Vref2[1]=1;
                Vref2[2]=1;
                Vref2[3]=1;
                Vref2[4]=1;
                Vref2[5]=1;
                Vref2[6]=1;
                Vref2[7]=1;
                Vref2[8]=1;
                Vref1[0]=0;
                Vref1[1]=0;
                Vref1[2]=0;
                Vref1[3]=0;
                Vref1[4]=0;
                Vref1[5]=0;
                Vref1[6]=0;
                Vref1[7]=0;
                Vref1[8]=0;

        end

end
```

```
        V(Vref1_7) <+ transition( Vref1[7], tdel, trise, tfall );
        V(Vref1_6) <+ transition(Vref1[6], tdel, trise, tfall );
        V(Vref1_5) <+ transition(Vref1[5], tdel, trise,tfall);
        V(Vref1_4) <+ transition(Vref1[4], tdel, trise,tfall);
        V(Vref1_3) <+ transition(Vref1[3], tdel, trise,tfall);
        V(Vref1_2) <+ transition(Vref1[2], tdel, trise,tfall);
        V(Vref1_1) <+ transition(Vref1[1], tdel, trise,tfall);
        V(Vref1_0) <+ transition(Vref1[0], tdel, trise,tfall);
        V(Vref2_7) <+ transition(Vref2[7], tdel, trise,tfall);
        V(Vref2_6) <+ transition(Vref2[6], tdel, trise,tfall);
        V(Vref2_5) <+ transition(Vref2[5], tdel, trise,tfall);
        V(Vref2_4) <+ transition(Vref2[4], tdel, trise,tfall);
        V(Vref2_3) <+ transition(Vref2[3], tdel, trise,tfall);
        V(Vref2_2) <+ transition(Vref2[2], tdel, trise,tfall);
        V(Vref2_1) <+ transition(Vref2[1], tdel, trise,tfall);
        V(Vref2_0) <+ transition(Vref2[0], tdel, trise,tfall);
        V(Vef1_n)  <+ transition(Vref1[8], tdel, trise,tfall);
        V(Vref2_n) <+ transition(Vref2[8], tdel, trise,tfall);
        V(Vin_n) <+ transition(Vin[8], tdel, trise,tfall);
        V(Vin_7) <+ transition(Vin[7], tdel, trise,tfall);
        V(Vin_6) <+ transition(Vin[6], tdel, trise,tfall);
        V(Vin_5) <+ transition(Vin[5], tdel, trise,tfall);
        V(Vin_4) <+ transition(Vin[4], tdel, trise,tfall);
        V(Vin_3) <+ transition(Vin[3], tdel, trise,tfall);
        V(Vin_2) <+ transition(Vin[2], tdel, trise,tfall);
        V(Vin_1) <+ transition(Vin[1], tdel, trise,tfall);
        V(Vin_0) <+ transition(Vin[0], tdel, trise,tfall);
        V(En_vin) <+ transition(En_vin_sig, tdel, trise, tfall);
        V(EOC)  <+ transition(EOC_s,tdel,trise,tfall);
        end
endmodul
```

Appendix B
Digital control Oscillator (DCO) VerilogA

```
`include "constants.vams"
`include "disciplines.vams"

module squrJ2 (inp,out);
inoutinp;
electrical inp;
output out; voltage out;                    // output terminal
real freqT;
parameter real vl=0; //low output voltage
parameter real vh=2; //high output voltage
real freq, phase, dT, tt, ttol, jitter ;
integer n, seed;

analog begin
  @(initial_step) seed = -561;
freqT=V(inp);
tt=0.01/freqT;
ttol=0.01/freqT;
jitter=0.01/freqT;

  // freq to freq2
freq = freqT;

  // add the phase noise
freq = freq/(1 + dT*freq);

  // bound the time step to assure no cycles are skipped
```

```
  $bound_step(0.6/freqT);

  // phase is the integral of the freq modulo 2p
  phase = 2*`M_PI*idtmod(freq, 0.0, 1.0, -0.5);

  @(cross(phase + `M_PI/2, +1, ttol) or cross(phase - `M_PI/2, +1, ttol)) begin
dT = `M_SQRT2*jitter*$rdist_normal(seed,0, 1);
     n = (phase >= -`M_PI/2) && (phase < `M_PI/2);
  end

  // generate the output
    V(out) <+ transition(n ? vh : vl,330p ,tt);

end
endmodule



`include "constants.vams"
`include "disciplines.vams"

module ehabdco(Vref1_7,Vref1_6,Vref1_5,Vref1_4,Vref1_3,Vref1_2,Vref1_1,Vref1_0,En,clk);
electrical Vref1_7,Vref1_6,Vref1_5,Vref1_4,Vref1_3,Vref1_2,Vref1_1,Vref1_0,En,clk;
parameter real trise = 0.000001 from [0:inf);
parameter real tfall = 0.000001 from [0:inf);
parameter real tdel = 0.000001 from [0:inf);
parameter real vtrans_clk= 1;
real Vref1[0:8];
real comp_sig,EOC_s;
analog begin
```

```
if(V(clk)==1) begin
comp_sig=20000;
Vref1[0]=V(Vref1_0);
Vref1[1]=V(Vref1_1);
Vref1[2]=V(Vref1_2);
Vref1[3]=V(Vref1_3);
Vref1[4]=V(Vref1_4);
Vref1[5]=V(Vref1_5);
Vref1[6]=V(Vref1_6);
Vref1[7]=V(Vref1_7);
end
//0.7
if (Vref1[7]==1 && Vref1[6]==1 && Vref1[5]==1 && Vref1[4]==1 && Vref1[3]==1 &&
Vref1[2]==1 && Vref1[1]==1 && Vref1[0]==0) begin
        EOC_s=132000;
        end
//0.6
else if (Vref1[7]==1 && Vref1[6]==1 && Vref1[5]==0 && Vref1[4]==1 && Vref1[3]==1 &&
Vref1[2]==0 && Vref1[1]==1 && Vref1[0]==0) begin
        EOC_s=110000;
        end
//0.5
else if (Vref1[7]==1 && Vref1[6]==0 && Vref1[5]==1 && Vref1[4]==1 && Vref1[3]==0 &&
Vref1[2]==1 && Vref1[1]==1 && Vref1[0]==0) begin
        EOC_s=83000;
        end
//0.4
else if (Vref1[7]==1 && Vref1[6]==0 && Vref1[5]==0 && Vref1[4]==1 && Vref1[3]==0 &&
Vref1[2]==0 && Vref1[1]==1 && Vref1[0]==0) begin
        EOC_s=74000;
        end
```

```
//0.3
else if (Vref1[7]==0 && Vref1[6]==1 && Vref1[5]==1 && Vref1[4]==0 && Vref1[3]==1 &&
Vref1[2]==1 && Vref1[1]==0 && Vref1[0]==1) begin
        EOC_s=57000;
        end
else if (Vref1[7]==0 && Vref1[6]==0 && Vref1[5]==0 && Vref1[4]==0 && Vref1[3]==0 &&
Vref1[2]==0 && Vref1[1]==0 && Vref1[0]==0) begin
        EOC_s=00000;
        end
V(En)  <+ transition(EOC_s,tdel,trise,tfall);
end
endmodule
```

الملخص

مصادر الطاقة المتجددة الميكانيكية والضوئية والحرارية واشارات التردد اللاسلكي يتم تحويلها الي طاقة كهربائية لتخزينها بالبطاريات. الطاقة الناتجة من المصادر الحرارية او الضوئية تولد جهد ذو قيمة جهد ثابت والتالي يسهل شحن البطاريات دون الحاجة الي تقوميها باستخدام محول التيار المتردد/ التيار المستمر بينما الطاقة الناتجة من المجس الكهرومغناطيسي او اشارات التردد اللاسلكي تولد جهد ذو قيمة متغيرة ولكي يتم تخزين تلك الطاقة بالبطاريات. يتم تقوميها باستخدام محول التيار المتردد/ التيار المستمر الذي يقوم بتقويم الجهد المتغير الي جهد ثابت وبالتالي يسهل شحن البطاريات.

في هذا البحث تم استخدام الطاقة الناتجة من المجس الكهروضغطي لتشغيل الدوائر الإلكترونية في تطبيقات الطب الحيوي. الطاقة الناتجة يتم تقوميها باستخدام محول التيار المتردد/ التيار المستمر ذو كفاءة طاقة ٨٣% ونسبة تحويل الجهد ٣٠٠%.

يستخدم محول التيار المستمر/التيار المستمر لمطابقة جهد خرج محول التيار المتردد/ التيار المستمر مع قيمة جهد المكثف حيث تم استخدام محول التيار المستمر/التيار المستمر باستخدام عدد من المكثفات وذلك لسهولة التطبيق وعدم اللجوء الي استخدام الملفات والتي تستهلك مساحات اكبر من المكثفات وتجنب الحث الكهرومغناطيسي .

يتم توليد نطاق التردد المطلوب من ٥٧ كيلوهرتز الي ١٣٢ كيلوهرتز باستخدام مذبذب التحكم في الجهد الذي يستخدم جدول بحث لضمان أن التردد الذي تم توليده يطابق أقصى نقطة طاقة. يتم تحويل جهد خرج محول التيار المتردد/ التيار المستمر الي عدد من البت باستخدام محول الاشارة التناظرية الي اشارة رقمية لإنشاء جدول البحث وقد استخدمت دائرة السجل التقريبي لانها اقل استهلاك للطاقة والمساحة .

وايجاد علاقة بين الجهد الناتج من محول التيار المتردد/ التيار المستمر والتردد يؤدي الي حصولنا علي اقصي قدرة للطاقة المكتسبة باستخدام المجس الكهروضغطي والتي تتغير نتيجة الاهتزاز للمجس الكهروضغطي.

الاسهام في هذا العمل موضح علي عدد من نطاقات البحث. البحث الاول عمل مقارنة بين محولات التيار المتردد / تيار مستمر والتي لا تعمل باستخدام الصمام الثنائي حيث تم عمل مقارنة بين عدد من المعايير أيهما اقل جهد مستخدم والكفاءة والمساحة المستخدمة . البحث الثاني تصميم تقنية جديدة لمحول التيار المتردد / تيار مستمر وعمل مقارنة مع احدث الابحاث المنشورة في هذا النطاق. البحث الثالث تصميم للدوائر الإلكترونية لاستخدام الطاقة الناتجة من المجس الكهروضغطي في تطبيقات الطب الحيوي وما يشمل ذلك من دوائر فرعية مع مقارنة مع الابحاث المنشورة .

مهندس: ايهاب بلال عبد الحميد ابراهيم

تاريخ الميلاد: ١٩٨٧/٠٤/٠٨

الجنسية : مصري

تاريخ التسجيل: ٢٠١٣/٣/١

تاريخ المنح: ٢٠١٩/../..

القسم: هندسة الإلكترونيات والإتصالات الكهربية

الدرجة: ماجستير العلوم

المشرفون: ا.د. امين محمد نصار

ا.د. محمد سامح السعيد

د. حسن مصطفي حسن مصطفي

الممتحنون: أ.د. امين محمد نصار مشرف رئيسي

أستاذ في قسم الإلكترونيات بكلية الهندسة – جامعة القاهرة

د. حسن مصطفي حسن مشرف

استاذ مساعد في قسم الالكترونيات بكلية الهندسة – جامعة القاهرة

ا.د. أحمد نادر محيي الدين الممتحن الداخلي

استاذ في قسم الإلكترونيات بكلية الهندسة – جامعة القاهرة

ا.د.السيد مصطفي سعد الممتحن الخارجي

استاذ في قسم الإلكترونيات بكلية الهندسة – جامعة حلوان

عنوان الرسالة:

تصميم لنظام الطاقة المكتسبة متناهي الصغر باستخدام المجس الكهروضغطي

الكلمات الدالة

محول التيار المتردد / تيار مستمر، محول التيار المستمر / تيار مستمر ، أقصي نقطة طاقة، مذبذب التحكم في الجهد .

ملخص الرسالة:

استخدام الطاقة الناتجة من المجس الكهروضغطي لتشغيل الدوائر الإلكترونية في تطبيقات الطب الحيوي. الطاقة الناتجة يتم تقوميها باستخدام محول التيار المتردد/ التيار المستمر ذو كفاءة طاقة ٨٣% ونسبة تحويل الجهد ٣٠٠%.

يستخدم محول التيار المستمر/التيار المستمر لمطابقة جهد خرج محول التيار المتردد/ التيار المستمر مع قيمة جهد المكثف. يتم توليد نطاق التردد المطلوب من ٥٧ كيلوهرتز الي ١٣٢ كيلوهرتز باستخدام مذبذب التحكم في الجهد الذي يستخدم جدول بحث لضمان أن التردد الذي تم توليده يطابق أقصى نقطة طاقة. يتم تحويل جهد خرج محول التيار المتردد/ التيار المستمر الي عدد من البت باستخدام محول الاشارة التناظرية الي اشارة رقمية لإنشاء جدول البحث.

تصميم لنظام الطاقة المكتسبة
متناهي الصغر باستخدام المجس الكهرو ضغطي

اعداد

اسم الطالب

إيهاب بلال عبد الحميد إبراهيم

رسالة مقدمة إلى كلية الهندسة – جامعة القاهرة

كجزء من متطلبات الحصول على درجة

ماجستيرالعلوم

في

هندسة الإلكترونيات والاتصالات الكهربية

يعتمد من لجنة الممتحنين:

الاستاذ الدكتور:أمين محمد نصار **المشرف الرئيسى**

أستاذ في قسم الإلكترونيات بكلية الهندسة – جامعة القاهرة

الدكتور:حسن مصطفي حسن **مشرف**

استاذ مساعد في قسم الالكترونيات بكلية الهندسة – جامعة القاهرة

الاستاذ الدكتور: أحمد نادر محيي الدين **الممتحن الداخلي**

أستاذ في قسم الإلكترونيات بكلية الهندسة – جامعة القاهرة

الاستاذ الدكتور: السيد مصطفي سعد **الممتحن الخارجي**

أستاذ في قسم الإلكترونيات بكلية الهندسة – جامعة حلوان

كليــة الهندســة- جامعــة القاهــرة

الجيـزة-جمهوريـة مصـرالعربيــة

٢٠١٩

تصميم لنظام الطاقة المكتسبة
متناهي الصغر باستخدام المجس الكهرو ضغطي

اعداد

اسم الطالب

إيهاب بلال عبد الحميد إبراهيم

رسالة مقدمة إلى كلية الهندسة –جامعة القاهرة

كجزء من متطلبات الحصول على درجة

ماجستيرالعلوم

في

هندسة الإلكترونيات والاتصالات الكهربية

تحت اشراف

أ.د / آمين محمد نصار

استاذ في قسم الالكترونيات
والاتصالات الكهربية
كلية الهندسة - جامعة القاهرة

أ.د / محمد سامح السعيد

استاذ في قسم الالكترونيات
والاتصالات الكهربية
كلية الهندسة - جامعة القاهرة

د/ حسن مصطفي حسن

استاذ مساعد في قسم الالكترونيات
والاتصالات الكهربية
كلية الهندسة - جامعة القاهرة

كليــة الهندســة-جامعــة القاهــرة

الجيـزة-جمهوريـة مصـرالعربيـة

٢٠١٩

تصميم لنظام الطاقة المكتسبة
متناهي الصغر باستخدام المجس الكهرو ضغطي

اعداد

إيهاب بلال عبد الحميد إبراهيم

رسالة مقدمة إلى كلية الهندسة –جامعة القاهرة
كجزء من متطلبات الحصول على درجة
ماجستيرالعلوم
في
هندسة الإلكترونيات والاتصالات الكهربية

كليــة الهندســة - جامعــة القاهــرة
الجيـزة - جمهوريـة مصـرالعربيــة
٢٠١٩