NBTI and Process Variations Compensation Circuits Using Adaptive Body Bias

Hassan Mostafa, *Member, IEEE,* Mohab Anis, *Senior Member, IEEE,* and Mohamed Elmasry, *Fellow, IEEE*

***Abstract*—Reliability and variability have become big design challenges facing submicrometer high-speed applications and microprocessors designers. A low area overhead adaptive body bias (ABB) circuit is proposed in this paper to compensate for negative-bias temperature instability (NBTI) aging and process variations to improve the system reliability and yield. The proposed ABB circuit consists of a threshold voltage-sensing circuit and an on-chip analog controller. In this paper, post-layout simulation results, referring to an industrial hardware-calibrated STMicroelectronics 65-nm CMOS technology transistor model, are presented. The transistor model contains process variations and NBTI aging model cards, which are declared by STMicroelectronics to be Silicon verified. Cadence RelXpert, Virtuoso Spectre, and Virtuoso UltraSim tools are used to estimate the NBTI aging and process variations impacts on a circuit block case study, extracted from a real microprocessor critical path. These results show that the proposed ABB compensates effectively for NBTI aging and process variations. For example, the proposed ABB improves the timing yield from 74.4% to 99.7% at zero aging time and from 36.6% to 97.1% at 10 years aging time. In addition, the proposed ABB increases the total yield from 67% to 99.5% at zero aging time and from 35.9% to 97.1% at 10 years aging time.**

***Index Terms*—Adaptive body bias, deep submicrometer, negative-bias temperature instability, process variations.**

I. Introduction

RELIABILITY is one of the major design challenges facing high-speed applications and microprocessors designers. Shrinking geometries, lower power supplies, higher clock frequencies, and higher density circuits all have a great impact on reliability. As CMOS technology scales, negative-bias temperature instability (NBTI) becomes a significant reliability concern.

NBTI is the generation of interface traps under negative-bias conditions (i.e., $V_{GS} = -V_{DD}$) at elevated temperatures in pMOS transistors. NBTI is a growing threat to circuit reliability in scaled CMOS technologies [1]–[6]. These interface traps are formed due to crystal mismatches at the Si–SiO_2 interface. During Si oxidation, the majority of the atoms are bonded to oxygen, whereas some of the atoms are bonded with hydrogen, leading to the formation of weak Si–H bonds. When a pMOS transistor is negatively biased, the holes in the channel dissociate these weak Si–H bonds and the interface traps are formed. These traps are electrically active physical defects with their energy distributed between the valence band and the conduction band in the band diagram [1], [7], resulting in an increase in the absolute pMOS transistor threshold voltage, $|V_{tp}|$. This $|V_{tp}|$ increase results in performance degradation and timing yield loss over aging time.

The aggressive scaling of CMOS technology toward the nanometer regime has created large statistical process variations in the transistor parameters, such as threshold voltage, channel length, and mobility [8]–[10]. Therefore, the process variations are considered one of the most important design challenges for sub-100-nm CMOS technologies [8], [9], [11]. These process variations are classified into die-to-die (D2D) variations and within-die (WID) variations. In D2D variations, all the devices on the same die are assumed to have the same parameters. However, the devices on the same die are assumed to behave differently for WID variations [9].

Adaptive body bias (ABB) allows the tuning of the transistor threshold voltage, V_t, by controlling the transistor body-to-source voltage, V_{BS}. A forward body bias (FBB) (i.e., $V_{BS} > 0$) reduces V_t. Alternatively, a reverse body bias (RBB) (i.e., $V_{BS} < 0$) increases V_t. Therefore, the impacts of NBTI and process variations are mitigated by adopting the ABB technique. Practically, the implementation of the ABB is desirable to bias each device in a design independently (local ABB), to mitigate D2D and WID variations. However, supplying so many separate voltages inside a die results in a large area overhead. On the other hand, using the same body bias for all devices on the same die (global ABB) limits the capability to compensate for WID variations [12].

In [12] and [13], ABB is used to compensate for process variations and yield improvement by estimating the process parameters and using a digital controller to control the body bias. Recently, several NBTI monitoring circuits are introduced in [14]–[16]. These monitoring circuits output can be fed to an ABB circuit to compensate for the NBTI impact. These monitoring circuits utilize a phase-locked loop technique to determine the pMOS transistor deviation digitally and require a digital-to-analog converter to convert this digital deviation to the appropriate body-bias voltage, which is obtained by using a digital control module. These requirements impose large area overhead that limits the applicability of these circuits.

In this paper, a global ABB circuit is adopted for NBTI compensation. It is based on estimating the stressed pMOS

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The authors are with the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON N2L3G1 Canada (e-mail: hmostafa@uwaterloo.ca; manis@vlsi.uwaterloo.ca; elmasry@uwaterloo.ca).

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transistor threshold voltage, $|V_{tp_{\text{stressed}}}|$, in conjunction with an ABB control circuit, achieved by an on-chip analog circuit. This analog circuit generates the appropriate body-bias voltage, based on the $|V_{tp_{\text{stressed}}}|$ deviations due to NBTI. The main advantage of this ABB circuit is its lower area overhead compared to the NBTI monitoring circuits published in [14]–[16]. All the results reported in this paper are post-layout simulation results, referring to an industrial hardware-calibrated STMicroelectronics 65-nm CMOS technology, where process variations and NBTI stress are included in the transistor model card and declared by STMicroelectronics to be Silicon verified. In addition, the process and temperature variations impact on the pMOS transistor threshold voltage is reduced due to this global ABB circuit adoption as well.

This paper is organized as follows. Section II explains the proposed ABB circuit design. Simulation results are given in Section III. Finally, some conclusions are drawn in Section IV.

A. NBTI Aging

In [14] and [17], it is stated that the pMOS transistor threshold voltage increase due to NBTI, $\Delta|V_{tp_{\text{DC}}}|$, under constant dc stress (i.e., the pMOS transistor gate voltage is grounded), follows a power law model with respect to the aging time as follows [14], [17]:

$$\Delta|V_{tp_{\text{DC}}}| = K_{\text{DC}} \times t^{0.16} \tag{1}$$

where K_{DC} is a technology-dependent parameter (i.e., K_{DC} is a function of temperature, supply voltage, device geometry, and interfacial traps density) and t is the aging time in seconds. There exist several models for the NBTI that are based on different physical explanations. Recently, in [17], new explanation of the NBTI, based on switching oxide traps mechanism rather than the reaction–diffusion mechanism, explains most of the experimental data that were inconsistent with the reaction–diffusion model.

In real circuit operation, the effective ON time of the pMOS transistor is bounded by the operating frequency and the gate input probability. During the OFF time (i.e., the pMOS transistor gate voltage is connected to the supply voltage), the pMOS transistor experiences a recovery process, where $|V_{tp}|$ decreases back to its original value before stress. Accordingly, the pMOS transistor threshold voltage increase due to NBTI, $\Delta|V_{tp_{\text{AC}}}|$, under dynamic ac stress, is a scaled version of $\Delta|V_{tp_{\text{DC}}}|$ and is given by [14], [17]

$$\Delta|V_{tp_{\text{AC}}}| \approx \alpha \times \Delta|V_{tp_{\text{DC}}}| = \alpha \times K_{\text{DC}} \times t^{0.16} \tag{2}$$

where α is a prefactor dependent on the operating frequency and the gate input probability. It is reported that the pMOS transistor life time is much longer under ac stress than dc stress by a factor of 4X.

B. Process Variations

The primary sources of process variations are random dopant fluctuations (RDFs) and channel length variations. The RDF variations are classified as random variations, whereas the channel length variations are classified as systematic variations.

1) *RDF*: The number of dopants in the MOSFET depletion region decreases as technology scales. Due to the discreteness of the dopant atoms, there is a statistical random fluctuation of the number of dopants, within a given volume, around their average value. This fluctuation in the number of dopants in the transistor channel results in device threshold voltage variations. It has been shown that the threshold voltage variation, due to RDF, is normally distributed, and its standard deviation, $\sigma_{V_t,\text{RDF}}$, is inversely proportional to the square root of the transistor active area.
2) *Channel Length Variations*: For sub-90-nm nodes, optical lithography requires light sources with wavelengths much larger than the minimum feature sizes for the technology. Therefore, controlling the critical dimension (CD) at these technology nodes becomes so difficult. The variation in CD (i.e., channel length of the transistor) impacts directly the transistor V_t. In short-channel devices, the threshold voltage, V_t, has an exponential dependence on the channel length, L, due to charge sharing and drain-induced barrier lowering (DIBL) effects [17]. Thus, a slight variation in L introduces large variation in V_t due to this exponential dependence.

The system timing yield is affected by the process variations and the temperature variations as well as the aging NBTI effect.

II. Proposed ABB Circuit

In the proposed ABB circuit, the effect of NBTI on $|V_{tp}|$ is compensated by estimating the actual value of $|V_{tp}|$, which is impacted by NBTI, by using an estimation circuit. Then, the analog controller generates the appropriate body-bias voltage, V_{SB}, to mitigate the NBTI impact. The analog controller is a direct implementation of the relationship between $|V_{tp}|$ and V_{SB}. In [17] and [18], the relationship between $|V_{tp}|$ and V_{SB} for a pMOS transistor is given by

$$\begin{aligned} |V_{tp}| &= |V_{tpo}| + \Delta|V_{tp}|_{\text{BB}} \\ \text{and} \quad \Delta|V_{tp}|_{\text{BB}} &= \gamma(\sqrt{2\phi_F - V_{\text{SB}}} - \sqrt{2\phi_F}) \end{aligned} \tag{3}$$

where $|V_{tpo}|$ is the pMOS transistor threshold voltage at zero body bias (i.e., when $V_{\text{SB}} = 0$), $\Delta|V_{tp}|_{\text{BB}}$ is the body-bias effect on $|V_{tp}|$, γ is the body effect coefficient, and ϕ_F is the Fermi potential with respect to the midgap in the substrate [17], if $|V_{tpo}|$ is increased due to NBTI by $\Delta|V_{tp}|_{\text{NBTI}}$. Therefore, the body-bias voltage, V_{SB}, compensates for this NBTI by producing a threshold voltage change, $\Delta|V_{tp}|_{\text{BB}}$, that cancels out the NBTI change, $\Delta|V_{tp}|_{\text{NBTI}}$ (i.e., $\Delta|V_{tp}|_{\text{BB}} = -\Delta|V_{tp}|_{\text{NBTI}}$). The value of V_{SB} that compensates for the NBTI change is given by

$$V_{\text{SB}} = \frac{2\sqrt{2\phi_F}}{\gamma} \times \Delta|V_{tp}|_{\text{NBTI}} - \frac{1}{\gamma^2}(\Delta|V_{tp}|_{\text{NBTI}})^2 \tag{4}$$

where $\Delta|V_{tp}|_{\text{NBTI}}$ is the difference between the estimated threshold voltage, $|V_{tp_{\text{stressed}}}|$, which is impacted by the NBTI, and the nominal threshold voltage, $|V_{tpo}|$. Typically, the source of the pMOS transistor is connected to the supply voltage,

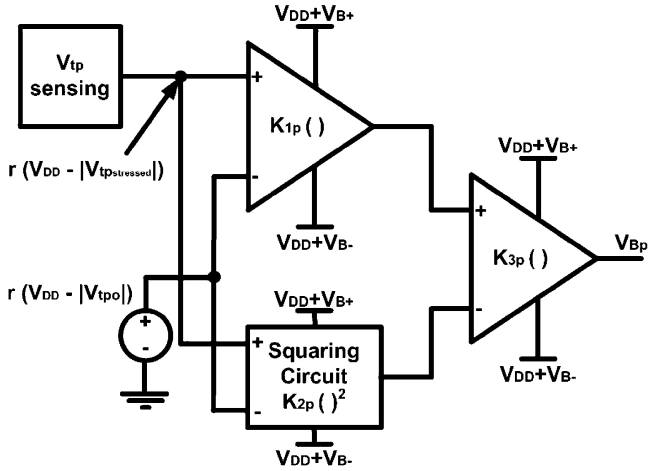

Fig. 1. Proposed ABB circuit for NBTI compensation.

$V_{\rm DD}$. Therefore, the body-bias voltages of the pMOS transistor, V_{Bp}, which result in NBTI compensation, is given by

$$V_{Bp} = V_{\rm DD} - \frac{2\sqrt{2\phi_F}}{\gamma}[|V_{tp_{\rm stressed}}| - |V_{tpo}|] + \frac{1}{\gamma^2}[|V_{tp_{\rm stressed}}| - |V_{tpo}|]^2. \quad (5)$$

The proposed ABB circuit is depicted in Fig. 1 for the bias voltage V_{Bp}. The sensing circuit, shown in Fig. 1, is used to estimate the actual value of $|V_{tp}|$, which is impacted by the NBTI under full stress (the worst-case NBTI effect). This sensing circuit outputs an estimate for the pMOS threshold voltage, denoted by $V_{\rm out} = r\ (V_{\rm DD} - |V_{tp_{\rm stressed}}|)$ that is applied to an amplifier circuit and a squaring circuit to produce the required bias voltage, which is capable of reducing the impact of NBTI.

In Fig. 1, the voltage source of the value $r\ (V_{\rm DD} - |V_{tpo}|)$ is a dc-bias voltage representing the ratio r multiplied by the difference between the supply voltage, $V_{\rm DD}$, and the pMOS transistor nominal threshold voltage value at zero body bias. The dc supply voltages of the amplifiers are set to $(V_{\rm DD} + V_{B+})$ and $(V_{\rm DD} + V_{B-})$ to limit the body-bias voltage, V_{Bp}, and to implement (5). According to Fig. 1 and recalling (5), the gains K_{1p}, K_{2p}, and K_{3p} are given by

$$K_{1p} \times K_{3p} = \frac{2\sqrt{2\phi_F}}{\gamma \times r} \quad \text{and} \quad K_{2p} \times K_{3p} = -\frac{1}{\gamma^2 \times r^2}. \quad (6)$$

The implementations of the sensing circuit, the amplifiers, and the squaring circuit are given in the following discussions.

A. Sensing Circuit

The sensing circuit, displayed in Fig. 2, is used to estimate the actual value of the threshold voltage of the pMOS transistor, which is impacted by NBTI under static dc stress. In this circuit, the pMOS transistor is sized with the same sizing as the pMOS transistor in the test circuit and the nMOS transistor is a native transistor. Native transistors are manufactured without additional threshold voltage implantation in the channel area and thus exhibit a natural threshold voltage in the manufacturing process. This natural threshold

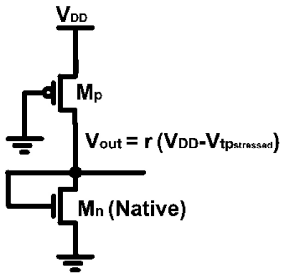

Fig. 2. pMOS transistor $|V_{tp}|$ sensing circuit.

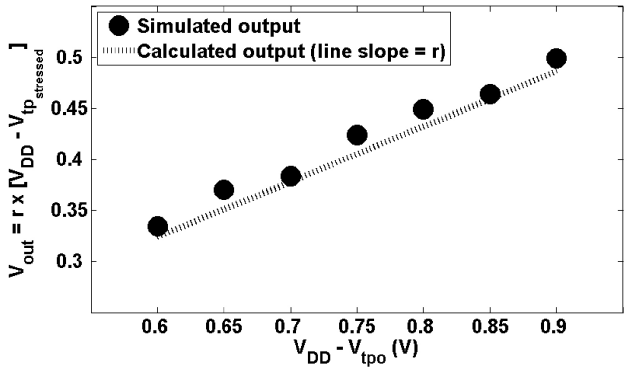

Fig. 3. Output of the pMOS threshold voltage sensing circuit shown in Fig. 2.

voltage is typically around 0 V [19]. The minimum size of the native transistor as introduced by the industrial hardware-calibrated STMicroelectronics 65-nm CMOS technology is 500 nm/300 nm that is used in this sensing circuit.

By using the $\alpha-$power law model, introduced in [20], and equating the dc currents of the nMOS and pMOS transistors, the output voltage of this circuit, $V_{\rm out}$, is expressed as

$$V_{\rm out} = V_{tn} + r \times [V_{DD} - |V_{tp_{\rm stressed}}|] \approx r \times [V_{\rm DD} - |V_{tp_{\rm stressed}}|] \quad (7)$$

$$\text{and} \quad r = \left(\frac{k_{p'}\frac{W}{L}|_p}{k_{n'}\frac{W}{L}|_n}\right)^{\frac{1}{\alpha}}$$

where $k_{n'}$ and $k_{p'}$ are the technological parameters, and $\frac{W}{L}|_n$ and $\frac{W}{L}|_p$ are the sizes of the nMOS and the pMOS transistors, respectively. It should be noted that the native nMOS transistor threshold voltage, V_{tn}, is assumed to be 0 V in (7) [19].

Fig. 3 displays the output voltage of the sensing circuit, $V_{\rm out}$, versus $(V_{\rm DD} - |V_{tpo}|)$. This figure is obtained from SPICE simulations by sweeping the threshold voltage of the industrial STMicroelectronics 65-nm CMOS technology transistor model and using $V_{\rm DD} = 1.0$ V and $r \approx 0.54$. Good agreements between the estimated threshold voltage values and their actual values prove that the threshold voltage sensing circuit is effective, when used in nanometer technologies. The maximum error between the estimated threshold voltage values and their corresponding actual values is 5.4%, and the average error is 3.2%.

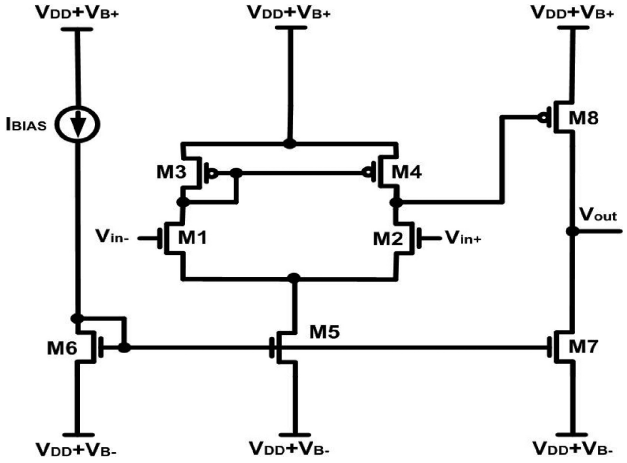

Fig. 4. Proposed two-stage amplifier circuit.

B. Amplifier Circuit

In the proposed ABB circuit in Fig. 1, two amplifiers with different gains and a large output voltage swing, $(V_{B+} - V_{B-})$, are required. Therefore, the two-stage configuration amplifier circuit, shown in Fig. 4, is utilized. The advantage of this configuration is that it isolates the gain and the output voltage swing requirements. The first stage is configured in a differential pair topology to provide the high-gain requirements. Typically, the second stage is configured as a common source stage to allow maximum output voltage swings [21]. Long channel transistor operation is assumed by making all the amplifier transistors lengths equal 130 nm, and therefore, all transistors are assumed to be in the pinch-off saturation region and the following transistors pairs, (M1 and M2), (M3 and M4), and (M6 and M7), are designed to be matched.

According to [22], the mismatch between these transistors threshold voltages is inversely proportional to the square root of the channel area (WL). Thus, by designing all the amplifier and squaring circuit transistors widths larger than 195 nm (the minimum width for STMicroelectronics 65-nm transistor is 120 nm) and lengths of 130 nm (the minimum length for STMicroelectronics 65-nm transistor is 60 nm), this mismatch effect is reduced.

Correspondingly, the amplifier gain, K, is written as

$$K = \underbrace{\frac{g_{m1}}{g_{d2} + g_{d4}}}_{} \times \underbrace{\frac{g_{m8}}{g_{d7} + g_{d8}}}_{} \tag{8}$$

where the first term represents the differential pair gain, the second term represents the second stage gain, g_m is the transistor transconductance, and g_d is the transistor drain-to-source output conductance. g_m and g_d are designed to achieve the required gain, which is achieved by the first stage, and the output voltage swing, which is achieved by the second stage, in each amplifier. It should be noted that the amplifier shown in Fig. 4 is a noninverting amplifier. However, this amplifier is configured as an inverting amplifier by changing the input terminals (i.e., V_{in+} and V_{in-} become the inputs to transistors M1 and M2, respectively).

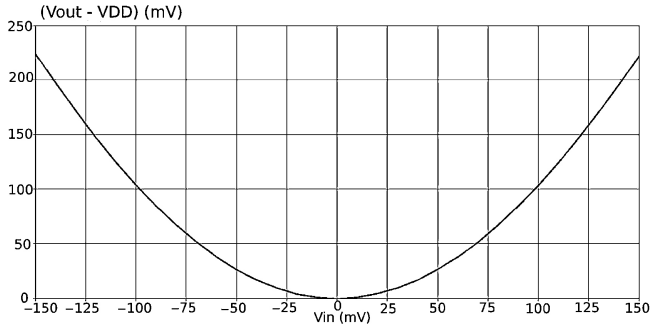

Fig. 6. Simulated squaring circuit output with V_{in} is varied from −0.15 V to 0.15 V and the gain is 10.0.

C. Squaring Circuit

One of the essential building blocks in the ABB circuit, shown in Fig. 1, is the squaring circuit. Several squaring circuits are reported in the literature [23], [24]. Fig. 5 depicts the squaring circuit used in the proposed ABB circuit. The proposed squaring circuit consists of a differential voltage generator circuit and a basic common source differential pair squaring circuit. The differential voltage generator circuit is utilized to adjust the squaring circuit output voltage dc-offset and the squaring circuit gain. Assuming long channel transistor operation, all transistors are operating in the pinch-off saturation region, and the transistors pairs, (Md1 and Md2), (Md6, Md7, Md10, and Md11), (Md5, Md9, and Md13), (Md3 and Md8), and (Md4 and Md12), are matched. The small signal current flowing through Md1 is $g_{m1}V_{in}/2$ that is equal to the small signal current flowing through Md8, which is $g_{m6}V_{o1}/2$ due to the current mirror action between these transistors. Therefore, $V_{o1} = (g_{m1}/g_{m6})V_{in}$. Similarly, due to the current mirror action between transistors Md4 and Md12, the voltage V_{o2} is $-(g_{m1}/g_{m10})V_{in}$. Since transistors Md6, Md7, Md10, and Md11 are matched, the two output voltages, V_{o1} and V_{o2}, are given by

$$V_{o1} = -V_{o2} = (g_{m1}/g_{m6})V_{in}. \tag{9}$$

These two output voltages, V_{o1} and V_{o2}, have an equal common-mode voltage, $V_{REF_{SQ}}$. When these two output voltages are applied to the basic squaring circuit, the resultant output voltage, $V_{out_{SQ}}$, is given by [24]

$$V_{out_{SQ}} = V_{DD} + \frac{(V_{B+} - |V_{tp}|)^2 - (V_{REF_{SQ}} + |V_{tp}|)^2}{2(V_{B+} - V_{REF_{SQ}} - 2|V_{tp}|)} + \frac{(g_{m1}/g_{m6})^2 \times V_{in}^2}{2(V_{B+} - V_{REF_{SQ}} - 2|V_{tp}|)} \tag{10}$$

where the transistors pairs, (Ms1 and Ms2) and (Ms4 and Ms5) are matched. It is evident that the squaring circuit output voltage dc-offset can be adjusted through $V_{REF_{SQ}}$, whereas the squaring circuit gain can be adjusted through the transconductance ratio, (g_{m1}/g_{m6}), and $V_{REF_{SQ}}$. Fig. 6 displays the simulation results for the squaring circuit in Fig. 5, where V_{in} is varied from −0.15 V to 0.15 V and the squaring circuit gain is 10.0.

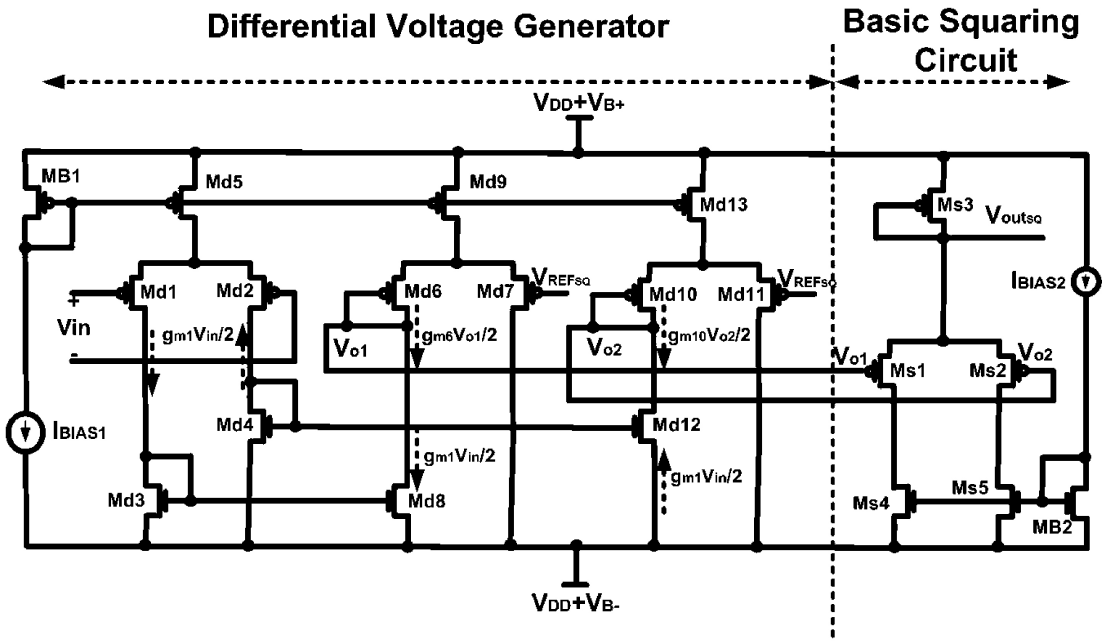

Fig. 5. Squaring circuit that consists of the differential voltage generator and the basic squaring circuit.

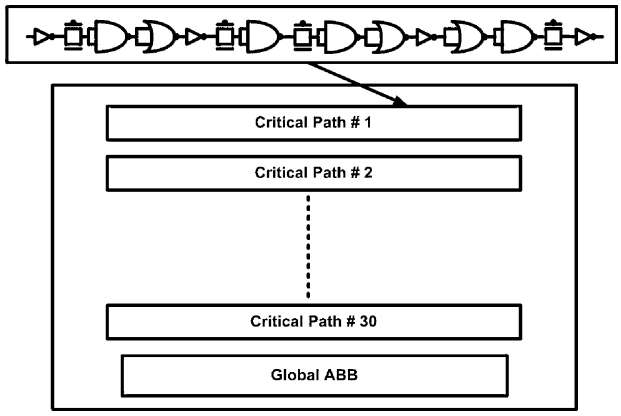

Fig. 7. Test circuit used in the simulation setup.

III. Simulation Results and Discussions

In the following simulation results, the layout of a circuit block, extracted from a real microprocessor critical path, is utilized to verify the proposed ABB effectiveness in NBTI aging and process variations compensation. This circuit block consists of 15 CMOS gates including CMOS inverter gates, NAND gates, NOR gates, and Transmission gates, similar to the test circuits used in [12] and [13]. Fig. 7 portrays the test circuit, which consists of 30 critical paths and a global ABB circuit.

This circuit block is selected to model the effect of the proposed ABB on the reliability and yield improvement of a real microprocessor design [13]. The figures of merit considered in this experiment are the oscillation frequency (F_{clk}), the dynamic power (P_{dyn}) of the circuit block when configured as a ring oscillator, and the leakage power (P_{leak}) of the circuit block when operating in static conditions [13]. The circuit block and the ABB circuits are implemented by using an industrial hardware-calibrated STMicroelectronics 65-nm CMOS transistor model. This model card includes the process variations and the NBTI stress effects that are declared by STMicroelectronics to be Silicon verified. The supply voltage, V_{DD}, equals 1.0 V. The reliability analysis is performed by using Cadence RelXpert, Virtuoso Spectre, and Virtuoso UltraSim tools.

The pMOS transistor parameters such as $|V_{tpo}|$, ϕ_F, and γ are determined from the transistor model card at a temperature $T = 125\,^{\circ}\text{C}$ and equal 0.204 V, 0.439 V, and 0.18, respectively. Accordingly, The ABB circuit parameters K_{1p}, K_{2p}, and K_{3p} equal -1.8, 10.0, and -10.6, respectively. All the above parameters are calculated at $T = 125\,^{\circ}\text{C}$ and $r = 0.54$. It should be mentioned that the technology parameter ϕ_F is linearly proportional to the temperature T in ^{o}K, accordingly, the ABB design is performed at the worst-case temperature $T = 125\,^{\circ}\text{C}$.

The junction leakage current and the breakdown considerations determine the RBB voltage bound, while the FBB is limited by the subthreshold leakage current and the forward biasing of the drain–bulk junction. According to [25] and [26], the upper limit of the FBB voltage for latch-up-free operation, in 65-nm CMOS technology with V_{DD} ranges from 0.9 V to 1.2 V, is 0.6V. Also, SPICE simulations are conducted by sweeping the FBB voltage for the pMOS transistor and show that the upper limit of the FBB voltage to prevent latch-up triggering for the pMOS transistor is 0.59 V. Therefore, the maximum FBB voltage used in this ABB is set to 0.5 V to ensure latch-up-free operation in case of fluctuations of the FBB voltage around 0.5 V. Accordingly, the FBB and the RBB maximum voltages (i.e., $V_{\text{DD}} + V_{B+}$ and $V_{\text{DD}} + V_{B-}$) are set to $1\,\text{V} \pm 0.5\,\text{V}$ [12]. The dc supply voltage $r(V_{\text{DD}} - |v_{tpo}|)$ is used as an off-chip supply voltage that can be tweaked during the chip-testing process to search for the best match of (6). This tweaking of this dc voltage helps in compensating for all the factors that affect the match of (6) such as process variations and power supply noise. Once this voltage is known, it can be programmed into the chip [12].

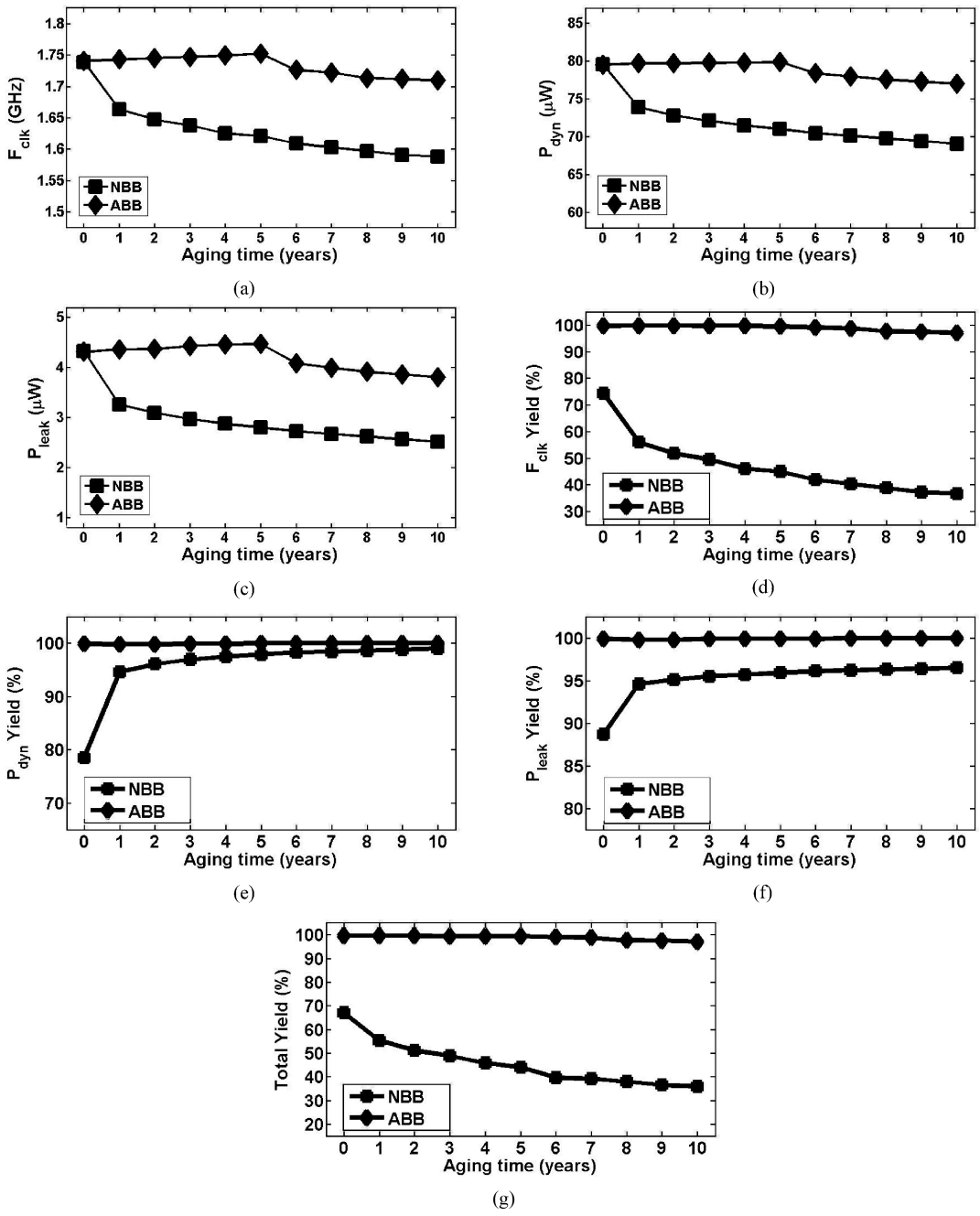

Fig. 8. Post-layout simulation results for the NBB case and the ABB case versus aging time at T = 125 °C considering (a) clock frequency (F_{clk}), (b) dynamic power (P_{dyn}), (c) leakage power (P_{leak}), (d) F_{clk} yield, (e) P_{dyn} yield, (f) P_{leak} yield, and (g) total yield.

The effectiveness of the proposed ABB circuit in mitigating the NBTI stress impact and the process variations is examined by performing post-layout simulations for the circuit block without the adoption of the ABB circuit. Then, the same simulations are repeated while the ABB circuit is adopted and the results are compared to the case when the ABB circuit is not utilized. In these simulations, the temperature used is T = 125 °C with the aging time changes from 0 to 10 years in 1 year step. The effect of changing the temperature is discussed later in this section.

The Monte Carlo analysis generates 5000 different dies. In each Monte Carlo statistical run (which is corresponding to a certain die), the die frequency is calculated as the minimum frequency of the die critical paths. Since the real microprocessor die contains hundreds of critical paths, the die power (i.e., the dynamic power and the leakage power) is calculated as the average power per critical path. This is performed by summing the critical paths powers and dividing by the number of critical paths per die.

A. NBTI Aging Mitigation

The effectiveness of the proposed ABB on mitigating F_{clk} degradation with aging time is displayed in Fig. 8(a). In this figure, F_{clk} is degraded due to NBTI aging at the NBB case by 4.4% at 1 year aging time and by 8.7% at 10 years aging time. It is evident that the ABB circuit not only keeps F_{clk} constant

but also improves it with aging up to 5 years aging time. This is because the ABB sensing circuit is represented by a dc stressed PMOS transistor, whereas the actual PMOS transistors are under dynamic ac stress. Accordingly, the ABB circuit provides more FBB than required that improves F_{clk}. After 5 years aging, the ABB case exhibits some F_{clk} reduction because the ABB is limited to a body-bias voltage of 0.5 V. Accordingly, the NBTI $|V_{tp}|$ increase is larger than the $|V_{tp}|$ reduction amount supplied by the ABB when the body-bias voltage becomes 0.5 V. However, this F_{clk} degradation percentage is 1.7% at 10 years aging compared to 8.7% for the NBB case.

Fig. 8(b) and (c) shows that P_{dyn} and P_{leak} are improved with aging time at the expense of degraded performance for the no body bias (NBB) case. Adopting the ABB circuit slightly increases P_{dyn} and P_{leak} up to 5 years aging time. For example, at 4 years aging time, P_{dyn} and P_{leak} are improved by 10.1% and 33.7%, respectively, for the NBB case whereas no improvement occurs in the ABB case (actually, P_{dyn} and P_{leak} increase for the first 5 years with ABB adoption). At 10 years aging time, P_{dyn} and P_{leak} are improved by 13.2% and 41.9%, respectively, for the NBB case and improved by 3.2% and 12.1%, respectively, for the ABB case.

B. Process Variations Mitigation

The F_{clk}, P_{dyn}, and P_{leak} yields are calculated by conducting 5000-point post-layout Monte Carlo statistical analysis by setting the target F_{clk}, P_{dyn}, and P_{leak} values to 1.6 GHz, 85 μW, and 6.5 μW, respectively, [12], [13]. It is evident from Fig. 8(d) that the F_{clk} yield at zero aging time is improved from 74.4% to 99.7% by adopting the ABB circuit. In order to improve the F_{clk} yield further, local ABB circuits should be utilized to account for the systematic WID variations (i.e., employing a local ABB circuit to each critical path). Employing local ABB circuits will improve the F_{clk} yield at the expense of larger area overhead compared to the global ABB circuit adopted in this paper. The F_{clk} yield degraded with aging time for the NBB case reaching 36.6% at 10 years aging time. The adoption of the ABB circuit enhances the F_{clk} yield and keeps it close to 100% (i.e., the F_{clk} yield is 97.1% at 10 years aging time).

Fig. 8(e) and (f) shows that the ABB circuit keeps the P_{dyn} and P_{leak} yields close to 100%. Although the P_{dyn} and P_{leak} yields are increasing with aging time for the NBB case, the ABB case is still showing higher yield values because the ABB circuit reduces the process variations impact. The total yield considering F_{clk}, P_{dyn}, and P_{leak} is displayed in Fig. 8(g). This total yield represents the percentage of dies that satisfy the F_{clk}, P_{dyn}, and P_{leak} constraints. The total yield is degraded from 67% at zero aging time to 35.9% at 10 years aging time for the NBB case. The ABB circuit keeps this yield close to 100% and reaches 97.1% at 10 years aging time.

C. Effect of Temperature on the ABB performance

The ABB design is performed at a temperature T = 125 °C that is the worst-case operating condition. When the operating temperature decreases, $|V_{tp}|$ increases by $(\Delta|V_{tp}|_T + \Delta|V_{tp}|_{NBTI})$, where $\Delta|V_{tp}|_T$ is the $|V_{tp}|$ increase due to temperature decrease and $\Delta|V_{tp}|_{NBTI}$ is the $|V_{tp}|$ increase due to NBTI. Decreasing the operating temperature results in increasing $\Delta|V_{tp}|_T$ [17] and decreasing $\Delta|V_{tp}|_{NBTI}$ (because K_{DC} is a function of temperature) [27]. This $|V_{tp}|$ change is sensed by the ABB sensing circuit and the corresponding body-bias voltage is generated. Therefore, the ABB circuit compensates also for temperature variations.

IV. Conclusion

The proposed ABB circuit has been shown to reduce the impacts of the NBTI aging and process variations. The ABB circuit consisted of a threshold voltage sensing circuit and an analog controller that generates the required body-bias voltage to compensate for NBTI aging and process variations. Post-layout simulation results, referring to an industrial hardware-calibrated STMicroelectronics 65-nm CMOS technology transistor model, showed that the proposed ABB compensates effectively for NBTI and process variations in a circuit block case study, extracted from a real microprocessor critical path. For example, the proposed ABB improved the F_{clk} yield from 74.4% to 99.7% at zero aging time and from 36.6% to 97.1% at 10 years aging time. In addition, the proposed ABB increases the total yield from 67% to 99.5% at zero aging time and from 35.9% to 97.1% at 10 years aging time. The main advantage of the proposed ABB is its lower area overhead compared to the previous state-of-the-art ABB techniques. Typically, the area overhead of the proposed ABB was less than that in [14]–[16].

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Hassan Mostafa (S'01–M'11) received the B.S. and M.A.Sc. degrees (hons.) in electronics from Cairo University, Cairo, Egypt, in 2001 and 2005, respectively, and the Ph.D. degree in electrical and computer engineering from the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, Canada, in 2011.

He is currently an NSERC Post-Doctoral Fellow with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, where he is involved in designing the next-generation field-programmable gate array (FPGA) in collaboration with Fujitsu Research Laboratories, Tokyo, Japan. He was involved in a project with Imec, Leuven, Belgium, in 2000. This project included modeling and fabricating the ion-sensitive field-effect transistor. He has authored or co-authored over 20 papers in international journals and conferences. His current research interests include analog circuits design, mixed-analog circuit design, low-power circuits, variation-tolerant design, soft error-tolerant design, statistical design methodologies, next generation FPGA, and Spintronics.

Mohab Anis (S'98–M'03–SM'09) received the B.S. degree (hons.) in electronics and communication engineering from Cairo University, Cairo, Egypt, in 1997, the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 1999 and 2003, respectively, the M.B.A. degree with a concentration in entrepreneurship and innovation, and the M.S. degree with a concentration in management of technology.

He is currently an Associate Professor with the Department of Electronics Engineering, the American University in Cairo, Cairo. Previously, he was a Tenured Associate Professor with the University of Waterloo, where he is currently an Adjunct Associate Professor. He has authored or co-authored over 100 papers in international journals and conferences and is the author of three books: *Multi-Threshold CMOS Digital Circuits-Managing Leakage Power* (Norwell, MA: Kluwer, 2003), *Low-Power Design of Nanometer FPGAs: Architecture and EDA* (San Mateo, CA: Morgan Kaufmann, 2009), and *Nanometer Variation-Tolerant SRAM: Circuits and Statistical Design for Yield* (New York: Springer, 2011). His current research interests include integrated circuit design and design automation for very large-scale integration systems in the nanometer regime.

Dr. Anis was the recipient of the 2009 Early Research Award from Ontario's Ministry of Research and Innovation, the 2004 Douglas R. Colton Medal for Research Excellence in recognition of his excellence in research, leading to new understanding and novel developments in microsystems in Canada, and the 2002 International Low-Power Design Contest. He is an Associate Editor of the *ACM Transactions on Design Automation of Electronic Systems*, the *Microelectronics Journal*, the *Journal of Circuits, Systems and Computers*, and the *ASP Journal of Low Power Electronics*. He has also been an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I since 2010 and the IEEE TRANSACTIONS ON VLSI SYSTEMS since 2011. From 2008 to 2009, he was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-II: EXPRESS BRIEFS. He is a Program Committee Member of several IEEE and ACM conferences. He was the General Chair of the 2010 International Conference on Microelectronics. He is an advocate of technological innovation, for which he founded INNOVETY LLC, Giza, Egypt, a management consulting and software development firm that focuses on innovation management practices.

Mohamed Elmasry (S'69–M'73–SM'79–F'88) was born in Cairo, Egypt, on December 24, 1943. He received the B.S. degree from Cairo University, Cairo, Egypt, in 1965, and the M.A.Sc. and Ph.D. degrees from the University of Ottawa, Ottawa, ON, Canada, in 1970 and 1974, respectively, all in electrical engineering.

He has worked in the area of digital integrated circuits and system design for the last 35 years. From 1965 to 1968, he was with Cairo University, and from 1972 to 1974, he was with Bell-Northern Research, Ottawa. Since 1974, he has been with the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, Canada, where, from 1986 to 1991, he was the NSERC/BNR Research Chair in very large-scale integration (VLSI) design. He is currently a Professor and the Founding Director of the VLSI Research Group, University of Waterloo. He has served as a Consultant to research laboratories in Canada, Japan, and the U.S. He is the Founding President of Pico Electronics, Inc., Waterloo. He has authored or co-authored over 400 papers and 14 books on integrated circuit design and design automation. He is the holder of several patents.

Dr. Elmasry was the recipient of several Canadian and international awards. He was with many professional organizations in different positions. He is a Founding Member of the Canadian Conference on VLSI, the Canadian Microelectronics Corporation, the International Conference on Microelectronics, MICRONET, and the Canadian Institute for Teaching Overseas. He is a Fellow of the Royal Society of Canada and the Canadian Academy of Engineers.