On-Chip Process Variations Compensation Using an Analog Adaptive Body Bias (A-ABB)

Hassan Mostafa, Mohab Anis, and Mohamed Elmasry

***Abstract*—An analog adaptive body bias (A-ABB) circuit is proposed in this paper. The A-ABB is used to compensate for die-to-die (D2D) and within-die (WID) parameter variations and accordingly, improves the circuit yield regarding the speed, the dynamic power, and the leakage power. The A-ABB consists of threshold voltage estimation circuits and analog control of the body bias performed by on-chip amplifier circuits. Circuit level simulation results of a circuit block case study, extracted from a real microprocessor critical path, referring to an industrial hardware-calibrated 65-nm CMOS technology transistor model, are demonstrated. This study shows that the proposed A-ABB reduces the standard deviations of the frequency, the dynamic power and the leakage power by factors of 6.6×, 8.8×, and 3.3×, respectively, when both D2D and WID variations are considered. In addition, in this presented case study, initial total yields of 16.8% and 5.2% are improved to 99.9% and 84.1%, respectively. The advantage of the proposed A-ABB is its lower area overhead allowing it to be used at lower granularity level than that of the previously published ABB circuits.**

***Index Terms*—Adaptive body bias (ABB), die-to-die (D2D) variations, parametric yield, process variations, within-die (WID) variations.**

I. Introduction

As CMOS technologies continue to scale towards the nanometer regime, the device parameters, such as threshold voltage, channel length, oxide thickness, and mobility, exhibit large statistical process variations [1]–[6]. These process variations are expected to worsen in future technologies, due to difficulties with printing nanometer scale geometries in standard lithography. Therefore, these variations are considered the primary design challenge as CMOS technology scales [1]–[3] and [7]. Process variations are classified as die-to-die (D2D) variations and within-die (WID) variations. In D2D variations, all the devices on the same die are assumed to have the same parameter values. However, the devices on the same die are assumed to behave differently, in WID variations [1]. Although D2D variations are originally considered the main source of process variations, WID variations have become the major design challenge as technology scales [2].

Adaptive body bias (ABB) allows the tuning of the transistor threshold voltage, V_t, by controlling the transistor body-to-source voltage, V_{BS}. A forward body bias (FBB) (i.e., $V_{BS} > 0$) reduces V_t, increasing the device speed at the expense of increased leakage power. Alternatively, a reverse body bias (RBB) (i.e., $V_{BS} < 0$) increases V_t, reducing the leakage power but slowing the device. Therefore, the impact of process variations is mitigated by speeding up slow and less leaky devices or slowing down devices that are fast and highly leaky [8] and [9]. The effect of the body terminal on controlling the transistor V_t is reduced with technology scaling which decreases the ability of the ABB circuit to reduce the process variations. For example, in 150-nm technology, the body terminal of the device is capable of changing the nMOS transistor V_t by ±64 mV whereas in 65-nm technology, the nMOS V_t is changed by ±52 mV through body biasing. Thus, although the ABB impact is reduced with technology scaling, it is still required for advanced CMOS technologies as reported recently in [10] and [11].

Practically, the implementation of the ABB is desirable to bias each device in a design independently, to mitigate D2D and WID variations. However, supplying so many separate voltages inside a die results in a large area overhead. On the other hand, using the same body bias for all devices on the same die limits their capability to compensate for WID variations. Thus, the granularity level of the ABB scheme is a tradeoff between the target yield and the associated area overhead. Recently, researchers have attempted to use ABB to maximize the system clock frequency or minimize the leakage power.

In [12], ABB is used to compensate for process variations by maximizing the die frequency subject to a power constraint. Also, ABB is used in [13] by estimating the process parameters and using a digital controller to control the body bias. In this paper, a novel analog ABB (A-ABB) circuit is proposed. It is based on V_t estimation circuits and adaptive control of the body bias, achieved by on-chip amplifier circuits. These amplifier circuits generate the appropriate body bias voltage based on the V_t fluctuations. The main advantage of the A-ABB circuit is its lower area overhead compared to the ABB circuits published in [12] and [13].

The rest of this paper is organized as follows. In Section II, the A-ABB circuit is analyzed. Simulation results are given in Section III. In Section IV, the A-ABB is compared with previous ABB circuits. Finally, some conclusions are drawn in Section V.

II. Proposed A-ABB Circuit

A. A-ABB Derivations

In the proposed A-ABB circuit, the effect of the process variations on V_t is compensated by estimating the actual values of V_t, which are impacted by process variations. This estimation is achieved by placing the V_t estimation circuits close to the critical path. Then, the analog amplifiers generate the appropriate body bias voltage V_{BS} to compensate for the impact of the process variations.

The ABB circuit is basically utilized for reducing the D2D and the systematic WID variations that exhibit high spatial correlation (i.e., two devices separated by a close distance behave more similarly than two devices spaced farther apart). Accordingly, there is a tradeoff between the ABB granularity level and the associated area overhead (i.e., the lower the granularity level is, the higher the associated area overhead and more systematic WID variations reduction). The ABB circuits are not efficient for random WID variations compensation because these random variations are spatially uncorrelated. In [14], it is stated that high performance digital logic circuits such as the microprocessor critical paths case study introduced in this paper, at high V_{DD}, are strongly affected by spatially correlated channel length variations. These channel length variations are mapped to the threshold voltage, V_t, due to the drain-induced-barrier-lowering (DIBL) short channel effect resulting in large systematic V_t WID variations.

In [8] and [15], the relationship between V_t and V_{BS} for an nMOS transistor is given by

$$V_t = V_{to} + \Delta V_t|_{BB}$$
$$\Delta V_t|_{BB} = \gamma\left(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}\right) \quad (1)$$

where V_{to} is the nMOS transistor threshold voltage at zero body bias (i.e., when $V_{BS} = 0$), $\Delta V_t|_{BB}$ is the body bias effect on V_t, γ is the body effect coefficient, and ϕ_F is the Fermi potential with respect to the

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TABLE I
65-nm TECHNOLOGY INFORMATION AT $T = 120\,^{\circ}\mathrm{C}$

	nMOS	pMOS
V_{to} (V)	0.352	-0.204
ϕ_F (V)	0.467	0.439
γ (dimensionless)	0.296	0.174

mid-gap in the substrate [15]. If V_{to} is increased due to the process variations by $\Delta V_t|_{PV}$. Therefore, V_{BS} compensates for this process variations impact by producing a threshold voltage change $\Delta V_t|_{BB}$ that cancels out the process variations change, $\Delta V_t|_{PV}$ (i.e., $\Delta V_t|_{BB} = -\Delta V_t|_{PV}$). The value of V_{BS} that compensates for the process variations change is given by

$$V_{BS} = \frac{2\sqrt{2\phi_F}}{\gamma} \times \Delta V_t|_{PV} - \frac{1}{\gamma^2}(\Delta V_t|_{PV})^2 \tag{2}$$

where $\Delta V_t|_{PV}$ is the difference between the estimated threshold voltage V_{te}, which is impacted by the process variations and the nominal threshold voltage V_{to}. Similarly, for the pMOS transistors, the relationship in (2) is used by replacing V_{BS} by V_{SB}. Typically, the sources of the nMOS transistors are connected to the ground (zero voltage) and the sources of the pMOS transistors are connected to the supply voltage V_{DD}. Therefore, the body bias voltages of the nMOS transistors, V_{Bn} and the pMOS transistors V_{Bp}, which result in process variations compensation, are expressed as

$$V_{Bn} = \frac{2\sqrt{2\phi_{F_n}}}{\gamma_n}[V_{tne} - V_{tno}] - \frac{1}{\gamma_n^2}[V_{tne} - V_{tno}]^2 \tag{3}$$

$$V_{Bp} = V_{DD} - \frac{2\sqrt{2\phi_{F_p}}}{\gamma_p}[|V_{tpe}| - |V_{tpo}|] + \frac{1}{\gamma_p^2}[|V_{tpe}| - |V_{tpo}|]^2. \tag{4}$$

The values of the transistor parameters V_{to}, ϕ_F, and γ are extracted from the transistor model and are tabulated in Table I.

The junction leakage current and the breakdown considerations determine the RBB voltage bound, while the FBB is limited by the subthreshold leakage current and the forward biasing of the drain-bulk junction. Accordingly, the FBB and the RBB maximum voltages are set to $\pm$ 0.5 V [12] (i.e., the body bias voltage changes around its normal value by $\pm$ 0.5 V).

Accordingly, (3) and (4) are linearized and approximated by

$$V_{Bn} = A_n \times [V_{tne} - V_{tno}] \tag{5}$$

$$V_{Bp} = V_{DD} - A_p \times [V_{tpe} - V_{tpo}] \tag{6}$$

where A_n and A_p are constant gains and equal 6.3 and 10.8, respectively.

B. A-ABB Circuit Design

The proposed A-ABB circuit is depicted in Fig. 1(a) and (b) for the bias voltages, V_{Bn} and V_{Bp}, respectively. A set of sensing circuits is used to estimate the actual values of the threshold voltages, which are impacted by the process variations [13].

In the nMOS threshold voltage sensing circuit, shown in Fig. 1(a), the pMOS transistor is sized with minimum area and acts as a current source. The nMOS transistor is a diode-connected transistor and V_{REF}

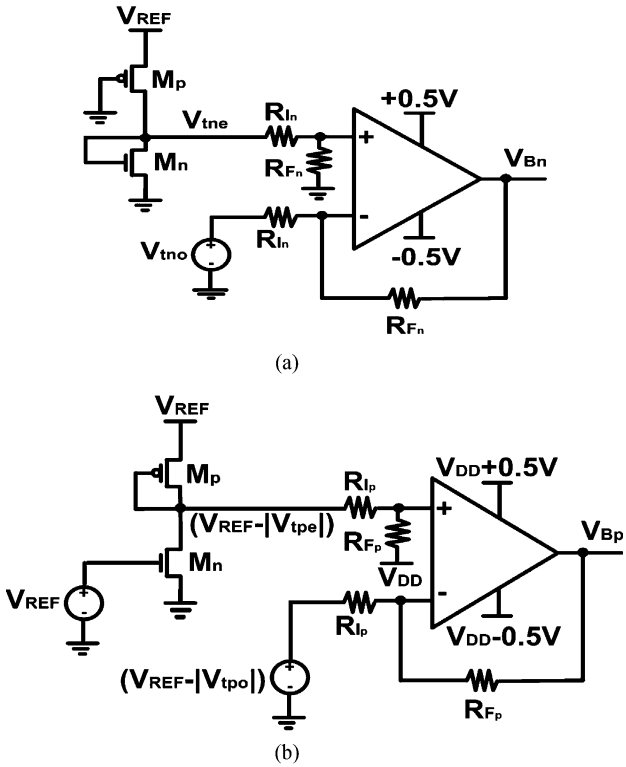

Fig. 1. A-ABB for (a) nMOS body bias control V_{Bn} and (b) pMOS body bias control V_{Bp}.

is a reference voltage. By using the α-power law model, introduced in [16] and equating the dc currents of the nMOS and pMOS transistors, the output voltage of this circuit V_{outn} is stated as

$$V_{\mathrm{outn}} = V_{tn} + r_n \times [V_{\mathrm{REF}} - |V_{tp}|]$$
$$r_n = \left(\frac{k_{p'}\frac{W}{L}|_p}{k_{n'}\frac{W}{L}|_n}\right)^{1/\alpha} \tag{7}$$

where V_{tn} and $|V_{tp}|$ are the threshold voltages, $k_{n'}$ and $k_{p'}$ are the technological parameters and $W/L|_n$ and $W/L|_p$ are the sizes of the nMOS and the pMOS transistors, respectively. By sizing this circuit such that $W/L|_n \gg W/L|_p$, (7) is rewritten as

$$V_{\mathrm{outn}} \approx V_{tn}. \tag{8}$$

Therefore, the output voltage of the nMOS threshold voltage sensing circuit represents the actual nMOS transistor threshold voltage, which is impacted by the process variations and, denoted by V_{tne}.

Similarly, by sizing the pMOS threshold voltage sensing circuit, depicted in Fig. 1(b), such that $W/L|_p \gg W/L|_n$, the output voltage of this circuit V_{outp} is given by

$$V_{\mathrm{outp}} \approx V_{\mathrm{REF}} - |V_{tp}|. \tag{9}$$

This output voltage is denoted by $V_{\mathrm{REF}} - |V_{tpe}|$ and represents the actual pMOS transistor threshold voltage, which is impacted by process variations.

SPICE simulations are performed by sweeping the threshold voltage parameters of the industrial 65 nm CMOS technology transistor model and using $V_{\mathrm{REF}} = 0.5$ V, $r_n = r_p \approx 0.075$. The estimated threshold voltages values are in good agreement with the actual values, which proves that the threshold voltage sensing circuits are effective in

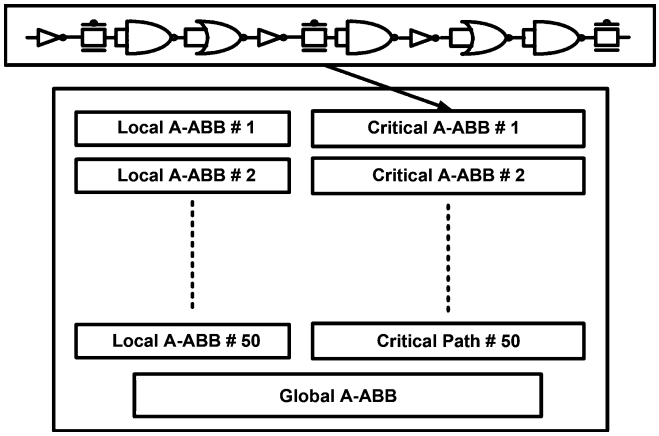

Fig. 2. Test circuit used in the simulation setup.

nanometer technologies. The maximum error between the estimated threshold voltage values and their corresponding actual values is 4.5% and the average error is 2.7%.

The amplifier circuit, shown in Fig. 1(a), is designed such that $R_{F_n}/R_{I_n} = 6.3$ whereas, the amplifier circuit, shown in Fig. 1(b), is designed such that $R_{F_p}/R_{I_p} = 10.8$.

C. Effect of Process and Temperature Variations on the Proposed A-ABB Circuit

A 5000 point Monte Carlo analysis, including the mismatch between transistors and resistors is performed. An industrial hardware-calibrated 65-nm CMOS technology transistor statistical models are used to investigate the effect of process variations on the proposed A-ABB circuit.

The process variations (D2D and WID variations) are included in the design kit and declared by STMicroelectronics to be Silicon verified. Simulation results reveal that the ratios between the standard deviations of the nMOS and pMOS sensing circuits outputs to their mean values are less than 1.3%. The amplifiers gains exhibit standard deviations to means ratios less than 0.6%. Therefore, the A-ABB circuit is insensitive to process variations. In addition, the sensing and amplifier circuits are found to be insensitive to the temperature variations in the range of $-30\,^{\circ}$C to $120\,^{\circ}$C. The maximum change in the sensing circuits outputs and the amplifier circuits gains, relative to their nominal values, is less than 0.3% and 0.8%, respectively, over the specified temperature range.

III. Simulation Results and Discussions

A. Test Circuit Description

The newly developed A-ABB circuit is applied to a circuit block, extracted from a real microprocessor critical path, to verify its effectiveness in process variations compensation. This circuit block consists of 11 CMOS gates including CMOS inverter gates, NAND gates, NOR gates, and transmission gates, similar to the test circuits used in [12] and [13]. Fig. 2 portrays the test circuit, which consists of 50 critical paths, a global A-ABB circuit and 50 local A-ABB circuits. The global A-ABB provides same bias voltages to all the die critical paths. Therefore, its effectiveness, in reducing WID variations, is limited. The distributed local A-ABB circuits supply different bias voltages to each critical path, achieving better results in reducing WID variations, at the expense of higher area overhead than that in the global A-ABB circuit.

This circuit block is selected to model the effect of the proposed A-ABB on the yield improvement of a real microprocessor design [13]. The figures of merit considered in this experiment are the oscillation frequency ($F_{\rm clk}$), the dynamic power ($P_{\rm dyn}$) of the circuit block when configured as a ring oscillator and the leakage power ($P_{\rm leak}$) of the circuit block when operating in static conditions [13]. The circuit block and the A-ABB circuits are implemented by using an industrial hardware-calibrated 65-nm CMOS technology. The supply voltage, $V_{\rm DD}$, equals 1.0 V and circuit level simulations are conducted. The effectiveness of the proposed A-ABB circuit is proved by showing its ability on reducing the D2D and WID variations.

B. Simulation Setup

First, the global A-ABB circuit is enabled and all the local A-ABB circuits are disabled. The global A-ABB sensing circuit is placed close to any critical path (critical path number 50 is selected in this test circuit). Based on the threshold voltage variations of this critical path, the global A-ABB provides the body bias voltages to all the die critical paths. Since the body bias voltages are determined based on the threshold voltage calculations of a single critical path, this global A-ABB circuit does not reduce the WID variations effectively.

Following that, the local A-ABB circuits are enabled and the global A-ABB is disabled. Each local A-ABB sensing circuit is placed close to its corresponding critical path, as shown in Fig. 2 and supplies the appropriate body bias voltages to this critical path. Therefore, the use of the local A-ABB is very efficient in accounting for WID variations. The granularity level of the global A-ABB circuit is the whole die while the granularity level of the local A-ABB circuits is the critical path.

The Monte Carlo analysis generates 5000 different dies. In each Monte Carlo statistical run (which is corresponding to a certain die), the die frequency is calculated as the minimum frequency of the die critical paths. Since the real microprocessor die contains hundreds of critical paths, the die power (i.e., the dynamic power and the leakage power) is calculated as the average power per critical path. This is performed by summing the critical paths powers and dividing by the number of critical paths per die.

C. Global A-ABB Versus Local A-ABB

1) Global A-ABB: In this case, the global A-ABB circuit is enabled and all the local A-ABB circuits are disabled. The following observations are extracted for the global A-ABB control case.

- The global A-ABB circuit reduces the standard deviations of $F_{\rm clk}$ $P_{\rm dyn}$ and $P_{\rm leak}$ (i.e., $\sigma_{F_{\rm clk}}$, $\sigma_{P_{\rm dyn}}$ and $\sigma_{P_{\rm leak}}$), by factors of 4.2×, 3.6×, and 1.9×, respectively, when WID variations are ignored and by factors of 4×, 2.4×, and 1.5×, respectively, when WID variations are considered.
- From the above results, the global A-ABB circuit is better for D2D variations compensation than for WID variations compensation. This result is because only one A-ABB circuit is used for all the die critical paths. Therefore, the utilization of a local A-ABB circuit for each critical path is essential to minimize the effects of the WID variations.

2) Local A-ABB: In this case, the global A-ABB circuit is disabled and all the local A-ABB circuits are enabled.

The following observations are extracted for the local A-ABB control case.

- The local A-ABB circuits achieve slightly more process variations reduction than that of the global A-ABB circuit, when WID variations are ignored. This is expected since when WID variations are ignored, the global A-ABB is sufficient and no need for the local A-ABB.
- When WID variations are taken into account, the local A-ABB circuits achieve significantly more process variations reduction than that of the global A-ABB circuit. For example, $F_{\rm clk}$, $P_{\rm dyn}$, and $P_{\rm leak}$ standard deviations are reduced by factors of 6.6×, 8.8×, and 3.3×. This demonstrates the need for the local A-ABB for WID variations compensation.

IV. Comparison With Previous ABB Realizations

Holding a direct comparison with previous ABB circuits is not viable because of the different technology and different goal in process variations compensation. In the following comparison, the performance of the A-ABB in reducing process variations and the associated area overhead are the aspects of comparison with the previous ABB circuits in [12] and [13].

A. Process Variations Compensation

1) Comparison With the ABB in [12]: The results in [12] are obtained from test chip measurements. According to Section III-C, the global A-ABB circuit and the local A-ABB circuits result in a reduction of the relative standard deviation of the clock frequency ($\sigma/\mu|_{F_{\rm clk}}$) by factors of 4× and 6.6×, respectively, for 65-nm CMOS technology. In [12], it is reported that the $\sigma/\mu|_{F_{\rm clk}}$ is reduced by factors of 4.1× and 5.9×, respectively, for 150-nm CMOS technology. Thus, the A-ABB circuits exhibit approximately same (for global A-ABB) or larger (for local A-ABB) process variations reduction than that in the ABB circuit in [12], taking into account that the 65-nm CMOS technology, used in this paper, introduces more process variations than the 150-nm CMOS technology, adopted in [12].

2) Comparison With the ABB in [13]: In [13], circuit level simulations results are reported for 130-nm CMOS technology, when only global ABB circuit is adopted. The only D2D variations case and both D2D and WID variations case are considered at a temperature of $T = 120\,^{\circ}$C. Thus, in the following comparison, only the global A-ABB is considered.

In [13], it is reported that adopting the ABB scheme and considering only the D2D variations, results in increasing the overall yield from 16.8% to 100%. Also, when both the D2D and the WID variations are considered, the overall yield increases from 13% to 86.8%. The global A-ABB is capable of improving the overall yield from 16.8% to 99.9% when only the D2D variations are considered. When both the D2D and the WID variations are considered, the global A-ABB increases the overall yield from 5.2% to 84.1%. Accordingly, the global A-ABB circuit is capable of achieving an overall yield close to that in [13]. It should be noted that the 65-nm CMOS technology, used in this paper, introduces more process variations than the 130-nm CMOS technology, adopted in [13].

B. Associated Area Overhead

The newly developed A-ABB circuit comprises of two sensing circuits and two amplifiers. In the ABB circuit in [12], a critical path mimic is used and the desired clock frequency is applied externally. The output of the critical path mimic is compared to the externally applied clock frequency by using a phase detector (PD). The output of the PD is used to enable a 5-bit digital counter whose value represents the desired body bias to apply. Finally, the 5-bit digital output from the counter is converted to an analog body bias voltage by using a digital-to-analog converter (DAC) followed by a bias amplifier. Therefore, the ABB in [12] consists of a critical path mimic, PD, two 5-bit counters, two 5-bit DAC circuits and two bias amplifier circuits.

The ABB circuit reported in [13] utilizes a set of threshold voltage sensing circuits to estimate the actual threshold voltage values. The output of these sensing circuits is converted to a digital word by using an analog-to-digital converter (ADC). A control unit is used to select the optimum body bias code stored in a programmable read only memory (PROM) unit, based on the ADC output word. The output of the PROM is then converted to an analog body bias voltage by using a DAC followed by a bias amplifier. Therefore, the ABB in [13] consists of two sensing circuits, two ADCs, control unit, PROM, two DACs, and two bias amplifier circuits.

From the above discussion, the A-ABB circuit exhibits lower area overhead compared to [12] and [13]. This low area overhead allows the use of the A-ABB at smaller granularity level (i.e., critical path level or cluster of gates level) with lower area overhead than that of the ABB circuits in [12] and [13].

C. Design Considerations

1) The resolution of the DAC and/or the ADC, used in the ABB circuits in [12] and [13] limits their capability in process variations compensation. For example, it is reported in [12] through test chip measurements that 300 mV bias resolution results in relative frequency variations $\sigma/\mu|_{F_{\rm clk}} = 1.47\%$ whereas using 32 mV bias resolution reduces $\sigma/\mu|_{F_{\rm clk}}$ to 0.69%. The A-ABB does not suffer from this resolution limit because no ADC or DAC is required in the A-ABB circuit.
2) There are several design issues that will increase the area overhead of the A-ABB such as the guard rings (to isolate analog and digital circuits), triple-well process (for nMOS body bias control) and excess power grid routing requirements. These area overheads are the same for the A-ABB and any ABB circuit such as the ABB circuits in [12] and [13]. Thus, these area overheads are not included in the comparison introduced in Section IV.
3) In [17] and [18], the impact of the low granularity (fine-grain) ABB on the test cost is discussed. In [17], statistical analysis on several benchmarks circuits shows that the ABB design maintains the test cost at its minimum under process variations while keeping the test quality at its highest level. This is because the adoption of the ABB makes slow critical paths faster which results in reducing the number of critical paths to be tested. In addition, the work in [18] introduces a gate clustering method for minimizing the test cost when fine-grain ABB is used. Accordingly, the increase in the testing workload, when the fine-grain ABB is used, is reduced by applying this gate clustering method given that the number of critical paths to be tested is decreased.

V. Conclusion

The A-ABB circuit consists of threshold voltage sensing circuits and on-chip amplifier circuits that generate the required body bias voltages to compensate for process variations. Simulation results show that when both D2D and WID variations are taken into account, the proposed global A-ABB results in frequency, dynamic power and leakage power variations reduction by factors of 4×, 2.4×, and 1.5×, respectively. Whereas when the local A-ABB circuits are used, the frequency, dynamic power and leakage power variations are reduced by factors of 6.6×, 8.8×, and 3.3×, respectively. The main advantage of the proposed A-ABB is its low area overhead compared to the previous state-of-the-art ABB techniques. Therefore, it can be used at a smaller granularity level (fine-grain).

References

[1] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter variations and impact on circuits and microarchitecture," in *Proc. 40th Conf. Des. Autom. (DAC)*, 2003, pp. 338–342.
[2] H. Masuda, S. Ohkawa, A. Kurokawa, and M. Aoki, "Challenge: Variability characterization and modeling for 65-nm to 90-nm processes," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2005, pp. 593–599.
[3] M. Meterelliyoz, P. Song, F. Stellari, J. P. Kulkarni, and K. Roy, "Characterization of random process variations using ultralow-power, high-sensitivity, bias-free sub-threshold process sensor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1838–1847, Aug. 2010.
[4] S. Borkar, T. Karnik, and V. De, "Design and reliability challenges in nanometer technologies," in *Proc. 41st Conf. Des. Autom. (DAC)*, 2004, p. 75.

[5] K. Bowman, S. Duvall, and J. Meindl, "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration," *IEEE J. Solid-State Circuits*, vol. 37, no. 2, pp. 183–190, Feb. 2002.

[6] A. Keshavarzi, G. Schrom, S. Tang, S. Ma, K. Bowman, S. Tyagi, K. Zhang, T. Linton, N. Hakim, S. Duvall, J. Brews, and V. De, "Measurements and modeling of intrinsic fluctuations in MOSFET threshold voltage," in *Proc. Int. Symp. Low Power Electron. Des. (ISLPED)*, 2005, pp. 26–29.

[7] ITRS, "The International Technology Roadmap for Semiconductors," 2010. [Online]. Available: http://public.itrs.net

[8] S. H. Kulkarni, D. M. Sylvester, and D. Blaauw, "Design-time optimization of post-silicon tuned circuits using adaptive body bias," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 27, no. 3, pp. 481–494, Mar. 2008.

[9] J. Gregg and T. W. Chen, "Post silicon power/performance optimization in the presence of process variations using individual well-adaptive body biasing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 3, pp. 366–376, Mar. 2007.

[10] H. Jeon, Y. Kim, and M. Choi, "Standby leakage power reduction technique for nanoscale CMOS VLSI systems," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 5, pp. 1127–1133, May 2010.

[11] K. Kang, S. P. Park, K. Kim, and K. Roy, "On-chip variability sensor using phase-locked loop for detecting and correcting parametric timing failures," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 2, pp. 270–280, Feb. 2010.

[12] J. W. Tschanz, J. T. Kao, S. G. Narendra, R. Nair, D. A. Antoiadis, A. P. Chandrakasan, and V. De, "Adaptive body bias for reducing impacts of die-to-Die and within-die parameter variations on microprocessor frequency and leakage," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1396–1402, Nov. 2002.

[13] M. Olivieri, G. Scotti, and A. Trifiletti, "A novel yield optimization technique for digital CMOS circuits design by means of process parameters run-time estimation and body bias active control," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 5, pp. 630–638, May 2005.

[14] N. Drego, A. Chandrakasan, and D. Boning, "Lack of spatial correlation in MOSFET threshold voltage variation and implications for voltage scaling," *IEEE Trans. Semicond. Manuf.*, vol. 22, no. 2, pp. 245–255, May 2009.

[15] L. William, *MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4*. New York: Wiley, 2001.

[16] T. Sakurai and A. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, Apr. 1990.

[17] B. Paul and K. Roy, "Impact of body bias on delay fault testing of sub-100 nm CMOS circuits," *J. Electron. Test., Theory Appl.*, vol. 22, no. 2, pp. 115–124, Apr. 2006.

[18] K. Hamamoto, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Tuning-friendly body bias clustering for compensating random variability in subthreshold circuits," in *Proc. IEEE Int. Symp. Low Power Electron. Des. (ISLPED)*, 2009, pp. 51–56.