Adaptive Body Bias for Reducing the Impacts of NBTI and Process Variations on 6T SRAM Cells

Hassan Mostafa, *Student Member, IEEE*, Mohab Anis, *Senior Member, IEEE*, and Mohamed Elmasry, *Fellow, IEEE*

***Abstract*—Reliability and variability have become big design challenges facing submicrometer SRAM designers. A low area overhead adaptive body bias (ABB) circuit is proposed in this paper to compensate for NBTI aging and process variations to improve the SRAM reliability and yield. The proposed ABB circuit consists of a threshold voltage sensing circuit and an on-chip analog controller. Postlayout simulation results, referring to an industrial hardware-calibrated STMicroelectronics 65 nm CMOS technology transistor model, are presented. The transistor model contains process variations and NBTI aging model cards, which are declared by STMicroelectronics to be silicon verified. Cadence RelXpert, Virtuoso Spectre, and Virtuoso UltraSim tools are used to estimate the NBTI aging and process variations impacts on the SRAM array. These results show that the proposed ABB compensates effectively for NBTI aging and process variations. For example, the proposed ABB reduces the read failure probability from 0.32% to 0.05% and the SNM degradation from 10.9% to 2.6% at 10 years aging time. In addition, the proposed ABB enhances the soft errors immunity of the SRAM cell by reducing the critical charge degradation from 12.7% to 3.4% at 10 years aging time.**

***Index Terms*—Adaptive body bias, deep submicrometer, negative bias temperature instability, process variations, soft errors, SRAM cells.**

I. Introduction

RELIABILITY is one of the major design challenges facing submicrometer static random access memories (SRAMs) designers. Shrinking geometries, lower power supplies, higher clock frequencies, and higher density circuits all have a great impact on SRAM reliability [1]–[3]. As CMOS technology scales, soft errors and negative bias temperature instability (NBTI) become the major reliability concerns.

Soft errors, caused by Alpha particles and high energy neutrons [2], [3], induce a current pulse that disturbs the circuit node voltage [1]. In SRAMs, this disturbance causes bit flips (a 0-to-1 flip or a 1-to-0 flip) if the charge collected by the particle strike at the storage node, is more than a minimum value called critical charge (Q_{critical}). Q_{critical} is used as a measure of the SRAM vulnerability to soft errors [1], [4]. This Q_{critical} exhibits an exponential relationship with the soft error rate (SER) [1], and consequently, Q_{critical} should be designed high enough, to limit the SER. SRAM cells are vulnerable to soft errors due to their lower node capacitance.

NBTI is the generation of interface traps under negative bias conditions (i.e., $V_{GS} = -V_{DD}$) at elevated temperatures in pMOS transistors. NBTI is a growing threat to circuit reliability in scaled CMOS technologies [5]–[8]. These interface traps are formed due to crystal mismatches at the Si-SiO_2 interface. During Si oxidation, the majority of the atoms are bonded to oxygen, whereas some of the atoms are bonded with hydrogen, leading to the formation of weak Si-H bonds. When a pMOS transistor is negatively biased, the holes in the channel dissociate these weak Si-H bonds and the interface traps are formed. These traps are electrically active physical defects with their energy distributed between the valence band and the conduction band in the band diagram [9], resulting in an increase in the absolute pMOS transistor threshold voltage, $|V_{\mathrm{tp}}|$. This $|V_{\mathrm{tp}}|$ increase not only leads to reduced temporal performance but also causes reliability degradation and potential device failure [9]. Typically, this $|V_{\mathrm{tp}}|$ increase results in increasing the SRAM SER (because it decreases the strength of the SRAM pMOS transistors which reduces Q_{critical} [10]), reducing the SRAM static noise margin (SNM) [11], [12], and increasing the read failure probability which results in SRAM yield loss [12].

Moreover, SRAM cells show the largest sensitivity to process variations due to their small device sizes. Process variations in logic circuits cause delay spread which reduces the parametric yield, whereas, for SRAM cells, process variations cause the memory to functionally fail, which reduces the functional yield. The aggressive scaling of CMOS technology towards the nanometer regime has created large statistical process variations in the transistor parameters such as threshold voltage, channel length, and mobility. Therefore, the process variations are considered one of the most important design challenges for sub-100-nm CMOS technologies. These process variations are classified into die-to-die (D2D) variations and within-die (WID) variations. In D2D variations, all the devices on the same die are assumed to have the same parameters. However, the devices on the same die are assumed to behave differently for WID variations.

Adaptive body bias (ABB) allows the tuning of the transistor threshold voltage, V_t, by controlling the transistor body-to-source voltage, V_{BS}. A forward body bias (FBB) reduces V_t whereas a reverse body bias (RBB) increases V_t. Therefore, the impacts of NBTI and process variations are mitigated by adopting the ABB technique. Practically, the implementation of the ABB is desirable to bias each device

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in a design independently (local ABB), to mitigate D2D and WID variations. However, supplying so many separate voltages inside a die results in a large area overhead. On the other hand, using the same body bias for all devices on the same die (global ABB) limits their capability to compensate for WID variations [13].

The effect of the body terminal on controlling the transistor V_t is reduced with technology scaling which decreases the ability of the ABB circuit to reduce the process variations. For example, in 150 nm technology, the body terminal of the device is capable of changing the pMOS transistor V_t by ± 64 mV whereas in 65 nm technology, the pMOS V_t is changed by ± 52 mV through body biasing. Thus, although the ABB impact is reduced with technology scaling, it is still required for advanced CMOS technologies as reported recently in [14] and [15].

In [13] and [16], ABB is used to compensate for process variations and yield improvement by estimating the process parameters and using a digital controller to control the body bias. Recently, several NBTI monitoring circuits are introduced in [17]–[19]. These monitoring circuits output can be fed to an ABB circuit to compensate for the NBTI impact. These monitoring circuits utilize a phase locked loop (PLL) technique to determine the pMOS transistor deviation digitally and require a digital to analog converter (DAC) to convert this digital deviation to the appropriate body bias voltage, which is obtained by using a digital control module. These requirements impose large area overhead which limits the applicability of these circuits. In [20], the output of an NBTI sensing circuit is used as a measure of the NBTI stress and also this output is used as a body bias for the pMOS transistors in the actual circuit. The nonlinear relationships between this sensing circuit output voltage and the threshold voltage deviation and also between the body bias voltage and the threshold voltage limit the ability of this circuit to compensate for NBTI.

In this paper, an ABB circuit is adopted for NBTI compensation. It is based on estimating the stressed pMOS transistor threshold voltage, $|V_{\mathrm{tp_{stressed}}}|$, in conjunction with an adaptive body bias control circuit, achieved by an on-chip analog circuit. This analog circuit generates the appropriate body bias voltage, based on the $|V_{\mathrm{tp_{stressed}}}|$ deviations due to NBTI. The main advantage of this ABB circuit is its lower area overhead compared to the NBTI monitoring circuits published in [17]–[19] and higher NBTI and process variations impacts reduction compared to [20]. All the results reported in this paper are postlayout simulation results, referring to an industrial hardware-calibrated STMicroelectronics 65 nm CMOS technology where process variations and NBTI stress are included in the transistor model card and declared by STMicroelectronics to be Silicon verified. In addition, the process and temperature variations impact on the pMOS transistor threshold voltage is reduced due to this ABB circuit adoption as well.

This paper is organized as follows: Section II quantifies the impact of NBTI aging and process variations on the SRAM cells. Section III explains the proposed ABB circuit design. Simulation results are given in Section IV. Section V focuses on the factors that affect the proposed ABB performance. A comparison between the proposed ABB and the previously published NBTI compensation circuits is given in Section VI. Finally, some conclusions are drawn in Section VII.

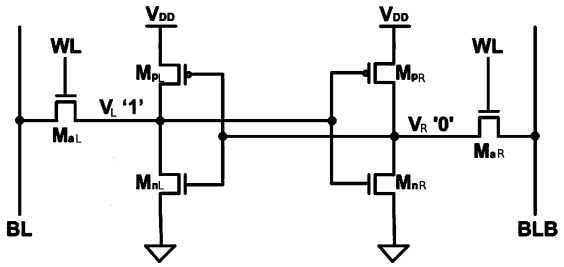

Fig. 1. The 6T SRAM cell with Node V_L is assumed to be at logic "1" and node V_R is assumed to be at logic "0."

II. The Impact of NBTI on SRAM Cells

In [12], [17], [21], it is stated that the pMOS transistor threshold voltage increase due to NBTI, $\Delta|V_{\mathrm{tp_{dc}}}|$, under constant dc stress (i.e., the pMOS transistor gate voltage is grounded), follows a power law model with respect to the aging time as follows [17], [21]:

$$\Delta|V_{\mathrm{tp_{dc}}}| = K_{\mathrm{dc}} \times t^{0.25} \tag{1}$$

where K_{dc} is a technology dependent parameter (i.e., K_{dc} is a function of temperature, supply voltage, device geometry, and interfacial traps density) and t is the aging time in seconds. In real circuit operation, the effective ON time of the pMOS transistor is bounded by the operating frequency and the gate input probability. During the OFF time (i.e., the pMOS transistor gate voltage is connected to the supply voltage), the pMOS transistor experiences a recovery process, where $|V_{\mathrm{tp}}|$ decreases back to its original value before stress [12]. Accordingly, the pMOS transistor threshold voltage increase due to NBTI, $\Delta|V_{\mathrm{tp_{ac}}}|$, under dynamic ac stress, is a scaled version of $\Delta|V_{\mathrm{tp_{dc}}}|$ and given by [12], [17], [21]

$$\Delta|V_{\mathrm{tp_{ac}}}| \approx \alpha \times \Delta|V_{\mathrm{tp_{dc}}}| = \alpha \times K_{\mathrm{dc}} \times t^{0.25} \tag{2}$$

where α is a prefactor dependent on the operating frequency and the gate input probability. In (12), it is reported that the pMOS transistor life time is much longer under ac stress than dc stress by a factor of 4X.

Fig. 1 shows a typical six transistor (6T) SRAM cell. Transistors M_{nL} and M_{nR} are the pull down nMOS transistors at the left and right sides, respectively, M_{pL} and M_{pR} are the pull up pMOS transistors at the left and right sides, respectively, and M_{aL} and M_{aR} are the access nMOS transistors at the left and right sides, respectively. Under NBTI degradation, the $|V_{\mathrm{tp}}|$ of the two pMOS transistors M_{pL} and M_{pR} increase with aging time according to (2). The gate input probabilities (the probability that the pMOS transistor is ON) at nodes V_L and V_R are denoted by p_L and p_R, respectively. Due to the symmetric structure of the SRAM cell, p_L and p_R add up to 1.0 (i.e., $p_L + p_R = 1.0$) [12]. Therefore, the $|V_{\mathrm{tp}}|$ degradation of the two pMOS transistors is not equal. In the following, the impact of the NBTI $|V_{\mathrm{tp}}|$ increase on the SRAM cell SNM, read failure

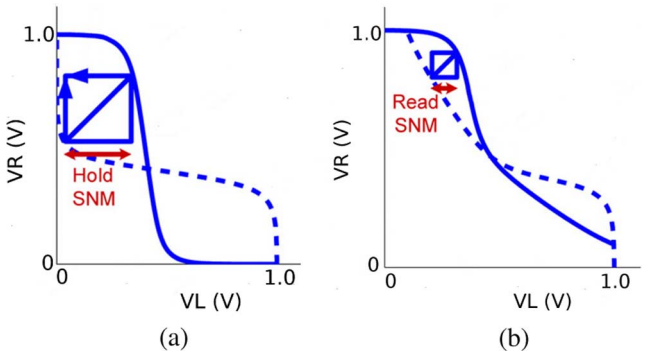

Fig. 2. The 6T SRAM cell SNM computation through the VTC curves for (a) HOLD mode when the word line is "0" and (b) READ mode when the word line is "1."

probability, read access time, write margin (WM), subthreshold leakage, and SER is discussed.

A. Static Noise Margin (SNM)

SNM is the noise stability measure of the SRAM cells and is defined as the minimum dc noise voltage necessary to change the state of the SRAM cell [22]. SNM is computed as the side length of a maximum square nested between the two voltage transfer characteristic (VTC) curves of the SRAM cell (i.e., one VTC for inverter M_{nL}-M_{pL} and the other VTC for inverter M_{nR}-M_{pR} as shown in Fig. 2. Depending on the SRAM operation, the SNM is classified as HOLD SNM (when the word line is "0" and the cell is holding the data) or READ SNM (when the word line is "1" and the data is read from the cell) as shown in Fig. 2 [12], [22].

The READ SNM is more sensitive to threshold voltage deviations than the HOLD SNM. This is because in the HOLD mode, the nodes V_L and V_R are strongly coupled to each other making the cell less sensitive to threshold voltage deviations. However, in the READ mode, the connection of the bit lines to nodes V_L and V_R through the access transistors increases the cell sensitivity to the threshold voltage deviations [12].

The SNM degrades over aging time under stressed conditions because the trip point of the left inverter is reduced due to the $|V_{\rm tp}|$ increase of transistor M_{pL} (assuming V_L = "1" and V_R = "0"). Accordingly, the cell becomes more vulnerable to flipping compared to the unstressed conditions [11]. In [12], it is shown that the HOLD SNM degrades by less than 3% whereas the READ SNM degrades by more than 10% at a temperature of 125 °C over 3 years aging time ($t = 10^8$ s) with $p_L = p_R = 0.5$.

B. Read Failure Probability and Read Access Time

Read failure probability is defined as the probability of a destructive read operation. The destructive read operation occurs when a voltage rise at the node storing "0" (i.e., V_R in Fig. 1) exceeds the trip point of the load inverter (i.e., M_{nL}-M_{pL} inverter in Fig. 1) and flips the original data during a read operation. This destructive read does not occur at the node storing "1" because the bit lines are charged to V_{DD} before the read operation. Correspondingly, the node storing "1" is not affected during the read operation. The main reason for read failures is the process variations which affect the device parameters. The primary sources of process variations are random dopant fluctuations (RDF) and channel length variations. The RDF variations are classified as random variations whereas the channel length variations are classified as systematic variations.

The read failure probability is affected by the process variations and the temperature variations as well as the aging NBTI effect. The aging NBTI effect results in increasing the read failure probability further by reducing the inverter trip point. In [11] and [12], the read failure probability increases under stressed conditions by a factor of 2.9X compared to the unstressed case at a temperature of 125 °C over 3 years aging time ($t = 10^8$ s) with $p_L = p_R = 0.5$. The read access time is not impacted by the NBTI because this time is determined by discharging the bit line through nMOS transistors M_{nR} and M_{aR} which are not affected by the NBTI (assuming V_R = "0" as shown in Fig. 1) (11).

C. Write Margin (WM)

WM is the measure of the SRAM cell write stability and is defined as the maximum BL voltage that cause the cell to flip when the BLB is kept at V_{DD} (assuming V_L = "1" and V_R = "0") [23]. As the pMOS transistor threshold voltage, $|V_{\rm tp}|$, increases with aging time due to NBTI, the node storing "1" (i.e., V_L in Fig. 1) gets weaker and writing a "0" to this node becomes easier [11], [12]. Accordingly, the WM improves (i.e., decreases) over aging time which also reduces the write failure probability. In [12], the WM is reduced by about 1.4% which reduces the write failure probability from 12% to 5% at a temperature of 125 °C over 3 years aging time ($t = 10^8$ s) with $p_L = p_R = 0.5$.

D. Subthreshold Leakage

As the pMOS transistor threshold voltage increases with aging time, the subthreshold leakage current decreases exponentially, and accordingly, the SRAM total leakage is reduced with aging. In [12], the leakage current of the SRAM cell is reduced by 13% at a temperature of 125 °C over 3 years aging time ($t = 10^8$ s) with $p_L = p_R = 0.5$. It should be noted that the leakage reduction is maximized when $p_L = p_R = 0.5$. However, if the gate input probabilities are not equal (i.e., $p_L \neq p_R$), one of the pMOS transistors exhibits more $|V_{\rm tp}|$ increase compared to the other. Unfortunately, the reduced leakage current through this higher $|V_{\rm tp}|$ transistor is compensated by less probabilities of OFF time. For example, if $p_L = 1.0$ and $p_R = 0$, there is no leakage reduction because the higher $|V_{\rm tp}|$ transistor (i.e., M_{pL} in this example) is always ON and accordingly, the leakage current is only determined through M_{pR}, which is not impacted by NBTI.

E. Soft Error Rate (SER)

For the proper operation of the SRAM cell, the pMOS pull-up transistors are sized to be weaker than the nMOS pull-down transistors. Consequently, the data node storing logic "1" (i.e., V_L in Fig. 1) is the most susceptible to particle strikes. It has been reported that $Q_{\rm critical}$ of a 0-to-1 flip in SRAM is about 22X larger than that for a 1-to-0 flip [10], [24]. When a particle strike occurs at node V_L, the injected current pulls this node voltage down to "0" against the pMOS transistor M_{pL} current

which tries to recover the node voltage. Due to NBTI, M_{pL} current is reduced due to the increased $|V_{\rm tp}|$ which reduces $Q_{\rm critical}$ and increases the SER. In [10], the sensitivity of $Q_{\rm critical}$ to transistor M_{pL} threshold voltage, $|V_{\rm tpL}|$, is given by:

$$\frac{\Delta Q_{\rm critical}}{\Delta |V_{\rm tpL}|} = -\frac{Q_{\rm critical}}{V_{DD} - |V_{\rm tpL}|} \tag{3}$$

where V_{DD} is the supply voltage. According to (3), $Q_{\rm critical}$ is reduced by 6.25% for $V_{DD} = 1.0$ V, $|V_{\rm tpL}| = 0.204$ V, and $\Delta|V_{\rm tpL}| = 50$ mV. This $Q_{\rm critical}$ reduction results in a large increase in the SER due to the exponential relationship, especially, in large size SRAM modules.

III. Proposed ABB Circuit

In the proposed ABB circuit, the effect of NBTI on $|V_{\rm tp}|$ is compensated by estimating the actual value of $|V_{\rm tp}|$, which is impacted by NBTI, by using an estimation circuit. Then, the analog controller generates the appropriate body bias voltage, $V_{\rm SB}$, to mitigate the NBTI impact. The analog controller is a direct implementation of the relationship between $|V_{\rm tp}|$ and $V_{\rm SB}$. In [21], [25], the relationship between $|V_{\rm tp}|$ and $V_{\rm SB}$ for a pMOS transistor is given by

$$\begin{aligned} |V_{\rm tp}| &= |V_{\rm tpo}| + \Delta|V_{\rm tp}|_{\rm BB} \text{ and} \\ \Delta|V_{\rm tp}|_{\rm BB} &= \gamma(\sqrt{2\phi_F - V_{\rm SB}} - \sqrt{2\phi_F}) \end{aligned} \tag{4}$$

where $|V_{\rm tpo}|$ is the pMOS transistor threshold voltage at zero body bias (i.e., when $V_{\rm SB} = 0$), $\Delta|V_{\rm tp}|_{\rm BB}$ is the body bias effect on $|V_{\rm tp}|$, γ is the body effect coefficient, and ϕ_F is the Fermi potential with respect to the mid-gap in the substrate [21]. If $|V_{\rm tpo}|$ is increased due to NBTI by $\Delta|V_{\rm tp}|_{\rm NBTI}$. Therefore, the body bias voltage, $V_{\rm SB}$, compensates for this NBTI by producing a threshold voltage change, $\Delta|V_{\rm tp}|_{\rm BB}$, that cancels out the NBTI change, $\Delta|V_{\rm tp}|_{\rm NBTI}$ (i.e., $\Delta|V_{\rm tp}|_{\rm BB} = \Delta|V_{\rm tp}|_{\rm NBTI}$). The value of $V_{\rm SB}$ that compensates for the NBTI change is given by

$$V_{\rm SB} = \frac{2\sqrt{2\phi_F}}{\gamma} \times \Delta|V_{\rm tp}|_{\rm NBTI} - \frac{1}{\gamma^2}(\Delta|V_{\rm tp}|_{\rm NBTI})^2 \tag{5}$$

where $\Delta|V_{\rm tp}|_{\rm NBTI}$ is the difference between the estimated threshold voltage, $|V_{\rm tp_{stressed}}|$, which is impacted by the NBTI, and the nominal threshold voltage, $|V_{\rm tpo}|$. Typically, the source of the pMOS transistor is connected to the supply voltage, V_{DD}. Therefore, the body bias voltages of the pMOS transistor, V_{Bp}, which result in NBTI compensation, is given by

$$\begin{aligned} V_{Bp} = V_{DD} - \frac{2\sqrt{2\phi_F}}{\gamma}[|V_{\rm tp_{stressed}}| - |V_{\rm tpo}|] \\ + \frac{1}{\gamma^2}[|V_{\rm tp_{stressed}}| - |V_{\rm tpo}|]^2. \end{aligned} \tag{6}$$

The proposed ABB circuit is depicted in Fig. 3 for the bias voltage V_{Bp}. The sensing circuit, shown in Fig. 3, is used to estimate the actual value of $|V_{\rm tp}|$, which is impacted by the NBTI under full stress (the worst case NBTI effect). This sensing circuit outputs an estimate for the pMOS threshold voltage, denoted by $V_{\rm out} = r(V_{DD} - |V_{\rm tp_{stressed}}|)$ which is applied to an amplifier circuit and a squaring circuit to produce the required bias voltage, which is capable of reducing the impact of NBTI.

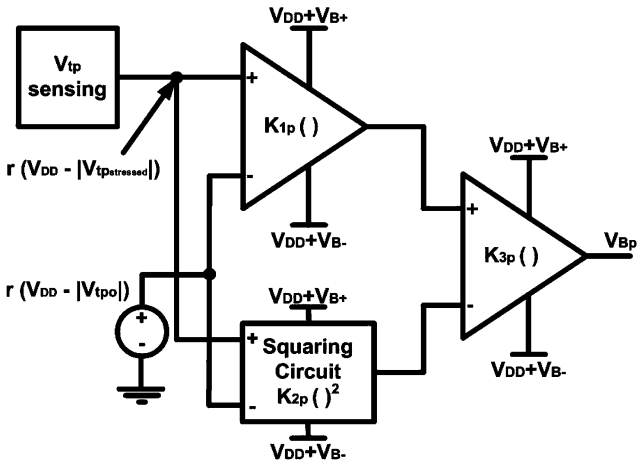

Fig. 3. The proposed ABB circuit for NBTI compensation.

In Fig. 3, the voltage source of the value $r(V_{DD} - |V_{\rm tpo}|)$ is a dc bias voltage representing the ratio r multiplied by the difference between the supply voltage, V_{DD}, and the pMOS transistor nominal threshold voltage value at zero body bias. The dc supply voltages of the amplifiers are set to $(V_{DD} + V_{B+})$ and $(V_{DD} + V_{B-})$ to limit the body bias voltage, V_{Bp}, and to implement (6). According to Fig. 3 and recalling (6), the gains K_{1p}, K_{2p}, and K_{3p} are given by:

$$K_{1p} \times K_{3p} = \frac{2\sqrt{2\phi_F}}{\gamma \times r} \text{ and } K_{2p} \times K_{3p} = -\frac{1}{\gamma^2 \times r^2}. \tag{7}$$

The ABB circuit is basically utilized for reducing the D2D and the systematic WID variations that exhibit high spatial correlation (i.e., two devices separated by a close distance behave more similarly than two devices spaced farther apart). Accordingly, there is a trade-off between the ABB granularity level and the associated area overhead (i.e., the lower the granularity level is, the higher the associated area overhead and more systematic WID variations reduction). The ABB circuits are not efficient for random WID variations compensation because these random variations are spatially uncorrelated. SRAM cells are affected by spatially correlated channel length variations. These channel length variations are mapped to the threshold voltage, $\rm V_t$, due to the drain-induced-barrier-lowering (DIBL) short channel effect resulting in large systematic $\rm V_t$ WID variations.

It should be mentioned that the proposed ABB is capable of compensating for both the NBTI and systematic process variations (D2D and WID variations) impacts. NBTI results on increasing $|V_{\rm tp}|$ with aging time, whereas systematic process variations result in increasing or decreasing $|V_{\rm tp}|$ by a fixed amount. Accordingly, if the resultant $|V_{\rm tp}|$ due to NBTI and variations is increased, FBB is supplied by the ABB circuit. On the other hand, if the resultant $|V_{\rm tp}|$ due to NBTI and variations is decreased, RBB is supplied by the ABB circuit. For example, at zero aging time, the percentage of SRAM arrays samples receiving RBB is 41% and the percentage of the samples receiving FBB is 59%. At an aging time of 10 years, the NBTI shift dominates and the percentage of the samples receiving FBB is 99%.

The implementations of the sensing circuit, the amplifiers, and the squaring circuit are given in the following discussions.

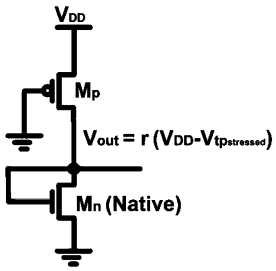

Fig. 4. The pMOS transistor $|V_{\rm tp}|$ sensing circuit.

A. Sensing Circuit

The sensing circuit, displayed in Fig. 4, is used to estimate the actual value of the threshold voltage of the pMOS transistor, which is impacted by NBTI under static dc stress. In this circuit, the pMOS transistor is sized with the same sizing as the SRAM pMOS transistor and the nMOS transistor is a native transistor. Native transistors are manufactured without additional threshold voltage implantation in the channel area and thus exhibit a natural threshold voltage in the manufacturing process. This natural threshold voltage is typically around 0 V (26). The minimum size of the native transistor as introduced by the industrial hardware-calibrated STMicroelectronics 65 nm CMOS technology is 500 nm/300 nm which is adopted in this sensing circuit.

By using the α—power law model, introduced in [27], and equating the dc currents of the nMOS and pMOS transistors, the output voltage of this circuit, $V_{\rm out}$, is expressed as:

$$\begin{aligned} V_{\rm out} &= V_{tn} + r \times [V_{DD} - |V_{\rm tp_{stressed}}|] \\ &\approx r \times [V_{DD} - |V_{\rm tp_{stressed}}|] \text{ and} \\ r &= \left(\frac{k_{p'} \frac{W}{L}|_p}{k_{n'} \frac{W}{L}|_n} \right)^{1/\alpha} \end{aligned} \tag{8}$$

where $k_{n'}$ and $k_{p'}$ are the technological parameters, and $W/L|_n$ and $W/L|_p$ are the sizes of the nMOS and the pMOS transistors, respectively. It should be noted that the native nMOS transistor threshold voltage, V_{tn}, is assumed to be 0 V in (8) [26].

Fig. 5 displays the output voltage of the sensing circuit, $V_{\rm out}$, versus $(V_{DD} - |V_{\rm tpo}|)$. This figure is obtained from SPICE simulations by sweeping the threshold voltage of the industrial STMicroelectronics 65 nm CMOS technology transistor model and using $V_{DD} = 1.0$ V and $r \approx 0.54$. Good agreements between the estimated threshold voltage values and their actual values, prove that the threshold voltage sensing circuit is effective, when used in nanometer technologies. The maximum error between the estimated threshold voltage values and their corresponding actual values is 5.4%, and the average error is 3.2%.

B. Amplifier Circuit

In the proposed ABB circuit in Fig. 3, two amplifiers with different gains and a large output voltage swing, $(V_{B+} - V_{B-})$, are required. Therefore, the two-stage configuration amplifier circuit, shown in Fig. 6, is utilized. The advantage of this configuration is that it isolates the gain and the output voltage swing requirements. The first stage is configured in a differential pair topology to provide the high gain requirements. Typically, the second stage is configured as a common source stage to allow

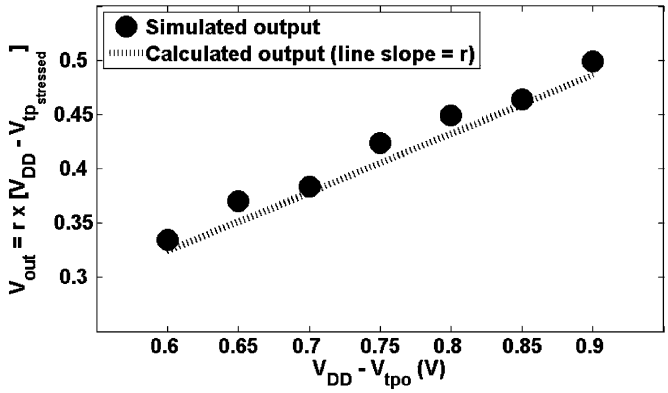

Fig. 5. The output of the pMOS threshold voltage sensing circuit shown in Fig. 4.

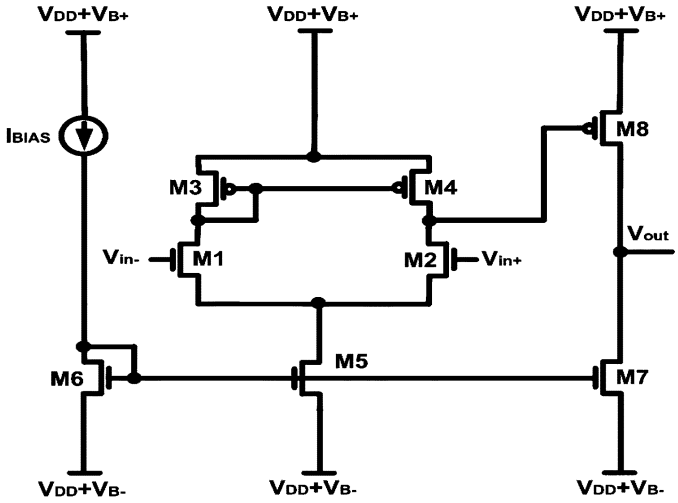

Fig. 6. The two-stage amplifier circuit.

maximum output voltage swings [28]. Long channel transistor operation is assumed by making all the amplifier transistors lengths equal 130 nm, and therefore, all transistors are assumed to be in the pinch-off saturation region and the following transistors pairs, (M1 and M2), (M3 and M4), and (M6 and M7), are designed to be matched.

According to [29], the mismatch between these transistors threshold voltages is inversely proportional to the square root of the channel area (WL). Thus, by designing all the amplifier and squaring circuit transistors widths larger than 195 nm (the minimum width for STMicroelectronics 65 nm transistor is 120 nm) and lengths of 130 nm (the minimum length for STMicroelectronics 65 nm transistor is 60 nm), this mismatch effect is reduced.

Correspondingly, the amplifier gain, K, is written as

$$K = \underbrace{\frac{g_{m1}}{g_{d2} + g_{d4}}} \times \underbrace{\frac{g_{m8}}{g_{d7} + g_{d8}}} \tag{9}$$

where the first term represents the differential pair gain, the second term represents the second stage gain, g_m is the transistor transconductance, and g_d is the transistor drain-to-source output conductance. g_m and g_d are designed to achieve the required gain, which is achieved by the first stage, and the output voltage swing, which is achieved by the second stage, in each amplifier. It should be noted that the amplifier shown in Fig. 6 is

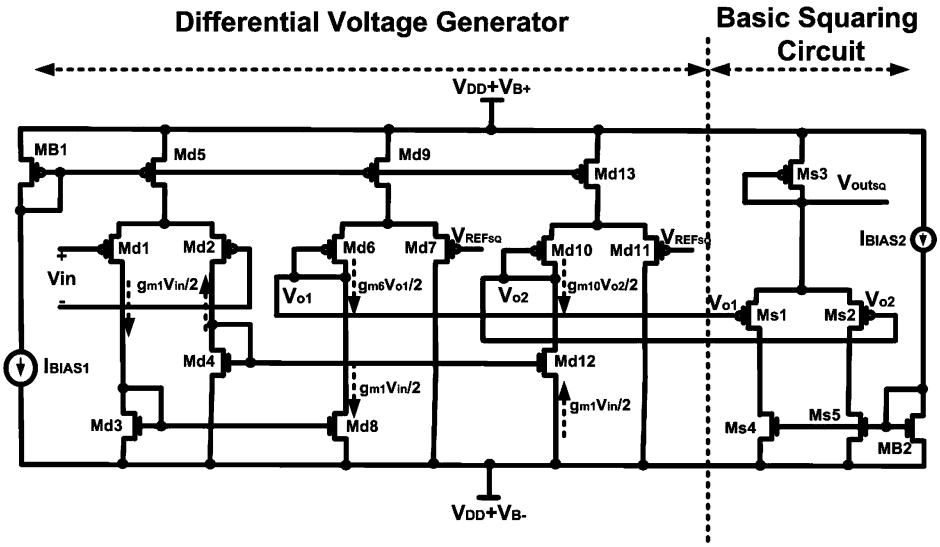

Fig. 7. The squaring circuit which consists of the differential voltage generator and the basic squaring circuit.

a noninverting amplifier. However, this amplifier is configured as an inverting amplifier by changing the input terminals (i.e., $V_{\text{in}+}$ and $V_{\text{in}-}$ become the inputs to transistors M1 and M2, respectively).

C. Squaring Circuit

One of the essential building blocks in the ABB circuit, shown in Fig. 3, is the squaring circuit. Several squaring circuits are reported in the literature [30], [31]. Fig. 7 depicts the squaring circuit used in the ABB circuit. The proposed squaring circuit consists of a differential voltage generator circuit and a basic common source differential pair squaring circuit. The differential voltage generator circuit is utilized to adjust the squaring circuit output voltage dc-offset and the squaring circuit gain. Assuming long channel transistor operation, all transistors are operating in the pinch-off saturation region, and the transistors pairs, (Md1 and Md2), (Md6, Md7, Md10, and Md11), (Md5, Md9, and Md13), (Md3 and Md8), and (Md4 and Md12), are matched. The small signal current flowing through Md1 is $g_{m1}V_{\text{in}}/2$ which is equal to the small signal current flowing through Md8 which is $g_{m6}V_{o1}/2$ due to the current mirror action between these transistors. Therefore, $V_{o1} = (g_{m1}/g_{m6})V_{\text{in}}$. Similarly, due to the current mirror action between transistors Md4 and Md12, the voltage V_{o2} is $-(g_{m1}/g_{m10})V_{\text{in}}$. Since transistors Md6, Md7, Md10, and Md11 are matched, the two output voltages, V_{o1} and V_{o2}, are given by

$$V_{o1} = -V_{o2} = \left(\frac{g_{m1}}{g_{m6}}\right) V_{\text{in}}. \tag{10}$$

These two output voltages, V_{o1} and V_{o2}, have an equal common mode voltage, $V_{\text{REF}_{\text{SQ}}}$. When these two output voltages are applied to the basic squaring circuit, the resultant output voltage, $V_{\text{out}_{\text{SQ}}}$, is given by [31]

$$V_{\text{out}_{\text{SQ}}} = V_{DD} + \frac{(V_{B+} - |V_{\text{tp}}|)^2 - (V_{\text{REF}_{\text{SQ}}} + |V_{\text{tp}}|)^2}{2(V_{B+} - V_{\text{REF}_{\text{SQ}}} - 2|V_{\text{tp}}|)} + \frac{(\frac{g_{m1}}{g_{m6}})^2 \times V_{\text{in}}^2}{2(V_{B+} - V_{\text{REF}_{\text{SQ}}} - 2|V_{\text{tp}}|)} \tag{11}$$

where the transistors pairs, (Ms1 and Ms2) and (Ms4 and Ms5) are matched. It is evident that the squaring circuit output voltage dc-offset can be adjusted through $V_{\text{REF}_{\text{SQ}}}$, whereas the squaring circuit gain can be adjusted through the transconductance ratio, (g_{m1}/g_{m6}), and $V_{\text{REF}_{\text{SQ}}}$. Fig. 8 displays the simulation results for the squaring circuit in Fig. 7, where V_{in} is varied from -0.15 V to 0.15 V and the squaring circuit gain is 10.0.

D. The Effect of Process and Temperature Variations on the Proposed ABB Circuit

A 5000 point postlayout Monte Carlo analysis, including the mismatch between transistors is performed. An industrial hardware-calibrated 65 nm CMOS technology transistor statistical models is used to investigate the effect of process variations on the proposed sensing, amplifier, and squaring circuits. In [32], [33], it has been demonstrated that the utilization of statistical transistor models is capable of accounting for both D2D and WID variations. A very good fitting with the measured data is reported in [32], [33], not only for the mean and standard deviation values, but also for the correlation between nMOS and pMOS transistors data. These statistical models are available in the design kits provided by STMicroelectronics. The process variations (D2D and WID variations) are included in the transistor design kit and declared by STMicroelectronics to be silicon verified. In this design kit, several process parameters are treated as variants such as the threshold voltage, mobility, drain-to-source resistance, Drain-induced-barrier-lowering (DIBL) coefficient, all junction capacitances, and doping concentration. For example, the threshold voltage is varied within the $\pm 3\sigma$ design space with standard deviation to mean ratio, $(\sigma/\mu)_{Vt} \approx 12\%$. Also, in this design kit, the WID variations (mismatch effect) are modeled as inversely proportional to the transistor area (WL) [29]. These statistical models are used in all the following Monte Carlo simulations.

Postlayout simulation results reveal that the maximum ratio between the standard deviation of the sensing, amplifier, and squaring circuits parameters (i.e., gain, output voltage swing,

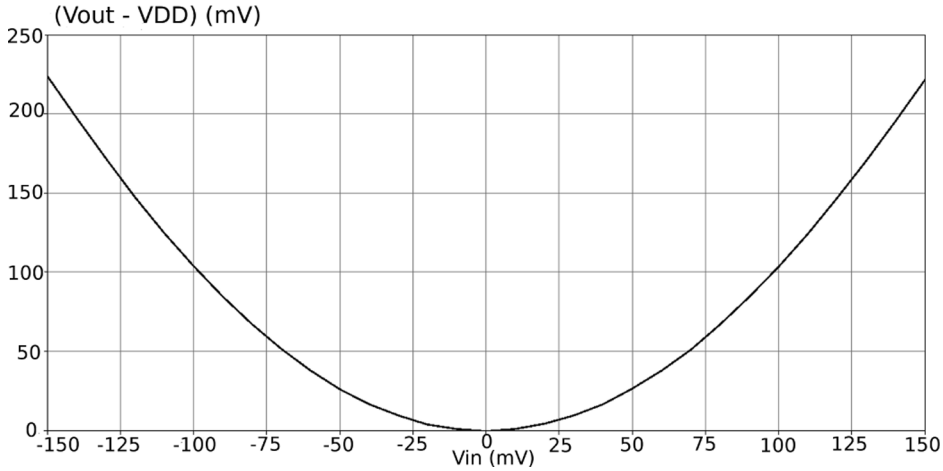

Fig. 8. The simulated squaring circuit output with $V_{\rm in}$ is varied from -0.15 V to 0.15 V and the gain is 10.0.

and dc offset) to their mean values is less than 1.1%, 0.6%, and 0.9%, respectively. Therefore, the newly developed ABB circuit is insensitive to process variations. In addition, the same sensing, amplifier, and squaring circuits are found to be insensitive to the temperature variations over the -30 °C to 125 °C range. The maximum change in the sensing, amplifier, and squaring circuits parameters, relative to their nominal values, is less than 1.9%, 0.8%, and 0.7%, respectively, over the specified temperature range. According to these results, the proposed ABB circuit is insensitive to process and temperature variations.

IV. Simulation Results and Discussions

In the following simulation results, the layout of a 512 6T low-V_t SRAM cells column is utilized with $V_{DD} = 1$ V and an operating frequency of 1 GHz, referring to an industrial hardware-calibrated STMicroelectronics 65 nm CMOS transistor model. This model card includes the process variations and the NBTI stress effects which are declared by STMicroelectronics to be Silicon verified. Low-V_t SRAM design is selected in this paper because it is more sensitive to NBTI as reported recently in [11]. The reliability analysis is performed by using Cadence RelXpert, Virtuoso Spectre, and Virtuoso UltraSim tools. The pMOS transistor parameters such as $|V_{\rm tpo}|$, ϕ_F, and γ are determined from the transistor model card at a temperature $T = 125$ °C and equal 0.204 V, 0.439 V, and 0.18, respectively. Accordingly, The ABB circuit parameters K_{1p}, K_{2p}, and K_{3p} equal -1.8, 10.0, and -10.6, respectively. All the above parameters are calculated at $T = 125$ °C and $r = 0.54$. It should be mentioned that the technology parameter ϕ_F is linearly proportional to the temperature T in °K, accordingly, the ABB design is performed at the worst case temperature $T = 125$ °C.

The junction leakage current and the breakdown considerations determine the RBB voltage bound (V_{B+}), while the FBB voltage (V_{B-}) is limited by the subthreshold leakage current and the forward biasing of the drain-bulk junction. According to [34], [35], the upper limit of the FBB voltage for latch-up free operation, in 65 nm CMOS technology with V_{DD} ranges from 0.9 V to 1.2 V, is 0.6 V. Also, SPICE simulations are conducted by sweeping the FBB voltage for the pMOS transistor and show that the upper limit of the FBB voltage to prevent latch-up triggering for the pMOS transistor is 0.59 V. Therefore, the maximum FBB voltage used in this ABB is set to 0.5 V to ensure latch-up free operation in case of fluctuations of the FBB voltage around 0.5 V. Moreover, the RBB voltage is selected to be 0.5 V as well resulting in a junction leakage current less than 1.0 nA for each SRAM cell. Accordingly, the FBB and the RBB maximum voltages (i.e., $V_{DD}+V_{B+}$ and $V_{DD}+V_{B-}$) are set to 1 V ± 0.5 V [13].

The effectiveness of the proposed ABB circuit in mitigating the NBTI stress impact and the process variations is examined by performing postlayout simulations for the SRAM column without the adoption of the ABB circuit. Then, the same simulations are repeated while the ABB circuit is adopted and the results are compared to the case when the ABB circuit is not utilized. In these simulations, the temperature used is $T = 125$ °C with input signal probability $p_L = p_R = 0.5$ with the aging time changes from 0 to 10 years.

A. SNM

Fig. 9(a) shows the HOLD SNM degradation percentage versus aging time for the no body bias (NBB) case and the ABB case. It is evident that the ABB circuit not only keep the HOLD SNM constant but also improves it with aging up to 5 years aging time. This is because the ABB sensing circuit is represented by a dc stressed PMOS transistor whereas the SRAM PMOS transistors exhibit 50% stress probability because $p_L = p_R = 0.5$. Accordingly, the ABB circuit provides more FBB than required which improves the HOLD SNM. After 5 years aging, the ABB case exhibits some HOLD SNM degradation because the ABB is limited to a body bias voltage of 0.5 V. Accordingly, the NBTI $|V_{\rm tp}|$ increase is larger than the $|V_{\rm tp}|$ reduction amount supplied by the ABB when the body bias voltage becomes 0.5 V. However, this HOLD SNM degradation percentage is 1% at 10 years aging compared to 4.3% for the NBB case.

Similarly, the READ SNM degradation percentage, displayed in Fig. 9(b), exhibits improvement for the ABB case up to 5 years aging time. At 10 years aging time, the ABB case READ SNM degradation percentage is 4.3X less compared to that of the NBB case. Also, it should be noted that the READ SNM is more sensitive to NBTI than the HOLD SNM. For example, the READ SNM degradation percentage at 10 years aging time is 10.9% whereas the HOLD SNM degradation percentage is 4.3% at the same aging time.

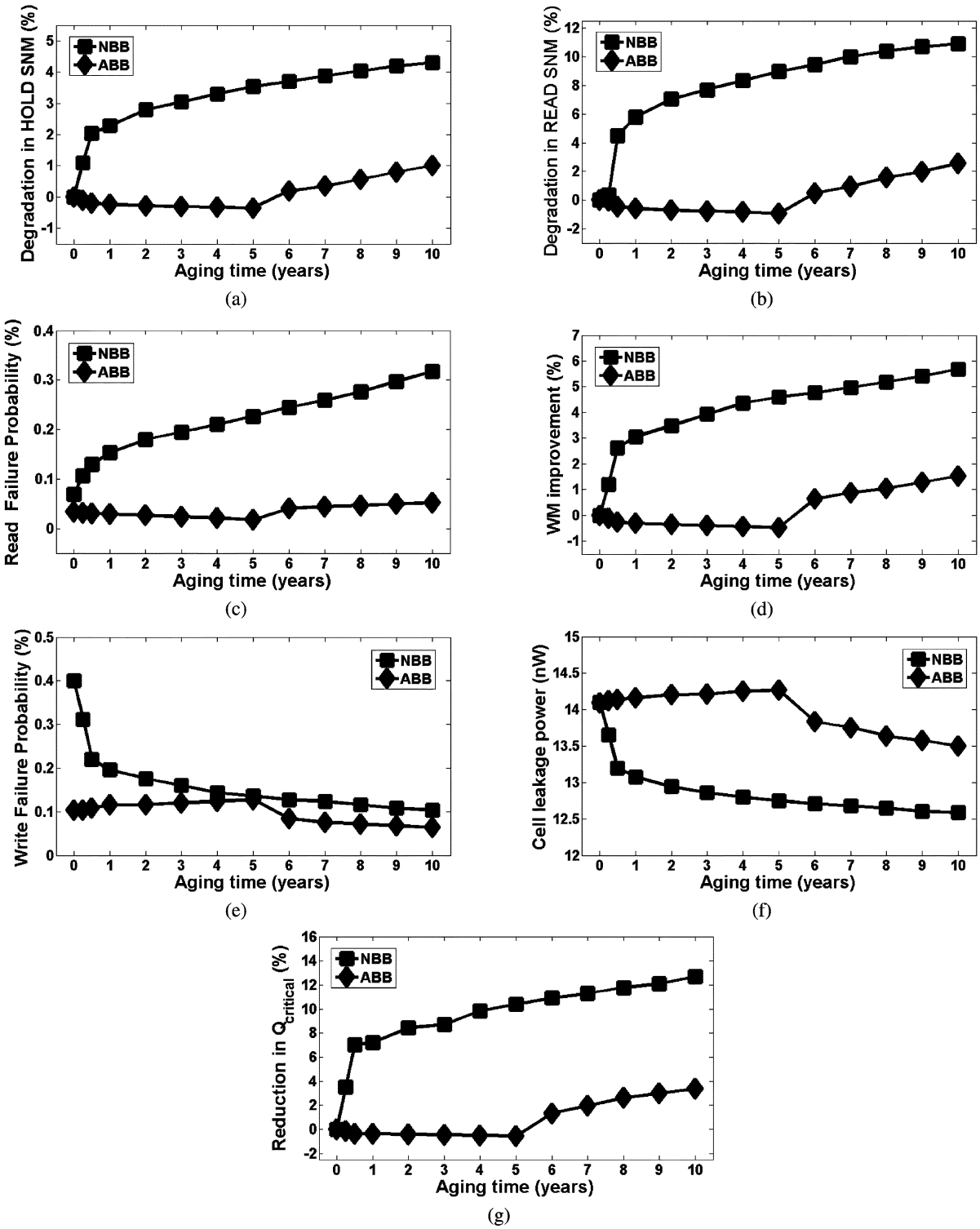

Fig. 9. Postlayout simulation results for the NBB case and the ABB case versus aging time at $T = 125$ °C and $p_L = p_R = 0.5$ considering: (a) HOLD SNM degradation percentage; (b) READ SNM degradation percentage; (c) read failure probability; (d) WM improvement; (e) write failure probability; (f) leakage power; and (g) the 1-to-0 flip critical charge reduction.

B. Read Failure Probability

The ABB circuit adoption helps in mitigating both the NBTI and the process variations impact on the PMOS transistors. Accordingly, at zero aging time, the ABB adoption reduces the read failure probability from 0.07% to 0.03% (i.e., the number of SRAM cells that fail in the read operation is reduced from 734 cells to 356 cells in a 1 Mb SRAM block) as portrayed in Fig. 9(c). The ABB circuit improves the read failure probability up to 5 years aging time. At 10 years aging time, the ABB case shows a reduction in the read failure probability by a factor of 6.4X compared to that of the NBB case. The number of Monte Carlo points in these simulations is 10 000.

C. WM and Write Failure Probability

The WM and the write failure probability are improved with NBTI which is shown in Fig. 9(d) and (e). The WM is increased at an aging time of 10 years by 5.7% and the write failure probability is reduced from 0.4% at zero aging time to 0.1%. Unfortunately, the ABB circuit adoption results in WM degradation (due to the $|V_{\rm tp}|$ compensation) in the first 5 years. From 5 years to 10 years aging time, the ABB circuit allows some increase of the WM but still less than that of the NBB case. For example, at 10 years aging time, the WM is increased by 1.6% for the ABB case whereas it is increased by 5.7% for the NBB case.

In the mean time, the write failure probability is reduced by the ABB circuit as well due to the process variations compensation effect. The write failure probability is reduced at zero aging time due to the ABB adoption by a factor of 3.9X and at 10 years aging time by a factor of 1.6X as shown in Fig. 9(e). In addition, the ABB adoption results in lower write failure probability over all the aging time period.

D. Leakage

Fig. 9(f) displays the SRAM cell leakage power for both the NBB and the ABB cases. As reported in [12], the leakage power decreases with NBTI aging and this reduction is maximized when $p_L = p_R = 0.5$. Correspondingly, the NBTI effect results in reducing the leakage current by 10.8% over 10 years aging time. The ABB increases the leakage power in the first 5 years. Following that, the ABB reduces the leakage power for aging time larger than 5 years. However, this leakage power reduction is still less than that in the NBB case.

E. $q_{\rm critical}$

The critical charge, $Q_{\rm critical}$, is calculated only for the 1-to-0 flip which is affected by the NBTI and is much smaller than the 0-to-1 flip as mentioned in Section II-E. $Q_{\rm critical}$ is calculated by applying an exponential current pulse at node V_L given by [10]

$$i_{\rm injected}(t) \approx \frac{Q}{\tau} \times \exp\left(\frac{-t}{\tau}\right) \tag{12}$$

where Q is the total charge deposited by this current pulse at the struck node and τ is the falling time constant. The simulations are performed with $\tau = 200$ ps and Q is varied in SPICE transient simulations to find the value of Q that results in cell flipping. Then, $Q_{\rm critical}$ is calculated by using the following [10]:

$$Q_{\rm critical} = Q\left(1 - \exp\left(\frac{-t_f}{\tau}\right)\right) \tag{13}$$

where t_f is the cell flipping time. Fig. 9(g) portrays that $Q_{\rm critical}$ decreases with NBTI aging time and reaches up to 12.7% reduction at an aging time of 10 years. The ABB adoption increases $Q_{\rm critical}$ in the first 5 years and then $Q_{\rm critical}$ decreases. At an aging time of 10 years, the ABB reduces $Q_{\rm critical}$ degradation percentage by a factor of 3.8X as displayed in Fig. 9(g).

Moreover, it should be noted that the NBTI impact grows faster for the first year aging time. It has been shown by simulations that the $|V_{\rm tp}|$ increase due to NBTI is 31.5 mV at 1 year aging time whereas it becomes 37.4 mV at 2 years aging time. At 5 years aging time, the $|V_{\rm tp}|$ increase becomes 47 mV which is close to the maximum ABB compensation. At 10 years aging time, the $|V_{\rm tp}|$ increase becomes 56 mV.

TABLE I
POSTLAYOUT SIMULATION RESULTS FOR $T = 0$ °C, $T = 60$ °C, AND $T = 125$ °C CONSIDERING THE NBB AND THE ABB CASES AT AN AGING TIME OF 10 YEARS WITH $p_L = p_R = 0.5$

T =		125^oC	60^oC	0^oC
NBB	HOLD SNM degradation (%)	4.3	3.9	3.8
	READ SNM degradation (%)	10.9	8.7	6.7
	READ failure probability (%)	0.32	0.02	0
	WM improvement (%)	5.7	5.3	5.0
	Write failure probability (%)	0.1	0.08	0.02
	Leakage power (nW)	12.59	1.85	0.11
	$Q_{critical}$ reduction (%)	12.7	8.1	7.6
ABB	HOLD SNM degradation (%)	1.0	0.96	0.94
	READ SNM degradation (%)	2.6	2.2	1.4
	READ failure probability (%)	0.05	0	0
	WM improvement (%)	1.5	1.4	1.4
	Write failure probability (%)	0.06	0.05	0
	Leakage power (nW)	13.5	1.95	0.15
	$Q_{critical}$ reduction (%)	3.4	1.4	1.3

V. FACTORS AFFECTING THE PROPOSED ABB PERFORMANCE

A. The Effect of Temperature on the ABB Performance

The ABB design is performed at a temperature $T = 125$ °C which is the worst case operating condition for the SRAM cells. When the operating temperature decreases, $|V_{\rm tp}|$ increases by $(\Delta|V_{\rm tp}|_T + \Delta|V_{\rm tp}|_{\rm NBTI})$, where $\Delta|V_{\rm tp}|_T$ is the $|V_{\rm tp}|$ increase due to temperature decrease and $\Delta|V_{\rm tp}|_{\rm NBTI}$ is the $|V_{\rm tp}|$ increase due to NBTI. Decreasing the operating temperature results in increasing $\Delta|V_{\rm tp}|_T$ [21] and decreasing $\Delta|V_{\rm tp}|_{\rm NBTI}$ (because $K_{\rm dc}$ is a function of temperature) [11]. This $|V_{\rm tp}|$ change is sensed by the ABB sensing circuit and the corresponding body bias voltage is generated. Therefore, the ABB circuit compensates also for temperature variations. Table I shows the effect of the temperature on the ABB performance in mitigating NBTI and process variations impacts. It is evident from this table that the ABB circuit is working effectively as the temperature varies.

B. The Effect of Unequal Gate Input Probabilities on the ABB Performance

All the above simulation results are performed by using equal gate input probabilities (i.e., $p_L = p_R = 0.5$). The effect of unequal gate input probabilities on the proposed ABB performance is tabulated in Table II.

The gate input probabilities $p_L = 0$ and $p_R = 1$ means that $V_L =$ "0" and $V_R =$ "1" over the 10 years aging time. This results in maximum NBTI degradation in the right pMOS transistor, M_{pR}, and no degradation in M_{pL}. Accordingly, the

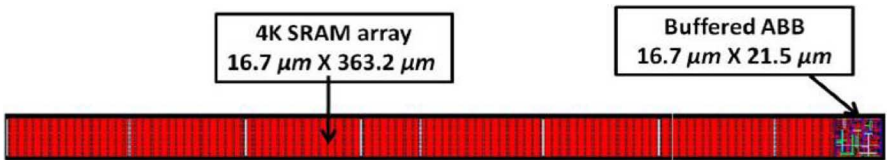

Fig. 10. Layout of the proposed buffered ABB adopted to a 4K SRAM array (8 columns, each column consists of 512 SRAM cells.

TABLE II
POSTLAYOUT SIMULATION RESULTS FOR DIFFERENT GATE INPUT PROBABILITIES CONSIDERING THE NBB AND THE ABB CASES AT AN AGING TIME OF 10 YEARS WITH $T = 125$ °C

p_L/p_R		0.5/0.5	0/1 or 1/0	0.25/0.75 or 0.75/0.25
NBB	HOLD SNM degradation (%)	4.3	7.3	5.3
	READ SNM degradation (%)	10.9	14.1	12.2
	READ failure probability (%)	0.32	0.4	0.33
	WM improvement (%)	5.7	7.6	4.6
	Write failure probability (%)	0.1	0.06	0.1
	Leakage power (nW)	12.59	14.1	12.8
	$Q_{critical}$ reduction (%)	12.7	15.5	14
ABB	HOLD SNM degradation (%)	1.0	3.5	2.3
	READ SNM degradation (%)	2.6	5.8	4.5
	READ failure probability (%)	0.05	0.09	0.07
	WM improvement (%)	1.5	3.1	0.22
	Write failure probability (%)	0.06	0.04	0.08
	Leakage power (nW)	13.5	18.3	14.1
	$Q_{critical}$ reduction (%)	3.4	9.9	5.6

highest SNM degradation, the highest read failure probability, and highest Q_{critical} reduction occur in this situation for the NBB and the ABB cases. On the other side, the highest WM improvement and the lowest write failure probability occur in this case. Since the leakage current is measured through the OFF transistor (i.e., M_{pL} in this case) which is not impacted by NBTI, the leakage power equals the same value at zero aging time (i.e., leakage $\text{power} = 14.1$ nW) with no leakage reduction. The leakage current increases by 30% for the ABB case because the ABB circuit applies the maximum body bias voltage for both pMOS transistors although the transistor M_{pL}, through which the leakage current is calculated in this case, is not impacted by NBTI. This forward body bias adoption for M_{pL} results in increasing the leakage current of the cell.

The gate input probabilities $p_L = 0.25$ and $p_R = 0.75$ results in unequal degradation in the two pMOS transistors (i.e., M_{pL} is less degraded than M_{pR}). Accordingly, the SRAM parameters are dependent on the SRAM cell data status at 10 years aging time. Therefore, the SRAM parameters are calculated for the SRAM status when $V_L =$ "0" and $V_R =$ "1" and also when $V_L =$ "1" and $V_R =$ "0". Following that, the SNM, WM, and Q_{critical} is calculated as the minimum of these two statuses whereas the leakage power is calculated as the maximum of these two statuses. The failure probabilities are calculated by using the following (12) where the failure probability is denoted by FP:

$$FP = FP|_{V_L=\text{"0"} \text{ and } V_R=\text{"1"}} \times p_R + FP|_{V_L=\text{"1"} \text{ and } V_R=\text{"0"}} \times p_L. \quad (14)$$

It is evident from Table II that the ABB circuit reduces the NBTI and process variations impacts effectively for the unequal input gate probabilities. In addition, the cases ($p_L = 1$ and $p_R = 0$) and ($p_L = 0.75$ and $p_R = 0.25$) provide similar results to the cases ($p_L = 0$ and $p_R = 1$) and ($p_L = 0.25$ and $p_R = 0.75$), respectively, due to the SRAM similarity.

C. The Adoption of the Proposed ABB to Larger SRAM Arrays

In all the above simulation results, the proposed ABB circuit is adopted to a 512 SRAM cells column. The same simulation results are obtained when the proposed ABB circuit is adopted to a 1024 SRAM cells array (i.e., 2 columns, each column consists of 512 SRAM cells). However, the proposed ABB circuit fails in providing the correct body bias voltage when adopted to 3 SRAM columns array (i.e., 1536 SRAM cells).

Accordingly, the ABB circuit output must be buffered to ensure low output impedance and to be able to drive a larger number of SRAM cells. The voltage buffer is implemented by an operational amplifier as a unity-gain amplifier. The buffered ABB output is able to drive up to 11 SRAM columns, each column consists of 512 SRAM cells.

Correspondingly, several buffers are utilized to supply the output of the proposed ABB circuit to cover the whole SRAM array. For example, each buffer output is applied to a 4K SRAM array (i.e., 8 SRAM columns, each column consists of 512 SRAM cells). Adopting only one ABB circuit with multiple buffers (Global ABB circuit) is unable to compensate for the systematic WID variations. In order to compensate for these WID variations, one buffered ABB circuit should be adopted to each 4K SRAM array (Local ABB circuits) as shown in Fig. 10.

Postlayout simulations are conducted again for the 4K SRAM array with a buffered ABB circuit and the results are approximately the same as the results obtained when the unbuffered ABB circuit is adopted to a 512 SRAM cells column (the difference between these simulation results is less than 0.5%).

Fig. 10 displays the layout of a 4K SRAM array with the buffered ABB circuit. The layout area of the 4K SRAM is 6065 μm^2 whereas the buffered ABB layout area is 359 μm^2. Thus, the SRAM area is increased by 5.9% with the adoption of local ABB circuits with a granularity level of 4K SRAM array. Increasing the granularity level (i.e., 16K SRAM array) by using one ABB circuit with 4 voltage buffers, results in reducing the

TABLE III
COMPARISON BETWEEN THE PROPOSED ABB AND THE ABB IN [20] AT AN AGING TIME OF 10 YEARS WITH $T = 125$ °C AND $p_L = p_R = 0.5$

	NBB	Proposed ABB	ABB in [20]
HOLD SNM degradation (%)	4.3	1.0	3.5
READ SNM degradation (%)	10.9	2.6	9.0
READ failure probability (%)	0.32	0.05	0.28
WM improvement (%)	5.7	1.5	4.6
Write failure probability (%)	0.1	0.06	0.14
Leakage power (nW)	12.59	13.5	12.8
$Q_{critical}$ reduction (%)	12.7	3.4	10.4

area overhead. Therefore, there is a trade-off between the granularity level used and the associated area overhead. Also, the ability of the ABB circuit in compensating for WID systematic variations is reduced by increasing the granularity level.

VI. COMPARISON WITH PREVIOUS NBTI COMPENSATION CIRCUITS

Holding a direct comparison with previous NBTI compensation circuits is not viable because most of the these circuits are NBTI degradation monitoring circuits only [17]–[19]. These monitoring circuits output can be fed to an ABB circuit to compensate for the NBTI impact. These monitoring circuits utilize PLL technique to determine the pMOS transistor deviation digitally and require a digital to analog converter (DAC) to convert this digital difference to the appropriate body bias voltage, which is obtained by using a digital control module. These requirements impose large area overhead which limits the applicability of these circuits compared to the proposed ABB circuit.

The ABB circuit introduced in [20] for NBTI compensation utilizes on-chip analog circuits. In [20], the difference between the current flowing through a stressed pMOS transistor and the current flowing through an nMOS transistor is converted into an output voltage. This output voltage is used as a body bias for the pMOS transistors in the actual circuit. The nonlinear relationships between this sensing circuit output voltage and the threshold voltage deviation and also between the body bias voltage and the threshold voltage limit the ability of this circuit to compensate for NBTI.

The performance of the ABB in [20] is compared to that of the proposed ABB in Table III for an aging time of 10 years with $T = 125$ °C and $p_L = p_R = 0.5$ by conducting postlayout simulations. The transistors sizes given in [20] are utilized for the industrial hardware-calibrated STMicroelectronics 65 nm CMOS technology. It is evident from Table III that the performance of the ABB in [20] in compensating for NBTI is lower than that in the proposed ABB. Moreover, the write failure probability increases with the adoption of the ABB in [20] because it does not compensate for process variations since both the sensed pMOS current and the nMOS current exhibit the same systematic process variations impact.

Furthermore, the output voltage of the ABB in [20] provides a body bias voltage of 0.8 V (i.e., a FBB voltage of 0.2 V with respect to $V_{DD} = 1$ V) whereas the proposed ABB output voltage is 0.5 V (i.e., a FBB voltage of 0.5 V with respect to $V_{DD} = 1$ V) at an aging time of 10 years. This 0.8 V body bias voltage is not capable of compensating for the NBTI degradation at 10 years aging time effectively as shown in Table III because more FBB voltage is required to compensate for the large $|V_{\rm tp}|$ shift due to NBTI at 10 years aging time. In addition, the leakage power of the SRAM cell is larger when the proposed ABB is adopted than that in the case when the ABB in (20) is adopted by a factor of 1.1X. This leakage power increase is because the proposed ABB supplies more FBB than that in the ABB in [20] which results in increasing the leakage power.

Also, the layout area of the unbuffered ABB is 263.7 μm^2 which is larger than that in [20] by a factor of 1.2X. However, the proposed ABB performance is much better than that of the ABB in [20]. In addition, the ABB in [20] requires the utilization of two power supplies of values 1 V and 2 V. The maximum allowable supply voltage for the industrial hardware-calibrated STMicroelectronics 65 nm CMOS technology is 1.56 V which makes the adoption of the ABB in [20] very difficult in commercial CMOS technologies. It should be noted that the simulations in [20] are conducted by using predictive models which lack the hardware-calibrated NBTI and process variations model cards, used in this comparison.

VII. CONCLUSION

The proposed ABB circuit has been shown to reduce the impacts of the NBTI aging and process variations on the SRAM cells. The ABB circuit consists of a threshold voltage sensing circuit and an analog controller that generates the required body bias voltage to compensate for NBTI aging and process variations. Postlayout simulation results, referring to an industrial hardware-calibrated STMicroelectronics 65 nm CMOS technology transistor model, show that the proposed ABB compensates effectively for NBTI and process variations. For example, the proposed ABB reduces the read failure probability from 0.32% to 0.05% and the SNM degradation from 10.9% to 2.6% at 10 years aging time. In addition, the proposed ABB enhances the soft errors immunity of the SRAM cell by reducing the critical charge degradation from 12.7% to 3.4% at 10 years aging time. The main advantage of the proposed ABB is its lower area overhead compared to the previous state-of-the-art ABB techniques. Typically, the area overhead of the proposed ABB is less than that in [17]–[19]. Although the proposed ABB exhibits a larger layout area than that in [20] by a factor of 1.2X, the proposed ABB performance is much better than that in [20] as proved in this paper.

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