A Bias-Dependent Model for the Impact of Process Variations on the SRAM Soft Error Immunity

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***Abstract*—Nanometer SRAM cells are more susceptible to the particle strike soft errors and the increased statistical process variations, in advanced nanometer CMOS technologies. In this paper, an analytical model for the critical charge variations accounting for both die-to-die (D2D) and within-die (WID) variations, over a wide range of bias conditions, is proposed. The derived model is verified and compared to Monte Carlo simulations by using industrial hardware-calibrated 65-nm CMOS technology. This paper shows the impact of the coupling capacitor, one of the most common soft error mitigation techniques, on the critical charge variability. It demonstrates that the adoption of the coupling capacitor reduces the critical charge variability. The derived analytical model accounts for the impact of the supply voltage, from 0.1 to 1.2 V, on the critical charge and its variability.**

***Index Terms*—Deep sub-micrometer, process variations, reliability, soft errors, static random access memory (SRAM).**

I. Introduction

Reliability is one of the major design challenges for sub-micrometer CMOS technology. Shrinking geometries, lower power supply, higher clock frequencies, and higher density circuits all have a great impact on reliability [1]–[4]. As CMOS technology further scales, soft errors become one of the major reliability concerns. Soft errors are caused by alpha particles and high energy neutrons. These particles generate charges which disturb the node voltage and lead to soft errors [2]. In memory elements such as static random access memory (SRAM) and flip-flops, if the charge collected by the particle strike at the storage node, is more than a minimum value, the node is flipped and a soft error occurs. This minimum value is called a critical charge ($Q_{\rm critical}$), which is used as a measure of the memory element immunity to soft errors [2], [4]. This critical charge exhibits an exponential relationship with the soft error rate (SER) [2], and consequently, this critical charge should be designed high enough, to limit the SER. SRAM cells are more vulnerable to soft errors due to their lower node capacitance.

Process variations are expected to worsen in future technologies, due to difficulties with printing nanometer scale geometries in standard lithography. Therefore, these variations are considered another main challenge in CMOS technology scaling [5], [6]. They are classified as die-to-die (D2D) variations and within-die (WID) variations. In D2D variations, all the devices on the same die are assumed to have the same parameters values. However, the devices on the same die are assumed to behave differently in WID variations [5]. Due to the existence of process variations, the critical charge has variations around its nominal value which results in SRAM failure to meet robustness constraints.

Recently, researchers have attempted to calculate the critical charge nominal value as well as addressing the impact of process variations on the critical charge in memory elements such as SRAM cells and flip-flops. However, most of this research is conducted by using Monte Carlo analysis tools [1], which are time consuming and not scalable with technology. From a design perspective, few articles have been published on modeling the critical charge and its variations [7], [8]. However, all these models consider only the super-threshold SRAM cells with only D2D variations taken into account.

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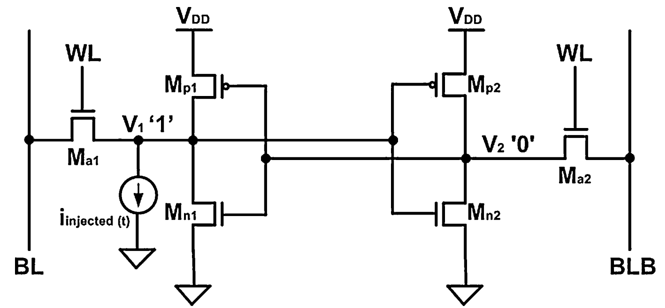

Fig. 1. SRAM cell with the particle strike current pulse ($i_{\rm injected}(t)$).

The tradeoff between performance and power consumption makes the super-threshold SRAM design essential for high performance with the drawback of large power consumption. On the other hand, it makes the sub-threshold SRAM design, while energy efficient, has the drawback of performance degradation. To retain the excellent energy efficiency while reducing performance loss, near-threshold SRAM design is proposed [9]. Accordingly, an analytical critical charge variability model, accounting for all the SRAM cell operating regions and considering D2D and WID variations, is of paramount importance, to predict the SER variability over wide range of bias conditions.

In this paper, an analytical model of the critical charge variability, accounting for both D2D and WID variations, is proposed, for a wide range of bias conditions including super-threshold, near-threshold, and sub-threshold SRAM operation. The derived model is simple, scalable in terms of technology scaling. Moreover, it shows explicit dependence on design parameters such as node capacitance, transistors sizing, transistor parameters, and supply voltage. The results are verified by using SPICE transient and Monte Carlo simulations and an industrial 65-nm CMOS technology transistor model.

The rest of this paper is organized as follows. In Section II, the proposed critical charge model derivations are explained. The critical charge variability model is introduced in Section III. The proposed model is compared with SPICE transient and Monte Carlo simulations in Section IV. Finally, some conclusions are drawn in Section V.

II. Critical Charge Model Derivations

Fig. 1 shows a typical six transistor (6T) SRAM cell. It consists of two cross-coupled inverters, that store two complementary logic values ("1" and "0") at their output nodes. These output nodes are denoted by V_1 and V_2. The SRAM cell has its highest susceptibility to particle strikes in the standby mode, in which, the storage nodes are disconnected from the highly capacitive bitlines. Thus, the access transistors M_{a1} and M_{a2} are excluded from the analysis. Assume that node V_1 stores logic "1" and accordingly node V_2 stores logic "0."

The critical charge are calculated for a 1-to-0 flip at node V_1 or a 0-to-1 flip at node V_2. In the following analysis, it is assumed that node V_1 is more susceptible to soft errors while the other case can be derived in a similar tendency. Therefore, in order to determine the critical charge model at node V_1, the particle strike is modeled by an exponential current pulse, connected to node V_1, given by [8]

$$i_{\rm injected}(t) \approx \frac{Q}{\tau} \times \exp(-t/\tau) \quad (1)$$

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where Q is the total charge deposited by this current pulse at the struck node, and τ is the falling time [2]. The nodal current equation at node V_1 is written as

$$C_1 \frac{dV_1}{dt} = [i_{p1} - i_{n1}] - i_{\text{injected}}(t) \tag{2}$$

where C_1 is node V_1 capacitance; i_{p1} is the pMOS transistor, M_{p1}, restoring current, which tries to pull-up node V_1; i_{n1} is the nMOS transistor M_{n1} current; and $i_{\text{injected}}(t)$ is the injected current pulse given in (1).

From (2), when the currents $[i_{p1} - i_{n1}]$ and $i_{\text{injected}}(t)$ are equal, node V_1 voltage attains a certain minimum value $V_{\min}$. The time at which $V_{\min}$ occurs is denoted by $t_{\min}$ and given by

$$t_{\min} = \tau \ln\left(\frac{Q}{\tau[i_{p1} - i_{n1}]}\right). \tag{3}$$

By solving the differential equation in (2) and using (3), The value of $V_{\min}$ is given by

$$V_{\min} = V_{\text{DD}} - \frac{1}{C_1}(Q - [i_{p1} - i_{n1}][t_{\min} + \tau]). \tag{4}$$

In this model, we assume that once node V_1 voltage hits its minimum value $V_{\min}$, the pMOS transistor M_{p1}, restoring current causes V_1 voltage to either recover to logic "1" and no flipping occurs, or flip to logic "0" and flipping occurs. This assumption is justified by noting that after the time $t_{\min}$, the injected current $i_{\text{injected}}(t)$ continues decaying exponentially according to (1). Therefore, the goal is to find the condition on the current component, $[i_{p1} - i_{n1}]$, that causes node V_1 to flip. This restoring current is controlled by its gate voltage V_2.

Due to the fact that the inverter switching voltage V_M is defined as the threshold between logic "1" and logic "0." If $V_{\min}$ is slightly below the switching voltage of the second inverter, V_{M2}, V_2 rises to logic "1" decreasing the current component $[i_{p1} - i_{n1}]$ and resulting in a soft error. For simplicity, V_M is assumed to be $V_{\text{DD}}/2$.

Consider the flipping case (i.e., $V_{\min} < V_{\text{DD}}/2$), node V_2 voltage stays around 0 V, for the time interval over which V_1 is approaching $V_{\min}$ (i.e., $t_{\min}$), and then starts to rise. Furthermore, V_1 is assumed to remain constant at $V_{\min}$, until V_2 rises and exceeds $V_{\text{DD}}/2$. The time at which V_2 hits $V_{\text{DD}}/2$ is denoted by t_f, which refers to the SRAM cell flipping time. These assumptions are validated by noticing that once V_2 hits $V_{\text{DD}}/2$, the positive feedback of the cell becomes strong enough to continue flipping the cell state. In addition, these assumptions are verified in the simulation results (see Section IV). Now, the value of Q, that just cause V_1 to flip, is obtained by equating $V_{\min}$ to $V_{\text{DD}}/2$ and given by

$$Q = C_A(V_{\text{DD}}/2) + [i_{p1} - i_{n1}][t_{\min} + \tau]. \tag{5}$$

By substituting (5) in (3), $t_{\min}$ is calculated by solving the following:

$$t_{\min} = \tau \ln(\gamma + t_{\min}/\tau), \quad \text{where } \gamma = 1 + \frac{C_A(V_{\text{DD}}/2)}{\tau[i_{p1} - i_{n1}]}. \tag{6}$$

Equation (6) is a nonlinear equation that is solved numerically by using the Lambert W function (also called the Omega function), $\Omega(x)$ [10]. $t_{\min}$ is expressed as

$$t_{\min} = \tau[-\gamma - \Omega_{-1}(-\exp(-\gamma))] \tag{7}$$

where $\Omega_{-1}(x)$ is defined for $(\exp(-1) \le x < 0)$ [10].

Now, the objective is to find the flipping time t_f. t_f is the sum of $t_{\min}$, and the time delay that V_2 takes to rise from 0 V to $V_{\text{DD}}/2$ (this time is denoted by t_{up}). This delay is driven by transistors M_{p2} and M_{n2}, where their gate voltage V_1 is constant at $V_{\text{DD}}/2$. By solving the nodal current equation at node V_2, the delay t_{up} is expressed as

$$t_{\text{up}} = \frac{C_2 V_{\text{DD}}/2}{[i_{p2} - i_{n2}]} \tag{8}$$

where C_2 is the capacitance of node V_2. Thus, the critical charge Q_{critical} is obtained as follows [7], [8]:

$$Q_{\text{critical}} = Q(1 - \exp(-t_f/\tau)). \tag{9}$$

In the above derivation, the currents i_{p1}, i_{n1}, i_{p2}, and i_{n2}, has a gate to source voltage $|V_{GS}|$, of $V_{\text{DD}}, 0, V_{\text{DD}}/2$, and $V_{\text{DD}}/2$, respectively. These currents have different dependence on $|V_{GS}|$ based on whether the transistors are operating in the super-threshold region (i.e., $|V_{GS}| \gg |V_t|$), the near-threshold region (i.e., $|V_{GS}| \approx |V_t|$) or the sub-threshold region (i.e., $|V_{GS}| \ll |V_t|$), where $|V_t|$ is the transistor threshold voltage. A unified physical current formula, that is used for all the transistor operating regions, is introduced in [11] and given by

$$i = K \frac{\left\{\ln\left[1 + \exp\left(\frac{|V_{GS}| - |V_t|}{2n}\right)\right]\right\}^2}{1 + \ln\left[1 + \exp\left(\frac{|V_{GS}| - |V_t|}{E_{\text{sat}} L}\right)\right]} \tag{10}$$

where n is the sub-threshold swing coefficient, E_{sat} is the velocity saturation electric field, L is the transistor channel length, and K is a fitting parameter that is extracted from simulations. Also, n and E_{sat} are obtained from the transistor model files.

III. Statistical Critical Charge Variation Model

Process variations affect device parameters, resulting in fluctuations in the critical charge. The primary sources of process variations, that affect the device parameters, are random dopant fluctuations (RDF), channel length variations, and line edge roughness (LER). All these process variation sources affect on the device threshold voltage, V_t. In this paper, the proposed model deals with the D2D and systematic variations by using corner based analysis. However, the random variations are treated by using the following statistical analysis.

From the equations derived in Section III-A, it is evident that the critical charge Q_{critical} is dependent on the threshold voltages of transistors M_{p1}, M_{p2}, M_{n1}, and M_{n2}, which are denoted by $V_{tp1}, V_{tp2}, V_{tn1}$, and V_{tn2}, respectively. A small change in these threshold voltages results in an incremental change in the critical charge that is calculated by using Taylor expansion around the nominal value. The standard deviation of the critical charge variations is calculated as follows:

$$\sigma_{Q_{\text{critical}}} = \left\{\left(\frac{\partial Q_{\text{critical}}}{\partial V_{tp1}}\right)^2 \sigma_{V_{tp1}}^2 + \left(\frac{\partial Q_{\text{critical}}}{\partial V_{tp2}}\right)^2 \sigma_{V_{tp2}}^2 + \left(\frac{\partial Q_{\text{critical}}}{\partial V_{tn1}}\right)^2 \sigma_{V_{tn1}}^2 + \left(\frac{\partial Q_{\text{critical}}}{\partial V_{tn2}}\right)^2 \sigma_{V_{tn2}}^2\right\}^{0.5} \tag{11}$$

where $\sigma_{Vtp1}, \sigma_{Vtp2}, \sigma_{Vtn1}$, and σ_{Vtn2} are the standard deviations of the threshold voltages $V_{tp1}, V_{tp2}, V_{tn1}$, and V_{tn2}, respectively. The partial derivative terms in (13) are computed numerically at the mean threshold voltages. It should be noted that the correlation between the different transistors threshold voltages is neglected for random WID variations [12]. This is due to the fact that V_t of the four transistors, in consideration, are identified as four independent and uncorrelated Gaussian random variables. This assumption simplifies the derivation of (13).

IV. Results and Discussion

In all the following simulations, an industrial 65-nm technology, with technological parameters shown in Table I, is employed. The

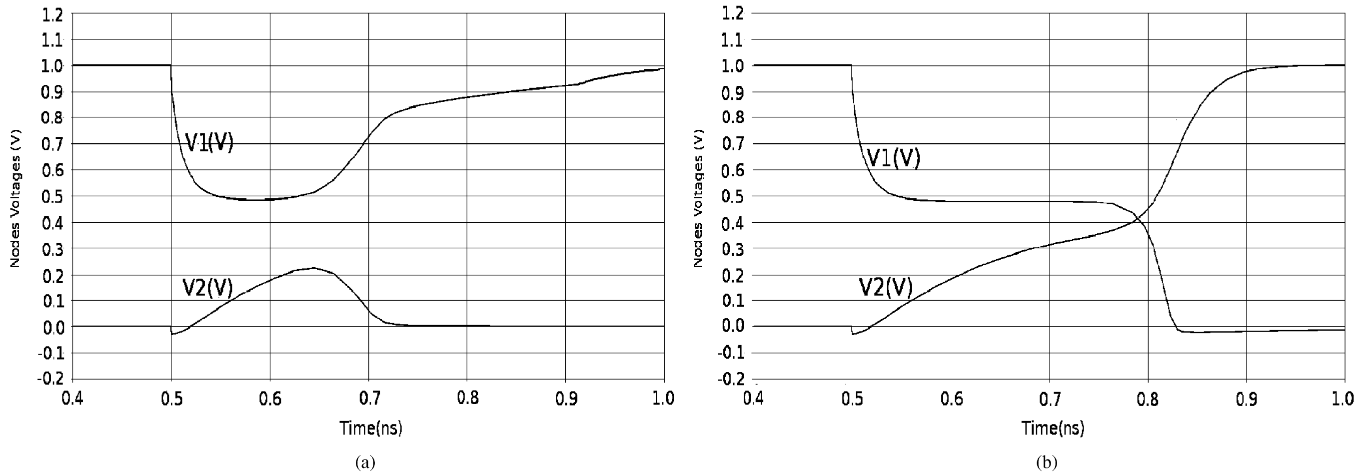

Fig. 2. Two nodes V_1 and V_2 for $V_{\rm DD} = 1.0$ V in (a) the non-flipping case and (b) the flipping case. The clock frequency is 1 GHz and $\tau = 250$ ps.

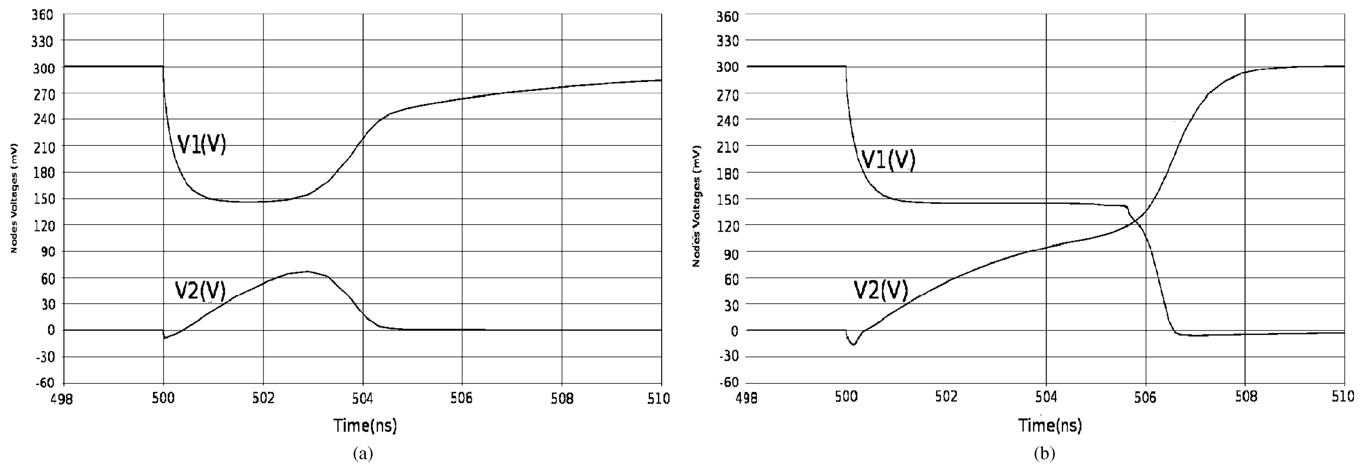

Fig. 3. Two nodes V_1 and V_2 for $V_{\rm DD} = 0.3$ V in (a) the non-flipping case and (b) the flipping case. The clock frequency is 1 MHz and $\tau = 250$ ps.

TABLE I
65-nm TECHNOLOGY INFORMATION AND SRAM SIZING [13]

	NMOS	PMOS
W/L ($\mu m/\mu m$)	0.195/0.065	0.11/0.065
V_{to} (mV)	342	-204
$\sigma_{V_{to}}$ (mV)	25.8	34.3

SRAM cell is sized such that its stability is maintained, as reported in [13].

A. Verification of the Model Assumptions

The assumptions used in deriving (3) and (4) are verified. The two nodes V_1 and V_2 voltages in the non-flipping case are shown in Figs. 2(a) and 3(a) for $V_{\rm DD} = 1$ V and $V_{\rm DD} = 0.3$ V, respectively. It is clear that, since V_2 voltage does not hit $V_{\rm DD}/2$, the SRAM cell is recovered. Figs. 2(b) and 3(b) show that when the V_2 node voltage hits $V_{\rm DD}/2$, the SRAM cell exhibits a soft error for $V_{\rm DD} = 1$ V and $V_{\rm DD} = 0.3$ V, respectively. Moreover, Figs. 2(b) and 3(b) show that node V_2 voltage is around 0 V as long as node V_1 voltage is falling. Once node V_1 voltage hits $V_{\min}, V_1$ stays constant at $V_{\min}$, whereas, node V 2 voltage rises to $V_{\rm DD}/2$.

It should be noted that the actual value of the inverter threshold voltage, V_M is slightly less than $V_{\rm DD}/2$. However, the difference between them is less than 4% of $V_{\rm DD}$ and is ignored. Also, the clock frequencies used in Figs. 2 and 3 are 1 GHz and 1 MHz, respectively, because the SRAM cell timing response is slower when $V_{\rm DD} = 0.3$ V than that when $V_{\rm DD} = 1.0$ V.

B. Verification of the Model Estimated Critical Charge

To verify the critical charge nominal value, and the critical charge variations model, the analytical model is compared to the simulation results using SPICE transient and Monte Carlo simulations. These simulations are performed to validate the nominal critical charge, and the critical charge variability model, respectively. In the following, the validation results for this model are presented. A large number of Monte Carlo runs (4000 runs) are used to provide a good accuracy in determining the critical charge mean and standard deviation. For each Monte Carlo run, the value of the current pulse charge, Q, that causes the cell to flip is determined. Then, the simulations are repeated for different $V_{\rm DD}$ values (from 0.1 to 1.2 V), to find the effect of reducing $V_{\rm DD}$ on the critical charge mean and variations. The SRAM sizing, shown in Table I, is used in the simulation setups. Hardware-calibrated statistical models are used to account for V_t variations.

1) Nominal Critical Charge: Fig. 4 shows the nominal critical charge value calculated from the proposed model, and compared to

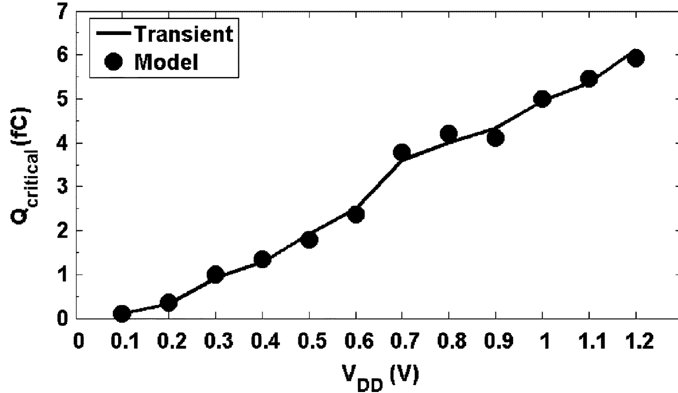

Fig. 4. Q_{critical} versus V_{DD} for $\tau = 250$ ps.

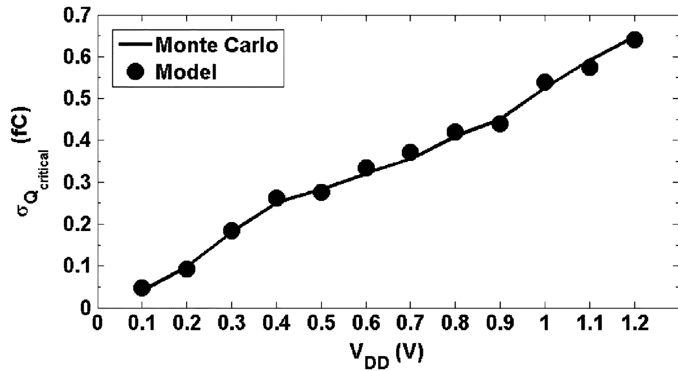

Fig. 5. Critical charge variations, $\sigma_{Q_{\mathrm{critical}}}$, versus V_{DD} for $\tau = 250$ ps.

the transient simulations results for different supply voltage values. It is obvious from Fig. 4 that reducing the supply voltage decreases the critical charge, which is expected.

2) Critical Charge Variations: In Section III, the derivation of the critical charge standard deviation using the proposed model is described. Fig. 5 shows the simulation result for $\sigma_{Q_{\mathrm{critical}}}$ for different V_{DD} values. Note that each data point represents $\sigma_{Q_{\mathrm{critical}}}$ calculated from 4000 Monte Carlo runs. Also, Fig. 5 shows the results from the proposed model. The model results exhibit a good match with the simulation results. Moreover, these results demonstrate that as V_{DD} is reduced for low power applications, $\sigma_{Q_{\mathrm{critical}}}$ is decreased.

C. Effect of the Coupling Capacitor on the Critical Charge Relative Variability

One of the most common techniques to mitigate soft errors in SRAM cells is increasing its node capacitance. Thus it is important to see the impact of increasing the node capacitance on the relative critical charge variations. Usually, a coupling capacitor, C_c, is employed between the storage nodes (V_1 and V_2). This coupling capacitor C_c increases the nodal capacitances of the SRAM cell storage nodes, and therefore, their critical charge is increased significantly. The model capacitances C_1 and C_2, have to be modified to account for C_c, by applying the Miller effect as follows [8]:

$$C_1' = C_1 + 2C_c \qquad C_2' = C_2 + 2C_c. \tag{12}$$

Fig. 6 portrays the overall relative variations $(\sigma_{Q_{\mathrm{critical}}}/\mu_{Q_{\mathrm{critical}}})$ versus C_c obtained from Monte Carlo simulations, and from the proposed model, for different values of V_{DD}, when $\tau = 250$ ps. The proposed model is in good agreement with Monte Carlo simulation results. It is obvious from Fig. 6 that, as C_c and V_{DD} increase, $\sigma_{Q_{\mathrm{critical}}}/\mu_{Q_{\mathrm{critical}}}$ decreases. The decreasing rate of $(\sigma_{Q_{\mathrm{critical}}}/\mu_{Q_{\mathrm{critical}}})$ is larger for higher values of V_{DD}.

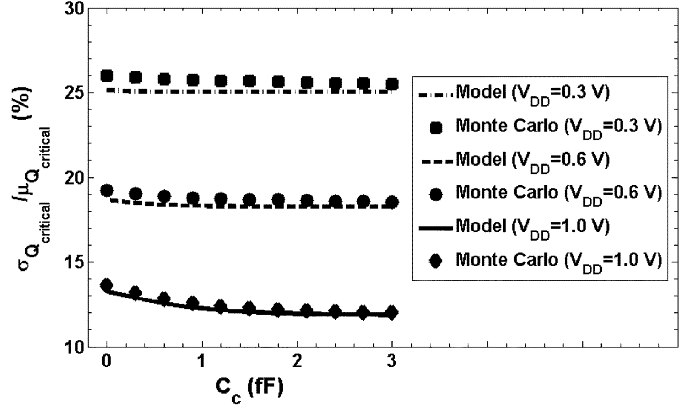

Fig. 6. Overall relative variations $(\sigma_{Q_{\mathrm{critical}}}/\mu_{Q_{\mathrm{critical}}})$ versus C_c for different values of V_{DD} when $\tau = 250$ ps.

D. Accuracy of the Proposed Model

Q_{critical} from the proposed model is compared with transient simulation results for different values of τ, V_{DD}, and C_c. The maximum error is 7.2%, and the average error is 3.8%. Also, $\sigma_{Q\mathrm{critical}}$ exhibits a maximum error of 11.3%, and an average error of 6.9%. Good agreement between the proposed model and the simulation results justifies all the assumptions used to derive the model. It should be mentioned that the unified current in (10) has different precision for different SRAM operating regions. This precision affects the accuracy of the proposed model for different operating regions. The maximum Q_{critical} error for the sub-threshold region ($V_{\mathrm{DD}} = 0.1$ to 0.3 V), the near-threshold region ($V_{\mathrm{DD}} = 0.4$ to 0.6 V), and the super-threshold region ($V_{\mathrm{DD}} = 0.7$ to 1.2 V), are 4.2%, 6.1%, and 7.2%, respectively. The average Q_{critical} error for the sub-threshold, the near-threshold, and the super-threshold regions, are 2.9%, 3.8%, and 3.6%, respectively. Also, The maximum $\sigma_{Q\mathrm{critical}}$ error for the sub-threshold, the near-threshold, and the super-threshold regions, are 7.6%, 9.2%, and 11.3%, respectively, whereas the average $\sigma_{Q\mathrm{critical}}$ error for the sub-threshold, the near-threshold, and the super-threshold regions, are 5.3%, 6.9%, and 6.5%, respectively.

Finally, the proposed analytical model advantages are summarized as follows.

1) The proposed model accounts for different bias conditions including the super-threshold, the near-threshold, and the sub-threshold SRAM design.
2) In [8], the value of the injected current pulse charge Q is obtained via iterative transient simulations by increasing Q by a small amount ($\sim$ 0.001 fC) in SPICE till flipping occurs. Although this method is used in calculating D2D variations by using corner-based or worst-case methods, in which the value of Q is obtained by using SPICE simulations at the required corner. This technique can not be used for the WID statistical variations, since Q must be calculated for each statistical run. Consequently, the model in [8] accounts only for D2D variations. In (5), Q is calculated analytically without performing any SPICE simulations. Therefore, the limitation in [8] for WID variations modeling is refined.
3) Both D2D and WID variations are taken into account in the proposed model. The WID variations modeling is much more complex and difficult than D2D variations modeling because D2D variations are easily modeled by using corner-based techniques

which assume that all devices on a given die have the same parameter value, that is shifted away from the mean by a fixed amount (i.e., shifting all devices threshold voltage, length, or width, by a fixed amount). Then, the new value of the critical charge is calculated from the proposed model analytical formulas at this corner. However, WID variations modeling requires representing each device parameter, within the same die, by a separate random variable. Equation (11) models the impact of the WID variations on the critical charge. The simulations results are shown only for WID variations modeling due to space limitations.

4) Several design insights are extracted from the proposed model such as the impact of the supply voltage, the coupling capacitor adoption, transistors sizes, and the pulse width, on the critical charge variability. These results are not included in this paper due to space limitations.
5) The proposed model is useful for the statistical SRAM design framework. In this framework, constraints on the SRAM static noise margin, writing current, leakage power, area, and critical charge, are imposed. An optimization problem is solved by finding the SRAM six transistors sizes that maximize the overall SRAM yield (i.e., maximize the number of SRAM cells that satisfy all the constraints) under process variations. Analytical formulas for the critical charge mean and standard deviation are required for this statistical framework design. The critical charge constraint is obtained from the SER constraint.
6) In the proposed model, the inverter threshold voltage, V_M, is assumed to equal $(V_{\mathrm{DD}}/2)$. This assumption is verified for the proposed SRAM sizing. However, if V_M is far from $(V_{\mathrm{DD}}/2)$, the proposed model should be derived again by replacing $(V_{\mathrm{DD}}/2)$ by V_M. The dependence of V_M on the threshold voltages results in fluctuations of V_M around its nominal value. The relative variations of V_M to its nominal value is found to be less than 0.8% for all SRAM operating regions. Therefore, V_M is considered constant from the variability perspective. Accordingly, the value of V_M should be calculated for the SRAM cell size, by performing SPICE simulations, and used in the proposed model.
7) The proposed model can be used for future CMOS technology nodes (i.e., 45, 32, and 22 nm), since, the transistor model parameters such as the technology parameters and the threshold voltage standard deviation σ_{V_t} can be easily obtained. Therefore, the proposed model is scalable in terms of technology scaling and can be used to predict the critical charge variability for future technology nodes.

V. Conclusion

In this paper, an analytical model accounting for both D2D and WID variations over a wide range of SRAM bias conditions, including super-threshold, near-threshold, and sub-threshold regions, is proposed. The proposed model deals with the D2D variations, by using corner-based methods. Moreover, it deals with the WID variations, by using statistical techniques. The accuracy of the proposed model is validated by transient and Monte Carlo SPICE simulation results, for an industrial 65-nm technology, over a wide range of supply voltages and coupling capacitors. The proposed model shows that, the use of the coupling capacitor in the SRAM cell, as a soft error mitigation technique, decreases the relative critical charge variations.

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