Novel Timing Yield Improvement Circuits for High-Performance Low-Power Wide Fan-In Dynamic OR Gates

Hassan Mostafa, *Student Member, IEEE*, Mohab Anis, *Senior Member, IEEE*, and Mohamed Elmasry, *Fellow, IEEE*

***Abstract*—Dynamic gates are preferred in the design of high-performance modules in modern microprocessors due to the relatively high speed of dynamic gates compared with that of standard CMOS gates. These high performance modules have strict timing constraints. Due to the increased process variations in scaled technologies, the dynamic circuit delay exhibits a substantial variability around its nominal value. This delay variability results in violating the timing constraints, and correspondingly, causes a timing yield loss. In this paper, novel negative capacitance circuits are developed, for the first time, to statistically improve the timing yield under process variations. Post layout simulation results, referring to an industrial hardware-calibrated TSMC 65 nm CMOS technology, show that the adoption of the negative capacitance circuit to a 64-input wide dynamic OR gate is capable of improving the timing yield from 50% to 100%. Moreover, the negative capacitance circuit adoption results in reducing the delay variability at the expense of excess power overhead.**

***Index Terms*—Deep sub-micron, domino logic circuits, negative capacitance circuit, process variations, register file, timing yield improvement.**

I. Introduction

REGISTER files are one of the most essential modules in the critical path of modern microprocessors [1], [2]. The basic operation of a register file is to store temporary and intermediate variables that are being used in the execution of a sequence of instructions. Fig. 1 depicts the block diagram of the Intel Pentium 4 processor architecture [1], [3]. In this processor, two register files are employed in the data path, which are marked with a dotted box in Fig. 1. These register files are the integer register file, denoted by Integer RF, and the floating point register file, denoted by FP RF. Data are read from or written to these register files with each instruction execution. Therefore, fast register file architectures are crucial in achieving a high-performance operation in microprocessors [1].

Fig. 2(a) demonstrates the block diagram of a simplified register file, which is composed of an array of Static Random Access Memory (SRAM) cells based registers, a read port, and a write port. Typically, register files have multiple read and write ports and also have many more registers. Read and write ports are generally implemented by using multiplexers (MUXs) and de-multiplexers (DE-MUXs) circuits, respectively. Typically, these MUXs and DE-MUXs circuits are realized by utilizing OR and inverter gates, as shown in Fig. 2(b). This figure illustrates a simple 4×1 MUX with 4-input lines (D_0, D_1, D_2, and D_3), 2-bit address lines (S_0 and S_1), and one output (Out). Therefore, a register file with 2^n registers requires n-bit address lines, and hence, $(n+1)$-input intermediate OR gates and a 2^n-input output OR gate. As a result, for large register files, wide fan-in dynamic OR gates are required for address coding/decoding. Also, the propagation delay of the wide fan-in dynamic OR gate increases linearly with fan-in [4]. This makes the wide dynamic OR gate an excellent choice for the implementation of high-performance modules.

The aggressive scaling of CMOS technology towards the nanometer regime has created large statistical process variations in the transistor parameters such as threshold voltage, channel length, and mobility [5]–[8]. Therefore, the process variations are considered one of the most important design challenges

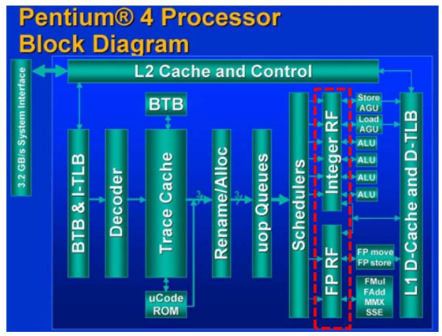

Fig. 1. Intel Pentium 4 processor block diagram [3].

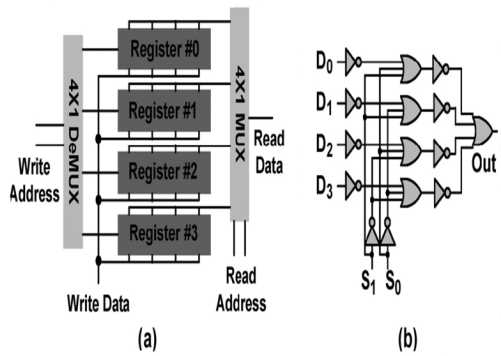

Fig. 2. (a) Block diagram of a simplified register file and (b) Read port implemented using 4×1 MUX [1].

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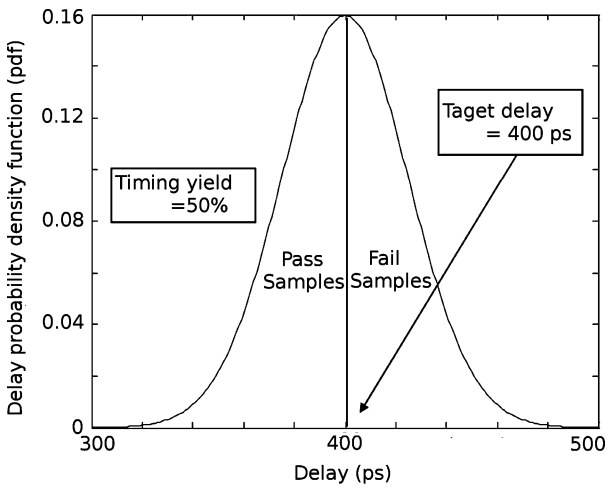

Fig. 3. Delay pdf due to process variations. It shows, intuitively, that 50% of circuits do not meet the target delay (400 ps in this example) [17].

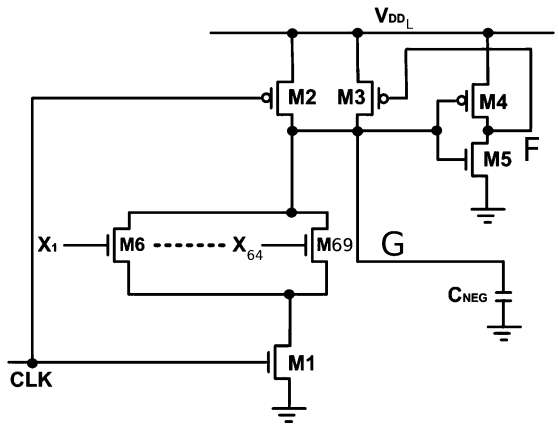

Fig. 4. The 64-input dynamic OR gate circuit with a negative capacitance employed at the highly capacitive output node, G.

for sub-100-nm CMOS technologies. These process variations are classified into die-to-die (D2D) variations and within-die (WID) variations. In D2D variations, all the devices on the same die are assumed to have the same parameters. However, the devices on the same die are assumed to behave differently for WID variations [5], [9], [10]. The process variations result in dynamic OR gate delay variability. Consequently, some of the fabricated circuits do not meet the target delay, resulting in a timing yield degradation. Consider as an intuitive example, a dynamic OR gate circuit that is designed for a specific target delay. Due to random process variations, the delay can be modeled by a normal distribution with the probability density function (pdf) in Fig. 3 [9], [10]. Here, 50% of the total number of circuits do not meet the desired target delay constraint due to process variations. Therefore, the dynamic circuits must be designed by using statistical design tools [11], [12], and process variations compensation circuits [13], [14], to improve the timing yield.

In [15]–[18], statistical gate sizing tools are used to improve the timing yield. The timing yield improvement begins with sizing the dynamic OR gate for the target delay, A_o. Following that, a Monte Carlo statistical analysis is conducted to calculate the standard deviation of the delay variability, σ. The main idea of the timing yield improvement is to shift the delay pdf, centered around its mean A_o, to a new delay pdf with a mean A'_o. The relationship between A'_o and A_o is given by

$$A'_o = A_o - n\sigma \tag{1}$$

where σ is the standard deviation of the delay variability around A_o, and "n" depends on the desired timing yield, Y_o, and is obtained from the normal distribution tables. For example, if the desired timing yield is 99.87% $(\mathrm{Y}_o = 99.87\%)$, then "n" equals 3.0 from the normal distribution tables. The delay reduction from A_o to A'_o is accomplished by iterative statistical gate sizing. Despite its effectiveness in improving the timing yield, statistical gate sizing might not achieve the desired timing yield under a given power constraint [17]. By other words, the power overhead, associated with the statistical gate sizing, is not controlled and might exceed the power constraint. Accordingly, the statistical gate sizing fails to achieve the target timing yield improvement with the power constraint satisfaction. In addition, the statistical gate sizing technique fails in some cases to achieve the target timing yield as reported in [15].

In this paper, a negative capacitance circuit is added at the highly capacitive output node, G, of a wide fan-in 64-input dynamic OR gate, as shown in Fig. 4. This negative capacitance connection reduces node G parasitic capacitance, and correspondingly, improves the timing yield without changing the gate sizing. The timing yield improvement is achieved by calculating the amount of the negative capacitance that should be added to the parasitic capacitance, at node G to shift the dynamic OR gate delay pdf center from A_o to A'_o without affecting the gate sizing. It should be emphasized that this negative capacitance implementation is introduced for timing yield improvement at the expense of excess power dissipation. This means that although the negative capacitance adoption reduces the OR gate dynamic power, the total power (the OR gate power and the negative capacitance power) increases [19].

The paper is organized as follows: Section II introduces the negative capacitance circuit implementation techniques. Three negative capacitance circuits are proposed and analyzed in Section III. Section IV provides a discussion of the statistical timing yield improvement technique by using the negative capacitance circuit adoption. Simulation results and discussions of the three developed negative capacitance circuits are given in Section V. Finally, some conclusions are drawn in Section VI.

II. Negative Capacitance Circuit Implementation Techniques

In this section, two negative capacitance circuit implementation techniques are explained. The first technique is based on the Miller equivalent of a non-inverting amplifier with a feedback capacitance. The second technique is based on the negative impedance converter loaded with a capacitance.

A. Miller Effect Based Negative Capacitance Circuit

The negative capacitance circuit is designed by using a capacitance, C_F, connected between the input and output nodes of a

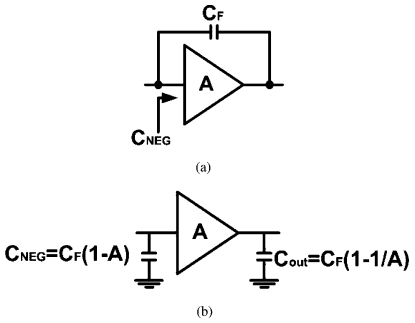

Fig. 5. (a) Negative capacitance implementation using a non-inverting amplifier with a feedback capacitance. (b) Miller equivalent circuit of (a) [19], [21].

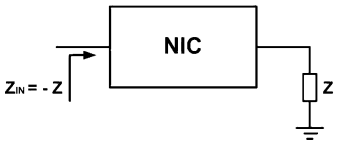

Fig. 6. NIC based negative capacitance implementation [19], [20].

non-inverting amplifier with gain A as displayed in Fig. 5(a). Applying the Miller effect on this circuit results in the equivalent circuit in Fig. 5(b). The input equivalent capacitance of this circuit, $\mathrm{C_{NEG}}$, is given by

$$C_{\mathrm{NEG}} = C_F(1 - A) \tag{2}$$

Therefore, when the amplifier gain, A, is larger than unity, $\mathrm{C_{NEG}}$ takes on negative values and a negative capacitance circuit is developed.

In (2), the negative capacitance $\mathrm{C_{NEG}}$ is achieved only and only if the amplifier gain, A, is constant and independent of frequency (i.e., the amplifier bandwidth is sufficiently larger than the NOR gate maximum operating frequency). This means that the closed loop response of the amplifier in the time domain is faster than that of the NOR gate. Unfortunately, the requirement to increase the speed of the amplifier results in increasing the power overhead of the negative capacitance circuit.

B. Negative Impedance Converter (NIC) Based Negative Capacitance Circuit

The Negative Impedance Converter (NIC) is a two-port circuit whose input impedance is the negative of the load impedance at its output port, as shown in Fig. 6 [19]–[21]. When the NIC circuit is loaded with a capacitance, C_L, at its output node, an equivalent negative capacitance is seen at the input node. Therefore, a negative capacitance, $\mathrm{C_{NEG}}$, circuit is implemented. The value of this $\mathrm{C_{NEG}}$ is given by

$$C_{\mathrm{NEG}} = -\beta C_L \tag{3}$$

where β is dependent on the NIC circuit implementation.

Similarly, in (3), the negative capacitance $\mathrm{C_{NEG}}$ is achieved only and only if the factor β is constant with frequency (i.e., the NIC bandwidth is sufficiently larger than the NOR gate maximum operating frequency). This means that the closed loop response of the NIC in the time domain is faster than that of the NOR gate. Unfortunately, the requirement to increase the speed of the NIC results in increasing the power overhead of the negative capacitance circuit.

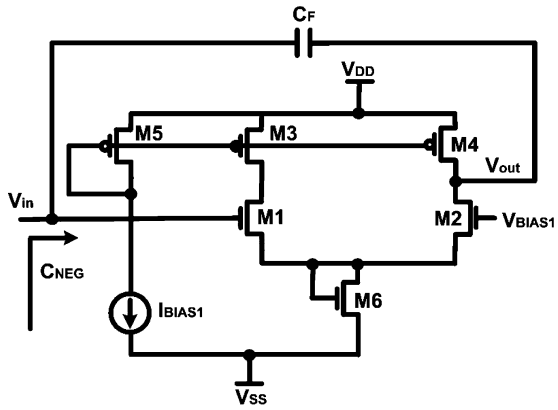

Fig. 7. Proposed differential-pair amplifier based negative capacitance (DA-NC) circuit implementation.

III. Proposed Negative Capacitance Circuits

A. Differential-Pair Amplifier Based Negative Capacitance (DA-NC) Circuit

In Fig. 7, a non-inverting differential-pair amplifier, with gain A, is employed with a feedback capacitance, C_F, to implement the Miller effect based negative capacitance circuit. When the following transistor pairs, (M1 and M2) and (M3, M4, and M5) are matched, the differential-pair amplifier gain, A, is given by

$$A \approx \frac{g_{m1}}{g_{d2} + g_{d4}} \tag{4}$$

where g_{m1} is the transconductance of transistor M1. g_{d2} and g_{d4} are the drain-to-source output conductance of transistors M2 and M4, respectively. Therefore, the gain, A, is controlled by the amplifier transistors sizes, the DC bias voltage, V_{BIAS1}, and the DC bias current, I_{BIAS1}. Considering the effect of the input capacitance of the DA-NC circuit, C_{M1}, (2) is rewritten as $C_{\mathrm{NEG}} - C_{M1} = C_F(1 - A)$. For example, to achieve a negative capacitance, $C_{\mathrm{NEG}} = -2$ fF with an input capacitance $C_{M1} = 1$ fF, if the feedback capacitance, $C_F = 1$ fF, the required differential-pair amplifier gain, A is 4.0.

In Fig. 4, the 64-input dynamic OR gate highly capacitive output node, G, is initially pre-charged to the OR gate supply voltage, V_{DD_L}. Then, depending on the inputs, the node G is either maintained at logic "1" or pulled down to ground (logic "0"). The idea of the DA-NC circuit is to allow node G to see a reduced capacitance (Due to the negative capacitance circuit adoption), when discharging from V_{DD_L} to $V_{DD_L}/2$. Therefore, the fall time is reduced due to this negative capacitance adoption. When the output node G reaches $V_{DD_L}/2$, the positive feedback of the keeper transistor (i.e., transistors M3–M5) circuit becomes strong enough to continue discharging node G to ground. Accordingly, the input dynamic range (i.e., the range of the input voltage over which the amplifier exhibits a linear gain) of the differential-pair amplifier in Fig. 7, should include the range from V_{DD_L} to $V_{DD_L}/2$. This wide input dynamic range results in reducing the amplifier gain. Therefore, there is

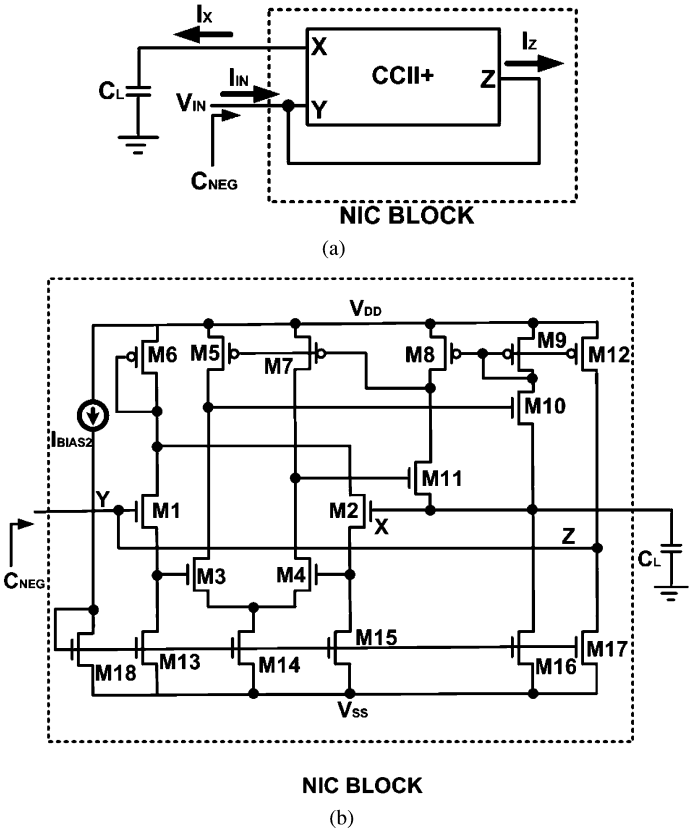

Fig. 8. (a) NIC based negative capacitance circuit using CCII+ [19]. (b) Circuit implementation of this negative capacitance [22].

a trade-off between the amplifier gain and the input dynamic range.

In addition, the amplifier bandwidth must be sufficiently larger than the NOR gate operating frequency to achieve a negative capacitance according to (2) which results in increasing the negative capacitance power overhead and reducing the amplifier gain due to the constant gain-bandwidth product of the amplifier.

B. Current Conveyor Based Negative Capacitance (CC-NC) Circuit

The NIC based negative capacitance circuit is implemented by using the positive second generation current conveyor (CCII+) [19], [20], [22]. This current conveyor based negative capacitance (CC-NC) circuit block is shown in Fig. 8(a), and its implementation is illustrated in Fig. 8(b).

The CCII+ is a three terminal analog circuit with terminals X, Y, and Z. The function of the CCII+ is defined as [22]

$$\begin{bmatrix} v_x \\ i_y \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & +1 & 0 \\ 0 & 0 & 0 \\ +1 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ v_y \\ v_z \end{bmatrix} \tag{5}$$

Therefore, the CCII+ performs a voltage conveying action from terminal Y to terminal X, and a current conveying action from terminal X to terminal Z. In addition, no current is flowing into terminal Y. If ε_v, the error in conveying the voltage at node Y to node X, and ε_i, the error in conveying the input current at node X to node Z, are considered, the input voltage at terminal Y in Fig. 8(a) is given by: $V_{\rm IN} = V_Y = V_X/(1-\varepsilon_v) = I_X/[sC_L(1-\varepsilon_v)]$. The input current at terminal Y is given by: $I_{\rm IN} = -I_Z = -I_X(1-\varepsilon_i)$, since the current $I_Y = 0$. Correspondingly, the input impedance at terminal Y is given by: $Z_{\rm IN} = V_{\rm IN}/I_{\rm IN} = -1/[sC_L(1-\varepsilon_v)(1-\varepsilon_i)] = -1/[sC_{\rm NEG}]$. Thus, the value of $C_{\rm NEG}$ is given by: $C_{\rm NEG} = -(1-\varepsilon_v)(1-\varepsilon_i)C_L$. Thus, the constant, β, is given by [19]

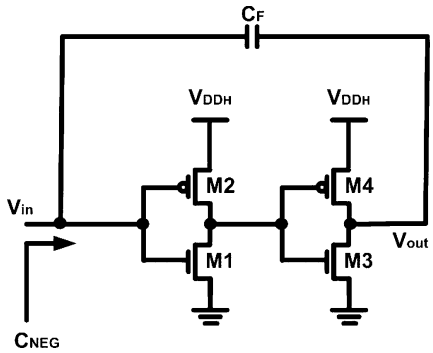

Fig. 9. Proposed two-inverters buffer based negative capacitance (B-NC) circuit implementation.

$$\beta = (1-\varepsilon_v)(1-\varepsilon_i) \tag{6}$$

where ε_v is the error in conveying the voltage at node Y to node X, and ε_i is the error in conveying the input current at node X to node Z. Considering the effect of the input capacitance of the CC-NC circuit, C_Y, (3) is rewritten as $C_{\rm NEG} - C_Y = -\beta C_L$.

The main advantage of the CCII+ over the differential-pair amplifier is that the CCII+ does not exhibit a constant gain-

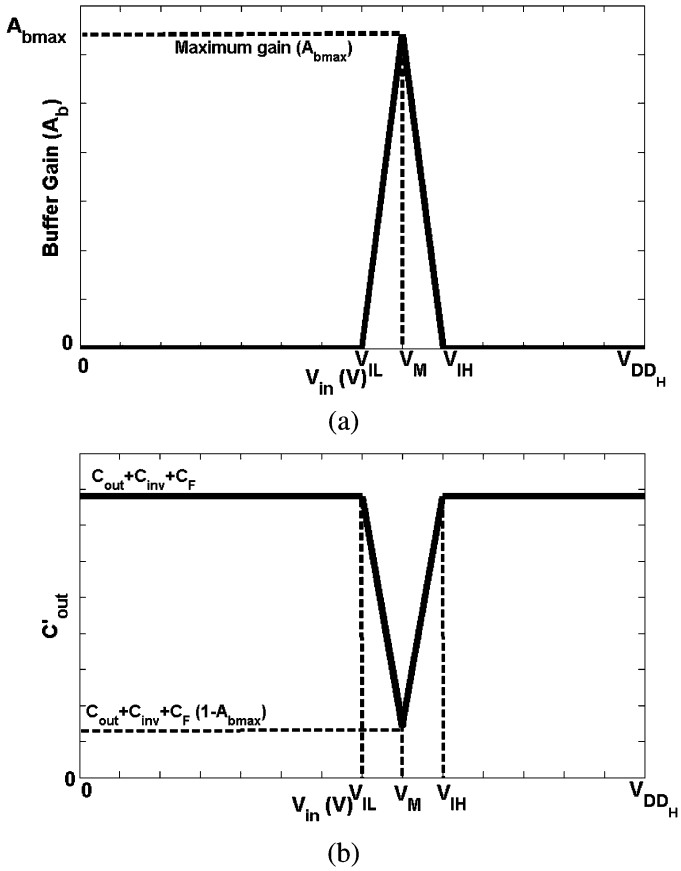

Fig. 10. (a) Two-inverters buffer gain, A_b, versus the input voltage, $V_{\rm in}$. (b) Total capacitance at node G, $C'_{\rm out}$, when the B-NC is adopted.

bandwidth product [23], whereas the differential-pair amplifier does. For example, if the differential-pair amplifier gain-bandwidth product is 5 GHz, and the input signal frequency is 5 GHz, the maximum gain, achieved by this amplifier, is limited to unity and the DA-NC fails to implement a negative capacitance circuit. Accordingly, the CC-NC is the best alternative for high frequency input signals, because the CCII+ is not prone to the constant gain-bandwidth product limitation. However, the CC-NC power dissipation and area are larger than those in the DA-NC. In addition, from (2) and (3), the capacitance, C_L, used in the CC-NC, is larger than the capacitance, C_F, used in the DA-NC to implement the same negative capacitance value.

Moreover, the CCII+ speed must be faster than the NOR gate speed to achieve a negative capacitance according to (3) which results in increasing the negative capacitance power overhead and making the factor β less than unity. Accordingly, a larger $\rm C_L$ value is required to compensate the reduction of the factor β. The advantage of the CC-NC over the DA-NC is that the reduction of the factor β of the CCII+ (due to the large bandwidth requirements) is much less than the reduction of the gain A of the amplifier because the CCII+ is not prone to the constant gain-bandwidth product limitation while the differential amplifier is.

C. Buffer Based Negative Capacitance (B-NC) Circuit

The DA-NC and the CC-NC circuits are implemented by using analog building blocks such as the differential-pair amplifier and the CCII+, respectively. These analog circuits tend to be power-hungry due to the high levels of DC biasing. Therefore, Fig. 9 displays the implementation of a digital two-inverters buffer based negative capacitance (B-NC) circuit. The B-NC circuit belongs to the Miller effect based negative capacitance technique by applying a two-inverters buffer as a non-inverting amplifier.

The gain of this two-inverters buffer, A_b, is illustrated in Fig. 10(a) versus the buffer input voltage ($V_{\rm in}$), where V_{DD_H} is the buffer supply voltage, V_M is the buffer threshold voltage, V_{IL} is the maximum buffer input voltage that results in zero output voltage, and V_{IH} is the minimum buffer input voltage that results in an output voltage equals to the supply voltage, V_{DD_H}. The maximum gain, $A_{b_{\max}}$, occurs at the buffer threshold voltage, V_M. Fig. 10(b) displays the corresponding total capacitance at node G (including the negative capacitance), $C'_{\rm out}$, as a function of $V_{\rm in}$, where $C_{\rm inv}$ is the input capacitance of the buffer circuit, and $C_{\rm out}$ is the total capacitance at node G without the negative capacitance adoption.

Similar to the DA-NC circuit, the B-NC circuit should allow node G to see a reduced capacitance (Due to the negative capacitance circuit adoption), when discharging from V_{DD_L} to $V_{DD_L}/2$. Therefore, the fall time is reduced due to this negative capacitance. To achieve this fall time reduction, the buffer maximum gain, $A_{b_{\max}}$, is designed to occur at an input voltage of V_{DD_L}. Thus, the buffer threshold voltage, V_M, should be designed equal to V_{DD_L}. According to Fig. 10(b), the output

capacitance, C'_{out}, is averaged over the input voltage from $V_{DD_L}/2$ to V_{DD_L} and given by

$$C'_{\text{out}} = C_{\text{out}} + \underbrace{C_{\text{inv}} + C_F\left(1 + A_{b_{\max}}\left(\frac{V_{IL}}{V_{DD_L}} - 1\right)\right)}_{C_{\text{NEG}}} \tag{7}$$

The value of V_{IL}, and $A_{b_{\max}}$ are calculated by conducting SPICE DC analysis. The values of C_{out}, and C_{inv} are obtained from the layout parasitic extractions by using the CALIBRE tool provided by Mentor Graphics. According to [24], increasing the buffer transistors sizes increases the maximum buffer gain, $A_{b_{\max}}$, while using high-V_t transistors results in reducing $A_{b_{\max}}$ value.

To calculate the relationship between V_{DD_H}, the buffer supply voltage, and V_{DD_L}, the dynamic OR gate supply voltage, the well-known alpha-power law model for the transistors current [25] is adopted. In [25], the transistor current in the saturation region is modeled as:

$$i_n = K_{n'}(W/L)(V_{GS} - V_{tn})^{\alpha_n} \tag{8}$$

where V_{tn} is the threshold voltage, $\mathrm{K}_{n'}$ is a technological parameter, α_n is the velocity saturation exponent ranges from 1 to 2, depending on whether the transistor is in deep velocity or pinch-off saturation, and W and L are the width and length of the transistor channel, respectively. According to this model, the inverter switching voltage, V_M, is given by [25]

$$V_M = \frac{r\,(V_{DD_H} - |V_{tp}|) + V_{tn}}{1 + r} \quad \text{where}$$
$$r = \left(\frac{K_{p'}(W/L)_p}{K_{n'}(W/L)_n}\right)^{1/\alpha} \quad \text{and } \alpha = \alpha_n = \alpha_p \tag{9}$$

where V_{tn} and V_{tp} are the threshold voltages, α_n and α_p are the velocity saturation exponents, $\mathrm{K}_{n'}$ and $\mathrm{K}_{p'}$ are the technology parameters, and $(\mathrm{W/L})_n$, and $(\mathrm{W/L})_p$ are the aspect ratios of the nMOS and pMOS transistors, respectively. Thus, by equating V_M to V_{DD_L}, the buffer supply voltage, V_{DD_H}, is given by

$$V_{DD_H} = \left(1 + \frac{1}{r}\right) \times V_{DD_L} + |V_{tp}| - \frac{V_{tn}}{r} \tag{10}$$

Unfortunately, the B-NC circuit exhibits a large power due to the static power which occurs because the maximum input voltage to the inverter equals V_{DD_L} (the node G maximum voltage) is unable to turn the inverter pMOS transistor completely OFF as the inverter supply voltage is V_{DD_H} [24]. In order to reduce this static power, the difference between V_{DD_H} and V_{DD_L} should be designed slightly larger than $|V_{tp}|$.

From (10), the difference $V_{DD_H} - V_{DD_L} = (V_{DD_L} - V_{tn})/r + |V_{tp}|$ which implies that by increasing r and using high-V_t buffer transistors, this difference is designed close to $|V_{tp}|$. For example, if standard-V_t transistors are adopted with $V_{tn} = 0.31$ V and $|V_{tp}| = 0.35$ V as provided by TSMC 65 nm CMOS technology model files and assuming $\mathrm{r} = 2$, the difference $V_{DD_H} - V_{DD_L} = 0.6$ V which is higher than $|V_{tp}|$ by a factor of 1.7X. However, the difference $V_{DD_H} - V_{DD_L} = 0.57$ V (close to $|V_{tp}|$ value of 0.54 V), when high-V_t transistors are utilized with $V_{tn} = 0.49$ V and $|V_{tp}| = 0.54$ V and $\mathrm{r} = 10$. This makes the B-NC circuit dissipates lower power than that of the DA-NC and the CC-NC circuits. Moreover, the B-NC circuit provides a higher gain and correspondingly lower feedback capacitance requirement than that of the DA-NC and the CC-NC circuits. Therefore, the B-NC circuit is only suitable for CMOS technologies which allow dual supply voltage and dual threshold voltage utilization.

It should be noted that the speed of the buffer amplifier must be faster than that of the NOR gate to achieve a negative capacitance based on (2). Since the utilization of high-V_t transistors (to reduce the power consumption) results in reducing the speed of the buffer amplifier, thus, the buffer transistor sizes should be increased to compensate for this speed reduction. This, in turn, results in increasing the negative capacitance power overhead and more capacitive loading at node G (i.e., larger C_{inv} values). Therefore, there is a trade-off between the buffer speed requirement and the negative capacitance value (which is affected by increasing C_{inv}) and the associated power overhead.

IV. Statistical Timing Yield Improvement Using Negative Capacitance

Assume that the dynamic OR gate circuit is designed such that the nominal delay is the target delay, A_o (This can be performed at any design corner), the circuit delay, A_o, is given by [24]

$$A_o = \zeta C_{\text{out}} \tag{11}$$

where ζ is a proportionality constant, dependent on the output resistance of the dynamic OR circuit, and C_{out} is the circuit parasitic output capacitance.

Due to the process variations, this dynamic OR gate circuit delay is normally distributed around this nominal value. Therefore, the resulting timing yield is $\sim$ 50% as shown in Fig. 3. It should be noted that the impact of the process variations on C_{out} is neglected with respect to the impact on the output resistance [26]. This is due to the fact that the output resistance depends on the transistors threshold voltage, the main source of the variability [5], [6], [26]. To improve the timing yield, the delay variability, which is centered around A_o, is shifted to a new center A'_o given by

$$A'_o = A_o - n\sigma' \tag{12}$$

where σ' is the standard deviation of the delay variability around A'_o, and "n" is dependent on the desired timing yield, Y_o, as explained in (1). It should be mentioned that (12) can be used only when σ' is known in advance. These two conditions are satisfied when the negative capacitance circuit is adopted as will be discussed in this section. In statistical gate sizing [15]–[17], (12) should not be used because σ' might be larger or smaller than σ, and also σ' is not known in advance for the new gate sizing.

Fig. 11 illustrates how the timing yield is improved by shifting the delay pdf to a shorter mean delay, A'_o.

In [15]–[17], the circuit delay, A_o, is reduced to A'_o by using the gate sizing. This technique might fail in achieving the required timing yield with an acceptable power overhead. Therefore, many iterations are required. In this paper, the delay, A_o, is

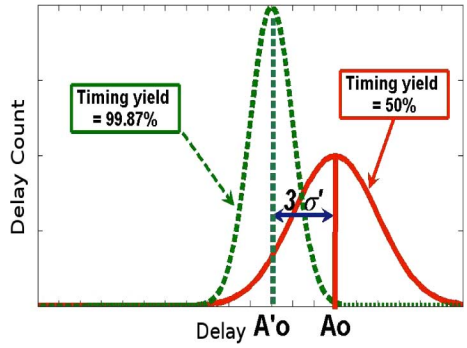

Fig. 11. Timing yield improvement is obtained by shifting the delay pdf center from A_o to A'_o. In this case, $A'_o = A_o - 3\sigma'$ as σ' is less than σ and is known in advance.

reduced by adding a negative capacitance at the output node of the dynamic OR gate. Therefore, the proposed negative capacitance technique gives more degrees of freedom to achieve the desired timing yield with an acceptable power overhead. The addition of the negative capacitance, C_{NEG}, at the circuit output node results in a modified output capacitance, C'_{out}, which is given by

$$C'_{\text{out}} = C_{\text{out}} + C_{\text{NEG}} \tag{13}$$

and accordingly, the modified circuit delay, A'_o, is expressed as

$$A'_o = \zeta C'_{\text{out}} \tag{14}$$

By using (11)–(14), the negative capacitance, C_{NEG}, which achieves the desired timing yield improvement, is expressed as

$$C_{\text{NEG}} = \frac{-n\sigma'}{\zeta}. \tag{15}$$

From (11), the delay A_o variability, $\Delta A_o = \Delta\zeta\, C_{out}$, and from (14), the delay A'_o variability, $\Delta A'_o = \Delta\zeta\, C'_{out}$, assuming that the capacitances, C_{out} and C'_{out}, are constants from the variability perspective. From (13), $C'_{out} < C_{out}$ because C_{NEG} has a negative value. Therefore, $\Delta A'_o < \Delta A_o$ which explains why the adoption of the negative capacitance reduces the delay variability. The ratio between σ' and σ is obtained by computing

$$\frac{\sigma'}{\sigma} = \frac{\Delta A'_o}{\Delta A_o} = \frac{C'_{\text{out}}}{C_{\text{out}}} = 1 + \frac{C_{\text{NEG}}}{C_{\text{out}}}. \tag{16}$$

From (15) and (16), C_{NEG} is given by

$$C_{\text{NEG}} = \frac{-\frac{n\sigma}{\zeta}}{1 + \frac{n\sigma}{A_o}}. \tag{17}$$

It should be noted that the negative capacitance, C_{NEG}, exhibits some variations due to its circuit implementation. However, these variations contribution to σ' is ignored in (16) and (17) to have an initial guess for the required value of C_{NEG}. This contribution should be calculated because the negative capacitance circuit has different implementations such as DA-NC, CC-NC, and B-NC circuits. If the negative capacitance circuit variability is taken into account, the delay variability, is expressed as follows:

$$\frac{\Delta A'_o}{A'_o} = \frac{\Delta\zeta}{\zeta} + \frac{\Delta C_{\text{NEG}}}{C_{\text{out}} + C_{\text{NEG}}}. \tag{18}$$

Since the factor $(\Delta\zeta)/(\zeta) = (\Delta A_o)/(A_o)$, the standard deviation σ' is given by [26]

$$\left(\frac{\sigma'}{A'_o}\right)^2 = \left(\frac{\sigma}{A_o}\right)^2 + \underbrace{\frac{(\sigma_{C_{\text{NEG}}}/C_{\text{NEG}})^2}{((C_{\text{out}} + C_{\text{NEG}})/C_{\text{NEG}})^2}}_{C_{\text{NEG}}\text{ variability}}. \tag{19}$$

The negative capacitance circuit should be designed such that its variability contribution to σ' is small (i.e., the contribution of the factor ζ is dominant). Thus, (17) is valid and the negative capacitance contribution to σ' is neglected. However, if this contribution is not neglected and taken into account, (17) is used as an initial guess and then the following algorithm is adopted.

1) Calculate the initial value of C_{NEG} by using (17).
2) Conduct Monte Carlo simulations while the negative capacitance circuit is adopted.
3) Determine the values of A'_o and σ'.
4) Calculate the value of the timing yield. If the timing yield is greater than or equal to 99.87%, the target timing yield improvement is achieved and the algorithm stops. If the timing yield is less than 99.87%, calculate the new C_{NEG} by using the new σ' value by using (15).
5) Repeate steps 2–4 above.

This negative capacitance, C_{NEG}, is designed by using the DA-NC, the CC-NC, and the B-NC circuits. In Section V, the three negative capacitance circuits are adopted for the 64-input dynamic OR gate, and the simulation results are discussed.

V. Simulation Results and Discussions

The 64-input dynamic OR gate in Fig. 4 is applied to verify the proposed timing yield improvement technique. The parasitic capacitances at the intermediate node G are large due to the 64 nMOS transistors diffusion capacitances. Therefore, the negative capacitance, C_{NEG}, is connected to this node, as shown in Fig. 4.

The dynamic OR gate is designed to achieve a nominal high-to-low delay at node G, A_o, of 433 ps, and an associated total average power dissipation of 62.8 μW at temperature T = 120°C with a layout area of 135.8 μm^2. The supply voltage used in the dynamic OR gate design, V_{DD_L}, is 0.8 V [27]. The OR gate design is performed by using post layout simulations referring to an industrial hardware-calculated TSMC 65 nm CMOS technology. Low-V_t transistors are utilized for the OR gate transistors to achieve high performance. The total capacitance at the node G of the OR gate, C_{out}, is calculated from the circuit layout, by using the CALIBRE tool provided by Mentor Graphics, and equals 15.1 fF (this layout capacitance includes all the parasitic capacitances coupled to node G). Therefore, the constant ζ, defined in (11), equals 28.68 ps/fF.

A 5 000 point Monte Carlo analysis, including the mismatch between transistors is performed. An industrial hardware-calibrated TSMC 65 nm CMOS technology transistor statistical

models is used to investigate the effect of process variations on the simulated circuits. In [28], [29], it has been demonstrated that the utilization of statistical transistor models is capable of accounting for both D2D and WID variations. A very good fitting with the measured data is reported in [28], [29], not only for the mean and standard deviation values, but also for the correlation between nMOS and pMOS transistors data. These statistical models are available in the design kits provided by TSMC. The process variations (D2D and WID variations) are included in the transistor design kit and declared by TSMC to be Silicon verified. In this design kit, several process parameters are treated as variants such as the threshold voltage, mobility, drain-to-source resistance, Drain-induced-barrier-lowering (DIBL) coefficient, all junction capacitances, and doping concentration. For example, the threshold voltage, V_t, is varied within the $\pm 3\sigma$ design space with standard deviation to mean ratio, $(\sigma/\mu)_{Vt} \approx 12\%$. Also, in this design kit, the WID variations (mismatch effect) are modeled as inversely proportional to the transistor area (WL) [30]. These statistical models are used in all the following Monte Carlo simulations.

A typical histogram of the OR gate high-to-low delay at node G is shown in Fig. 12(a). The standard deviation of this delay, σ, is 58.5 ps. Accordingly, the required negative capacitance value, $\mathrm{C_{NEG}}$, for a timing yield $\mathrm{Y}_o = 99.87\%$ (i.e., "n" $= 3.0$) is obtained from (17) and equals -4.4 fF. Then, the values of A'_o and σ' are calculated as 308.2 ps and 41.6 ps, respectively. This negative capacitance is implemented by using the three proposed negative capacitance circuits in Section III (i.e., DA-NC, CC-NC, and B-NC circuits) as follows. In the following, post layout SPICE transient and Monte Carlo simulations of the OR gate circuit alone and the OR gate with the negative capacitance circuits (DA-NC, CC-NC, and B-NC) connected to node G, are conducted to calculate the delay, the delay variability, and the power consumption overhead.

The adoption of the negative capacitance circuits to the dynamic wide fan-in OR gate is utilized for timing yield improvement of the high-to-low delay at node G. However, the precharge delay (low-to-high delay at node G) is also affected by the negative capacitance circuit adoption. Therefore, the DA-NC and the B-NC circuits are disabled during the precharge phase by adding a tail nMOS transistor driven by the clock signal (This is because the Miller based negative capacitance circuit realizes a positive capacitance when the voltage at node G is rising from 0 to $V_{DD_L}/2$). This results in a slight increase of the precharge delay by 4% and 6% (i.e., the precharge delay increases from 93 ps to 97 ps and 99 ps) due to the DA-NC and the B-NC circuits, respectively. The power and area overheads of these circuits are calculated including this tail transistor. The CC-NC circuit does not suffer from this problem and results in reducing the precharge delay by 15% (i.e., the precharge delay decreases from 93 ps to 81 ps). This is because the CC-NC realizes a negative capacitance when the voltage at node G is falling from V_{DD_L} to 0 or rising from 0 to V_{DD_L}.

A. DA-NC Circuit

The differential-pair based negative capacitance (DA-NC) circuit in Fig. 7 is adopted to implement the required negative capacitance of -4.4 fF. The input capacitance of the DA-NC circuit, C_{M1}, is calculated from the layout by using the CALIBRE tool provided by Mentor Graphics and equals 0.5 fF (this means that the actual negative capacitance to be implemented is -4.9 fF to compensate for C_{M1}). The feedback capacitance, C_F, is implemented by using a metal-insulator-metal capacitor (MIM-CAP), provided by TSMC. The value of C_F is chosen to be 4.9 fF, with an area of 1.96 μm^2. Accordingly, the required amplifier gain, A, is 2.0. The differential amplifier is designed with $V_{\mathrm{DD}} = 0.8$ V, $V_{\mathrm{SS}} = 0$ V, $V_{\mathrm{BIAS1}} = 0.43$ V, and $I_{\mathrm{BIAS1}} = 25$ μA.

The amplifier bandwidth, over which the gain, A, is independent of frequency, is calculated to be 3.4 GHz which is sufficiently larger than the NOR gate maximum operating frequency of 2.5 GHz (this maximum operating frequency is calculated

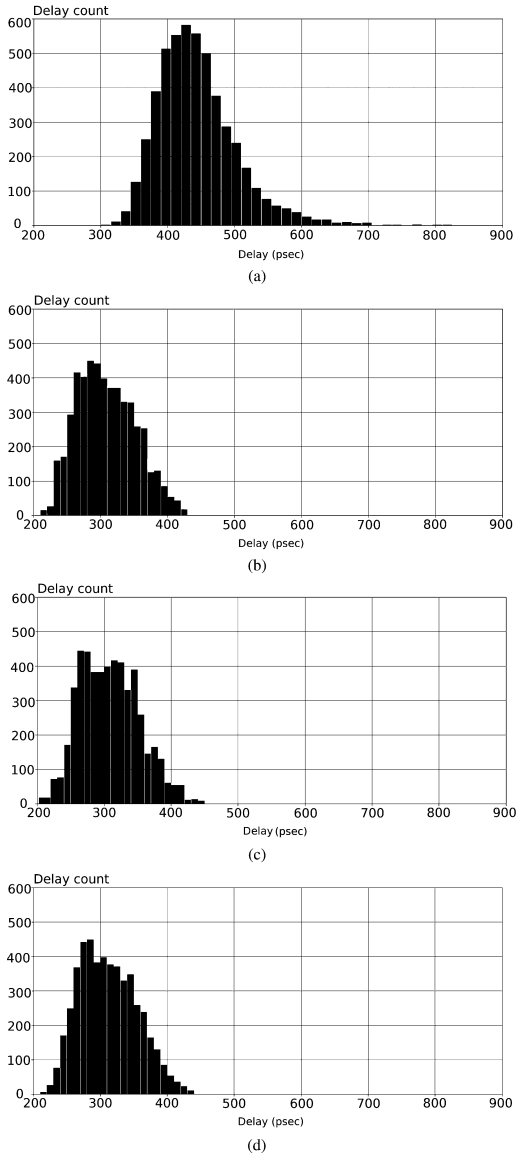

Fig. 12. Delay histograms for the 64-input dynamic OR gate using the 5 000 points Monte Carlo analysis. (a) Before employing the negative capacitance ($\mu = 433$ ps and $\sigma = 58.5$ ps). (b) After employing the DA-NC circuit ($\mu = 315.7$ ps and $\sigma = 43.6$ ps). (c) After employing the CC-NC circuit ($\mu = 310$ ps and $\sigma = 44.9$ ps), and (d) After employing the B-NC circuit ($\mu = 312.5$ ps and $\sigma = 43.9$ ps).

based on a high-to-low delay of 308.2 ps and a precharge delay of 93.5 ps). It should be noted that if the amplifier gain $\mathrm{A} = 3.0$, for instance, the amplifier bandwidth becomes less than 2.5 GHz and the NOR gate delay is not reduced as expected by adopting the negative capacitance circuit.

From (2), the negative capacitance variability is given by

$$\frac{\Delta C_{\mathrm{NEG}}}{C_{\mathrm{NEG}}} = \frac{\Delta C_F}{C_F} + \frac{\Delta A}{A-1}. \tag{20}$$

Thus, the standard deviation of C_{NEG} is given by [26]

$$\left(\frac{\sigma_{C_{\mathrm{NEG}}}}{C_{\mathrm{NEG}}}\right)^2 = \left(\frac{\sigma_{C_F}}{C_F}\right)^2 + \frac{(\sigma_A/A)^2}{((A-1)/A)^2}. \tag{21}$$

Monte Carlo simulation results reveal that the ratio between the amplifier gain A standard deviation to its mean value equals 3.2%. The feedback capacitance, C_F, relative variability is provided by TSMC to be 9.6%. According to (21), the relative variations of $\mathrm{C}_{\mathrm{NEG}}$ equals 11.5%. The ratio of σ'/A'_o is calculated from (19) and equals 14.3% whereas if the negative capacitance variability contribution (the second term in (19)) is ignored, the ratio of σ'/A'_o equals 13.5% (this value is obtained by calculating $\sigma/A_o = 58.5$ ps/433 ps). Accordingly, the negative capacitance variations is ignored in this negative capacitance implementation and (17) is applied because the error in σ'/A'_o when the negative capacitance variability contribution is ignored equals 5.6% (i.e., $(14.3 - 13.5)/14.3$) and also because the resulting timing yield is larger than the target yield of 99.87%.

A typical histogram of the OR gate high-to-low delay at node G is shown in Fig. 12(b). It is evident from Fig. 12(a) and (b) that the DA-NC circuit shifts the delay pdf as required. Fig. 12(b) indicates that 100% of the dynamic circuits samples have delays less than the target delay of 433 ps. Moreover, it is found that the power dissipation is reduced from 62.8 μW to 60.4 μW (3.8% power reduction). This power reduction occurs because reducing the output capacitance results in reducing the dynamic power. In addition, the adoption of the negative capacitance reduces the delay standard deviation from 58.5 ps to 43.6 ps (25.5% variability reduction). The DA-NC circuit exhibits a total average power consumption of 58.3 μW, including the biasing circuit power consumption. The total power dissipation of the OR gate with the negative capacitance circuit is 118.7 μW and the total layout area equals 239.9 $\mu\mathrm{m}^2$.

B. CC-NC Circuit

The CCII+ based negative capacitance (CC-NC) circuit in Fig. 8 is utilized to implement the required negative capacitance of -4.4 fF. The input capacitance of the CC-NC circuit, C_Y, is calculated from the layout by using the CALIBRE tool provided by Mentor Graphics and equals 1.2 fF (this means that the actual negative capacitance to be implemented is -5.6 fF to compensate for C_Y).

In order to design the CCII+ bandwidth sufficiently larger than the OR gate maximum operating frequency of 2.5 GHz, the factor $\beta \approx 0.86$. Accordingly, the load capacitance $\mathrm{C}_L = 6.5$ fF implemented by using a metal-insulator-metal capacitor (MIM-CAP), provided by TSMC, with an area of 2.7 $\mu\mathrm{m}^2$. Following that, the CCII+ circuit is designed by using $\mathrm{V_{DD}} = 0.8$ V, $\mathrm{V_{SS}} = 0$ V, and $\mathrm{I_{BIAS2}} = 20$ μA.

From (3), the negative capacitance variability is given by

$$\frac{\Delta C_{\mathrm{NEG}}}{C_{\mathrm{NEG}}} = -\frac{\Delta C_L}{C_L} - \frac{\Delta \beta}{\beta}. \tag{22}$$

Thus, the standard deviation of C_{NEG} is given by [26]

$$\left(\frac{\sigma_{C_{\mathrm{NEG}}}}{C_{\mathrm{NEG}}}\right)^2 = \left(\frac{\sigma_{C_L}}{C_L}\right)^2 + \left(\frac{\sigma_\beta}{\beta}\right)^2. \tag{23}$$

Monte Carlo simulation results reveal that the ratio between the factor β standard deviation to its mean value equals 9.2%. The load capacitance, C_L, relative variability is provided by TSMC to be 9.6%. Accordingly, the relative variations of $\mathrm{C}_{\mathrm{NEG}}$ equals 13.3%. The ratio of σ'/A'_o is calculated from (19) and equals 14.6% whereas if the negative capacitance variability contribution is ignored, the ratio of σ'/A'_o equals 13.5%. Accordingly, the negative capacitance variations is ignored in this negative capacitance implementation and (17) is applied because the error in σ'/A'_o when the negative capacitance variability contribution is ignored equals 7.5% (i.e., $(14.6 - 13.5)/14.6$) and also because the resulting timing yield is larger than the target yield of 99.87%.

A typical histogram of the OR gate high-to-low delay at node G is shown in Fig. 12(c). It is evident from Fig. 12(c) and (a) that the CC-NC circuit shifts the delay pdf as required. Fig. 12(c) shows that 99.88% of the dynamic circuits samples have delays less than the target delay of 433 ps. Moreover, it is found that the power dissipation is reduced from 62.8 μW to 57.6 μW (8.3% power reduction). In addition, the delay standard deviation is reduced from 58.5 ps to 45 ps (23% variability reduction). The CC-NC circuit exhibits a total average power consumption of 118.6 μW. This power consumption is larger than that of the DA-NC circuit. The total power dissipation of the OR gate with the negative capacitance circuit is 176.2 μW and the total layout area equals 299.2 $\mu\mathrm{m}^2$.

C. B-NC Circuit

The two-inverters buffer based negative capacitance (B-NC) circuit shown in Fig. 9 is employed to implement the required negative capacitance of -4.4 fF. The B-NC is designed with high-V_t transistors ($V_{tn} = 0.49$ V and $|V_{tp}| = 0.54$ V as provided by TSMC 65 nm CMOS technology transistor model files), the ratio $r = 10$, and accordingly, $V_{DD_H} = 1.37$ V by using (10). The value of α is calculated by fitting the $\mathrm{Log\,I}_D$-$\mathrm{Log\,V}_{GS}$ characteristics to the alpha-power model and equals 1.25. The post layout SPICE DC simulations reveal that $V_{IL} = 0.71$ V and $A_{b_{\max}} = 32$. The value of the buffer input capacitance, C_{inv}, is calculated by using the layout parasitic extraction CALIBRE tool and equals 0.96 fF. Thus, in order to achieve a negative capacitance $C_{\mathrm{NEG}} = -4.4$ fF, the value of $C_F = 2.1$ fF by recalling (7). This feedback capacitance is implemented by using a metal-insulator-metal capacitor (MIM-CAP), provided by TSMC with an area of 0.9 $\mu\mathrm{m}^2$.

The transient response of the buffer circuit is measured by using post layout transient simulations and it is found that the decaying slope of the buffer circuit output waveform around

$V_{DD_H}/2$ equals -3.7 V/nsec whereas the decaying slope of the NOR gate output waveform around $V_{DD_L}/2$ equals -1.2 V/nsec. Accordingly, the speed of the buffer circuit is faster than that of the NOR gate to ensure that (2) can be applied.

From (7), the B-NC negative capacitance is expressed as

$$C_{\mathrm{NEG}} = C_{\mathrm{inv}} + C_F\,\theta \quad \text{where } \theta = 1 + A_{b_{\max}}\left(\frac{V_{IL}}{V_{DD_L}} - 1\right). \quad (24)$$

Thus, from (24), the negative capacitance variability is given by

$$\frac{\Delta C_{\mathrm{NEG}}}{C_{\mathrm{NEG}}} = \frac{C_{\mathrm{NEG}} - C_{\mathrm{inv}}}{C_{\mathrm{NEG}}}\left(\frac{\Delta C_F}{C_F} + \frac{\Delta\theta}{\theta}\right). \quad (25)$$

Thus, the standard deviation of C_{NEG} is given by [26]

$$\left(\frac{\sigma_{C_{\mathrm{NEG}}}}{C_{\mathrm{NEG}}}\right)^2 = \left(\frac{C_{\mathrm{NEG}} - C_{\mathrm{inv}}}{C_{\mathrm{NEG}}}\right)^2\left[\left(\frac{\sigma_{C_F}}{C_F}\right)^2 + \left(\frac{\sigma_\theta}{\theta}\right)^2\right]. \quad (26)$$

Monte Carlo simulation results reveal that the ratio between the factor θ standard deviation to its mean value equals 6.9%. The feedback capacitance, C_F, relative variability is provided by TSMC to be 9.6%. Accordingly, the relative variations of C_{NEG} equals 14.4%. The ratio of σ'/A'_o is calculated from (19) and equals 14.8% whereas if the negative capacitance variability contribution is ignored, the ratio of σ'/A'_o equals 13.5%. Accordingly, the negative capacitance variations is ignored in this negative capacitance implementation and (17) is applied because the error in σ'/A'_o when the negative capacitance variability contribution is ignored equals 8.8% (i.e., $(14.8-13.5)/14.8$) and also because the resulting timing yield is larger than the target yield of 99.87%.

A typical histogram of the OR gate high-to-low delay at node G is shown in Fig. 12(d). It is evident from Fig. 12(d) and (a) that the B-NC circuit shifts the delay pdf as required. Fig. 12(d) signifies that 99.94% of the dynamic circuits samples have delays less than the target delay of 433 ps. Moreover, it is found that the power dissipation is reduced from 62.8 μW to 59 μW (6.1% power reduction). In addition, the delay standard deviation is reduced from 58.5 ps to 43.9 ps (25% variability reduction). The B-NC circuit exhibits a total average power consumption of 16.9 μW. This power consumption is smaller than that of the DA-NC and the CC-NC circuits by factors of 3.5X and 7X, respectively. The total power dissipation of the OR gate with the negative capacitance circuit is 75.2 μW and the total layout area equals 169.1 μm^2.

The wide fan-in dynamic OR gate suffers from high noise sensitivity due to the subthreshold leakage current flowing through the evaluation pull down network [31] which increases with technology scaling. Accordingly, noise immunity has become a great concern, especially, in the design of wide fan-in gates. This makes it necessary to discuss the effect of the proposed negative capacitance circuits on the dynamic OR gate noise immunity. According to [31]–[33], the noise immunity is quantified by using the unity noise gain (UNG) metric. The UNG is defined as the amplitude of input noise V_{noise} that causes an equal amplitude noise pulse at the OR gate output node F (i.e., UNG $= V_{\mathrm{noise}}$ such that $V_{\mathrm{noise}} = V_F$). UNG captures the critical input noise strength, as any noise pulse larger than UNG is amplified due to the nonlinear behavior of the transistor [33]. Thus, all the inputs X1–X64 are driven by noise pulses with the same duration of 100 ps [32] and varying amplitude. The pulse amplitude is swept till a glitch, with the same amplitude of the inputs, occurs at the output node F.

Post layout simulation results show that the UNG of the OR gate without the negative capacitance adoption equals 466 mV whereas the adoption of the DA-NC, CC-NC, and B-NC reduces the UNG value to 444 mV, 435 mV, and 449 mV, respectively. Accordingly, the adoption of the negative capacitance circuit results in slightly reducing the OR gate noise immunity.

The simulation results for the three negative capacitance circuits are tabulated in Table I. The following observations are extracted from Table I.

1) All the three negative capacitance circuits achieve higher yield values than the target yield of 99.87% for both the delay at node G and node F constraints. The delay histograms at node F are not shown, since they exhibit similar results to the ones in Fig. 12. In addition, the adoption of the DA-NC, CC-NC, and B-NC circuits reduces the OR gate delay variability at node G by 25.5%, 23%, and 25%, respectively. Also, at node F, the adoption of the DA-NC, CC-NC, and B-NC circuits reduces the OR gate delay variability by 23%, 20%, and 26%, respectively. The delay standard deviations at node F are less than those at node G due to the averaging effect. This averaging effect results in averaging and reducing the random variations through the output OR gate inverter.
2) The adoption of the DA-NC, CC-NC, and B-NC circuits results in reducing the OR gate power by 3.8%, 8.3%, and 6.1%, respectively. However, the negative capacitance circuit itself dissipates power. The B-NC circuit power dissipation is less than that of the DA-NC and the CC-NC by factors of 3.5X and 7X, respectively. The total power of the OR gate with the DA-NC, CC-NC, and B-NC circuits adopted equals 118.7 μW, 176.2 μW, and 75.9 μW, respectively. Also, the associated power overheads of the DA-NC, CC-NC, and B-NC circuits are 55.9 μW, 113.4 μW, and 13.1 μW, respectively (by subtracting power dissipation of the OR gate without the negative capacitance circuit adoption from the total power dissipation of the OR gate with the negative capacitance circuit adopted).
3) The OR gate power standard deviation increases with the adoption of the negative capacitance circuit. This increase is 13%, 9.7%, and 9.7% for the DA-NC, CC-NC, and B-NC circuits, respectively.
4) The best negative capacitance circuit is the B-NC circuit, as long as the technology supports the dual supply voltage (dual-V_{DD}) and the dual threshold voltage (dual-V_t) requirements. This circuit dissipates the lowest power consumption and utilizes the smallest added capacitance (2.1 fF).
5) If the dual-V_t and the dual-V_{DD} are not supported by the CMOS technology, the second candidate is the DA-NC circuit, because it exhibits less power dissipation and added

TABLE I
POST LAYOUT SIMULATION RESULTS FOR THE DYNAMIC 64-INPUT OR GATE WITHOUT C_{NEG} AND WITH DA-NC, CC-NC, AND B-NC CIRCUITS ADOPTED. SIMULATIONS ARE PERFORMED AT A TEMPERATURE $\mathrm{T} = 120°\mathrm{C}$ (WORST CASE DELAY)

	Without C_{NEG}	**With C_{NEG}**		
		DA-NC	**CC-NC**	**B-NC**
Node G delay				
μ **(psec)**	433	315.7	310	312.5
σ **(psec)**	58.5	43.6	44.9	43.9
σ/μ **(%)**	13.5	13.8	14.5	14
Node F delay				
μ **(psec)**	442.2	326.9	324.3	320
σ **(psec)**	53.6	41.2	42.7	39.6
σ/μ **(%)**	12.1	12.6	13.2	12.4
OR gate power				
μ **(μW)**	62.8	60.4	57.6	59
σ **(μW))**	3.9	4.4	3.9	4
σ/μ **(%)**	6.2	7.0	6.8	6.8
C_{NEG} **power**				
μ **(μW)**		58.3	118.6	16.9
σ **(μW))**		2.8	5.7	1.5
σ/μ **(%)**		5	4.8	8.9
Total Power (μW)	62.8	118.7	176.2	75.9
Total Area (μm^2)	135.8	239.9	299.2	169.1
UNG (mV)	466	444	435	449
Capacitance added (fF)		4.9	6.5	2.1
Technology Considerations				Dual-V_{DD} Dual-V_t

capacitance than that of the CC-NC. If the OR gate frequency is high such that the B-NC and DA-NC circuits speeds are not faster than the OR gate speed, the CC-NC is the best choice, because it is not prone to the gain-bandwidth product limitation at the expense of higher power dissipation and added capacitance value than those of the DA-NC and the B-NC circuits.

VI. CONCLUSION

In this paper, three novel negative capacitance circuits are developed to reduce the effects of process variations on dynamic circuits. These circuits are DA-NC, CC-NC, and B-NC. Post layout simulation results, referring to an industrial hardware-calibrated TSMC 65 nm CMOS technology, show that the adoption of these negative capacitance circuits results in improving the timing yield to values larger than 99.87% by reducing the delay mean and variability. The recommended negative capacitance circuit is the B-NC circuit when the technology supports the dual supply voltage (dual-V_{DD}) and the dual threshold voltage (dual-V_t) requirements. This circuit dissipates the lowest power consumption and utilizes the smallest added capacitance. If the dual-V_t and the dual-V_{DD} are not supported by the CMOS technology, the second candidate is the DA-NC circuit, because it exhibits less power dissipation and added capacitance than that of the CC-NC. If the OR gate frequency is high such that the B-NC and DA-NC circuits speeds are not faster than the OR gate speed, the CC-NC is the best choice, because it is not prone to the gain-bandwidth product limitation at the expense of higher power dissipation and added capacitance value than those of the DA-NC and the B-NC circuits.

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