Comparative Analysis of Process Variation Impact on Flip-Flops Soft Error Rate

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***Abstract*—Due to CMOS technology scaling, devices are getting smaller, faster, and operating at lower supply voltages. The reduced capacitances and power supply voltages and the increased chip density to perform more functionality result in increasing the soft errors and making them one of the essential design constraints at the same level as delay and power. Even though the impact of process variations on the performance and the power consumption has been investigated by many researchers, its impact on soft errors has not been paid enough attention. This impact is investigated in this paper for 65-nm CMOS technology. The soft error yield is defined in this paper similar to the timing yield and the power yield. This paper shows that the soft error yield of the sense-amplifier based flip flop (SA-FF) is very poor. Therefore, soft error mitigation techniques are required when using this flip-flop topology. The semi-dynamic flip-flop (SDFF) exhibits the best soft error yield behavior with a very high performance at the expense of large power requirement. Finally, some design insights are proposed to guide flip-flops designers to select the best flip-flop topology that satisfies their specific circuit soft error rate constraints.**

I. Introduction

Reliability is one of the major design challenges for sub-micron CMOS technology. Shrinking geometries, lower supply voltages, higher clock frequencies, and higher density circuits all have a great impact on reliability [1-7]. As CMOS technology further scales, soft errors become one of the major reliability concerns. Soft errors result when energy particles hit a silicon substrate, the kinetic energy of the particle generates electron-hole pairs as they pass through the p-n junctions. Some of the collected charges will recombine to form a very short duration current pulse that disturbs the struck node voltage and can lead to soft errors [2]. In memory elements, this disturbance can cause bit flips (0-to-1 flip or 1-to-0 flip) which may corrupt the logic state of the circuit. However, in combinational circuits it may cause a temporary change in the output node voltage. This temporary change may be tolerated, unless it is latched by a succeeding memory element. For memory elements such as Static Random Access Memory (SRAM) and flip-fops, if the charge collected ($Q_{collected}$) by the particle strike at the storage node is more than a minimum value, the node is flipped and a soft error occurs. This minimum value is called a critical charge ($Q_{critical}$) which can be used as a measure of memory element vulnerability to soft errors [2,5,7-10].

Soft errors are mitigated in background memories such as SRAM cells by providing error correction techniques. However, these techniques can not be used with flip-flops. In addition, the demand for higher performance has moved the clock frequencies up to multi-GHz in microprocessors and other advanced applications. These increased clock frequencies increase the probability that a flip-flop will latch on to an error since this latching occurs at each clock edge. Furthermore, The increased clock frequencies lead to a very deep pipelining which means that hundreds of thousands of flip-flops are required to control the data flow. Hence, soft errors in flip-flops may result in latching incorrect data causing the overall system to malfunction [11]. Therefore, analysis of soft errors vulnerability on different flip-flops topologies is of paramount importance.

Process variation is another design challenge for CMOS technology scaling. The device parameters, such as threshold voltage, channel length, oxide thickness, and mobility, will have large statistical process variations [12-16]. The process variations can be classified as die-to-die (inter-die) variations or within-die (intra-die) variations. In die-to-die variations, all devices on the same die are assumed to have the same parameters. However, devices on the same die are assumed to behave differently for within-die variations [12]. Although die-to-die variations were originally considered as the main source of process variations, within-die variations have now become the major design challenge as technology scales [14,15].

The impact of process variation on soft errors is investigated in [1]. Unfortunately, the work in [1] uses worst case analysis which leads to completely pessimistic and misleading results. The work in [17] attempts to remedy the worst case analysis used in [1] by using Monte Carlo analysis. However, no comparative analysis of the impact of process variation on soft errors vulnerability among different flip-flops topologies is provided. This comparative analysis, when performed, will provide flip-flops designers beneficial design insights on selecting the most reliable flip-flop topology while taking the process variations impact into account. In addition, only the threshold voltage and gate length variations are considered in [17] ignoring other process variation parameters. In this paper, a comparative analysis of process variations impact on flip-flops soft error vulnerability is introduced. The process variations of all device parameters, such as threshold voltage, channel length, oxide thickness, and mobility, are considered.

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The paper is organized as follows: Section II describes the flip-flops selection criterion, the simulation setup, and the soft error yield definition. Simulation results accompanied with the design insights are given in section III. Finally, some conclusions are drawn in section IV.

II. Simulation Setup

A. Flip-Flops Selection

Four different flip-flops are selected to represent the various trade-off choices between performance and power dissipation [11]. Figures 1 and 2 depict the transmission-gate master-slave flip-flop (TG-MSFF) and the modified clocked CMOS master-slave flip-flop (M-C^{2}MOS-MSFF), respectively. Both of them are implemented by cascading two complementary latches. This master-slave implementation results in robust flip-flop with a good hold time behavior. Moreover, they are used in standard libraries [11] which makes it so important to include them in this comparison.

Figure 3 shows one of the fastest flip-flops, a semi-dynamic flip-flop (SD-FF) [18]. This flip-flop can be considered as a pulsed latch, since it samples the input data to the flip-flop output during a very short transparency period around the clock sampling edge. Accordingly, the input data can arrive after the clock edge. Therefore, this flip-flop is used in high performance VLSI applications due to its relatively short data-to-output delay at the expense of a poor hold time behavior and an excessive power consumption. Figure 4 denotes a sense-amplifier based flip-flop (SA-FF) with a NAND SR-latch [19]. This flip-flop can be viewed as a compromise between the master-slave robustness and the pulsed latches high performance.

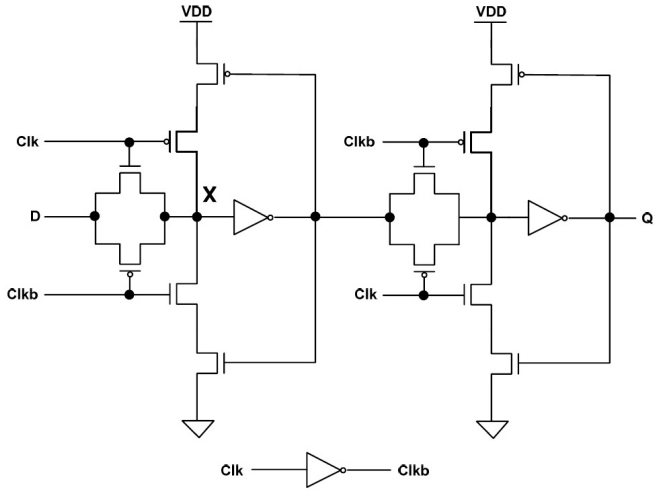

Fig. 1. The Transmission Gate based Master-Slave Flip-Flop (TG-MSFF)

B. Optimum Power Delay Product (PDP)

All flip-flops are optimized for minimum PDP using a STMicroelectronics 65-nm CMOS technology transistor model, a 1V power supply voltage, a typical process corner, a clock frequency of 1 GHz and pseudorandom input data

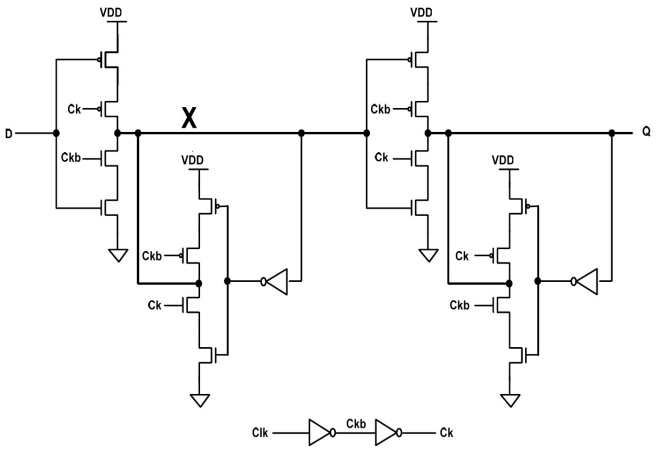

Fig. 2. The Modified Clocked CMOS Master-Slave Flip-Flop (M-C^{2}MOS-MSFF)

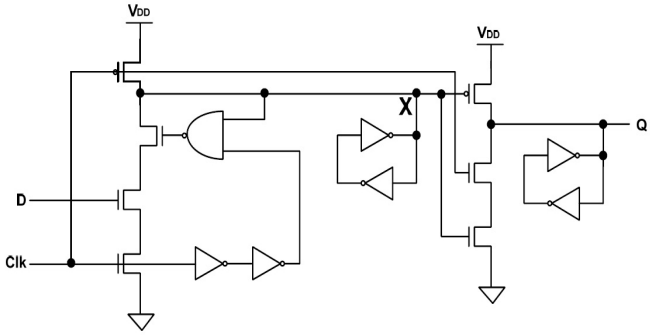

Fig. 3. The Pulsed Semi-Dynamic Flip-Flop (SD-FF)

with 50% data activity [20]. The measured PDP is obtained by multiplying the data-to-output delay, and the total power consumption which includes both internal power dissipation and the local clock/data power dissipation [20]. The optimum setup time for each flip-flop is determined to achieve minimum PDP. The optimization process is conducted by using the CFSQP (C Version Feasible Sequential Quadratic Programming) optimization technique, implemented in Spectre-RF. This algorithm is based on the finite difference perturbation (FDP) method to determine how sensitive the PDP is to each device size. Then, the algorithm provides the optimal sizing and setup time to achieve the minimum PDP.

C. Functional Yield Improvement using Setup Time Margin

Monte Carlo analysis, including the mismatch between transistors is performed on the flip-flops at the optimal PDP point. An industrial hardware-calibrated statistical STMicroelectronics 65-nm CMOS transistor model is used in this Monte Carlo analysis. In this model, the transistor parameters such as the threshold voltage and the channel length are modeled by a normal distribution within the $\pm 3\sigma$ design space. The number of Monte Carlo analysis points used is 5000 points to provide a good accuracy.

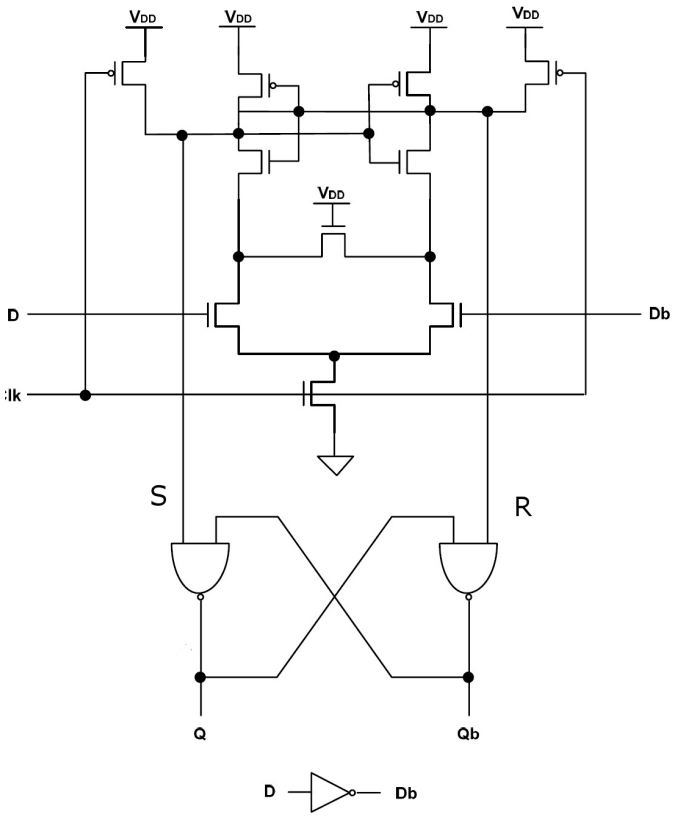

Fig. 4. The Sense-Amplifier based Flip-Flop (SA-FF)

In the PDP optimization process, the optimum setup time is obtained using a typical process corner to minimize the PDP. This results in a poor functional yield, since the setup time constraint of some of the flip-flops simulated Monte Carlo points will be violated. Typically, the functional yield of the flip flops with this setup time ranges from 85% to 95%. A setup time margin is added to achieve a functional yield greater than 99.9% [11]. This setup time margin is determined by sweeping the setup time and calculating the functional yield and the mean data-to-output delay. The setup time that achieves a functional yield greater than 99.9% and minimum data-to-output delay is selected.

D. Soft Error Modeling

The Soft error rate (SER) can be calculated by using the following equation which describes the relationship between the SER and $Q_{critical}$ [8,21].

$$SER \ \alpha \ N_{flux} \times CS \times \exp(-Q_{critical}/Q_s) \tag{1}$$

where N_{flux} refers to the intensity of the neutron flux, CS is the cross section area of the node, and Q_s is the charge collection efficiency which strongly depends on doping [22]. Therefore, $Q_{critical}$ can be modeled as a measure of the SER for different flip-flops topologies. Since the recombination of the collected charges results in a very short duration current pulse which might cause soft error. This current pulse can be approximated by the following equation [22]:

$$I(t) = I_{peak} \times [\exp(-t/\tau_a) - \exp(-t/\tau_b)] \tag{2}$$

where I_{peak} represents the current pulse amplitude, τ_a is the collection time constant, and τ_b is the ion-track establishment time constant.

In this paper, the particle strike is modeled as a current source connected to the flip-flop circuit nodes. The parameters τ_a and τ_b equals 200ps and 10ps respectively. I_{peak} is varied iteratively to achieve the minimum amount of charge, $Q_{critical}$, which results in a bit flip at the output node. Hence, $Q_{critical}$ can be given by:

$$Q_{critical} = minimum[\int_0^{t_f} I(t)dt] \tag{3}$$

where t_f refers to the flipping time of the output node and I(t) is the current pulse model given in equation (2). The critical charge is calculated at all nodes of each flip-flop for the 1-to-0 flip and the 0-to-1 flip at the output node. Then, the node that has the smallest critical charge is selected as the most susceptible node to soft errors. Following that, the same Monte Carlo setup mentioned in subsection II.C is conducted, and the critical charge distribution is obtained.

E. Soft Error Yield

The process variation impact allows some flip-flops samples to have critical charge values larger than the nominal value, and other flip-flops samples to have smaller values. Although the flip-flops with larger critical charge values are less vulnerable to soft errors, the flip-flops with smaller values will be negatively impacted by the process variations. This is similar to the delay variability due to process variations, as some samples will have less delay than the nominal delay (which is desirable) and other samples will have more delay which may violate the timing constraint. Hence, the soft error yield can be defined in a similar manner as the timing yield. By using the critical charge distribution obtained in the previous subsection, and at a given collected charge $Q_{collected}$, the probability of flipping can be computed by using Figure 5 as follows:

$$Probability\ of\ flipping = \int_0^{Q_{collected}} f(Q_{critical})dQ_{critical} \tag{4}$$

Then, the soft error yield is given by:

$$\begin{aligned} &Soft\ \ error\ \ yield \\ &= \quad 1 - \int_0^{Q_{collected}} f(Q_{critical})dQ_{critical} \end{aligned} \tag{5}$$

III. Simulation Results and Discussions

A. Nominal Critical Charge

Table 1 summarizes the nominal critical charge values and the corresponding nodes for the 1-to-0 and the 0-to-1 flips for the selected flip-flops. It should be noted that the SA-FF critical charge has to be determined for the two nodes S and R because node R is more susceptible to soft errors in case of

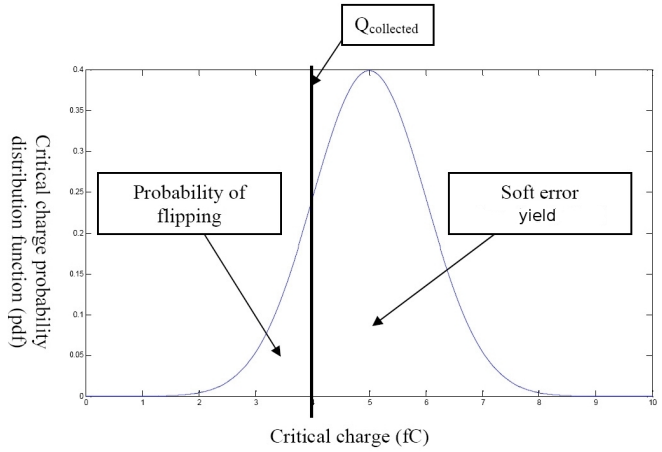

Fig. 5. The critical charge probability distribution function and the soft error yield definition.

a 1-to-0 flip while node S is more susceptible to soft errors in case of a 0-to-1 flip.

According to results in Table 1, the least vulnerable flip-flop to soft errors is the SD-FF. Its critical charge is 30X and 6X higher than that of the SA-FF for the 1-to-0 flip and the 0-to-1 flip respectively. This advantage is due to its cross coupled inverters connected at node X which fight to keep this node at its logic state. Moreover, this pulsed flip-flop latches its input to its output during the transparency period which comes after the clock edge at which the particle strike current pulse model is injected. The SA-FF exhibits the smallest $Q_{critical}$ due to the SR latch since any error occurs at nodes S or R results in flipping the output node state immediately. Therefore, this flip-flop has a very small flipping time (t_f).

The master-slave flip-flops exhibit roughly the same critical charge nominal value which lies half-way between the SD-FF and the SA-FF critical charge values. The master-slave flip-flops exhibit a long flipping time, since, the error at node X in both master-slave based flip-flops takes longer time to propagate to the output node. In addition, node X will be in the hold mode, when it is connected to the back to back inverters, which reduces its susceptibility to soft errors. Figure 6 shows the critical charge of all the flip-flops relative to the critical charge of the SA-FF.

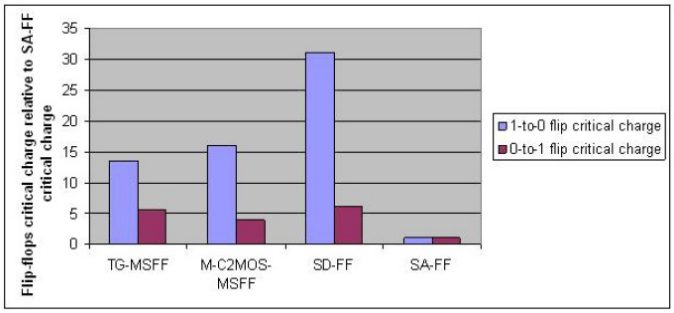

Fig. 6. The critical charge of the selected flip-flops relative to that of the SA-FF flip flop

Table 1: The nominal critical charge values for different flip-flops

	TG-MSFF	M-C^{2}MOS-MSFF	SD-FF	SA-FF	
Most susceptible node	X	X	X	S	R
$Q_{critical}$(fC) (1-to-0 flip)	2.91	3.51	6.70	0.72	0.22
$Q_{critical}$(fC) (0-to-1 flip)	3.94	3.15	4.35	0.71	1.85

B. Critical Charge Distribution

The critical charge distributions for the selected flip-flops are tabulated in Table 2. It is shown that the TG-MSFF exhibits small critical charge variations for both the 1-to-0 and the 0-to-1 flips. The reason for these small variations in the TG-MSFF is that the soft error occurs at node X, takes longer path to affect the output node (this long path consists of two inverters and a transmission gate). This long path exhibits more averaging effect which results in more cancelation of random variations. Correspondingly, this flip-flop has small critical charge variations. The SA-FF suffers from higher critical charge variations which are 2.5X and 3.6X higher than that of the TG-MSFF for the 1-to-0 flip and the 0-to-1 flip respectively. There are two main reasons for these higher variations. The first reason is due to the differential architecture used in the SA-FF which suffers from transistors mismatch variations (within die variations). The second reason is the short path from nodes S or R to the output node which has small averaging effect. The SD-FF has critical charge variations for the 1-to-0 flip which is 4.4X higher compared to its 0-to-1 flip variations. This large difference between the 1-to-0 and 0-to-1 flips is due to the pre-charge performed at node X. This pre-charge results in holding this node at logic '1' and, hence, reduces the variations effect when flipping this node from state '1' to state '0'. This yields small variations for the output in the case of a 0-to-1 flip, since the output node is the invert of node X.

Table 2: The critical charge mean and percentage standard deviation of the selected flip-flops considering process variations

		TG-MSFF	M-C^{2}MOS-MSFF	SD-FF	SA-FF	
					S	R
$Q_{critical}$ (1-to-0 flip)	Mean (fC)	2.93	3.5	5.51	0.65	0.23
	σ(%)	14.6	38.4	24.2	36.9	24.8
$Q_{critical}$ (0-to-1 flip)	Mean (fC)	3.91	3.11	4.36	0.69	1.36
	σ(%)	6.6	16.9	5.5	9.6	24

C. Soft Error Yield

The soft error yield is a good measure of the flip-flop immunity to soft errors. It represents the percentage of flip-flops that will function properly under soft errors. In other words, a soft error yield of 90% means that 10% of the fabricated flip-flops will malfunction due to the impact of process variations on soft errors. Using equation (5), the soft error yield as a function of the collected charge ($Q_{collected}$) is shown in Figures 7 and 8 for the 1-to-0 flip and the 0-to-1 flip respectively. It should be noted that for the SA-FF, the node that has less nominal critical charge is selected for these calculations which is node R for the 1-to-0 flip and node S for the 0-to-1 flip.

For a given value of $Q_{collected}$, the soft error yield can be computed easily from these figures. It is clear that for the 1-to-0 flip case shown in Figure 7, the SD-FF has the highest soft error yield while the SA-FF has the smallest. However, the TG-MSFF and the M-C^{2}MOS-MSFF give different soft error yield depending on the value of $Q_{collected}$. i.e. for $Q_{collected}$ = 2.5 fC, the soft error yield of the TG-MSFF is higher than that of the M-C^{2}MOS-MSFF while for $Q_{collected}$ = 3.5 fC, the soft error yield of the TG-MSFF is smaller than that of the M-C^{2}MOS-MSFF. On the other hand, for the 0-to-1 flip case, the SD-FF has the highest soft error yield. Following the SD-FF, is the TG-MSFF then the M-C^{2}MOS-MSFF and finally the SA-FF has the lowest soft error yield.

D. Design Insights

The discussion above shows that the best choice of flip-flops for soft error yield would be the SD-FF. This flip-flop exhibits a high performance as well at the expense of large power dissipation. If the primary objective is the power budget, master-slave flip-flops are preferred specially the TG-MSFF, since it has smaller critical charge variations than that of the M-C^{2}MOS-MSFF. Finally, the SA-FF has a very poor soft error yield. Since the SA-FF is preferred in differential circuits, soft error mitigation techniques should be applied to improve its soft error yield as introduced in [9,23].

IV. Conclusion

A comparative analysis of soft error yield of different flip-flops topologies is introduced in this paper. The SA-FF is the most vulnerable flip-flop to soft errors and its soft error yield is very poor. The reason for that is due to its small flipping time. The least vulnerable flip-flop to soft errors is SD-FF with critical charge of 30X and 6X higher than that of the SA-FF for the 1-to-0 flip and the 0-to-1 flip respectively. Moreover, the SA-FF has the highest critical charge variations due to its sensitivity to transistor mismatch. This paper recommends that the SD-FF is the best choice for high soft error yield and high performance at the expense of large power. When the major concern is the power budget, master-slave flip-flops are preferred. If the SA-FF has to be used, soft error mitigation techniques should be adopted, since the SA-FF has a very poor soft error yield.

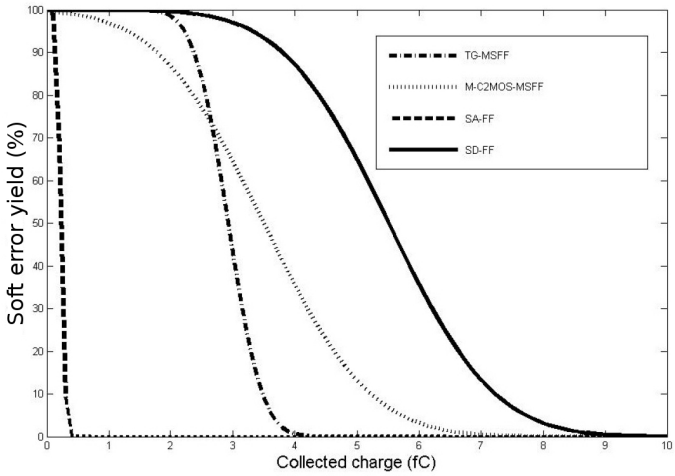

Fig. 7. The soft error yields for the selected flip-flops for 1-to-0 flip

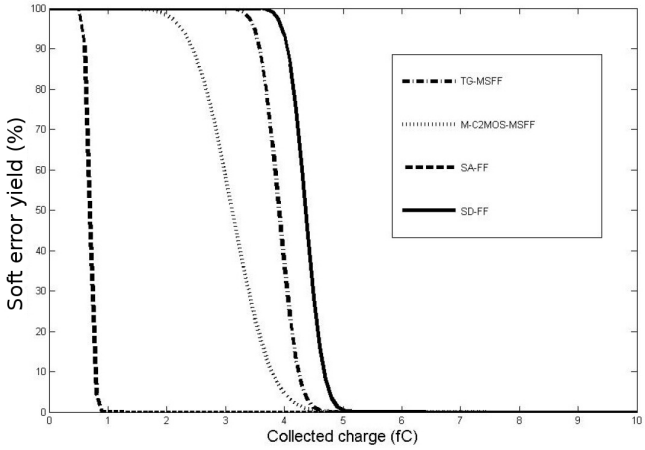

Fig. 8. The soft error yields for the selected flip-flops for 0-to-1 flip

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