Statistical Model for Ring Oscillator Phase Noise Variability Accounting for within-Die Process Variation

Faizal Khalek[1], Hassan Mostafa [2], Mohab Anis [2]
[1]Multimedia University, Malaysia, [2]University of Waterloo, Canada

Abstract

Phase noise is one of the most restricted specifications in oscillators, especially ring oscillators. Phase noise will exhibit large fluctuations around its nominal value due to the increased process variation with technology scaling. These fluctuations will cause some fabricated ring oscillators not to meet the phase noise constraint and, hence, result in yield loss. This yield loss is expected to become worse especially for sub-90-nm technology nodes. In this paper, an analytical model for the phase noise variability in ring oscillators is proposed. The proposed model has been verified using Monte Carlo SPICE simulations for an industrial 65-nm CMOS technology and is found in good agreement. The model shows that for the commonly used differential-pair-based ring oscillators, the main contribution in phase noise variability comes from the differential pair tail transistor. It also shows that the phase noise variability is reduced as the supply voltage increases. These results can be used to mitigate the phase noise variability and improve the yield through proper sizing of the tail transistor or higher supply voltage.

1. Introduction

Phase noise is one of the relevant design parameters for the oscillator design. It is important for the designer to achieve the desired phase noise for the frequency stability. This frequency stability is required in digital circuits for the precision timing specifications. Moreover, it is also important for analog circuits to have small phase noise, i.e. from mixing the unintended frequency. Hence, the phase noise prediction is an important criterion to make sure the designed oscillator phase noise meets the specification.

Process variations are expected to worsen in future technologies due to difficulties with printing nanometer scale geometries using standard lithography. Hence, they are considered another main challenge of CMOS technology scaling [1, 2]. They can be classified into die-to-die (D2D) variations (inter-die) and within-die (WID) variations (intra-die). In D2D variations, all devices on the same die are assumed to have the same parameters values. However, devices on the same die are assumed to behave differently when considering the WID variations [1]. Although D2D variations were originally considered the main source of process variations, WID variations are posing the major design challenge as technology scales. Due to increased process variation in scaled technologies, the device variability will introduce fluctuations to the designed phase noise that will increase as technology scaling continued.

Generally, device variability is predicted by the Monte Carlo simulation. Monte Carlo simulation deals with the transistor statistical variation data to characterize the prediction output. However, Monte Carlo simulation is computationally expensive, time consuming, and non-scalable with technology. Therefore, a proposed statistical model will be developed to estimate the phase noise variation. This model will be a guide for phase noise yield improvement on the circuit level.

There are a few research work targeted the oscillator phase noise variations [3, 4]. Unfortunately, the work in [3] performs Monte Carlo simulations to predict the phase noise variability which gives no design insights to the oscillator designers to reduce this variability. In addition, the work in [4] focuses on the device mobility variations, however, the transistor threshold voltage and channel length variations are the dominant variation sources in sub-micron technologies.

The proposed statistical model in this paper will account mainly for WID variations. The model can be used in variation mitigation techniques at the circuit level. Furthermore, it will provide some design insights to the oscillator designer to improve the phase noise yield. The introduced model will be accurate, simple, and scalable with technology as compared to Monte Carlo simulations. The rest of the paper is organized as follows: in Section 2, the sources of process variation are discussed. Meanwhile, the analytical model derivations and assumptions are presented in Section 3.The analytical results are compared to the Monte Carlo simulations for model justification in Section 4. Finally, a conclusion will be given in Section 5.

2. Process Variations

Device variations tend to be higher on deep submicron technologies due to device size shrinking. The size of transistor determines the threshold voltage fluctuation and it is also contributes to the channel length variation.

The main process variations of the device can be categorized into two; which are random dopant fluctuations (RDF) and channel length variation. The RDF will affect threshold voltage and it is determined by the active area of the transistor. It can be modeled with the Gaussian distribution and its standard deviation can be characterized by

$$\sigma_{Vth,RDF} \propto \frac{k}{\sqrt{WL}} \quad (1)$$

where k is a technology constant, W is a width and L is a channel length.

Meanwhile, the channel length variation is due to the fabrication limitation in deep submicron technologies. In sub-90-nm technology nodes, the standard lithography difficulty in printing small dimensions results in channel length variations [1]. By this channel length variation, the threshold voltage also is affected through charge sharing and drain-

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induced barrier lowering (DIBL) effects. Therefore, the threshold voltage is determined by the negative exponential of the channel length. It can be modeled as [5]

$$V_{th} \approx V_{tho} - (\zeta + \eta V_{DS})e^{-L/\lambda} \quad (2)$$

where V_{tho} is a long channel threshold voltage, ζ is a charge sharing coefficient, η is a DIBL effect coefficient, λ is a characteristic length and L is a channel length.

There are few other device variations such as oxide charge variation, mobility fluctuations, gate oxide thickness variation and channel width variation [5]. However, these variations do not largely contribute to the threshold voltage variation.

Threshold voltage variation contributes to the local area mismatch; hence give certain offset to the prediction value. With this offset, the output could be off from the circuit tolerance and the circuit will be malfunctioned. Therefore, with simple analytical model, the offset can be determined easily and efficiently.

3. Analytical Model Derivation & Assumption

There are many phase noise models published as a guide for the calculation wise [6, 7, 8]. Most of the published models in the literature are either too complex which gives high accuracy or overestimated due to excessive simplifications. However, there is a simple phase noise model and its calculation result is close to the simulation result introduced recently in [8]. This phase noise model will be the base for our analytical model derivation. It should be mentioned that our objective is to estimate the phase noise variability, not the phase noise nominal value which can be obtained from [8]. The phase noises of the oscillator are due to white noise and flicker noise. However for this paper, the flicker noise is not included by assuming constant tuning current. So, the derivation is based on the white noise model as described in [8] as white noise is the dominant noise source of phase noise.

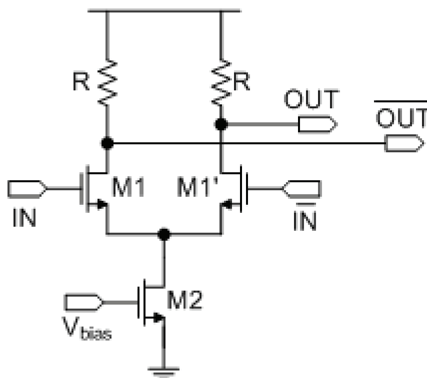

Figure 1: Differential pair delay cell

The ring oscillator consists of a number of differential-pair delay cells as the one shown in Fig. 1. There are three main components of the differential pair delay cell which are loads, differential-pair transistors and tail transistor (current source). Each of these components contributes to the white noise that affects the oscillator. It can be expressed as

$$L(f) = \frac{2kT}{I \ln 2}\left[\gamma\left(\underbrace{\frac{3/4}{V_{effd}}}_{1} + \underbrace{\frac{1}{V_{efft}}}_{2}\right) + \underbrace{\frac{1}{V_{op}}}_{3}\right]\left(\frac{f_o}{f}\right)^2 \quad (3)$$

where k is a Boltzman constant, T is a temperature and γ is a transistor noise factor, I is a current source, V_{effd} is a differential pair overdrive voltage, V_{efft} is a tail transistor overdrive voltage, V_{op} is a output voltage, f_o is a oscillation frequency and f is a offset frequency.

The oscillator current in the Eq. 3 is obtained from the alpha power law [9]. This current can be determined by $I = k(V_{GSt} - V_{th})^{\alpha}$, where k is a technology parameter and α can be determined by fitting the transistor I-V curve to the alpha power law equation.. Meanwhile, V_{effd} is an overdrive voltage of the differential pair and V_{efft} is an overdrive voltage of the tail transistor. Here, we proposed to use overdrive voltage instead of trans-conductance for the variability derivations.

As in Eq. 3, there are few parameters that depend on the threshold voltage. These parameters are the sources of the variation and it will affect phase noise variability prediction. According to [5], the current variation depends on the transistor region where $\Delta I = -g_m \Delta V_{th}$. Therefore, for the tail transistor, it needs to operate in the saturation region (pinch-off or velocity saturation) to minimize current variation. In addition, the phase noise model (Eq. 3) is derived by using alpha power law which is valid for the saturation region [10].

3.1 Derivations

Since the threshold voltage variation is random, the tail variation and differential pair variation are uncorrelated. Therefore, variation for each component can be described independently. The phase noise spread will be characterized by the phase noise standard deviation.

A. The tail transistor variation

The tail transistor is known as a current source of the oscillator circuit. This current determines the total power consumption and contributes to the oscillation frequency. On the other hand, the tail transistor also contributes to the phase noise variation. It is due to the threshold voltage parameter as described in Eq. 3. Therefore, phase noise variation that respect to the tail transistor can be determined by

$$\sigma_{L(tail)} = \frac{\partial L}{\partial Vth_{(tail)}} \sigma_{Vth(tail)} \quad (4)$$

where $\sigma_{Vth(tail)}$ is a tail transistor threshold voltage variation. It shows the variation by the tail transistor is a function of α and overdrive voltage where

$$\sigma_{L(tail)} = f\left[\frac{\alpha}{(Vgs_{(tail)} - Vth_{(tail)})}\right] \quad (5)$$

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B. The differential pair variation

Meanwhile for the differential pair, the variation is

$$\sigma_{L(diff)} = \frac{\partial L}{\partial Vth_{(diff)}} \sigma_{Vth(diff)} \quad (6)$$

where $\sigma_{Vth(diff)}$ is a differential pair threshold voltage variation. This variation is only affected on parameter 1 as in Eq. 3.

C. The passive load variation

Oscillator in Fig. 1 also can be analyzed as differential amplifier to find out the mismatches where both of the inputs are grounded and find out the offset at the output. The offset can be determined by

$$V_{OS,in}^2 = \left(\frac{V_{GS}-V_{th}}{2}\right)^2 \left[\left(\frac{\Delta R_D}{R_D}\right)^2 + \left(\frac{\Delta(W/L)}{(W/L)}\right)^2\right] + \Delta V_{th}^2 \quad (7)$$

where W is a width, L is a length and R_D is a load resistor.

From Eq. 7, obviously the offset is due to the threshold voltage variation which is obtained earlier. In addition, the mismatch of the resistors and the mismatch of the transistors width/length also contribute to the offset. However, these two mismatches (resistor and transistor width/length) can be minimized by proper layout [11]. Therefore, we assume these two mismatches are small and not totally contribute to the phase noise variation.

D. Total phase noise Variation

Total phase noise variation can be determined by summing the variations on the tail and the differential pair (since they are uncorrelated). So, the total phase noise variation can be calculated as

$$\sigma_L = \sqrt{\sigma_{L(tail)}^2 + \sigma_{L(diff)}^2} \quad (8)$$

3.2 Relative Phase Noise Variation

Total standard deviation in Eq. (8) gives design insight for designing the oscillator. We can find out a relative variation for each component by dividing its standard deviation to the total phase noise, e.g. $\sigma_{(tail)}$ / L(f). From this relative variation, we can determine the design parameters that most affect phase noise variation.

From Eq. (5), phase noise variations due to the tail transistor are depending on alpha and overdrive voltage. These two parameters can be manipulated to minimize the phase noise variation. By using shorter channel length, value of alpha decreases but the threshold voltage variation, σ_{Vth} will increase. So, there is a trade-off by manipulating the transistor channel length for reducing the variation. The other option is by increasing the overdrive voltage. However, with this option we need to pay for the power consumption.

On the differential pair component, the overdrive voltage (on the differential pair) is affected by the threshold voltage variation. It is not a major contributor for the phase noise variation. However, both of the variation sources are included in the statistical model calculation.

4. Results and Discussions

The delay stage as in Fig. 1 is designed by using minimum channel length to show the threshold voltage variation impacts and it is used in 65-nm process technology.

The proposed statistical model is justified with the spice model through Monte Carlo simulations of the ring oscillator. This simulation is using SPECTRE RF where it is setup to simulate the phase noise due to the white noise.

The Monte Carlo simulation is configured to the mismatch variation for 1000 runs and its phase noise variation is tabulated in a histogram graph. The mean and standard deviation of the distribution are analyzed and compared with the proposed statistical model. This methodology is repeated for different supply voltage values (1.0V to 1.2V) for design insight information on how the supply voltage affects the phase noise variability. This is an essential step for low power applications which is performed by lowering the supply voltage.

Figure 2, 3 and 4 show the phase noise variation distribution for various supply voltages (1.0V to 1.2V). The means are the phase noise prediction and standard deviations are the phase noise variation. The distribution (histogram graph) is a Gaussian as predicted on the early chapter. This is due to the random process variation of the transistor. These histograms are the reference to justify the proposed statistical model. Depicted in these three histograms, it can be shown the phase noise prediction (μ value) is decreases as we pump higher supply voltage. So, the phase noise is less for higher $V_{DD.}$ It also knows the phase noise variation (standard deviation) decreases as V_{DD} is increased. This is due to the higher voltage headroom to occupy the overdrive voltage for the oscillator. However, we need to pay for the power consumption as mentioned in Table 1.

Figure 5 shows the results from our proposed statistical model and Monte Carlo simulation results. It is also representing the data from the histograms (Figure 2, 3 and 4) for the comparison purposes. The y-axis is a phase noise where the unit is V^2/Hz and the x-axis is V_{DD}. From Figure 5, good agreement is found between the proposed model and Monte Carlo simulation results. This justifies our proposed model which can be used for the designer to estimate oscillator phase noise variation and the phase noise yield.

Meanwhile, the relative phase noise due to the tail transistor is higher compared to the relative phase noise due to the differential pair. However, as V_{DD} scaling is applied, the phase noise variation from the differential pair is increases. This is due to the lower overdrive voltage of a differential pair.

Table 1: Ring oscillator performance

V_{DD} (V)	1	1.1	1.2
σ/μ (Tail) %	22.76	23.43	23.92
σ/μ (Diff. Pair) %	2.66	1.73	1.19
Power Consumption (μW)	52.81	64.34	76.42

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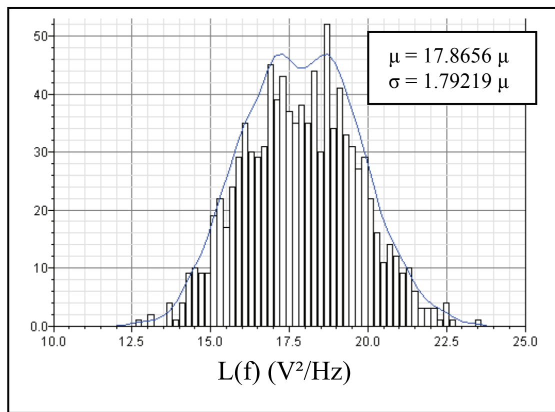

Figure 2: Histogram from Monte Carlo for 1.0V

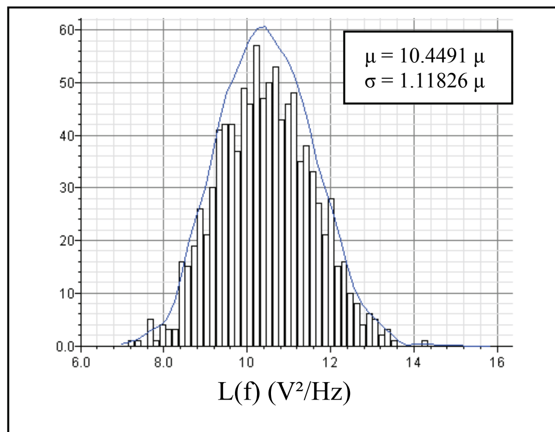

Figure 3: Histogram from Monte Carlo for 1.1V

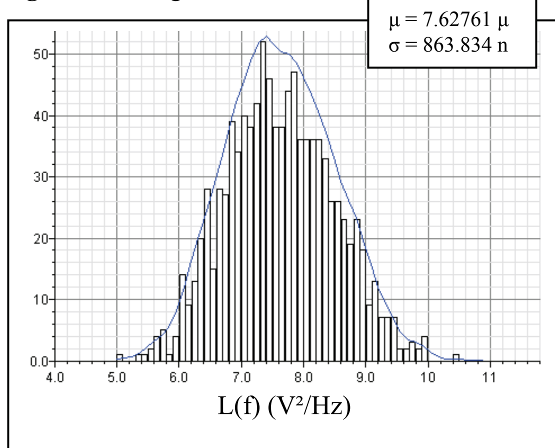

Figure 4: Histogram from Monte Carlo for 1.2V

5. Conclusion

Simple statistical model of the phase noise variation due to the white noise is derived. The proposed statistical model gives good agreement with the Monte Carlo simulation results. From the derivation, we know that there are certain parameters can be referred for the designer as a design insight, i.e. α and overdrive voltage. The effects of V_{DD} scaling also presented on this paper. Here, we know that the phase noise variation is less for higher V_{DD}. Meanwhile, phase noise variation due to the differential pair is increased as V_{DD} is reduced.

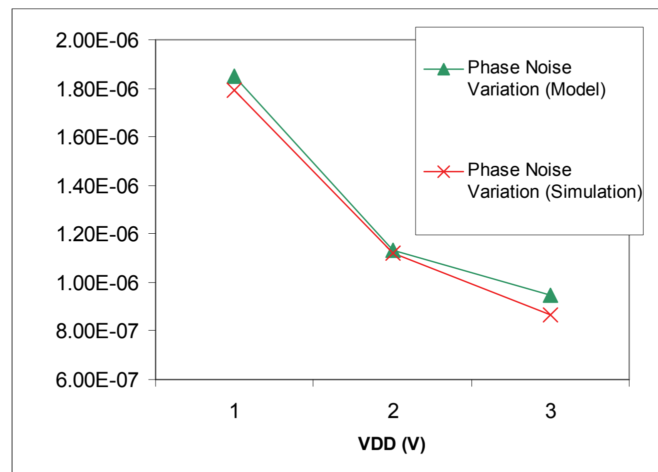

Figure 5: Ring oscillator phase noise and its variation from the Monte Carlo simulation. It also shows the results from statistical model.

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