The Impact of Timing Yield Improvement Under Process Variation on Flip-Flops Soft Error Rate

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***Abstract*—In deeply pipelined synchronous systems, any violation of the timing constraints of the flip-flops can cause the overall system to malfunction. Due to CMOS technology scaling, increased process variations result in a large delay variability causing unacceptable loss in the timing yield. Several variation tolerant techniques are introduced to mitigate this variability challenge by improving the timing yield. In the mean time, devices are getting smaller, faster, and operating at lower supply voltages. These reduced capacitances and power supply voltages combined with the increased chip density to perform more functionality increase the soft errors susceptibility and make it one of the essential design challenges. Moreover, there are many flip-flops topologies that vary in their relative performance and power consumption which make the selection decision very difficult to flip-flops designers especially under variability and soft errors challenges. Therefore, a comparative analysis between these different flip-flops topologies considering these scaling challenges is beneficial to guide the flip-flops designers in selecting the best topology for their specific application constraints. This paper presents a comparative analysis of the timing yield improvement impact on flip-flops soft error rate by using the STMicroelectronics 65-nm CMOS technology. The analyzed flip-flops are compared for power and power-delay product (PDP) overheads to achieve this timing yield improvement. Then, they are compared for the soft error susceptibility. Finally, it is shown that the timing yield improvement improves the flip-flops soft error immunity significantly.**

I. Introduction

As CMOS technology continues to scale towards the nanometer regime, the transistor parameters, such as threshold voltage, channel length, mobility, and oxide thickness, will have large statistical process variations [1-6]. Consequently, these process variations result in delay uncertainty. Thus, the deterministic design methodologies should be replaced by the statistical design methodologies [1,7]. The process variations can be classified as die-to-die (D2D) variations or within-die (WID) variations. In D2D variations, all devices on the same die are assumed to have the same parameters. However, devices on the same die are assumed to behave differently for WID variations [2]. Although D2D variations were originally considered as the major source of process variations, WID variations have now become the main design challenge as technology scales [4,5].

Moreover, the demand for higher performance has moved the clock frequencies up to multi-GHz in microprocessors and other advanced VLSI applications. These increased clock frequencies lead to very deep pipelining which means that hundreds of thousands of flip-flops are required to control the data flow under strict timing constraints. A violation of the timing constraints at a flip-flop may result in latching incorrect data causing the overall system to malfunction [8]. Deterministic gate sizing tools size the circuits to optimize the power-delay-product (PDP). However, due to process variations, a large number of circuits might not meet the target delay. Consider as an intuitive example a flip-flop that is designed for optimum PDP, which exhibits a specific target delay. Due to random process variations, the delay will be normally distributed with the probability density function (pdf) shown in Figure 1. This figure shows that 50% of the total number of flip-flops will not meet the desired target delay constraint. Therefore, the flip-flops have to be designed using statistical sizing tools to improve the timing yield [1,9,10].

Reliability is another major challenge for sub-micron CMOS technology. Shrinking geometries, lower supply voltages, higher clock frequencies, and higher density circuits all have a great impact on reliability [11-17]. As CMOS technology scales, soft errors become one of the major reliability concerns. Soft errors result when energy particles hit a silicon substrate, the kinetic energy of the particle generates electron-hole pairs as they pass through the p-n junctions. Some of the collected charges will recombine to form a very short duration current pulse that disturbs the struck node voltage and can lead to soft errors [12]. In memory elements, this disturbance can cause bit flips (0-to-1 flip or 1-to-0 flip) which may corrupt the logic state of the circuit. However, in combinational circuits it may cause a temporary change in the output node voltage. This temporary change may be tolerated, unless it is latched by a succeeding memory element. For memory elements such as Static Random Access Memory (SRAM) and flip-fops, if the charge collected ($Q_{collected}$) by the particle strike at the storage node is more than a minimum value, the node is flipped and a soft error occurs. This minimum value is called a critical charge ($Q_{critical}$) which can be used as a measure of memory element vulnerability to soft errors [12,15,17-20].

Soft errors are mitigated in background memories such as SRAM cells by providing error correction techniques. However, these techniques can not be used with flip-flops. In addition, The increased clock frequencies increase the probability that a flip-flop will latch on to an error since this latching occurs at each clock edge. Therefore, analysis of soft errors vulnerability on different flip-flops topologies is of paramount importance. Soft error yield is introduced in this

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paper as a measure for the impact of process variations on soft error immunity.

In this paper, a complete comparative analysis of process variation impact on flip-flops soft error vulnerability will be introduced. These flip-flops will be sized using statistical gate sizing algorithm to improve the timing yield. The effect of this timing yield improvement on the soft error yield will be discussed as well as the required power and PDP overheads to achieve this timing yield improvement. This paper provides some design insights to help flip-flops designers in selecting the best flip-flop topology for scaled technologies. This paper is organized as follows: Section II introduces the selected flip-flops topologies and summarizes the flip-flops timing characteristics. Section III describes the simulation procedure and setup. Simulation results are given in section IV. Finally, some conclusions are drawn in section V.

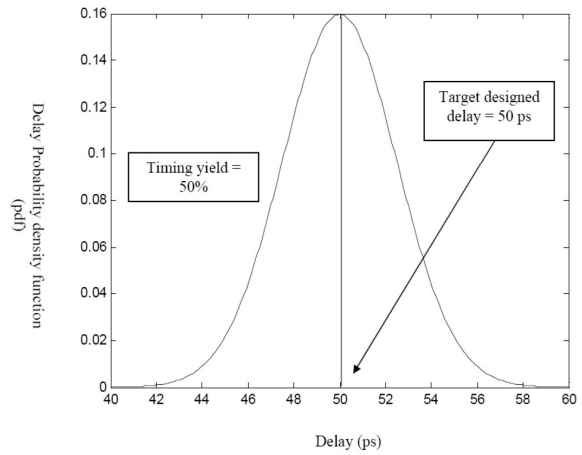

Fig. 1. The delay pdf due to process variations under deterministic gate sizing algorithms. It shows, intuitively, that up to 50% of flip flops will not meet the target delay (50 ps in this example)

II. Flip-Flops Timing Characteristics and Selection

A clock signal is used in clocked registers to control the timing of the data latching process. These clocked registers can be classified into latches and flip-flops. Latches are described as level-sensitive registers, because the input data is latched when the clock signal maintains a specific voltage level. Flip-flops are called edge-triggered registers, since the input data is latched by a transition edge in the clock signal waveform. The flip-flop can sample the input data correctly if the following constraints are satisfied:

• Setup time (T_{setup}) is defined as the minimum time that the input data should be available before the clock sampling edge arrival.

• Hold time (T_{hold}) is defined as the minimum time that the input data should be available after the clock sampling edge.

The timing relations among the input data, clock signal, and output data of a flip-flop can be obtained by the following timing characteristics [21]:

• Clock-to-output delay (T_{Clk-Q}) represents the delay from the sampling clock edge (Clk) to the time the latched data is valid at the output (Q).

• Data-to-output delay (T_{D-Q}) represents the delay from a transition of the input data (D) to the time the latched data is valid at the output (Q). This delay is determined as the sum of the setup time and the clock-to-output delay.

Four different flip-flops have been selected representing different trade-off choices between performance and power dissipation [1,22]. Figures 2 and 3 show the transmission-gate master-slave flip-flop (TG-MSFF) and the modified clocked CMOS master-slave flip-flop (M-C^{2}MOS-MSFF) respectively. Both of them are implemented by cascading two complementary latches. This master-slave implementation results in robust flip-flop. Moreover, they are used in standard libraries [1,22] which make it so important to include them in this comparison. Figure 4 shows one of the fastest flip-flops which is called semi-dynamic flip-flop (SD-FF) [23]. This flip-flop can be considered as a pulsed latch since it samples the input data to the flip-flop output during a very short transparency period around the clock sampling edge. Accordingly, the input data may arrive after the clock edge. Therefore, this flip-flop is used in high performance VLSI applications due to its relatively short data-to-output delay at the expense of poor hold time behavior and excess power consumption. Figure 5 shows a sense-amplifier based flip-flop (SA-FF) with a NAND SR-latch [24]. This flip-flop can be viewed as a compromise between the master-slave robustness and pulsed latches high performance.

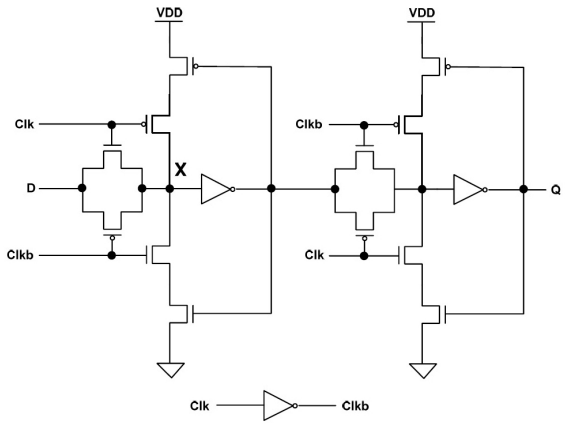

Fig. 2. The Transmission Gate based Master-Slave Flip-Flop (TG-MSFF)

III. Simulation Procedure and Setup

A. Optimum PDP Design

All flip-flops are optimized for minimum PDP by using a STMicroelectronics 65-nm CMOS technology transistor model, a 1V power supply voltage, a typical process corner, a clock frequency of 1 GHz and pseudorandom input data with a 50% data activity [21]. The measured PDP is obtained by multiplying the data-to-output delay (T_{D-Q}), and the total power consumption which includes both the internal power dissipation and the local clock/data power dissipation [21].

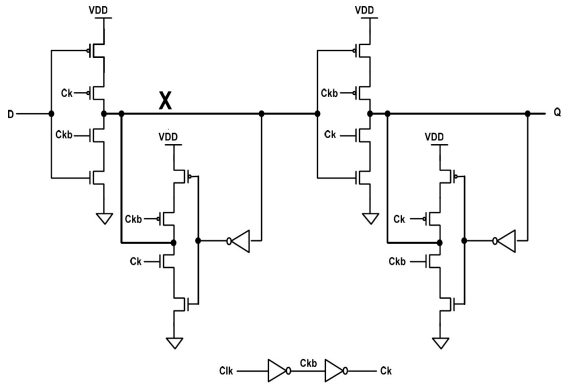

Fig. 3. The Modified Clocked CMOS Master-Slave Flip-Flop (M-C^{2}MOS-MSFF)

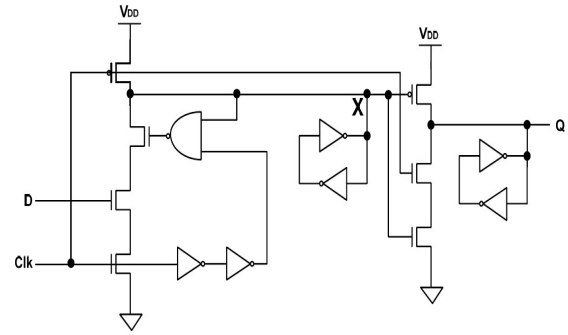

Fig. 4. The Pulsed Semi-Dynamic Flip-Flop (SD-FF)

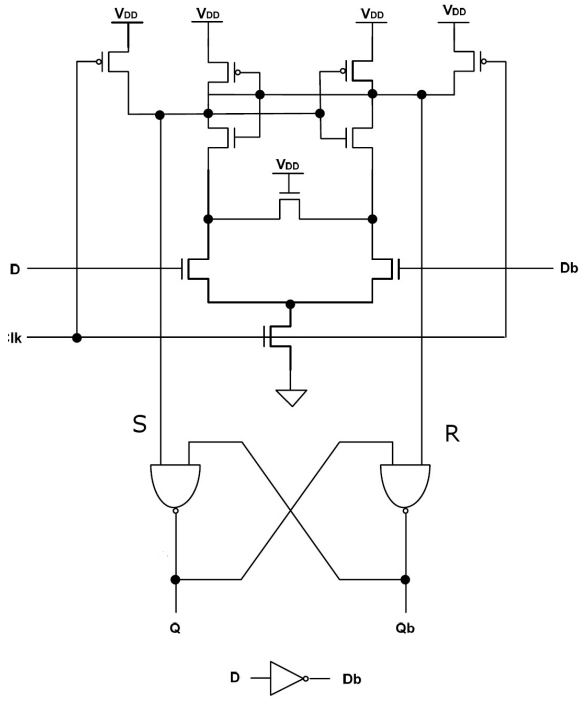

Fig. 5. The Sense-Amplifier based Flip-Flop (SA-FF)

The optimum setup time for each flip-flop is determined to achieve minimum PDP. The optimization process is conducted by using the CFSQP (C Version Feasible Sequential Quadratic Programming) optimization technique, implemented in Spectre-RF. This algorithm is based on the finite difference perturbation (FDP) method to determine how sensitive the PDP is to each device size. Then the algorithm provides the optimal sizing and setup time to achieve the minimum PDP.

B. Impact of Process Variations on Flip-Flop Delay

Monte Carlo analysis, including the mismatch between transistors is performed on the flip-flops at the optimal PDP point. An industrial hardware-calibrated statistical STMicroelectronics 65-nm CMOS transistor model is used in this Monte Carlo analysis. In this model, the transistor parameters such as the threshold voltage and the channel length are modeled by a normal distribution within the $\pm 3\sigma$ design space. The number of the Monte Carlo analysis points used is 5000 points to provide a good accuracy. The delay, power, and PDP variability are then obtained.

C. Functional Yield Improvement Using Setup Time Margin

The optimum setup time determined in Subsection III.A, is obtained by using a typical process corner to minimize the PDP. This results in a poor functional yield, since the setup time constraint of some of the flip-flop simulated Monte Carlo points will be violated. Typically, the functional yield of the flip flops with this setup time ranges from 85% to 95%. A setup time margin is added to achieve a functional yield greater than 99.9% [1,22]. This setup time margin is determined by sweeping the setup time and calculating the functional yield and the mean delay (T_{D-Q}). The setup time that achieves a functional yield greater than 99.9% and minimum (T_{D-Q}) is selected.

D. Timing Yield Improvement Using Gate Sizing

The delay variability is obtained from the Monte Carlo simulations by adopting the modified setup time. The timing yield of all the flip flops at the target delay (assumed to be the optimal delay achieved at minimum PDP) is less than 50%. A simplified gate sizing algorithm is employed. It is similar to that in [9] but the Lagrangian Relaxation (LR) optimization technique is replaced by the CFSQP optimization technique, implemented in Spectre-RF. This algorithm utilizes the finite difference perturbation (FDP) method to determine how sensitive the delay and power are to each device size. This algorithm can be considered as one of the sensitivity based sizing algorithms. Figure 6 represents the gate sizing algorithm flow diagram. It starts with a given delay constraint (A_o) and timing yield constraint (Y_o), where (A_o) is the optimal delay obtained at minimum PDP. Then, the gate sizing values obtained for the minimum PDP are used as an initial gate sizing values. Monte Carlo statistical analysis is then applied to obtain the delay variability. The standard deviation (σ) of the obtained delay distribution is calculated. Following that, the new delay constraint (A_o') is obtained by using the following equation:

$$A'_o = A_o - n * \sigma \tag{1}$$

where n is dependent on the target timing yield value (Y_o) and can be obtained from the normal distribution tables. For example, in this paper, a timing yield of 99.87% (Y_o = 99.87%) is required, which means that "n" must equal 3.0 from the normal distribution tables. Following the calculation of (A_o'), an optimization problem is solved by employing CFSQP to determine the new gate sizing that matches the delay (A_o') and minimizes the total power consumption. These steps are repeated, until the timing yield constraint is achieved. It should be emphasized that the delay pdf changes after each iteration because the variations in the threshold voltage are a strong function of the transistor width [1,9]. If the delay standard deviation decreases or does not change from iteration n to iteration n+1, the timing yield constraint is met and the algorithm stops. However, if the delay standard deviation increases, more iterations are required to reduce the mean delay, resulting in higher power and PDP overheads. Figure 7 illustrates how this gate sizing algorithm improves the timing yield by moving the delay pdf to a shorter mean delay. Figure 8 displays the effect of the delay standard deviation on the number of iterations required. Then, the power and PDP overheads, required to achieve this timing yield improvement, are calculated for each flip-flop.

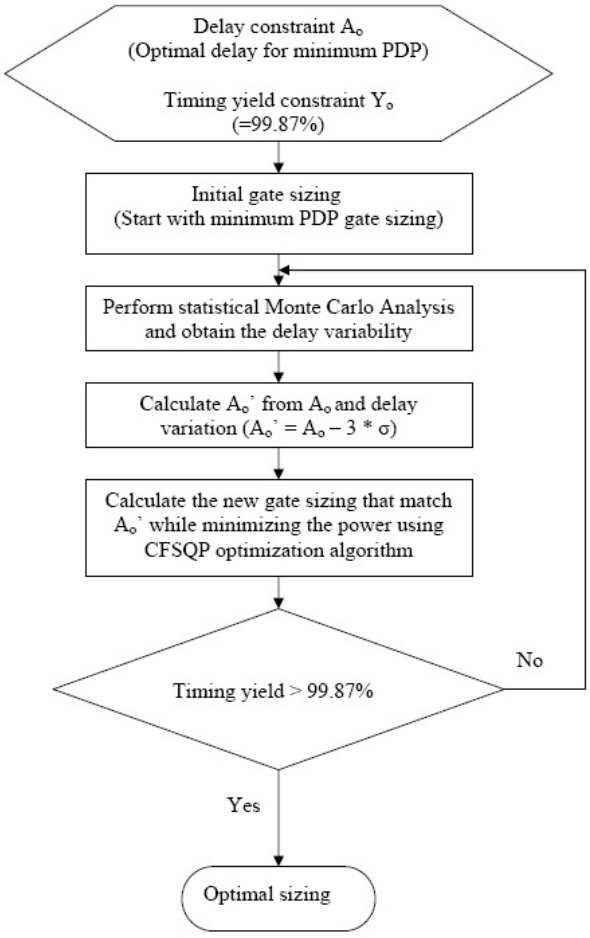

Fig. 6. The gate sizing algorithm flow diagram

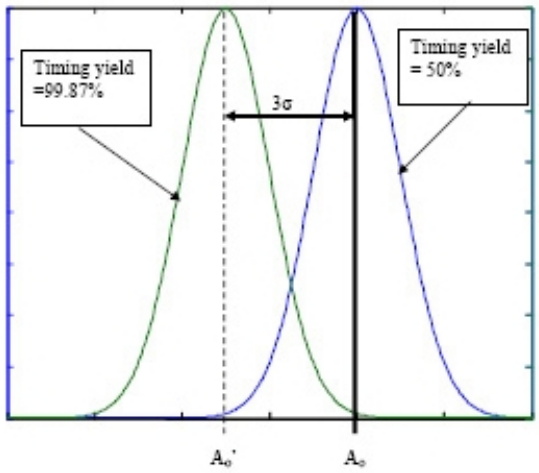

Fig. 7. The timing yield improvement under process variations employing gate sizing

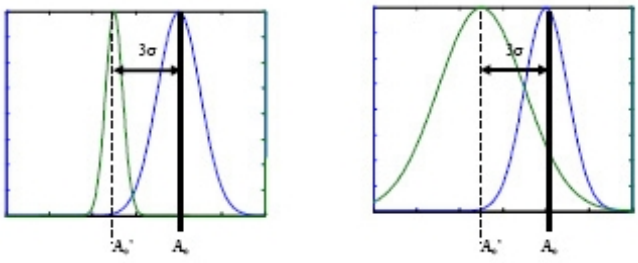

Fig. 8. The delay standard deviation effect on the algorithm number of iterations. If the standard deviation decreases, the timing yield constraint is met in a single iteration. However, if it increases, more iterations are required to achieve the target timing yield

E. Soft Error Modeling

The Soft error rate (SER) can be calculated by using the following equation which describes the relationship between the SER and $Q_{critical}$ [25].

$$SER \;\; \alpha \;\; N_{flux} \times CS \times \exp(-Q_{critical}/Q_s) \qquad (2)$$

where N_{flux} refers to the intensity of the neutron flux, CS is the cross section area of the node, and Q_s is the charge collection efficiency which strongly depends on doping [26]. Therefore, $Q_{critical}$ can be modeled as a measure of the SER for different flip-flops topologies. Since the recombination of the collected charges results in a very short duration current pulse which might cause soft error. This current pulse can be approximated by the following equation [26]:

$$I(t) = I_{peak} \times [\exp(-t/\tau_a) - \exp(-t/\tau_b)] \qquad (3)$$

where I_{peak} represents the current pulse amplitude, τ_a is the collection time constant, and τ_b is the ion-track establishment time constant.

In this paper, the particle strike is modeled as a current source connected to the flip-flop circuit nodes. The parameters τ_a and τ_b equals 200ps and 10ps respectively. I_{peak} is varied iteratively to achieve the minimum amount of charge, $Q_{critical}$,

which results in a bit flip at the output node. Hence, $Q_{critical}$ can be given by:

$$Q_{critical} = minimum[\int_0^{t_f} I(t)dt] \quad (4)$$

where t_f refers to the flipping time of the output node and I(t) is the current pulse model given in equation (3). The critical charge is calculated at all nodes of each flip-flop for the 1-to-0 flip and the 0-to-1 flip at the output node. Then, the node that has the smallest critical charge is selected as the most susceptible node to soft errors. Following that, the same Monte Carlo setup mentioned in subsection III.B is conducted, and the critical charge distribution is obtained.

F. Soft Error Yield

The process variation impact allows some flip-flops samples to have critical charge values larger than the nominal value, and other flip-flops samples to have smaller values. Although the flip-flops with larger critical charge values are less vulnerable to soft errors, the flip-flops with smaller values will be negatively impacted by the process variations. This is similar to the delay variability due to process variations, as some samples will have less delay than the nominal delay (which is desirable) and other samples will have more delay which may violate the timing constraint. Hence, the soft error yield can be defined in a similar manner as the timing yield. By using the critical charge distribution obtained in the previous subsection, and at a given collected charge $Q_{collected}$, the probability of flipping can be computed by using Figure 9 as follows:

$$Probability\ of\ flipping = \int_0^{Q_{collected}} f(Q_{critical})dQ_{critical} \quad (5)$$

Then, the soft error yield is given by:

$$\begin{aligned} &Soft\ \ error\ \ yield \\ &= \quad 1 - \int_0^{Q_{collected}} f(Q_{critical})dQ_{critical} \end{aligned} \quad (6)$$

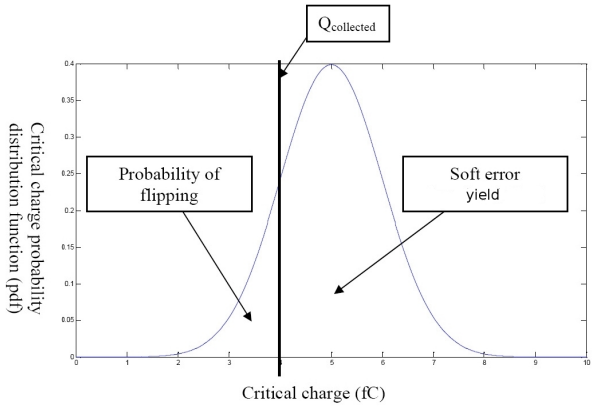

Fig. 9. The critical charge probability distribution function and the soft error yield definition.

IV. Simulation Results and Discussions

A. Timing yield Improvement and Required Power and PDP Overheads

Table 1 summarizes the simulations results for all the flip-flops. The comparison is performed for the improved timing yield flip-flops. The optimal T_{D-Q} delay is adopted as the target delay constraint for timing yield improvement for each flip-flop. The SD-FF has a 2.4X higher performance compared to the M-C^{2}MOS-MSFF at the expense of a 1.4X higher power dissipation. Figure 10 shows the relative power and the relative PDP overhead of the improved timing yield flip-flops.

According to the results in Figure 10, the SA-FF has a power overhead of 58.2% which is 1.7X higher than that of the TG-MSFF. Moreover, the SA-FF suffers 25.26% PDP overhead which is 2.8X higher than that of the TG-MSFF. The reason for this is that the SA-FF implementation utilizes a symmetric cross-coupled architecture which suffers from devices mismatch more than all other flip-flops. The M-C^{2}MOS-MSFF delay standard deviation increases from one iteration to the next. Consequently, this flip-flop requires the highest number of gate sizing algorithm iterations which increases the required power overhead to minimize its mean delay. The SD-FF has the same PDP overhead as the M-C^{2}MOS-MSFF while having 1.2X less power overhead. The TG-MSFF exhibits the lowest power and PDP overheads of 30.87% and 9%. This advantage is due to the fact that its delay standard deviation decreases with iterations. This flip flop takes the lowest number of gate sizing algorithm iterations. Correspondingly, its power overhead is smaller than that of each of the other flip-flops.

Figures 11, 12, 13, and 14 show the average power consumption versus the T_{D-Q} delay space for the improved timing yield flip-flops. It is evident that all but one of the flip-flops have a timing yield $>$ 99.87%, where the optimal delay is the timing constraint. The TG-MSFF exception, achieves a timing yield of 99.6%, at most. This emphasizes the need for a more efficient algorithm. However, we do not attempt to automate the process since this is not the main purpose of this research. Moreover, a timing yield of 99.6% is close to the timing yield objective of 99.87%.

Table 1: Simulation results for different flip flops designs

		(TG-MSFF)	(M-C^{2}MOS-MSFF)	(SD-FF)	(SA-FF)
T_{D-Q} delay	Optimal (ps)	48.61	76.36	32.55	49.6
	Mean (ps)	40.71	57.67	26.1	39.35
	σ (%)	6.71	4.62	5.89	6.51
Power	Optimal (μW)	8.86	11.48	16.28	12.74
	Mean (μW)	11.65	17.74	23.69	20.21
	σ (%)	2.0	1.18	1.9	1.56
	Relative overhead (%)	30.87	53.92	44.8	58.2
PDP	Optimal (fJ)	0.43	0.88	0.53	0.632
	Mean (fJ)	0.47	1.02	0.62	0.8
	σ (%)	5.54	4.5	5.6	6.0
	Relative overhead (%)	9.0	15.77	15.7	25.26

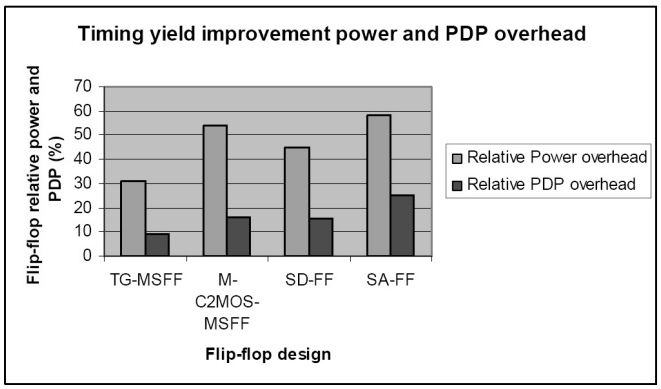

Fig. 10. The relative power and PDP overheads due to timing yield improvement

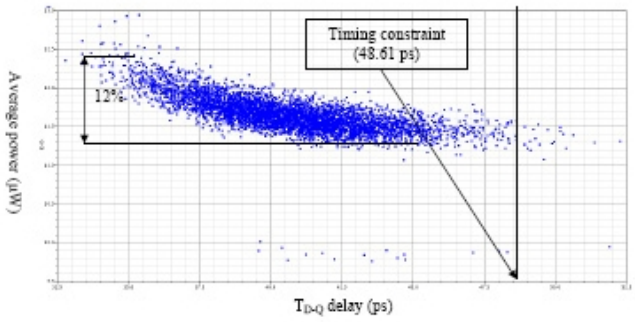

Fig. 11. The power-delay spread of the TG-MSFF

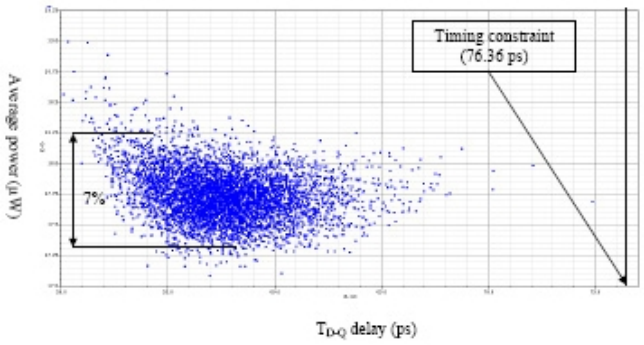

Fig. 12. The power-delay spread of the M-C^{2}MOS-MSFF

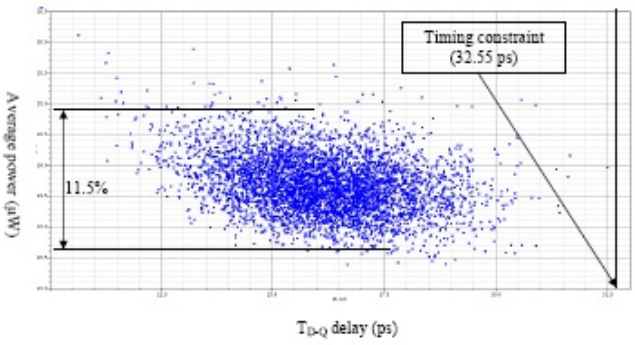

Fig. 13. The power-delay spread of the SD-FF

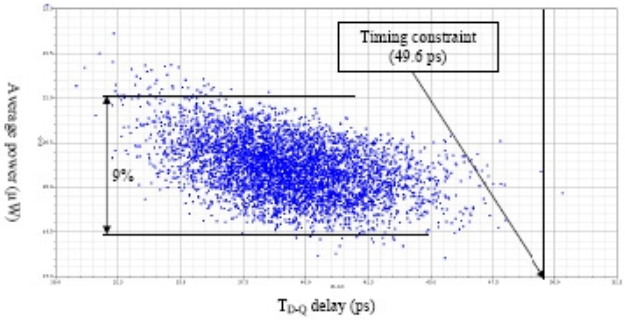

Fig. 14. The power-delay spread of the SA-FF

Table 2: The nominal critical charge values for the selected flip-flops

TG-MSFF			M-C^{2}MOS-MSFF	SD-FF SA-FF		
Most susceptible node		X	X	X	S	R
$Q_{critical}$ (fC) (1-to-0 flip)	Minimum PDP	2.91	3.51	6.70	0.72	0.22
	Improved Timing yield	3.99 6.9		38.95	1.94	0.31
$Q_{critical}$ (fC) (0-to-1 flip)	Minimum PDP	3.94	3.15	4.35	0.71	1.85
	Improved Timing yield	5.75 5.17		5.93	1.11	2.1

B. Nominal Critical Charge

Table 2 summarizes the nominal critical charge values and the corresponding nodes for the 1-to-0 and the 0-to-1 flips for the selected flip-flops. It should be noted that the SA-FF critical charge has to be determined for both nodes S and R because node R is more susceptible to soft errors in the case of 1-to-0 flip while node S is more in the case of 0-to-1 flip. The values for the nominal critical charge are obtained for two different flip-flops sizing scenarios. One for optimum PDP and the other for timing yield improvement. According to the results in Table 2, the least vulnerable flip-flop to soft errors is SD-FF. It has the largest critical charge for both the 1-to-0 and the 0-to-1 flips in the two sizing scenarios. This advantage is due to its cross coupled inverters connected at node X which fight to keep this node at its logic state. Moreover, this pulsed flip-flop latches its input to its output during the transparency period which comes after the clock edge at which the particle strike current pulse model is injected. The SA-FF exhibits the smallest $Q_{critical}$ due to the SR latch since any error occurs at S or R results in flipping the output node immediately. Hence, this flip-flop has very small flipping time (t_f).

The master-slave flip-flops exhibit roughly the same critical charge nominal value which lies half-way between the SD-FF and the SA-FF critical charge values. The master-slave flip-flops exhibit a long flipping time, since, the error at node X in both master-slave based flip-flops will take longer time to propagate to the output node. In addition, node X will be in the hold mode, when it is connected to the back to back inverters, which reduces its susceptibility to soft errors. Figures 15 and 16 show how the timing yield improvement increases the soft error immunity of all the flip flops. This can be simply justified

since the timing yield improvement increases the aspect ratio of the devices, and hence, increases their nodal capacitances. Correspondingly, the critical charge value is increased. For the 1-to-0 flip case, the critical charge increases due to the timing yield improvement by a factor ranging from 1.4X to 5.8X. on the other hand, for the 0-to-1 flip case, this factor ranges from 1.4X to 1.6X. It should be noted that although the largest power and PDP overheads to achieve this timing yield improvement occurs in the SA-FF, its critical charge increasing factor is still small. The SD-FF exhibits a large critical charge increasing factor of 5.8X in the case of 1-to-0 flip. This large factor is due to the sizing used to reduce the flip-flop T_{D-Q} delay to achieve the target timing yield increase the size of the NAND gate which increases the capacitance at node X.

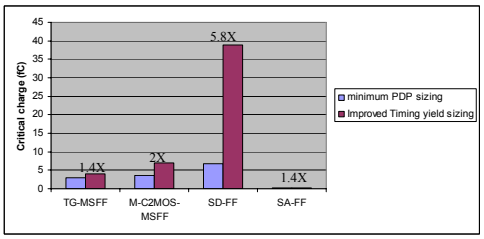

Fig. 15. The critical charge increase due to timing yield improvement for 1-to-0 flip

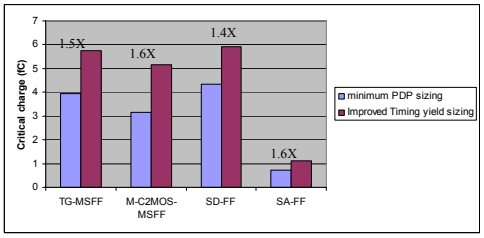

Fig. 16. The critical charge increase due to timing yield improvement for 0-to-1 flip

C. Critical Charge Distribution

The critical charge distributions for the selected flip-flops are tabulated in Table 3. It is shown that the TG-MSFF exhibits small critical charge variations for both 1-to-0 and 0-to-1 flips for both sizing scenarios. The reason for these small variations in the TG-MSFF is that the soft error occurs at node X will exhibit longer path to affect the output node (two inverters and a transmission gate). This long path exhibits averaging effect which results in random variations cancelation. Correspondingly, this flip-flop will exhibit small critical charge variations. The SA-FF suffers from higher critical charge variations. There are two main reasons for these higher variations. The first reason is due to the differential architecture used in the SA-FF which suffers from the transistors mismatch variations (within die variations). The second reason is the smallest path from nodes S or R to the output node which has small averaging effect. It is obvious that the timing yield improvement increases the critical charge mean while reducing the critical charge variance. There are only two cases (shown in bold in Table 3) in which the timing yield improvement is no longer capable of reducing the critical charge variations. These two cases related to the SD-FF which actually has the largest critical charge mean in the two sizing scenarios adopted. Moreover, the critical charge variations increased in the first case by a factor of 1.1X while kept constant in the second case. Hence, it can be concluded that the timing yield improvement is a good technique to achieve good performance and at the same time improves the circuit immunity to soft errors. Figures 17 and 18 show the percentage critical charge variations occurs as a result of the timing yield improvement for the 1-to-0 and 0-to-1 flip cases respectively. The case of the SD-FF is highlighted in both figures.

Table 3: The critical charge mean and percentage standard deviation of the selected flip-flops under process variations for the two sizing cases

			TG-MSFF	M-C^{2}MOS-MSFF	SD-FF	SA-FF	
						S	R
$Q_{critical}$ (1-to-0 flip)	Minimum PDP	Mean (fC)	2.93	3.5	5.51	0.65	0.23
		σ(%)	14.6	38.4	**24.2**	36.9	24.8
	Improved Timing Yield	Mean (fC)	3.95	6.66	38.87	1.76	0.31
		σ(%)	10.9	18.6	**27.4**	25.3	13.9
$Q_{critical}$ (0-to-1 flip)	Minimum PDP	Mean (fC)	3.91	3.11	4.36	0.69	1.36
		σ(%)	6.6	16.9	**5.5**	9.6	24
	Improved Timing Yield	Mean (fC)	5.7	5.14	5.9	1.12	1.63
		σ(%)	5.4	8.7	**5.5**	7.4	15.2

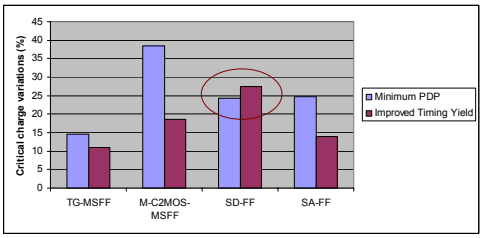

Fig. 17. The timing yield improvement impact on the critical charge standard deviation percentage for the 1-to-0 flip

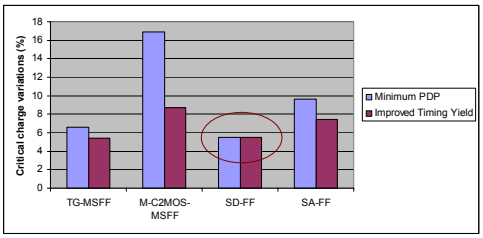

Fig. 18. The timing yield improvement impact on the critical charge standard deviation percentage for the 0-to-1 flip

D. Soft Error Yield

The soft error yield is a good measure of the flip-flop immunity to soft errors. It represents the percentage of flip-flops that will function properly under soft errors. In other words, a soft error yield of 90% means that 10% of the fabricated flip-flops will malfunction due to the impact of process variations on soft errors. Using equations (5) and (6), the soft error yield as a function of the collected charge ($Q_{collected}$) is shown in Figures 19-22 for the 1-to-0 flip and the 0-to-1 flip respectively for both sizing scenarios. According to these figures, the soft error yield is increased for all flip-flops under timing yield improvement even the SD-FF that shows increased critical charge variations.

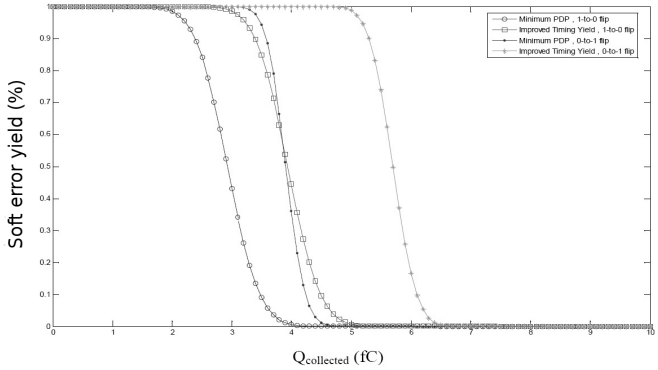

Fig. 19. The TG-MSFF soft error yield for 1-to-0 flip and 0-to-1 flip with the two sizing scenarios

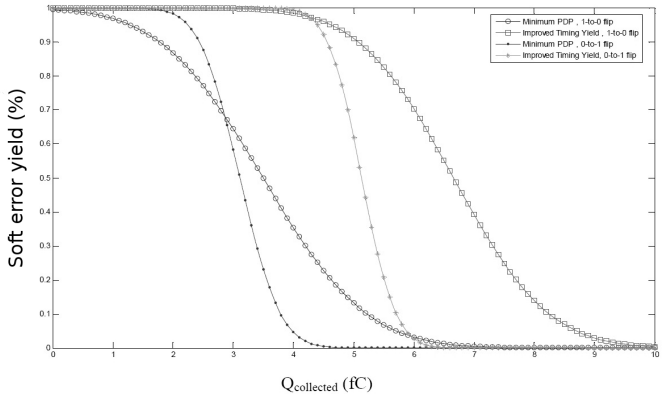

Fig. 20. The M-C^{2}MOS-MSFF soft error yield for 1-to-0 flip and 0-to-1 flip with the two sizing scenarios

For a given value of $Q_{collected}$, we can easily get the soft error yield from these figures. It is clear from these figures that the SD-FF has the highest soft error yield as compared to other flip-flops in both sizing scenarios while the SA-FF has the smallest. However, the TG-MSFF and the M-C^{2}MOS-MSFF give different soft error yield depending on the value of $Q_{collected}$.

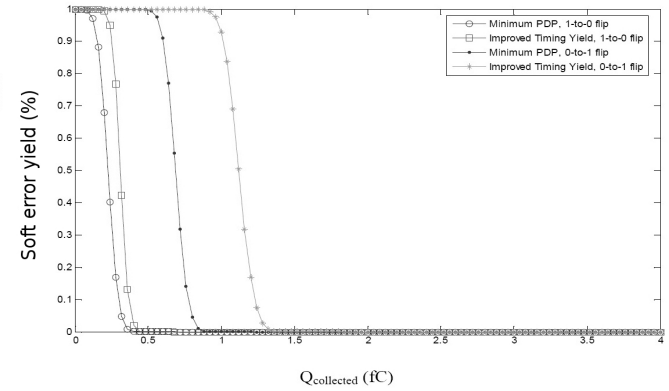

Fig. 21. The SA-FF soft error yield for 1-to-0 flip and 0-to-1 flip with the two sizing scenarios

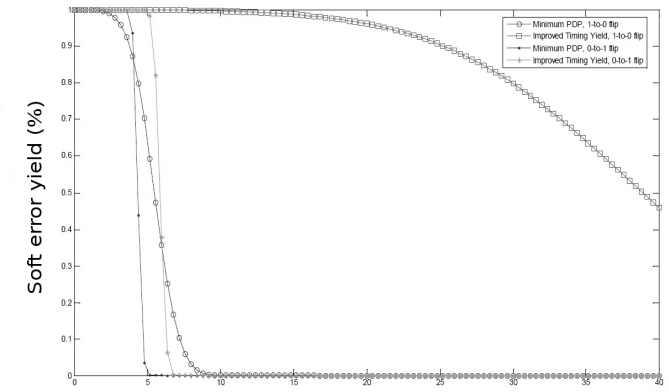

Fig. 22. The SD-FF soft error yield for 1-to-0 flip and 0-to-1 flip with the two sizing scenarios

V. Conclusion

A comparative analysis of timing yield improved four commonly used flip-flops is introduced. The SA-FF suffers from devices mismatch which results in power overhead of 1.7X higher than that of the TG-MSFF and PDP overhead of 2.8X higher than that of the TG-MSFF. Moreover, the impact of this timing yield improvement on the soft error yield is investigated. Simulations results show that the timing yield improvement increases the soft errors immunity since increasing the transistor sizing will increase the nodal capacitances. However, The SA-FF is the most vulnerable flip-flop to soft errors and its soft error yield is very poor even under timing yield improvement. The reason for that is due to its small flipping time and more sensitivity to transistor mismatch (within die variations). The least vulnerable flip-flop to soft errors is SD-FF with high soft error yield. This work recommends that the SD-FF is the best choice for high soft error yield and high performance at the expense of higher power. When the power budget is the major concern, master-slave flip-flops are preferred. If the SA-FF should be used, soft error mitigation techniques are required for proper operation since the SA-FF has a poor soft error yield.

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