Novel Low-Power Accurate Wide-band CMOS Negative-Second-Generation-Current-Conveyor Realizations Based on Floating-Current-Source Building Blocks

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***Abstract*—This paper presents two novel Floating Current Source (FCS) based CMOS negative second generation current conveyor (CCII-) realizations suitable for very large scale implementation. The proposed realizations provide high voltage and current tracking accuracy, as well as large voltage and current transfer bandwidths. Simulations show that the first proposed wide band CCII- bandwidth is about 972 MHz. Targeting low power dissipation, a second low power version of the wide band CCII- is proposed at the expense of lower bandwidth. In addition, a fair comparison is held between the proposed realizations and the only FCS-based CCII- realizations in the literature to show the strength of the proposed circuits.**

***Index Terms*—Accurate CMOS current conveyor; Floating current source; Wide band; Low power; Analog circuits**

I. Introduction

SECOND Generation Current Conveyor (CCII) is a very versatile building block in analog circuits [1-3]. One type of the CCII is the negative second generation current conveyor (CCII-) which is defined by:

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix} \quad (1)$$

Therefore, the CCII- performs a voltage conveying action from node Y to node X and a current conveying action from node X to node Z. The input resistance r_x should be designed as small as possible since node X is a current-input and a voltage-output node. Node Z output resistance r_z should be designed as high as possible since it is a current-output node. In addition, the voltage conveying and current conveying actions should be performed as accurate as possible over a wide-band of frequencies to be suitable for high frequency applications.

The demand for accurate CMOS CCII- suitable for high frequency applications has led designers to do extra effort in finding realizations that meet these requirements [4]-[17]. The Floating Current Source (FCS) shown in Fig.1.a was introduced to be used as an output stage for current-mode feedback amplifiers [11]-[13].

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Following that, the FCS is used as the output stage of the accurate CCII- proposed in [14] to perform the required current conveying action. The FCS has also been recently used in the realization of fully differential voltage second generation current conveyor [18].

In this paper the FCS is analyzed in a way that should help in understanding the operation of the proposed negative second generation current conveyor (CCII-). The floating current source, FCS, shown in Fig.1.a [11] provides two balanced output currents and its block diagram is shown in Fig.1.b. These two output currents are given by [15].

$$I_{o1} = -I_{o2} = -\frac{1}{2} v_d [\sqrt{K_n}\sqrt{2I_B - \frac{K_n v_d^2}{4}} + \sqrt{K_p}\sqrt{2I_B - \frac{K_p v_d^2}{4}}] \quad (2)$$

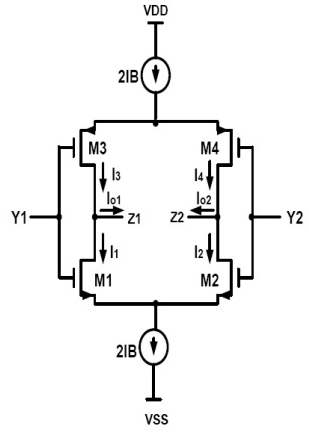
$$\text{where} \qquad v_d = V_1 - V_2 \quad (3)$$

V_1 and V_2 are the voltages applied to Y_1 and Y_2 respectively.

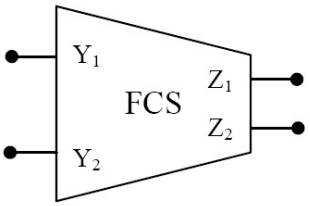
$$K_n = \mu_n C_{ox} \frac{W1}{L1} \quad (4)$$

$$K_p = \mu_p C_{ox} \frac{W3}{L3} \quad (5)$$

A novel wide band and high accuracy FCS based CMOS CCII- is proposed in this paper. The proposed CCII- utilizes the FCS in its voltage conveying and current conveying sections. Holding a fair comparison with the FCS based CCII- reported in [14], the proposed circuit achieves wider voltage and current transfer bandwidths. Moreover, the proposed circuit achieves higher voltage and current transfer accuracies and also less power keeping approximately all other parameters slightly with the same accuracy. Since, an essential demand of today's integrated circuits applications is to reduce the power dissipation of the analog circuits. Hence, a novel low power version of the proposed CCII- is also presented in this paper. This low power version dissipates less power at the expense of lower bandwidth. This circuit is compared as well with the FCS based CCII- reported in [14] and shows better performance in all aspects.



(a)



(b)

Fig. 1. (a) The floating current source (FCS) [11] and (b) its block diagram of the FCS

For all the circuits examined in this paper, the supply voltages are ±1.5 V SPICE simulations are performed with model parameters of 0.5 μm CMOS process provided by MOSIS (AGILENT).

II. The Proposed FCS Based CCII- Circuits

A. Novel Accurate Wide-Band FCS Based CCII-

The CMOS realization of the proposed accurate wide-band FCS based CCII- is shown in Fig.2. The voltage conveying action is provided using negative feedback in this proposed circuit. Moreover, this proposed circuit allows independent control of the CCII- voltage conveying and current conveying dynamic ranges. The utilization of two cascaded gain stages results in a small impedance level at the input node of the proposed CCII-, as well as voltage and current gains very close to unity. The block diagram of this realization is shown in Fig.3. All the transistors (M_1-M_{12}) are matched. Assuming that all the transistors operate in the saturation region, the operation of the circuit can be explained as follows. The first FCS (M_1-M_4) provides two output balanced currents I_{o1} and I_{o2} which are given by Eq. (2) where $v_d = v_x - v_y$. The second FCS (M_5-M_8) provides also two output balanced currents I_{o3} and I_{o4} which are also given by the same Eq. (2).

The currents I_{o1}, I_{o2}, I_{o3}, and I_{o4} are forced to be zero currents and from Eq. (2) we have v_d = 0 and, consequently, $v_x = v_y$ and the voltage at terminal X will follow the voltage at terminal Y. The third FCS is responsible for conveying the X terminal current to the Z terminal. It should be noted that

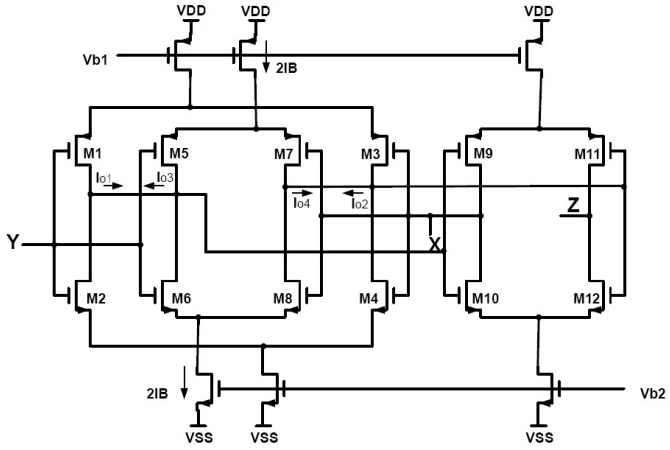


Fig. 2. The proposed accurate wide band FCS based CCII-.

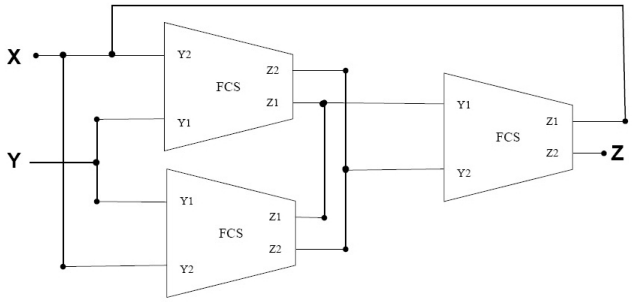


Fig. 3. Block diagram of the circuit shown in Fig.2.

the FCS is used as the only building block in this proposed circuit.

Taking the finite value of the transistor transconductance g_m and drain to source conductance g_d into consideration, the small signal voltage transfer gain from the Y terminal to the X terminal is approximately given by:

$$A_v = \frac{v_x}{v_y} = \frac{1}{1 - \frac{(g_{d3}+g_{d4})(g_{d7}+g_{d8})(g_{d9}+g_{d10})}{(g_{m1}+g_{m2})(g_{m5}+g_{m6})(g_{m9}+g_{m10})}} \tag{6}$$

The small signal input resistance seen at terminal X is approximately given by:

$$r_x = \frac{(g_{d3}+g_{d4})(g_{d7}+g_{d8})}{(g_{m1}+g_{m2})(g_{m5}+g_{m6})(g_{m9}+g_{m10})} \tag{7}$$

The small signal current transfer gain between the X and Z terminals is approximately given by:

$$A_i = \frac{i_z}{i_x} = -\frac{1 + \frac{g_{o1}+g_{do2}}{2(g_{m9}+g_{m10})}}{1 - \frac{g_{o1}+g_{do2}}{2(g_{m9}+g_{m10})}} \tag{8}$$

Where g_{o1} and g_{o2} are the effect of non-ideal current sources in the circuit that will be represented by CMOS transistors and they are equal to the drain to source conductance

of the biasing transistors. The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d11} + g_{d12}} \tag{9}$$

B. Low Power FCS Based CCII-

The novel accurate wide-band FCS based CCII- shown in Fig.2 withdraws large standby currents due to using three FCS. To minimize the power dissipation, only two FCS are used to realize the CCII- in this section. This circuit consumes less power at the expense of lower bandwidth as will be shown in this section. This proposed two FCS based CCII- is shown in Fig.4. The block diagram of this circuit is shown in Fig.5. All the transistors (M_1-M_{12}) are matched. Assuming that all the transistors operate in the saturation region, the operation of the circuit is similar to the proposed CCII- shown in Fig.2. The first FCS (M_1-M_4) provides two output balanced currents that are forced to be zero and from Eq. (2) the voltage at terminal X will follow the voltage at terminal Y. The second FCS is responsible for conveying the X terminal current to the Z terminal. The connection between nodes Y_2 and Z_2 shown in Fig.5 is used to control the input common mode voltage of the current conveying FCS. This is not performed in the circuit shown in Fig.2 since the parallel FCS architecture used for the voltage follower stage helps in controlling it.

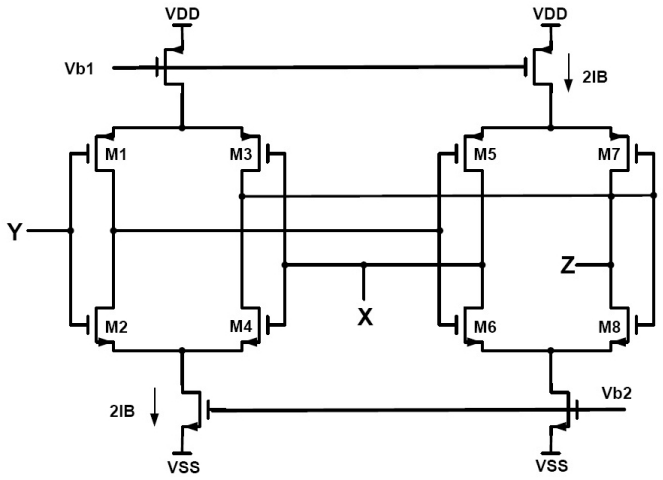


Fig. 4. The low power version of the FCS based CCII-.

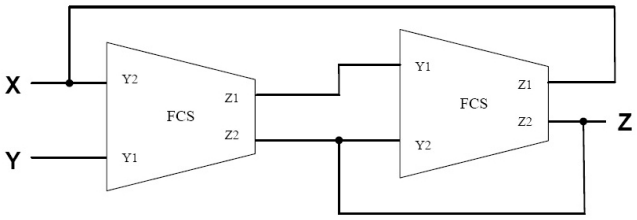


Fig. 5. Block diagram of the circuit shown in Fig.4.

The small signal voltage transfer gain from the Y terminal to the X terminal is approximately given by:

$$A_v = \frac{v_x}{v_y} = \frac{1}{1 - \frac{(g_{d3}+g_{d4})(g_{d5}+g_{d6})}{(g_{m1}+g_{m2})(g_{m5}+g_{m6})}} \tag{10}$$

The small signal input resistance seen at terminal X is approximately given by:

$$r_x = \frac{(g_{d3} + g_{d4})}{(g_{m1} + g_{m2})(g_{m5} + g_{m6})} \tag{11}$$

The small signal current transfer gain between the X and Z terminals is approximately given by:

$$A_i = \frac{i_z}{i_x} = -\frac{1 + \frac{g_{o1}+g_{do2}}{2(g_{m5}+g_{m6})}}{1 - \frac{g_{o1}+g_{do2}}{2(g_{m5}+g_{m6})}} \tag{12}$$

The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d7} + g_{d8}} \tag{13}$$

By using equations (6) and (10), comparing the voltage transfer gain of this low power circuit with the first proposed circuit shown in Fig.2 shows that for the same transistor parameters (i.e, all transistors have the same sizing of 50μm/1μm and I_B=50μA which gives $g_d/g_m \approx 0.03$), the first proposed CCII- exhibits $A_v = \frac{1}{1-(0.03)^3}$ = 1.000027 while the low power version provides a voltage transfer gain of $A_v = \frac{1}{1-(0.03)^2}$ = 1.0009. Therefore, the first proposed CCII- exhibits more accurate voltage following action. Similarly, by using equations (7) and (11), the first proposed circuit input resistance, r_x, is 33.3X lower than that of the low power CCII-. The current transfer gain, A_i and the output resistance is equal r_z are equal for the tow proposed circuits. The main advantage of the second proposed CCII- is its low power consumption since it utilizes only two FCS blocks while the first proposed circuits utilizes three FCS blocks.

III. Comparison with Previous FCS Based CCII- [14]

The CMOS realization of the CCII- proposed in [14] is shown in Fig.6. The input stage is implemented using a simple differential amplifier (M_1-M_5), while the output stage is implemented using the FCS stage (M_6-M_{13}). The block diagram of this two-gain stage configuration is shown in Fig.7. Assuming that each of the groups of the transistors (M_1 and M_2), (M_3 and M_4) as well as (M_6-M_9) are matched and all the transistors operate in the saturation region, the circuit operation can be explained as follows. The structure is based on the long tail differential pair (M_1 and M_2). The current mirror formed by M_3 and M_4 forces equal currents (I_B) in the transistors M_1 and M_2. This operation drives the gate to source voltages of M_1 and M_2 to be equal and, consequently, forces the voltage at terminal X to follow the voltage at terminal Y. The FCS stage is responsible for conveying the X terminal current to the Z terminal.

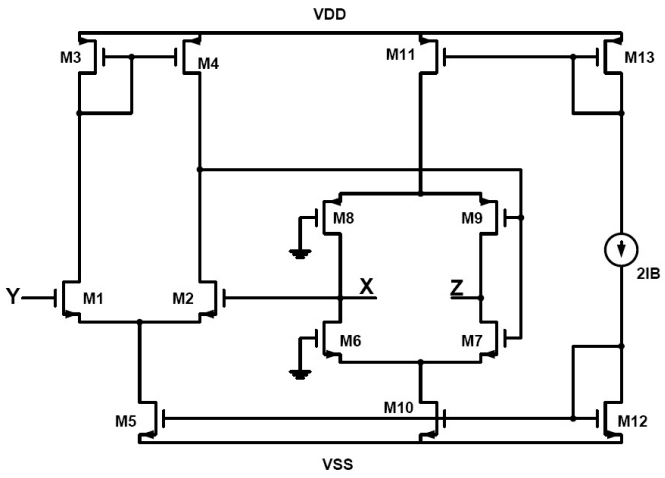


Fig. 6. CCII- realization proposed in [14].

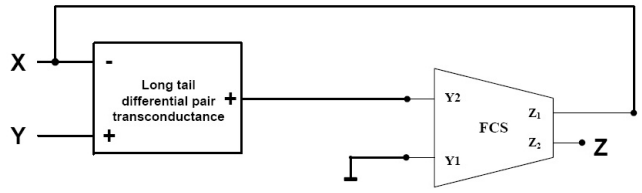


Fig. 7. Block diagram of the circuit shown in Fig.6.

The small signal voltage transfer gain from the Y terminal to the X terminal is given approximately by:

$$A_v = \frac{v_x}{v_y} = \frac{1}{1 - \frac{(g_{d2}+g_{d4})(g_{d6}+g_{d8})}{g_{m2}(g_{m6}+g_{m8})}} \tag{14}$$

The small signal input resistance seen at terminal X is given approximately by:

$$r_x = (\frac{2(g_{d2}+g_{d4})}{g_{m2}(g_{m6}+g_{m8})}) \parallel (\frac{2}{g_{d6}+g_{d8}}) \tag{15}$$

The small signal current transfer gain between the X and Z terminals is given approximately by:

$$A_i = \frac{i_z}{i_x} = -\frac{1 + \frac{g_{d10}+g_{d11}}{2(g_{m6}+g_{m8})}}{1 - \frac{g_{d10}+g_{d11}}{2(g_{m6}+g_{m8})}} \tag{16}$$

The output resistance at terminal Z is given by

$$r_z = \frac{1}{g_{d7}+g_{d9}} \tag{17}$$

By comparing the voltage transfer gain of the CCII- in [14] given in equation (14) with those of the proposed CCII- circuits given in equations (6) and (10), it is evident that the two proposed circuits provide better voltage tracking accuracy than that in [14]. Moreover, the proposed CCII- realizations provide lower input resistance r_x. In addition, the current tracking accuracy and the output resistance r_z are equal in all circuits.

IV. Simulation Results and Discussions

The proposed FCS based CCII- circuits are simulated using equal transistors aspect ratios of 50 μm /1 μm. The biasing current $2I_B$ = 100 μA (Using V_{b1}= 0.12 volts and V_{b2}= 0.59 volts). Simulation results are tabulated in Table 1 and shown for the first proposed circuit in Figs. 8, 9 and 10 while the second proposed circuit simulation results are shown in Figs. 11, 12 and 13.

Table 1: Performance parameters of the circuits shown in Figs.2, 4, and 6

Parameter	The CCII- given in [14]	The first proposed CCII-	The second proposed CCII-	Unit
Input voltage dynamic range	-0.9 to 1	-0.47 to 0.47	-0.9 to 1.02	V
Voltage offset range	4.7 to 5	0 to 0.3	-0.3 to 0.1	mV
A_v (average value) of open circuit voltage transfer gain	1.003245	1.000043	1.001231	V/V
Open loop gain (voltage section)	66	89	83	dB
3-dB Bandwidth of open circuit voltage transfer gain	516	972	578	MHz
Input current dynamic range	-100 to 100	-100 to 100	-100 to 100	µA
Current offset range	0.7 to -6	0	0	µA
A_i (average value) of short circuit current transfer gain	-0.99992	-0.99996	-0.99997	A/A
3-dB Bandwidth of short circuit current transfer gain	22	378	561	MHz
r_x	18.7	3.7	13.4	Ω
Power dissipation	0.79	0.62	0.41	mW

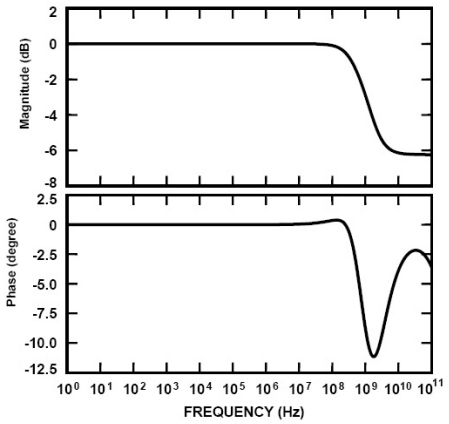


Fig. 8. Frequency characteristics (log scale) of the open circuit voltage transfer gain between Y and X (VX/VY) for the circuit shown in Fig.2.

The CCII- circuit proposed in [14] is also simulated to provide a fair comparison using transistors aspect ratios as reported in Table 2. This CCII- circuit is compensated by using two capacitors C_1 = 5pF (connected between the gate of M_7 and the drain of M_{10}) and C_2 = 5pF (connected between the gate of M_7 and the drain of M_{11}).The biasing current $2I_B$ =

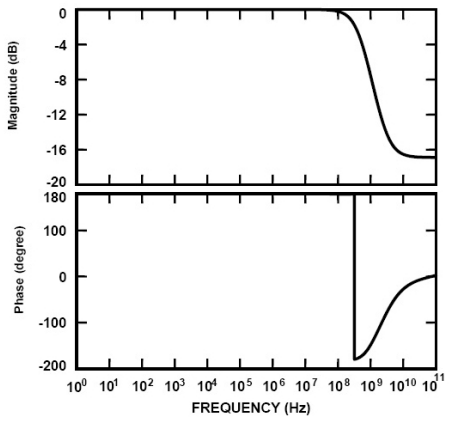


Fig. 9. Frequency characteristics (log scale) of the short circuit current transfer gain between X and Z (IZ/IX) for the circuit shown in Fig.2.

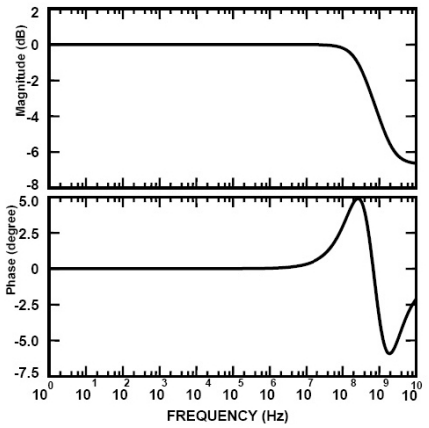


Fig. 11. Frequency characteristics (log scale) of the open circuit voltage transfer gain between Y and X (VX/VY) for the circuit shown in Fig.4.

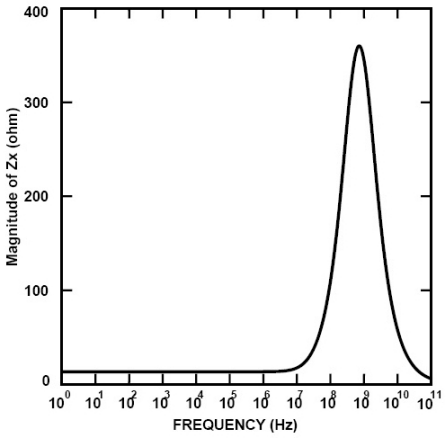


Fig. 10. Input impedance at terminal X versus frequency (log scale) for the circuit shown in Fig.2.

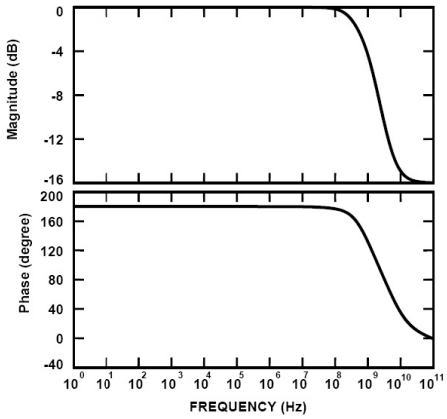


Fig. 12. Frequency characteristics (log scale) of the short circuit current transfer gain between X and Z (IZ/IX) for the circuit shown in Fig.4.

100 μA. Simulation results are tabulated in Table 1 and not shown here due to space limitations.

It is important to note that the FCS reported in [11]-[13] is used as an output current follower stage for the CCII- but the strength of this novel CCII- circuit realization shown in Fig.2 is using the FCS block for both the input voltage follower and the output current follower stages. Moreover, the mismatch between the bias transistors can be controlled through the sizing since the mismatch is inversely proportional to the square root of the transistor gate area [19]. One of the key points of the proposed FCS based circuits is that there are no constraints on the transistor sizes. Hence, the mismatch can be controlled by increasing the transistors sizing under performance metrics constraints.

From Table 1, it is evident that the first proposed circuit exhibits better voltage following accuracy, lower voltage and current offset ranges, and higher open loop gain compared to the circuit reported in [14]. Moreover, the first proposed circuit voltage transfer bandwidth and current transfer bandwidth are 1.9X and 17.2X, respectively, higher compared to the circuit proposed in [14]. In addition, this first proposed circuit has 5X lower input resistance and 1.3X lower power consumption than that of the CCII- reported in [14]. All other parameters are the same with one exception of the input voltage dynamic range which is better in the CCII- introduced in [14].

The low power CCII- provides better performance than the circuit proposed in [14] in all performance parameters while its power consumption is 1.9X lower than that of the CCII- circuit in [14].

This discussions and results show the strength of the proposed circuits in comparison with the only FCS based CCII-, up to the author knowledge. One more advantage of the proposed circuits is that no compensation capacitors are needed in them which allows them to exhibit higher bandwidth than that in [14].

V. Application using the Proposed CCII- (Inverting Current Integrator)

The CCII- has precise unity voltage gain between nodes X and Y as well as precise unity gain between nodes Z and X. Therefore, the CCII- can be used in amplifier applications without any overall negative feedback. The advantage of this approach is that the traditional closed loop gain-bandwidth trade-off of negative feedback operational amplifier is avoided.

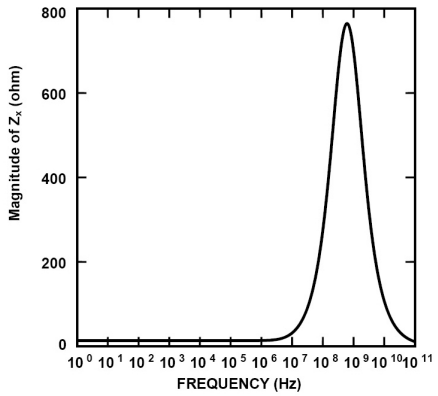


Fig. 13. Input impedance at terminal X versus frequency (log scale) for the circuit shown in Fig.4.

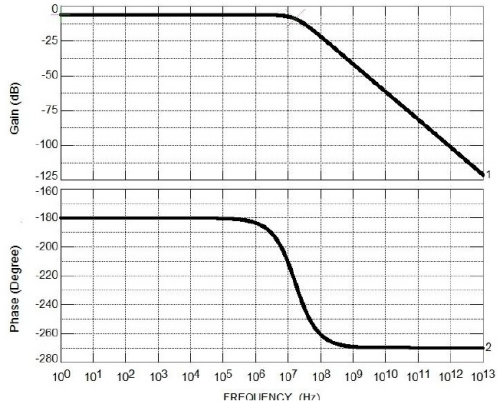


Fig. 15. The gain magnitude (dB) and phase (Degree) of the inverting current integrator shown in Fig. 14.

Table 2: Transistor aspect ratios of the circuit shown in Fig. 6

Transistor	W(μm)/L(μm)
M1,M2, M6-M9	50/1
M3, M4	50/2.5
M5, M10-M13	100/2.5

However, to maintain a high level of accuracy without the use of negative feedback, a high quality CCII- realization should be employed.

Fig.14 shows a simple CCII- based inverting current integrator [1-3]. The resistor R should be fairly small to minimize the stray capacitance at node X. This integrator circuit is simulated using the two proposed CCII- circuits with R=100Ω and C=100pF. Fig.15 shows the current integrator gain and phase versus frequency using the low power CCII- shown in Fig.4. It can be noticed that the cut-off frequency of this integrator circuit is about 16.1 MHz which equals approximately $1/(2\pi RC)$.

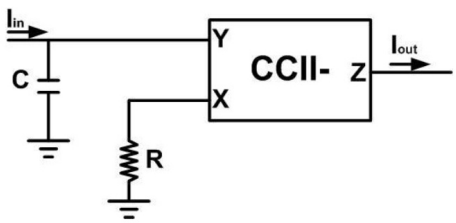


Fig. 14. Simple inverting current integrator as an application for the CCII- shown in Fig. 4.

VI. Conclusion

A novel accurate FCS based CCII- circuit suitable for high frequency applications is given. Simulation results and fair comparisons between the proposed CCII- and the CCII- reported in [14], proved the strength of the proposed circuit realization. Targeting a remarkable reduction in the power dissipation, the low power version of the proposed circuit is also given.

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