Statistical Timing Yield Improvement of Dynamic Circuits Using Negative Capacitance Technique

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***Abstract*—Dynamic logic circuits are considered the best choice for high performance applications due to their relatively high speed. These high performance applications have strict timing constraints. Moreover, process variations create a large variability in the dynamic circuit delay in scaled technologies impacting the timing yield. In this paper, the negative capacitance is adopted, for the first time, for statistical timing yield improvement under process variations. Simulation results show that the adoption of the negative capacitance at the output of a 16-input dynamic NOR gate improves the timing yield by reducing the dynamic circuit delay. In addition, the negative capacitance adoption results in power saving of 10% and reduces the delay variability by 57.6%.**

I. Introduction

The aggressive scaling of CMOS technology towards the nanometer regime has created large statistical variations in the transistor parameters, such as threshold voltage, channel length, and mobility [1-4]. Process variations can be classified as die-to-die (D2D) variations or within-die (WID) variations. In D2D variations, all devices on the same die are assumed to have the same parameters. However, devices on the same die are assumed to behave differently for WID variations [1]. Moreover, the demand for higher performance has moved the clock frequencies up to multi-GHz in microprocessors and other advanced applications. These increased clock frequencies make it necessary to use dynamic circuits which are the best choice for high speed applications [5].

Process variations result in delay variability. Consequently, some of the fabricated circuits do not meet the target delay resulting in timing yield degradation. Consider as an intuitive example, a dynamic circuit that is designed for a specific target delay. Due to random process variations, the delay can be modeled by a normal distribution with the probability density function (pdf) shown in Figure 1. Here, 50% of the total number of dynamic circuits do not meet the desired target delay constraint. Therefore, the dynamic circuits must be designed by using statistical design tools to improve the timing yield. In [6-8], statistical gate sizing tools are used to improve the timing yield. Despite its effectiveness, statistical gate sizing may not achieve the desired timing yield under a given power constraint [6,8].

In this paper, a negative capacitance is added at the output node of a high fan-in (16-input) dynamic NOR gate to reduce its parasitic capacitance, and correspondingly, improve the timing yield without changing the gate sizing. This negative capacitance reduces the dynamic NOR gate delay and power as well. Therefore, it breaks the popular power-performance trade-off. The value of this negative capacitance is determined statistically to achieve the desired timing yield under a given power constraint. The paper is organized as follows: Section II introduces the negative capacitance realization techniques. The statistical timing yield improvement technique using the negative capacitance is proposed in Section III. Simulation results and future work are given in Sections IV and V, respectively. Finally, some conclusions are drawn in Section VI.

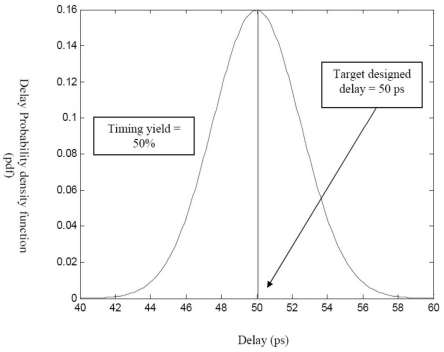

Fig. 1. The delay pdf due to process variations. It shows, intuitively, that up to 50% of dynamic circuits do not meet the target delay (50 ps in this example) [8]

II. Negative Capacitance Realizations

A. Miller Effect Based Realization

The negative capacitance can be realized by using a capacitance C_F connected between the input and output nodes of a non-inverting amplifier with gain A as shown in Figure 2.a. Applying Miller effect on the circuit shown in Figure 2.a results in the equivalent circuit shown in Figure 2.b. The input capacitance to this circuit, C_{NEG} is given by:

$$C_{NEG} = C_F\ (1 - A) \tag{1}$$

Therefore, when the amplifier gain A is larger than unity, C_{NEG} takes on negative values and a negative capacitance is realized. An implementation of this Miller effect based negative capacitance circuit is introduced in [9] and shown in Figure 3. For example, if C_{NEG} = -2fF is desired, then A=2 requires that C_F = 2fF. The gain, A, of the circuit shown

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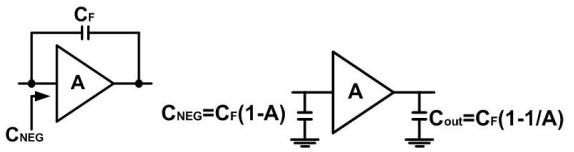


(a) (b)

Fig. 2. (a) The negative capacitance implementation using a non-inverting amplifier with a feedback capacitance and (b) The Miller equivalent circuit of (a) [9].

in Figure 3, when transistors M_1 and M_2 are matched, is given by [9]:

$$A \approx \frac{g_{m1}}{2g_{m3}} \tag{2}$$

where g_{m1} and g_{m3} are the transconductance gain of transistors M_1 and M_3, respectively. Therefore, the gain, A, can be varied by changing the sizes of transistors M_1 and M_3.

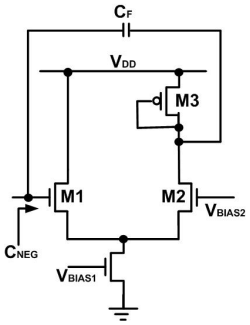


Fig. 3. Miller effect based negative capacitance circuit realization [9].

B. Negative Impedance Converter (NIC) Based Realization

The Negative Impedance Converter (NIC) is a two-port circuit whose input impedance is the negative of the load impedance at its output port as shown in Figure 4 [10]. When the NIC circuit is loaded with a capacitance C_L at its output node, an equivalent negative capacitance is seen at the input node, and therefore, a negative capacitance is realized. The value of this negative capacitance, C_{NEG}, is given by:

$$C_{NEG} = -\beta\ C_L \tag{3}$$

where β is a constant dependent on the NIC circuit implementation. One simple implementation of the NIC circuit is given in [10] and shown in Figures 5.a and 5.b. This implementation is based on the positive second generation current conveyor (CCII+) [10,11]. The constant β is given by [10]:

$$\beta = (1 - \varepsilon_v)\ (1 - \varepsilon_i) \tag{4}$$

where ε_v is the error in conveying the voltage at node Y to node X and ε_i is the error in conveying the input current at node X to node Z.

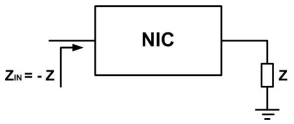
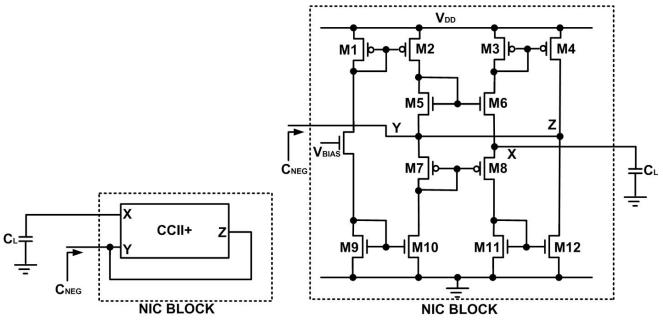


Fig. 4. NIC based negative capacitance implementation [10].



(a) (b)

Fig. 5. (a) The NIC based negative capacitance realization using CCII+ and (b) The circuit realization of this negative capacitance [10].

III. Statistical Timing Yield Improvement using Negative Capacitance

Assuming that the dynamic circuit is designed such that the nominal delay is the target delay, A_o (this can be performed at any design corner). The circuit delay, A_o, can be given by [5]:

$$A_o = \zeta\ C_{out} \tag{5}$$

where ζ is a proportionality constant dependent on the output resistance of the circuit and C_{out} is the circuit parasitic output capacitance.

Due to process variations, this circuit delay is normally distributed around this nominal value. Therefore, the resulting timing yield is ∼50%. It should be noted that the impact of process variations on C_{out} can be neglected with respect to its impact on the output resistance. This is because the output resistance depends on the transistors threshold voltage which is the main source of variability (due to Random Dopant Fluctuations (RDF)) [1,2]. In order to improve the timing yield, the delay variability which is centered around A_o is shifted to a new center $A_o^{'}$. where $A_o^{'}$ is given by [8]:

$$A_o^{'} = A_o - n\ \sigma \tag{6}$$

where σ is the standard deviation of the delay variability and "n" is dependent on the desired timing yield, Y_o, and is obtained from the normal distribution tables. For example, if the desired timing yield is 99.87% (Y_o = 99.87%), "n" equals 3.0 from the normal distribution tables. Figure 6 illustrates how the timing yield is improved by shifting the delay pdf to a shorter mean delay $A_o^{'}$. In [6-8], the circuit delay, A_o, is reduced to $A_o^{'}$ by using gate sizing. This technique may fail in achieving the required timing yield with acceptable power overhead, and therefore, many iterations are required. In this paper, the delay, A_o, is reduced by adding a negative

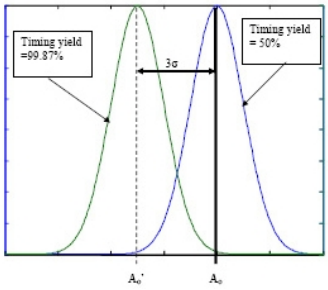


Fig. 6. The timing yield improvement is obtained by shifting the delay pdf center from A_o to $A_o^{'}$

capacitance at the output node. Therefore, the proposed negative capacitance technique requires no iterations and gives more degrees of freedom to achieve the desired timing yield with acceptable power overhead. The addition of the negative capacitance, C_{NEG}, at the circuit output node results in a modified output capacitance, $C_{out}^{'}$, which is given by:

$$C_{out}^{'} = C_{out} + C_{NEG} \tag{7}$$

and accordingly, the modified circuit delay, $A_o^{'}$, is given by:

$$A_o^{'} = \zeta \; C_{out}^{'} \tag{8}$$

By using equations (3-6), the negative capacitance, C_{NEG}, that achieves the desired timing yield improvement, is given by:

$$C_{NEG} = \frac{-\; n \; \sigma}{\zeta} \tag{9}$$

This negative capacitance, C_{NEG}, can be realized by using the Miller effect or the NIC methods discussed in Section II. If the Miller effect method is selected, the designer can select the design values of C_F and the non-inverting amplifier gain A. In addition, there are several implementations to realize the non-inverting amplifier which provide more design flexibility. Also, if the NIC method is chosen, there exist several NIC implementations. All these design flexibilities allow the dynamic circuit designer to trade-off the required timing yield improvement with the associated power and area overheads.

IV. Simulation Results and Discussions

In this section, a 16-input dynamic NOR gate, shown in Figure 7, is chosen to verify the proposed timing yield improvement technique. This high fan-in dynamic NOR gate is prefered in high speed applications since its propagation delay is increasing linearly with fan-in [12]. The NOR gate is designed to achieve a nominal high-to-low delay (A_o) of 102.4 psec and an average power dissipation of 23.34 μW. The inputs X2 to X16 are at logic "0" while the input X1 is changing from logic "0" to logic "1". The total capacitance at the output node of the NOR gate, C_{out}, is calculated to be 9.38 fF. Therefore, the constant ζ, defined in equation (5), equals 10.92 psec/fF. Monte Carlo analysis with 5000 points is conducted by using an industrial hardware-calibrated statistical 65-nm CMOS model. A typical histogram of the NOR gate delay is shown in Figure 8.a. The standard deviation of the NOR gate delay (σ) is 10.61 psec. Accordingly, $A_o^{'}$ = 70.57 psec for a timing yield Y_o = 99.87% (i.e., "n" = 3.0). Thus, the required value of the negative capacitance, C_{NEG}, to achieve the desired timing yield is obtained from equation (9) and equals - 2.915 fF. This negative capacitance can be realized by using the Miller effect or the NIC methods. In this

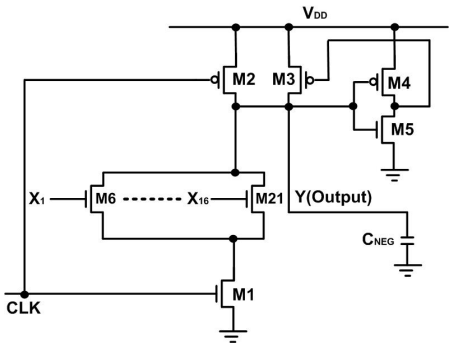
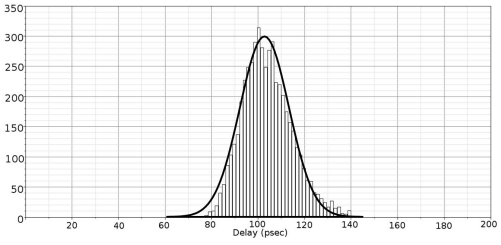
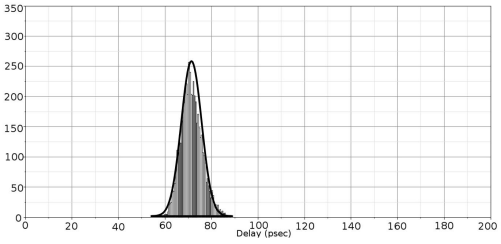


Fig. 7. 16-input dynamic NOR gate circuit with a negative capacitance employed at its output node.



(a)



(b)

Fig. 8. Delay histogram for the 16-input dynamic NOR gate using Monte Carlo Analysis (a) Before employing the negative capacitance (μ= 102.4 psec and σ= 10.61 psec) and (b) After employing the negative capacitance (μ= 70.6 psec and σ= 4.5 psec).

section, the negative capacitance is realized using the circuit shown in Figure 3 with C_F = 1 fF and A = 3.9. Monte Carlo analysis is conducted again and a typical histogram of the NOR gate delay is shown in Figure 8.b. It is evident from Figure 8.a and Figure 8.b that the negative capacitance technique shifts the delay pdf as required. Figure 8.b shows that all the dynamic circuits samples have a delay less than the

target delay of 102.4 psec. Moreover, it is found that the power dissipation is reduced from 23.34 μW to 21 μW (10% power saving). This power reduction is because reducing the output capacitance results in reducing the dynamic power. In addition, the adoption of the negative capacitance reduces the delay variability. The delay standard deviation is reduced from 10.61 psec to 4.5 psec (57.6% variability reduction). The reason for this standard deviation reduction can be explained analytically by recalling equations (5) and (8). From equation (5), the delay A_o variability, $\Delta A_o = \Delta\zeta\ C_{out}$, and from equation (8), the delay A'_o variability, $\Delta A'_o = \Delta\zeta\ C'_{out}$, assuming that the capacitances, C_{out} and C'_{out} are constants from variability perspective. From equation (7), $C'_{out} < C_{out}$ as C_{NEG} has a negative value. Therefore, $\Delta A'_o < \Delta A_o$ which explains why the adoption of the negative capacitance reduces the delay variability. It should be noted that the negative capacitance, C_{NEG}, exhibits some variations due to its circuit realization. However, this variations is found to be less than the parameter ζ variability by a factor of 7X. Also, the negative capacitance is realized by using the NIC based method shown in Figure 5. However, these results are not shown in this paper due to space limitations.

V. Design Considerations and Future Work

A. Stability

One of the important drawbacks of using the negative capacitance is that it affects the circuit stability. This stability problem arises when $|C_{NEG}| \geq C_{out}$. Fortunately, this happens only when the delay, A'_o, is negative which is unreasonable.

B. The C_{NEG} Circuit Power Consumption

In Section IV, the negative capacitance is realized directly by using the Miller effect and the NIC based methods without minimizing the associated power overhead. However, for a given power budget, the architecture and design of the amplifier circuit (used in the Miller effect method) or the NIC circuit can be changed to achieve the desired timing yield within the available power budget. The optimization of the negative capacitance circuit is an open research topic for further future work.

C. Adaptive Negative Capacitance

The negative capacitance technique introduced in this paper is used at the design cycle and before any circuit fabrication. This method can be used adaptively after fabrication by using the block diagram shown in Figure 9. In this figure, if the circuit delay exceeds a target delay, the control circuit output adjusts the value of the negative capacitance to reduce the circuit delay adaptively (Online). This adaptive negative capacitance is currently under research considering its power and area overheads and stability.

VI. Conclusion

The negative capacitance technique has been shown to reduce the effects of process variations on dynamic circuits. The adoption of a negative capacitance at the output node of a 16-input dynamic NOR gate improves the timing yield ($>$ 99.9%), reduces the dynamic circuit power dissipation by 10%, and results in reducing the delay variability by 57.6%. These results are promising for scaled CMOS technologies since the popular power-performance trade-off can be broken by using the proposed negative capacitance technique.

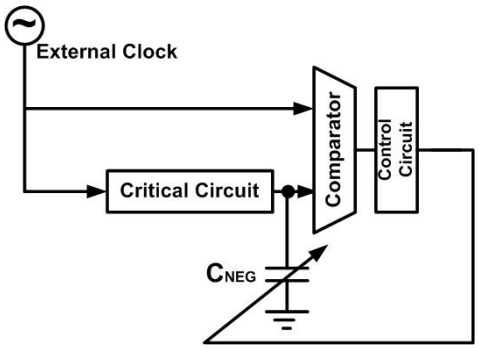


Fig. 9. The proposed adaptive negative capacitance technique for timing yield improvement

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