Analytical Soft Error Models Accounting for Die-to-Die and Within-Die Variations in Sub-Threshold SRAM Cells

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***Abstract*—Sub-threshold SRAM cells are attractive because of their low leakage power and low access energy. However, the susceptibility of sub-threshold SRAM cells to soft errors is high due to their low supply voltage, high density, and shrinking geometry. Moreover, the increase in statistical variations in advanced nanometer CMOS technologies poses a major challenge for sub-threshold circuits designers. In this paper, analytical models for the sub-threshold SRAM critical charge variations, which account for both die-to-die (D2D) and within-die (WID) variations, are proposed. The derived models are then compared with Monte Carlo simulations by using industrial hardware-calibrated 65-nm CMOS technology. This paper also provides novel design insights such as the impact of the coupling capacitor, one of the most common soft error mitigation techniques, on the critical charge variability. In addition, it demonstrates that the relative critical charge variability is minimum at a certain temperature value. Then, the circuit designer can employ these results with temperature control techniques to minimize the critical charge variability in the early design cycles, especially, for applications with strict soft error rate (SER) constraints. In addition, the proposed models show that the device sub-threshold swing coefficient can be optimized to minimize the relative critical charge variability.**

***Index Terms*—Circuit modeling and optimization, critical charge, process variation, soft error rate (SER), sub-threshold SRAM.**

I. Introduction

SUB-THRESHOLD digital circuit design is one of the best energy saving techniques for applications with strict energy constraints [1]–[7]. Static Random Access Memory (SRAM) cells comprise a significant percentage of the total area of many digital chips [8], [9]. For this reason, SRAM cells leakage power dominates the total leakage power of the chip. Moreover, the large switched capacitances in the SRAM cells bit-lines and word-lines increase the SRAM cells access energy [8], [9]. The design of sub-threshold SRAM cells reduces both leakage power and access energy. In addition, sub-threshold SRAM cells operate at sub-threshold voltages that are compatible with the sub-threshold logic to allow system integration [2]. However, reliability and process variations are the main design challenges for sub-threshold SRAM cells [1].

Reliability is the first significant design challenge in the design of sub-threshold SRAM cells. Shrinking geometries, lower power supply, and higher density circuits all have a great impact on reliability [10]–[16]. As CMOS technology further scales, soft errors become one of the major reliability concerns. Soft errors are caused by two types of radiation: 1) alpha particles emitted by radioactive impurities in integrated circuits (ICs) and package materials and 2) high energy neutrons resulting from the interaction between cosmic rays and the earth's atmosphere [12], [13]. When an alpha particle hits a silicon substrate, the particle generates electron-hole pairs as it passes through the p-n junctions. Though a neutron does not ionize the material directly, the neutron does collide with nuclei, resulting in secondary charged nuclear fragments, capable of inducing electron-hole pairs.

The generated charges are transported to circuit nodes by drift and diffusion mechanisms, causing a current pulse that disturbs the node voltage and can lead to soft errors [11]. In memory elements, this disturbance can result in bit flips (0-to-1 flip or 1-to-0 flip) which can corrupt the logic state of the circuit. However, in combinational circuits, this disturbance brings about a temporary change in the output node voltage. This temporary change is tolerated, unless it is latched by a succeeding memory element. For memory elements such as SRAM cells and flip-flops, if the charge, collected by the particle strike at the storage node, is more than a minimum value, the node is flipped and a soft error occurs. This minimum value is called a critical charge (Q_{critical}), which can be used as a measure of the memory element vulnerability to soft errors [11], [14], [16]–[19].

This critical charge, Q_{critical}, exhibits an exponential relationship with the soft error rate (SER) [11], and consequently, Q_{critical} should be designed high enough to limit the SER. It should be pointed out that estimating the value of Q_{critical} does not give the absolute value of the SER, since the SER depends on other parameters such as the particle strike type, energy, striking angle, and track length through the Silicon substrate. However, knowing the value of Q_{critical} provides an estimate of the soft errors susceptibility of the circuit and can be used to further estimate the SER. In particular, sub-threshold SRAM cells are vulnerable to soft errors due to their lower supply voltages and node capacitances. Therefore, soft errors investigation and modeling in sub-threshold SRAM cells becomes of paramount importance.

In future technologies, process variations are expected to worsen due to difficulties with printing nanometer scale ge-

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ometries in standard lithography. Therefore, these variations are considered the second design challenge for sub-threshold SRAM cells designers [20]–[25]. Process variations are classified as die-to-die (D2D) variations and within-die (WID) variations. In D2D variations, all the devices on the same die are assumed to have the same parameters values. However, the devices on the same die are assumed to behave differently in WID variations [20]. Although the D2D variations are originally considered the primary source of process variations, the WID variations are posing the major design challenge as technology scales [21], [22]. Due to these process variations, the critical charge has variations around its nominal value. These critical charge variations pose a challenge to sub-threshold SRAM cells designers, particulary in applications with strict SER constraints.

Recently, researchers have attempted to calculate the critical charge nominal value and address the impact of process variations on the critical charge in super-threshold memory elements such as SRAM cells and flip-flops. However, most of this research utilize Monte Carlo analysis tools [10], [26]–[28] which are time consuming and provide few design insights. Moreover, these Monte Carlo analysis tools are not scalable with CMOS technology because Monte Carlo analysis has to be conducted for each new technology node to calculate the critical charge variability. However, the analytical models can be adopted to predict the critical charge variability for future technology nodes without performing any simulations.

In [29], an analytical model is presented to estimate the critical charge for super-threshold SRAM cells. Despite the accuracy of this model in estimating the critical charge, this model depends mainly on SPICE simulations and can be used only for D2D variations as discussed in Section II-A. These D2D variations are estimated by applying traditional techniques (such as corner-based and worst-case analysis) that have been already performed in [29]. These techniques, though, tend to be inefficient, and completely pessimistic in the presence of relatively large variations. Therefore, statistical design-oriented techniques are required, especially for the WID variations [30]. According to the literature, an analytical model of the critical charge and its variability for sub-threshold SRAM cells has not been attempted before.

In this paper, a reference analytical model of sub-threshold SRAM critical charge, accounting for both D2D and WID variations, is proposed. This model is further approximated to provide more design insights on the impact of process variations on the critical charge. The derived model is simple and scalable in terms of technology scaling. Moreover, the model is explicitly dependent on design parameters such as node capacitance, transistors sizing, transistor parameters, temperature, and supply voltage. The results are compared to SPICE transient simulations, Monte Carlo simulations, and an industrial hardware-calibrated 65-nm CMOS technology transistor model is adopted in these comparisons. These results are particularly relevant in the design of nanometer technology when WID variations dominate the process variations [22].

The rest of this paper is organized as follows. In Section II, the reference model assumptions and derivations are proposed for both the nominal critical charge value and its variability. This reference model is further approximated in Section III to provide some design insights to circuit designers. The two proposed models are compared with SPICE transient and Monte Carlo simulations in Section IV. In Section V, the design insights, extracted from the proposed models, are discussed. Finally, some conclusions are drawn in Section VI.

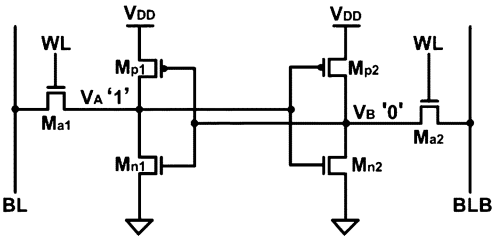


Fig. 1. Conventional super-threshold 6T SRAM cell.

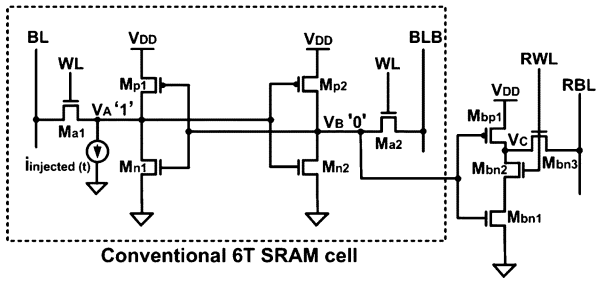


Fig. 2. Sub-threshold 10T SRAM cell which consists of a conventional 6T SRAM cell and an extra read buffer to improve the noise margins [2]. In this 10T sub-threshold SRAM cell, the particle strike is modeled by a current pulse source ($i_{\mathrm{injected}}(t)$). V_A is assumed to be at logic "1" and V_B is assumed to be at logic "0".

II. Reference Model Assumptions and Derivations

Fig. 1 depicts the conventional six transistor (6T) SRAM cell. It consists of two cross-coupled inverters that store two complementary logic values "1" and "0" at their output nodes, V_A and V_B. This 6T SRAM cell shown in Fig. 1 cannot be used in the sub-threshold operation due to poor noise margins and is limited to the super-threshold operation [2], [4]. Therefore, several SRAM cells are reported in the literature to overcome the poor noise margins problem by adding extra transistors. For example, the 10T SRAM cell shown in Fig. 2 has four extra transistors implementing a read buffer that isolates the reading and writing ports [2]. Thus, the WL, BL, and BLB lines are used for the writing operation whereas the RWL and RBL are used for the reading operation. Most of the sub-threshold SRAM cells reported in the literature utilize the same two port cell topology [4], [50]–[52]. The core of these sub-threshold SRAM implementations is the two cross-coupled inverters. These two cross-coupled inverters used in the sub-threshold SRAM cells might be designed asymmetrically to improve the noise margins.

The conventional SRAM cell shown in Fig. 1 has its highest susceptibility to particle strikes in the standby mode because the storage nodes are disconnected from the highly capacitive bitlines [29]. However, the sub-threshold SRAM cell shown in Fig. 2 has its highest susceptibility to particle strikes when in

the reading mode or the standby mode. This is because in both reading and standby modes, the storage nodes are disconnected from the highly capacitive bitlines. The buffer node V_C is driven by V_B and is connected to the highly capacitive RBL during the reading operation. Thus, V_C is less susceptible to particle strikes than V_A and V_B.

Accordingly, only the storage nodes V_A and V_B are considered in the following analysis. Thus, the access transistors, M_{a1} and M_{a2}, and the read buffer extra transistors, M_{bn1}, M_{bn2}, M_{bn3}, and M_{bp1} are excluded from the analysis. Assume that V_A stores logic "1" and accordingly V_B stores logic "0". Thus, transistors, M_{p1} and M_{n2}, are conducting more sub-threshold currents than transistors, M_{n1} and M_{p2}, to maintain V_A and V_B voltages, respectively.

In the super-threshold 6T SRAM cell design, the pMOS pull-up transistors are designed to be weaker than the nMOS pull-down transistors for proper operation. Consequently, the data node storing logic "1" (V_A in Fig. 1) is the most susceptible to particle strikes [31]. Therefore, super-threshold SRAM critical charge modeling considers only the 1-to-0 flipping case and ignores the 0-to-1 flipping case [29]. However, this assumption cannot be applied in the sub-threshold SRAM cell, because the nMOS transistor might become the weaker transistor, depending on the sizing and the technology parameters. In the sub-threshold region, the sub-threshold current is modeled as [32], [33]

$$i_{\text{sub}} = i_o \exp\left(\frac{V_{GS} - V_t}{nV_T}\right)\left[1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right] \quad (1)$$

where

$$i_o = \mu_o C_{ox}\left(\frac{W}{L}\right)(V_T)^2 \exp(1.8) \quad n = 1 + \frac{3T_{ox}}{W_{dm}}, \quad V_T = \frac{KT}{q} \quad (2)$$

where V_{GS} and V_{DS} are the transistor gate-to-source and drain-to-source voltages, respectively, V_t is the transistor threshold voltage, μ_o is the zero bias mobility, C_{ox} is the gate oxide capacitance, n is the sub-threshold swing coefficient, T_{ox} is the gate oxide thickness, W_{dm} is the maximum depletion layer width, V_T is the thermal voltage, K is the Boltzman constant, T is the temperature in degrees Kelvin, q is the electron charge, and W and L are the transistor channel width and length, respectively.

Therefore, the ratio between transistors M_{n2} and M_{p1} currents is given by (calculated when $V_A = V_B = V_{\text{DD}}/2$)

$$\frac{i_{n2_{\text{sub}}}}{i_{p1_{\text{sub}}}} = \frac{\mu_n\left(\frac{W}{L}\right)_{n2}}{\mu_p\left(\frac{W}{L}\right)_{p1}} \exp\left(\frac{|V_{tp1}| - V_{tn2}}{nV_T}\right). \quad (3)$$

In typical CMOS technologies, the pMOS transistor threshold voltage, $|V_{tp}|$, and mobility, μ_p, are lower than V_{tn} and μ_n, the nMOS transistor threshold voltage and mobility, respectively [34]. Thus, if the ratio, $\mu_n(W/L)_{n2}/\mu_p(W/L)_{p1}$, is much less than $\exp((V_{tn2} - |V_{tp1}|)/nV_T)$, the nMOS transistor, M_{n2}, will be weaker than the pMOS transistor, M_{p1}, and the data node storing logic "0" (V_B in Fig. 2) is the most susceptible to particle strikes. Therefore, in sub-threshold SRAM critical charge modeling, the most susceptible node to particle strikes must be determined in advance. Sometimes, the critical charge values for the 1-to-0 flip and 0-to-1 flip cases are comparable, and both should be modeled and investigated.

A. Critical Charge Model

In the following analysis, the first case when the ratio, $\mu_n(W/L)_{n2}/\mu_p(W/L)_{p1}$, is much larger than $\exp((V_{tn2} - |V_{tp1}|)/nV_T)$ is investigated. Here, V_A is more susceptible to particle strike than V_B. The other case, when V_B is more susceptible to particle strike, is addressed later in this section. The particle strike is modeled by a double exponential current pulse (connected at node V_A in Fig. 2) and given by [35]

$$i_{\text{injected}}(t) = \frac{Q}{\tau_f - \tau_r} \times [\exp(-t/\tau_f) - \exp(-t/\tau_r)] \quad (4)$$

where Q is the total charge deposited by this current pulse at the struck node, and τ_f and τ_r are the falling time and the rising time constants, respectively [35]. Although several current pulse waveforms are reported in [11], the current pulse waveform in (4) has the advantage of being accurate and simple for the proposed analytical model. Typically, for a particle induced current pulse, τ_f is much larger than τ_r [11], [29]. Based on this fact and for model simplicity, (4) is approximated as a single exponential current pulse as given in the following equation:

$$i_{\text{injected}}(t) \approx \frac{Q}{\tau} \times \exp(-t/\tau) \quad (5)$$

where τ is equal to τ_f in (4). It should be emphasized that the current pulse parameter, τ, models the device's response to the particle strike. As a result, τ is very sensitive to the physical conditions of the particle strike event such as the particle energy, the particle strike angle, the particle track length through the Silicon substrate, and the location of the particle track with respect to the reverse biased p-n junctions [35]. For example, the current pulse expressed in (5) can have a varying pulse width, τ, from a few picoseconds to hundreds of picoseconds. The narrow current pulse represents the worst-case situation, because the critical charge, Q_{critical}, is minimal. This narrow current pulse corresponds to an event in which the track of an ionized particle intersects the drain of the nMOS transistor in the OFF-state (such as M_{n1} in the analyzed case) and therefore, passes in the proximity of the reverse biased p-n junction. This means that the charge collection mechanism is dominated by the drift current, due to local electric fields in the reverse biased p-n junction, in a very short time. However, the charge collection mechanism is dominated by the diffusion current in the events in which the particle track does not intersect the drain [11]. Theoretical studies showed that, typically, 80%–90% of the neutron induced SER is represented by the events in which the current pulse is relatively wide [11], [46]. Such a discussion demonstrates that both narrow and wide current pulses must be considered in the Q_{critical} calculations. Therefore, the simulation results presented in Section IV considers the value of Q_{critical} and its variability for different values of τ.

The nodal current equation at node V_A is written as

$$C_A \frac{dV_A}{dt} = [i_{p1_{\text{sub}}} - i_{n1_{\text{sub}}}] - i_{\text{injected}}(t) \quad (6)$$

where C_A is node V_A capacitance; $i_{p1_{\text{sub}}}$ is the sub-threshold restoring current of the pMOS transistor, M_{p1}, which tries to

pull-up V_A to the supply voltage ($V_{\rm DD}$); $i_{n1_{\rm sub}}$ is the nMOS transistor, M_{n1}, sub-threshold current; and $i_{\rm injected}(t)$ is the injected current pulse given in (5).

From (6), the values of Q and τ that equalize $[i_{p1_{\rm sub}} - i_{n1_{\rm sub}}]$, and $i_{\rm injected}(t)$ currents are obtained. Hence, V_A voltage attains a certain minimum value $V_{\rm min}$. The time at which $V_{\rm min}$ occurs is denoted by $t_{\rm min}$ and given by

$$t_{\rm min} = \tau \ln\left(\frac{Q}{\tau\left[i_{p1_{\rm sub}} - i_{n1_{\rm sub}}\right]}\right). \tag{7}$$

By solving the differential equation in (6) and using (7), The value of $V_{\rm min}$ is given by

$$V_{\rm min} = V_{\rm DD} - \frac{1}{C_A}\left(Q - \left[i_{p1_{\rm sub}} - i_{n1_{\rm sub}}\right]\left[t_{\rm min} + \tau\right]\right). \tag{8}$$

The subthreshold currents, $i_{p1_{\rm sub}}$ and $i_{n1_{\rm sub}}$, are given by (assuming $V_B \approx 0$)

$$\begin{aligned} i_{p1{\rm sub}} &= i_{p1o}\exp\left(\frac{V_{\rm DD} - |V_{tp1}|}{nV_T}\right) \\ &\quad \times \left[1 - \exp\left(\frac{-(V_{\rm DD} - V_A)}{V_T}\right)\right] \\ i_{n1{\rm sub}} &= i_{n1o}\exp\left(\frac{-V_{tn1}}{nV_T}\right)\left[1 - \exp\left(\frac{-V_A}{V_T}\right)\right] \end{aligned} \tag{9}$$

where

$$\begin{aligned} i_{p1o} &= \mu_p C_{ox}\left(\frac{W}{L}\right)_{p1}(V_T)^2\exp(1.8) \\ i_{n1o} &= \mu_n C_{ox}\left(\frac{W}{L}\right)_{n1}(V_T)^2\exp(1.8). \end{aligned} \tag{10}$$

Since V_A changes from $V_{\rm DD}$ to $V_{\rm min}$ over the time interval $[0, t_{\rm min}]$, the currents $i_{p1_{\rm sub}}$ and $i_{n1_{\rm sub}}$ vary during the same time interval. In order to simplify the solution of the differential equation in (6), the currents, $i_{p1_{\rm sub}}$ and $i_{n1_{\rm sub}}$, are averaged over this time interval and are considered constants. Furthermore, $V_{\rm DD}$ and $V_{\rm min}$ are assumed to be greater than $3V_T$ ($\approx$75 mV at room temperature). Therefore, the term $[1 - \exp(-V_A/V_T)] \approx 1$ and the term, $[1 - \exp(-(V_{\rm DD} - V_A)/V_T)]$, is averaged over the time interval $[0, t_{\rm min}]$. This average value is denoted by β_1 and given by

$$\begin{aligned} \beta_1 &= \frac{1}{V_{\rm DD} - V_{\rm min}}\int_{V_{\rm min}}^{V_{\rm DD}}\left[1 - \exp\left(\frac{-(V_{\rm DD} - V_A)}{V_T}\right)\right]dV_A \\ &\approx 1 - \frac{V_T}{V_{\rm DD} - V_{\rm min}}. \end{aligned} \tag{11}$$

The model in [29] calculates Q, the total charge deposited at the struck node to cause a bit flip, by iteratively increasing Q by a small amount ($\sim$0.001 fC) in SPICE until the node voltages flip. Accordingly, the model in [29] depends mainly on SPICE transient simulations since it has no analytical formula for Q and determines Q iteratively using SPICE transient simulations. In addition, for D2D variations modeling using corner-based analysis, the value of Q can be obtained using SPICE transient simulations at the specified corner. This D2D variations modeling has been already performed in [29]. However, if the model in [29] is adopted for WID variations modeling, the value of Q has to be determined for each statistical run (since each statistical run has its own parameters variations). This seems to be inefficient and time consuming since a large number of statistical runs is usually required (10 000 runs). Therefore, the missing analytical formula for Q makes [29] unsuitable to model WID variations analytically. The proposed model provides an analytical formula for Q in the preceding derivations and can be used to model the D2D and WID variations analytically without performing any SPICE simulations.

In this proposed model, it is assumed that once V_A voltage hits its minimum value $V_{\rm min}$, the restoring current of the pMOS transistor, M_{p1}, causes V_A voltage to either recover to logic "1" and no flipping occurs, or flip to logic "0" and flipping occurs. This assumption is justified by noting that after the time $t_{\rm min}$, the injected current, $i_{\rm injected}(t)$, continues to decay exponentially. Consequently, the goal is to find the condition on the restoring current, $i_{p1{\rm sub}}$, that causes V_A to flip. This restoring current is controlled by its gate voltage, V_B. Accordingly, if V_B is rising, the source-to-gate voltage of M_{p1} decreases, and correspondingly, the restoring current decreases resulting in a soft error. Likewise, if V_B is falling, the restoring current increases, and correspondingly, V_A voltage recovers and no flipping occurs.

Due to the fact that the inverter switching voltage (V_M) is defined as the threshold between logic "1" and logic "0" (i.e., when the inverter input slightly exceeds V_M, the inverter output is assumed to be at logic "0" and vice versa). If $V_{\rm min}$ is slightly below the switching voltage of the second inverter, V_{M2}, V_B rises to logic "1", decreasing the restoring current, and resulting in a soft error. V_M is obtained by equating the inverter pMOS and nMOS subthreshold currents, assuming that the input and output voltages equal V_M. Thus, V_M is given by (assuming V_M and $(V_{\rm DD} - V_M) \geq 3V_T$)

$$V_M = \frac{1}{2}\left[V_{\rm DD} - |V_{tp}| + V_{tn} + nV_T\ln\left(\frac{i_{po}}{i_{no}}\right)\right]. \tag{12}$$

Now, for the flipping case (i.e., $V_{\rm min} < V_{M2}$), V_B voltage is assumed to stay around 0 V for the time interval over which V_A is approaching $V_{\rm min}$ (i.e., $t_{\rm min}$), and then starts to rise. Furthermore, V_A is assumed to remain constant at $V_{\rm min}$, until V_B rises and exceeds the switching threshold of the first inverter, V_{M1}. These assumptions are summarized in the following equation [29]:

$$\text{for } 0 \leq t \leq t_{\rm min}\begin{cases} V_A(t) : V_{\rm DD} \rightarrow V_{\rm min} \\ V_B(t) \approx 0V \end{cases}$$

and

$$\text{for } t_{\rm min} \leq t \leq t_f\begin{cases} V_A(t) \approx V_{\rm min} \\ V_B(t) : 0V \rightarrow V_{M1} \end{cases} \tag{13}$$

where t_f is the flipping time at which V_B hits V_{M1}. This assumption is validated by noticing that once V_B hits V_{M1}, the positive feedback of the cell becomes strong enough to continue flipping the cell state. Equation (13) allows decoupling the cross-coupled inverters of the SRAM cell, as proposed in [29].

From (8) and for a given τ, the value of Q that just cause V_A to flip is obtained by equating $V_{\min}$ with V_{M2}. As a result, Q is determined by

$$Q = C_A(V_{\rm DD} - V_{M2}) + [i_{p1_{\rm sub}} - i_{n1_{\rm sub}}]\,[t_{\min} + \tau]. \quad (14)$$

By substituting (14) in (7), $t_{\min}$ is calculated by solving the following equation:

$$t_{\min} = \tau \ln(\gamma + t_{\min}/\tau) \quad (15)$$

where

$$\gamma = 1 + \frac{C_A(V_{\rm DD} - V_{M2})}{\tau\,[i_{p1_{\rm sub}} - i_{n1_{\rm sub}}]}. \quad (16)$$

Equation (15) is a nonlinear equation that is solved numerically by using the Lambert W function (also called the Omega function), $\Omega(x)$ [36]. A more detailed definition of $\Omega(x)$ is given in the Appendix. $t_{\min}$ is expressed as

$$t_{\min} = \tau\,[-\gamma - \Omega_{-1}\,(-\exp(-\gamma))]\,. \quad (17)$$

Now, the objective is to find the flipping time t_f. t_f is the sum of $t_{\min}$, and the time delay that V_B takes to rise from 0 V to V_{M1} (this time is denoted by $t_{\rm up}$). This delay is driven by transistors M_{p2} and M_{n2}, where their gate voltage V_A is constant at V_{M2} [see (13)]. The nodal current equation at node V_B is given by

$$C_B \frac{dV_B}{dt} = i_{p2_{\rm sub}} - i_{n2_{\rm sub}} \quad (18)$$

where C_B is the capacitance of node V_B. The currents, $i_{p2_{\rm sub}}$ and $i_{n2_{\rm sub}}$, are given by

$$\begin{aligned} i_{p2{\rm sub}} &= i_{p2o}\exp\left(\frac{V_{\rm DD} - V_{M2} - |V_{tp2}|}{nV_T}\right) \\ &\quad \times \left[1 - exp\left(\frac{-(V_{\rm DD} - V_B)}{V_T}\right)\right] \\ i_{n2{\rm sub}} &= i_{n2o} exp\left(\frac{V_{M2} - V_{tn2}}{nV_T}\right)\left[1 - \exp\left(\frac{-V_B}{V_T}\right)\right] \end{aligned} \quad (19)$$

where

$$\begin{aligned} i_{p2o} &= \mu_p C_{ox}\left(\frac{W}{L}\right)_{p2}(V_T)^2\exp(1.8) \\ i_{n2o} &= \mu_n C_{ox}\left(\frac{W}{L}\right)_{n2}(V_T)^2\exp(1.8). \end{aligned} \quad (20)$$

Similarly, since V_B changes from 0 V to V_{M1} over the time interval $[t_{\min}, t_f]$, the currents, $i_{p2_{\rm sub}}$ and $i_{n2_{\rm sub}}$, vary during the same time interval. In order to simplify the solution of the differential equation in (18), the currents, $i_{p2_{\rm sub}}$ and $i_{n2_{\rm sub}}$, are averaged over this time interval and are considered constants. Furthermore, $V_{\rm DD}$ and V_M are assumed to be greater than $3V_T$. Consequently, the term $[1 - \exp((V_{\rm DD} - V_B)/V_T)] \approx 1$ and the term, $[1 - \exp(-V_B/V_T)]$, is averaged over the time interval $[t_{\min}, t_f]$. This average value is denoted by β_2 such that

$$\begin{aligned} \beta_2 &= \frac{1}{V_{M1}}\int_0^{V_{M1}}\left[1 - \exp\left(\frac{-V_B}{V_T}\right)\right]dV_B \\ &\approx 1 - \frac{V_T}{V_{M1}}. \end{aligned} \quad (21)$$

TABLE I
ANALYTICAL FORMULAS FOR THE CRITICAL CHARGE MODEL

$Q_{critical}$ = Q (1-exp(-t_f / τ))
Q = C_A $(V_{DD} - V_{M2}) + [i_{p1_{sub}} - i_{n1_{sub}}]$ $[t_{min} + \tau]$
$t_f = t_{min} + t_{up}$
$t_{min} = \tau$ $[-\gamma - \Omega_{-1}(-\exp(-\gamma))]$, $\gamma = 1 + \frac{C_A\ (V_{DD} - V_{M2})}{\tau\ [i_{p1_{sub}} - i_{n1_{sub}}]}$
t_{up} $= \frac{C_B\ V_{M1}}{[i_{p2_{sub}} - i_{n2_{sub}}]}$
$V_{M_{1,2}} = \frac{1}{2}\ [V_{DD} - \lvert V_{tp_{1,2}}\rvert + V_{tn_{1,2}} + n\ V_T\ \ln(\frac{i_{p_{1,2^o}}}{i_{n_{1,2^o}}})]$
$i_{p_{1,2o}} = \mu_p\ C_{ox}\ (\frac{W}{L})_{p_{1,2}}\ (V_T)^2\ exp(1.8)$,
$i_{n_{1,2o}} = \mu_n\ C_{ox}\ (\frac{W}{L})_{n_{1,2}}\ (V_T)^2\ exp(1.8)$
$i_{p1sub} = \beta_1\ i_{p1o}\ exp(\frac{V_{DD} - \lvert V_{tp1}\rvert}{nV_T})$
$i_{n1sub} = i_{n1o}\ exp(\frac{-V_{tn1}}{nV_T})$
$i_{p2sub} = i_{p2o}\ exp(\frac{V_{DD} - V_{M2} - \lvert V_{tp2}\rvert}{nV_T})$
$i_{n2sub} = \beta_2\ i_{n2o}\ exp(\frac{V_{M2} - V_{tn2}}{nV_T})$
$\beta_1 = 1 - \frac{V_T}{V_{DD} - V_{M2}}$, $\beta_2 = 1 - \frac{V_T}{V_{M1}}$

By solving the differential equation in (18), the delay $t_{\rm up}$ is expressed as

$$t_{\rm up} = \frac{C_B V_{M1}}{[i_{p2_{\rm sub}} - i_{n2_{\rm sub}}]}. \quad (22)$$

Thus, the critical charge $Q_{\rm critical}$, is obtained as follows [29], [37]–[40]

$$\begin{aligned} Q_{\rm critical} &= \int_0^{t_f} i_{\rm injected}(t)dt \\ &= Q\,(1 - \exp(-t_f/\tau))\,. \end{aligned} \quad (23)$$

The analytical formulas of the proposed critical charge reference (exact) model are summarized in Table I. It is important to notice that the parameter τ listed in Table I is independent of the circuit parameters and depends mainly on the physical conditions of the particle strike event.

B. Statistical Critical Charge Variation Model

Process variations affect device parameters, resulting in fluctuations in the critical charge. The primary sources of process variations that affect the device parameters are as follows.

1) *Random Dopant Fluctuations (RDF).* The number of dopants in the MOSFET depletion region decreases as technology scales. Due to the discreteness of the dopant atoms, there is a statistical random fluctuation of the

number of dopants within a given volume around their average value [30], [32]. This fluctuation in the number of dopants in the transistor channel results in device threshold voltage variations. It has been demonstrated that the threshold voltage variation, due to RDF, is normally distributed, and its standard deviation inversely proportional to the square root of the transistor active area [30], [32], [41].

2) *Channel Length Variations.* For sub-90-nm nodes, optical lithography utilizes light sources with wavelengths much larger than the minimum feature sizes for the technology [23]. Therefore, controlling the critical dimension (CD) at these technology nodes is so difficult. The variation in CD (i.e., the channel length of the transistor) impacts, directly, the transistor threshold voltage, V_t. In short channel devices, V_t has an exponential dependence on the channel length L due to charge sharing and drain-induced barrier lowering (DIBL) effects [30], [32], [34]. As a result, a slight variation in L introduces a large variation in V_t due to the exponential dependence.

Although the RDF and channel length variations are considered the dominant sources of device variations [22], there are many other sources such as line edge roughness (LER), oxide charge variations, and mobility fluctuations, gate oxide thickness variations, channel width variation, and aging effects that affect the device threshold voltage variations [32].

From a circuit modeling perspective, the total variation in V_t, due to RDF, channel length variation, as well as other sources of variation, is modeled as [30]

$$\sigma_{V_t} = \sqrt{\sigma^2_{V_t,\mathrm{RDF}} + \sigma^2_{V_t,L} + \sigma^2_{V_t,\mathrm{Other}}}. \tag{24}$$

Throughout this paper, the interest is in the total variation in threshold voltage (σ_{Vt}), as modeled in (24).

From Table I, it is evident that the critical charge Q_{critical} is dependent on the threshold voltages of transistors M_{p1}, M_{p2}, M_{n1}, and M_{n2}, represented by V_{tp1}, V_{tp2}, V_{tn1}, and V_{tn2}, respectively. A small change in these threshold voltages results in an incremental change in the critical charge, $Q_{\mathrm{critical}}(\Delta(Q_{\mathrm{critical}}))$, which is calculated by using Taylor expansion around the nominal value as follows:

$$\Delta Q_{\mathrm{critical}} = \frac{\partial Q_{\mathrm{critical}}}{\partial V_{tp1}}\Delta V_{tp1} + \frac{\partial Q_{\mathrm{critical}}}{\partial V_{tp2}}\Delta V_{tp2} + \frac{\partial Q_{\mathrm{critical}}}{\partial V_{tn1}}\Delta V_{tn1} + \frac{\partial Q_{\mathrm{critical}}}{\partial V_{tn2}}\Delta V_{tn2} \tag{25}$$

where ΔVt_{p1}, ΔVt_{p2}, ΔVt_{n1}, and ΔVt_{n2} are the variations of the threshold voltages. The partial derivative terms in (25) are computed numerically at the mean threshold voltages. Therefore, the standard deviation of the critical charge variations is found as follows:

$$\sigma_{Q_{\mathrm{critical}}} = \left\{ \left(\frac{\partial Q_{\mathrm{critical}}}{\partial V_{tp1}}\right)^2 \sigma^2_{V_{tp1}} + \left(\frac{\partial Q_{\mathrm{critical}}}{\partial V_{tp2}}\right)^2 \sigma^2_{V_{tp2}} + \left(\frac{\partial Q_{\mathrm{critical}}}{\partial V_{tn1}}\right)^2 \sigma^2_{V_{tn1}} + \left(\frac{\partial Q_{\mathrm{critical}}}{\partial V_{tn2}}\right)^2 \sigma^2_{V_{tn2}} \right\}^{0.5} \tag{26}$$

where σ_{Vtp1}, σ_{Vtp2}, σ_{Vtn1}, and σ_{Vtn2} are the standard deviations of the threshold voltages, V_{tp1}, V_{tp2}, V_{tn1}, and V_{tn2}, respectively.

This reference model is valid for the following assumptions.

1) The dominant source of variations is the transistor threshold voltage, V_t, random variations. The channel length variations are assumed to affect only V_t through the short channel effects. Although the variations in the channel length also introduce fluctuations in the input gate capacitance, their contribution is much smaller than the variations in the threshold voltage [30], [42].
2) The channel length systematic variations are ignored in the proposed models and only the channel length random variations are considered since in the systematic variations, the channel lengths of all the SRAM cell transistors are shifted by the same amount and these variations can be modeled using corner based methods. However, the main focus of the proposed statistical models is on random WID variations which are much more difficult to be modeled. Therefore, the proposed statistical models consider only random variations of the channel length which are captured in the threshold voltage through the DIBL effects.
3) The impact of process variations on the critical charge variations is computed by using a linear approximation. This assumption is valid, since WID variations are usually small and can be linearized around the nominal value [42]–[46]. Under this linear approximation, the critical charge mean value is equal to its deterministic value, when no variations are introduced. Therefore, process variations affect only the variance of the critical charge (i.e., the critical charge spread around its nominal value). According to [42]–[46], this linear approximation is valid as long as the WID variation sigma is smaller than the nominal value. If the WID variations sigma is comparable to the nominal value, the proposed models are not accurate. In the proposed models, it is found that as long as sigma/nominal <0.5, the percentage error between Q_{critical} obtained from the transient (with no variations) and from Monte Carlo (when variations are included) is less than 5%. This is verified by simulations in Section IV and this percentage error is less than 2%.
4) According to [47], the correlation between the different transistors threshold voltages can be neglected for WID variations. This is due to the fact that the RDF is random, and therefore, V_t of the four transistors in consideration are identified as four independent and uncorrelated Gaussian random variables [48]. This assumption simplifies the derivation of (26).

It should be emphasized that the previous analysis is valid for the 1-to-0 flip, when V_A is more susceptible to soft errors than V_B. This occurs when $\mu_n(W/L)_{n2}/\mu_p(W/L)_{p1}$ is much larger than $\exp((V_{tn2} - |V_{tp1}|)/nV_T)$. However, when $\mu_n(W/L)_{n2}/\mu_p(W/L)_{p1}$ is much less than $\exp((V_{tn2} - |V_{tp1}|)/nV_T)$, V_B is more susceptible to soft errors than V_A. Therefore, the 0-to-1 flip case should be considered. Accordingly, the previous analysis can be repeated by

replacing (6), (18) by the following differential equations at nodes A and B:

$$C_B\frac{dV_B}{dt} = [i_{p2_{sub}} - i_{n2_{\rm sub}}] + i_{\rm injected}(t) \quad (27)$$

$$C_A\frac{dV_A}{dt} = [i_{p1_{\rm sub}} - i_{n1_{\rm sub}}]. \quad (28)$$

Consequently, all the previously derived equations are used again for the 0-to-1 flip case by replacing C_A and C_B by C_B and C_A, respectively; the parameters of the transistors M_{p1}, M_{p2}, M_{n1}, and M_{n2} by the parameters of the transistors M_{p2}, M_{p1}, M_{n2}, and M_{n1}, respectively; and Q by $-Q$.

III. Approximate Model Assumptions and Derivations

The model introduced in Section II for the critical charge variations, is calculated numerically. Therefore, it does not present any obvious design insights for WID variations due to its complexity. However, the model can be used for the D2D variations by adopting corner-based (or worst-case) analysis methods. In this section, this complex model is approximated to account for the critical charge variations from a design perspective. The following assumptions are made to derive this approximate model.

1) In sub-threshold SRAM cell, the flipping time, t_f, is larger than τ due to the lower supply voltages and smaller sub-threshold currents values (typically, $t_f/\tau \geq 3$). Therefore, the critical charge expression in (23) is approximated by $Q_{\rm critical} \approx Q$ for the critical charge variability calculations.
2) The variation of the inverter threshold voltage V_{M2}, expressed in (12), which is dependent on V_{tp2} and V_{tn2} is calculated to be less than 1%, relative to its mean value. As a result, the variations in V_{M2} are ignored, and V_{M2} is assumed constant from the variations perspective. Therefore, $\sigma_{Q_{\rm critical}}$ is dependent on only the variations in V_{tp1} and V_{tn1} through $i_{p1\rm sub}$ and $i_{n1\rm sub}$, respectively.
3) The current $i_{n1\rm sub}$ expressed in Table I, is neglected with respect to $i_{p1\rm sub}$, if $V_{tn1} \geq 3nV_T$. This condition is always satisfied, since $3nV_T \approx 125$ mV at room temperature for current CMOS technologies and the threshold voltages take on higher values than 125 mV. Thus, the V_{tp1} contribution to $\sigma_{Q_{\rm critical}}$ dominates all other threshold voltages variations.

By adopting these assumptions, $Q_{\rm critical}$ is approximated by the following equation:

$$Q_{\rm critical} \approx \tau i_{p1_{\rm sub}} \left|\Omega_{-1}\left(-\exp(-\gamma)\right)\right|. \quad (29)$$

Similarly, $\sigma_{Q_{\rm critical}}$ is approximated by the following equation:

$$\sigma_{Q_{\rm critical}} = \left|\frac{\partial Q_{\rm critical}}{\partial V_{tp1}}\right|\sigma_{V_{tp1}} \approx \left|\frac{\partial Q}{\partial V_{tp1}}\right|\sigma_{V_{tp1}} \approx \tau\frac{i_{p1_{\rm sub}}}{nV_T}\left[1+(\gamma-1)(1+\theta)+\frac{t_{\rm min}}{\tau}\right]\sigma_{V_{tp1}} \quad (30)$$

where

$$\theta = \frac{\partial\Omega_{-1}\left(-\exp(-\gamma)\right)}{\partial\gamma} = -\frac{\Omega_{-1}\left(-\exp(-\gamma)\right)}{1+\Omega_{-1}\left(-\exp(-\gamma)\right)}. \quad (31)$$

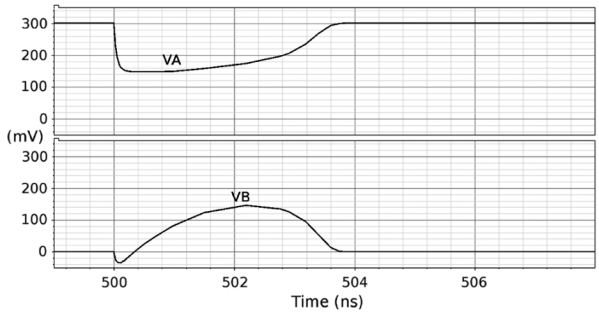


Fig. 3. V_A and V_B voltages in the non-flipping case when V_A voltage falls down till it hits $V_{\rm min}$ then it recovers back to $V_{\rm DD}$. In this case, V_B voltage does not hit V_{M1}, and therefore, V_A recovers. In this simulation, $V_{\rm DD} = 0.3$ V and $\tau = 500$ ps. In this case, the value of $V_{M1} = V_{M2} \approx 147.8$ mV.

Equation (30) is simplified further by using the formulas tabulated in Table I, and $\sigma_{Q_{\rm critical}}$ is approximated further by

$$\sigma_{Q_{\rm critical}} \approx \left(\frac{\tau i_{p1_{\rm sub}}\sigma_{V_{tp1}}}{nV_T}\right) \times \left|\frac{\Omega_{-1}\left(-\exp(-\gamma)\right)\left(\gamma+\Omega_{-1}\left(-\exp(-\gamma)\right)\right)}{1+\Omega_{-1}\left(-\exp(-\gamma)\right)}\right|. \quad (32)$$

Thus, the relative critical charge variation, $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$, is given by the following equation:

$$\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}} \approx \left|\left(\frac{\sigma_{V_{tp1}}}{nV_T}\right)\frac{\gamma+\Omega_{-1}\left(-\exp(-\gamma)\right)}{1+\Omega_{-1}\left(-\exp(-\gamma)\right)}\right|. \quad (33)$$

IV. Results and Discussions

A. Consistency Check of the Proposed Models

First, the assumptions in (13) are justified. Fig. 3 shows V_A and V_B voltages in the non-flipping case. It is clear that since V_B voltage cannot hit V_{M1}, the SRAM cell recovers. However, in Fig. 4, V_B hits V_{M1}, and hence, the SRAM cell exhibits a soft error. Moreover, Fig. 4 depicts that the V_B voltage is approximately 0 V, as long as the V_A voltage is falling. Once the V_A voltage reaches $V_{\rm min}$, the V_A voltage stays constant at $V_{\rm min}$, whereas the V_B voltage starts to rise to V_{M1}. These results ensure that the assumptions made in (13) are realistic. It should be mentioned that the minimum voltage, $V_{\rm min}$, shown in Fig. 4 at which V_A stays constant before flipping to 0 V (≈146.9 mV), is slightly less than $V_{\rm min}$ shown in Fig. 3 (≈148.4 mV) for the non-flipping case. This demonstrates that the flipping occurs, when $V_{\rm min}$ is less than $V_{M2}(V_{M2} \approx 147.8$ mV). In all the simulations, an industrial hardware-calibrated 65-nm CMOS technology transistor model, whose technological parameters are listed in Table II, is employed. The SRAM cell is sized as reported in [45].

A consistency check is performed to the proposed models of the critical charge nominal value and the critical charge variations. The analytical models are compared to the simulation results from SPICE transient and Monte Carlo simulations. These simulations are performed to validate the nominal critical charge and the critical charge variability models for both the proposed reference and the approximate models.

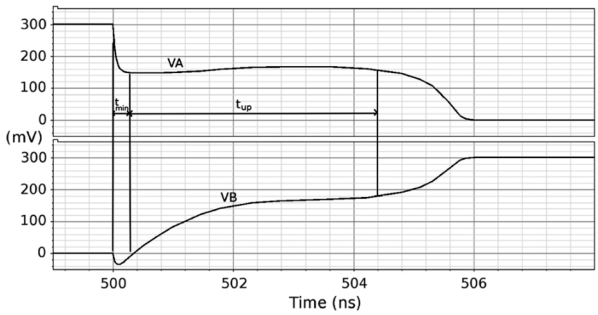


Fig. 4. V_A and V_B voltages in the flipping case when V_B voltage hits V_{M1}, and hence, the SRAM cell exhibits a soft error. The minimum voltage $V_{\min}$ shown in this case at which V_A stays constant before flipping to 0 V ($\approx$146.9 mV) is slightly less than $V_{\min}$ shown in the non-flipping case in Fig. 3 ($\approx$148.4 mV). In this simulation, $V_{\rm DD} = 0.3$ V and $\tau = 500$ ps. In this case, the value of $V_{M1} = V_{M2} \approx 147.8$ mV.

TABLE II
65-nm TECHNOLOGY INFORMATION AND SRAM CELL SIZING [45]

	NMOS	PMOS
W/L ($\mu m/\mu m$)	0.195/0.065	0.11/0.065
V_t (mV)	348	294
σ_{V_t} (mV)	26.7	35.5
n	1.6	1.6

In the following, the validation results for these models are presented. A high number of Monte Carlo runs (10 000 runs) are used to provide a good accuracy in determining the critical charge mean and standard deviation. For each Monte Carlo run, the value of the current pulse charge, Q, which causes the cell to flip, is determined. Then, the simulations are repeated for different $V_{\rm DD}$ (from 0.15 V to 0.3 V) to find the effect of reducing $V_{\rm DD}$ on the critical charge mean and variations. The SRAM cell sizing shown in Table II is used in the simulation setups. Hardware-calibrated statistical models are used to account for V_t variations. Typically, the random variations are inversely proportional to the square root of the gate area $(\mathrm{W}*\mathrm{L})$, as explained in Section II-B [32], [41]. Therefore, the pMOS transistors have higher V_t variations than the nMOS transistors, since the pMOS transistors exhibit a lower driving strength (smaller size) than the nMOS transistors in the SRAM cell.

Fig. 5 displays the nominal critical charge which is obtained by using the transient simulations, $Q_{\rm critical}$, and Monte Carlo simulations, $\mu_{Q_{\rm critical}}$. Clear agreement between $Q_{\rm critical}$ and $\mu_{Q_{\rm critical}}$ justifies the linearity approximation assumption in Section II-B (i.e., process variations affect only on the critical charge variance (spread) and have no effect on its mean). The percentage error between $Q_{\rm critical}$ obtained from the transient (with no variations) and from Monte Carlo (when variations are included) is less than 2%.

Fig. 6 demonstrates the nominal critical charge value calculated from the proposed reference and approximate model versions, and compared to the transient simulation results for different supply voltage values. It should be noted that the approximate model is proposed mainly for the WID variations estimation, although the model still shows an acceptable match for the nominal critical charge value. These results are obtained by using $\tau = 500$ ps to ensure that the primary assumption in (5) is satisfied ($\tau_r = 20$ ps and $\tau_f = 500$ ps). It is evident from Figs. 5 and 6 that reducing the supply voltage decreases the critical charge, which is expected.

Fig. 7 depicts the values of $Q_{\rm critical}$, computed from the proposed models and from SPICE transient simulations for different current pulse widths (by varying τ from 250 to 750 ps). The approximate model results are not revealed in this figure since the approximate model is primarily introduced for the estimation of the WID variations. In Fig. 7, It is observed that as the current pulse width increases (i.e., the diffusion current dominates), the critical charge increases.

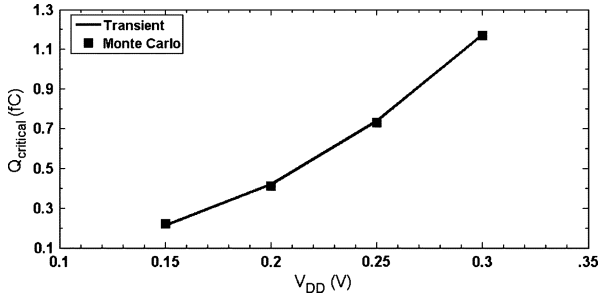


Fig. 5. $Q_{\rm critical}$ versus $V_{\rm DD}$ for $\tau = 500$ ps from the transient simulations (when no variations are introduced) and from Monte Carlo simulations. Clear agreement between $Q_{\rm critical}$ (obtained from transient simulations) and $\mu_{Q_{\rm critical}}$ (obtained from Monte Carlo simulations) justifies the linearity approximation assumption.

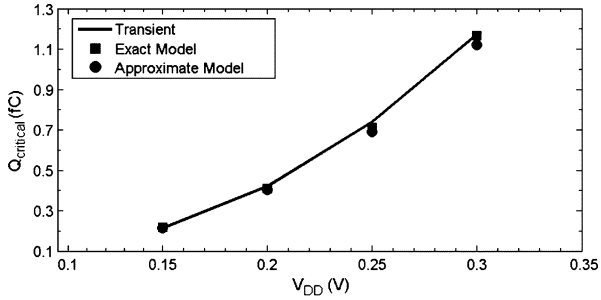


Fig. 6. $Q_{\rm critical}$ versus $V_{\rm DD}$ for $\tau = 500$ ps from SPICE transient simulations. Also shown the results from the proposed reference and approximate models.

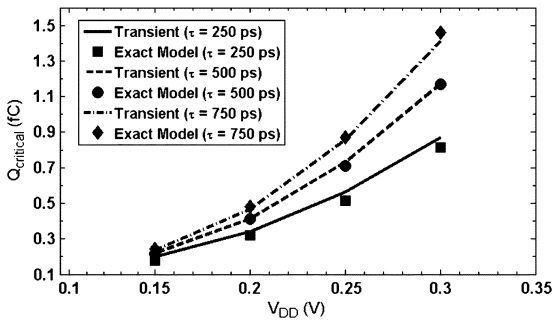


Fig. 7. $Q_{\rm critical}$ versus $V_{\rm DD}$ for different values of τ (250, 500, and 750 ps) from the transient simulations and from the proposed reference model.

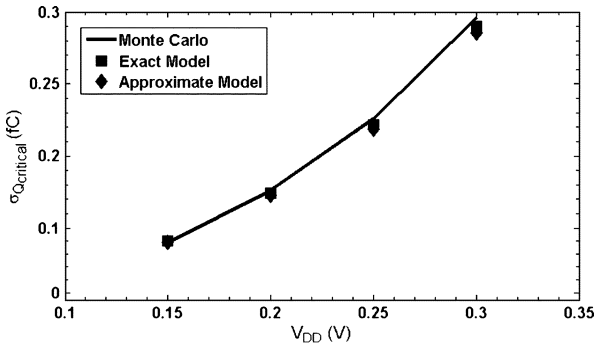


Fig. 8. Critical charge variations, $\sigma_{Q_{\rm critical}}$, versus $V_{\rm DD}$ for $\tau = 500$ ps from Monte Carlo simulations and from the proposed reference and approximate models.

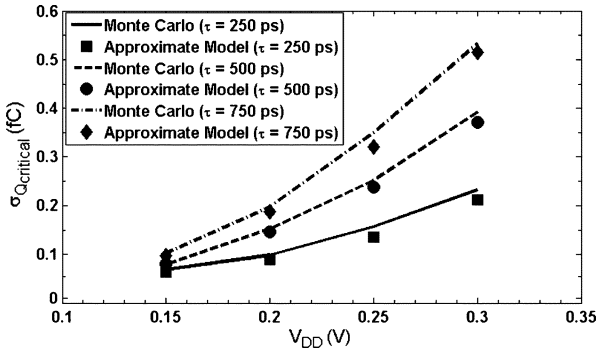


Fig. 9. Critical charge variations $\sigma_{Q_{\rm critical}}$ versus $V_{\rm DD}$ for different values of τ (250, 500, and 750 ps) from Monte Carlo simulation and from the proposed approximate model.

In Sections II-B and III, the derivation of the critical charge standard deviation, by employing the reference model and the approximate model, is described. Fig. 8 shows the simulation results for $\sigma_{Q_{\rm critical}}$ for different $V_{\rm DD}$ values. Note that each data point represents $\sigma_{Q_{\rm critical}}$ calculated from 10 000 Monte Carlo runs. Also, Fig. 8 exhibits the results from the proposed models. The results of both models match those of the simulations. Fig. 9 shows the critical charge standard deviation, $\sigma_{Q_{\rm critical}}$, obtained from simulations and from the approximate model for different values of τ. It is demonstrated that as τ is reduced, the critical charge variations are reduced. Also, reducing the supply voltage, $V_{\rm DD}$, reduces $\sigma_{Q_{\rm critical}}$. It is important to mention that only the approximate model is used in all the following results and discussions.

From (29), $Q_{\rm critical}$ is a function of τ, $i_{p1_{\rm sub}}$, and γ. However, γ is also a function of τ, $i_{p1_{\rm sub}}$, C_A, and $V_{\rm DD}$. Therefore, to investigate the effect of these parameters on $Q_{\rm critical}$, (29) is rewritten as follows by using the fact that $\gamma = 1 + (C_A(V_{\rm DD} - V_{M2})/\tau i_{p1_{\rm sub}})$, as shown in (34) at the bottom of the page.

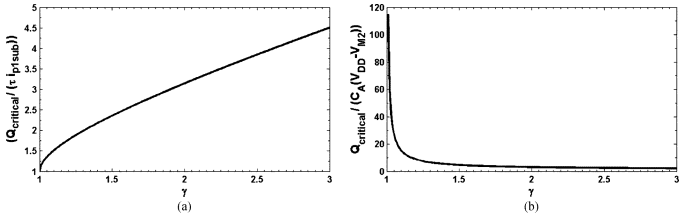


Fig. 10. (a) $(Q_{\rm critical}/(\tau i_{p1_{\rm sub}}))$ versus γ for a constant $(\tau i_{p1_{\rm sub}})$ illustrating that as γ increases, $Q_{\rm critical}$ increases and (b) $(Q_{\rm critical}/(C_A(V_{\rm DD} - V_{M2}))$ versus γ for a constant $(C_A(V_{\rm DD} - V_{M2}))$ showing that as γ increases, $Q_{\rm critical}$ is reduced in this case.

Fig. 10(a) plots $(Q_{\rm critical}/(\tau i_{p1_{\rm sub}}))$ versus γ for a constant $(\tau i_{p1_{\rm sub}})$, and illustrates that as γ increases, $Q_{\rm critical}$ increases. Therefore, increasing C_A and/or $V_{\rm DD}$ increases γ, and accordingly, increases $Q_{\rm critical}$. Fig. 10(b) plots $(Q_{\rm critical}/(C_A(V_{\rm DD} - V_{M2})))$ versus γ for a constant $(C_A(V_{\rm DD} - V_{M2}))$ and shows that as γ increases, $Q_{\rm critical}$ is reduced. Therefore, increasing τ and/or $i_{p1_{\rm sub}}$ reduces γ, and accordingly, increases $Q_{\rm critical}$. This result can be justified since increasing $i_{p1_{\rm sub}}$, the transistor M_{p1} restoring current, increases $Q_{\rm critical}$.

Fig. 7 portrays these results for $V_{\rm DD}$ and τ, and demonstrates that increasing any of them increases $Q_{\rm critical}$. Fig. 11 illustrates the effect of C_A and $i_{p1_{\rm sub}}$ on $Q_{\rm critical}$ and compares these results to SPICE transient simulation results. The sub-threshold current, $i_{p1_{\rm sub}}$, is varied by changing the width of transistor M_{p1}, W_{p1}. The capacitance, C_A, is varied by employing a variable coupling capacitor, C_c, between nodes V_A and V_B. This coupling capacitor, C_c, is one of the most common soft errors mitigation techniques employed in SRAM cells. Then, The model capacitances, C_A and C_B, are obtained by applying the Miller theorem as follows [29]:

$$\begin{aligned} C'_A &= C_A + 2C_c \\ C'_B &= C_B + 2C_c. \end{aligned} \tag{35}$$

Similarly, the same analysis, applied to $Q_{\rm critical}$, is repeated for $\sigma_{Q_{\rm critical}}$ and shown in Fig. 12(a) and (b). From these figures, $\sigma_{Q_{\rm critical}}$ increases when any of the parameters τ, C_A, $i_{p1_{\rm sub}}$, and $V_{\rm DD}$ increases. From (32), $\sigma_{Q_{\rm critical}}$ is proportional to $(\sigma_{V_{tp1}}\ i_{p1_{\rm sub}})$, since $\sigma_{V_{tp1}}\ \alpha\ (1/\sqrt{W_{p1}})$ and $i_{p1_{\rm sub}}\ \alpha\ W_{p1}$, $\sigma_{Q_{\rm critical}}$ is proportional to $\sqrt{W_{p1}}$. Therefore, increasing $i_{p1_{\rm sub}}$ by increasing W_{p1}, reduces $\sigma_{V_{tp1}}$, but results in increasing $\sigma_{Q_{\rm critical}}$.

Fig. 9 validates these results for $V_{\rm DD}$ and τ, and shows that an increase in any of them, increases $Q_{\rm critical}$. Fig. 13 shows the

$$\begin{cases} \dfrac{Q_{\rm critical}}{\tau i_{p1_{\rm sub}}} \approx \left|\Omega_{-1}\left(-\exp(-\gamma)\right)\right|, & \text{for } (\tau i_{p1_{\rm sub}}) = \text{constant} \\ \dfrac{Q_{\rm critical}}{C_A(V_{\rm DD}-V_{M2})} \approx \dfrac{C_A(V_{\rm DD}-V_{M2})}{\gamma-1} \times \left|\Omega_{-1}\left(-\exp(-\gamma)\right)\right|, & \text{for } (C_A(V_{\rm DD} - V_{M2})) = \text{constant} \end{cases} \tag{34}$$

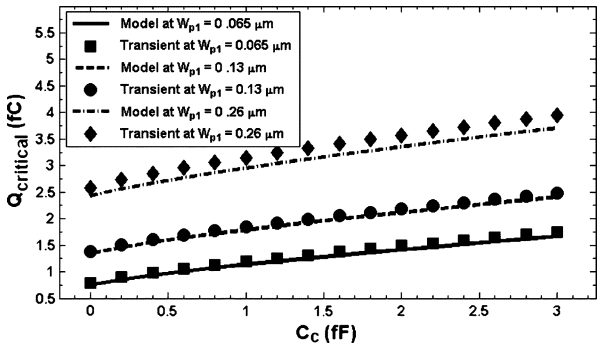


Fig. 11. Effect of adding a coupling capacitor C_c, for different values of W_{p1} (0.065, 0.13, and 0.26 μm) on $Q_{\rm critical}$ from the proposed model and transient simulations. It shows that increasing C_c and/or W_{p1}, increases $Q_{\rm critical}$. In this figure, $V_{\rm DD} = 0.3$ V, and $\tau = 500$ ps.

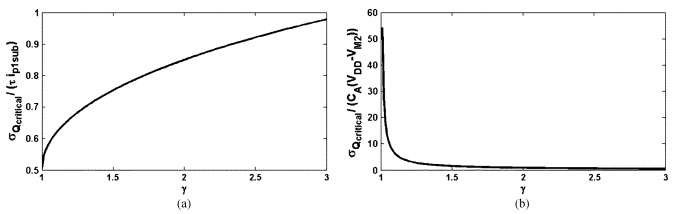


Fig. 12. (a) $(\sigma_{Q_{\rm critical}}/(\tau i_{p1_{\rm sub}}))$ versus γ for a constant $(\tau i_{p1_{\rm sub}})$ illustrating that as γ increases, $\sigma_{Q_{\rm critical}}$ increases and (b) $(\sigma_{Q_{\rm critical}}/(C_A(V_{\rm DD}-V_{M2}))$ versus γ for a constant $(C_A(V_{\rm DD}-V_{M2}))$ showing that as γ increases, $\sigma_{Q_{\rm critical}}$ is reduced in this case.

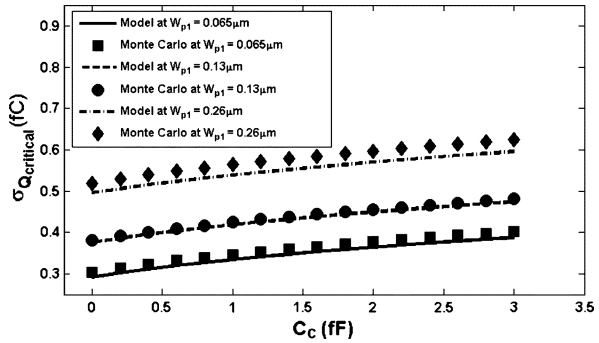


Fig. 13. Effect of adding a coupling capacitor C_c for different values of W_{p1} (0.065, 0.13, and 0.26 μm) on $\sigma_{Q_{\rm critical}}$ from the proposed model and Monte Carlo simulations. It shows that increasing C_c and/or W_{p1}, increases $\sigma_{Q_{\rm critical}}$. In this figure, $V_{\rm DD} = 0.3$ V, and $\tau = 500$ ps.

effect of C_A and W_{p1} on $\sigma_{Q_{\rm critical}}$, comparing these results to Monte Carlo simulation results.

By using (33), the relative critical charge variation $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ is plotted versus γ for a constant $(\sigma_{V_{tp1}}/nV_T)$, in Fig. 14. According to this figure, increasing C_A and/or $V_{\rm DD}$ results in reducing $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$, whereas, $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ is reduced by reducing τ. The effect of W_{p1} on $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ is different from its effect on either $Q_{\rm critical}$ or $\sigma_{Q_{\rm critical}}$. Although increasing W_{p1} increases $Q_{\rm critical}$ and $\sigma_{Q_{\rm critical}}$, it results in reducing $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ due to the dependence of $\sigma_{V_{tp1}}$ on W_{p1} [see (33)]. Figs. 15 and 16 compare these results to Monte Carlo simulations.

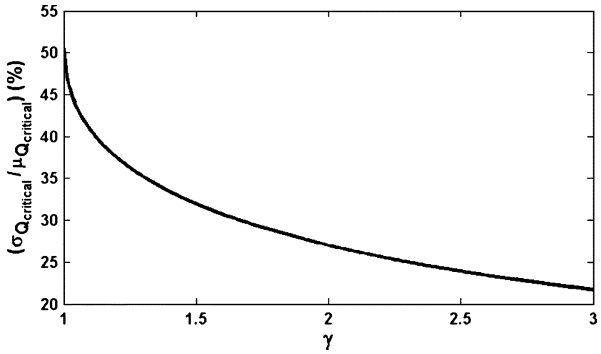


Fig. 14. Relative critical charge variation $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ versus γ for a constant $(\sigma_{V_{tp1}}/nV_T)$. It shows that as γ increases $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ is reduced.

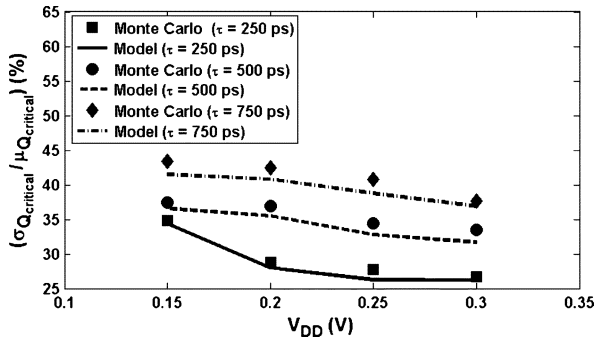


Fig. 15. Relative critical charge variation $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$, versus $V_{\rm DD}$ for different values of τ (250, 500, and 750 ps) from Monte Carlo simulations and from the proposed model.

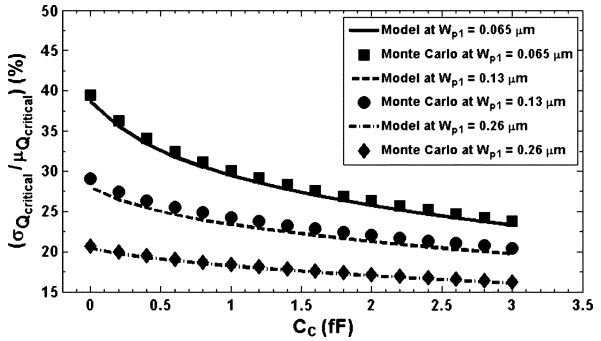
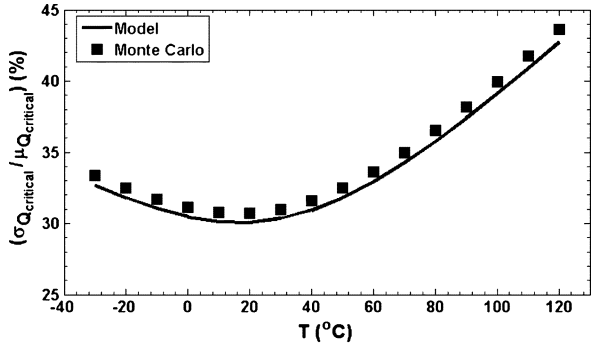


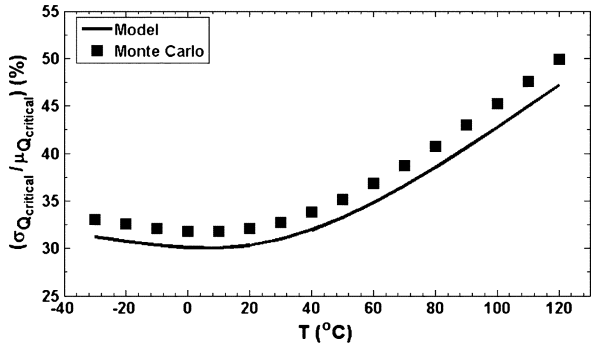
Fig. 16. Effect of adding a coupling capacitor, C_c, for different values of W_{p1} (0.065, 0.13, and 0.26 μm) on $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ from the proposed model and Monte Carlo simulations. It shows that increasing C_c and/or W_{p1} results in reducing $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$. In this figure, $V_{\rm DD} = 0.3$ V, and $\tau = 500$ ps.

B. Effect of the Temperature on the Critical Charge Relative Variations

Furthermore, the effect of the temperature T on $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ is obtained by using (33), and is shown in Fig. 17(a) and (b) for $V_{\rm DD}$ equals 0.3 and 0.25 V, respectively. These results are compared to Monte Carlo simulations. Fig. 17(a) shows that $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ exhibits a minimum value at $T \approx 15\,^{\circ}$C, when $V_{\rm DD} = 0.3$ V. In addition, $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ exhibits a minimum value at $T \approx 7\,^{\circ}$C, when $V_{\rm DD} = 0.25$ V. In the other cases, when $V_{\rm DD}$ equals



(a)



(b)

Fig. 17. (a) $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ versus T when $V_{\rm DD} = 0.3$ V and $\tau = 500$ ps, showing that $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ exhibits a minimum value at $T = 15\,^{\circ}$C and (b) $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ versus T when $V_{\rm DD} = 0.25$ V and $\tau = 500$ ps showing that $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ exhibits a minimum value at $T = 7\,^{\circ}$C.

0.2 and 0.15 V, $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ exhibits its minimum at $T < -30\,^{\circ}$C and are not shown in these figures. In general, as $V_{\rm DD}$ is reduced, the temperature, at which $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ is minimum, is reduced. This result is essential when the SRAM cells are used in applications with strict SER constraints such as space and satellite applications. Temperature control techniques are employed to keep the temperature at the values that keep $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ at its minimum value.

C. Effect of the Sub-Threshold Swing Coefficient on the Critical Charge Relative Variations

The effect of the sub-threshold swing coefficient n on $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ is plotted in Fig. 18 illustrating that increasing n results in reducing $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$. Therefore, increasing n can be used as a device optimization technique to mitigate the critical charge variability in subthreshold SRAM cells. This sub-threshold device optimization is pivotal for applications with strict SER constraints.

D. Proposed Models Accuracy

In Fig. 19, $Q_{\rm critical}$, from the proposed reference model, is plotted versus the transient simulation results for different values of τ, $V_{\rm DD}$, W_{p1}, C_A, and T. The maximum error is 4.6%, and the average error is 2.1%. Fig. 20 shows $\sigma_{Q\rm critical}$ from the approximate model plotted versus Monte Carlo simulation results for different values of τ, $V_{\rm DD}$, W_{p1}, C_A, and T. The maximum error is 12.2%, and the average error is 5.4%. Good agreement between the proposed models and the simulation results justifies all the assumptions used to derive the models, as explained in Sections II and III.

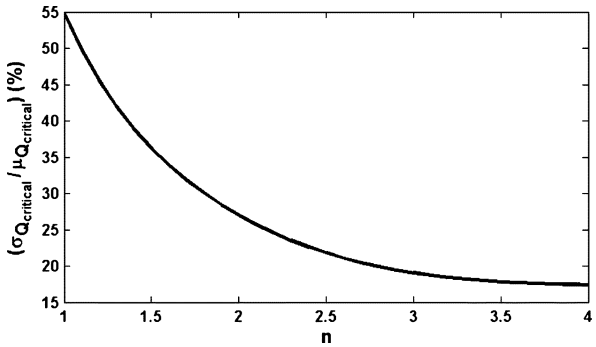


Fig. 18. Effect of the sub-threshold swing coefficient n on $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ for the case when $V_{\rm DD} = 0.3$ V and $\tau = 500$ ps. As n increases, $(\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}})$ is reduced.

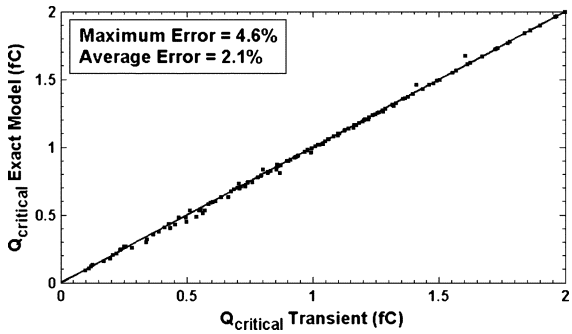


Fig. 19. $Q_{\rm critical}$ from the proposed reference model is plotted versus the transient simulation results for different values of τ, $V_{\rm DD}$, W_{p1}, C_A, and T.

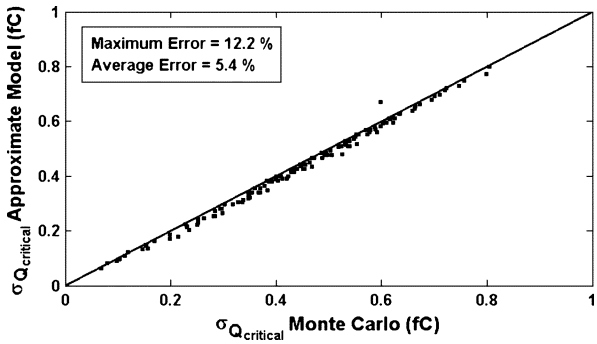


Fig. 20. $\sigma_{Q\rm critical}$ from our approximate model plotted versus Monte Carlo simulation results for the same ranges of τ, $V_{\rm DD}$, W_{p1}, C_A, and T.

As shown in the previous discussions, the proposed models are based on easily measurable parameters, which can be directly extracted from the measurements or technology information (i.e., C_A, C_B, σ_{V_t}, V_t, and n).

V. Design Insights

In this section, some design insights, extracted from the proposed models in this paper, are reported. Equations (29), (32), and (33) provide the following design insights.

1) Increasing the supply voltage, $V_{\rm DD}$, results in increasing both $Q_{\rm critical}$ and $\sigma_{Q_{\rm critical}}$. However, $\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}}$ is reduced by increasing $V_{\rm DD}$. Therefore, the SER variations

are readily minimized by the proper selection of the supply voltage $V_{\rm DD}$.

2) From the formulas in Table I, the critical charge nominal value for the SRAM cell is estimated, accurately, without time consuming transient simulations. Since $Q_{\rm critical}$ exhibits an exponential relationship with the SER, $Q_{\rm critical}$ should be designed high enough by proper circuit design to limit the SER.
3) Increasing the coupling capacitor, C_c, results in increasing $Q_{\rm critical}$ and $\sigma_{Q_{\rm critical}}$. However, $\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}}$ is reduced by increasing C_c. Since this coupling capacitor is one of the most common techniques to increase $Q_{\rm critical}$ and mitigate soft errors, it should be designed carefully to achieve an acceptable $\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}}$ level.
4) The particle strike current pulse width, τ, affects the critical charge calculations. Wide current pulse models (large values of τ) result in a larger $Q_{\rm critical}$, larger $\sigma_{Q_{\rm critical}}$, and larger $\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}}$. Therefore, the accurate physical modeling of the particle strike should be investigated.
5) In sub-threshold SRAM design, $\sigma_{Q_{\rm critical}}$ is dominated by transistor M_{p1} threshold voltage variations $(\sigma_{V_{tp1}})$. The contribution of $(\sigma_{V_{tp1}})$, calculated from the reference proposed model, is more than 96% in all cases. Thus, the assumption used in deriving the approximate model is justified. This assumption is valid as long as t_f is greater than 3τ, which is not applicable in super-threshold SRAM cells.
6) W_{p1} is the only sizing parameter that affects the critical charge in this derivation case (for example, it is W_{p2} if V_B is at logic "1"). Increasing W_{p1} results in increasing $Q_{\rm critical}$ and $\sigma_{Q_{\rm critical}}$ whereas increasing W_{p1} results in reducing $\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}}$. Therefore, for a given $Q_{\rm critical}$ variation constraint, the SRAM sizing can be designed to meet this constraint by using the proposed models at the design phase (before fabrication).
7) From (33), the relative critical charge variation, $\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}}$, exhibits a minimum value at a certain temperature T. Temperature control techniques (throttling techniques) can be used to keep the temperature at the value that results in a minimum $\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}}$, limiting the SER spread.
8) Increasing the sub-threshold swing coefficient n results in reducing $\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}}$. Consequently, the transistor can be optimized for sub-threshold operation to minimize $\sigma_{Q_{\rm critical}}/\mu_{Q_{\rm critical}}$.

Although this paper has focused on the critical charge and its variability modeling for the sub-threshold SRAM cell, the proposed models can be extended to model them in sub-threshold flip-flops circuits. This is possible because all the flip-flops topologies consist of an embedded cross-coupled inverters as those in the SRAM cell. Also, The proposed models can be used for the asymmetric sub-threshold SRAM cells or flip-flops, in which $V_{M1} \neq V_{M2}$, as long as the models assumptions are satisfied (i.e., V_{M1}, V_{M2}, $V_{\rm DD}-V_{M1}$, and $V_{\rm DD}-V_{M2} \geq 3V_T$ for the reference model and $t_f/\tau \geq 3$ and $V_{tn1} \geq 3\ nV_T$ for the approximate model). As a conclusion, our proposed models are valid for any sub-threshold SRAM cell or sub-threshold flip-flop in which the implementation core is the two cross-coupled inverters and these cross-coupled inverters are satisfying the proposed models stated conditions.

Furthermore, the focus is mainly on WID variations in this paper, since, from a circuit perspective, WID variations are much more complex and difficult to be modeled than D2D variations. The D2D variations can be easily modeled by using corner-based models, as introduced in [29]. However, WID variations require accounting for the critical charge variations in each SRAM cell differently. The proposed reference and approximate models can account for both the D2D and WID variations accurately.

VI. Conclusion

In sub-threshold SRAM cells design, process variation in transistor parameters continues to be a growing challenge, especially WID variations. These variations have a strong impact on critical charge variability. In this paper, two analytical models that account for both D2D and WID variations are proposed. The proposed models account for the D2D variations by using corner-based or worst-case methods. Moreover, the models deal with the WID variations by using statistical techniques. The accuracy of the novel models is validated by transient and Monte Carlo SPICE simulation results for an industrial hardware-calibrated 65-nm technology over a wide range of supply voltages, particle strike induced current pulse widths, transistor parameters, temperature, and coupling capacitors. By using the newly derived models, the impact of the transistor parameters, supply voltage, and induced current pulse width on the nominal critical charge value and on its variability is illustrated.

In addition, the proposed models demonstrate that the use of the coupling capacitor in the SRAM cell, as a soft error mitigation technique, is limited by the critical charge variations. The proposed models demonstrate that the relative critical charge variability exhibits a minimum at a certain temperature value. This result can be used by circuit designers to keep the temperature at this value, by using temperature control techniques, to minimize the relative critical charge variability. Moreover, the proposed models show that the transistor sub-threshold swing coefficient can be optimized to minimize the critical charge variability. These results are particulary relevant for applications with strict SER constraints.

The two derived statistical models are scalable, bias dependent, and require only the knowledge of easily measurable parameters. Moreover, the models are very efficient compared with the Monte Carlo simulations. This makes them very useful in the early design cycles, sub-threshold SRAM design optimization, and technology prediction. Furthermore, the proposed models can be extended for the sub-threshold flip-flops critical charge variability, since all flip-flops topologies consist of an embedded cross-coupled inverters, similar to those in the SRAM cell. Also, these models are not limited to the conventional 6T SRAM cells. They can be extended to the new sub-threshold SRAM cells designs reported recently in the literature, since all these new designs have two cross-coupled inverters as their core. Finally, the proposed models facilitate the estimation of the critical charge variability due to both D2D and WID variations at the design phase, and provide vital design insights that aid circuit designers to keep the sub-threshold SRAM cells SER at an acceptable level.

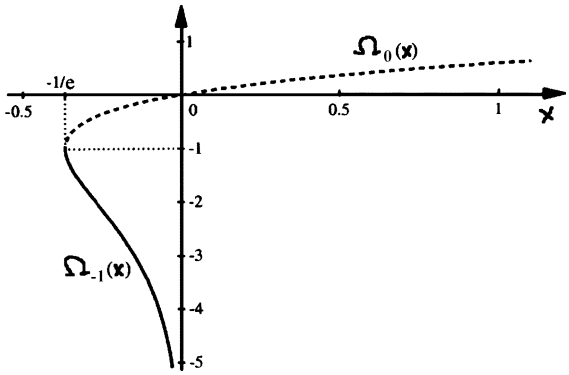


Fig. 21. Two real branches of the Omega function. Solid line: $\Omega_{-1}(x)$ defined for $\{\exp(-1) \leq x < 0\}$ (of interest to us in this paper). Dashed line:$\Omega_{-1}(x)$ defined for $\{\exp(-1) \leq x < \infty\}$. The two branches meet at point $(\exp(-1), 1)$ [36].

APPENDIX

In mathematics, the Lambert W function, named after Johann Heinrich Lambert, also called the Omega function $\Omega(x)$, is the inverse function of $f(x) = x\exp(x)$ and x is any complex number. If x is real and $\{\exp(-1) \leq x < 0\}$, two possible real values of $\Omega(x)$ exist. The branch, satisfying $\{-1 \leq \Omega(x)\}$, is denoted by $\Omega_0(x)$ and is called the principal branch of $\Omega(x)$, and the other branch, satisfying $\{\Omega(x) \leq -1\}$, is denoted by $\Omega_{-1}(x)$. If x is real and $\{x \geq 0\}$, there is a single real value for $\Omega(x)$ which also belongs to the principal branch, $\Omega_0(x)$. Both real branches $\Omega_0(x)$ and $\Omega_{-1}(x)$, for real x, are plotted in Fig. 21 [36]. The real branch $\Omega_{-1}(x)$ is used in the proposed model.

REFERENCES

[1] A. Wang, B. H. Calhoun, and A. P. Chandrakasan, *Sub-Threshold Design for Ultra Low-Power Systems*. New York: Springer, 2006.

[2] B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 680–688, Mar. 2007.

[3] B. H. Calhoun and A. P. Chandrakasan, "Static noise margin variation for sub-threshold SRAM in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1673–1679, Jul. 2006.

[4] N. Verma and A. P. Chandrakasan, "A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 141–149, Jan. 2008.

[5] A. Wang and A. P. Chandrakasan, "A 180 mV FFT processor using sub-threshold circuit techniques," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2004, pp. 292–293.

[6] H. Li, J. Mundy, W. Patterson, D. Kazazis, A. Zaslavsky, and R. I. Bahar, "A model for soft errors in the sub-threshold CMOS inverter," in *Proc. 2nd Workshop Syst. Effects Logic Soft Errors (SELSE2)*, 2006.

[7] N. Verma, J. Kwong, and A. P. Chandrakasan, "Nanometer MOSFET variation in minimum energy sub-threshold circuits," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 163–174, Jan. 2008.

[8] N. Kim, K. Flautner, D. Blaauw, and T. Mudge, "Circuit and micro-architectural techniques for reducing cache leakage power," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 2, pp. 167–184, Feb. 2004.

[9] K. Osada, J. L. Shin, M. Khan, Y. Liou, K. Wang, K. Shoji, K. Kuroda, S. Ikeda, and K. Ishibashi, "Universal-Vdd 0.65 V–2.0 V 32-kB cache using a voltage-adapted timing-generation scheme and a lithographically symmetrical cell," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1738–1744, Nov. 2001.

[10] Q. Ding, R. Luo, and Y. Xie, "Impact of process variation on soft error vulnerability for nanometer VLSI circuits," in *Proc. ASICON*, 2005, pp. 1023–1026.

[11] T. Heijmen, D. Giot, and P. Roche, "Factors that impact the critical charge of memory elements," in *Proc. 12th IEEE Int. On-Line Testing Symp. (IOLTS)*, 2006, pp. 57–62.

[12] T. P. Ma and P. V. Dressendorfer, *Inonizing Radiation Effects in MOS Devices and Circuits*. New York: Wiley, 1989.

[13] T. Nakamura, M. Baba, E. Ibe, Y. Yahag, and H. Kameyama, *Terrestrial Neutron-Induced Soft Errors in Advanced Memory Devices*. Singapore: World Scientific Publishing, 2008.

[14] R. Ramanarayanan, V. Degalahal, N. Vijaykrishnan, M. J. Irwin, and D. Duarte, "Analysis of soft error rate in flip-flops and scannable latches," in *Proc. ASIC*, 2003, pp. 231–234.

[15] K. Ramakrishnan, R. Rajaraman, S. Suresh, N. Vijaykrishnan, Y. Xie, and M. J. Irwin, "Variation impact on SER of combinational circuits," in *Proc. Int. Symp. Quality Electron. Des. (ISQED)*, 2007, pp. 911–916.

[16] T. Heijmen, "Soft error vulnerability of sub-100-nm flip-flops," in *Proc. 14th IEEE Int. On-Line Testing Symp. (IOLTS)*, 2008, pp. 247–252.

[17] P. Hazucha and C. Svensson, "Impact of CMOS technology scaling on the atmospheric neutron soft error rate," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2586–2594, Dec. 2000.

[18] P. Shivakumar, S. W. Keckler, D. Burger, M. Kistler, and L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic," in *Proc. Int. Conf. Dependable Syst. Netw.*, 2002, pp. 389–398.

[19] R. C. Baumanm, "Soft errors in advanced semi-conductor devices-part I: The three radiation sources," *IEEE Trans. Device Mater. Reliab.*, vol. 1, no. 1, pp. 17–22, Mar. 2001.

[20] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter variations and impact on circuits and microarchitecture," in *Proc. 40th Conf. Des. Autom. (DAC)*, 2003, pp. 338–342.

[21] K. Bowman, S. Duvall, and J. Meindl, "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration," *IEEE J. Solid-State Circuits*, vol. 37, no. 2, pp. 183–190, Feb. 2002.

[22] H. Masuda, S. Ohkawa, A. Kurokawa, and M. Aoki, "Challenge: Variability characterization and modeling for 65-nm to 90-nm processes," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2005, pp. 593–599.

[23] J. Tschanz, K. Bowman, and V. De, "Variation tolerant circuits: Circuit solutions and techniques," in *Proc. Des. Autom. Conf. (DAC)*, 2005, pp. 762–763.

[24] ITRS, "The international technology roadmap for semiconductors," [Online]. Available: http://public.itrs.net

[25] J. P. de Gyvez and H. Tuinhout, "Threshold voltage mismatch and intra-die leakage current in digital CMOS circuits," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 157–168, Jan. 2004.

[26] Q. Ding, R. Luo, H. Wang, H. Yang, and Y. Xie, "Modeling the impact of process variation on critical charge distribution," in *Proc. Syst. Chip Conf. (SOC)*, 2006, pp. 243–246.

[27] E. H. Cannon, A. J. Klein Osowski, R. Kanj, D. D. Reinhardt, and R. V. Joshi, "The impact of aging effects and manufacturing variation on SRAM soft-error rate," *IEEE Trans. Device Mater. Reliab.*, vol. 8, no. 1, pp. 145–152, Mar. 2008.

[28] T. Heijmen and B. Kruseman, "Alpha-particle-induced SER of embedded SRAMs affected by variations in process parameters and by the use of process options," *Solid-State Electron.*, vol. 49, pp. 1783–1790, 2005.

[29] S. M. Jahinuzzaman, M. Sharifkhani, and M. Sachdev, "Investigation of process impact on soft error susceptibility of nanometric SRAMs using a compact critical charge model," in *Proc. Int. Symp. Quality Electron. Des. (ISQED)*, 2008, pp. 207–212.

[30] M. H. Abu-Rahma and M. Anis, "A statistical design-oriented delay variation model accounting for within-die variations," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 27, no. 11, pp. 1983–1995, Nov. 2008.

[31] V. Degalahal, N. Vijaykrishnan, and M. Irwin, "Analyzing soft errors in leakage optimized SRAM design," in *Proc. IEEE Int. Conf. VSLI Des.*, 2003, pp. 227–233.

[32] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. New York: Cambridge University Press, 1998.

[33] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[34] W. Liu, *MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4*. New York: Wiley, 2001.

[35] G. R. Srinivasan, P. C. Murley, and H. K. Tang, "Accurate, predictive modeling of soft error rate due to cosmic rays and chip alpha radiation," in *Proc. IEEE Int. Reliab. Phys. Symp.*, 1994, pp. 12–16.
[36] F. Chapeau-Blondeau and A. Monir, "Numerical evaluation of the Lambert W function and application to generation of generalized Gaussian noise with exponent 1/2," *IEEE Trans. Signal Process.*, vol. 50, no. 9, pp. 2160–2165, Sep. 2002.
[37] J. M. Palau, G. Hubert, K. Coulie, B. Sagnes, M.-C. Calvet, and S. Fourtine, "Device simulation study of the SEU sensitivity of SRAMs to internal ion tracks generated by nuclear reactions," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 2, pp. 225–231, Apr. 2001.
[38] Y. Z. Xu, H. Puchner, A. Chatila, 0. Pohland, B. Bruggeman, B. Jin, D. Radaelli, and S. Daniel, "Process impact on SRAM alpha-particle SEU performance," in *Proc. IEEE Int. Reliab. Phys. Symp.*, Phoenix, AZ, 2004, pp. 294–299.
[39] B. Zhang, A. Arapostathis, S. Nassif, and M. Orshansky, "Analytical modeling of SRAM dynamic stability," in *Proc. IEEE/ACM Int. Conf. Comput. Aided Des.*, San Jose, CA, 2006, pp. 315–322.
[40] R. C. Jaeger, R. M. Fox, and S. E. Diehl, "Analytic expressions for the critical charge in CMOS static RAM cells," *IEEE Trans. Nucl. Sci.*, vol. 30, no. 6, pp. 4616–4619, Dec. 1983.
[41] K. Takeuchi, T. Tatsumi, and A. Furukawa, "Channel engineering for the reduction of random dopant placement induced threshold voltage fluctuations," in *Int. Electron Devices Meet., IEDM, Techn. Dig.*, 1996, pp. 841–844.
[42] H. Masuda, S. Okawa, and M. Aoki, "Approach for physical design in sub-100 nm era," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2005, pp. 5934–5937.
[43] M. Eisele, J. Berthold, D. Schmitt-Landsiedel, and R. Mahnkopf, "The impact of intra-die device parameter variations on path delays and on the design for yield of low voltage digital circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 4, pp. 360–368, Jul. 1997.
[44] Y. Cao and L. T. Clark, "Mapping statistical process variations towards circuit performance variability: An analytical modeling approach," in *Proc. Des. Autom. Conf. (DAC)*, 2005, pp. 658–663.
[45] M. R. de Alba-Rosano and A. D. Garcia-Garcia, "Measuring leakage power in nanometer CMOS 6T SRAM cells," in *Proc. IEEE Int. Conf. Reconfigurable Comput. FPGAs*, 2006, pp. 1–7.
[46] S. V. Walstra and C. Dai, "Circuit-level modeling of soft errors in integrated circuits," *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 3, pp. 358–364, Sep. 2005.
[47] J. T. Horstmann, U. Hilleringmann, and K. Goser, "Correlation analysis of the statistical electrical parameter fluctuations in 50 nm MOS transistors," in *Proc. 28th Eur. Solid-State Devices Conf.*, 1998, pp. 512–515.
[48] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 24, no. 12, pp. 1859–1879, Dec. 2005.
[49] G. Hubert, N. Buard, C. Weulersse, T. Carriere, M.-C. Palau, J.-M. Palau, D. Lambert, J. Baggio, F. Wrobel, F. Saigne, and R. Gaillard, "A review of DASIE code family contribution to SEU/MBU understanding," in *Proc. Int. Online Test Symp. (IOLTS)*, 2005, pp. 87–94.
[50] F. Moradi, D. T. Wisland, S. Aunet, H. Mahmoodi, and T. V. Cao, "65-nm sub-threshold 11T SRAM for ultra low voltage applications," in *Proc. IEEE Int. Syst.-on-Chip (SOC) Conf.*, 2008, pp. 113–118.
[51] T. Kim, J. Liu, and C. H. Kim, "An 8T sram cell utilizing reverse short channel effect for write margin and read performance improvement," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2007, pp. 241–244.
[52] S. Lin, Y. Kim, and F. Lombardi, "A 32-nm SRAM design for low power and high stability," in *Proc. Midw. Symp. Circuits Syst. (MWSCAS)*, 2008, pp. 422–425.

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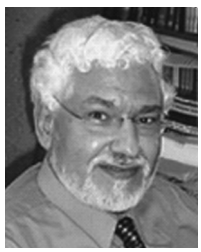

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