Journal of Circuits, Systems, and Computers
Vol. 19, No. 5 (2010) 997–1014
© World Scientific Publishing Company
DOI: 10.1142/S0218126610006566

World Scientific
www.worldscientific.com

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

NOVEL FCS-BASED LAYOUT-FRIENDLY ACCURATE WIDE-BAND LOW-POWER CCII– REALIZATIONS*,†

HASSAN MOSTAFA‡, HEWIDA MOHAMED§ and A. M. SOLIMAN¶

Electronics and Communications Engineering Department,
Cairo University, Giza, Egypt
‡*hassanmostafahassan@yahoo.com*
‡*hmostafa@uwaterloo.ca*
§*cinderlla29@hotmail.com*
¶*asoliman@ieee.org*

Received 29 October 2009
Accepted 18 January 2010

This paper presents two novel Floating Current Source (FCS)-based CMOS negative second generation current conveyor (CCII–) realizations suitable for very large scale implementation. The proposed realizations provide high voltage and current tracking accuracy, as well as large voltage and current transfer bandwidths. Simulation results show that the first proposed wide-band CCII– bandwidth is about 972 MHz. Targeting low-power dissipation, a second low-power version of the wide-band CCII– is proposed at the expense of lower bandwidth and accuracy. The proposed CCII– realizations are layout-friendly because they can be easily fabricated in a systematic modular layout fashion. In addition, a fair comparison is held between the proposed realizations and the only FCS-based CCII– realizations in the literature to show the strength of the proposed circuits. The proposed two CCII– realizations show excellent immunity to process variations and transistor mismatch. In addition, they are insensitive to the temperature variations. Finally, two common CCII– applications are presented.

Keywords: Accurate CMOS current conveyor; floating current source; layout-friendly; wide-band; low-power; analog circuits.

1. Introduction

Second Generation Current Conveyor (CCII) is a very versatile building block in analog circuits.[1–4] One type of the CCII is the negative second generation current

*FCS accounts for the floating current source and CCII– accounts for the negative second generation current conveyor.
†This paper was recommended by Regional Editor Piero Malcovati.
‡The author is currently with the University of Waterloo, Waterloo, Canada.

conveyor (CCII−) which is defined by:

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix}. \quad (1)$$

Therefore, the CCII− performs a voltage conveying action from node Y to node X and a current conveying action from node X to node Z. The input resistance r_x should be designed as small as possible since node X is a current-input and a voltage-output node. Node Z output resistance r_z should be designed as high as possible since it is a current-output node. In addition, the voltage conveying and current conveying actions should be performed as accurate as possible over a wide-band of frequencies to be suitable for high frequency applications.

The demand for accurate CMOS CCII− suitable for high frequency applications has led designers to do extra effort in finding realizations that meet these requirements.[4−20] The Floating Current Source (FCS) shown in Fig. 1(a) was introduced to be used as an output stage for current-mode feedback amplifiers.[11−13] Following that, the FCS is used as the output stage of the accurate CCII− proposed in Ref. 14 to perform the required current conveying action. The FCS has also been recently used in the realization of fully differential voltage second generation current conveyor.[4,21]

According to the literature, there is no realization of a CCII− circuit that is independent of the transistors sizing (i.e., minimum size transistors can be adopted) and layout friendly (i.e., it consists of repeated building blocks, and accordingly, the

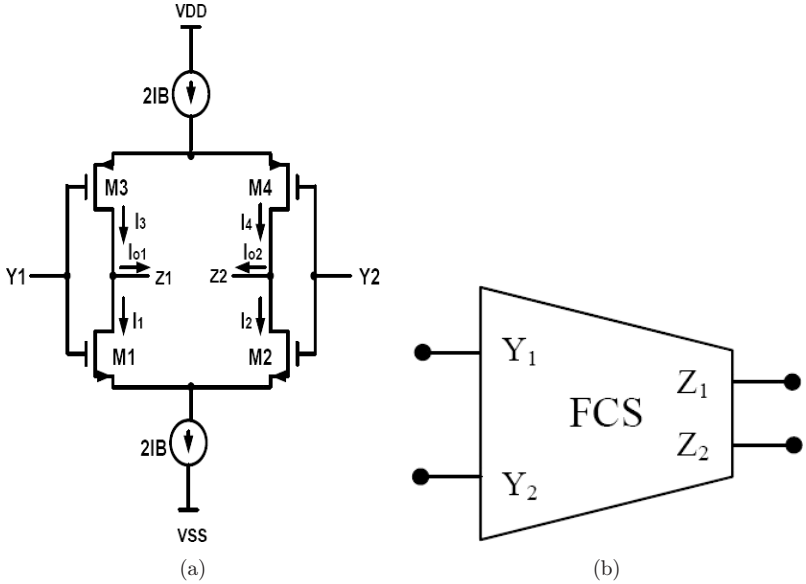

Fig. 1. (a) The floating current source (FCS)[11] and (b) its block diagram of the FCS.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com by 82.129.216.246 on 02/12/13. For personal use only.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

layout and fabrication processes are simpler). In this paper, the first proposed CCII– realization consists of three FCS blocks and the second proposed realization consists of two FCS blocks. Both realizations are independent of the transistors sizes while achieving higher bandwidth and accuracy than the circuit introduced in Ref. 14.

A novel wide-band and high accuracy FCS-based CMOS CCII– is proposed in this paper. The proposed CCII– utilizes the FCS in its voltage conveying and current conveying sections for the first time as usually the FCS is used in the CCII– for the current conveying action only. Holding a fair comparison with the FCS-based CCII– reported in Ref. 14, the proposed circuit achieves wider voltage and current transfer bandwidths. Moreover, the proposed circuit achieves higher voltage and current transfer accuracies and also less power keeping approximately all other parameters slightly with the same accuracy. Since, an essential demand of today's integrated circuits applications is to reduce the power dissipation of the analog circuits. Hence, a novel low-power version of the proposed CCII– is also presented in this paper. This low-power version dissipates less power at the expense of lower bandwidth and accuracy. This circuit is compared as well with the FCS-based CCII– reported in Ref. 14 and shows better performance in all aspects. For all the circuits examined in this paper, the supply voltages are ± 1.5 V SPICE simulations are performed with model parameters of 0.5 μm CMOS process provided by MOSIS (AGILENT).

2. The Proposed FCS-Based CCII– Circuits

2.1. *Floating current source (FCS)*

In this section, the FCS is analyzed in a way that should help in understanding the operation of the proposed FCS-based negative second generation current conveyor (CCII–). The floating current source, FCS, shown in Fig. 1(a)[11] provides two balanced output currents and its block diagram is shown in Fig. 1(b). These two output currents are given by[15]

$$I_{o1} = -I_{o2} = -\frac{1}{2} v_d \left[\sqrt{K_n} \sqrt{2I_B - \frac{K_n v_d^2}{4}} + \sqrt{K_p} \sqrt{2I_B - \frac{K_p v_d^2}{4}} \right], \tag{2}$$

where

$$v_d = V_1 - V_2 \,. \tag{3}$$

V_1 and V_2 are the voltages applied to Y_1 and Y_2, respectively; $2I_B$ is the FCS bias current; and K_n and K_p are technology parameters of the nMOS and pMOS transistors, respectively, and given by

$$K_n = \mu_n C_{ox} \frac{W1}{L1} \,, \tag{4}$$

$$K_p = \mu_p C_{ox} \frac{W3}{L3} \,, \tag{5}$$

where μ_n and μ_p are the mobility of the nMOS and pMOS transistors, respectively; C_{ox} is the oxide capacitance per unit area; and $\frac{W1}{L1}$ and $\frac{W3}{L3}$ are the aspect ratios of transistors $M1$ and $M3$, respectively.

According to Eq. (2), the FCS is usually used for the current conveying action of the CCII− since it provides two balanced output currents, I_{o1} and I_{o2}, which are equal in magnitudes and out of phase by 180°. The novel idea in this paper is to use this FCS in the voltage conveying action as well. This is accomplished by forcing these two output currents to be zero (i.e., $I_{o1} = -I_{o2} = 0$). Consequently, the voltage difference $v_d = 0$ and therefore, $V_1 = V_2$.

2.2. *Novel accurate wide-band FCS-based CCII–*

The CMOS realization of the proposed accurate wide-band FCS-based CCII− is shown in Fig. 2. The voltage conveying action is provided using negative feedback in this proposed circuit. Moreover, this proposed circuit allows independent control of the CCII− voltage conveying and current conveying dynamic ranges. The utilization of two cascaded gain stages results in a small impedance level at the input node of the proposed CCII−, as well as voltage and current gains very close to unity. The block diagram of this realization is shown in Fig. 3. All the transistors (M_1−M_{12}) are matched. Assuming that all the transistors operate in the saturation region, the operation of the circuit can be explained as follows. The first FCS (M_1−M_4) provides two output balanced currents I_{o1} and I_{o2} which are given by Eq. (2) where $v_d = v_x - v_y$. The second FCS (M_5−M_8) provides also two output balanced currents I_{o3} and I_{o4} which are also given by the same Eq. (2).

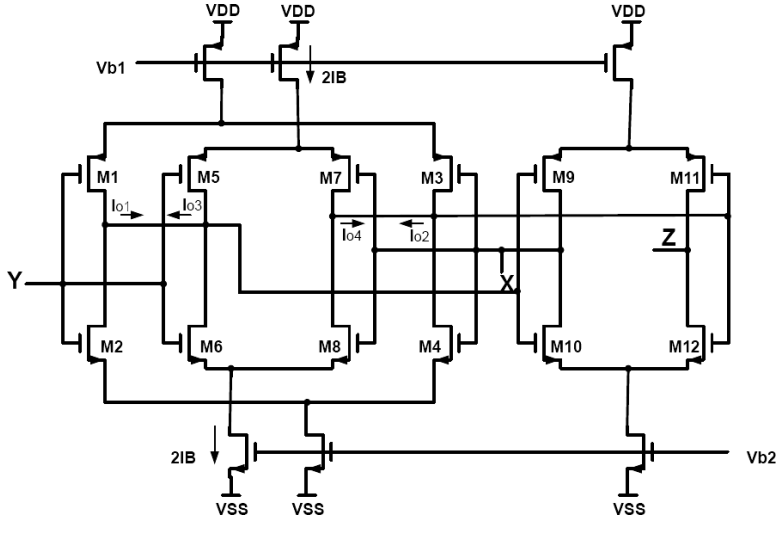

Fig. 2. The proposed accurate wide-band FCS-based CCII–.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com by 82.129.216.246 on 02/12/13. For personal use only.

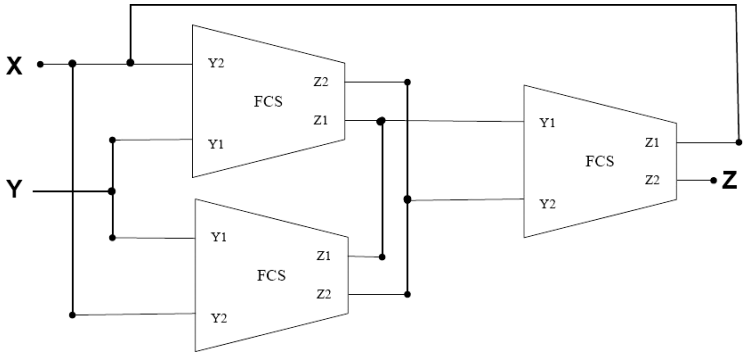

Fig. 3. Block diagram of the circuit shown in Fig. 2.

The currents I_{o1}, I_{o2}, I_{o3} and I_{o4} are forced to be zero currents and from Eq. (2) we have $v_d = 0$ and, consequently, $v_x = v_y$ and the voltage at terminal X will follow the voltage at terminal Y. The third FCS is responsible for conveying the X terminal current to the Z terminal. It should be noted that the FCS is used as the only building block in this proposed circuit.

Taking the finite value of the transistor transconductance g_m and drain to source conductance g_d into consideration, the small signal voltage transfer gain from the Y terminal to the X terminal is approximately given by:

$$A_v = \frac{v_x}{v_y} = \frac{1}{1 - \frac{(g_{d3}+g_{d4})(g_{d7}+g_{d8})(g_{d9}+g_{d10})}{(g_{m1}+g_{m2})(g_{m5}+g_{m6})(g_{m9}+g_{m10})}} \,. \tag{6}$$

The small signal input resistance seen at terminal X is approximately given by:

$$r_x = \frac{(g_{d3}+g_{d4})(g_{d7}+g_{d8})}{(g_{m1}+g_{m2})(g_{m5}+g_{m6})(g_{m9}+g_{m10})} \,. \tag{7}$$

The small signal current transfer gain between the X and Y terminals is approximately given by:

$$A_i = \frac{i_z}{i_x} = -\frac{1 + \frac{g_{o1}+g_{do2}}{2(g_{m9}+g_{m10})}}{1 - \frac{g_{o1}+g_{do2}}{2(g_{m9}+g_{m10})}} \,, \tag{8}$$

where g_{o1} and g_{o2} are the effect of non-ideal current sources in the circuit that will be represented by CMOS transistors and they are equal to the drain to source conductance of the biasing transistors. The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d11} + g_{d12}} \,. \tag{9}$$

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

The main advantages of this proposed three FCS blocks CCII− are the systematic layout by using three similar blocks of the FCS circuit and the independence of the transistors aspect ratios. In addition, this proposed circuit achieves higher design metrics than the circuit introduced in Ref. 14 as will be explained in Sec. 3.

2.3. *Low-power FCS-based CCII−*

The novel accurate wide-band FCS-based CCII− shown in Fig. 2 withdraws large standby currents due to using three FCS blocks. To minimize the power dissipation, only two FCS are used to realize the CCII− in this section. This circuit consumes less power at the expense of lower bandwidth and accuracy as will be shown in this section. This proposed two FCS-based CCII− is shown in Fig. 4. The block diagram of this circuit is shown in Fig. 5. All the transistors (M_1−M_{12}) are matched. Assuming that all the transistors operate in the saturation region, the operation of the circuit is similar to the proposed CCII− shown in Fig. 2. The first FCS (M_1−M_4) provides two output balanced currents that are forced to be zero and from Eq. (2) the voltage at terminal X will follow the voltage at terminal Y. The second FCS is responsible for conveying the X terminal current to the Z terminal. The connection between nodes Y_2 and Z_2 shown in Fig. 5 is used to control the input common mode voltage of the current conveying FCS. This is not performed in the circuit shown in Fig. 2 since the parallel FCS architecture used for the voltage follower stage helps in controlling it.

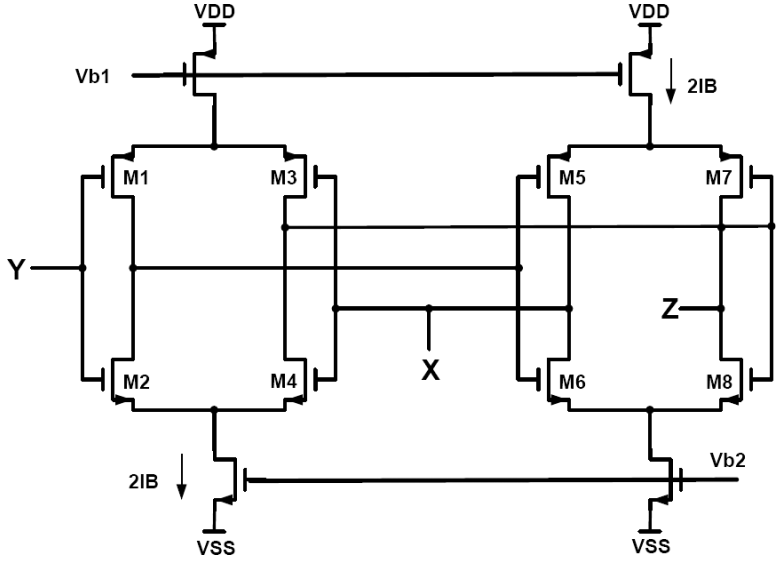

Fig. 4. The low-power version of the FCS-based CCII−.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

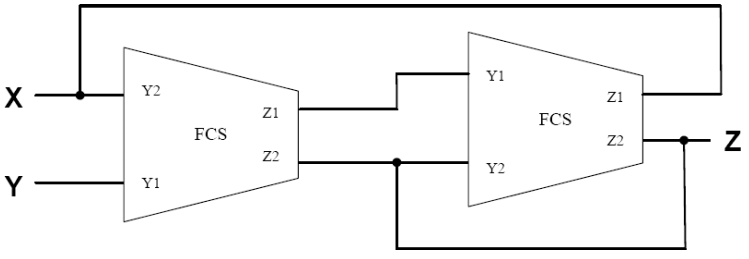

Fig. 5. Block diagram of the circuit shown in Fig. 4.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

The small signal voltage transfer gain from the Y terminal to the X terminal is approximately given by:

$$A_v = \frac{v_x}{v_y} = \frac{1}{1 - \frac{(g_{d3}+g_{d4})(g_{d5}+g_{d6})}{(g_{m1}+g_{m2})(g_{m5}+g_{m6})}} . \tag{10}$$

The small signal input resistance seen at terminal X is approximately given by:

$$r_x = \frac{(g_{d3} + g_{d4})}{(g_{m1} + g_{m2})(g_{m5} + g_{m6})} . \tag{11}$$

The small signal current transfer gain between the X and Z terminals is approximately given by:

$$A_i = \frac{i_z}{i_x} = -\frac{1 + \frac{g_{o1}+g_{do2}}{2(g_{m5}+g_{m6})}}{1 - \frac{g_{o1}+g_{do2}}{2(g_{m5}+g_{m6})}} . \tag{12}$$

The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d7} + g_{d8}} . \tag{13}$$

By using Eqs. (6) and (10), comparing the voltage transfer gain of this low-power circuit with the first proposed circuit shown in Fig. 2 shows that for the same transistor parameters (i.e, all transistors have the same sizing), the first proposed CCII– exhibits $A_v = \frac{1}{1-(g_d/g_m)^3}$ while the low-power version provides a voltage transfer gain of $A_v = \frac{1}{1-(g_d/g_m)^2}$. As a numerical example, for transistor sizes of $50\,\mu$m/$1\,\mu$m and $I_B = 50\,\mu$A, $g_d/g_m \approx 0.03$. Therefore, the first proposed CCII– exhibits $A_v = \frac{1}{1-(0.03)^3} = 1.000027$ while the low-power version provides a voltage transfer gain of $A_v = \frac{1}{1-(0.03)^2} = 1.0009$. Thus, the first proposed CCII– exhibits more accurate voltage following action. Similarly, by using Eqs. (7) and (11), the first proposed circuit input resistance, r_x, is 33.3X lower than that of the low-power CCII–. The current transfer gain, A_i and the output resistance r_z are equal for the two proposed circuits. The main advantage of the second proposed CCII– is its low-power consumption

since it utilizes only two FCS blocks while the first proposed circuits utilizes three FCS blocks.

3. Comparison with Previous FCS-Based CCII–[14]

The CMOS realization of the CCII– proposed in Ref. 14 is shown in Fig. 6. The input stage is implemented using a simple differential amplifier (M_1-M_5), while the output stage is implemented using the FCS stage (M_6-M_{13}). The block diagram of this two-gain stage configuration is shown in Fig. 7. Assuming that each of the groups of the transistors (M_1 and M_2), (M_3 and M_4) as well as (M_6-M_9) are matched and all the transistors operate in the saturation region, the circuit operation can be explained as follows. The structure is based on the long tail differential pair (M_1 and M_2). The current mirror formed by M_3 and M_4 forces equal currents (I_B) in the transistors M_1 and M_2. This operation drives the gate to source voltages of M_1 and M_2 to be equal and, consequently, forces the voltage at terminal X to follow the voltage at terminal Y. The FCS stage is responsible for conveying the X terminal current to the Z terminal.

The small signal voltage transfer gain from the Y terminal to the X terminal is given approximately by:

$$A_v = \frac{v_x}{v_y} = \frac{1}{1 - \frac{(g_{d2}+g_{d4})(g_{d6}+g_{d8})}{g_{m2}(g_{m6}+g_{m8})}} \,. \tag{14}$$

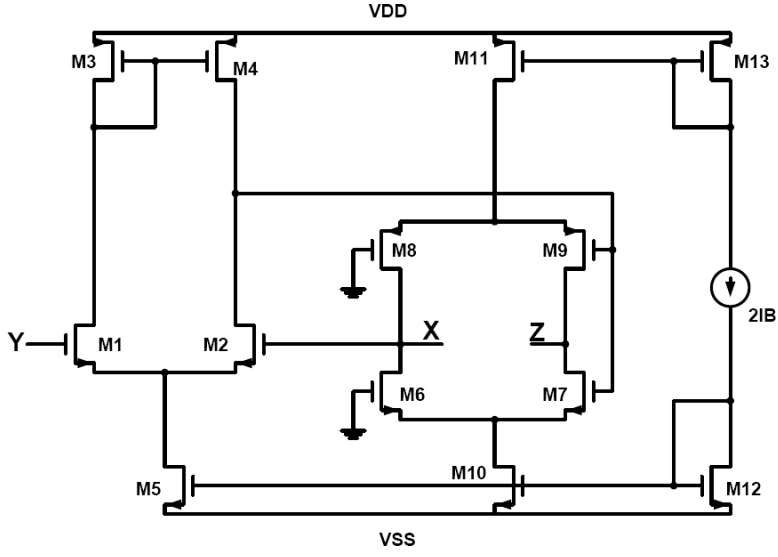

Fig. 6. CCII– realization proposed in Ref. 14.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

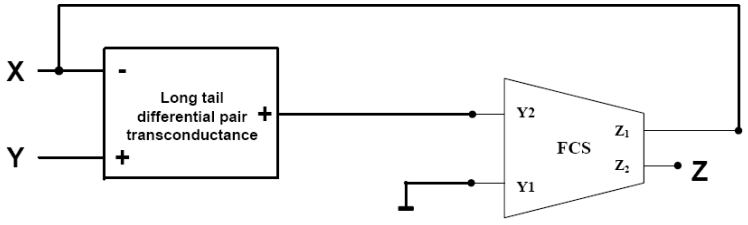

Fig. 7. Block diagram of the circuit shown in Fig. 6.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

The small signal input resistance seen at terminal X is given approximately by:

$$r_x = \left(\frac{2(g_{d2}+g_{d4})}{g_{m2}(g_{m6}+g_{m8})}\right) \Big\| \left(\frac{2}{g_{d6}+g_{d8}}\right). \tag{15}$$

The small signal current transfer gain between the X and Z terminals is given approximately by:

$$A_i = \frac{i_z}{i_x} = -\frac{1+\frac{g_{d10}+g_{d11}}{2(g_{m6}+g_{m8})}}{1-\frac{g_{d10}+g_{d11}}{2(g_{m6}+g_{m8})}}. \tag{16}$$

The output resistance at terminal Z is given by

$$r_z = \frac{1}{g_{d7}+g_{d9}}. \tag{17}$$

By comparing the voltage transfer gain of the CCII− in Ref. 14 given in Eq. (14) (i.e., $A_v = \frac{1}{1-2(g_d/g_m)^2}$) with those of the proposed CCII− circuits given in Eqs. (6) and (10) (i.e., $A_v = \frac{1}{1-(g_d/g_m)^3}$ and $A_v = \frac{1}{1-(g_d/g_m)^2}$), it is evident that the two proposed circuits provide better voltage tracking accuracy than that in Ref. 14. Moreover, the proposed CCII− realizations provide lower input resistance r_x. In addition, the current tracking accuracy and the output resistance r_z are equal in all circuits.

Therefore, the proposed CCII− circuit realizations have the advantage of systematic layout and independent transistors sizing. In addition, they have smaller Silicon area, better accuracy, higher bandwidth, and lower power consumption than the circuit proposed in Ref. 14 while keeping all other parameters slightly constants.

4. Simulation Results and Discussions

The proposed FCS-based CCII− circuits are simulated using equal transistors aspect ratios of 50 μm/1 μm. The biasing current $2I_B = 100\,\mu$A (Using $V_{b1} = 0.12$ volts and $V_{b2} = 0.59$ volts). The transistors sizes and the bias current are the same for all circuits to hold a fair comparison. Simulation results are tabulated in Table 1 and shown for the first proposed circuit in Figs. 8−10 while the second proposed circuit simulation results are shown in Figs. 11−13.

Table 1. Performance parameters of the circuits shown in Figs. 2, 4, and 6.

Parameter	The CCII− given in Ref. 14	The first proposed CCII−	The second proposed CCII−	Unit
Input voltage dynamic range	−0.9 to 1	−0.47 to 0.47	−0.9 to 1.02	V
Voltage offset range	4.7 to 5	0 to 0.3	−0.3 to 0.1	mV
A_v (average value) of open circuit voltage transfer gain	1.003245	1.000043	1.001231	V/V
Open loop gain (voltage section)	66	89	83	dB
3-dB bandwidth of open circuit voltage transfer gain	516	972	578	MHz
Input current dynamic range	−100 to 100	−100 to 100	−100 to 100	μA
Current offset range	0.7 to −6	0	0	μA
A_v (average value) of short circuit current transfer gain	−0.99992	−0.99996	−0.99997	A/A
3-dB bandwidth of short circuit current transfer gain	22	378	561	MHz
r_x	18.7	3.7	13.4	Ω
Power dissipation	0.79	0.62	0.41	mW

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

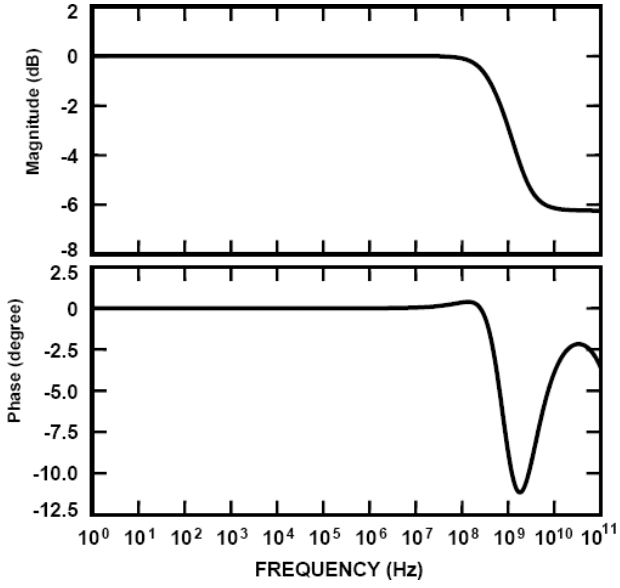

Fig. 8. Frequency characteristics (log scale) of the open circuit voltage transfer gain between Y and X (VX/VY) for the circuit shown in Fig. 2.

The CCII− circuit proposed in Ref. 14 is also simulated to provide a fair comparison using transistors aspect ratios as reported in Table 2. This CCII− circuit is compensated by using two capacitors $C_1 = 5\,\text{pF}$ (connected between the gate of M_7 and the drain of M_{10}) and $C_2 = 5\,\text{pF}$ (connected between the gate of M_7 and the

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

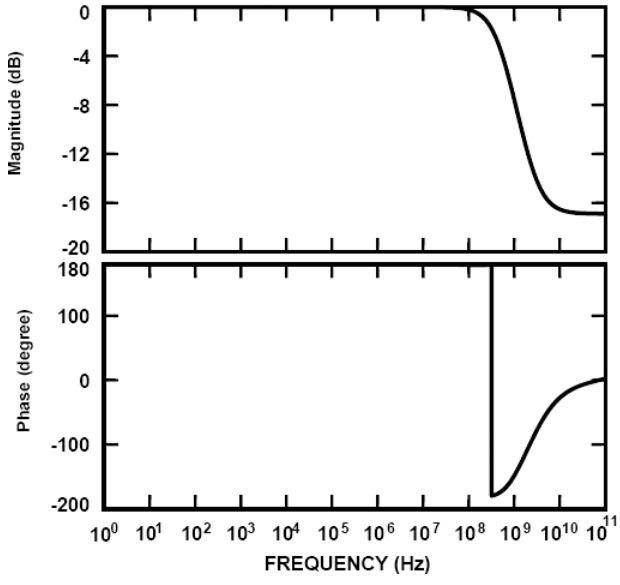

Fig. 9. Frequency characteristics (log scale) of the short circuit current transfer gain between X and Z (IZ/IX) for the circuit shown in Fig. 2.

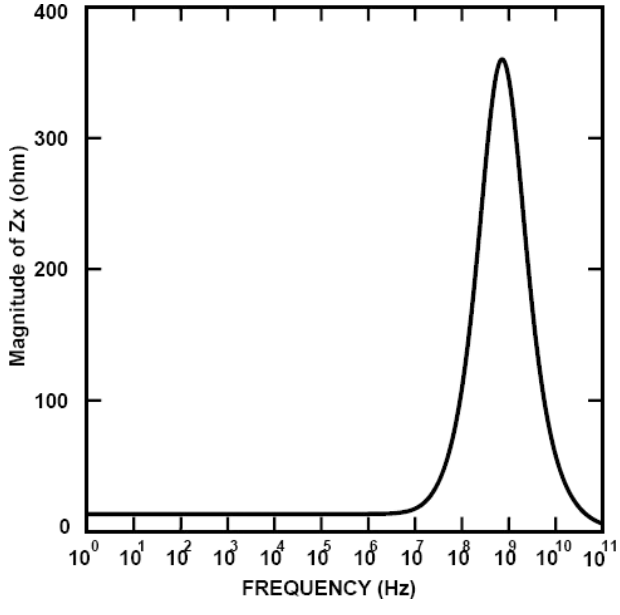

Fig. 10. Input impedance at terminal X versus frequency (log scale) for the circuit shown in Fig. 2.

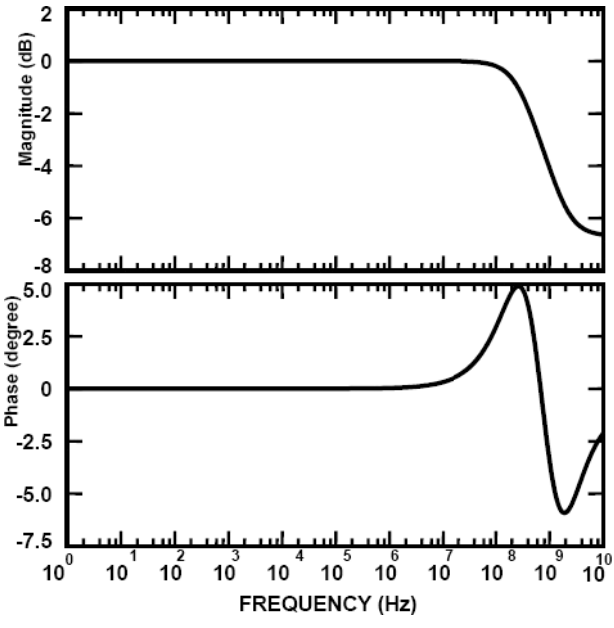

Fig. 11. Frequency characteristics (log scale) of the open circuit voltage transfer gain between Y and X (VX/VY) for the circuit shown in Fig. 4.

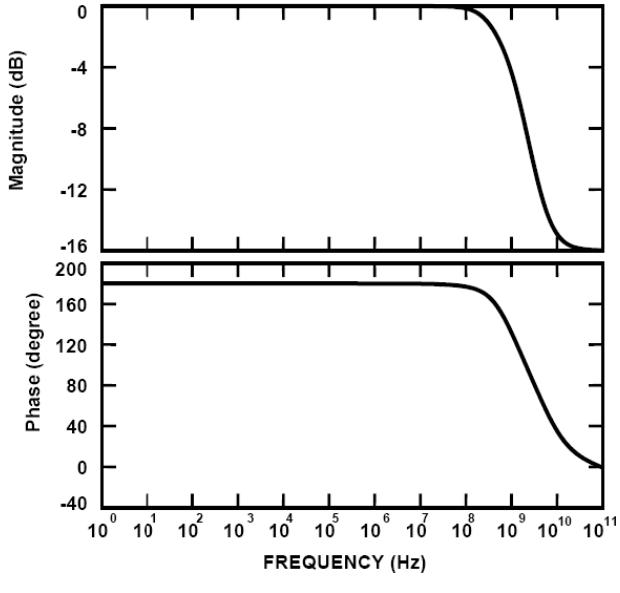

Fig. 12. Frequency characteristics (log scale) of the short circuit current transfer gain between X and Z (IZ/IX) for the circuit shown in Fig. 4.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

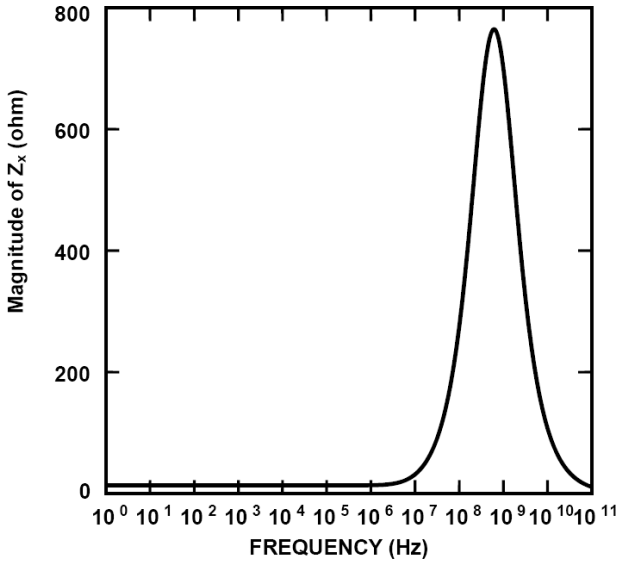

Fig. 13. Input impedance at terminal X versus frequency (log scale) for the circuit shown in Fig. 4.

Table 2. Transistor aspect ratios of the circuit shown in Fig. 6.

Transistor	$W(\mu\text{m})/L(\mu\text{m})$
M_1, M_2, M_6–M_9	50/1
M_3, M_4	50/2.5
M_5, M_{10}–M_{13}	100/2.5

drain of M_{11}). The biasing current $2I_B = 100\,\mu$A. Simulation results are tabulated in Table 1.

It is important to note that the FCS reported in Refs. 11 to 13 is used as an output current follower stage for the CCII− but the strength of this novel CCII− circuit realization shown in Fig. 2 is using the FCS block for both the input voltage follower and the output current follower stages. Moreover, the mismatch between the bias transistors can be controlled through the sizing since the mismatch is inversely proportional to the square root of the transistor gate area.[22,23] One of the key points of the proposed FCS-based circuits is that there are no constraints on the transistor sizes. Hence, the mismatch can be controlled by increasing the transistors sizing under performance metrics constraints. Accordingly, they provide systematic layout and arbitrary transistors sizes.

From Table 1, it is evident that the first proposed circuit exhibits better voltage following accuracy, lower voltage and current offset ranges, and higher open loop

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

gain compared to the circuit reported in Ref. 14. Moreover, the first proposed circuit voltage transfer bandwidth and current transfer bandwidth are 1.9X and 17.2X, respectively, higher compared to the circuit proposed in Ref. 14. In addition, this first proposed circuit has 5X lower input resistance and 1.3X lower power consumption than that of the CCII− reported in Ref. 14. All other parameters are the same with one exception of the input voltage dynamic range which is better in the CCII− introduced in Ref. 14. The low-power CCII− provides better performance than the circuit proposed in Ref. 14 in all performance parameters while its power consumption is 1.9X lower than that of the CCII− circuit in Ref. 14. This discussions and results show the strength of the proposed circuits in comparison with the only FCS-based CCII−, up to the author knowledge. One more advantage of the proposed circuits is that no compensation capacitors are needed in them which allows them to exhibit higher bandwidth than that in Ref. 14.

Moreover, the transient response of the closed loop circuit is simulated for an input square wave at terminal Y of the first proposed CCII− in Fig. 2. The input square wave has 0.8 V peak to peak amplitude, 1 GHz fundamental frequency, and 1 ps rise time. The output at terminal X is shown in Fig. 14. It is evident that it represents a faithful replica of the input square wave with no overshoots or oscillations.

In addition, post-layout simulations are conducted on the two proposed CCII− circuits. Transistor level simulations backannotated with parasitic capacitances extracted from the layout are used to compute all the figure of merits again for the two proposed CCII− realizations in Figs. 2 and 4. The results are in very good agreement with the pre-layout simulations with a maximum error of 6.2% and an average error of 3.6%.

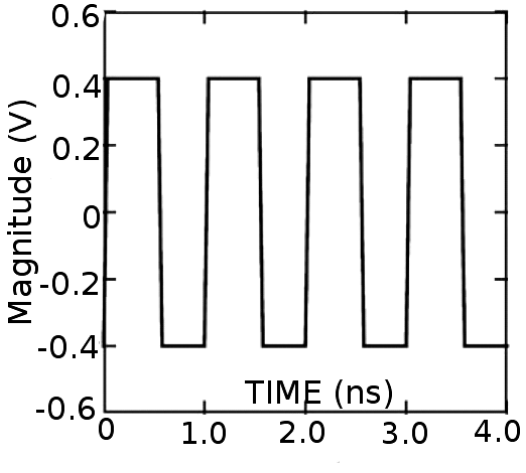

Fig. 14. The transient response of the CCII− circuit shown in Fig. 2.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

Monte Carlo analysis, including mismatch between transistors, is conducted for the two proposed CCII– realizations. The low power CCII– shown in Fig. 4 shows a voltage tracking accuracy standard deviation percentage of 3.3% and a current tracking accuracy standard deviation percentage of 2.9%. These values are larger than that of the first CCII– realization shown in Fig. 2 by a factors of 1.2X and 1.5X. The standard deviation percentage equals the ratio between the standard deviation and the nominal value ($\sigma/\mu(\%)$). These results show that the two proposed CCII– realizations are insensitive to process variations and transistors mismatch. Finally, the proposed CCII– realizations in Figs. 2 and 4 have been found to be practically insensitive to temperature variations over the -30 to 110°C range, thanks to the feedback loop.

5. Applications Using the Proposed CCII–

5.1. *Inverting transconductance amplifier*

The transconductance amplifier configuration is shown in Fig. 15. The transconductance gain is given by:

$$\text{Transconductance gain} = \frac{I_o}{V_i} = -\frac{1}{R}\,. \tag{18}$$

The transconductance amplifier is simulated using $R = 1\,\Omega, 10\,\Omega, 0.1\,\text{k}\Omega, 1\,\text{k}\Omega$ and $10\,\text{k}\Omega$. The different gains of the inverting transconductance amplifier are shown in Fig. 16. It is evident that the bandwidth is around 400 MHz and that increasing the transconductance amplifier gain slightly affects the bandwidth. Therefore, the gain bandwidth product is not constant, which is the main advantage of using CCII– over conventional operational amplifiers, which suffer from constant gain bandwidth product.

5.2. *Inverting current integrator*

The CCII– has precise unity voltage gain between nodes X and Y as well as precise unity gain between nodes Z and X. Therefore, the CCII– can be used in amplifier

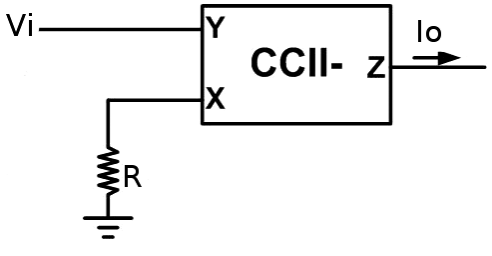

Fig. 15. Simple inverting transconductance amplifier as an application for the CCII– shown in Fig. 4.

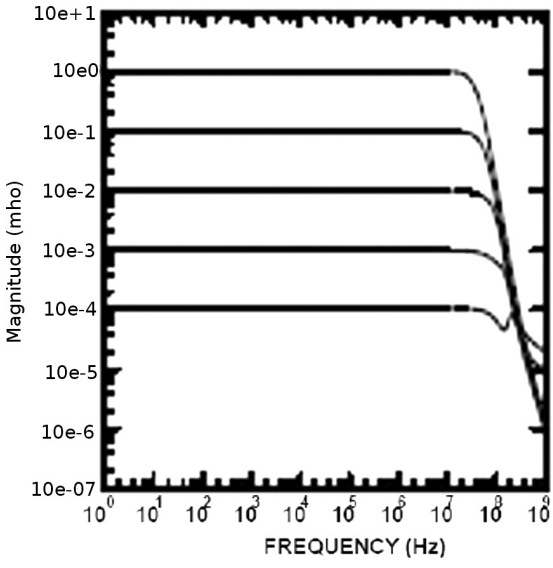

Fig. 16. Frequency characteristics of the transconductance gain magnitude of the transconductance amplifier configuration shown in Fig. 15.

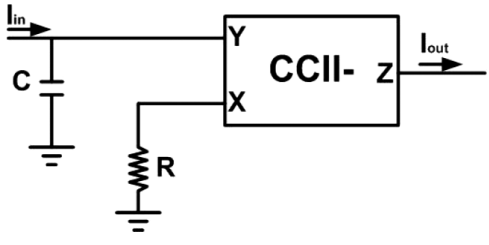

Fig. 17. Simple inverting current integrator as an application for the CCII− shown in Fig. 4.

applications without any overall negative feedback. The advantage of this approach is that the traditional closed loop gain-bandwidth trade-off of negative feedback operational amplifier is avoided. However, to maintain a high level of accuracy without the use of negative feedback, a high quality CCII− realization should be employed.

Figure 17 shows a simple CCII− based inverting current integrator.[1–3] The resistor R should be fairly small to minimize the stray capacitance at node X. This integrator circuit is simulated using the two proposed CCII− circuits with $R = 100\,\Omega$ and $C = 100\,\mathrm{p}F$. Figure 18 shows the current integrator gain and phase versus frequency using the low-power CCII− shown in Fig. 4. It can be noticed that the cut-off frequency of this integrator circuit is about 16.1 MHz which equals approximately $1/(2\pi RC)$.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

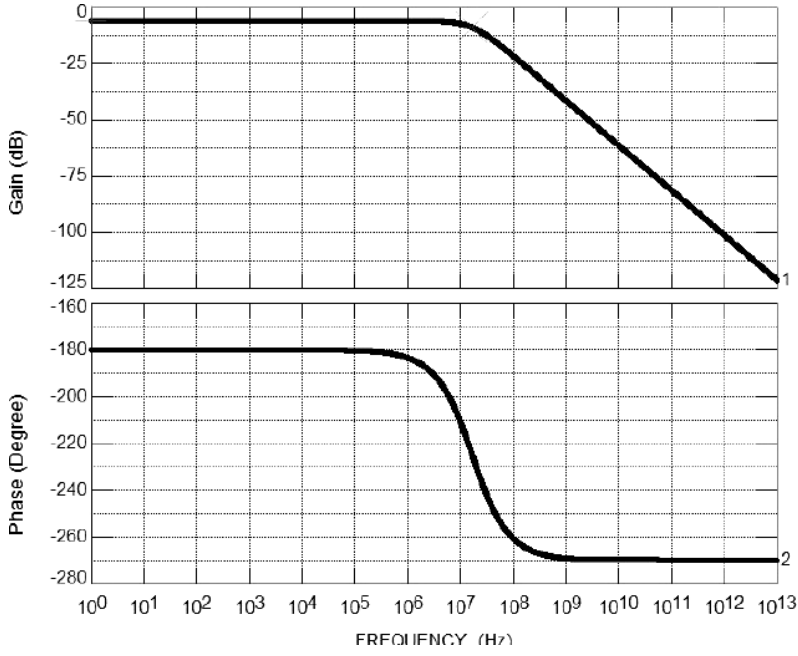

Fig. 18. The gain magnitude (dB) and phase (Degree) of the inverting current integrator shown in Fig. 17.

6. Conclusion

A novel accurate FCS-based CCII− circuit suitable for high frequency applications is given. Simulation results and fair comparisons between the proposed CCII− and the CCII− reported in Ref. 14, proved the strength of the proposed circuit realization. Targeting a remarkable reduction in the power dissipation, the low-power version of the proposed circuit is also given. The proposed circuits have better performance metrics as well as they are layout-friendly, independent of the transistors sizes, and require no compensation capacitances.

References

1. A. S. Sedra and K. C. Smith, The current conveyor — A new circuit building block, *IEEE Proc.* (1968), pp. 1368−1369.
2. A. S. Sedra and K. C. Smith, A second generation current conveyor and its applications, *IEEE Trans. Circuit Theory* (1970), pp. 132−134.
3. F. Gohh, G. W. Roberts and A. S. Sedra, The current conveyor: History, progress and new results, *IEE Proc.* (1990), pp. 63−77.
4. H. Mostafa and A. M. Soliman, Novel low-power accurate wide-band CMOS negative-second-generation-current-conveyor realizations based on floating-current-source building blocks, *Proc. IEEE Toronto Int. Conf. Science and Technology for Humanity 2009* (*TIC-STH 2009*) (2009), pp. 720−725.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com
by 82.129.216.246 on 02/12/13. For personal use only.

5. W. Surakampontorn, V. Riewruja, K. Kumwachara and K. Dejhan, Accurate CMOS based current conveyors, *IEEE Trans. Inst. Measurements* (1995), pp. 699−702.
6. G. Palmisano and G. Palumbo, A simple CMOS CCII+, *Int. J. Circuit Theory and Applications* (1995), pp. 599−603.
7. S. Liu, H. Tsao and J. Wu, CCII based continuous time filters with reduced gain bandwidth sensitivity, *IEE Proc.* (1991), pp. 210−216.
8. A. M. Ismail and A. M. Soliman, Wideband CMOS current conveyor, *Electronic Letters* (1998), pp. 2368−2369.
9. U. Yodprasit, High-precision CMOS current conveyor, *Electronic Letters* (2000), pp. 609−610.
10. T. Laopoulos, S. Sisko, M. Bafleur and Ph. Givelin, CMOS current conveyor, *Electronic Letters* (1992), pp. 2261−2262.
11. H. O. Elwan and A. M. Soliman, Low-voltage low-power CMOS current conveyors, *IEEE Trans. Circuits Systems I* (1997), pp. 828−835.
12. A. F. Arbel and L. Goldminz, Output stage for current-mode feedback amplifiers, theory and applications, *Analog Integrated Circuits and Signal Processing* (1992), pp. 234−255.
13. A. F. Arbel, Towards a perfect CMOS CCII, *Analog Integrated Circuits and Signal Processing* (1997), pp. 119−132.
14. A. F. Arbel, Review of research on ASP by the author, *IEEE Trans. Circuits Systems II* (2001), pp. 599−611.
15. I. A. Awad and A. M. Soliman, New CMOS realization of the CCII−, *IEEE Trans. Circuits Systems II* (1999), pp. 460−463.
16. M. A. Youssef and A. M. Soliman, A modified CMOS balanced output transconductor with extended linearity, *Analog Integrated Circuits and Signal Processing* (2003), pp. 239−244.
17. E. Bruun, CMOS current conveyors, *IEEE Int. Symp. Circuits and Systems* (1994), pp. 632−641.
18. F. Centurelli, A. D. Grasso, S. Pennisi, G. Scotti and A. Trifiletti, CMOS high-CMRR current output stages, *IEEE Trans. Circuits Syst. II* **54** (2007) 745−749.
19. S. Pennisi, A low-voltage design approach for class AB current-mode circuits, *IEEE Trans. Circuits Syst. II* **49** (2002) 273−279.
20. R. Mita, G. Palumbo and S. Pennisi, 1.5-V CCII+ with high current-driving capability, *IEEE Trans. Circuits Syst. II* **50** (2003) 187−190.
21. H. Mostafa, Novel high performance CMOS analog building blocks suitable for analog signal processing, Master Thesis, Cairo University, Egypt (2005).
22. E. A. Sobhy and A. M. Soliman, Realizations of fully differential voltage second generation current conveyor with an application, *Int. J. Circuit Theory and Applications* (2008).
23. M. J. M. Pelgrom, H. P. Tuinhout and M. Vertregt, Transistor matching in analog CMOS applications, *Int. Electron Devices Meeting* (*IEDM '98*) *Technical Digest* (1998), pp. 915−918.

J CIRCUIT SYST COMP 2010.19:997-1014. Downloaded from www.worldscientific.com by 82.129.216.246 on 02/12/13. For personal use only.