*Frequenz*
*60 (2006)*
*11-12*

# Novel Accurate Wideband CMOS Current Conveyor

By Hassan M. Hassan, Ahmed M. Soliman

***Abstract*** – Novel CMOS Class-A positive type second generation current conveyor (CCII) suitable for high frequency applications is proposed. It provides accurate voltage and current tracking as well as low input impedance.

***Index Terms*** – wideband, CMOS current conveyor, analog circuits

## 1. Introduction

In 1968 Smith and Sedra introduced the first generation current conveyor (CCI) [1] and in 1970 the second generation current conveyor (CCII) was proposed by the same two authors [2]. Since then the CCII, which is essentially a combined voltage and current follower, has proved to be functionally flexible and versatile [3]. The demand for accurate CCII suitable for high frequency applications has led designers to find CCII realizations that meet these requirements [4-10]. Some of these realizations target higher accuracy but lose bandwidth in return [7].

In this paper, a novel accurate and wideband CCII is proposed. It resembles Yodprasit CCII proposed in [7] (Fig. 1). The proposed realization (Fig. 2) is based on a new idea. Its voltage follower section is based on a differential amplifier to equate the source voltages of the input transistors (M1 and M2) while their drains are connected. This addition of source follower sections at the input stage enables the proposed CCII to achieve high accuracy while providing wider voltage and current transfer bandwidths.

For all the circuits examined in this paper, the supply voltages are ± 1.5 V. TOP SPICE simulations were carried out with model parameters of 0.5 μm CMOS process provided by MOSIS (AGILENT).

## 2. Novel accurate and wideband CCII

### 2.1 Circuit description

The CMOS realization of the proposed wideband and low input resistance CCII is shown in Fig. 2. The groups of the transistors (M1-M4), (M5 and M7), (M8 and M9), (M10 and M11), (M13 and M15) as well as (M16 and M17) are matched. Assuming that

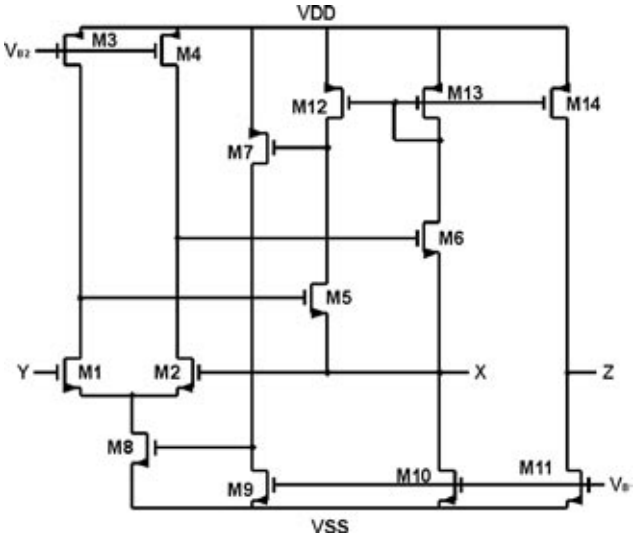


Fig. 1: The CCII realization reported in [7]

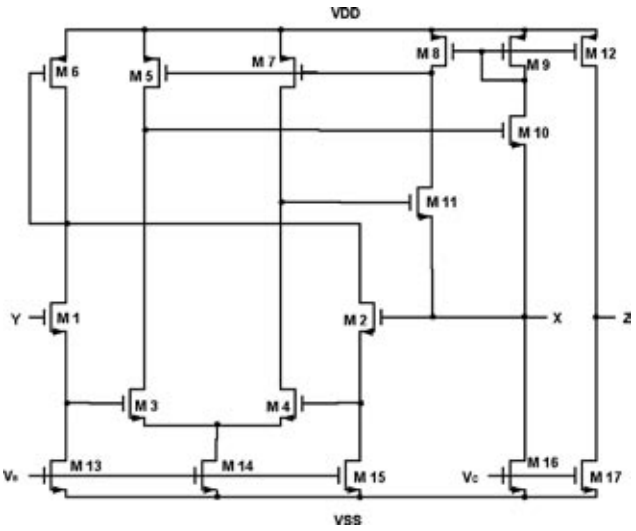


Fig. 2: The proposed wideband and low input resistance CCII

all the transistors operate in the saturation region, the operation of the circuit can be explained as follows. M13, M14, M15, M16 and M17 serve as DC current sources. M13, M15, M16 and M17 hold IB each, while M14, M16 and M17 hold 2IB each. The current mirror formed by M5 and M7 forces equal currents IB in the transistors M3 and M4. This operation drives the gate-to-source voltages of M3 and M4 to be equal and, consequently, forces the voltage at the source of M1 to be equal to the voltage at the source of M2. Since M1 and M2 are biased by equal currents IB. The voltage at terminal Y will be conveyed to terminal X. the source followers used at the input stage provide wider bandwidth compared to Yodprasit CCII introduced in [7].Current mirrors formed by (M8, M9 and M12) are responsible of conveying the current at terminal X to the terminal Z.

The block diagram of the proposed wideband and low resistance CCII+ is shown in Fig. 3. It consists of the following: a differential input transconductance amplifier which is implemented by (M3 and M4) where G3 = gm3 = gm4 and five transconductance amplifiers where G1 = G2 = gm1, G4 = gm11 = G5 = gm10, G6 = gm12, G7 = gm8, G8 = gm5 = G9 = gm7. The voltage following action is a result of the negative feedback closed loop structure implemented by blocks G2, G3 and G4. In this manner, both accuracy in the voltage transfer gain and low resistance at terminal X are achieved for high open loop gains.

Taking the finite value of the transistor transconductance $g_m$ and drain to source conductance $g_d$ into consideration, the small signal voltage transfer gain from the Y terminal to the X terminal is given approximately by:

$$A_v = \frac{V_x}{V_y} = \frac{g_{m3}g_{m5}g_{m8}g_{m10}}{g_{m3}g_{m5}g_{m8}g_{m10} + (g_{d3}+g_{d5})^2(g_{d9}+g_{d10})(g_{d8}+g_{d11})}$$

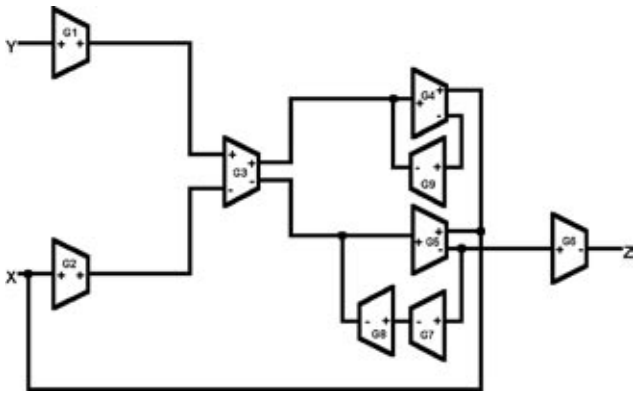


Fig. 3: Block diagram of the circuit shown in Fig. 2

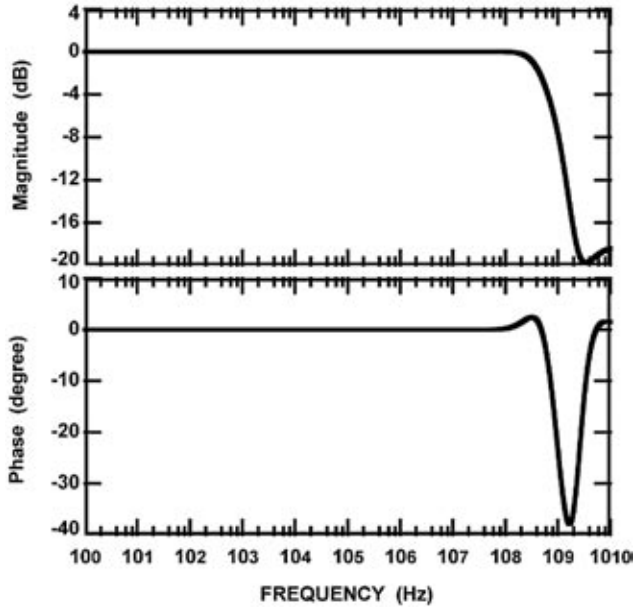


Fig. 4: Frequency characteristics of the open circuit voltage transfer gain between Y and X (VX/VY) for the circuit shown in Fig. 2

The small signal input resistance seen at terminal X is given approximately by:

$$r_x = \frac{(g_{d3}+g_{d5})^2(g_{d9}+g_{d10})(g_{d8}+g_{d11})}{(g_{d10}+g_{d11}+g_{d16})(g_{m3}g_{m5}g_{m8}g_{m10}+(g_{d3}+g_{d5})^2(g_{d9}+g_{d10})(g_{d8}+g_{d11}))}$$

The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d12}+g_{d17}}$$

### 2.2 Simulation results

Transistors aspect ratios are reported in Table 2. Simulation results are tabulated in Table 3 and shown in Figs. 3, 4, and 5. These results can be described as follows. The input voltage range is from -1V to 0.3V. The voltage offset varies from 1mV to -0.2mV within the input voltage range. The average value of the open circuit voltage transfer gain equals 0.99996. The open loop gain of the voltage section equals 88dB. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 536 MHz (Fig. 3). The input current range is from -100μA to 100μA. The current offset varies from 0.16μA to 7.5μA within the input current range. The average value of the short circuit current transfer gain equals 0.98211. The short circuit current transfer bandwidth exhibits a 3-dB frequency of 107 MHz (Fig. 4).The input resistance at terminal X at DC equals 0.82 Ω (Fig. 5). The total harmonic distortion (THD) of an input sinusoid of frequency 100 KHz and amplitude 0.5V peak to peak is 0.005%. The power dissipation of the circuit equals 0.87 mW.

Table 1: Transistors aspect ratios of the circuit shown in Fig.1

| Transistor | W(μm)/L(μm) |
|---|---|
| M1,M2 | 50/1 |
| M3,M4,M10,M11 | 20/2.5 |
| M5,M6 | 40/0.5 |
| M7,M12,M13 | 50/2.5 |
| M8 | 40/2.5 |
| M9 | 10/2.5 |
| M14 | 100/2.5 |

Table 2: Transistors aspect ratios of the circuit shown in Fig. 2

| Transistor | W(μm)/L(μm) |
|---|---|
| M1-M4 | 50/1 |
| M5-M9 | 50/2.5 |
| M10,M11 | 40/0.5 |
| M12 | 100/2.5 |

Also, the transient response of the closed loop circuit is simulated for an input square wave at terminal Y. The input square wave has 0.4V peak to peak amplitude, 0.5 MHz fundamental frequency and 1ns rise time. The output at terminal X is shown in Fig. 6. It can be noticed that it represents a faithful replica of the input square wave with no overshoots or oscillations.

A fair comparison can be held between the proposed CCII+ and Yodprasit CCII+ reported in [7]. From Table 3, it can be observed

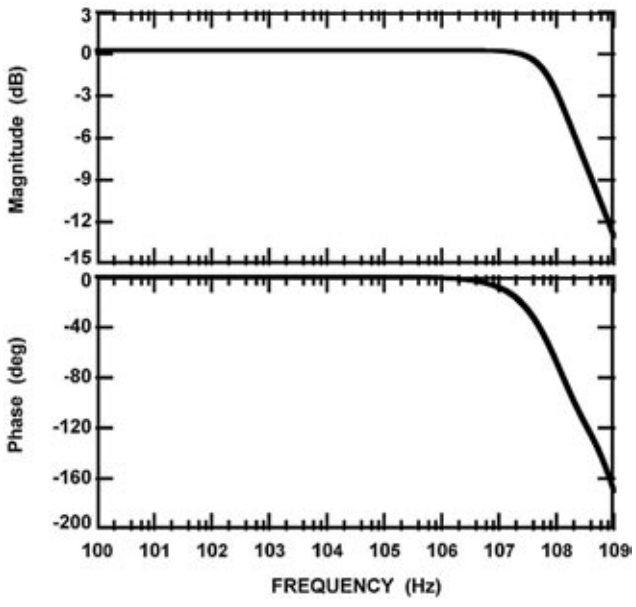


Fig. 5: Frequency characteristics of the short circuit current transfer gain between X and Z (IZ/IX) for the circuit shown in Fig. 2

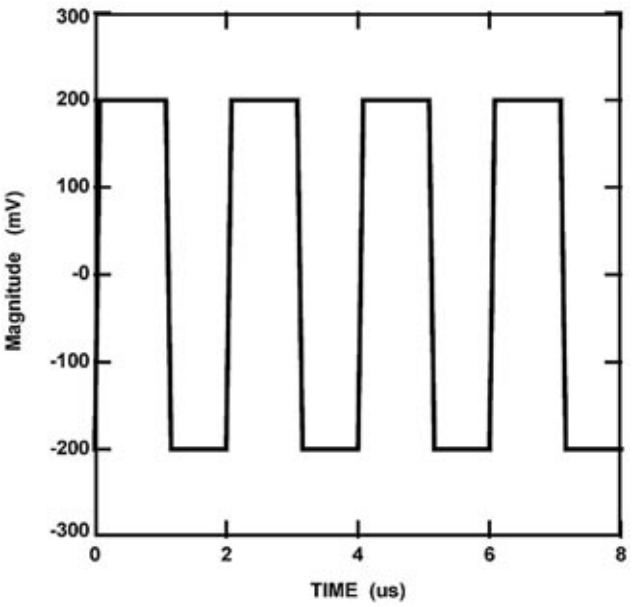


Fig. 6: Input impedance at terminal X for the circuit shown in Fig. 2

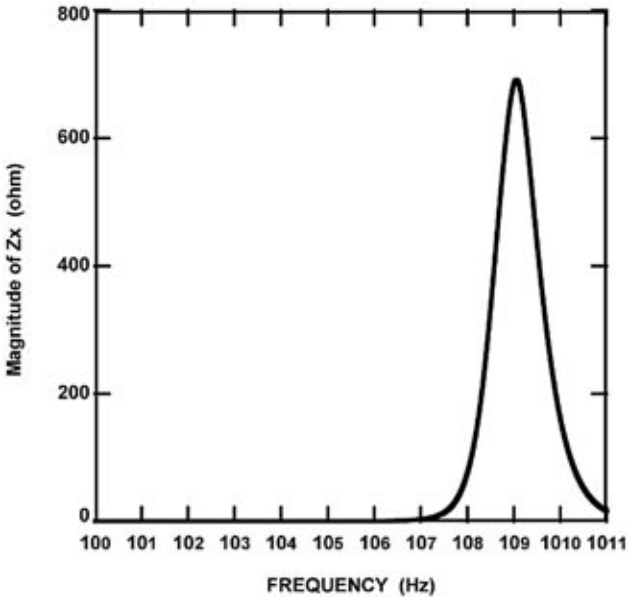


Fig. 7: The transient response of the circuit shown in Fig. 2

that the proposed CCII+ achieves better performance in all parameters paying some loss in the voltage transfer gain and more power dissipation which is yet acceptable in many applications.

Table 3: Parameters of the circuits shown in Fig. 1 and Fig. 2

| Parameter | Unit | Yodprasit CCII+ [7] | The proposed CCII+ |
|---|---|---|---|
| Input voltage range | V | -0.67 to 0.2 | -1 to 0.3 |
| Voltage offset range | mV | -0.001 to – 0.01 | 1 to -0.2 |
| Av (average value) of open circuit voltage transfer gain | V/V | 0.99999 | 0.99996 |
| Maximum deviation from Av | - | 0.003 % | 0.06 % |
| Open loop gain | dB | 98 | 88 |
| 3 db-Bandwidth of open circuit voltage transfer gain | MHz | 12.3 | 536 |
| Input current range | μ A | -50 to 50 | -100 to 100 |
| Current offset range | μ A | 0.92 to 5.01 | 0.16 to 7.5 |
| Ai (average value) of short circuit current transfer gain | A/A | 1.01593 | 0.98211 |
| Maximum deviation from Ai | - | 6 % | 9.9 % |
| 3 db-Bandwidth of short circuit current transfer gain | MHz | 7 | 107 |
| rx | Ω | 0.99 | 0.82 |
| THD for a sinusoid of 100 KHz | - | 0.02 % | 0.005% |
| Power consumption | mW | 0.66 | 0.87 |

## 3. Conclusion

Novel class-A accurate CMOS CCII suitable for high frequency applications is presented in this paper. Simulations results proved the strength of the proposed CCII realization compared to Yodprasit CCII realization reported in the literature [7]. The proposed CCII exhibits wider voltage and current bandwidths and also provides high accuracy. Moreover, the proposed circuit provides lower input impedance.

## References

[1] K. C. Smith, and A. Sedra, “The current conveyor-A new circuit building block,” IEEE Proc., vol. 56, pp. 1368-1369, 1968.

[2] A. Sedra, and K. C. Smith, “A second generation current conveyor and its applications,” IEEE Trans. Circuit Theory, vol.17, pp. 132-134, Feb. 1970.

[3] F. Gohh, G. W. Roberts, and A. Sedra, “The current conveyor: History progress and new results,” IEE Proc.-G, vol. 137, no. 2, pp. 63-77, April 1990.

[4] W. Surakampontorn, V. Riewruja, K. Kumwachara, and K. Dejhan, “Accurate CMOS based current conveyors,” IEEE Trans. Instr. Measurements, vol. 40, pp. 699-702, Aug. 1991.

[5] S. Liu, H. Tsao, and J. Wu, “CCII based continuous time filters with reduced gain bandwidth sensitivity,” IEE Proc.-G, vol. 138, no. 2, pp. 210-216, April 1991.

[6] H. O. Elwan, and A. M. Soliman, ”Low-voltage low-power CMOS current conveyors,” IEEE Trans. Circuits Syst. I, vol. 44, no. 9, pp. 828-835, Sept. 1997.

[7] U. Yodprasit, ”High-precision CMOS current conveyor,” Electron. Lett., vol. 36, no. 7, pp. 609-610, March 2000.

[8] G. Palmisano, and G. Palumbo, ”A simple CMOS CCII+,” Int. J. Circuit Theory and Applications, vol. 23, pp. 599-603, 1995.

[9] B. Wilson, ”Performance analysis of current conveyors,” Electron. Lett., vol. 25, no. 23, pp. 1596-1598, Nov. 1998.

[10] G. Palmisano, G. Palumbo, and S. Pennisi, “Design strategies for class A CMOS CCIIS,” Analog Integrated Circuits and Signal Processing, vol. 19, pp. 75-85, 1999.

Mr. Hassan M. Hassan
Dr. Ahmed M.Soliman
Faculty of Engineering
Cairo University
Cairo
EGYPT
E-mail: asoliman@idsc.net.eg

(Received on February 27, 2006)
(Revised on March 2, 2006)