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A Modified CMOS Realization of the Operational Transresistance Amplifier (OTRA)

By Hassan Mostafa, Ahmed M. Soliman

Abstract – A modified CMOS realization of the operational transresistance amplifier (OTRA) is presented. A fair comparison with Salama and Soliman OTRA [1] shows that the modified OTRA provides better performance in all parameters. The OTRA is suitable for analog VLSI applications since it does not suffer from constant gain bandwidth product. Hence, it can exhibit wide bandwidth at high gain values. Moreover, an OTRA based variable gain amplifier (VGA) is introduced. A detailed analysis taking the effect of the finite transresistance gain in consideration is provided.

Index Terms – CMOS operational transresistance amplifier, analog VLSI applications, variable gain amplifier, wireless communications,

1. Introduction

Recently, great interest has been devoted to the design of the operational transresistance amplifiers (OTRA) [1, 3-5]. This great interest is mainly because the OTRA is not slew limited in the same fashion as voltage op amps [1]. It can provide a high bandwidth independent of the gain. Hence, it does not suffer from constant gain bandwidth product like voltage op amps circuits [4].

The supply voltages are ± 1.5 V. The reference DC current source I_B is taken as 25 µA. The CMOS model for all circuits is identical. The transistor model is 0.5 µm CMOS process provided by MOSIS (AGILENT). The aspect ratios for all equivalent transistors are equal. The symbol of the OTRA is shown in Fig.1.

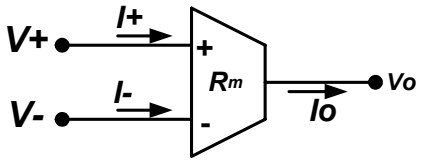

Fig.1: Block diagram of the OTRA

The operational transresistance amplifier (OTRA) is a three terminal analog building block that is defined by the following matrix equation:

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix} \quad (1)$$

Where R_m is the transresistance gain.

Both the input and output terminals are characterized by low impedance. The input terminals are virtually grounded leading to circuits that are insensitive to stray capacitances [2-4]. Ideally the transresistance gain, R_m, approaches infinity, and applying external negative feedback will force the two input currents, I_+ and I_-, to be equal.

In the second section of this chapter one of the OTRA circuit realizations reported in [1] is examined and simulation results are given. In the third section of this chapter a novel low power, large open loop transresistance gain and high gain bandwidth product OTRA is proposed. In the fourth section of this chapter an OTRA based variable gain amplifier (VGA) is proposed.

2. Salama and Soliman OTRA [1]

2.1 Circuit description

The CMOS realization of the OTRA proposed in [1] is shown in Fig.2. It is based on the cascaded connection of the modified differential current conveyor (MDCC) [2] and a common source

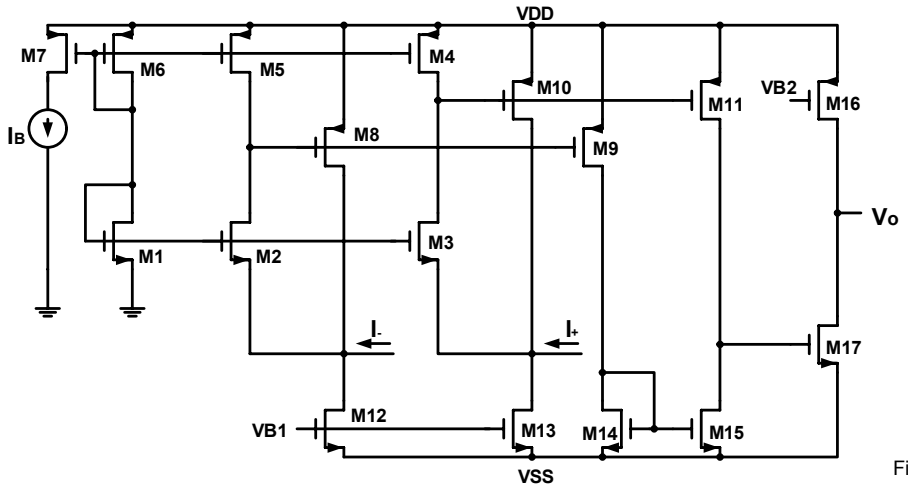

Fig. 2: OTRA realization proposed in [1]

amplifier [1]. Assuming that each of the groups of the transistors (M1-M3), (M4-M7), (M8 and M9), (M10 and M11), (M12 and M13) as well as (M14 and M15) are matched. And assuming that all the transistors operate in the saturation region, the circuit operation can be explained as follows. The current mirrors formed by (M4-M7) forces equal currents (I_B) in the transistors M1, M2 and M3.

This operation drives the gate to source voltages of M1, M2 and M3 to be equal and, consequently, forces the two input terminals to be virtually grounded. The current mirrors formed by the transistor pairs (M4 and M5), (M8 and M9), (M10 and M11) and (M14 and M15) provide the current differencing operation, whereas the common source amplifier (M17) achieves the high gain stage.

2.2 Simulation results

Transistors aspect ratios are reported in Table 1. The biasing current I_B = 25µA. The biasing voltages V_{B1} = -0.5 V and V_{B2} = 0.1 V. Simulation results are tabulated in Table 3 and shown in Figs. 3, 4 and 5.

These results can be described as follows. The input differential current range is from -50µA to 50µA (Fig.3). The offset current equals 1.25µA. The input resistance equals 15.5 Ω (Fig.4). The DC open loop transresistance gain equals 80 dBΩ (= 10 KΩ) (Fig.5). The gain bandwidth product equals 372 GHz.Ω (Fig.5). The power dissipation of the circuit equals 0.9 mW.

Table 1: Transistors aspect ratios of the circuit shown in Fig.2

Transistor	W(µm)/L(µm)
M1- M3	100/2.5
M4 - M7	50/2.5
M8 - M11	50/2.5
M12,M13	30/2.5
M14,M15	50/2.5
M16	10/2.5
M17	50/0.5

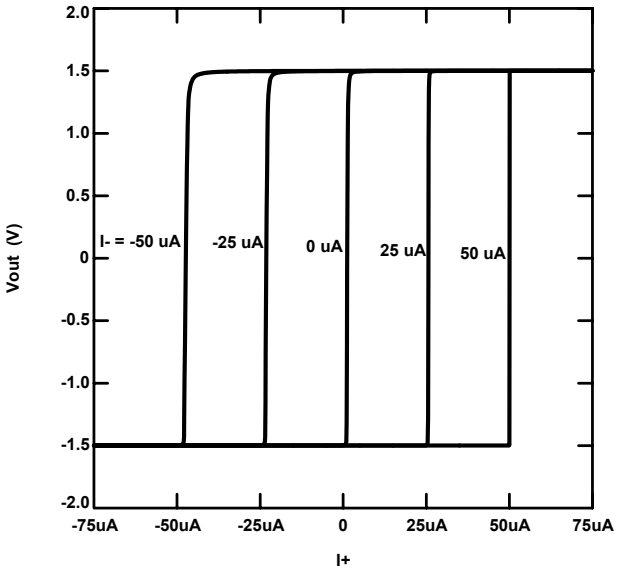

Fig. 3: The output voltage of the circuit shown in Fig.2

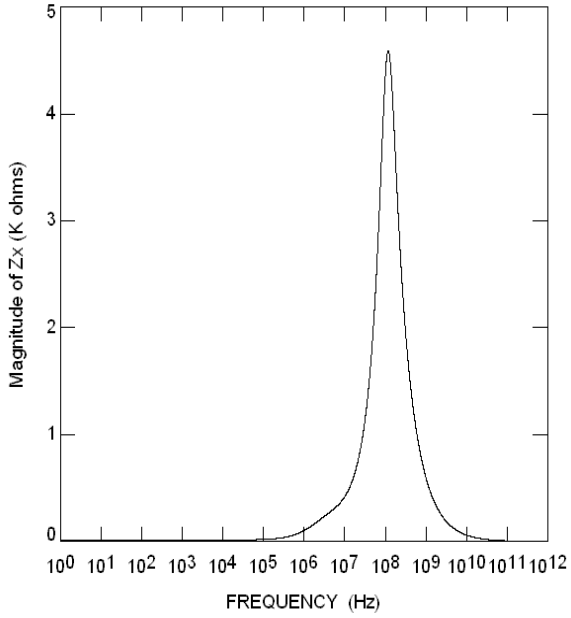

Fig. 4: Input impedance at terminal X for the circuit shown in Fig.2

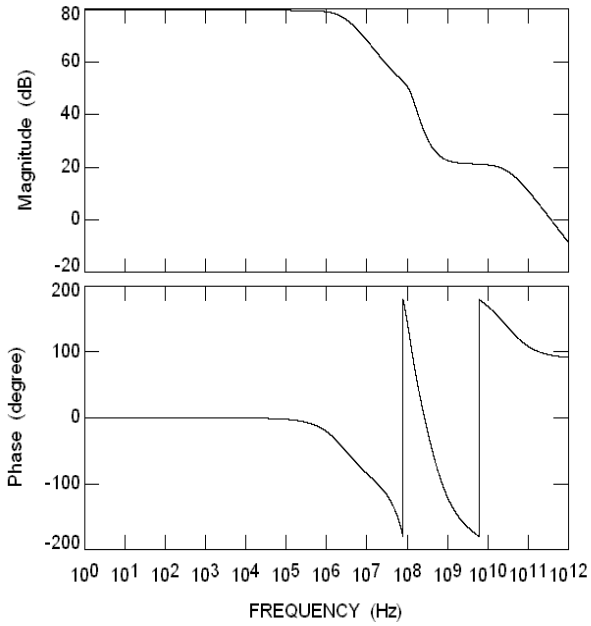

Fig. 5: Frequency characteristics of the open loop transresistance gain for the circuit shown in Fig.2

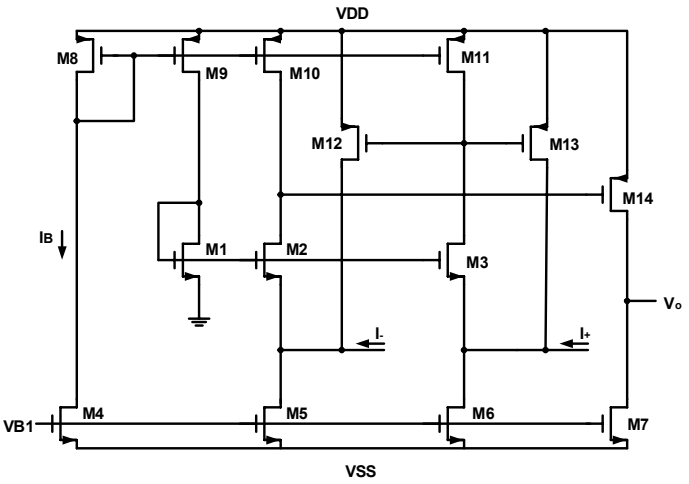

Fig. 6: The proposed modified OTRA

3. The proposed modified OTRA

3.1 Circuit description

The CMOS realization of the proposed low power wide band OTRA is shown in Fig.2. It is based on the cascaded connection of the modified differential current conveyor (MDCC) [2] and a common source amplifier [1]. Assuming that each of the groups of the transistors (M1-M3), (M5 and M6), (M8-M11) and (M12 and M13) are matched. And assuming that all the transistors operate in the saturation region, the circuit operation can be explained as follows.

The current mirrors formed by (M8-M11) forces equal currents (I_B) in the transistors M1, M2 and M3. This operation drives the gate to source voltages of M1, M2 and M3 to be equal and, consequently, forces the two input terminals to be virtually grounded.

The current mirrors formed by the transistor pairs (M10 and M11) and (M12 and M13) provide the current differencing operation, whereas the common source amplifier (M14) achieves the high gain stage. It is clear that the modified OTRA has smaller number of current mirrors than Salama and Soliman OTRA introduced in [1] which reduces the transistor mirror mismatch effect and also increases the frequency capabilities. Moreover, the proposed OTRA uses smaller number of transistors which reduces the power dissipation.

3.2 Simulation results

Transistors aspect ratios are reported in Table 2. The biasing current I_B = 25μA. The biasing voltage V_{B1} = -0.5 V. Simulation results are tabulated in Table 3 and shown in Figs. 7, 8 and 9. These results can be described as follows. The input differential current range is from -50μA to 50μA (Fig.7). The offset current equals 0.1μA.

The input resistance equals 4.2 Ω (Fig.8). The DC open loop transresistance gain equals 162 dBΩ (= 126 MΩ) (Fig.9). The gain bandwidth product equals 617 GHz.Ω (Fig.9). The power dissipation of the circuit equals 0.6 mW.

The advantage of the proposed modified OTRA circuit shown in Fig. 6 is proved by the following comparison. From Table 3, it is clear that the proposed OTRA provides less offset current than Salama and Soliman OTRA. And also the proposed OTRA exhibits more DC open loop transresistance gain and more gain bandwidth product than Salama and Soliman OTRA.

The open loop transresistance gain increased from 80 dBΩ to 162 dBΩ. The gain bandwidth product increased from 372 GHz.Ω to 617 GHz.Ω. Moreover, the proposed OTRA has smaller input resistance and lower power dissipation than Salama and Soliman OTRA. Keeping the fair comparison criterion, the proposed OTRA has a sharp peak at its open loop transresistance gain which can be removed using compensation techniques.

Table 2: Transistors aspect ratios of the circuit shown in Fig.6

Transistor	W(μm)/L(μm)
M1- M3	100/2.5
M4	10/2.5
M5, M6	30/2.5
M7	10/2.5
M8- M11	50/2.5
M12, M13	100/2.5
M14	50/0.5

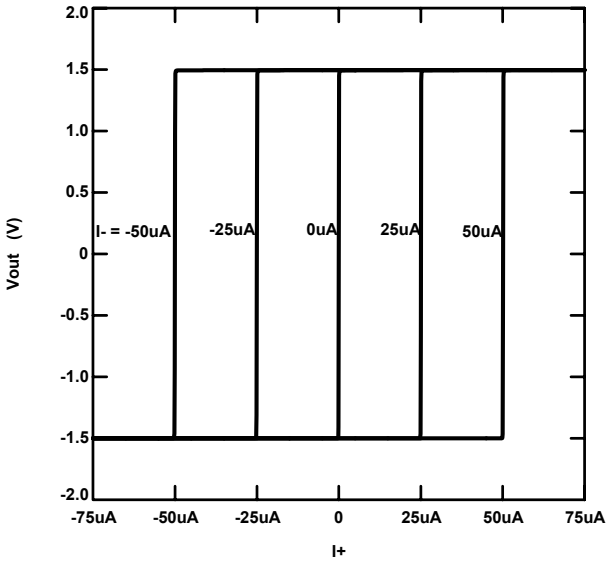

Fig. 7: The output voltage of the circuit shown in Fig.6

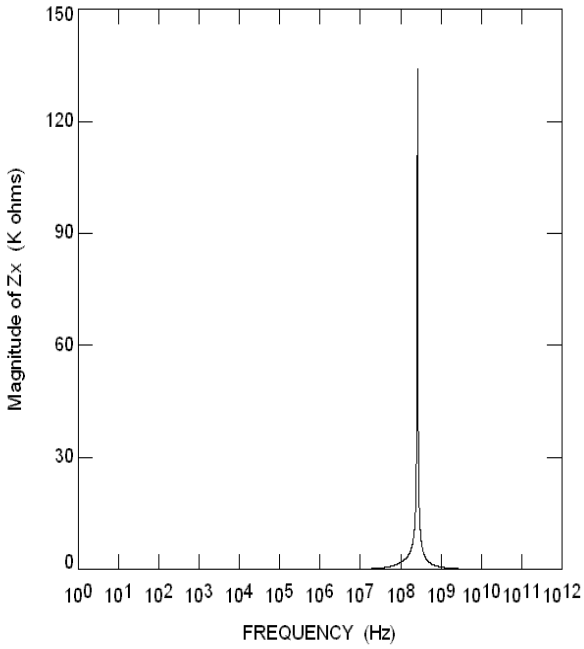

Fig. 8: Input impedance at terminal X for the circuit shown in Fig.6

Table 3: Parameters of the circuits shown in Fig.2 and Fig.6

Parameter	Salama and Soliman OTRA [1]	The proposed OTRA	Unit
Input current dynamic range	-50 to 50	-50 to 50	μA
Offset current	1.25	0.1	μA
DC open loop transresistance gain	80	162	dBΩ
Gain bandwidth product	372	617	GHz. Ω
Input resistance	15.5	4.2	Ω
Power dissipation	0.9	0.6	mW

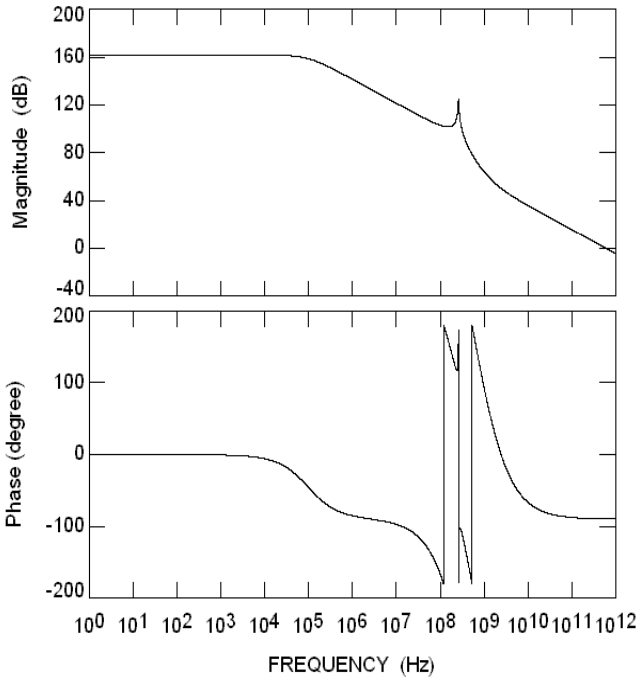

Fig. 9: Frequency characteristics of the open loop transresistance gain for the circuit shown in Fig.6

4. OTRA-based digitally controlled voltage-mode VGA

4.1 Introduction

Variable gain amplifiers (VGAs) are used in many applications in order to maximize the dynamic range of the overall system. Hearing aids [6], disk drives [7, 8], and wireless communications are examples of such systems. In a wireless communication system, the portability of the terminal implies that the received signal has a very wide dynamic range. This necessitates the use of an automatic gain control (AGC) circuit. Its function is to automatically adjust the gain of the receive path so that the signal processed by the baseband section circuitry appears to be at a constant level regardless of the actual signal strength received at the antenna.

The AGC contains mainly two blocks, a variable gain amplifier (VGA) and a signal strength detector which feeds back the control signal used to adjust the gain of the VGA. In modern wireless systems, all of the baseband signal processing is implemented digitally by a digital signal processor (DSP). A VGA controlled by an analog signal, will need additional digital-to-analog converter (DAC) in the AGC loop, increasing both complexity and delay. Hence, an essential requirement of the VGA is to be digitally controlled.

The gain of the VGA should increase linearly on the decibel scale in order to achieve a wide gain control. Although traditional VGA topologies based on high open loop gain op-amps or operational transconductance amplifiers (OTAs) provide good results, they suffer from slew rate limitations and finite gain bandwidth product.

Third generation wireless communication systems utilize wide band code division multiple access (WCDMA) techniques [4]. Thus, the transmitted signal is to be spread over a wider range of bandwidth. It is thus necessary to investigate new CMOS amplifier based VGA structures that is not slew limited and also can provide large bandwidth independent of the gain. This can be done by using the OTRA-based voltage-mode digitally controlled VGA.

4.2 Circuit description

The novel voltage-mode digitally controlled VGA configuration is shown in Fig.10. The VGA circuit is operating in a coarse and fine arrangement. It consists of two stages. The first stage represents a coarse gain control stage. The second stage represents a fine gain control stage. It can be showed that the voltage gain of each stage is given by:

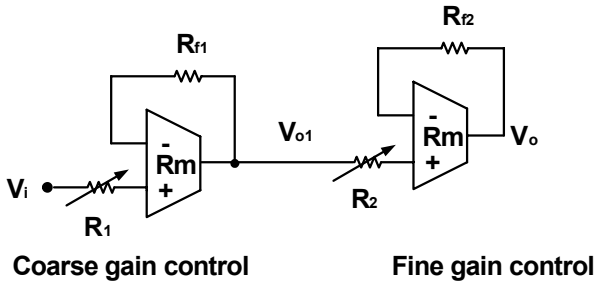

Fig. 10: The voltage-mode digitally controlled VGA using the OTRA [4]

$$\text{Voltage gain of the second stage } = \frac{V_o}{V_{o_1}} = \frac{R_{f2}}{R_2}.\frac{1}{1+sR_{f_2}C_p} \qquad (2)$$

$$\text{Voltage gain of the second stage } = \frac{V_o}{V_{o_1}} = \frac{R_{f2}}{R_2}. \qquad (3)$$

Taking the effect of the finite transresistance gain, R_m, and using the single pole model. The transresistance gain is given by:

$$R_m(s) = \frac{R_o}{1+\frac{s}{\omega_o}} \qquad (4)$$

Where R_o is the DC open loop transresistance gain and ω_o is the transresistance cut off frequency.

For high frequency applications, the transresistance gain, $R_m(s)$, may be expressed as

$$R_m(s) = \frac{1}{sC_p} \qquad (5)$$

Where

$$C_p = \frac{1}{R_o\omega_o} \qquad (6)$$

Hence, the voltage gain of each stage will be given by:

$$\text{Voltage gain of the first stage } = \frac{V_{o_1}}{V_i} = \frac{R_{f_1}}{R_1}.\frac{1}{1+sR_{f_1}C_p} \qquad (7)$$

$$\text{Voltage gain of the second stage } = \frac{V_o}{V_{o_1}} = \frac{R_{f2}}{R_2}.\frac{1}{1+sR_{f_2}C_p} \qquad (8)$$

It is clear from equation (7) that the gain of the first stage can be varied independently of the bandwidth by changing the resistance R_1. Similarly, from equation (8) the gain of the second stage amplifier can be varied independently of the bandwidth by

changing the resistance R_2. The first stage operates in a 6-dB step (coarse gain control) while the second VGA stage provides the precise 1-dB gain stepping (fine gain control).

The digital control structure of the resistors R_1 and R_2 is shown in Fig.11 and Fig.12 respectively. The resistance R_1 is given by [9]:

$$R_1 = R_{11} + \overline{d_{10}}\left\{R_{12} + \overline{d_{11}}\left\langle R_{13} + \overline{d_{12}}\left(R_{14} + \overline{d_{13}}[R_{15} + \overline{d_{14}}(R_{16} + \overline{d_{15}}R_{17})]\right)\right\rangle\right\} \tag{9}$$

Where R_{1i} (i = 1, 2, 3…, 7) are polysilicon resistors and d_{1n} (n = 0, 1, 2…, 5) are the digital inputs that control the value of R_1. Table 4 shows the values of these resistors in terms of the feedback resistor R_{f_1}. The digital inputs and the corresponding gains are shown in Table 5. Similarly, the resistance R_2 is given by [9]:

$$R_2 = R_{21} + \overline{d_{20}}\left\{R_{22} + \overline{d_{21}}\left(R_{23} + \overline{d_{22}}[R_{24} + \overline{d_{23}}(R_{25} + \overline{d_{24}}R_{26})]\right)\right\}) \tag{10}$$

Where R_{2i} (i = 1, 2, 3…, 6) are polysilicon resistors and d_{2n} (n = 0, 1, 2…, 4) are the digital inputs that control the value of R_2. Table 6 shows the values of these resistors in terms of the feedback resistor R_{f_2}. The digital inputs and the corresponding gains are shown in Table 7.

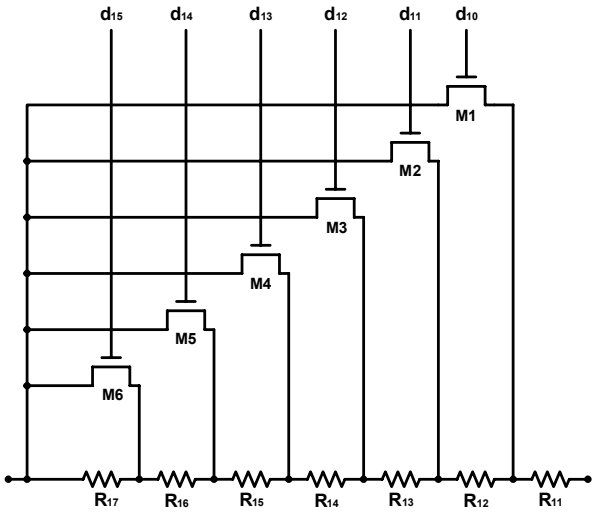

Fig. 11: The digitally controlled resistance R1 [9]

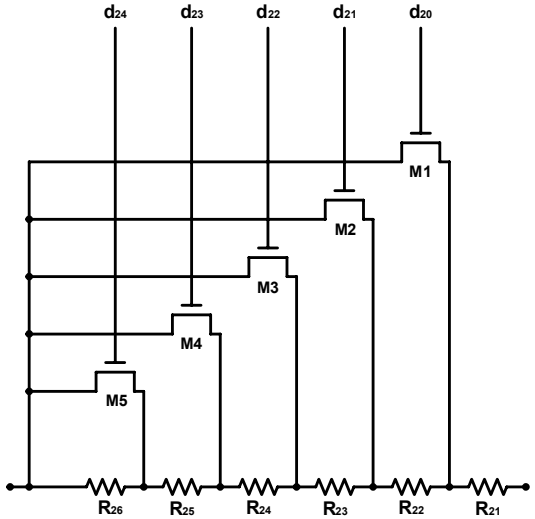

Fig. 12: The digitally controlled resistance R2 [9]

Table 4: The values of the resistors used to control the resistance R_1 of the first stage

Resistor	Value
R_{11}	$R_{f1}/64$
R_{12}	$R_{f1}/64$
R_{13}	$R_{f1}/32$
R_{14}	$R_{f1}/16$
R_{15}	$R_{f1}/8$
R_{16}	$R_{f1}/4$
R_{17}	$R_{f1}/2$

Table 5: The digital inputs and the corresponding gain of the first stage

Gain (dB)	d_{10}	d_{11}	d_{12}	d_{13}	d_{14}	d_{15}
0	0	0	0	0	0	0
6	0	0	0	0	0	1
12	0	0	0	0	1	0
18	0	0	0	1	0	0
24	0	0	1	0	0	0
30	0	1	0	0	0	0
36	1	0	0	0	0	0

Table 6: The values of the resistors used to control the resistance R2 of the second stage

Resistor	Value
R_{21}	0.563 R_{f2}
R_{22}	0.069 R_{f2}
R_{23}	0.077 R_{f2}
R_{24}	0.087 R_{f2}
R_{25}	0.097 R_{f2}
R_{26}	0.109 R_{f2}

Table 7: The digital inputs and the corresponding gain of the second stage

Gain (dB)	d_{20}	d_{21}	d_{22}	d_{23}	d_{24}
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	1	0	0
4	0	1	0	0	0
5	1	0	0	0	0

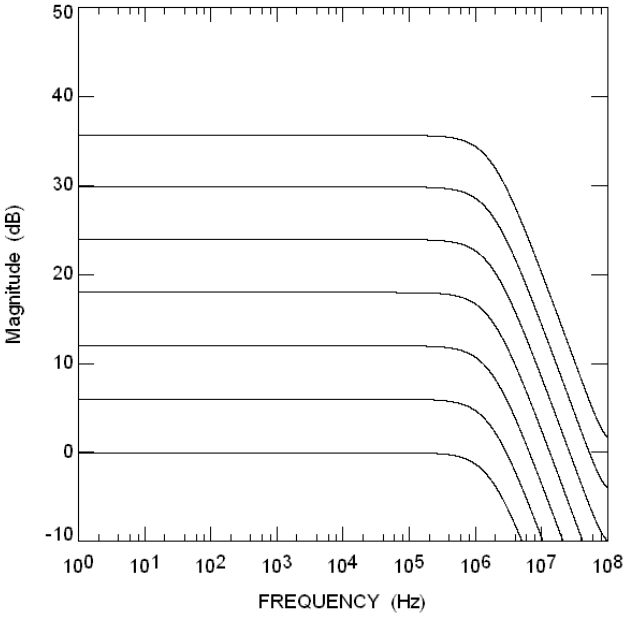

Fig.13: Frequency characteristics of the first stage of the voltage-mode digitally controlled VGA shown in Fig.10 using the OTRA circuit shown in Fig.6 with different gains from 0 dB to 36 dB with 6 dB gain step

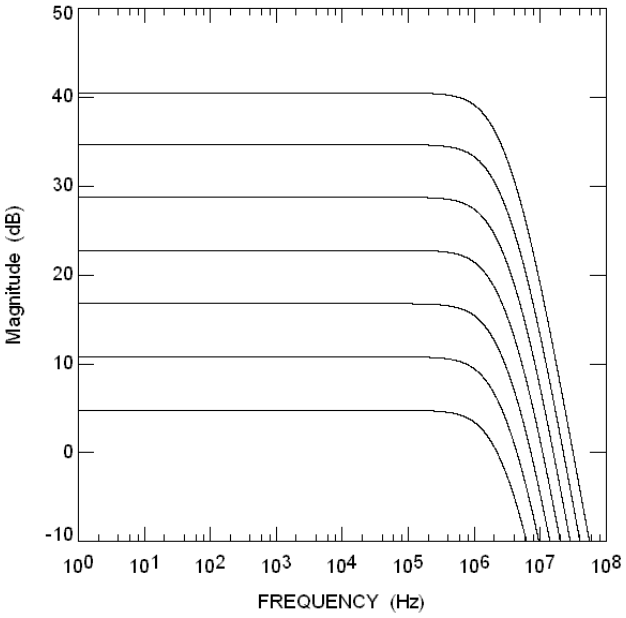

Fig.15: Frequency characteristics of the overall voltage-mode digitally controlled VGA shown in Fig.12 using the OTRA circuit shown in Fig.6 with different gains from 5 dB to 41 dB with 6 dB gain step

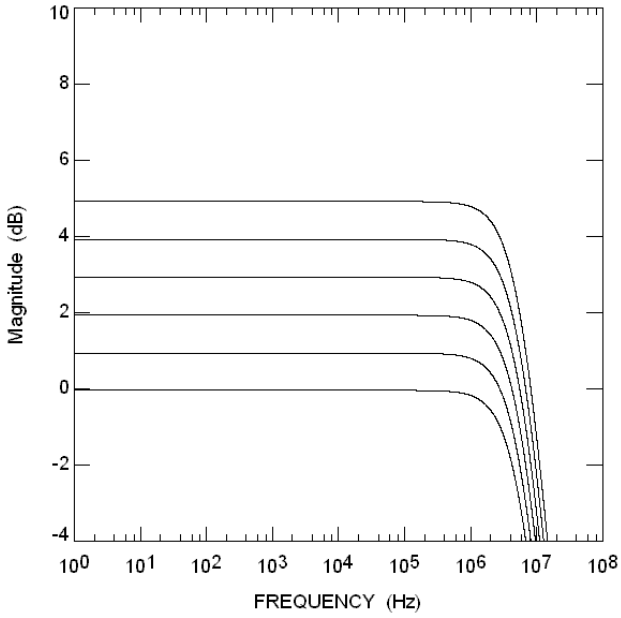

Fig.14: Frequency characteristics of the second stage of the voltage-mode digitally controlled VGA shown in Fig.10 using the OTRA circuit shown in Fig.6 with different gains from 0 dB to 5 dB with 1 dB gain step

4.3 Simulation results

The voltage-mode digitally controlled VGA is simulated using R_{f1} = 64 kΩ and R_{f2} = 20 kΩ. The circuit is compensated by using capacitors C_1 = 1.5 pF (connected between the output terminal of the first stage (V_{o1}) and its input terminal (V_i)) and C_2 = 1.5 pF (connected between the output terminal of the second stage (V_o) and its input terminal (V_{o1})).

The switching transistors used in the digitally controlled resistors R_1 and R_2 have the same aspect ratio (W = 100 μm and L = 0.5 μm). Fig.13 shows the different gains of the first stage (coarse gain control) ranging from 0 dB to 36 dB with a 6 dB gain step.

Fig.14 shows the different gains of the second stage (fine gain control) ranging from 0 dB to 5 dB with a 1 dB gain step. Fig.15 shows the different gains of the overall VGA circuit ranging from 5 dB to 41 dB with a 6 dB gain step. It is clear that the bandwidth is about 2 MHz for the maximum gain of 41 dB. The average gain error is about 0.241 dB. The power dissipation of the circuit is about 1.165 mW.

5. Conclusion

This paper presents a modified CMOS realization of the operational transresistance amplifier. The OTRA is not slew limited in the same fashion as voltage op amps. Moreover, it can provide a high bandwidth independent of the gain. Hence, it does not suffer from constant gain bandwidth product like voltage op amps circuits. Simulation results and a fair comparison between the proposed modified OTRA and Salama and Soliman OTRA proved the strength of the proposed realization. Digitally controlled voltage-mode variable gain amplifier (VGA) based on the proposed realization is also introduced.

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Hassan Mostafa

Dr. Ahmed M. Soliman
Electronics and Communications
Engineering Department
Faculty of Engineering
Cairo University
Giza
EGYPT
Fax: +20-2-5723486
E-mail: amsoliman@ieee.org

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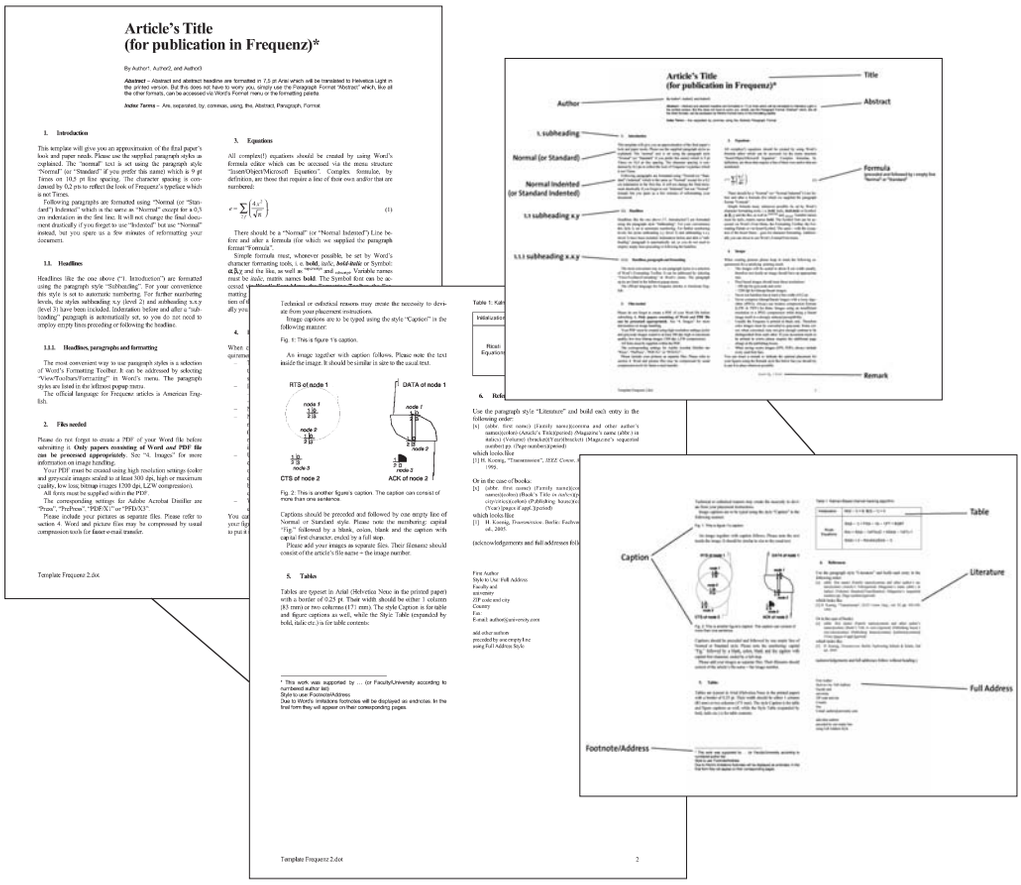

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