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A high-efficiency piezoelectric-based integrated power supply for low-power platforms

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ABSTRACT

In this paper, a high-efficiency piezoelectric-based integrated power supply (PEPS) is proposed. The proposed PEPS supplies low-power platforms (i.e., Passive infrared sensor) with 51.4% power conversion efficiency (PCE). The piezoelectric transducer designing and modeling are developed using COMSOL. Furthermore, a Verilog-A model is presented to be integrated with the proposed power management unit where the output DC supply is 3.3 V. Finally, a prototype of the proposed PEPS is implemented using UMC 0.13 μm CMOS technology, the design occupies approximately 0.092 mm^2.

1. Introduction

Energy harvesting is the process of collecting energy from different sources in the environment such as solar power, heat, mechanical power, and RF. Harvesting is highlighted to be an alternative solution for conventional batteries which have some durability limitations and not Eco-friendly [1]. Some applications, such as implanted devices in the human body and satellite systems, work on energy harvesting since conventional batteries occupy a large area and can not be replaced regularly [2]. The need for a long-life battery has become a demand in all potable and portable applications. One of the best sources of harvesting renewable energy is a piezoelectric harvester. Piezoelectricity is the property of certain materials to induce charges on its surfaces when stress or vibration is applied to the material. These charges generate a voltage difference which is used to power electronic circuits [3]. Consequently, a lot of research is conducted in this field.

The paper starts with the literature review as in section two, it discusses the previously published designs and what is new in the proposed system. In section three, the system architecture is introduced which elaborates more the different sub blocks. Then, the post layout simulation results of the proposed design are discussed in section four. Reaching section five, the results of the whole system such as the power efficiency and the power consumption are clarified. Then, these results are discussed and concluded in the results and discussion section. Finally, the paper ends with a conclusion that summarizes the work done.

2. Literature review

Various research work proposed several techniques to harvest piezoelectric energy and power different applications. However, a fully integrated system starting from the piezoelectric transducer with power converters and maximum power point tracking (MPPT) is not presented at the complete system level in the literature, up to the authors knowledge.

In [4], the author presented a full chip including the harvester with an active-diode based rectifier with a trickle charger only. However, the paper did not present either DC-DC converter nor MPPT. Some other papers like [5] focused on improving the AC-DC converter circuit design

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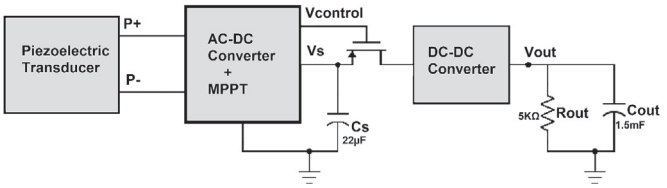

Fig. 1. Proposed piezoelectric-based power supply block diagram.

and represented the piezoelectric transducer as a simple RLC circuit. On the other hand, in Refs. [6], a simple AC-DC converter is used while adding a charge storage unit and voltage monitoring circuit. After realizing the importance of DC-DC converter, papers like [7,8] implemented voltage regulator after the AC-DC converter but no detailed explanation is given for it. Whereas in Ref. [9], the authors implemented a DC-DC converter using both DC-DC buck converter and DC-DC boost converter which consume large implementation area. Moreover, in Ref. [10], the off-the-shelf components used occupied more area. Finally, in Ref. [11], an AC-DC converter with an integrated MPPT circuit is introduced while a simple model for the piezoelectric transducer is utilized and a commercial transducer is used for validation. As a conclusion, a compact design that includes the whole system starting with transducer designing and modeling followed by power conversion and tracking is required.

Fig. 1 portrays the proposed system and the main work contributions are summarized as follows:

- This work focuses more on the system level by designing the Piezoelectric (PZT) transducer itself on the COMSOL platform and optimizing its design parameters to match that of the AC-DC converter maximum efficiency.
- This work presents a VerilogA model for the PZT transducer to simulate it using the same CAD tool (Cadence Spectre). This helps in the co-design at the device and circuit levels of abstraction.
- This work implements a hybrid design for a power management unit that includes an optimized AC-to-DC converter with an integrated MPPT and a DC-to-DC converter for voltage regulation. Some of the blocks are inherited from Ref. [1] with proper citation given that the main focus of this work is on the system level not only the circuit level from the device/circuit co-design perspective.
- This work redesigns all the inherited blocks to achieve low area and low power consumption. This includes improving the comparator design to drive high gate capacitance and improving the power conversion efficiency (PCE) as the load resistance increases. Moreover, all the results in this work are provided at the post-layout simulation level.

3. System architecture

3.1. Piezoelectric transducer

This paper presents a model of vibrational energy harvester designed with a bimorph piezoelectric cantilever that has an end mass. It converts the vibration energy applied to the structure into electrical energy. The model is used to find the resonance frequency of the harvested energy, output voltage, harvested power and optimal value of excitation frequency for maximum power transfer. Piezoelectric transducer with resonating harvester has the ability to resonate at low frequency and high stress [12]. The model is designed and simulated with the finite element analysis in COMSOL-5.2 Multi-physics. The piezoelectric transducer model consists of a cantilever deposited by two piezoelectric material layers with a mass at the end of the cantilever to lower the resonant frequency. The cantilever is a steel substrate sandwiched by two layers of the piezoelectric material of Lead Zirconate Titanate (PZT-5H). (PZT-5H) is the commonly used material among Piezo ceramic which

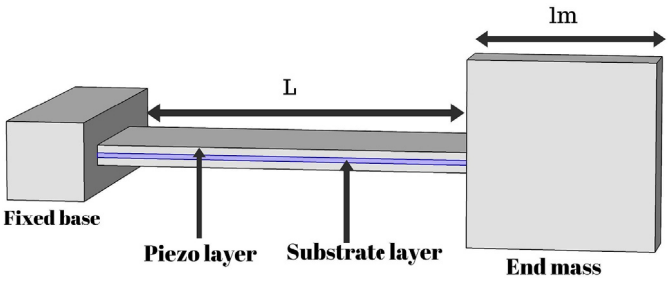

Fig. 2. Schematic diagram of the piezoelectric transducer model.

Table 1
The piezoelectric design parameters.

Parameter	Description	Value
L	Length of the Cantilever (mm)	25
b	width of the Cantilever (mm)	8
h_p	Thickness of Piezoelectric layer (mm)	0.15
h_s	Thickness of Substrate layer (mm)	0.1
l_m	Length of end mass (mm)	2.5
l_w	Width of end mass (mm)	2.5
Y_P	Young's modulus of Piezoelectric material (GPa)	105
Y_s	Young's modulus of Substrate material (GPa)	105
ρ_s	Mass density of Substrate material and end mass (kg/m^3)	7500
ρ_p	Mass density of Piezoelectric material (kg/m^3)	9000
R_{load}	Load resistance (Ω)	11k

developed firstly around 1952 at the Tokyo Institute of Technology. PZT is a very brittle material and hence prone to crack if it is exposed to high stress. Moreover, it is physically strong, flexible and inexpensive to manufacture. The top and bottom surfaces of the bimorph form the electrodes that are wired to the load. Fig. 2 shows a schematic of the energy harvester transducer model [13].

Finite element analysis in COMSOL Multiphysics is used to model the piezoelectric transducer. The piezoelectric layers are connected to a load resistance which is equivalent to the input impedance of the second block of the system (the AC-DC converter). An acceleration of 1 g is applied at the end mass. The model is simulated to obtain the output voltage and the harvested power as a function of the excitation frequency. The material properties and geometric properties of the model are given in Table 1.

The harvested power of a piezoelectric film under vibration depends on its geometry, piezoelectric material properties, the resonance frequency of the material and the output load. For maximum power density extraction, the material must be vibrated at its resonance frequency. It is clear that the output electrical power density decreases when the resonant frequency deviates from the vibration frequency.

1) The Modeling of the piezoelectric transducer. In order to identify the interaction between the transducer and other system components, it is modeled with lumped elements. The transducer model is represented by discrete circuit elements. Modeling of the lumped mechanical domain is represented as circuit elements. For example, the capacitor represents the potential energy in the system, resistor models the dissipation of power and the inductor represents the stored kinetic energy in the system. The voltage source is the effort done by the system [14]. Fig. 3 shows the circuit model which describes the electromechanical coupling of the piezoelectric transducer at resonance and the elements are defined as:

$$(V_m = \frac{ma}{r^2}, L_m = \frac{m}{r^2}, C_m = \frac{r^2}{k}, R_m = \frac{d}{r^2})$$

Where (r) is the electromechanical coupling factor.
(m) is the effective mass of the structure.
(a) is the acceleration acting on the harvester end mass.
(d) is the damping coefficient.
(k) is the stiffness of the system.
(C_p) is the internal capacitance of the piezoelectric material.

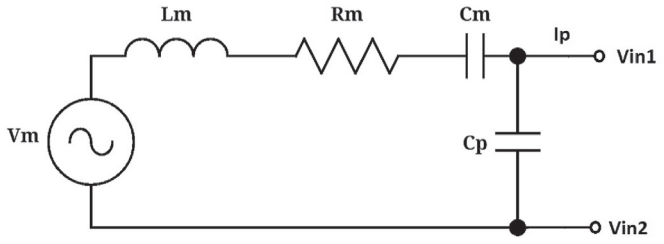

Fig. 3. Equivalent circuit of the piezoelectric transducer at resonance [13].

3.2. AC-DC converter

For the AC power transducers, the output power is generated in the form of AC current with a certain frequency [15]. On the other hand, most systems are powered by a DC current, this is why AC-DC converter is needed [16].

The idea of AC-DC converter is to control the direction of the current to make sure that the polarity of the terminals connected to the load does not change with the changing AC input signal [17,18]. The AC-DC converters are originally designed based on the full-wave rectifiers using diodes [19–25].

The adopted rectifier architecture of the AC-DC converter, shown in Fig. 4, is called hybrid rectifier topology with self-starting up capability [11]. The design consists of two parts, the first part is a passive rectifier used for the self-start up operation. It consists of two NMOS diode-connected transistors, that kick in if vibration starts to provide AC-DC rectification. Initially, the active rectifier is off, as Vs is zero and incapable of activating it.

On The second part is the active rectifier that consists of two active diodes each one has NMOS transistor and a comparator. It operates when the harvester powers up the capacitor Cs and these active diodes eventually eliminate the voltage drop ($\Delta V = V_s - V_{in} = V_{sd} \cong 300$ mV) caused by NMOS diode-connected transistor, the output power and voltage increase. The active diodes have the ability to be turned on and off completely without the use of reverse current control especially when used in vibration harvesting systems where the frequency of vibration is low. Thus, it is not recommended to implement the reverse current control technique in the targeted low power systems that adds more complexity and power loss in the system.

1) Theory of operation: When $V_{in1} > V_{in2}$, MP1 is on when V_{in1} exceeds V_{thp}. While V_{in2} is lower than ground making the comparator output CMP2 "high", turning right active diode on which directs current from the V_{in1} to the storage capacitor Cs through MP1 ($V_s = V_{in1} - V_{sd}$).

In contrast, when $V_{in1} < V_{in2}$, MP2 is on when V_{in2} exceeds V_{thp}. While V_{in1} is lower than ground making the comparator output CMP1 "high", activating left active diode which directs current from the V_{in2} to the storage capacitor Cs through MP2 ($V_s = V_{in1} - V_{in2}$), as comparators make super-diode with zero-dropout acting as switch.

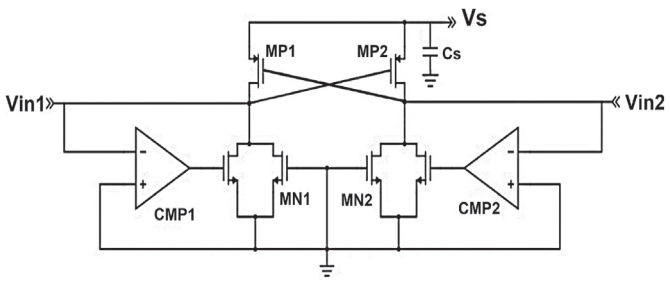

Fig. 4. Hybrid rectifier topology with self-starting up capability [9].

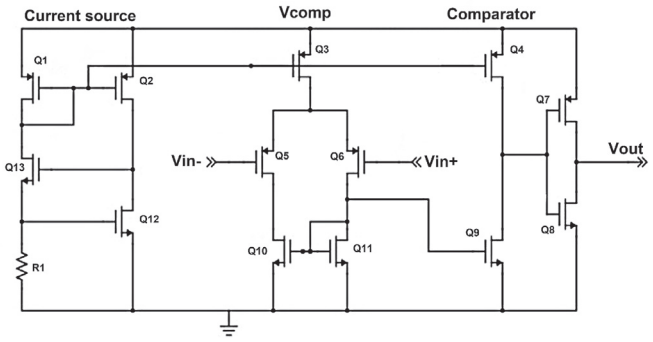

Fig. 5. Voltage independent current source and comparator in sub-threshold operation.

The optimal output voltage of the transducer and the maximum harvested power are given by Ref. [9]:

$$P(t) = \frac{2I_p V_s}{\pi} - 4V_s^2 f C_p - I_{CMP} V_s \tag{1}$$

$$V_{s,optimal} = \frac{I_p}{4\pi f C_p} \tag{2}$$

where

- f is the environmental vibration frequency.
- I_p is the amplitude of current from the transducer.
- I_{CMP} is the current drawn from the comparator.

2) Ultra-low power Comparator. The Ultra-low power comparator implementation is portrayed in Fig. 5 and is designed to work in the sub-threshold region. The current source is designed to drive a small current from the source in the range of nano-amperes. Whereas, the use of the inverter is to enhance the driving capabilities of the comparator to drive large gate capacitance. The comparator is powered using $V_{comp} = 1$ V, from the capacitor divider discussed later, for more power saving.

3.3. Maximum power point tracking (MPPT)

MPPT is a technique or an algorithm that is mostly used in solar cells or systems to get the highest power from the cell despite any changes that may affect the cell-like atmospheric conditions. MPPT technique works on keeping the current and voltage at the optimized level to get the highest power from the cell [26]. MPPT is not a technique that uses a mechanical system to get optimum power from the cell but it is a fully electrical technique that depends on the IV characteristics of the load [27].

There are different algorithms for MPPT such as Artificial Neural Network Control, Fractional Short Circuit Current, Incremental Conductance, Perturb and Observe, Fractional Open Circuit Voltage, three Point Weight Comparison, Closed Loop MPP and Fuzzy Control [28].

In a vibration tracking unit for piezoelectric transducer, the utilization of the fractional open circuit MPPT method has low power overhead in the order of microwatts and is efficient for low power applications [11].

The time-multiplexing mechanism, illustrated in Fig. 6, is implemented similar to that in Refs. [11]. MPPT adaptively senses the vibration status and directly generates an optimal output reference voltage V_{REF} for the AC-DC converter for maximum power harvesting. Along with a control block in which a pulse generator is used to generate the tracking pulse to control the time-multiplexing operation. In addition, a control unit that compares the output voltage of the energy harvester with the MPP (maximum power point) reference voltage V_{REF} to produce the control signals. V_{REF} has been estimated as in Ref. [11] using

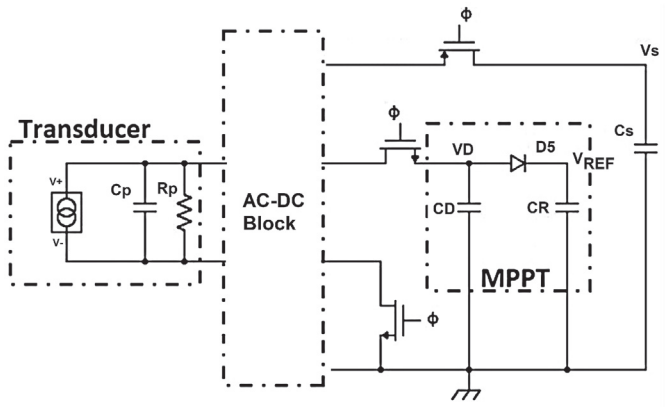

Fig. 6. Implemented design of the energy harvester and the MPPT unit along with the transducer model showing the time-multiplexing mechanism (ϕ is the tracking signal).

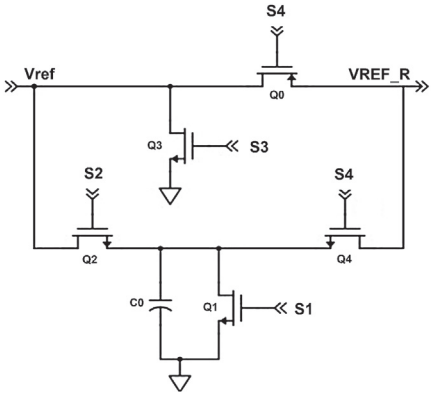

Fig. 7. Refreshing unit circuit.

the proposed mathematical model of the transducer as follows:

$$C\,\frac{dV_D(t)}{dt} + \frac{V_D(t)}{R_p} = I_P * \sin(2\pi ft) \tag{3}$$

$$V_D(t) = \frac{I_P}{2\pi fC} * \sin(2\pi ft - \frac{\pi}{2}) + \frac{I_p}{2\pi fC} * \exp(\frac{-t}{R_pC}) + V_D(0) * \exp(\frac{-t}{R_pC}) \tag{4}$$

Where R_p represents the shunt resistance across C_p that the piezoelectric current I_p experiences. Since R_p is very large, $\exp(\frac{-t}{R_pC}) \Rightarrow 1$ and $V_D(0) = 0$.

Correspondingly, the peak value of V_D occurs at $t = \frac{T}{2}$ which is approximated as in Ref. [9] by:

$$V_{D,peak} = V_D(t = \frac{T}{2}) = \frac{I_P}{\pi fC} = V_{REF} = \frac{1}{4}V_{s,optimal} \tag{5}$$

Where

- $C = C_D + C_p$

C_D is designed to equal at least 15 times C_p, and is designed carefully to have $V_{REF} = V_{D,peak}$ [11].

The time needed for the piezoelectric transducer to reverse the current direction is almost one vibrational cycle from the start of the tracking process and another half-cycle to reach a positive peak value on C_D. MPPT consists of the following:

1) Refreshing Unit: A refreshing unit as shown in Fig. 7, is used to periodically refresh the previously-stored V_{REF} and provide a new refreshed value to the control unit as implemented in Ref. [11]. It is located between the tracking unit and the control unit. As it solves the problem when C_R that holds V_{REF} gets a value lower than the previous one. C_R can't be discharged because the active diode prevents the current flows from C_R to C_D leading to a wrong V_{REF} value been sent to the control unit.

a) Working principle: The refreshing unit consists of 4 NMOS devices, 1 PMOS, and a small on-chip capacitor C_0. The operation starts when a new tracking pulse arrives, C_0 is discharged to ground through Q_1. Then, Q_2 is turned on and starts charging the sharing between C_0 and C_R which holds V_{REF}. Since C_0 is much smaller than C_R, the voltage across it is close to V_{REF} in a small period of time. Following that, Q_3 is turned on to discharge C_R at the same time when the output of the refreshing unit is connected to C_0 through Q_4 and C_R is disconnected from VREF_R, then enough time is left for C_R to be charged with new V_{REF} and the voltage is maintained across it even after the tracking pulse goes off. The output of the refreshing unit (VREF_R) is hooked back to C_R through Q_0 and disconnected from C_0 by turning off Q_4.

2) Pulse generator: The pulse width of the tracking signal directly affects the time of the energy harvesting from the piezoelectric transducer. Thus, the duty cycle of the tracking signal should be kept as low as possible. On the other hand, the vibration frequency varies with the environment in real-life applications, which makes it difficult to design a pulse generator of different frequency values. Therefore, the signal from the transducer is used to generate the tracking signal of pulse width 2T to assure that the minimum requirement of 1.5T is satisfied.

a) Working principle: The terminals of the transducer are fed into a comparator that generates pulses that have the same frequency of the ambient vibration. A digital counter and a D-flip flop with asynchronous reset are used to produce a tracking pulse with a fixed duty cycle of 1/64, i.e., around 1.56%.

A 6-bits digital counter, shown in Fig. 8, is used to divide the frequency of the vibration over 64, the counter consists of a series of 6 D-flip flops. In each one, $\overline{Q}$ is connected to D input and the input signal is connected to clock terminal (Clk), where the output signal is half the frequency of the input signal. D-flipflop is used with an asynchronous reset signal that has a period of 4T and pulse width of 2T to generate the tracking signal. The circuit is powered from the C_s capacitor that acts as an initialization node for the tracking pulse generator. The last flip-flop is not clocked unless its Reset signal is High, which only happens after the first cycle, as initially "the signal CompOut" is zero at the onset of the oscillation of the transducer. The output is High for twice the period of oscillation (dominated by reset pin) every 64T (from frequency divider connected to last flip-flop clock). Therefore, no racing will happen within the circuit operation. Correspondingly, there is no need for a power-on reset (POR) circuit. The pulse generator's tracking signal is used to produce the associated control signals for the refreshing unit, as shown below:

$$S1 = \overline{Q' + C4 + CompOut} \tag{6}$$

$$S2 = \overline{Q' + C4 + CompOut'} \tag{7}$$

$$S3 = \overline{Q' + C4' + Out1} \tag{8}$$

$$S4 = Q\ \&\ Out1 \tag{9}$$

3) Control unit: The control unit as shown in Fig. 9, is a voltage band-band controller that keeps the output voltage of the energy harvester to approximately 4 times of V_{REF} as a result of (5). It consists of a Schmitt trigger and a resistor divider which is used to produce V_1 and V_2 to the control unit. The values of the resistors are chosen to make $V_1 = 0.25V_s + \delta v_1$ and $V_2 = 0.25V_s - \delta v_2$, respectively. Where δv_1 and δv_2 are two small voltage values represent 1.8% and 0.6% of $VREF_R$ respectively, the values for R_1, R_2 and R_3 are 45 kΩ, 370Ω and 15 kΩ

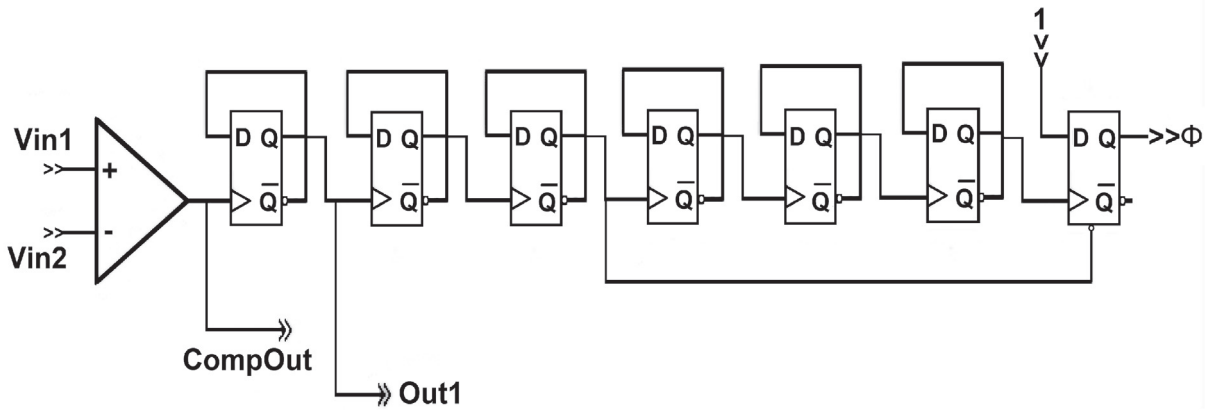

Fig. 8. Block diagram of the tracking pulse generator.

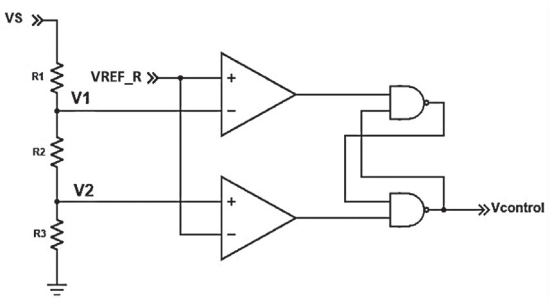

Fig. 9. Control unit circuit schematic [9].

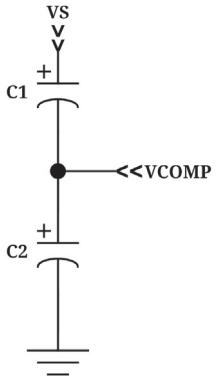

Fig. 10. Capacitor divider circuit schematic.

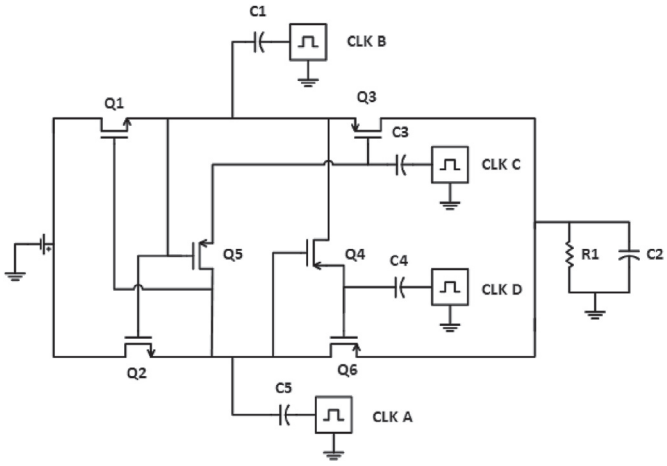

Fig. 11. Modified Pelliconi Charge Pump Circuit [31].

respectively. When V_s is charged up to $4V_1$ which is equal to $V_s + 4\delta v_1$, $V_{Control}$ becomes low and this turns on the operation state and wakes up the system from the sleep mode. Power is then transferred to the load. When V_s is lower than $4V_2$ which is equal to $V_s + 4\delta v_2$, $V_{Control}$ becomes high and this turns off the system.

4) Capacitor divider: To power up the circuits that operate in the sub-threshold region, for instance, the comparators, the control unit, and pulse generator circuits,a supply voltage of 1 V is needed to reduce the current driven from the source at higher voltages. A capacitor divider circuit as shown in Fig. 10 is used, the values of C_1 and C_2 are 2 μF and 3 μF respectively.

3.4. DC-to-DC converter

The DC-to-DC converter is considered as one of the most critical circuits. It can be found in most electronic devices such as cellular phones and laptop computers. Its main function is converting a DC supply voltage from a level to another whether increasing or decreasing. Most of the devices need a specific level of voltage as high voltage may destroy them or low voltage does not allow them to operate properly [29].

In the proposed system, the input voltage needs to be boosted from 2.5 V to 3.3 V to fit with the target application. A charge-pump based approach is chosen. Since it offers less implementation area compared to LC-based boost converters [30]. The working principle of the charge pump is based on accumulating the charges in the coupling capacitors until reaching the desired voltage at the output. The adopted design has been proposed in Ref. [31] and is denoted by the modified Pelliconi charge pump and shown in Fig. 11.

Considering the design of a simple Pelliconi charge pump: these instants (CLK C, CLK D, transistor Q4 and Q5 shown in Fig. 11) are ignored. As CLK A goes from high to low and CLK B goes from low to high, transistor Q1(Q2) will be turned off and transistor Q3(Q6) will be turned on simultaneously. But actually the Q1(Q2) will not be turned off completely when Q3(Q6) is turned on which provides a leakage path and the voltage holds at the capacitors Cap1 and Cap2 will be degraded. Therefore, the operation of the modified charge pump circuit is based on reducing the leakage current between the transistors during the clock transitions to increase the output voltage and the voltage conversion efficiency. The extra clocks (CLK C, CLK D) is to control the time intervals between the clock transitions.

The charge pump operates in four intervals. The first time interval T1: CLK A, CLK B, CLK C, CLK D are high, low, high and high respectively. At this moment, Q3 is turned off and Q1 is turned on to charge

Cap1 with VDD and Q1 is turned on to transfer charges from the input to Cap1. At the same time, the Cap2 is charged to 2VDD and Q6 is turned on to transfer the voltage from Cap2 to the output. Q5 is turned on to transfer charges from Cap2 to Cap3. Simultaneously, Q2 and Q3 are turned off to cut off the leakage path between Cap2 and the input and the leakage path between the output and Cap1 respectively.

At the second and fourth Intervals T2, T4: CLK A, CLK B, CLK C, CLK D are low, low, high and high respectively. At this interval, transistors Q1 and Q3 are turned off as the gate-source voltage is zero. At the same time, Q4 and Q5 are turned on to charge the Cap3 and Cap4 to 2VDD which keeps the PMOS devices (Q3 and Q6) off as the gate voltage across them is higher than their source voltage.

At the third interval T3: CLK A, CLK B, CLK C, CLK D are low, high, high and high respectively. At this moment, Q6 is turned off and Q2 is turned on to charge Cap2 to VDD as it transfers charges from the input to the Cap2. At the same time, Cap1 is charged to 2VDD and Q3 is turned on to transfer the voltage from C1 to the output. Q4 is turned on to transfer charges from Cap1 to Cap4. Simultaneously, Q1 and Q6 are turned off to cut off the leakage path between Cap1 and the input and the leakage path between the output and Cap2 respectively.

The four periods of operation are shown in Table 2 and their waveforms are shown in Fig. 12 [31]. These clocks are generated from off-chip oscillators that can take power from the transducer in case of charging or from the supercapacitor in case of discharge.

Table 2
The four periods of operation.

interval	T1	T2	T3	T4
CLKA	1	0	0	0
CLKB	0	0	1	0
CLKC	1	1	1->0	1
CLKD	1->0	1	1	1

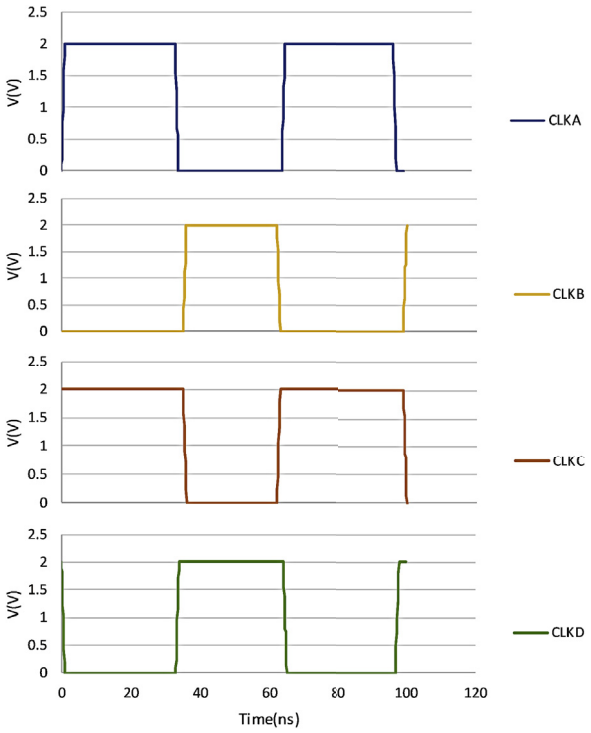

Fig. 12. The four periods of operation on the waveforms.

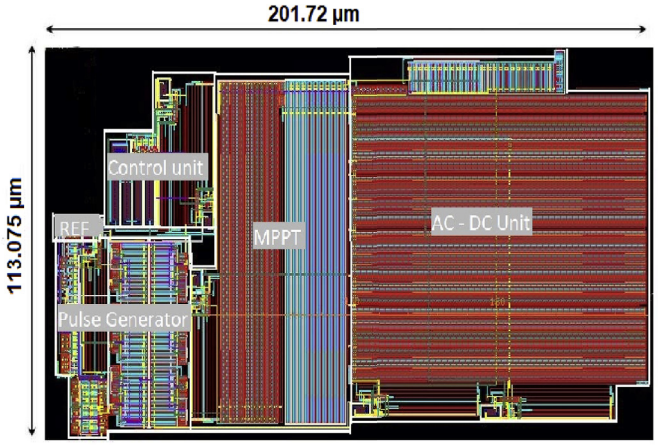

Fig. 13. The layout of the AC-DC block with the MPPT and its associated blocks.(Main Block).

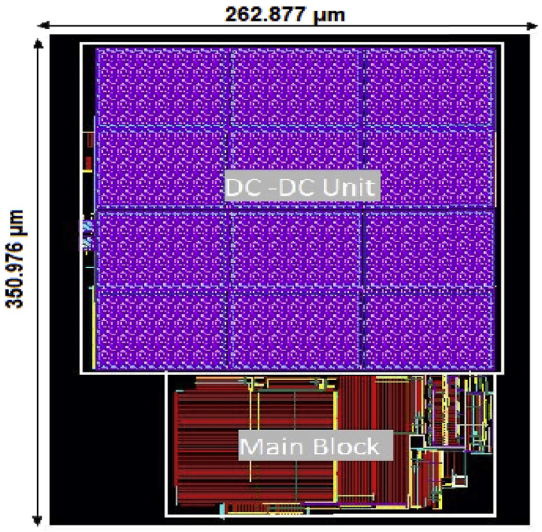

Fig. 14. The layout of the whole system.

4. Post-layout simulation

4.1. Layout

The system layout is shown in Figs. 13 and 14, and is implemented by using hardware-calibrated UMC 130 nm CMOS technology and all the following simulation results are post-layout simulations. The layout area of each block is listed in Table 3.

Table 3
Area of different blocks of the Layout.

Block	Area
AC-DC	10588.25 µm^2
control	1659.57 µm^2
MPPT	5382.08 µm^2
Pulse Generator	2783.22 µm^2
Refresh Circuit	37.3 µm^2
System AC-DC	22809.49 µm^2
System DC-DC	77184.64 µm^2
The whole system	92263.5 µm^2

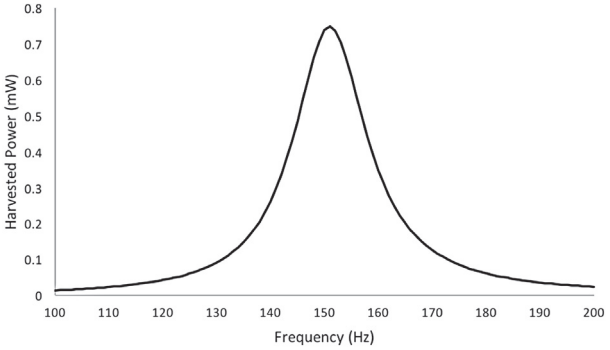

Fig. 15. Plot the of harvested power of the transducer versus the excitation frequency.

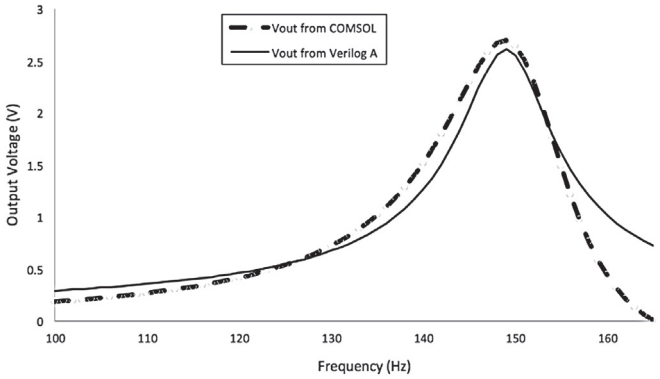

Fig. 16. Plot of the output voltage of the transducer versus the excitation frequency for COMSOL and Verilog-A models.

4.2. Piezoelectric transducer

The harvested power of the vibration energy harvester is plotted as a function of the excitation frequency as shown in Fig. 15. The maximum power harvested is located at the resonance frequency which is about 149 Hz.

The system model is simulated by Verilog A in order to validate the model and include the transducer in the whole system. The values of the output voltage from the transducer simulation in cadence have been compared with the results of COMSOL Multiphysics simulations as shown in Fig. 16 which shows good matching between the two models.

4.3. AC-to-DC converter with MPPT

Post layout simulation results of the input and the output of the AC-to-DC converter are plotted in Fig. 17. The transient waveform of the input (Vin1) and the output voltage of the AC-to-DC converter show high voltage conversion efficiency of 92.6% at the resonance frequency. The comparator current consumption for a wide range of supply voltage values, with the help of the capacitor divider, doesn't exceed 10 nA. This resulted in low static current which led to minimization in the power overhead of the comparators. This is very helpful as the comparators represent a large part of the whole system.

a) AC input response: At different frequencies in the range of the bandwidth of the transducer, different values of input voltages are generated. The response of the AC-to-DC converter with different values of input voltages is investigated as shown in Fig. 18.

b) Frequency response: The response of frequency variations is investigated, especially for leakage current which increases significantly with the increase of vibration frequency, as shown in Fig. 19.

c) Load variation response: The change in the output resistance affects the power conversion efficiency significantly, as shown in Fig. 20. Taking into consideration that the load resistance represents the DC-DC converter block in the system.

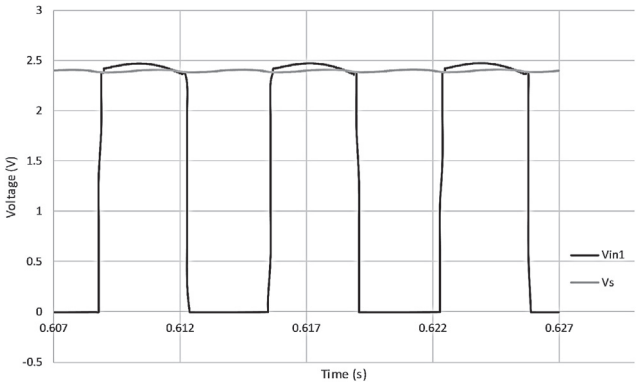

Fig. 17. The input (Vin1) and the output voltage of the AC-to-DC converter.

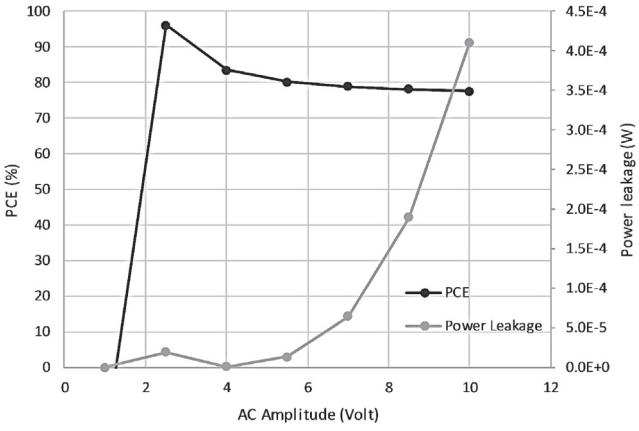

Fig. 18. Power conversion efficiency and power leakage Vs AC Amplitude voltage.

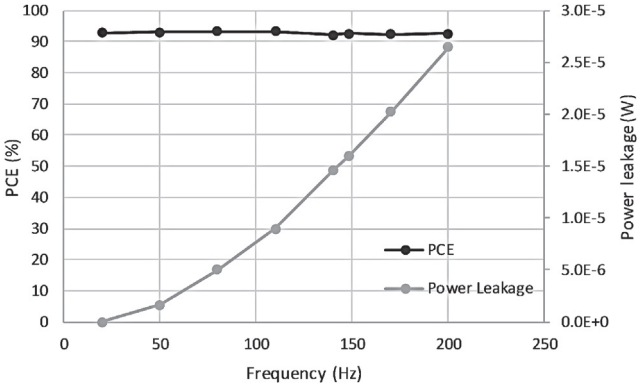

Fig. 19. Power conversion efficiency and power leakage Vs Frequency.

4.4. MPPT

a) Tracking Pulse generator: The MPPT unit is able to track the optimum voltage for maximum harvesting power, producing V_{REF} nearly equal to 0.25 V. Fig. 21 shows how Cs (22 μF) is charged by AC-DC and not affected by MPPT operation for the small duty cycle of the tracking signal.

b) Refreshing unit control: The associated signals that control the

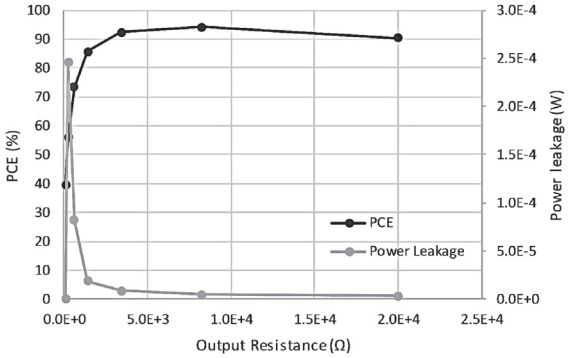

Fig. 20. Power conversion efficiency Vs Output resistance.

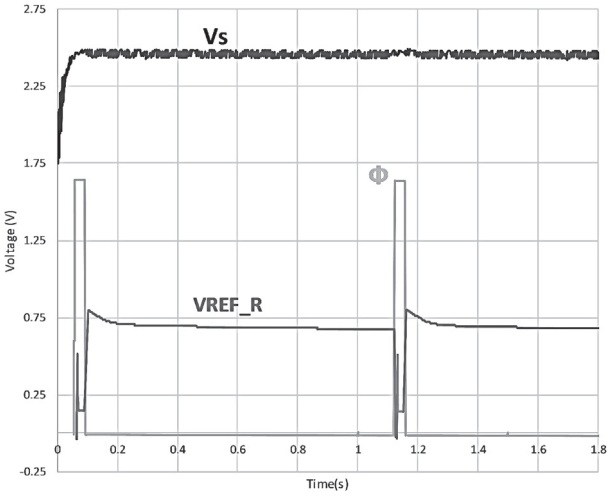

Fig. 21. Simulated waveforms of vibration tracking unit, VREF_R ≈ 0.25 Vs.

refreshing unit and update the V_{REF} and each tracking process cycle are shown in Fig. 22.

The whole MPPT block succeeds in capturing the optimal voltage for the maximum power extraction as shown in Fig. 20, and this increases the power conversion efficiency for the AC-to-DC converter from 85% in optimal condition to 91%.

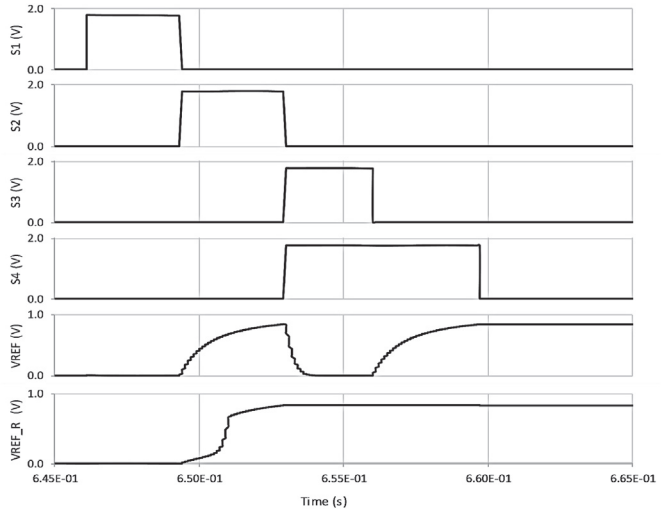

Fig. 22. Associated control signals and the operation of the Refreshing unit.

Table 4
Charge pump design parameters.

Component	Value
Cap1, Cap2	25.1 pF
Cap3, Cap4	25.57 fF
Q1, Q2	W = 10 μm, L = 340 nm
Q3, Q6	W = 10 μm, L = 300 nm
Q4, Q7	W = 5 μm, L = 300 nm
R1(out)	5 KΩ
Cap3(battery)	1.5 mF
Frequency	15.62 MHz
Input impedance	3.8 kΩ
Efficiency	73.3%

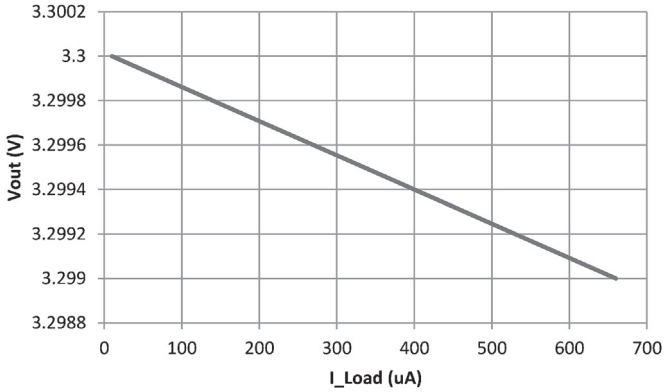

Fig. 23. Load Regulation of DC-to-DC converter.

4.5. DC-to-DC converter

The design has been simulated in Cadence Virtuoso using the values of the components showing in Table 4.

Conducting post-layout simulations show that the charge pump efficiency is 91.35%. Moreover, DC-DC converter load regulation is shown in Fig. 23 and equals −1.54 V/A. In addition, the line regulation is shown in Fig. 24 which equals 0.78 V/V, whereas the ripple factor is calculated by using $\sqrt{\left(\frac{I_{rms}}{I_{avg}}\right)^2 - 1}$, where I_{rms} is root mean square current and I_{avg} is average current and equals 0.0045, as shown in Fig. 25.

4.6. Corner analysis

As shown in Figs. 26 and 27, the PCE maximum value occurs at typical PMOS and NMOS conditions. The leakage power is maximum at

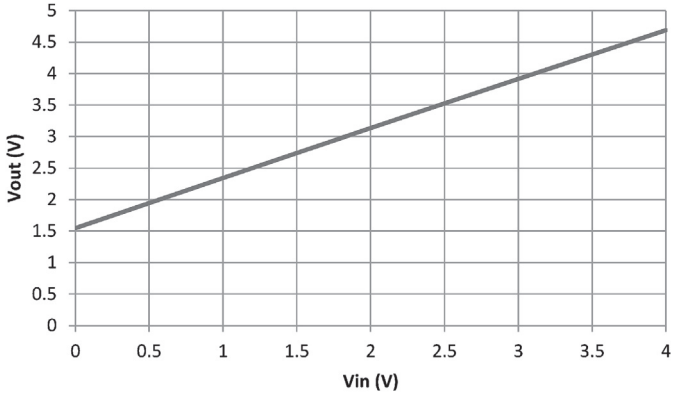

Fig. 24. Line Regulation of DC-to-DC converter.

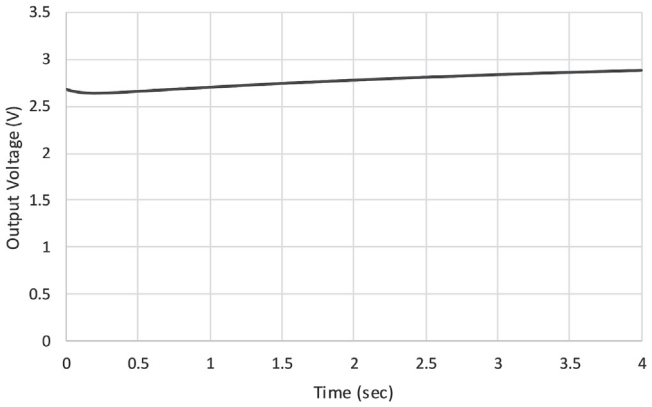

Fig. 25. DC-to-DC converter Output with ripple factor = 0.0045.

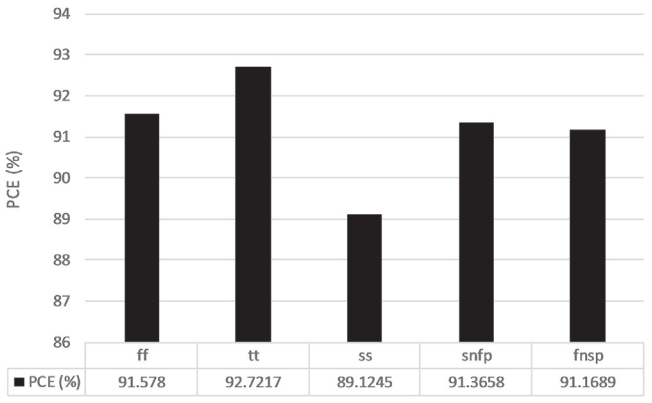

Fig. 26. Corner analysis results for power conversion efficiency for the AC-to-DC converter with load resistance of 5 kΩ.

"ff" (fast N fast P) condition as the comparators run in the sub-threshold region.

The corner analysis is mainly important for the AC-to-DC part of the system because the power leakage is mostly in it as it contains the majority of the transistors. While the DC-to-DC block specs are not affected much in the corner analysis.

4.7. Noise analysis

The output noise is the root mean square sum of the integrated noise caused by the whole system. As shown in Fig. 28, the output noise is dominated by flicker noise at the low frequencies where the AC-to-DC converter operates. Then, it decreases gradually to be dominated by thermal noise at higher frequencies where the DC-to-DC converter operates and the output is DC.

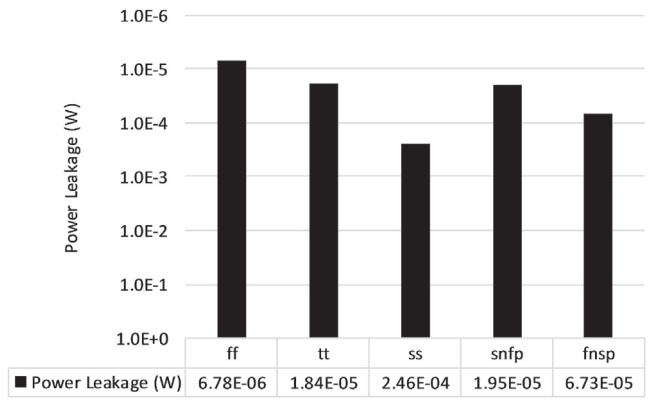

Fig. 27. Corner analysis results for power leakage of the AC-to-DC converter.

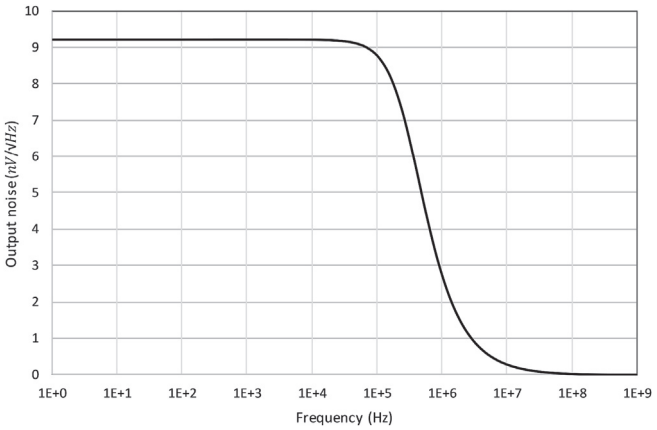

Fig. 28. Output Noise behavior.

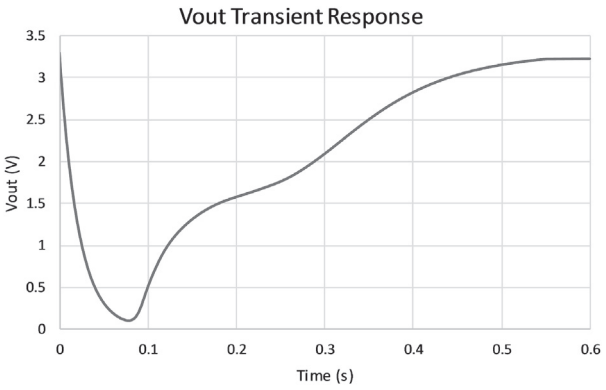

Fig. 29. Self-start operation and V_{out} stable at 3.3 V.

5. The whole system

The system shown in Fig. 1 has been post-layout simulated.

The system has the capability to self-start up when there is no power available. Then, it can sustain a stable operation as shown in Fig. 29. This figure demonstrates that the self-start up operation of the system when there is no energy stored in the supercapacitor Cout (1.5 mF) and that takes around $\frac{1}{2}$ a second. This demonstrates the ability of the implemented system to be used in the applications without a battery (i.e., self-powered systems).

The whole system except the DC-to-DC converter works at 149 Hz. As the DC-to-DC converter works at 15.625 MHz. This big difference in frequency generates the idea of simulating the whole system at the transducer's frequency. So, the DC-to-DC converter is implanted using Verilog-A by taking into account the non-idealities and the efficiency of the system. Then, the entire system is combined and simulated. To get the power conversion efficiency of the whole system, there are two ways. The first one is theoretically calculating the PCE from multiplying the efficiencies of each block. From the previous simulation results, the AC-to-DC converter combined with the MPPT block has an efficiency of 88%. While the DC-to-DC converter has an efficiency of 73%. So, the resulted efficiency of the whole system:

$$PCE_{system} = PCE_{AC-to-DC+MPPT} * PCE_{DC-to-DC} = 0.88 * 0.73 = 0.6424 = 64.24\% \quad (10)$$

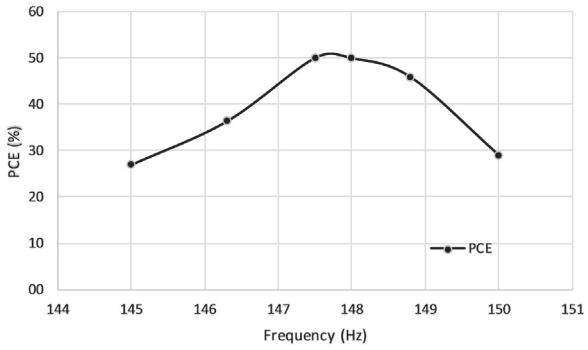

Fig. 30. Power conversion efficiency Vs frequency of vibration to whole system using a Verilog-A model for DC-to-DC converter.

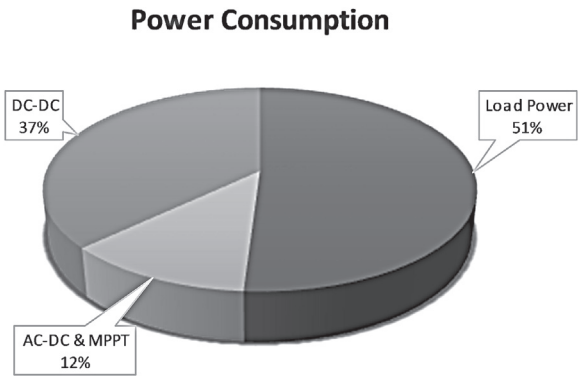

Fig. 31. Power consumption pie-chart.

The second way to get the PCE of the whole system is by dividing the power resulting from the system by the power supplied to the system. This is done by extracting these values through simulation. The harvested power from the system is modeled by the load resistance and the storage capacitor. While the supplied power to the system is generated by the piezoelectric transducer. Therefore, accurate efficiency is calculated from the following equation:

$$PCE_{system} = \frac{P_{res} + P_{cap}}{P_{in} + P_{cap}} \tag{11}$$

6. Results and discussion

In the presented system, the storage capacitor represents the battery which is considered as an input when it charges the system and output when it is being charged. The efficiency of the system at the resonance frequency = 51.4%, and the efficiency changes with changing the frequency of the transducer as in Fig. 30. This efficiency is less than calculated because the equation does not take into consideration the amount of power dissipated by the control unit, pulse generator, and refreshing unit. That resulted from the fact that these blocks are difficult to be estimated as they don't operate all the time but the final result of PCE incorporates all these sources of dissipation. The minimum load resistance that can be supported by the proposed system is 5 kΩ. Fig. 31 shows how the system power consumption is distributed among the system different blocks. It is apparent that the DC-DC converter consumes around 37% of the power, the AC-DC converter and the MPPT consumes about 12% from the harvested power, whereas the remaining power (i.e., 51.4%) is used by the target application.

Table 5 shows the performance of the proposed system compared to recently published work. In this work, the PCE is close to that of [4]. However, [4] occupies a larger area although [4] has not implemented the MPPT block or DC regulation. Moreover, [6] has included

Table 5
Performance comparison with previously published works.

	Aktakka's [4]	Ng's [6]	Oh's [7]	Do's [8]	Ramadass's [9]	Hou's [10]	Lu's [11]	This work
Process	0.18 µm CMOS	N/A	0.13 µm CMOS	0.18 µm CMOS	0.35 µm CMOS	N/A	0.35 µm CMOS	0.13 µm CMOS
Chip area	0.25 mm^2	171 mm^2 (sensor's area)	0.29 mm^2	0.072 mm^2	4.25 mm^2	25 (power mm^2 management chip)	1.68 mm^2	0.09 mm^2
Architecture	Rectifier	Rectifier + Voltage monitoring circuit	Rectifier + Voltage regulator	Rectifier + Voltage regulator	Rectifier + DC-DC Buck + DC-DC Boost + inductor sharing	LTC3331 microenergy collection chip	Rectifier + MPPT + switch or DC-DC converter	Rectifier + MPPT + Charge pump
Input Voltage	N/A	N/A	0.703 V	N/A	N/A	6 V (high potential) 5 V (low potential)	1.8 V	2.5 V
PZE transducer frequency	155 Hz	20–400 Hz	200 Hz	200 Hz	225 Hz	10.6 Hz	0–200 Hz	149 Hz
Storage unit	70 mF super capacitor	47 µF capacitor	N/A	N/A	storage capacitor	22 µF Lithium battery	N/A	1.5 mF super capacitor
Output Voltage	N/A	2.6 V	0.694 V	1.8 V	2.4 V	3 V	0–6 V	3.3 V
MPPT	No	No	No	No	No	No	Yes	Yes
Load Resistance	N/A	9.9 kΩ	45 kΩ	4 kΩ–25 kΩ	N/A	N/A	N/A	5 kΩ
Efficiency (PCE)	50–60 %	1.23 %	52.2 %	83.3 %	77–88 %	0.85 %	90 % <	51.4 %

the DC regulator which occupies a larger area and less PCE than that in the proposed system. Furthermore, the work in Ref. [7] has a slightly higher PCE while it occupies a larger area with no implementation for MPPT. In addition, the authors in Ref. [8] shows better PCE without the ability to regulate voltage or track the input power. On the other hand, other implementations that have used different CMOS technologies such as [9,11] exhibit better PCE with much higher area compared to the proposed system.

7. Conclusion

Piezoelectric is one of the promising energy harvesting methods as it provides an acceptable amount of power by changing the kinetic energy to electric energy. That's why this project focused on designing and implementing a fully integrated piezoelectric energy harvesting system. The proposed fully integrated system has the advantage of the device-circuit co-design by the design of the piezoelectric transducer using COMSOL Multi-physics CAD tool, modeling the device using Verilo A, integrating the device with the CMOS transistors. This enables energy harvesting systems designers to achieve higher system efficiencies by optimizing the overall system at the device-circuit levels. The proposed system achieves much lower area compared to other systems in the literature with comparable system efficiency. The proposed compact system is well-suited for low power applications.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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