A Novel Highly Linear Voltage-To-Time Converter (VTC) Circuit for Time-Based Analog-To-Digital Converters (ADC) Using Body Biasing

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Abstract: Time-based analog-to-digital converter is considered a crucial part in the design of software-defined radio receivers for its higher performance than other analog-to-digital converters in terms of operation speed, input dynamic range and power consumption. In this paper, two novel voltage-to-time converters are proposed at which the input voltage signal is connected to the body terminal of the starving transistor rather than its gate terminal. These novel converters exhibit better linearity, which is analytically proven in this paper. The maximum linearity error is reduced to 0.4%. In addition, the input dynamic range of these converters is increased to 800 mV for a supply voltage of 1.2 V by using industrial hardware-calibrated TSMC 65 nm CMOS technology. These novel designs consist of only a single inverter stage, which results in reducing the layout area and the power consumption. The overall power consumption is 18 μW for the first proposed circuit and 15 μW for the second proposed circuit. The novel converter circuits have a resolution of 5 bits and operate at a maximum clock frequency of 500 MHz.

1. Introduction

Analog-to-digital converter (ADC) is considered the link between the real world, represented by real-time analog signals (speech, radar, medical imaging, etc.), and the digitized world, represented by digital integrated circuits, microprocessors and microcontrollers. ADCs are the key components in most recent electronic devices especially in software-defined radio (SDR), biomedical devices and low-power electronic devices.

Recent ADC architectures are facing many serious limitations due to CMOS technology scaling [1]. One of these limitations is the degradation of the signal-to-noise ratio (SNR) due to the reduction of the supply voltage. Moreover, the dynamic range of analog input signal is reduced as the threshold voltage is not affected by the continuous scaling of CMOS transistors.

These limitations led to the design of the time-based analog-to-digital converter (T-ADC). In this ADC, the input voltage signal is converted to a delay signal first where the delay is proportional to the input signal value. Following that, this delay signal is converted to a digital code. This allows the

processing of the signal to be in the time domain [2]. This is an important advantage because time resolution has been improved in nanometer-scale devices due to the reduction of gate delay, despite the reduction in supply voltage.

The T-ADC consists of two stages, as shown in Figure 1a. The first stage is a voltage-to-time converter (VTC) that converts the input signal to delay pulses. The delay in each pulse is proportional to the value of the input voltage signal. The second stage is a time-to-digital converter (TDC) that converts these delay pulses to a digital code [3].

(**a**)　　　　　　　　　　　　　　　　　　　　　　　　　　(**b**)
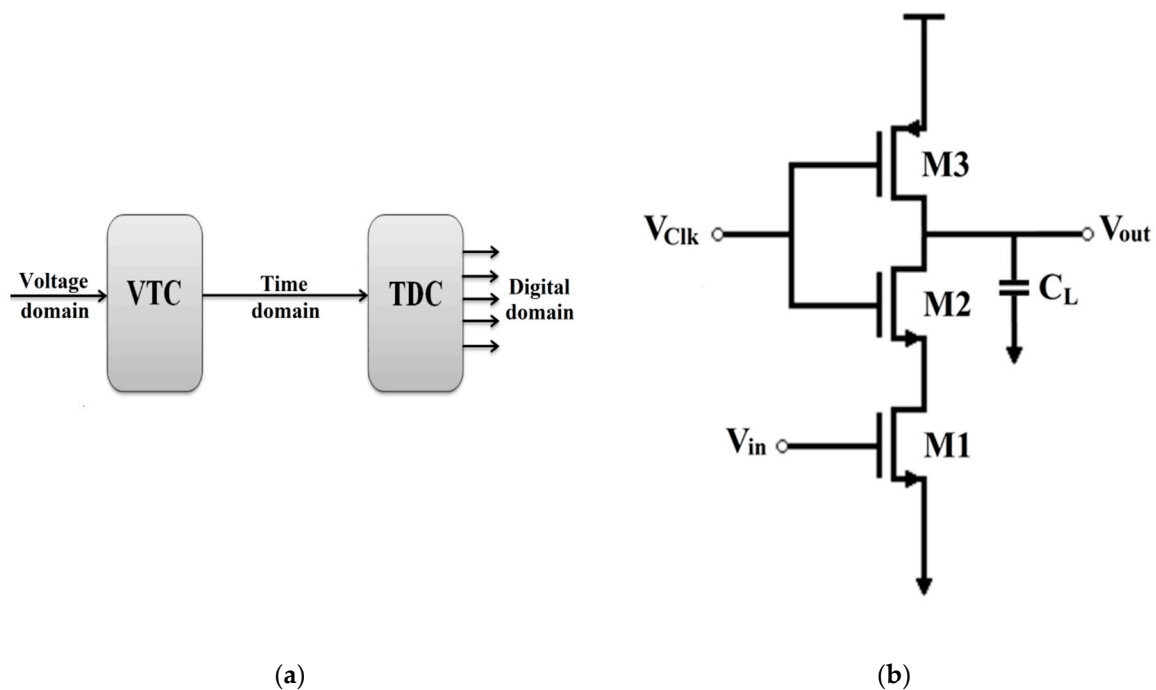
Figure 1. (**a**) Time-based analog-to-digital converter (ADC) architecture, and (**b**) simple current starving inverter.

The most commonly used VTC circuit is the simple current starving inverter shown in Figure 1b. It consists of a CMOS inverter with an NMOS starving transistor connected in the driver branch [3]. The input voltage, which is connected to the gate of the starving NMOS transistor, controls the current of the driver branch when the output of the inverter goes from '1' to '0'. In other words, the fall time of the output voltage of the inverter is directly proportional to the input voltage signal.

The performance of the VTC circuit is limited by two major drawbacks. These drawbacks are the output delay non-linearity and the limited dynamic range of the input signal. One of the main challenges in the design of the VTC circuit is the non-linearity that appears in the fall time of the output response for high input values. In other words, when the input voltage increases, the delay curves for the output exhibit much non-linearity, which results in inaccurate conversion of the input signal to digital code.

This non-linearity happens because during the fall time of the output signal, the starving transistor is operating in saturation mode with a current of:

$$I_D \; = \; \frac{K'}{2} \times \frac{W}{L} \, (V_{GS} - V_T)^2 \tag{1}$$

where k′ is a constant, W/L is the aspect ratio of the transistor, V_{GS} is the gate-to-source voltage, which is connected to the input signal, and V_T is the threshold voltage of the starving transistor. The fall-time output delay is determined as follows:

$$I_D = C \frac{dV}{dt}, \ dt = C \frac{dV}{I_D} \tag{2}$$

where C is the parasitic capacitance at the output, dV is the voltage change at the output during discharging from '1' to '0' and dt is the fall-time output delay.

From the two previous equations, it is obvious that the relation between the input voltage and the output delay time is non-linear, and this non-linearity increases by increasing the input voltage.

Limited dynamic range is also considered a major problem in the design of the VTC circuit. The input signal should not have small values because it is connected to the gate of the starving NMOS transistor. Thus, its value must be greater than the threshold voltage of the transistor to turn it on and create a path for the output to ground.

Many modified VTC circuits have been proposed by researchers [3–12] to overcome the previously mentioned drawbacks of the conventional VTC circuit. However, these circuits are not sufficiently linear and have low resolution. In Reference [3], a linearization scheme has been proposed achieving a maximum linearity error of 2%. However, the input dynamic range is only 200 mV. In Reference [4], a VTC circuit is proposed to operate at 5 GS/s. However, the circuit consumes high power of 3.6 mW and has a small input dynamic range of 100 mV. In Reference [5], the authors have modified the VTC circuit in Reference [4] to increase the input dynamic range to 140 mV. In Reference [6], a VTC circuit is proposed at which the input signal is compared with a voltage ramp. Although this design in Reference [6] consumes low power, it operates at a small sampling frequency of 1 MHz. In Reference [7], a differential VTC circuit is proposed to achieve a maximum linearity error of 3% at a very small input dynamic range of 172 mV.

In Reference [8], a VTC is proposed that consists of a track and hold circuit, level shifter and a pulse shape restorer which improves the linearity of the VTC. However, this design does not offer sufficient linearity and suffers from high power consumption. A VTC with a two-step transition inverter delay line is proposed in Reference [9]. However, this design has low sensitivity of 0.1 ps/mV and consumes relatively high power of 180 μW.

In Reference [10], a current-to-time converter (CDC) based on the conventional starved inverter is introduced. However, the maximum linearity error is 2.1% and the modified circuit operates at a low clock frequency of 50 MHz. In Reference [11], a modified VTC is introduced to increase the linearity but the power consumption of this design is high (3.35 mW), and the input dynamic range is limited to 400 mV. In Reference [12], a fully digital time-based ADC is proposed to reduce the chip area at which the power consumption is reduced to 380 μW but still relatively high.

Another promising approach is using Voltage-Controlled Oscillators (VCO) instead of the VTC at which the frequency of the VCO is proportional to the input voltage signal [13]. VCO-based ADCs are all-digital ADCs that operate at low power consumption levels and consume lower chip areas. However, VCO-based ADCs have a significant drawback which is the non-linearity of the VCO. Moreover, VCOs are sensitive to process, voltage and temperature (PVT) variations [14].

In Reference [13], an all-digital VCO-based ADC is proposed at which a digital linearization block is implemented. This linearization block uses polynomial-fit non-linearity estimation to suppress the non-linearity. However, this design consumes a relatively high power of 3.3 mW. In Reference [14], a second-order, VCO-based continuous-time (CT) ADC is proposed at which two VCOs are used as integrators to realize second-order quantization noise shaping. However, this design consumes high chip area (0.06 mm^2) and high power (1 mW). In Reference [15], a Nyquist-rate fully synthesizable Successive Approximation Register (SAR) voltage-input ADC is proposed which is based on the Dyadic Digital Pulse Modulation (DDPM). This design has a great advantage of exhibiting very low chip area (0.003 mm^2) and very small power consumption (3.1 μW). However, the sampling frequency is very

low (2.8 kS/s). In Reference [16], a VCO-based non-uniform sampling (NUS) analog-to-digital converter (ADC) is proposed. In this design, there is no need for any continuous-time (CT) comparator or reference generator as the proposed ADC shifts the conventional voltage-domain level crossing to the phase domain. This proposed ADC operates at high sampling frequency of 4 GHz. However, the power consumption is high (49.7 mW), and the chip area used is also high (0.244 m^2). In Reference [17], a voltage-to-frequency converter (VFC) is proposed to achieve a maximum linearity error of 3%. However, this design provides a small input dynamic range of 320 mV.

In this paper, two novel VTC circuits are proposed based on the body biasing technique, where the input signal is connected to the body terminal of the starving transistor rather than its gate terminal. The proposed VTC circuits achieve highly linear output delay response with a wide input dynamic range of 800 mV and a maximum linearity error of 0.55% for the first proposed VTC and 0.4% for the second proposed VTC.

The rest of the paper is organized as follows. Section 2 describes the proposed VTC circuits design and analysis in details. The simulation results are presented in Section 3, followed by a discussion on the important factors that affect the performance of the proposed VTC circuit in Section 4. Finally, the conclusions are stated in Section 5.

2. Proposed Circuits Design and Analysis

The theory of operation for the proposed circuits is based on the body biasing technique at which the input signal is connected to the body terminal of the starving transistor. The body biasing technique results in a highly linear drain current with respect to the body-to-source voltage of the starving transistors, as proven below.

The body biasing technique can be applied on a falling-time starving inverter at which the starving transistor is NMOS. In addition, it can be applied on a rise-time starving inverter at which the starving transistor is PMOS. Both cases are discussed below in detail.

2.1. First Proposed VTC

The proposed circuit is introduced as shown in Figure 2. The input signal is applied to the body terminal of the NMOS starving transistor. The output load capacitance C$_L$ equals to 30 fF (for FO4).
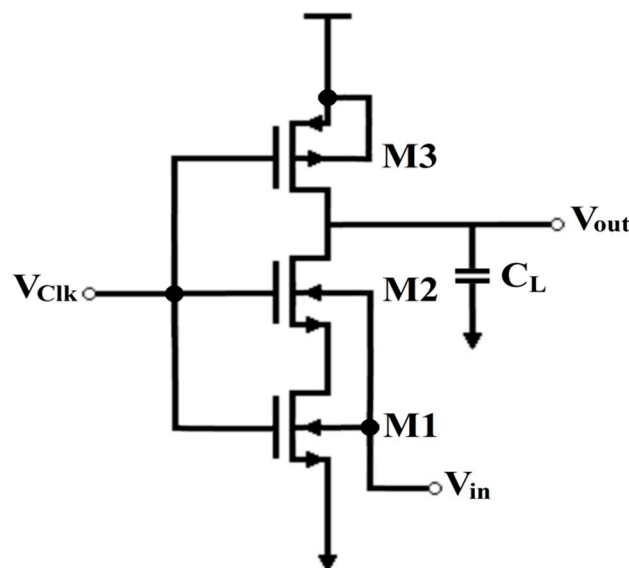

Figure 2. First proposed voltage-to-time converter (VTC) circuit.

In this VTC, the threshold voltage of the starving transistor, V_T, is a function of the body-to-source voltage (which represents the input signal) and is given by:

$$V_T = V_{To} + \gamma \left(\sqrt{\left|2\varnothing_f - V_{BS}\right|} - \sqrt{\left|2\varnothing_f\right|} \right) \tag{3}$$

where V_{TO} is the zero-bias threshold voltage, γ is the body effect factor, V_{BS} is the body-to-source voltage and $\varnothing_f$ is the Fermi potential.

The following analytical proof shows that the body biasing provides a linear relation between the drain current of the starving transistor (which represents the discharging current of the output load capacitance) and the body-to-source voltage. The proof is derived as follows:

$$\because \; I_D = \frac{K_n}{2} \left(V_{GS} - V_T \right)^2 \tag{4}$$

$$\therefore I_D = \frac{K_n}{2} \left(V_{GS}^2 - 2V_{GS}V_T + V_T^2 \right) \tag{5}$$

$$\because V_T = V_{To} - \gamma \sqrt{\left|2\varnothing_f\right|} + \gamma \sqrt{\left|2\varnothing_f - V_{BS}\right|} \tag{6}$$

$$\therefore V_T = V_{To} - \gamma \sqrt{\left|2\varnothing_f\right|} + \gamma \sqrt{\left|2\varnothing_f\right|} \sqrt{\left|1 - \frac{V_{BS}}{2\varnothing_f}\right|} \tag{7}$$

$$\because \; \sqrt{1+x} \cong 1 + \frac{x}{2}, \; for \; x < 1 \quad (Taylor \; series \; expansion) \tag{8}$$

$$\therefore V_T = V_{TO} - \gamma \sqrt{\left|2\varnothing_f\right|} + \gamma \sqrt{\left|2\varnothing_f\right|} \left(1 - \frac{V_{BS}}{2\left|2\varnothing_f\right|} \right) \tag{9}$$

$$\therefore V_T = V_{TO} - \gamma \sqrt{\left|2\varnothing_f\right|} \left(\frac{V_{BS}}{2\left|2\varnothing_f\right|} \right) \tag{10}$$

$$\therefore V_T = V_{TO} - \left(\frac{\gamma}{2\sqrt{\left|2\varnothing_f\right|}} \right) V_{BS} \tag{11}$$

$$\therefore V_T^2 \cong V_{TO}^2 - \left(\frac{V_{TO}\gamma}{\sqrt{\left|2\varnothing_f\right|}} \right) V_{BS} \tag{12}$$

Substitute (11) and (12) into (5):

$$\therefore \; I_D \cong K_1 + K_2 \, V_{BS} \tag{13}$$

where,

$$K_1 = \frac{K_n}{2} \left(V_{GS} - V_{TO} \right)^2 \tag{14}$$

$$K_2 = \frac{K_n \gamma}{2\sqrt{\left|2\varnothing_f\right|}} \left(V_{GS} - V_{TO} \right) \tag{15}$$

From (13) and (2):

$$dt = \frac{C \, dV}{K_1 + K_2 V_{BS}} \tag{16}$$

Multiplying both numerator and denominator by the factor $(k_1 - k_2.V_{BS})$, the fall time delay will be equal to:

$$dt = \frac{K_1 C\, dV}{K_1{}^2 - K_2{}^2 V_{BS}{}^2} - \frac{K_2 C\, dV\, V_{BS}}{K_1{}^2 - K_2{}^2 V_{BS}{}^2} \qquad (17)$$

Since V_{BS} is dominant over $V_{BS}{}^2$ for values below 1, it is clear that the fall time delay (discharging time) of the output signal is linearly proportional to the input signal voltage which is applied to the body terminal.

Adding more series-identical NMOS transistors to the starving transistor helps in improving the performance of the circuit in two ways. First, the overall (*W/L*) of the series NMOS transistors is decreased as follows:

$$\left(\frac{W}{L}\right)_{total} = \left(\frac{W}{L}\right)/N \qquad (18)$$

where *N* is the number of NMOS series transistors. This results in decreasing the discharge current which means that the delay time for the fixed voltage step of the input signal increases. Hence, the resolution of the proposed VTC circuit increases. Second, adding more series NMOS transistors decreases the gate-to-source voltage of the driver transistor M1. This guarantees that the driving transistor is kept in saturation to maintain linearity during all the discharging period of the output load capacitor.

Figure 3a shows the output delay of the proposed VTC circuit versus the number of series starving transistors (N). It is obvious that when the number of series starving transistors increases, the output delay range increases and the sensitivity (the rate of change of the output delay with respect to the input voltage) increases as well. The number of series starving transistors cannot exceed six for a clock frequency of 500 MHz as the output voltage will not have enough time to go logic '0'. For more series starving transistors, the clock frequency should be reduced for proper operation.
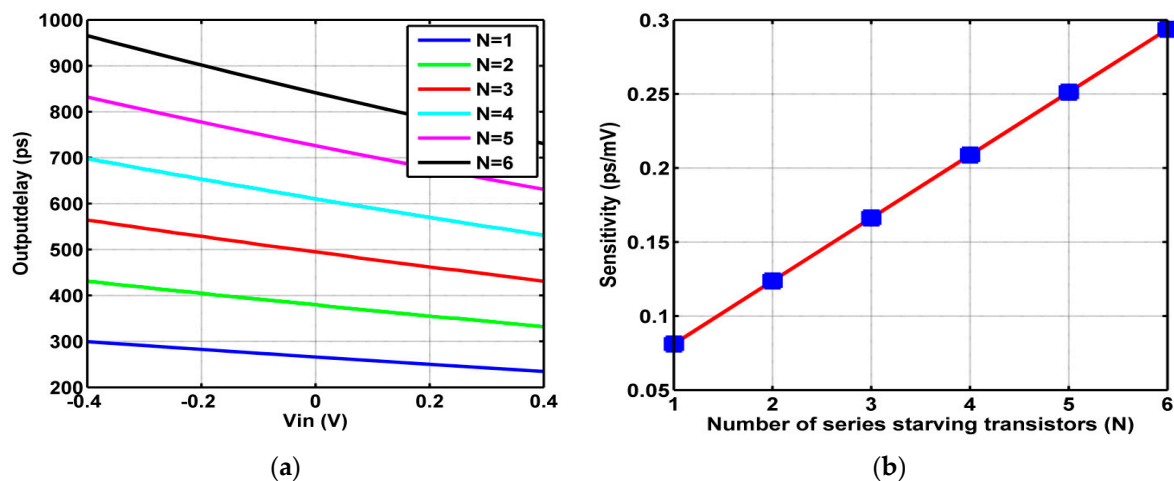

Figure 3. (**a**) Output delay versus number of series starving transistors (N), and (**b**) sensitivity versus number of series starving transistors (N).

Figure 3b shows the sensitivity of the proposed VTC circuit versus the number of series starving transistors (N). For N having the values of four, five and six, the resolution of the proposed VTC will be 5 bits (for a least significant bit (LSB) of 5 ps). Four starving transistors are used for the final architecture of the proposed VTC circuit as it has a lower quantization error than having more starving transistors. Figure 4 shows the final architecture of the proposed VTC circuit.
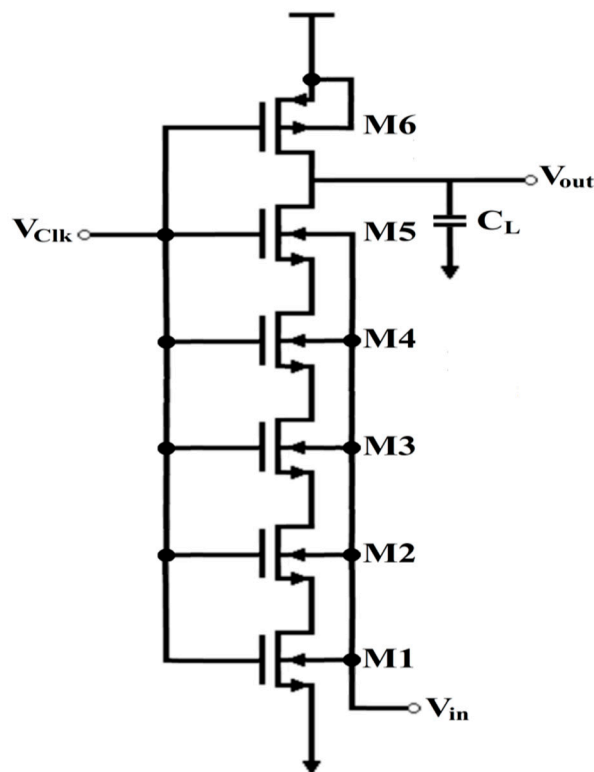
Figure 4. Final architecture of the first proposed VTC circuit.

The Forward Body Bias (FBB) voltage is limited by the forward biasing of the drain-bulk junction (the positive bound of the input voltage connected to the p-Well in case of NMOS and the negative bound of it below the supply voltage connected to the n-Well in case of PMOS). The FBB is also limited by the sub-threshold leakage current [18]. Moreover, the Reverse Body Bias (RBB) voltage bound is determined by the junction leakage current. In case of NMOS, the RBB voltage bound is the negative bound of the input voltage, connected to the p-Well, and the positive bound of over the supply voltage, connected to the n-Well in case of PMOS [18].

The upper limit of the FBB voltage is 0.6 V for latch-up free operation in 65 nm CMOS technology with a supply voltage that ranges from 0.9 to 1.2 V [18–20]. SPICE simulations are done by sweeping the FBB voltage of the PMOS transistor. These simulations show that the upper limit of the FBB voltage equals 0.59 V in order to prevent latch-up triggering for the NMOS transistor. Thus, the maximum FBB voltage is chosen to be equal to 0.4 V to avoid latch-up in case of FBB voltage fluctuations around 0.4 V. Moreover, the RBB voltage is also selected to be equal to 0.4 V. Hence, the FBB and the RBB maximum body voltages are chosen to be equal to ±0.4 V for NMOS devices and 1.2 ± 0.4 V for PMOS devices [18,21].

Thus, the input signal range is taken form −0.4 to 0.4 V, resulting in a full range of 800 mV. The maximum value of the input signal is 0.4 V to avoid latching up [18,21,22]. In other words, a short circuit path occurs between the supply voltage and ground when the body-to-source voltage exceeds 0.4 V in BULK-CMOS technology. This leads to a high current to pass, which results from parasitic bipolar devices in the CMOS circuits.

Latch-up can be avoided during the fabrication process by isolating NMOS and PMOS devices using an oxide trench along with a buried oxide layer. In addition, it can be avoided by increasing the spacing between CMOS devices, although this reduces packing density.

2.2. Second Proposed VTC

The second proposed VTC circuit has the same theory of operation as the first proposed VTC. However, the body biasing technique is applied on a rise-time starving inverter at which the starving transistor is PMOS. As it was proven before in the first proposed VTC, it is concluded that the rise time delay (charging time) of the output signal is linearly proportional to the input signal voltage which is applied to the body terminal.

Figure 5 shows the second proposed VTC circuit. Adding more series-identical PMOS transistors to the starving transistor helps in improving the performance of the circuit. The output delay of the proposed VTC circuit versus the number of PMOS series starving transistors (N_P) is shown in Figure 6a. The maximum number of series PMOS transistors that can be used is four for a clock frequency of 500 MHz. The sensitivity of the proposed VTC is shown in Figure 6b. For a 5-bit resolution VTC, four series PMOS starving transistors are used for better sensitivity and lower quantization noise.
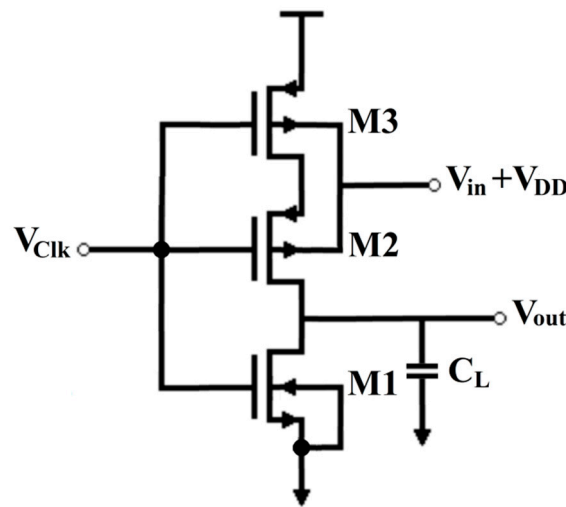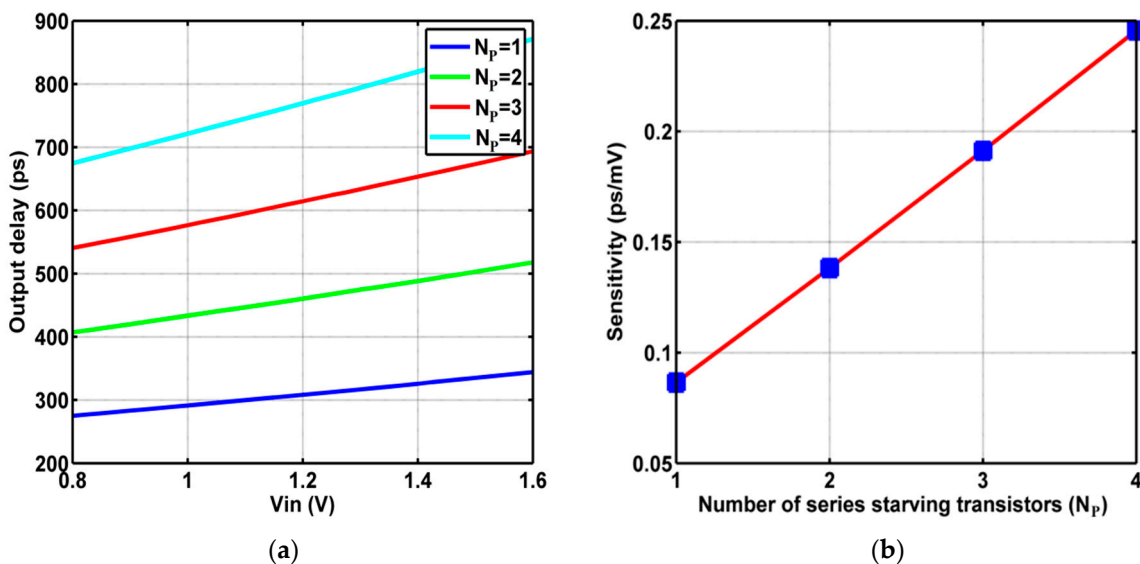

Figure 5. Second proposed VTC circuit.

(a)

(b)

Figure 6. (**a**) Output delay versus number of series starving transistors (N_P), and (**b**) sensitivity versus number of series starving transistors (N_P).

Figure 7 shows the final architecture of the second proposed VTC circuit. The input signal (V_{in}) in the second proposed VTC ranges from −0.4 to 0.4 V with an offset voltage of V_{DD}. This offset voltage

is added as the source of the starving PMOS transistor is connected to V_{DD} keeping the body-to-source voltage (V_{BS}) equal to V_{in}. This input dynamic range ensures that the body-to-source voltage does not exceed 0.4 V to avoid latching-up [18,21,22].
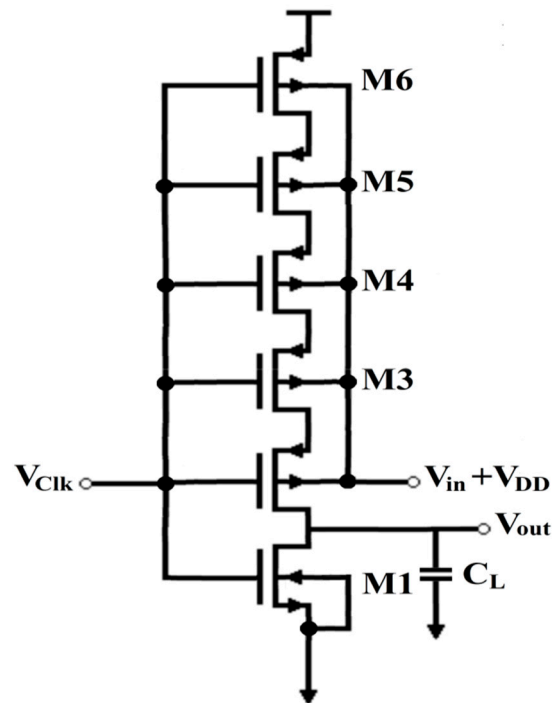

Figure 7. Final architecture of the second proposed VTC circuit.

There are several circuits that can be used to add the supply voltage (V_{DD}) to the input signal (V_{in}). One of these circuits is the non-inverting summing amplifier shown in Figure 8. In this circuit, the input signal (V_{in}) and the supply voltage (V_{DD}) are connected to the positive port of the operational amplifier. The resistors used in this circuit are identical to make the output of the amplifier equal to (V_{in} + V_{DD}). This circuit is implemented off-chip on the PCB (Printed Circuit Board).
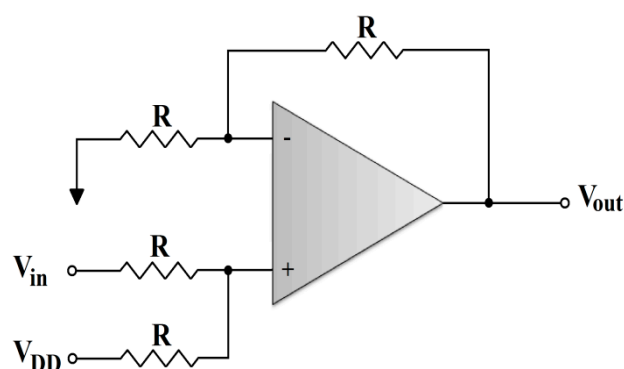

Figure 8. Non-inverting summing amplifier circuit.

3. Simulation Results

The proposed VTC circuits are simulated using Cadence Virtuoso with industrial hardware-calibrated 65 nm transistor device models provided by TSMC. The simulation is performed using a supply voltage of 1.2 V. The Least Significant Bit (LSB), which is mainly dependent on the TDC block, is assumed to be equal to 5 ps, resulting in a resolution of 5 bits for the proposed VTC circuits. The clock frequency equals to 500 MHz and the frequency of the input signal equals to

72.75 MHz. The size of all NMOS transistors used in the two proposed designs is identical and equal to (120 nm/60 nm). This is the minimum allowable size to achieve high output delay range for better resolution. The size of all PMOS transistors is twice that for the NMOS transistor and equal to (240 nm/60 nm).

Figure 9a shows the fall time of the output delay for the first proposed VTC circuit compared with a perfectly linear slope. Moreover, Figure 9b shows the rise time of the output delay for the second proposed VTC circuit compared with a perfectly linear slope. The linearity error for each of the first and second proposed circuits is calculated and plotted in Figure 10. It is obvious that the maximum linearity error significantly decreased to about 0.55% for the first proposed VTC and about 0.4% for the second proposed VTC.
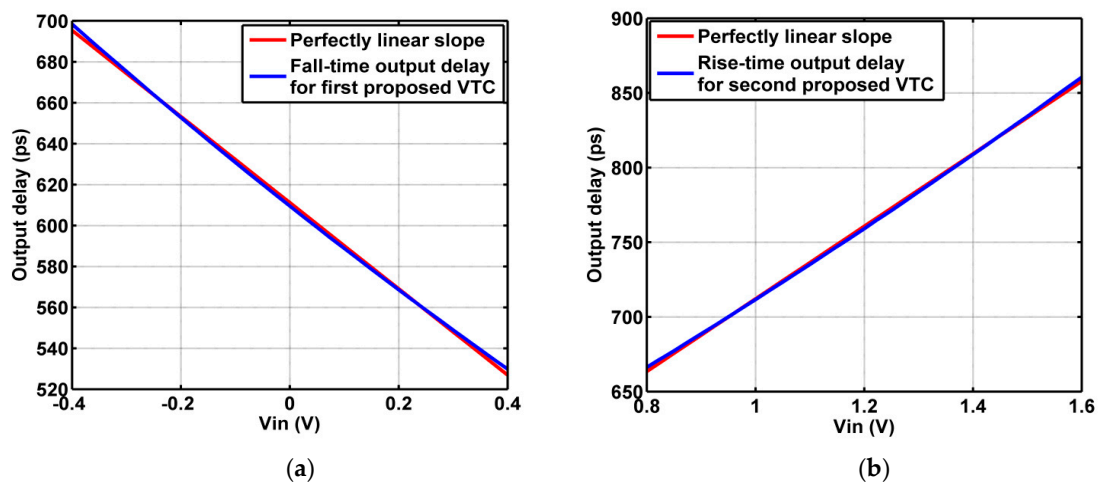

Figure 9. (**a**) Output delay versus a perfect linear slope for the first proposed VTC. (**b**) Output delay versus a perfect linear slope for the second proposed VTC.
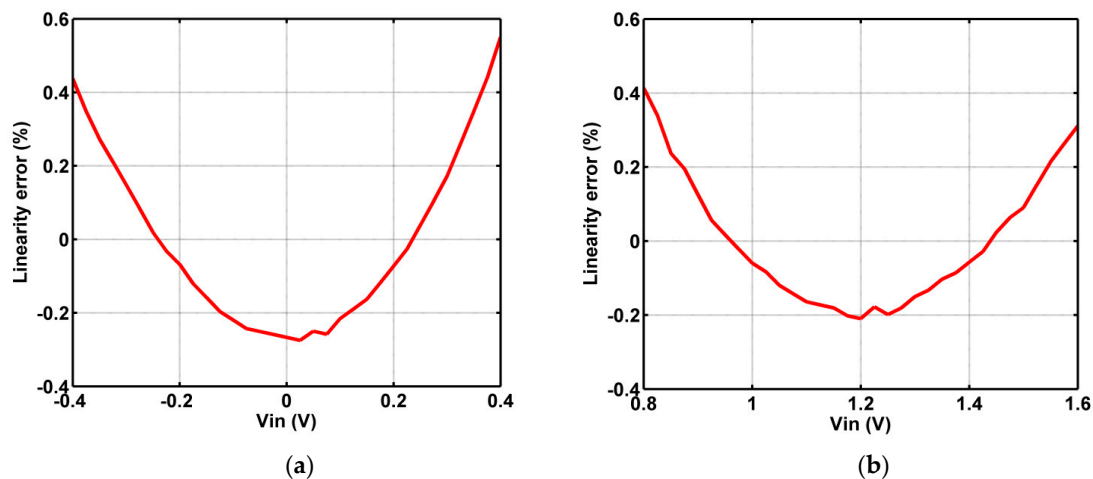

Figure 10. (**a**) Linearity error percentage for the first proposed VTC. (**b**) Linearity error percentage for the second proposed VTC.

Signal-to-quantization noise ratio (SQNR) is a very important parameter that affects the ADC performance. Figure 11a shows the SQNR for different input frequencies. It is obvious that for the effective number of bits (ENOB) to be greater than four, the maximum input frequency is equal to 105 MHz for the first proposed VTC and 95 MHz for the second proposed VTC. Figure 11b shows the power consumption for the proposed VTCs at different input frequencies. It is obvious that the second proposed VTC circuit exhibits lower power consumption than that for the first proposed VTC circuit.
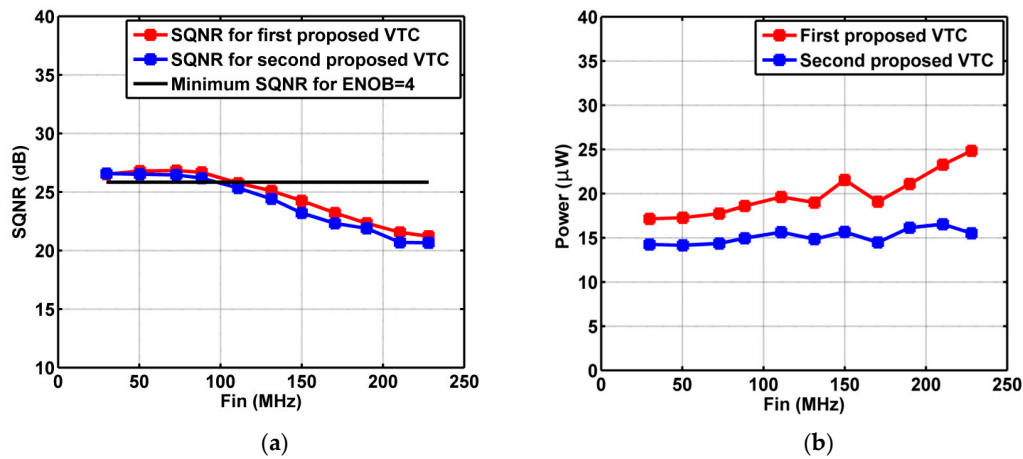
Figure 11. (**a**) Signal-to-quantization noise ratio (SQNR) for different input frequencies, and (**b**) power consumption for different input frequencies.

Figure of merit (FOM) represents the efficiency of the VTC in terms of the power consumption, sampling frequency and the input dynamic range. It can be expressed by two formulas, as follows [23]:

$$FOM1 = \frac{DR^2\, F_S}{P} \tag{19}$$

$$FOM2 = \frac{P}{2^{ENOB}F_s} \tag{20}$$

where DR is the input dynamic range, F_S is the sampling frequency and P is the overall power consumption.

Effective number of bits (ENOB) is calculated by using the FFT (Fast Fourier Transform) method with 1024 samples for an input sinusoidal signal at a frequency of 72.75 MHz and clock frequency of 500 MHz. This specific value for the input frequency is chosen to ensure coherent sampling is achieved for more accurate results [24]. The frequency spectrums of the first and second proposed circuits are shown in Figure 12. Table 1 shows a comparison between the proposed VTC designs and other modified VTCs [25–30]. It indicates that both proposed VTCs have the minimum power consumption while having a wide dynamic input range and better FOM values. Although the design proposed in Reference [25] has a wider input range and operates at higher sampling frequencies, the power consumed by this design is much higher than that for the proposed VTCs.
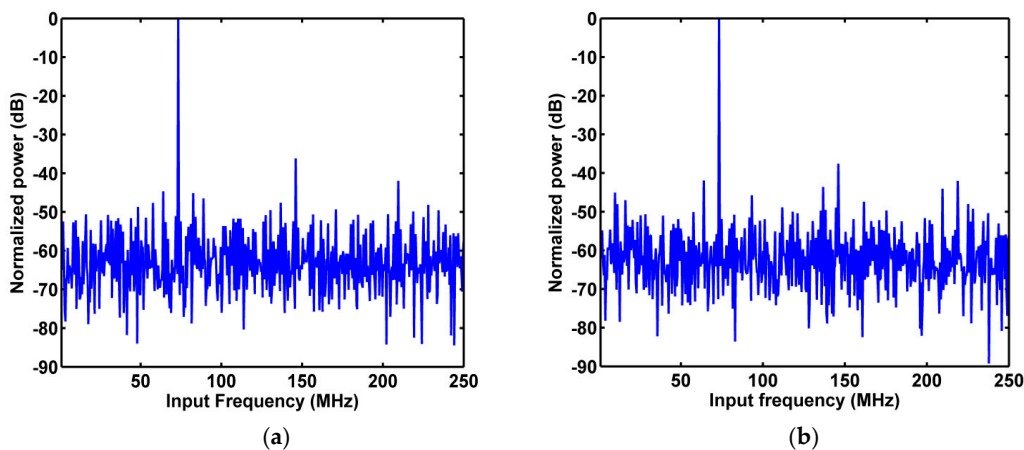

Figure 12. (**a**) Frequency spectrum for the first proposed VTC at F_{in} = 72.75 MHz, and (**b**) frequency spectrum for the second proposed VTC at F_{in} = 72.75 MHz.

Table 1. Performance comparison.

	First Proposed	Second Proposed	[13]	[14]	[15]	[16]	[25]	[26]	[27]	[28]	[29]	[30]
technology	65 nm	65 nm	65 nm	65 nm	40 nm	65 nm	65 nm	65 nm	65 nm	65 nm	65 nm	65 nm
supply Voltage (V)	1.2	1.2	0.6	1.2	0.7	1	1.2	1.0	1.0	1.2	1.05	1.2
dynamic Range (mV)	800	800	600	-	700	-	1200	200	800	600	360	1420
resolution (bits)	5	5	9	-	8	-	8	4	8	4	5	14
sampling Frequency (MHz)	500	500	205	205	0.0028	4000	500	5000	950	1200	5000	250
input Frequency (MHz)	72.75	72.75	7	2	30×10^{-6}	65	250	400	10	602	2500	100
ENOB	4.1637	4.1017	8.1	10.4	6.4	9.2	-	3.5	7.25	3.1	4.1	12.8
max. DNL (LSB)	±0.08	±0.08	-	-	-2.3	-	+0.38	+0.34	+0.6	+0.54	-	-
INL (LSB)/max. INL (LSB)	0.28/−0.44	−0.08/+0.52	−/+1.5	-	−/+2.2	-	−/+0.6	−/+0.38	−/+0.8	−/+0.78	-	-
power (mW)	0.018	0.015	3.3 *	1 *	0.0031 *	49.7 *	0.48	4.1	1.66	0.96	4	0.25
area (mm^2)	26.67×10^{-6}	11.16×10^{-6}	0.026 *	0.06 *	0.003 *	0.244 *	0.012	0.08	0.007 *	0.01 *	0.17 *	2×10^{-4}
FOM1 ($\times 10^{12}$)	17.78	21.33	0.0224	-	44×10^{-5}	-	1.5	0.049	0.366	0.45	0.162	2.1
FOM2 (Pj/step)	0.002	0.0017	0.235 *	0.1509 *	30.9 *	0.2148 *	-	0.62 *	0.016 *	0.196 *	0.17 *	0.00007
simulated/measured	simulated	simulated	measured	measured	measured	measured	measured	measured	measured	measured	measured	simulated

* These numbers are calculated for the whole ADC.

The layouts of the proposed VTC circuits are shown in Figure 13. The first VTC circuit occupies $26.67 \ \mu m^2$, whereas the second VTC circuit occupies $11.16 \ \mu m^2$. Both areas for the proposed VTCs are very small compared to other VTC circuits (as shown in Table 1) thanks to their simple design (one-stage circuit). It should be highlighted that twin-well/triple-well technologies are needed for the NMOS body control in order to isolate the p-well from the p-substrate (by using deep N-well), which results in a higher layout area. This is not needed for the PMOS body control.
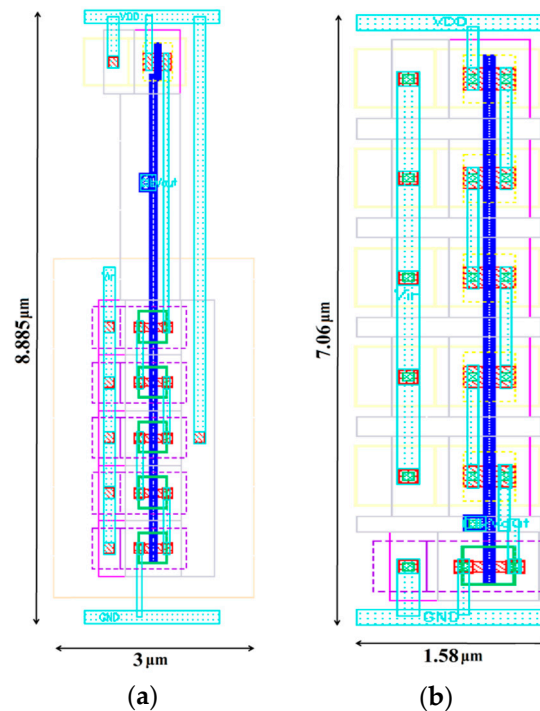
Figure 13. (**a**) Layout of the first proposed VTC circuit. (**b**) Layout of the second proposed VTC circuit.

It should be noted that the simulations provided in this work are post-layout simulations using CAD tools and nowadays, the CAD tools are accurate enough to produce results close to the measured results, especially for mature technologies such as the 65 nm technology.

The power has been calculated taking into consideration the dynamic power as well as the leakage power. However, the proposed circuit provides low power consumption, compared to other papers in the literature, due to its novelty in using the body terminal as an analog input terminal to improve the linearity. This is because usually, the body terminal carries very low current and accordingly, adds insignificant power consumption [18,21].

The proposed VTCs exhibit a significant performance in terms of linearity, power consumption and dynamic range. The proposed VTCs exhibit a maximum linearity error of 0.55% for a wide input dynamic range of 800 mV. The proposed VTCs have very low power consumption due to their simple circuit design, which also results in exhibiting a small chip area. However, the proposed VTCs suffer from low resolution and quite low sampling frequencies. The proposed designs are suitable for applications with limited power budget, such as internet of things (IoT) and wearable devices. In addition, the proposed VTC circuits can be applied for low-resolution ADCs for wireless communication receivers in multiple-input multiple-output (MIMO) systems as the power consumption is a much more important factor than resolution [31–33].

Many research results show that low-resolution quantization technology provides allowable channel capacity loss [31]. Moreover, it is claimed that low-resolution ADCs are better used in massive multi-user MIMO systems as they provide better throughput than that with high-resolution ADCs while keeping the power consumption at lower levels [32,33].

4. Discussion

There are important factors that affect the performance of the proposed VTC circuits. These factors are process-voltage-temperature (PVT) variations, time-to-digital converter (TDC), differential non-linearity (DNL), integral non-linearity (INL) and jitter.

4.1. Process-Voltage-Temperature (PVT) Variations

4.1.1. Process Variations

Process variations are very important factors that measure the performance of the VTC circuit. They affect the output delay of the circuit. Hence, the linearity of the VTC and ENOB are also affected. The performance of the proposed circuits is investigated in terms of maximum linearity error, sensitivity and ENOB for the three main process corners TT, FF and SS, as shown in Table 2. It is obvious that the sensitivity at SS corner increases to 0.405 ps/mV for the first proposed VTC and 0.424 ps/mV for the second proposed VTC. However, the maximum linearity error at SS corner increases to 1.3% for the first proposed VTC and 0.961% for the second proposed VTC.

Table 2. Performance of the proposed VTCs at process corners before calibration.

Process Corners	First Proposed VTC			Second Proposed VTC		
	TT	FF	SS	TT	FF	SS
Maximum Linearity error (%)	0.516	0.02	1.3	0.42	0.0670	0.961
Sensitivity (ps/mV)	0.21	0.1124	0.405	0.242	0.139	0.424
ENOB (bits)	4.16	4.1	3.5	4.1	3.922	3.6

The clock frequency used at process corners is reduced to 400 MHz as the output delay at SS corner exceeds 1 ns. Moreover, the input signal frequency is chosen to be nearly equal to 61.33 MHz to ensure coherent sampling is achieved. Coherent sampling guarantees that FFT results are accurate for proper calculation of ENOB. ENOB decreases to 3.5 bits at SS corner for the first proposed VTC and decreases to 3.6 bits for the second proposed VTC. As a result, calibration for the proposed circuits is needed to improve the linearity and ENOB for the proposed circuits at SS corner.

A calibration circuit for the first proposed VTC is proposed to improve the performance of the VTC at SS corner. The first proposed VTC and the calibration circuit are shown in Figure 14. The calibration circuit consists of a detection circuit and a stack of eight identical NMOS transistors connected between the output node of the VTC and the ground node. The function of the detection circuit is to detect the occurrence of SS corner.
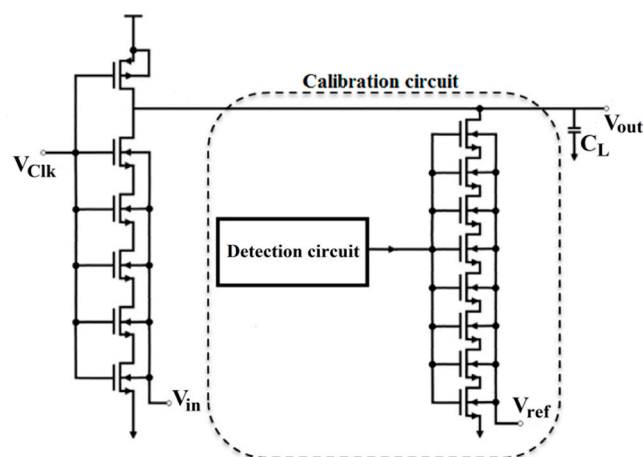
Figure 14. The first proposed VTC with the calibration circuit.

The detection circuit is shown in Figure 15. It consists of two inverters with different load capacitors and a D Flip-Flop (D-FF). The values of the load capacitances are adjusted such that the START signal edge comes before the STOP signal edge only when the circuit operates at SS corner. In this case, the inverted output of the D-FF (Q-bar) will be "1".
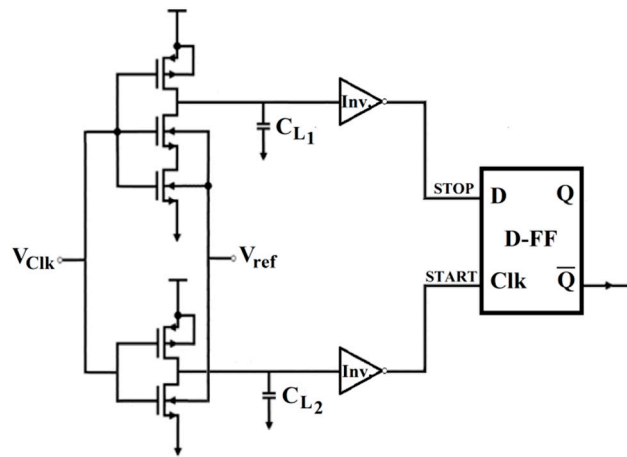

Figure 15. The detection circuit for calibration of the first proposed VTC.

The output of the D-FF activates the stack of NMOS transistors which results in increasing the discharging current of the load capacitance at the output node. This leads to a significant decrease in the output delay range at SS corner to be near the range obtained at the nominal corner TT. The value of the reference voltage (V_{ref}) is set to −0.4 V, which is the minimum allowed voltage. This allows the stack to drive a small current to keep the output sensitivity at acceptable levels at SS corner.

The detection circuit detects only SS corners and the inverted output of the D-FF keeps its state at '0' for TT and FF corners. Moreover, the values of the load capacitances are adjusted such that the state of the inverted output of the D-FF is '0' even if the circuit is subjected to temperature variations. This can be easily achieved as the additional delay produced from temperature variations is less than that at SS corner.

Table 3 shows the change in the performance of the first proposed VTC circuit before and after calibration at process corners. The maximum linearity error at SS corner improved after calibration to be equal to 0.38%. ENOB is also improved to be equal to 4.38 at SS corner after calibration. Although sensitivity is decreased at SS corner after calibration, it becomes near to that value at the nominal process corner. The value of the load capacitance C_{L1} equals 30 fF and the value of the load capacitance C_{L2} equals 55 fF.

Table 3. Performance of the first proposed VTC at process corners before and after calibration.

Process Corners	Before Calibration			After Calibration		
	TT	FF	SS	TT	FF	SS
Maximum Linearity error (%)	0.516	0.02	1.3	0.51	0.02	0.38
Sensitivity (ps/mV)	0.21	0.1124	0.405	0.21	0.1127	0.1624
ENOB (bits)	4.16	4.1	3.5	4.16	4.1	4.38

The second proposed VTC circuit is calibrated by the same technique. Figure 16 shows the calibrated second proposed VTC circuit. The calibration circuit consists of a detection circuit and a stack of eight identical PMOS transistors connected between the supply voltage and the output node of the VTC.
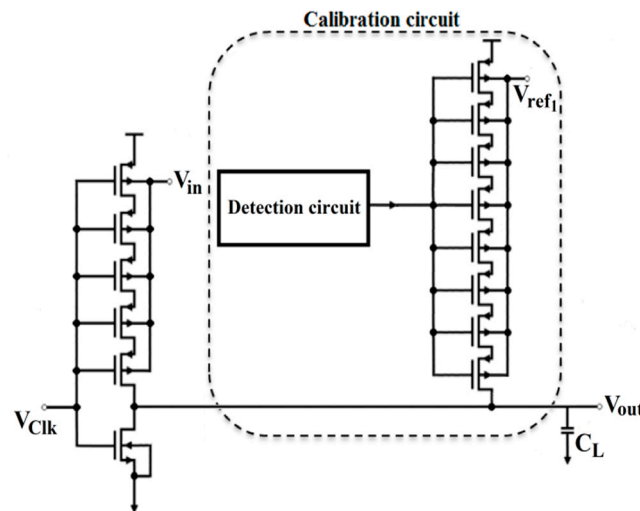
Figure 16. The second proposed VTC with the calibration circuit.

Figure 17 shows the detection circuit. It has the same theory of operation as in the detection circuit of the first proposed VTC. It detects the occurrence of SS corner at which the output of D-FF will be '0' at this corner only. This activates the stack to increase the charging current of the load capacitance at the output node. Similarly, the value of the reference voltage ($V_{ref\,1}$) is set to 1.6 V. This allows the stack to drive a small current to keep the output sensitivity at acceptable levels at SS corner. The value of the load capacitance C_{L1} equals 60 fF and the value of the load capacitance C_{L2} equals 30 fF. The value of the reference voltage ($V_{ref\,2}$) is set to 0.8 V.
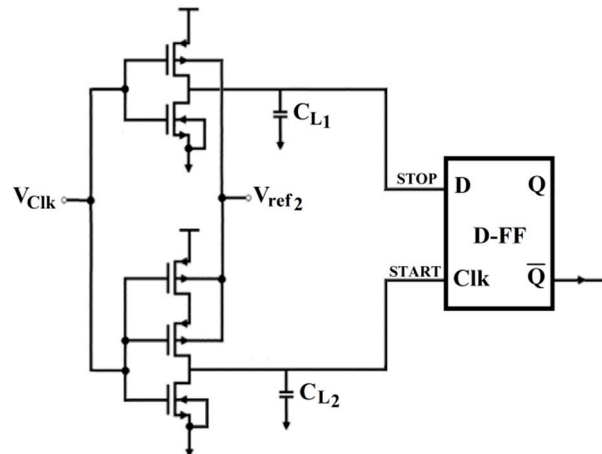
Figure 17. The detection circuit for calibration of the second proposed VTC.

Table 4 shows the change in the performance of the second proposed VTC circuit before and after calibration at process corners. The maximum linearity error at SS corner improved after calibration to be equal to 0.26%. ENOB is also improved to be equal to 4.35 at SS corner after calibration. The sensitivity of the second proposed VTC at SS corner after calibration becomes near to the value at TT process corner. All the NMOS transistors used in the calibration circuits are identical to each other, having the size of (120 nm/60 nm). In addition, all the PMOS transistors used are identical to each other, having the size of (240 nm/60 nm).

Table 4. Performance of the second proposed VTC at process corners before and after calibration.

Process Corners	Before Calibration			After Calibration		
	TT	FF	SS	TT	FF	SS
Maximum Linearity error (%)	0.42	0.067	0.961	0.42	0.068	0.26
Sensitivity (ps/mV)	0.242	0.139	0.424	0.243	0.139	0.1734
ENOB (bits)	4.1	3.922	3.6	4.178	4.26	4.35

4.1.2. Supply Voltage Variations

The supply voltage is one of the most important factors that affect the performance of the VTC circuit. The VTC output delay is calculated for different supply voltages for the two proposed VTC circuits, as shown in Figure 18.
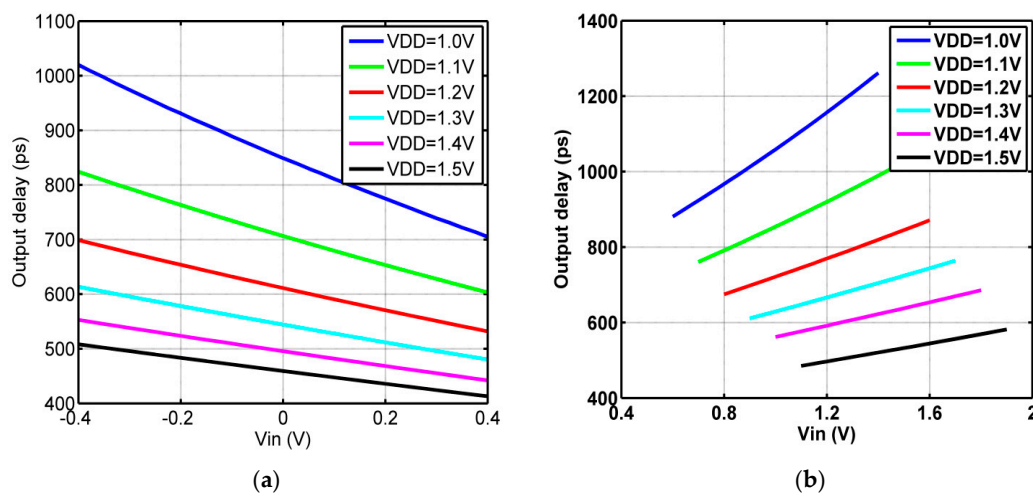
Figure 18. (**a**) Output delay of the first proposed VTC for different supply voltages. (**b**) Output delay of the second proposed VTC for different supply voltages.

As the supply voltage decreases, the output delay range increases, which results in increasing the sensitivity of the proposed VTC circuits, as shown in Figure 19. However, reducing the supply voltage results in degradation of the signal-to-noise ratio (SNR) that limits the performance of the whole ADC circuit [1].
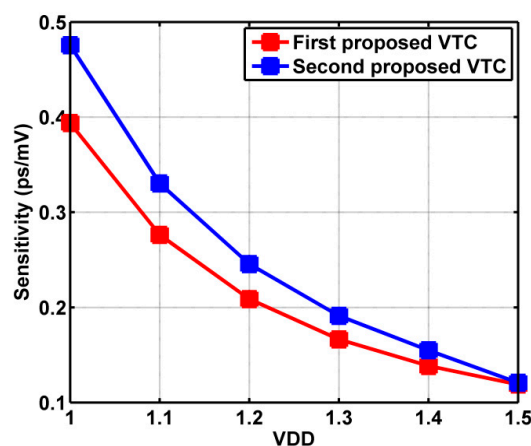
Figure 19. Sensitivity versus supply voltage for the two proposed VTC circuits.

4.1.3. Temperature Variations

Temperature variations have a significant effect on the operation speed of integrated circuits. As the temperature increases, the current driven by transistors decreases, causing additional latency to the output of the circuit. The effect of temperature variations on the linearity, sensitivity and ENOB of the proposed VTC circuits is investigated for a temperature range from −40 to 85 °C. Figure 20a shows the maximum linearity error versus temperature variations for the two proposed circuits. It is obvious that although the maximum linearity error increases with temperature, it does not exceed 1% for the given temperature range. The sensitivity of the proposed VTC circuits shows a slight increase by increasing the temperature, as shown in Figure 20b. Moreover, ENOB for the proposed VTC circuits keeps its value at an acceptable level for the given temperature range, as shown in Figure 20c. The input signal frequency is chosen to be nearly equal to 61.33 MHz at a clock frequency of 400 MHz. In sum, it is obvious that the two proposed VTC circuits show immunity in terms of linearity, sensitivity and ENOB against temperature variations and do not need calibration.
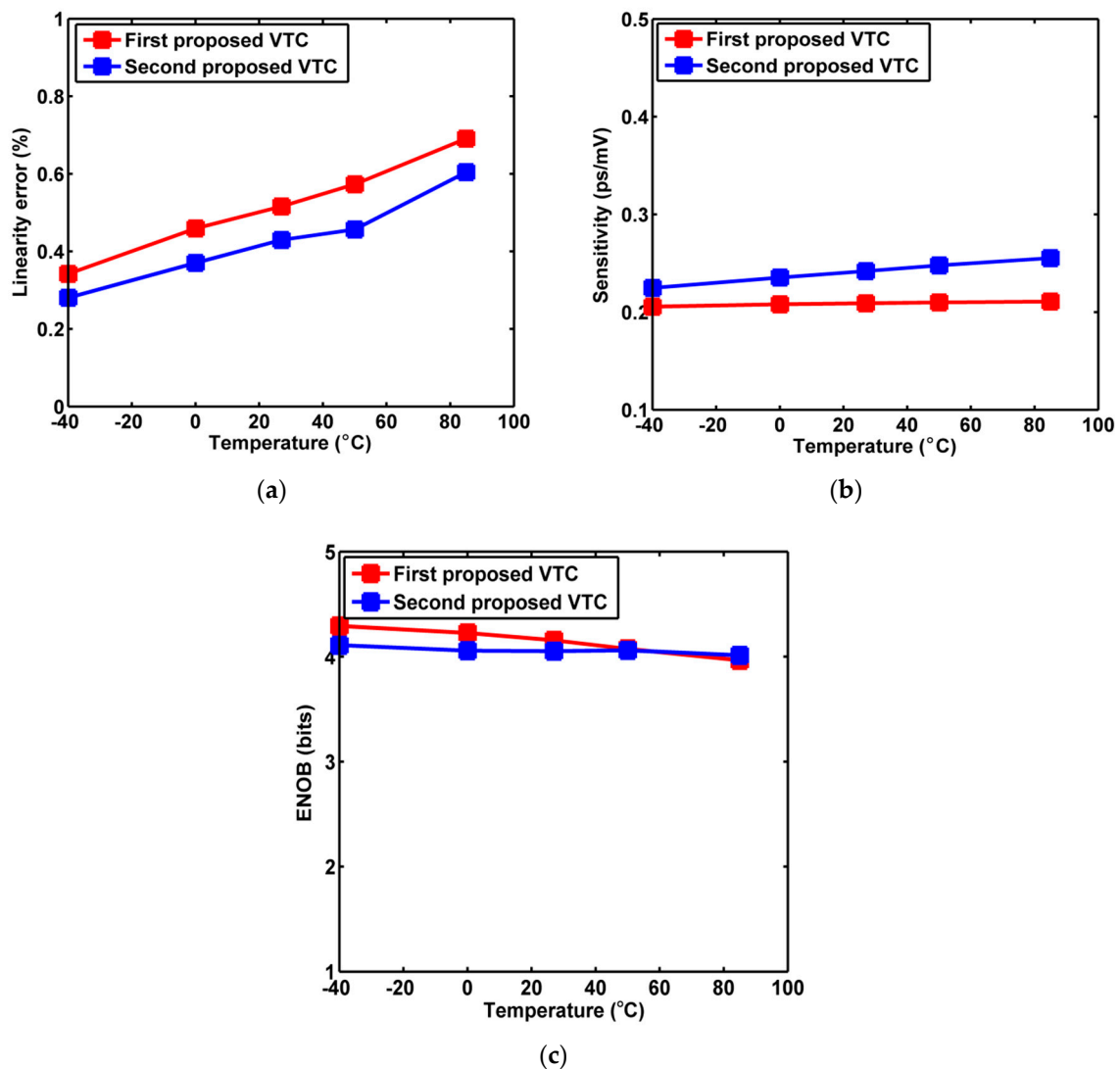

(**a**)

(**b**)

(**c**)

Figure 20. (**a**) Maximum linearity error versus temperature for the proposed VTCs, (**b**) sensitivity versus temperature for the proposed VTCs and (**c**) ENOB versus temperature for the proposed VTCs.

4.2. Time-To-Digital Converter (TDC)

The performance of the VTC is limited by the design of the time-to-digital converter (TDC) circuit that follows it. The TDC affects the linearity of the whole ADC and its performance should be investigated. Differential non-linearity (DNL) and integral non-linearity (INL) are the most important parameters that represent the linearity in the whole ADC. DNL represents the deviation in the conversion step of the ADC from its ideal value (1 LSB), while INL represents the deviation of the whole transfer function of the ADC from its ideal value [34]. DNL value should not exceed 1 LSB in order to avoid missing codes [34]. Thus, each of the two proposed VTC circuits is implemented with a 5-bit vernier delay-line TDC and the whole ADC is simulated.

For the first proposed VTC, an interface circuit is proposed after the VTC in order to drive STOP and START signals to the TDC. Figure 21 shows the interface circuit that is used for the first proposed VTC. The output of the VTC is inverted to produce the START signal. The STOP signal is a delayed version of the clock signal. The delay unit for the STOP signal is the VTC circuit with a reference voltage equivalent to the maximum delay that can be produced from the VTC ($V_{ref} = -0.4$ V).
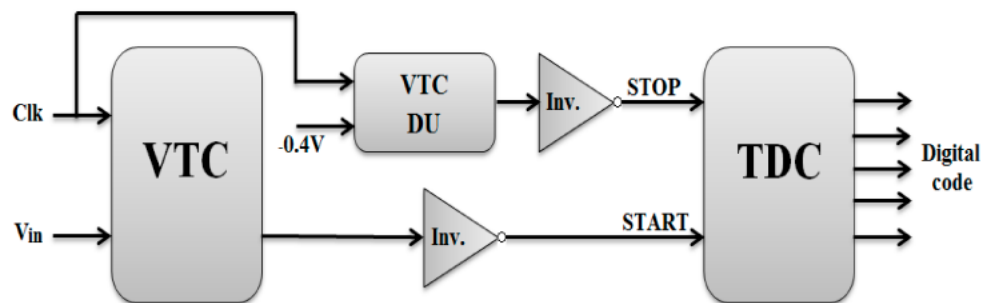

Figure 21. Interface circuit for the first proposed VTC.

A standard vernier delay-line TDC is used in this work. It is most commonly used as it has the advantage of having very high resolution that can be less than the minimum gate delay in the technology used. However, this resolution is limited by other factors such as noise, transistors' mismatch and the delay-line physical length [35]. Many TDC circuits based on the vernier delay-line technique are proposed [36–39] to achieve higher resolution that can reach 3.2 ps [40], 2 ps [41] or even more.

Figure 22 shows a 5-bit vernier delay-line. The delay units (DUs) are CMOS buffers which are controlled by controlling the body-to-source voltage, as shown in Figure 23. When the input signal value is minimum, the START signal comes after the STOP signal for all the D-FFs in the TDC and the output of all the flip-flops is '1'. On the other hand, when the input signal value is maximum, the START signal comes before the STOP signal for all the D-FFs in the TDC and the output of all the flip-flops is '0'. By varying the input signal, the output of the flip-flops will also vary. The output of the flip-flops is an inverted thermometer code. The thermometer code is first converted to a one-hot code using 01-generator circuits [42]. The 01-generator circuit is shown in Figure 24. Then, a digital code is generated using a fat tree encoder [43].
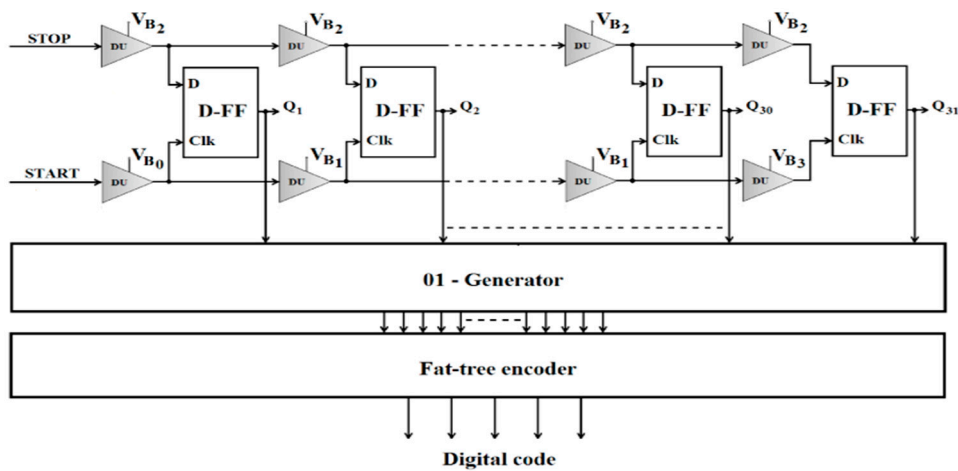
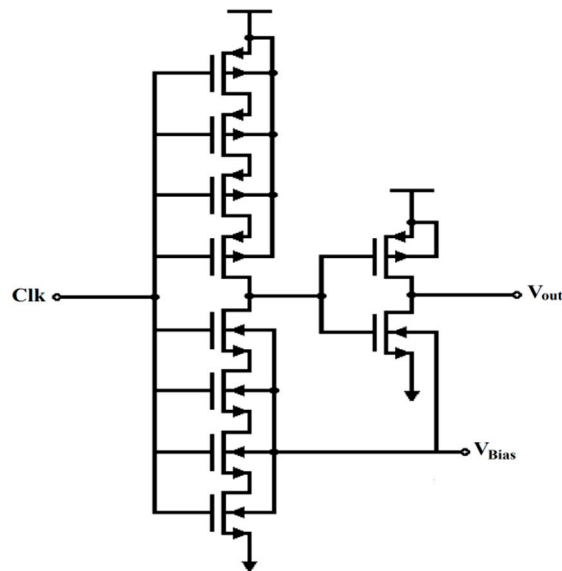**Figure 22.** Vernier delay-line time-to-digital converter (TDC).

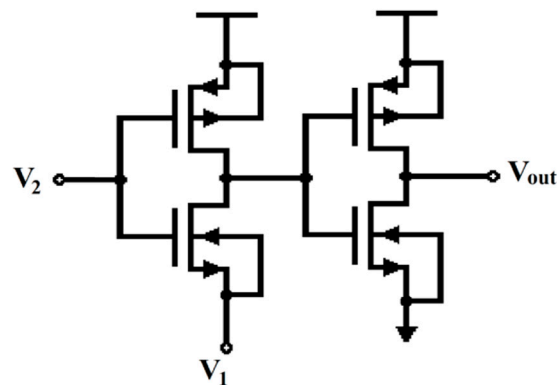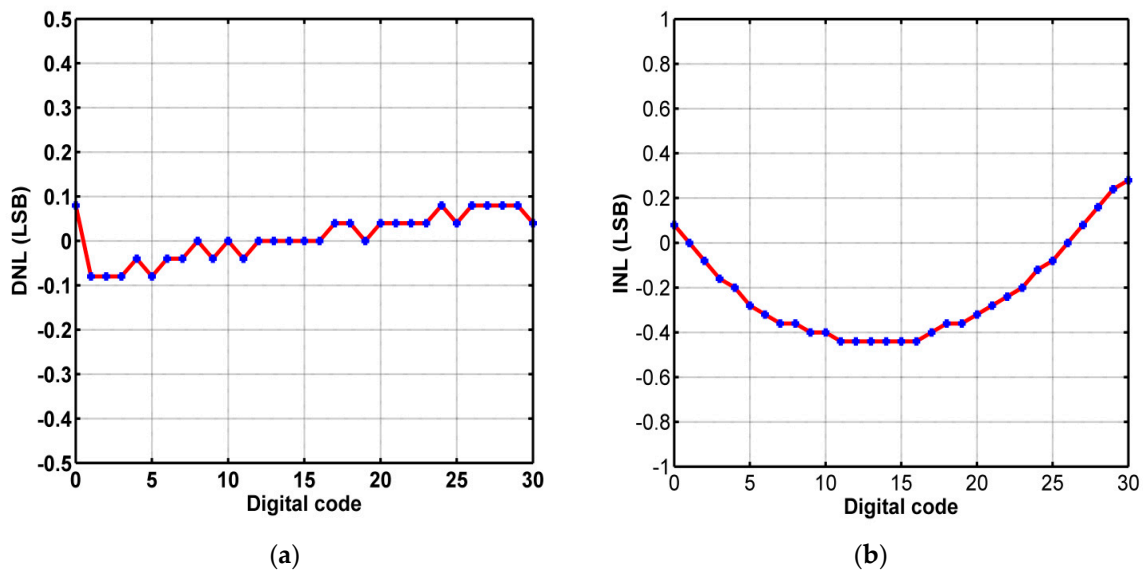**Figure 23.** Delay unit for the first proposed ADC.


Figure 24. 01-generator circuit.

The TDC is manually calibrated by adjusting the biasing voltages for the delay units. The values of the biasing voltages after calibration are $V_{B2} = 0.4$ V, $V_{B1} = 0.075$ V, $V_{B0} = 0.39$ V and $V_{B3} = 0.2$ V. DNL and INL are calculated for the ADC with accuracy of 1 mV (800 points are calculated for 800 mV input range). This means each digital code has 25 calculated points (LSB = 25 mV). Figure 25 shows

DNL and INL for the first proposed ADC. The maximum DNL equals ±0.08 LSB and INL equals 0.28 LSB (maximum INL equals −0.44 LSB).

(a)

(b)

Figure 25. (**a**) Differential non-linearity (DNL) for the first proposed ADC, and (**b**) integral non-linearity (INL) for the first proposed ADC.

For the second proposed VTC, the interface circuit is modified, at which the START and STOP signals are replaced by each other. Moreover, the inverters are replaced by buffers as the output delay of the VTC is a rise time. In addition, the reference voltage used equals 0.8 V, which is equivalent to the minimum output delay of the second proposed VTC. The interface circuit for the second proposed VTC is shown in Figure 26.
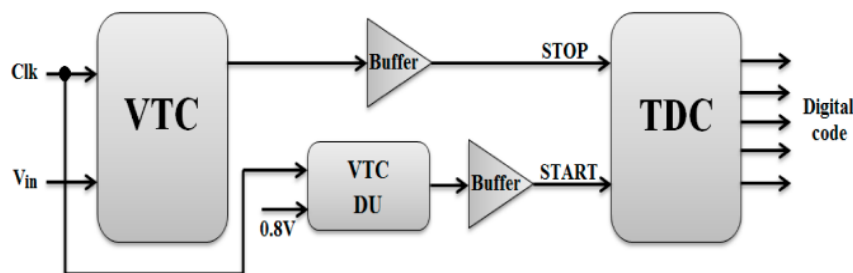
Figure 26. Interface circuit for the second proposed VTC.

The same TDC is used for the second proposed VTC and the delay units are controlled by controlling the body-to-source voltage, as shown in Figure 27. The theory of operation is the same as previously discussed for the first proposed circuit. After calibration, the values of the biasing voltages are $V_{B2} = 1$ V, $V_{B1} = 1.45$ V, $V_{B0} = 0.95$ V and $V_{B3} = 1.6$ V.
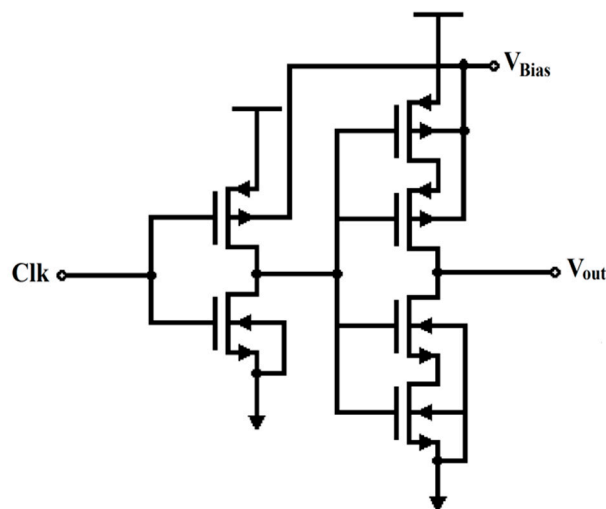
Figure 27. Delay unit for the second proposed ADC.

Figure 28 shows DNL and INL for the second proposed ADC. They are calculated with accuracy of 1 mV. The maximum DNL equals ±0.08 LSB and INL equals −0.08 LSB (maximum INL equals 0.52 LSB).
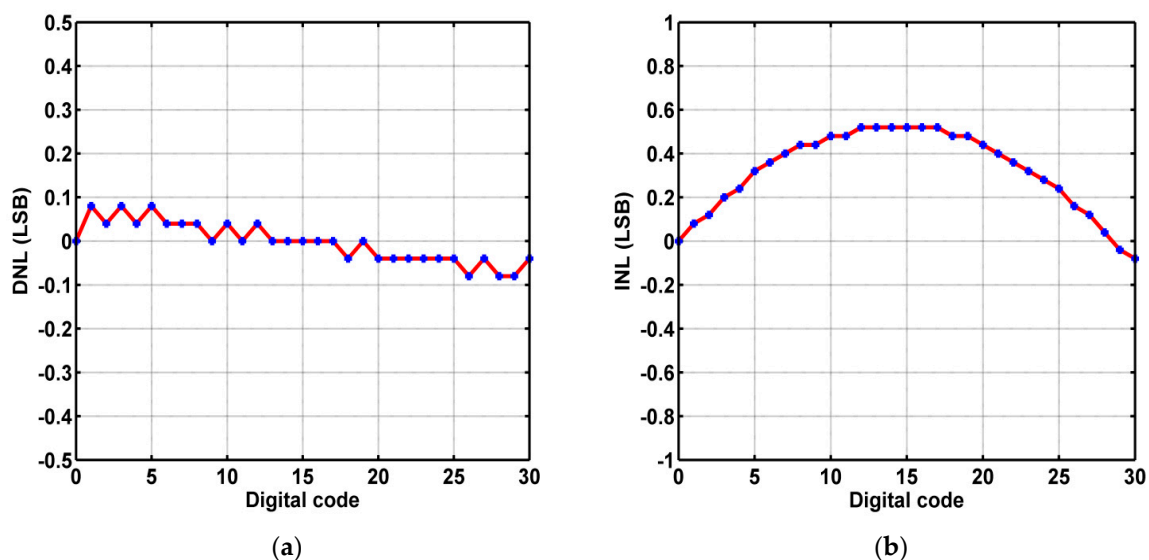

(a)

(b)

Figure 28. (**a**) DNL for the second proposed ADC, and (**b**) INL for the second proposed ADC.

In sum, the two proposed VTC circuits exhibit high performance when implemented with vernier delay-line TDC to construct the whole ADC circuit. DNL and INL for the proposed designs are compared with other modified designs in Table 1. It is obvious that the proposed designs have better DNL and INL results. All the NMOS transistors used in the interface circuit and the TDC are identical to each other, having the size of (120 nm/60 nm). In addition, all the PMOS transistors used are identical to each other, having the size of (240 nm/60 nm).

Figure 29 shows the layout of the two proposed ADCs. The layout includes the two proposed VTCs, the calibration circuits, the interface circuits and the TDC circuits. The first ADC occupies an area of 0.0092 mm^2, while the second ADC occupies an area of 0.0067 mm^2. The first ADC occupies a higher area than the second ADCs due to using triple-well technology (deep N-well layer) for the NMOS body control.
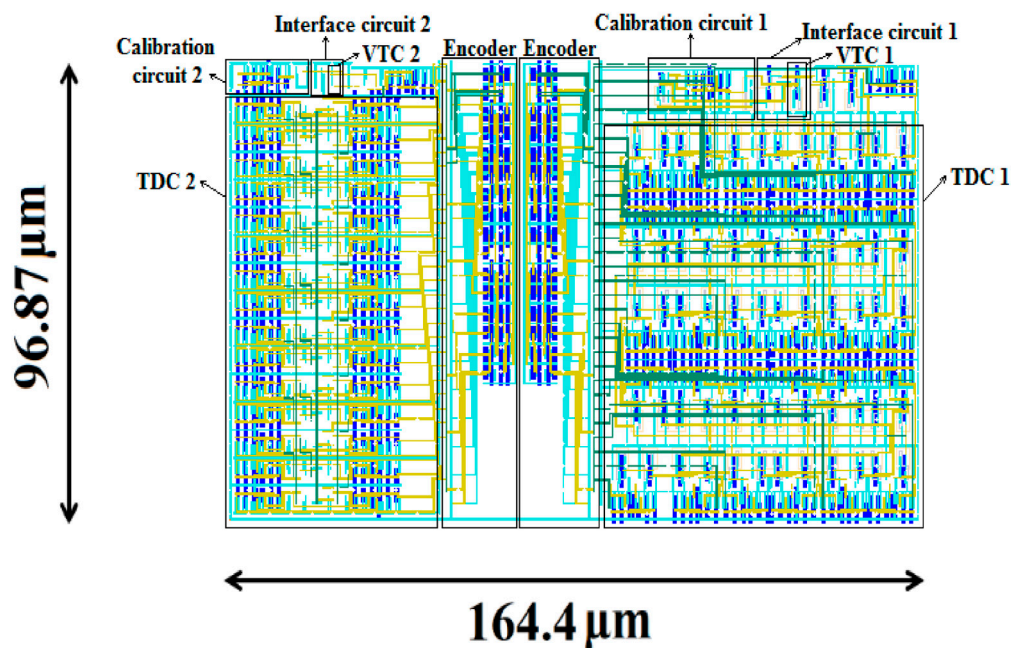
Figure 29. Layout of the two proposed ADCs.

4.3. Jitter

Jitter in VTC represents the random deviation of the output delay signal in the time domain from its ideal value. This shift resulted from random noise. There are possible sources of noise in the proposed VTC circuit that produce this jitter. These sources are thermal noise from the device, noise from the supply lines, noise from the input signal and noise from the following TDC block [5,24]. By considering the jitter effect during simulation of the proposed VTC circuits using transient noise analysis, it is concluded that jitter has an insignificant effect on linearity, sensitivity and ENOB. This is because the circuit is operating at moderate frequency and accordingly, the proposed VTC circuits tolerate the jitter. However, this places a limitation on the proposed VTC if used at high frequencies as the jitter might have a significant effect in this high-frequency case.

For the first proposed VTC, maximum linearity error is 0.55%, and sensitivity equals 0.2108. These values do not change significantly with jitter. ENOB equals 4.163 at F_{in} = 73.73 MHz and F_{Clk} = 500 MHz, and changes to 4.108 when jitter is considered. For the second proposed VTC, maximum linearity error is 0.4%, and sensitivity equals 0.243. These values do not change with jitter. ENOB equals 4.093 at F_{in} = 73.73 MHz and F_{Clk} = 500 MHz, and changes to 4.049 after taking jitter into account.

5. Conclusions

In this paper, two novel VTC circuits were proposed achieving better linearity with wide input dynamic range. The input signal was connected to the body terminal of the starving transistor instead of its gate terminal. The maximum linearity error was 0.55% for the first proposed VTC and 0.4% for the second proposed VTC, with an input dynamic range of 800 mV for a supply voltage of 1.2 V. The proposed VTCs can be used for a 5-bit time-based ADC at a maximum sampling frequency of 500 MHz in 65 nm CMOS technology. Thanks to their simple design, the proposed VTC circuits occupy a small area of 26.67 μm^2 for the first proposed VTC and 11.16 μm^2 for the second proposed VTC, while consuming very small power of 18 μW for the first proposed VTC and 15 μW for the second proposed VTC. The effect of PVT variations on the proposed designs was discussed. In addition, calibration circuits were proposed to overcome the limitations in the VTC circuits' performance due to these variations. Moreover, time-to-digital converter (TDC) and the jitter effect were discussed.

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