Multi-Partitioned Software Defined Radio Transceiver Based on Dynamic Partial Reconfiguration

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***Abstract*—Dynamic Partial Reconfiguration (DPR) proved itself for the implementation of multi-standard Software Defined Radio (SDR). Over the past few years, wireless communication standards witnessed great and rapid evolution. The market is always acquiring higher data rates and more special services. This leads to increase of design complexity, area, and power consumption. Deploying DPR technology on Field Programmable Gate Arrays (FPGAs) made it feasible to design and manufacture all wireless communications standards on the same hardware. Loading each standard on demand reduces area and power consumption. This work implements SDR transceiver system for five wireless communication standards: Bluetooth, Wi-Fi, 2G, 3G, and LTE on Zynq-7000 evaluation kit. A new partitioning approach is deployed to achieve best performance for all transceivers. The new approach proves its ability to reduce the allocated area and power consumption for all chains. Power reduction for 2G and Bluetooth is 98.43%, for 3G and Wi-Fi is 79.69%, for LTE is 50.09% compared with no DPR approach.**

***Keywords*—Software Defined Radio, Dynamic Partial Reconfiguration, Field Programmable Gate Array, and System on Chip.**

I. Introduction

Wireless Communication standards are continuously changing and upgrading to acheive better performance, new features, higher throughput, and new technologies. IC fabrication is becoming more difficult and costly impractical due to the increase of number of standards and technologies required to be implemented in different devices as the handset such as GSM, UMTS, LTE, Wi-Fi, and Bluetooth. The large number of analog and digital blocks of each standard has high power consumption which is a scarce resource for the handset [1]. In order to solve this issue, both user terminal and base station need to adopt dynamic communication chains. So, it is capable of supporting multiple standards which is denoted by Software Defined Radio (SDR).

Field Programmable Gate Arrays (FPGA) are the usual targeted technology for many development efforts due to their low cost and support of Dynamic Partial Reconfiguration (DPR) technology [2]. SDR is expected to be the most appropriate answer to multi-standards handset design challenges [3]. By applying the concept of DPR in SDR with the required capabilities, all standards are allowed to be upgraded by software without the need of hardware upgrading [4]. Various technologies can be used to implement SDR such as ASIC, DSP, and FPGA. Improvements in FPGAs makes realization of SDR possible.

DPR is a promising technology which offers the reconfiguration of a specified partition in FPGA during the run time which helps in implementing a multi-standard SDR [5]. SDR addresses the reconfiguration time of the specified partition on FPGA and switching between different standards to perform the baseband signal processing without affecting the overall performance of any of the standards [6].

This paper is organized as follows: Section II shows the related work. The DPR technique is illustrated in Section IV. Section V contains the simulation results of deploying the SDR using DPR. Finally, Section VI shows the paper conclusion and future work.

II. Background and Previous Work

DPR technique is used to switch between different configurations of LTE OFDM modulator in [7]. Variations are based on the size of the IFFT, number of subcarriers, cyclic prefix and window length. The implemented design on Virtex-7 is divided on four reconfigurable partitions and single static partition for the FFT. Similar design for LTE FFT is proposed in [8] where configuration is dependant on the FFT size.

The purposed dynamic cognitive radios in [9] implements the physical layer on the FPGA Programmable Logic (PL) and the Medium Access Control (MAC) layer on the ARM processor. Switching between different baseband modules is performed using custom partial reconfiguration controller to acheive high reconfiguration speed. Virtex-7 is used host the physical layer blocks.

The SDR physical layer implemented on Virtex-4 using DPR techinique in [2] using internal and external configuration modes. The reconfiguration time overhead is taken in

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consideration. Our recent contribution in [10] is implementing three transmitter chains: Wi-Fi, 3G, and LTE on the same hardware. Partioning is performed on three Reconfigurable Modules (RMs) and single static partition in order to save power and area. The implemented system in [11] is suffering from large switching time overhead due to using single reconfigurable partition.

This work implements five transceiver chains: GSM, UMTS, LTE, 802.11a, and Bluetooth V2 on the same hardware. A new partitioning algorithm is deployed to compute the best splitting critera to minimize the power consumption of all chains. The tranceiver is divided into multi-partitions in order to minimize area, power, and switching time of small chains such as 2G and Bluetooth.

III. Dynamic Partial Reconfiguration

The five transceiver chains implemented in [11] are used to deploy the concept of the SDR. The same test environment mentioned in [10] is used here to test the configuration of the five transceivers. Xilinx Partial Reconfiguration Controller (PRC) is used to control the Internal Configuration Access Port (ICAP) in order to reach the highest throughput while switching between different reconfigurable modules.

In order to achieve the best allocation for all chains, a new partitioning approach is proposed. The new technique proposes splitting both transmitter and receiver partitions into smaller partitions, in order to fit the area of small chains. Meanwhile there are some constrains taken in consideration in order to minimize the wasted area leading to increase of switching time and power consumption:

1) Sizes of the partitions must be relatively multiples of the minimum Reconfigurable Frame (RF) size. As mentioned in [11] the minimum RF area is (400 LUTs or 10 DSPs or 10 BRAMs).
2) Difference between areas of chosen mergable blocks in each chain must be small.
3) Since the FPGA resources (BRAMs and DSPs) are distributed in a certain style, partitions are placed in a certain way not only to fit the required area, but also to comply the rules of placement and routing.
4) Partitions must not be placed vertically in the same clock region, since it is mandatory to reset the whole partition after reconfiguration. Every clock region has its own reset pin.
5) Finally, as the number of partitions increase, the Partial Reconfiguration Controller (PRC) overhead time becomes much more significant.

A MATLAB code is developed satisfying the constraints mentioned earlier. The algorithm main aim is finding which blocks to be merged together in each chain in order to obtain the minimum power consumption and switching time. The procedures illustrated in Figure 1 are taken:

1) Calculate the utilized area of all blocks in the LTE chain that could be merged together in terms of LUTs. Iterations are done on the LTE chain specifically since it has the largest number of blocks.
2) Compare the weighted sum of each block in the LTE chain with the weighted sum of 3G blocks, then choose the blocks that will be merged together in each chain based on two aspects: the difference in the area must be very small; and the area of the partition should be nearly multiples of the minimum RF area (400 LUTs or 10 BRAMs or 10 DSPs).
3) Exclude the merged LTE blocks and repeat the operation on Wi-Fi, 2G, and finally the Bluetooth.
4) Merge the remaining LTE blocks together.

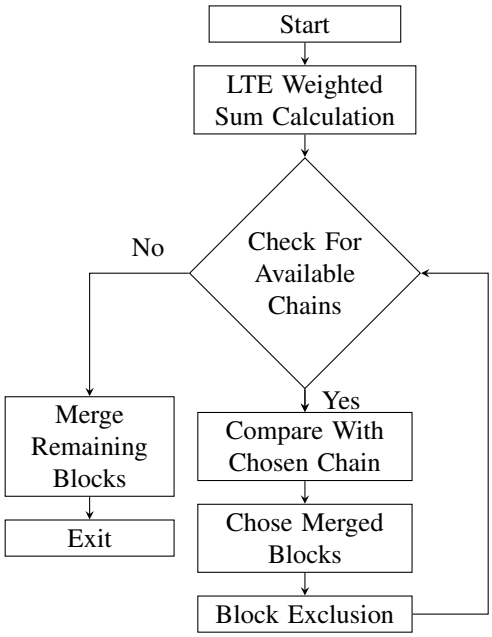

Fig. 1: Partitioning algorithm flow chart

Four approaches are deployed based on the results obtained by the MATLAB algorithm. The chains are portioned according to the following criteria:

- **Approach 1:**
  The simplest approach mentioned in [11], divides the chain into two partitions: one for the transmitter and the other for the receiver. The area of each partition is selected based on the size of the largest chain (LTE). Although this algorithm is the best fit for the LTE chain, the switching time of small chains such as 2G and Bluetooth increases due to the wasted allocated area which increases the bitstream file size.
- **Approach 2:**
  Another alternative approach suggests dividing each chain into many blocks instead of one partition to decrease the wasted area. The approach advises using five partitions for transmitters and other five for the receivers. The transmitter blocks of each chain are distributed on four partitions. The SC-FDMA is left in a fifth partition alone to reduce the area and power consumption of other chains. Similar partitions are applied at the receiver side. The advantage of this approach is reducing the area utilization of each chain. However, since Xilinx flow only supports serial configuration, the switching time increased

due to the large number of partitions. The PRC overhead becomes much more significant in such case.

- **Approach 3:**
  In order overcome the increase of switching time, a third approach is adopted advising to divide the transmitters of all chins on two partitions and leave the SC-FDMA in a fourth partition alone. This results in overall eight partitions; four for the transmitter and four for the receiver. Although this lead to decrease the switching time with reasonable area utilization, it's not offering the optimum for switching time.
- **Approach 4:**
  The final approach is deployed to solve the issues appearing in the former approaches.

The final approach proposed dividing the LTE transmitter and receiver each into three sub-blocks. The transmitters and receivers in all chains except the LTE are considered as two large non-dividable blocks while using the algorithm in order to minimize the overhead of the PRC as much as possible. As shown in Figure 2, the whole 2G and Bluetooth transmitters are nominated to be merged with LTE CRC, segmentation, and encoder. Meanwhile, the Wi-Fi and 3G transmitters shall be merged with the LTE rate matching, CBC, scrambler, and mapper. The rest is left in the third partition. At the receiver side, the 2G and Bluetooth are merged with the rate dematching. The 3G and Wi-Fi are nominated to be merged with LTE decoder, desegmentation, and de-CRC. The rest are suggested to occupy the third partition.

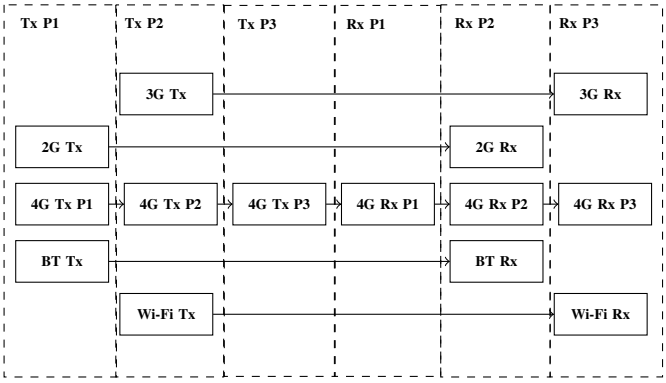

Fig. 2: Multi-partition approach block diagram

A buffer is used to replace the chain block in case of no operation. As shown in Figure 1, the LTE block in third partition at the transmitter side is replaced by a buffer in case of operating any other chain.

Figure 3 shows the floorplaning of the 6 partitions on the FPGA. Placement of all partitions is done in such shape in order to comply the placer rules and easily route the design.

In order to maintain the DPR flow and switch between the blocks shown in Figure 2, dynamic routing algorithm has been deployed. Due to the difference between the I/O ports of the chosen block of each chain to accommodate the RP, all the I/O pins has been reserved in the RTL and switching between them is performed using multiplexers. In order to pass the place and routing rules, a set of ports are chosen to share the I/O pins.

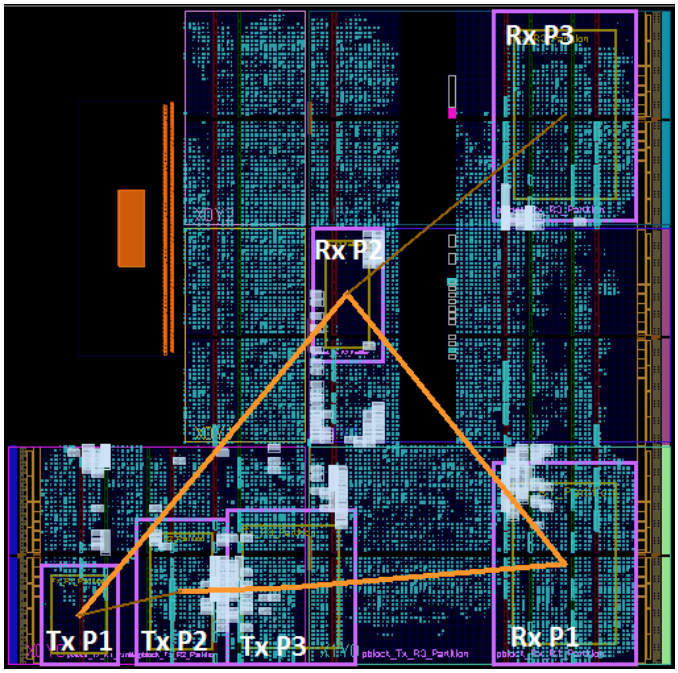

Fig. 3: Multi partition approach floorplan

Theoretical switching time calculations are performed using the following equation:

$$T = \frac{Partial\ Bit\ File\ Size\ In\ Bits}{Bus\ Width \times Max\ Clock\ Frequency} \quad (1)$$

Where the ICAP clock frequency is 100 MHz, and the data bus width is 32-bits. The sizes of the bit stream files used in the calculations are: 1201,1248,1785,2212, and 3810 Kbits for Bluetooth, 2G, 3G, Wi-Fi, and LTE transmitters respectively. The receivers bit stream files are of size: 2159, 2946, 2951, 3164, and 7134 Kbits.

Table I compares the theoretical calculated switching time with the measured actual time for all transceiver chains. In addition to the PRC overhead, placement and routing constraints has lead to increase the actual switching time.

TABLE I: Switching time

Standard	Theoretical Time (ms)	Actual Time (ms)
Bluetooth	1.05	1.29
2G	1.17	1.29
3G	1.48	1.83
Wi-Fi	1.68	1.83
LTE	3.42	4.95

Figure 4, shows a comparison between the switching time of different partitioning approaches suggested by the MATLAB algorithm.

The reasons behind the large the switching time in case of LTE are:

1) Configuring 6 partitions serially rather than 2 accumulates the configuration time of each partition while calculating the total time.

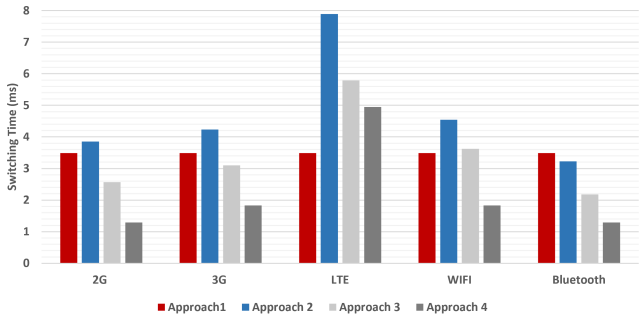

Fig. 4: Switching time across different partitioning approaches (ms)

2) Increasing the number of partitions makes the PRC overhead significant.

IV. Simulation Results

In order to evaluate the effectiveness of the purposed technique, a comparison is performed between the case of no DPR where all systems are statically implemented on the FPGA and multi partition approach with respect to power and area. Same equation used in [11] is used to express the utilized area of each approach in terms of LUTs.

The multi partition approach decreases the utilized area of the 2G and Bluetooth by 70.52%, the 3G and Wi-Fi by 53.36% compared to the case of no DPR as shown in Figure 5. Meanwhile, the 4G area increased by 12.65%, since FPGA resource distribution leads to selecting unwanted resources in all partitions.

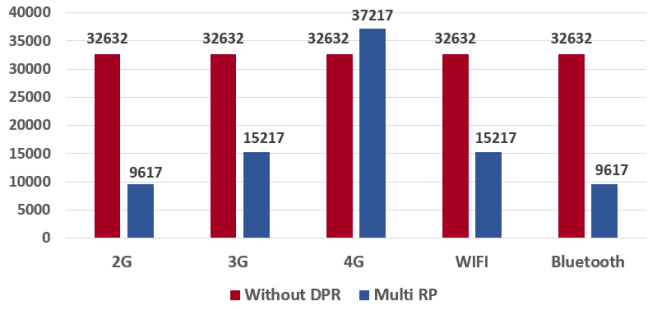

Fig. 5: Area utilization (LUTs)

Estimate power calculations are evaluated using Xilinx Vivado power analyzer. Calculations has been deployed by generating the Switching Activity Interchange Format (SAIF) on every partition in each chain. Routing overhead is taken into consideration while calculating the dynamic power.

Figure 6 shows that the new approach decreases the power consumption for 2G and Bluetooth by 98.58%, 3G and Wi-Fi by 80.59%, and LTE by 50.81% compared to the case of no DPR. The PRC power is added on each partition in case of DPR.

V. Conclusion And Future Work

The multi partition approach proved its ability to decrease the utilized area and power consumption of 2G and Bluetooth chains by 70.52% and 98.43% with respect to no DPR. The 3G and Wi-Fi area and power decreased by 53.36% and 79.69%. The area of the LTE increased by 12.65% but its power decreased by 50.09%. Data link and MAC layers implementation is future target to achieve system completeness.

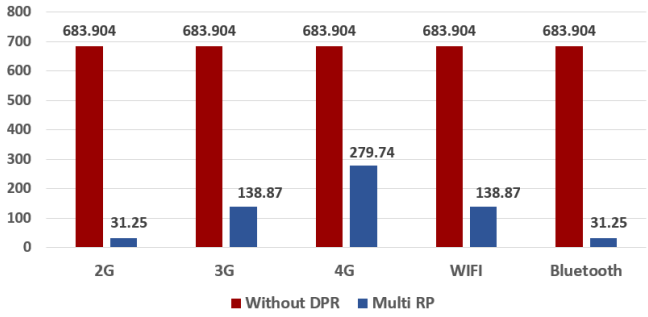

Fig. 6: Average power (mW)

VI. Acknowledgment

This work was partially funded by Zewail City of Science and Technology, AUC, Cairo University, NTRA, ITIDA, SRC, ASRT, the STDF, Intel, MCIT, NSERC.

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