Design Trade-offs for Neural Stimulators optimization

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***Abstract*—Recently, electrical stimulation has been widely used for biomedical applications, such as cardiac pacemaker, cochlear implant, muscle exercising, vision restoration, and seizure suppression. This paper presents two compact and power-efficient optimized neural stimulators for seizure suppression. These neural stimulators compromise between various design trade-offs such as adaptability with the load variations, multi-waveform generation for different seizures suppression, power efficiency, and linearity issues. The first design is an adaptable closed-loop current stimulator with a bipolar electrode, while the other design is a multi-waveform open-loop current stimulator with a unipolar electrode. Finally, the first design optimizes the power consumption to 429.68 µW and occupies 0.11 mm^2. However, the second design achieves a high-power efficiency equals 96.47 % and occupies 0.015 mm^2. Both stimulators are implemented using UMC 0.13 µm CMOS technology.**

***Index Terms*—neural stimulator, current stimulator, seizure suppression, adaptable stimulator, multi-waveform generation, exponential stimulator.**

I. Introduction

Nowadays, electrical stimulation attracts a lot of researchers, since it provides a safe treatment option for people with neurological conditions such as Parkinson's disease and Epilepsy [1], [2]. Typically, an implantable neural recording and stimulation system-on-chip (SoC) consists of three main blocks as follows: 1) a detector for neural recording, 2) a signal processor for detection and prediction, and 3) a stimulator to stimulate neurons with the proper current waveform [3]. The basic stimulator circuit consists of a digital-to-analog converter (DAC) and an output driver for generating the stimulus current.

In current-mode stimulation (CMS), the DAC output is converted into a stimulus current via a voltage-to-current converter (V/I). The V/I circuit requires a high output impedance, to resist any variations in the load impedance [4]. Moreover, the amount of charge supplied per stimulus is easily manipulated. Since the injected charge (Q) in tissue is expressed as follows:

$$Q = I \times T \quad (1)$$

Where I is the current amplitude which lasts for a period T. Moreover, controlling the injected charge amount with linear steps makes the neural stimulation safer. However, the degradation of the power efficiency is the major drawback of the CMS [4]. The stimulus current waveform can be either monophasic or biphasic [5], [6]. The monophasic is a unidirectional pulse that can be either positive or negative while the biphasic is a bidirectional pulse. This biphasic pulse is formed of an anodic pulse followed by a cathodic pulse with definite intervals of time. Based on the time intervals, the stimulation pulses can be either charge balanced [7] or charge imbalanced [5].

This paper aims to design an on-chip electrical stimulator that compromises between the output linearity and the power efficiency while maintaining the minimum power consumption. Moreover, two different design approaches are presented. The first design is an adaptable high-voltage stimulator with wide load impedance variations using standard CMOS technology and an updated version of Pelliconi charge pump to reduce the implementation area. However, the second design is a low-power multi-waveform current stimulator that multiplexes between the most common waveforms (rising exponential, falling exponential, and rectangular) while achieving a high-power efficiency.

The rest of the paper is organized as follows. Design and analysis for both stimulator designs are discussed in Section II, while the simulation results as well as the circuit layout are presented in Section III. Finally, a conclusion is drawn in Section IV.

II. Neural Stimulator Architectures

A. Adaptable High-Voltage Current Stimulator

The proposed stimulator design adapts the supply voltage (V_{DD}) based on the load impedance variations. Fig. 1 portrays the proposed closed-loop stimulator that adopts an H-bridge circuit topology similar to [8], [9], [10]. This adaptable stimulator uses a current controller (Anodic/Cathodic) to generate the control signals for a digitally controlled oscillator (DCO). Based on the DCO output frequency, the supply voltage for both the anodic and cathodic high-voltage output driver varies to adapt with the electrode impedance variations. When the electrode impedance increases, the output current decrease compared to a reference value. Therefore, the current controller enables DCO to increase the output frequency of the proposed charge pump circuit.

The charge pump circuit is used to step-up the input voltage to generate higher supply voltages. This enables the stimulator

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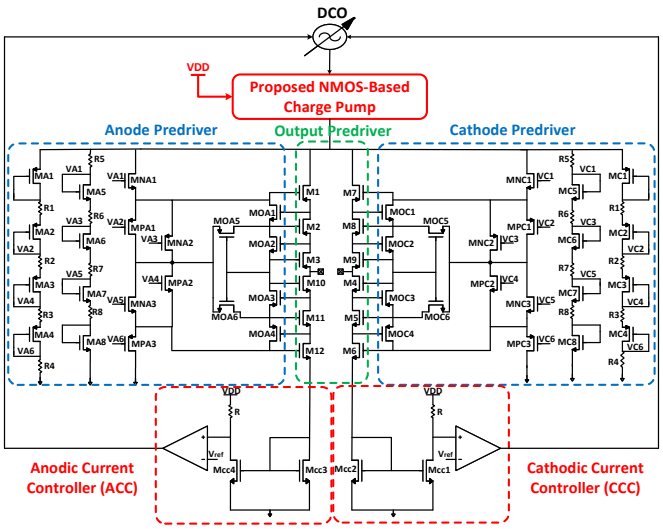


Fig. 1. Proposed Adaptable High-Voltage Current Stimulator

to cope with the load impedance variations while maintaining a constant output current. Fig. 2 (a) shows a Pelliconi charge pump [11], [12]that is implemented using NMOS and PMOS switches utilizing two non-overlapping clock signals (CLK and CLKB). Moreover, Pelliconi charge pump achieves a high-power efficiency, but it requires a large layout area to eliminate the source-body effect. Hence, a modified version of Pellconi charge pump is proposed in Fig. 2 (b), where the PMOS devices are replaced by diode-connected NMOS transistors which have less threshold voltage (V_T) to achieve a better efficiency [13].

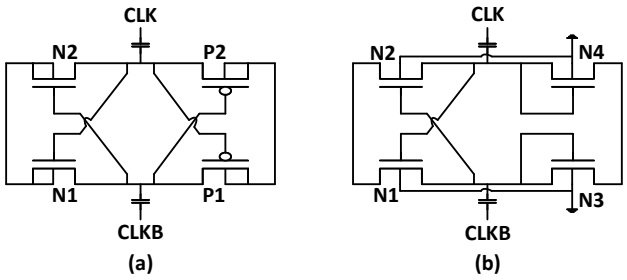


Fig. 2. (a) One Stage Pelliconi Charge Pump (b) Proposed NMOS-Based Charge Pump

The charge pump control circuit consists of two main parts: the current controller and DCO circuit. The current controller is highlighted in Fig. 1 by a red box consisting of a current mirror and simple I/V converter circuit with a low-power comparator [14]. The DCO circuit varies frequency based on the output of the current controller. Correspondingly, the charge pump efficiency varies with the load impedance variations from 44% to 67%.

B. A Low-Power Multi-Waveform Current Stimulator

This low-power current stimulator generates different waveforms (i.e., rising exponential, falling exponential, and rectangular) for different seizures suppression with emphasis on achieving a high-power efficiency. The proposed stimulator, shown in Fig. 3, operates in the subthreshold region to achieve high-power efficiency with low-power consumption. A new switching scheme technique is proposed between rising and falling ramp generators to reduce area, hence decrease power consumption. Moreover, the stimulator circuit utilizes a 4-bit binary weighted DAC to control the output current amplitude with gain boosting to increase the output resistance [15].

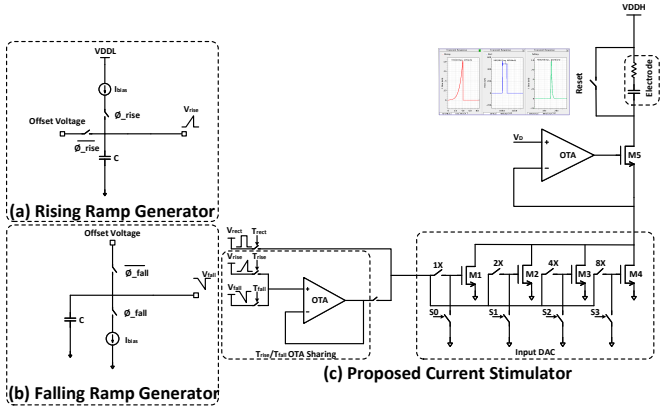


Fig. 3. Proposed Low-Power Multi-Waveform Current Stimulator

Starting from the I-V characteristics of the NMOS transistor operating in the subthreshold domain where $V_{GS} < V_T$, the output exponential stimulus current is achieved through the following equation [16]:

$$I_{DS} = I_{Do}\frac{W}{L}e^{\left(\frac{V_G}{\eta V_T}\right)} \tag{2}$$

Where I_{Do} is a technology parameter, η is a slope factor approximately equals to unity, V_T is the threshold voltage of NMOS transistor, V_G is the gate voltage, and $\frac{W}{L}$ is the aspect ratio of the transistor. Moreover, the rising exponential waveform is produced by applying the rising ramp voltage to the gate of an NMOS transistor biased in the subthreshold region. The achieved rising exponential current is more efficient than other design in [17].

Based on the control signals of the transistors (M1, M2, M3, and M4): the stimulator output current amplitude varies. The following equations explain the different waveforms generation as follows [15]:

$$I_{stim} = I_{Do}[M1 + 2M2 + 4M3 + 8M4]\frac{W}{L}e^{\frac{V_{rise}}{\eta V_T}} \times [u(t) - u(t - T_{rise})] \tag{3}$$

$$I_{stim} = I_{Do}[M1 + 2M2 + 4M3 + 8M4]\frac{W}{L}e^{\frac{V_{fall}}{\eta V_T}} \times [u(t) - u(t - T_{rise})] \tag{4}$$

$$I_{stim} = I_{Do}[M1 + 2M2 + 4M3 + 8M4]\frac{W}{L}e^{\frac{V_{rect}}{\eta V_T}} \times [u(t) - u(t - T_{rect})] \quad (5)$$

Where T_{rise}, T_{fall}, and T_{rect} are the time duration of the rising, falling, and rectangular stimulation current waveforms, respectively.

For a rising ramp generator, shown in Fig. 3 (a), a simple current integrator is designed with buffered single ended OTA to maintain a stable output voltage during the required cycle duration that is given by the following equation:

$$V_{rise} = V_{offset} + \frac{I_{bias}}{C}t \quad (6)$$

Where V_{rise} is the rising ramp voltage, V_{offset} is the offset voltage, I_{bias} is the biasing current, and C is the charging capacitor. The circuit mechanism works as follows: first, Ø_rise is high so the biasing current will charge the capacitor at time t. Then, Ø_rise is low. Hence, the capacitor will have an offset voltage till next cycle. Similarly, the falling ramp generator, shown in Fig. 3 (b), follows the same circuit mechanism as the rising ramp generator where Ø_fall is low, the capacitor is floating and has an offset voltage. Then, Ø_fall turns high, so the capacitor discharges where the output voltage of the falling ramp voltage (V_{fall}) is expressed as follows:

$$V_{fall} = V_{fall} - \frac{I_{bias}}{C}t \quad (7)$$

Finally, the offset voltage is maintained to be lower than the threshold voltage to ensure that the transistors are operating in the subthreshold region. Also, the charging/discharging duration depends on the required pulse width of the output current.

As shown in Fig. 3 (c), the proposed stimulator shares the same OTA circuit for both the rising ramp and the falling ramp to reduce the static power hence increase the circuit efficiency. Moreover, the output stage is formed by V/I converter biased in the subthreshold region as described before. In addition, the designed OTA is based on a simple current-based single-ended topology. The proposed stimulator reduces the power consumption through the discontinuous switching between the multiple input waveforms.

III. CIRCUIT LAYOUT AND POST-LAYOUT SIMULATION RESULTS

In this section, both neural stimulators are implemented and simulated using UMC 0.13 µm CMOS technology. The circuit layout, shown in Fig. 4, shows the proposed neural stimulators with highlighting on the main design blocks. Here are brief highlights of the proposed neural stimulator designs:

- Both designs are optimized on gate level through setting a more accurate aspect ratio to achieve a lower power consumption.
- For the adaptable high-voltage current stimulator, a new charge pump circuit is proposed for higher power efficiency with less implementation area based on NMOS switches only. Besides, the proposed circuit layout doesn't require a triple-well technology like other designs introduced in [8], [9].
- For the low-power multi-waveform current stimulator, a new architecture is proposed based on OTA sharing between multiple inputs (rising/falling ramps) for reducing the power consumption as well as the layout area.

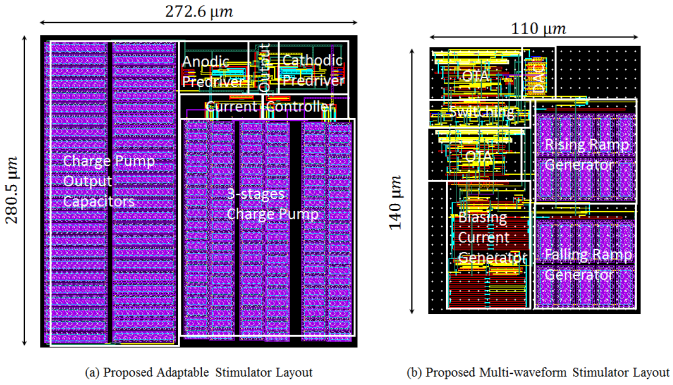


Fig. 4. Chip Layout for Both Stimulators

In Fig. 5, the biphasic output current of the adaptable high-voltage current stimulator versus the electrode impedance is shown. Based on the DCO output frequency, the adaptable stimulator copes with the electrode impedance variations from 24 KΩ till 150 KΩ while the output current varies at the worst case by ±13% with ±10% supply variations and the temperature varies from -40°C till 85 °C.

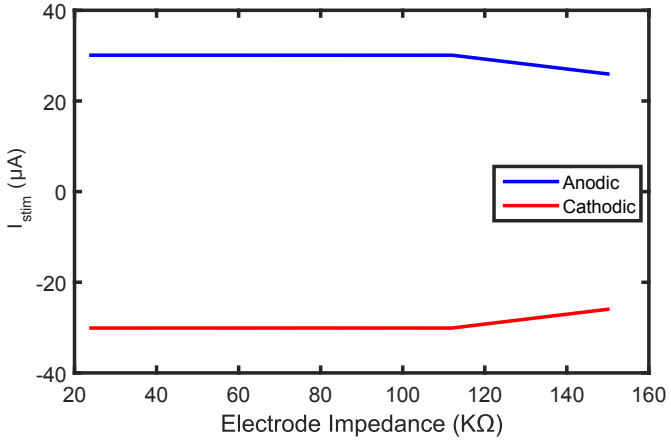


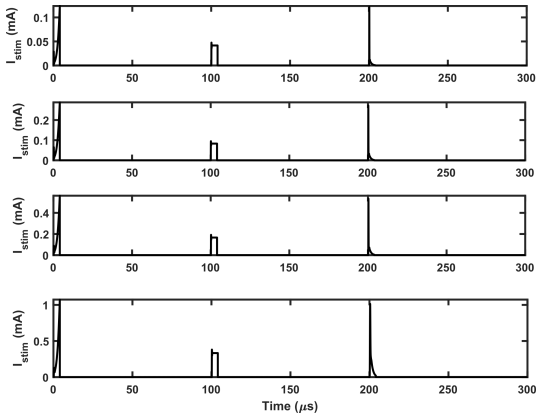
Fig. 5. Output Stimulation Current Versus Electrode Impedance Variations of Proposed Adaptable Stimulator

In Fig. 6 (a), the output current of the proposed low-power multi-waveform current stimulator is shown with different amplitudes. Besides, the output current amplitude varies from 0.001 mA till 1mA with an input pulse frequency equals 10 KHz. Moreover, the stimulator power efficiency (PE) of the proposed stimulator equals to 96.47 % where it is calculated based on the classical law of efficiency for a single current channel given by the following equation [18]:

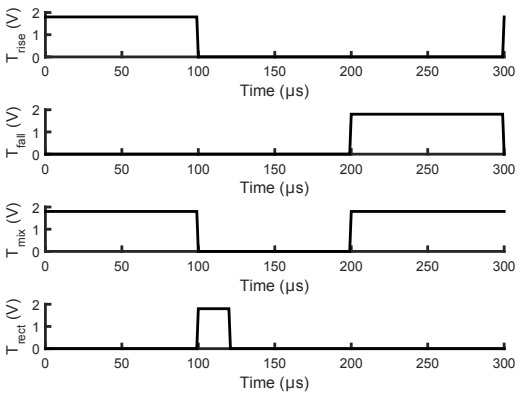
TABLE I
PERFORMANCE SUMMARY BETWEEN THIS WORK AND DIFFERENT NEURAL STIMULATORS

	[8]	[9]	[10]	[15]	Adaptable	Multi-Wave
Technology (µm)	0.35	0.35	0.065	0.18	0.13	0.13
Area (mm^2)	0.7	0.3	2	N/A	0.11	0.015
Supply Voltage (V)	3.3V	3.3V	2.5	1.8/3.3	3.3	1.8/3.3
Current Range (mA)	0.04	0.03	0.05-2	0-1	0.03	0.001-1
Stimulation Type	Biphasic	Biphasic	Biphasic	Monophasic	Biphasic	Monophasic
Load Impedance	(10-300)KΩ + 1µF	(24-200)KΩ	20KΩ + 0.02µF	1KΩ + 1µF	(24-150)KΩ + 0.2µF	1KΩ + 1µF
Static Power (mW)	$\leq$ 1.4	$\leq$ 0.56	0.3	0.0232	$\leq$ 0.43	0.0124
Efficiency (%)	N/A	N/A	N/A	94.7	N/A	96.47

$$PE = \frac{I_{stim} \times V_{load}}{P_{static} + I_{stim} \times V_{DDH}} \quad (8)$$



(a) Output Stimulation Current Waveforms



(b) Control Signals Waveforms

Fig. 6. Transient Simulation Waveforms of Proposed Multi-Waveform Stimulator

In Fig. 6 (b), the control signals (rise ramp, rectangular, fall ramp, and shared OTA control) for the proposed low-power multi-waveform current stimulator are shown. The output changes its rate every 100 µsec.

A Monte-Carlo analysis, shown in Fig. 7, is performed over 1000 samples on biasing current source to ensure the proper operation of the multi-waveform stimulator. The mean value (μ) equals 477 nA, while the standard deviation (σ) corresponds to 6%. Moreover, the output current of the stimulator varies by ±15% across PVT.

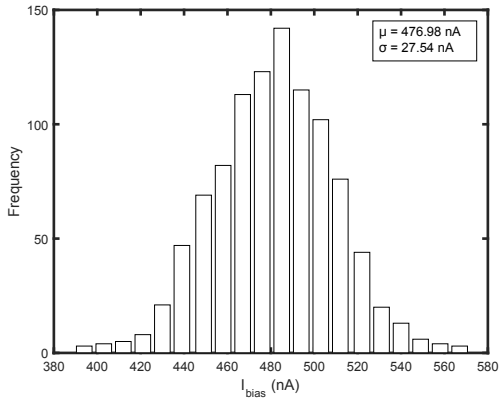


Fig. 7. Monte-Carlo Analysis for Generated I_{bias}

Finally, Table I shows a detailed comparison between this work and the recently published work presented in [9], [8], [10], and [15]. The proposed stimulator circuits provide good results compared to other work in the literature, especially for the power consumption reduction. It is obvious from Table I that the power consumption of the proposed adaptable stimulator circuit is lower than that in [8] and [9] by factors of 1.3X and 3X, respectively. Moreover, the multi-waveform stimulator reduces power consumption by 1.9X with slight PE improvement of 2%.

IV. Conclusion

In this paper, two compact designs for neural stimulation with a high-power efficiency are presented. Both stimulators address the different design trade-offs (i.e., linearity, power efficiency, electrode polarity, load adaptability, and multi-waveform). A biphasic adaptable high-voltage neural stimulator that operates at 3.3V and occupies 0.11 mm^2 is introduced as well as a unipolar high-efficiency multi-waveform that operates at 1.8/3.3V and occupies 0.015 mm^2.

Acknowledgment

This work was supported by the Egyptian Information Technology Industry Development Agency (ITIDA) under ITAC Program CFP # 96.

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