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ORIGINAL RESEARCH PAPER

A 0.002-mm^2 8-bit 1-MS/s low-power time-based DAC (T-DAC)

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Abstract

Digital-to-analogue converters (DACs) are essential blocks for interfacing the digital environment with the real world. A novel architecture, using a digital-to-time converter (DTC) and a time-to-voltage converter (TVC), is employed to form a low-power time-based DAC (T-DAC) that fits low-power low-speed applications. This novel conversion mixes the digital input code into a digital pulse width modulated (D-PWM) signal through the DTC circuit, then converts this D-PWM signal into an analogue voltage through the TVC circuit. This new T-DAC is not only an energy-efficient design but also an area-efficient implementation. Power optimization is achieved by controlling the supply voltage of the TVC circuit with a discontinuous waveform using a low bias current. Moreover, the implementation area is optimized by proposing a new DAC architecture with a coarse-fine DTC circuit. Post-layout simulations of the proposed T-DAC is conducted using industrial hardware-calibrated 0.13 μm. Complementary metal oxide semiconductor technology with a 1 V supply voltage, 1 MS/s conversion rate, and 0.9 μW power dissipation.

1 | INTRODUCTION

Nowadays, electrical stimulation is widely used for biomedical applications (i.e. seizure suppression, cardiac pacemaker, and cochlear implant). Electrical stimulation has the following advantages over treatments using drugs or surgery, (1) less destructive, (2) recoverable, and (3) flexible [1]. The basic stimulator circuit consists of a digital-to-analogue converter (DAC) and an output driver for the stimulus current. The DAC design has to show a good linearity with a moderate resolution (i.e. 4–8 bits) to control the amplitude of the output stimulus current [1]. Moreover, the DAC power consumption is required to be as low as possible to avoid excess heat that damages the brain tissues [1].

Complementary metal oxide semiconductor (CMOS) technology continues scaling down, and the analogue design does not take the full privileges of this scaling. The reason is that the threshold voltage, as well as the noise floor, do not decrease at the same pace as the supply voltage. This makes the design of cascaded analogue blocks more difficult. On the other hand, the digital design enjoys better switching characteristics of the transistor improving the speed as well as the power consumption of the whole design [2]. Targeting battery-powered biomedical and portable devices require low-power interface modules between the real world and the digital signal processors. These interface modules are either analogue-to-digital converters (ADCs) or DACs.

For DAC design, there are many implementation techniques such as resistor-string DAC [3], capacitor-resistor (C-R) DAC [4], charge redistribution DAC [5], cyclic DAC [6, 7], charge scaling with split-capacitor array DAC [8, 9], segmented DAC [10], current steering DAC [11], dual-capacitor array DAC [12], charge-sharing DAC [13, 14], sigma-delta DAC [15], and pipelined DAC [16, 17]. However, resistor-string DACs consume high power and occupy a large area. Meanwhile, the other DAC designs with charge control are power efficient, but they occupy large area and suffer from poor capacitors quality [18]. Moreover, current steering DACs have good linearity but consume high-power. Therefore, there is a rising demand for trade-off power consumption, area, and linearity for energy-efficient applications.

In the literature [3–17], several DAC designs have been presented to achieve low-power consumption in a small implementation area. Moreover, these designs are based on direct conversion from the digital domain to the analogue domain. Also, it is hard to design a low-power direct conversion DAC with an acceptable resolution due to several design challenges such as mismatch and offset errors. Here, a time-based DAC (T-DAC) is proposed. This T-DAC introduces

an indirect conversion technique that is used for optimizing both power consumption and implementation area with mismatch immunity. Furthermore, the T-DAC encodes the digital input word in terms of a delayed pulse through the digital-to-time converter (DTC) circuit, while this delayed pulse is converted into an analogue voltage through the time-to-voltage converter (TVC) circuit. The proposed T-DAC design is dominated by digital circuits, where it has several advantages such as (1) eliminating the need for a string of resistors or a bank of capacitors, (2) reducing the effect of the mismatch between the design components, (3) reducing the implementation area, (4) operating at low voltages, (5) consuming less power with technology scaling, and (6) scaling up to higher resolution regularly. The rest of the study is organized as follows. In Section 2, the proposed T-DAC architecture is described as well as the circuit implementation. The circuit layout and post-layout simulation results are provided in Section 3. Finally, a conclusion is drawn in Section 4.

2 | PROPOSED T-DAC ARCHITECTURE AND CIRCUIT IMPLEMENTATION

The proposed T-DAC, shown in Figure 1, converts the digital codes into a time delay representation through the DTC circuit during the first half period of the clock signal (CLK). Then, the output signal of the DTC circuit entitled D-PWM is converted into an analogue signal through the TVC circuit. The main idea is to code the digital input bits into a time delay difference between the input clock signal, and the output D-PWM signal.

2.1 | Digital-to-time converter

Figure 2 portrays the block diagram of the proposed coarse-fine DTC circuit. The proposed circuit processes the digital input word through two stages where the most significant bits (MSBs) (S4–S7) are processed by a 4-bit coarse stage. Then, the least significant bits (LSBs) (S0–S3) are processed by a 4-bit fine stage. The circuit works as follows: first, the input CLK is fed to an n-bit coarse delay line (CDL) to calculate the coarse resolution (T_C). Following that, the output delay that corresponds to the MSBs is selected through the first multiplexer (MUX_1). Second, the output signal from MUX_1 is fed to an m-bit delay line (FDL) to calculate the fine resolution (T_F). Then, the output delay that corresponds to LSBs is selected through the second multiplexer (MUX_2). Finally, the delayed pulse (MUX_2) is fed to an AND-gate with the inverted CLK (CLKB) to generate the output signal D-PWM.

The time resolutions for both CDL and FDL are calculated as follows: $T_C = \frac{T_{max}}{2^{n-1}}$ and $T_F = \frac{T_C}{2^m}$, where n and m are the control bits of both CDL and FDL, respectively, and T_{max} is the maximum output delay from the proposed coarse-fine DTC circuit. Moreover, T_C is divided by 2^m not $2^m - 1$ to ensure that the FDL returns to zero level with new input signal without overlapping with the selection process of the delayed input pulses.

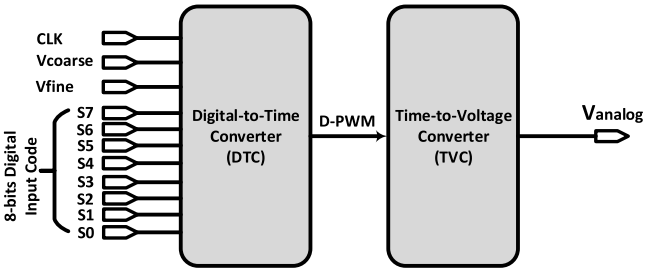

FIGURE 1 Proposed T-DAC block diagram. T-DAC, time-based digital-to-analogue converter

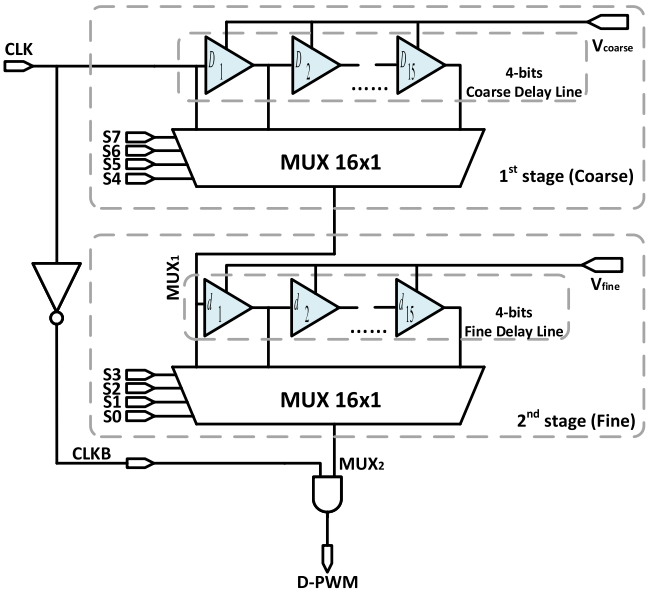

FIGURE 2 Proposed DTC circuit diagram. DTC, digital-to-time converter

To elaborate more on how the DTC works, Figure 3 shows an example of the D-PWM signal that corresponds to the digital input code 0000 0111. During the conversion process of this illustrated example, the MSBs choose the CLK signal without any delay from the coarse stage and LSBs to choose T_{F7} that is located in the middle between CLK and T_{C1}. Furthermore, MUX1 represents the CLK signal, that passes without any delay from the coarse section, versus fine signals in the same case. This shows the time difference that is calculated by bit masking between T_{F7} and CLKB. Finally, D-PWM signal is the midpoint between CLK and T_{C1}. On the other hand, the resolution is dominated by the fine step size that is limited by the accuracy of the fine delay cells. Moreover, common advanced techniques can be utilized to achieve a high-resolution that corresponds to a step size in the range of picoseconds at the expense of power consumption such as using the Vernier delay line that controls the delay using the difference between the two cells [19].

For generating a controllable delay for both CDL and FDL, a generic delay cell is implemented as shown in Figure 4. A basic current starved CMOS inverter is used to form a controllable delay cell, where the rising edge of the delay output clock is controlled through transistor P1, and the falling

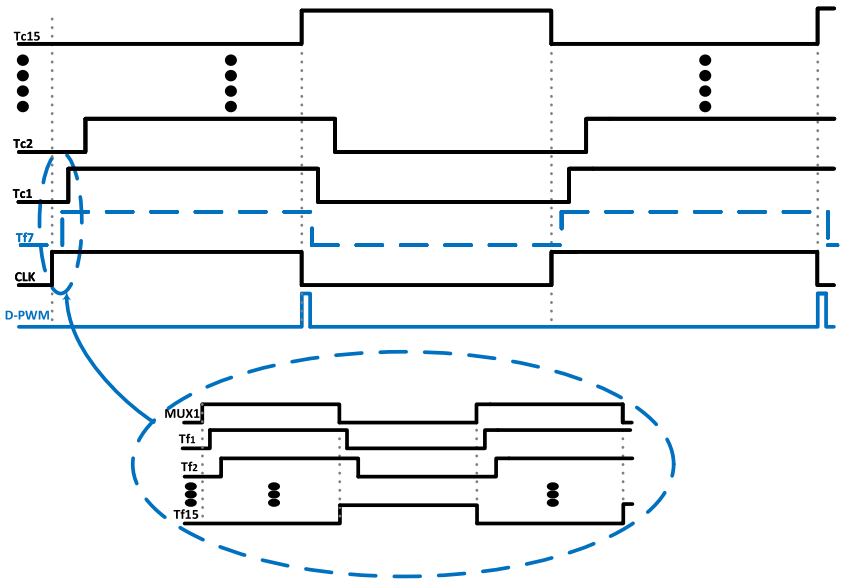

FIGURE 3 Timing diagram for DTC circuit. DTC, digital-to-time converter

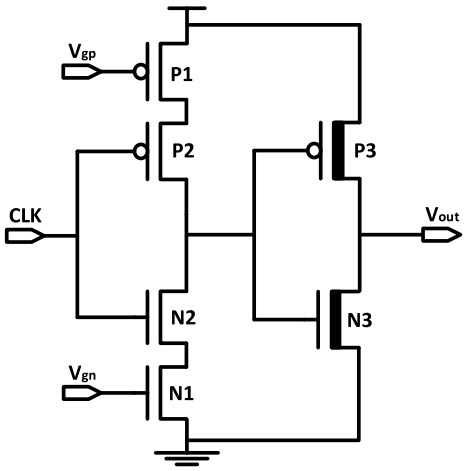

FIGURE 4 Controllable delay cell circuit schematic

edge is controlled through transistor N1. Also, the basic CMOS inverter that consists of two transistors P2 and N2 is followed by another CMOS inverter that is implemented by two high V_t transistors P3 and N3. Varying the output delay of the current starved inverter results in increasing the input rise time and fall time of the second inverter. This increase leads to a high short circuit power (P_{sc}) in the second inverter. This P_{sc} is reduced by using high V_t transistors [20]. The tuning process is performed by using two complementary control signals V_{gn} and V_{gp}. This means that each delay line requires 16 tuning voltages because the loading effect of each delay cell depends on the cell location. However, it is noticed that the loading of all the middle delay cells is the same. Therefore, the number of tuning voltages is optimized to be only three tuning voltages per each delay line. Area/power optimization of the proposed coarse-fine DTC circuit is achieved by estimating the number of used transistors as well as the load capacitance (C_L) which affects the dynamic power (P_{Dyn}) through the following equations:

$$Tr\ Count = \left(\left(\sum_{i=0}^{n-1} 2^i\right) * 6 + 2^n * 6\right)_C + \left(\left(\sum_{j=0}^{m-1} 2^j\right) * 6 + 2^m * 6\right)_F \quad (1)$$

$$Estim\ C_L = \left(\left(\sum_{i=0}^{n-1} 2^i\right) * 4C_u + 2^n * 4C_u\right)_C + \left(\left(\sum_{j=0}^{m-1} 2^j\right) * 4C_u + 2^m * 4C_u\right)_F \quad (2)$$

where C_u is the unit capacitance per transistor that is optimized on the gate level through setting the minimum aspect ratio with a stable functionality across variations, and both n and m have to be an integer. The equations are divided into two parts coarse (C) and fine (F) where the number of used transistors (Tr Count) and C_L of both input multiplexer and delay line per each stage are estimated. However, the input multiplexers (MUX_1 and MUX_2) are implemented using the transmission gate (TG). The first equation estimates the size of the input multiplexer in terms of a 2 × 1 multiplexer, then is multiplied by the number of transistors of a 2 × 1 multiplexer. However, the second equation estimates C_L at the output node of both the input multiplexer in terms of a 2 × 1 multiplexer and the controllable delay cell. Finally, it is apparent from Figure 5 where the segmentation ratio is swept to be $n + m = 8$ that the optimum area/power utilization is achieved using equal segmentation ratio (i.e. $n = m = 4$).

2.2 | Time-to-voltage converter

The TVC circuit, shown in Figure 6, is used to convert the D-PWM signal into an analogue voltage by generating a voltage ramp with a constant slope. This slope is expressed as follows:

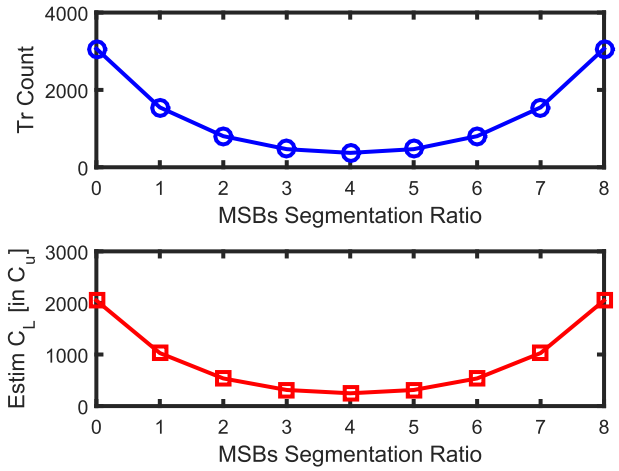

FIGURE 5 Area/power estimation versus MSB sub-array, bits. MSB, most significant bit

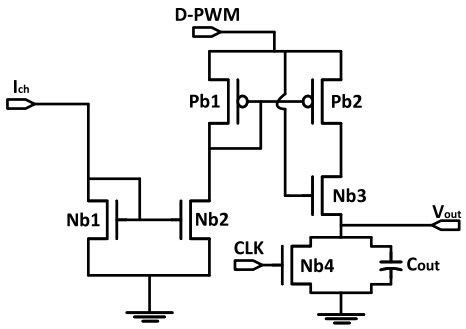

FIGURE 6 Proposed TVC circuit schematic. TVC, time-to-voltage converter

$$\frac{\Delta t}{\Delta V} = \frac{C_{out}}{I_{ch}} \tag{3}$$

where Δt is the time delay representation of the digital input code, C_{out} is the output capacitance, I_{ch} is the input charging current, and ΔV is the output analogue voltage. However, the output resistance of the implemented current mirror introduces non-linearity during the charging phase. To reduce this non-linearity, the output resistance of the current mirror transistors (Pb1 and Pb2) is increased by increasing the transistor channel length (L).

For low-power consumption, the TVC circuit is supplied through the output signal D-PWM that acts as V_{DD} limiting the maximum output full-scale voltage (V_{FS}) to be:

$$V_{FS} = V_{DD} - (V_{CS} + V_{ds}) \tag{4}$$

where V_{CS} is the compliance voltage of the charging current source, and V_{ds} is the voltage drop between the drain and the source to make the transistor Nb3 operating in the triode region. Using a discontinues supply waveform entitled D-PWM causes discharging of the output node when the D-PWM signal is low. However, the transistor (Nb3) is cascaded with the transistor Pb2 as a switch controlled by the same D-PWM signal preventing the current from discharging back from the output node. And C_{out} is connected in parallel with the transistor (Nb4) as a switch to reset it every cycle. Finally, to reduce the current mismatch of I_{ch}, L is increased relative to the transistor width (W) at fixed I_{ch} because the normalized current mismatch is inversely proportional to L [21]. Using small-signal analysis, the output resistance of the proposed TVC circuit (R_{out}) is derived as follows:

$$R_{out} = \frac{1 + \frac{r_o}{r_{ox}}}{g_m} \Big/\!\Big/ r_{oy} \approx \frac{2}{g_m} \tag{5}$$

where r_0 is the output resistance of the transistor Pb2, r_{0x} is the output resistance of the transistor Nb3, g_m is the transconductance of the transistor Nb3, and r_{0y} is the output resistance of the transistor Nb4. R_{out} is calculated and verified to be 1.6 MΩ fulfiling the circuit maximum conversion time of 1 μs. Linearizing V_{out} of the TVC circuit might be achieved by increasing the time constant of charging C_{out}. However, the time constant is increased through increasing R_{out} in order not to change Δt or C_{out}. Also, the conversion speed is dominated by the output pole given by:

$$f_{3-dB} = \frac{1}{2\pi R_{out} C_{out}} \tag{6}$$

Timing jitter represents another limitation for time-based data converters. Since, the T-DAC resolution is presented in the time domain. However, technology scaling helps in reducing the timing jitter by speeding up the switching characteristics and hence increasing the input slopes [22]. In the proposed T-DAC, the main jitter contributor is the CDL as the jitter variance ($\sigma^2_{t_{dN}}$) for an inverter is proportional to $\frac{C_L V_{DD}}{I_N^2}$. Also, the TG increases $\sigma^2_{t_{dN}}$ as TG adds more capacitance to the multiplexer implementation [23]. Moreover, the output of the DTC circuit is the difference between delayed input pulse, and CLKB to reduce the effect of the input jitter of the CLK. Finally, the simulated $\sigma^2_{t_{dN}}$ equals 71 ps that correspond to less than 10% of T_F.

3 | CHIP LAYOUT AND POST-LAYOUT SIMULATIONS

A prototype of the proposed T-DAC is implemented by using industrial hardware-calibrated 0.13 μm CMOS technology. The T-DAC layout is shown in Figure 7, where the different blocks are highlighted, and the overall area equals 0.002 mm^2. Moreover, the T-DAC operates with a 1 V supply voltage, while consuming 0.9 μW. In addition, an off-chip charging current (I_{ch}) equals 240 nA, C_{out} equals 96 fF, and T_{max} equals 240 ns. Finally, the prototype is simulated and verified using Cadence Virtuoso. In addition, both the

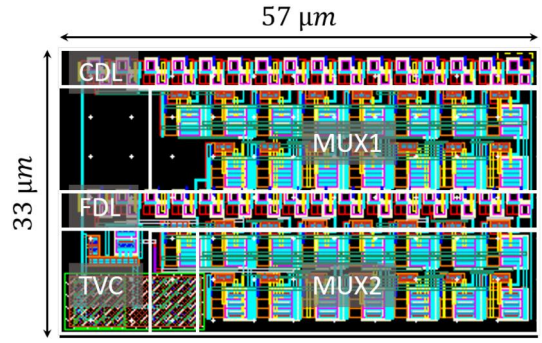

FIGURE 7 Chip layout for the proposed T-DAC architecture in 0.13 μm CMOS technology. CMOS, complementary metal oxide semiconductor; T-DAC, time-based digital-to-analogue converter

input and supply sources are modelled through the simulation setup as follows: (1) CLK where the rise and fall times equal 100 ps, (2) supply source where the supply variations equal ±10%, and (3) tuning the bias voltages with a step size of 5 mV.

In Figure 8, the output delay, and cell power consumption are simulated across different process, voltage and temperature (PVT) variations while varying the control voltage V_{gn} and V_{gp}. However, the output delay varies significantly with PVT variations, but it also supports the required delay values through the off-chip tuning voltages. To ensure that the rising and falling edges are delayed by roughly equal amounts, keeping the output pulse width from growing or shrinking relative to the input pulse width [24] is achieved by the following equation:

$$V_{gp} = V_{DD} - V_{gn} \tag{7}$$

While sweeping the control voltage V_{gn} and V_{gp}, the power consumption of the controllable delay cell is almost constant in the order of nW. However, the power consumption variation follows the same manner as the delay. Since, P_{sc} of the second inverter is still dominating the total power, the P_{Dyn} of the first current starved inverter running on a low frequency is insignificant compared to P_{sc}. On the other hand, the delay cell linearity is not one of the constraints in the proposed DTC circuit. Since, it generates a fixed delay for either CDL or FDL. Also, both delays (T_C and T_F) are marked in Figure 8(a) to show that the required delay can be obtained under any condition by varying V_{gn}. Moreover, this turnability in the delay cell implementation has many advantages as follows:

- Support generation of both delays (T_C and T_F).
- Introduce modularity on the proposed system implementation by having the same cell sizing for both CDL and FDL.
- Add immunity across PVT variations.

Figure 9 shows the output current i_{out} using Monte-Carlo simulations. The mean value (μ) of i_{out} equals 240.6 nA, and the standard deviation (σ) equals 39 nA over 1000 Monte-Carlo

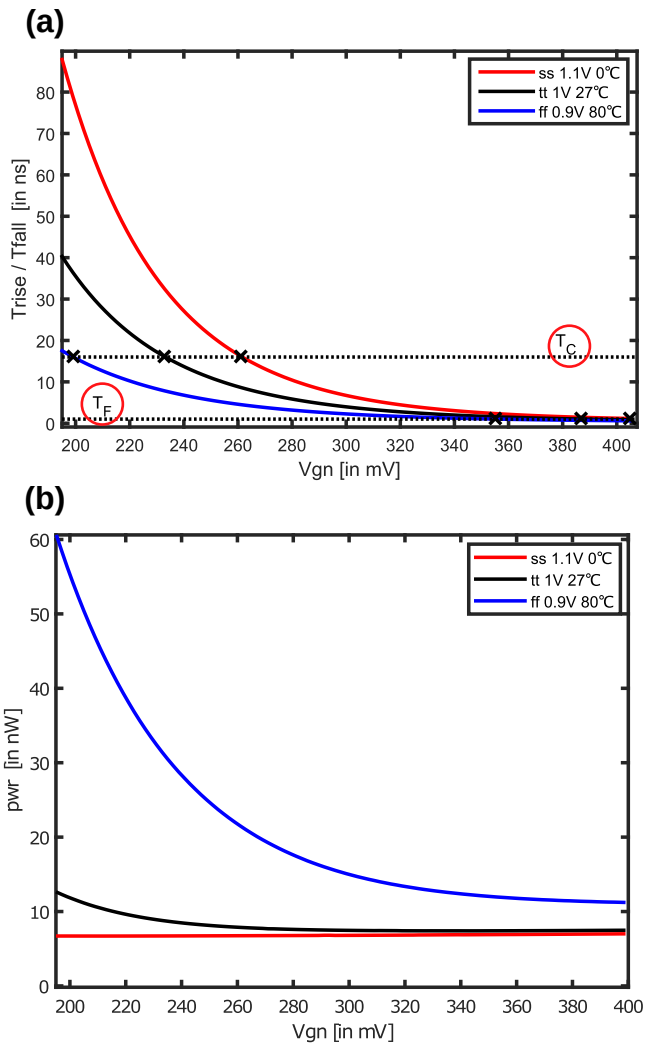

FIGURE 8 Delay cell characterisation versus V_{gn} across PVT variation: (a) rising/falling delay and (b) power consumption. PVT, process, voltage and temperature

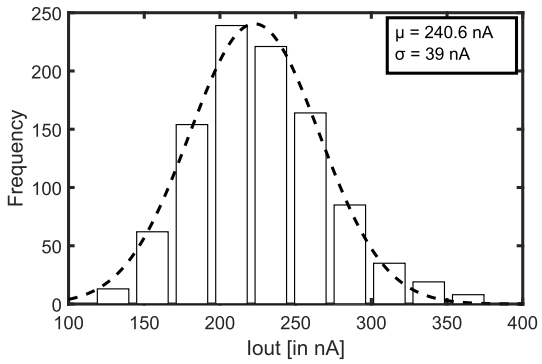

FIGURE 9 Monte-Carlo simulation of i_{out}

points. However, the output distribution with a nano-ampere current follows log-normal distribution according to [25] with a wide spread of variation (3σ). This mismatch can be calibrated with the first run by tuning the input biasing current

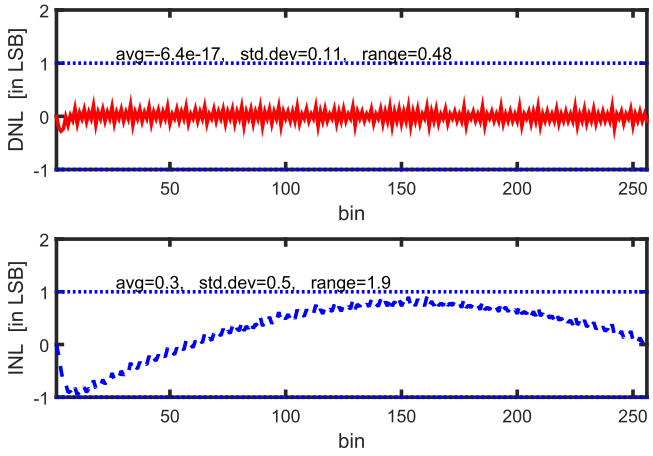

FIGURE 10 Simulated static non-linearities of 8-bit T-DAC. T-DAC, time-based digital-to-analogue converter

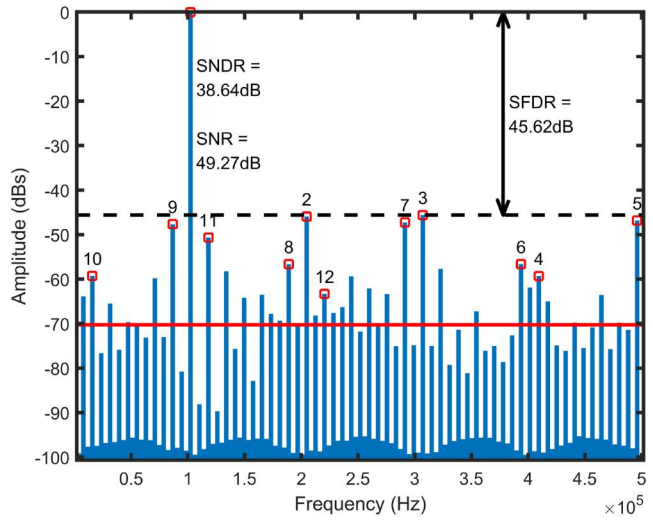

FIGURE 11 FFT of output spectrum at an input frequency = 101.56 kHz. FFT, fast Fourier transform

until the output voltage matches V_{FS} that corresponds to the maximum input code.

Figure 10 shows a static linearity test by simulating 10 samples/code while sweeping the full-scale range. The results show maximum −0.28 LSB, and −0.97 LSB for differential nonlinearity (DNL) and integral nonlinearity (INL), respectively. Moreover, the average DNL, and INL are approximately zero, and 0.3 LSB, respectively. In addition, the standard deviation of DNL, and INL is 0.11 LSB, and 0.5 LSB, respectively. Using an ideal ADC with an input sinusoidal signal of 101.56 kHz, the fast Fourier transform of the output signal of the proposed T-DAC is shown in Figure 11 where the signal-to-noise ratio, signal-to-noise and distortion ratio, and spurious-free dynamic range equal 49.27, 38.64, and 45.62 dBs, respectively.

Table 1 shows a detailed comparison between this work and other DAC architectures for low-voltage and low-power applications. This comparison shows the strength of this study compared to recently published study considering several design metrics. Compared with other low-power DACs, the proposed T-DAC exhibits lower power consumption over a capacitive DAC [28], that is implemented in 0.09 µm with supply scaling down to 0.5 V. However, the proposed T-DAC occupies less area than that in the capacitive DAC [3, 6, 26, 28], and [18] by factors of 3.25X, 189X, 11X, 300X, and 131X, respectively.

4 | CONCLUSION

Here, a low-power low-voltage CMOS T-DAC has been described. The proposed T-DAC is easily calibrated by varying the off-chip coarse-fine voltages of the delay lines, and the input bias current. This indirect conversion method optimizes both the power consumption and the layout area. Area optimization is done by implementing a coarse-fine DTC circuit where the loading effect in each delay line is compensated by three control voltages to the first cell, the

TABLE 1 A performance summary between this work and other DAC architectures

Spec	ICECS [18]	CICC [26]	TCASII [3]	NEWCAS [6]	LASCAS [27]	TVLSI [28]	IET [13]	This work
Process (µm)	0.5	1.2	0.35	0.35	0.18	0.09	0.09	0.13
V_{DD} (V)	3.3	0.9	3.3	3.3	1.8	0.5	±0.35	1
I_{Consum} (µA)	200	355	22	93	138	1.92	N/A	0.9
F_s (MS/s)	2	5	1	2	10	1.28	0.78	1
Res (bits)	8	6	10	10	12	9	8	8
Max DNL (LSB)	N/A	±0.35	±0.35	±0.75	±0.2	−0.501/0.578	−0.54/0.87	−0.28/+0.2
Max INL (LSB)	N/A	±0.46	+0.7/−0.55	±0.7	±0.3	−0.519/0.61	−0.9/0.8	−0.97/+0.93
V_{FS} (V)	2.5	0.5	2.5	3	1.18	0.5	N/A	0.6
Area (mm^2)	0.2622	0.6	0.022	0.3784	N/A	0.0065	0.0006	0.002
Power (µW)	660	319.5	72.6	306.9	248.4	0.96	N/A	0.9

Abbreviation: DAC, digital-to-analogue converter.

middle cells, and the last cell, respectively. Moreover, power optimization is done by utilizing a discontinuous supply voltage waveform for the analogue TVC circuit. A T-DAC implemented in 0.13 μm CMOS technology consumes 0.9 μW and runs on 1 MHz. In addition, the post-layout simulations show that INL and DNL are within −0.97/+0.93 and −0.28/+0.2, respectively. Moreover, the proposed architecture is advantageous in deep-submicron technology due to the technology scaling scalability. This T-DAC is well suited for biomedical applications such as neural stimulation and cardiac pacemaker. Thus, it operates at low voltage and low speed with an area efficient design while maintaining low power consumption.

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REFERENCES

1. Lin, C.-Y., Ker, M.-D.: Overview of on-chip stimulator designs for biomedical applications. J. Neurosci. Neuroeng. 1(2), 204–212 (2012)
2. Hassan, A.H., et al.: An ultra-low power voltage-to-time converter (VTC) circuit for low power and low speed applications. In: Proceedings of the IEEE international system-on-chip conference (SOCC), 178–182. Seattle (2016)
3. Perelman, Y., Ginosar, R.: A low-power inverted ladder D/a converter. IEEE Trans. Circuits Syst. II. 53(6), 497–501 (2006)
4. Youn, E., Jang, Y.: 12-bit 20M-S/s SAR ADC using C-R DAC and capacitor calibration. In: Proceedings of the 2018 international SoC design conference (ISOCC), pp. 1–2. Daegu, Korea (South) (2018)
5. Weyten, L., Audenart, S.: Two-capacitor DAC with compensative switching. Electron. Lett. 31(17), 1435–1437 (1995)
6. Kim, H., et al.: Design of a low power 10-bit cyclic D/A converter with a Johnson counter and a capacitor swapping technique. In: Proceedings of the IEEE north-east workshop on circuits and systems and TAISA sonference, pp. 1–4. Toulouse (2009)
7. Chen, P., Liu, T.-C.: Switching schemes for reducing capacitor mismatch sensitivity of quasi-passive cyclic DAC. IEEE Trans. Circuits Syst. II. 56(1), 26–30 (2009)
8. Abdelhalim, K., et al.: 64-Channel UWB wireless neural vector analyser SOC with a closed-loop phase synchrony-triggered neurostimulator. IEEE J. Solid-State Circuits. 48(10), 2494–2510 (2013)
9. Zhang, Z., et al.: A dynamic tracking algorithm based SAR ADC in bio-related applications. IEEE Access. 6, 62166–62173 (2018)
10. Saberi, M., Lotfi, R.: Segmented architecture for successive approximation analog-to-digital converters. IEEE Trans. VLSI Syst. 22(3), 593–606 (2014)
11. Park, G., Song, M.: A CMOS current-steering D/A converter with full-swing output voltage and a quaternary driver. IEEE Trans. Circuits Syst. II. 62(5), 441–445 (2015)
12. Narasimaiah, J.D., Bhat, M.S.: 14.5 fJ/conversion-step 9-bit 100-kS/s non-binary weighted dual capacitor array based area and energy efficient SAR ADC in 90 nm CMOS. IET Circuits Dev. Syst. 12(6), 671–680 (2018)
13. Narasimaiah, J.D., et al.: 11.39 fJ/conversion-step 780 kS/s 8 bit switched capacitor-based area and energy-efficient successive approximation register ADC in 90 nm complementary metal–oxide–semiconductor. IET Circuits Dev. Syst. 12(3), 249–255 (2018)
14. Chen, B., et al.: Precision passive-charge-sharing SAR ADC: analysis, design, and measurement results. IEEE J. Solid-State Circuits. 53(5), 1481–1492 (2018)
15. Kiss, P., et al.: Stable high-order delta-sigma digital-to-analog converters. IEEE Trans. Circuits Syst. I. 51(1), 200–205 (2004)
16. Wang, F.-J., et al.: A quasi-passive CMOS pipeline D/A converter. IEEE J. Solid-State Circuits. 24(6), 1752–1755 (1989)
17. Payandehnia, P., et al.: Digital correction of DAC nonlinearity in multi-bit feedback A/D converters: invited tutorial. In: Proceedings of the IEEE custom integrated circuits conference (CICC), pp. 1–8. Boston (2020)
18. Maloberti, F., et al.: Power consumption optimization of 8 bit, 2 MHz voltage scaling subranging CMOS 0.5-μm DAC, In: Proceedings of the international conference on electronics, circuits, and systems, pp. 1162–1165. Rodos, Greece (1996)
19. Dudek, P., et al.: A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line. IEEE J. Solid-State Circuits. 35(2), 240–247 (2000)
20. Mostafa, H., et al.: Novel timing yield improvement circuits for high-performance low-power wide fan-in dynamic OR gates. IEEE Trans. Circuits Syst. I. 58(8), 1785–1797 (2011)
21. Pelgrom, M.J.M., et al.: Matching properties of MOS transistors. IEEE J. Solid-State Circuits. 24(5), 1433–1439 (1989)
22. Amin, M., Leung, B.: Design techniques for linearity in time-based analog-to-digital converter. IEEE Trans. Circuits Syst. II. 63(5), 433–437 (2016)
23. Dutta, R., et al.: Flip-flops for accurate multiphase clocking: transmission gate versus current mode logic. IEEE Trans. Circuits Syst. II. 60(7), 422–426 (2013)
24. Macpherson, A.R.: A time-based 5GS/s CMOS analog-to-digital converter (PhD dissertation). University of Calgary. Canada (2013)
25. Rao, R., et al.: Statistical analysis of subthreshold leakage current for VLSI circuits. IEEE Trans. VLSI Syst. 12(2), 131–139 (2004)
26. Wong, L.S.Y., et al.: A 0.9 V 5 MS/s CMOS D/A converter with multi-input floating-gate MOS, In: Proceedings of the IEEE custom integrated circuits conference, pp. 305–308. Santa Clara (1997)
27. Yang, B.-D., et al.: An area-efficient coarse-fine resistor-string D/A converter. In: Proceedings of the IEEE Latin American symposium on circuits and systems, pp. 29–32. Foz do Iguacu (2010)
28. Lin, K.-T., et al.: A 0.5 V 1.28-MS/s 4.68-fJ/conversion-step SAR ADC with energy-efficient DAC and trilevel switching scheme. IEEE Trans. VLSI Syst. 24(4), 1441–1449 (2016)

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