LOW POWER DUAL MODE BLUETOOTH 5.1/BLUETOOTH LOW ENERGY RECEIVER DESIGN

By

Ahmed Magdy Afifi Azb

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
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Key Words:
Bluetooth; BLE; low-IF; mixer-first; RF front end; dual mode; high performance mode; low power mode; passive mixer; harmonic down-conversion; current reuse; complex pole; Gm-C filter

Summary:
This thesis presents low power Bluetooth5.1, BT5.1, and Bluetooth low energy, BLE, compliant receiver. The receiver has two modes of operation;

low power mode, and high performance mode. It brings up various techniques for low power consumption at both system and circuit level. Low IF mixer first architecture is utilized to optimize power consumption at system level. Furthermore, harmonic down-conversion in the low power mode enables quadrature LO generation. Reduced supply voltage, 500mV for VCOs and 700mV for front end chain, passive mixers, and current reuse address power minimization at circuit level. The proposed receiver utilizes an integrated configurable matching circuit. The proposed receiver is implemented in 65 nm CMOS technology and occupies an active area of 0.551 $\boldsymbol{mm^2}$ consuming only 697 µW and 1250 µW when operating in low power mode and high performance mode respectively. Low power mode RX achieves a noise figure of 12.82 dB and IIP3 of +5.58 dBm while provides image rejection by 81 dB. For high performance mode, the RX front end achieves a 6.3 dB noise figure, +2.6 dBm IIP3, and 65 dB image rejection.

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Thanks are also due to my invaluable network of supportive, generous and loving professors, and colleagues without whom I could not have achieved the whole thing.

Dedication

To

My Father,

My Mother,

My elder brother Alaa,

, and

My little brother Hossam

For their love and support

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Nomenclature

Abbreviation	Description
WSN	Wireless Sensor Network
IoT	Internet of Things
ULP	Ultra low power
RX	Receiver
TX	Transmitter
WuRX	Wake-Up receiver
BLE	Bluetooth Low Energy
BT	Bluetooth
RF	Radio Frequency
IF	Intermediate Frequency
LO	Local Oscillator
VCO	Voltage Controlled Oscillator
LNA	Low Noise Amplifier
LMV	LNA-Mixer-VCO
ADC	Analog-to-Digital
LTI	Linear Time Invariant
LTV	Linear Time Variant
ISM	Industrial, Scientific and Medical
SNR	Signal-to-Noise Ratio
BER	Bit Error Rate
IIP3	Third-order Intercept Point
IRR	Interference Rejection Ratio
NF	Noise Figure
PN	Phase Noise

ACR	Adjacent Channel Rejection
CMRR	Common Mode Rejection Ratio
OOB	Out-Of-Band
ADPLL	All-Digital Phase Locked Loop
GFSK	Gaussian Frequency Shift Keying
DQPSK	Differential Quadrature Phase Shift Keying
OOK	On Off Keying
SRO	super regenerative oscillator
BAW	Bulk Acoustic Wave
FBAR	Film Bulk Acoustic wave
SAW	Surface Acoustic Wave
ILO	injection locking oscillator
N-PPMs	N-path passive-mixers
PVT	Process, Voltage, and Temperature

Abstract

The continuous development of Wireless Sensor Network, WSN, based systems is highly motivating the need for Ultra Low Power, ULP, Radios where too many devices and sensors are equipped by a receiver (RX), a transmitter (TX), or a transceiver. These nodes are intended to operate in a self-powered energy-harvesting scheme to avoid the routine of battery change or recharge. Hence, these nodes are highly power consumption constrained.

WSN devices employ heavy duty cycling since they need not to be active all the time to reduce power. Another alternative technique is to use an always on Wake-Up receiver (WuRX) consuming few micro-watts or even sub-µW power while keeping the main receiver in sleep mode till receiving a wake up signal from the WuRX. The second approach is suitable for latency-critical applications.

Low data rates wireless standards tailored for low power applications are utilized in WSN nodes. Operating at low data rates, low power nodes can achieve better sensitivity levels which will allow TX power reduction by transmitting at lower power. Bluetooth Low Energy, BLE, is one of the best candidates as a wireless standard for WSN since Bluetooth technology is emerging and widely deployed and adopted due to its robustness, low-cost, and customization flexibility.

This thesis presents low power Bluetooth5.1, BT5.1, and Bluetooth low energy, BLE, compliant receiver. The receiver has two modes of operation; low power mode, and high performance mode. It brings up various techniques for low power consumption at both system and circuit level. Low IF mixer first architecture is utilized to optimize power consumption at system level. Furthermore, harmonic down-conversion in the low power mode enables quadrature LO generation. Reduced supply voltage, 500mV for VCOs and 700mV for front end chain, passive mixers, and current reuse address power minimization at circuit level. The proposed receiver utilizes an integrated configurable matching circuit. The proposed receiver is implemented in 65 nm CMOS technology and occupies an active area of 0.551 $\boldsymbol{mm^2}$ consuming only 697 µW and 1250 µW when operating in low power mode and high performance mode respectively. Low power mode RX achieves a noise figure of 12.82 dB and IIP3 of +5.58 dBm while provides image rejection by 81 dB. For high performance mode, the RX front end achieves a 6.3 dB noise figure, +2.6 dBm IIP3, and 65 dB image rejection.

Four phases passive mixer analysis based of Linear Time Variant, LTV, and Linear Time Invariant, LTI, models will be reviewed for fundamental LO component. Also, the analysis is extended to explain harmonic down-conversion properties of passive mixers and discuss the benefits and drawbacks.

The proposed receiver is the first one to utilize single receiver chain design realizing two modes of operation through fundamental and harmonic down-conversion based on passive mixers analysis at LO harmonics. Moreover, it offers high flexible configurability by adopting two modes of operation and Bluetooth and BLE compliance.

Chapter 1 : Introduction

1.1. Background

Bluetooth technology is a short range, robust, low power, low cost, and widely customizable communication system aiming to connect various fixed and portable devices [1]. Since earlier Bluetooth specification releases, it has been adopted in many applications due to its key features. Moreover, Bluetooth Low Energy (BLE) has been introduced for the first time in the fourth release of Bluetooth standard. Bluetooth/BLE operates in the same 2.4GHz ISM radio band as *IEEE 802.11b/g/n/ax* (WiFi) and *IEEE 802.15.4* (ZigBee).

As demand for ultra-low power (ULP) radios; like in Wireless Sensor Networks (WSN), wearable devices, medically implanted devices, wireless payment tags, etc; is rapidly increasing, BLE offers one of the best candidates as a wireless communication standard. Furthermore, BLE had been employed in wake up receivers (WuRX) in prior works achieving less than 250 µW power consumption [2] – [6] which enables efficient use of main receiver chains in WSN and also makes use of Energy Harvesters (EH) as the second approach of power reduction in WSN especially suitable for latency-critical applications, while the first well-known approach is duty cycling. Although Bluetooth has relaxed specifications, ultra-low power receivers, achieving sub-mW, are still a challenging task. Power-hungry blocks, like VCO, usually defines a lower limit for power performance.

Too many works have been done to realize ultra-low power radios using various techniques. LNA-Mixer-VCO (LMV) cell-based receiver has been introduced in [7], [8] where LNA current is recycled by stacked mixer and VCO. This technique, however, has reduced voltage headroom and block isolation; that's VCO may be pulled by RF blockers and VCO noise will add to RX noise. Ultra-low voltage supply receivers are popular low power radios approach. A 300mV RX in [9] extensively applies transformer coupling between RF blocks to maximize headroom and lowers transistor threshold voltage through forward body biasing. This comes at the cost of area and increase of leakage currents. Moreover, 180mV RX front end was introduced in [10] where I/Q generation is obtained by a passive RC-CR network in the RF path. According to [11], good matching should be preserved through careful layout. Also, as the supply voltage is reduced, IIP3 degrades accordingly. In addition, inductive loaded LNA is divided to two stages, one providing conventional LNA requirements and the second for driving subsequent RC-CR network and passive mixers which imposed extra area.

Other works focus on eliminating I and Q paths employed either in direct conversion or low-IF architecture. In [12], an All-Digital Phase Locked Loop (ADPLL) based receiver with hybrid loop achieves 20 dB Adjacent Channel Rejection (ACR) without the need for RF filters while eliminating two Analog-to-Digital (ADCs) and Q-channel to reduce power consumption. While in [13], conventional Low-IF has been adapted to employ single channel receiving method and ADPLL is reused as an ADC also to eliminate Q-path.

The proposed BT5.1/BLE receiver operates in two modes; low power, and high performance. In the low power mode, mixer down-converts RF signal using third harmonic of LO to compensate for the impact of I/Q, necessary for low-IF architecture adopted, LO generation on power consumption while normally down-converts RF signal using fundamental LO component in high performance mode. The receiver incorporates a configurable integrated matching circuit to adapt input impedance change between the two modes due to 4-phase passive mixers transparency at the front end. The mixer first architecture allows LNA to operate at IF, unlike conventional LNA first architecture where LNAs are at RF and hence require high power consumption. A configurable complex filter permits both BT5.1 and BLE operation in both receiver modes. Software at the top layer can drive the PHY layer to either mode or wireless standard. The proposed receiver utilizes reduced supply voltage and current reuse which enable achieving required transcondactunce, g_m, to meet specs of building blocks while at effective low power.

1.2. Organization of the thesis

The remainder of this thesis organized as follows. Chapter 2 reviews different power reduction techniques and receiver architectures in the literature. Chapter 2 presents the receiver system level design. The 4-phase passive mixer analysis is detailed and followed by the designs of the VCO and receiver building blocks in Chapter 2. Chapter 5 discusses the results and compares to the state of the art. Finally, the work contribution is summarized, and the conclusions are drawn.

Chapter 2 : Literature Review

2.1. Introduction

The continuous demand for the Wireless Sensor Network, WSN, based systems and the Internet of Things, IoT, technology pushes the limits for the performance of the RF transceivers. It has been driving development of wireless communication standards like Zigbee, WirelessHART, ISA 100.11a, 6LoWPAN, IEEE 802.15.4e, Bluetooth, and Bluetooth Low Energy (BLE). Moreover, innovations in radio architecture and circuit techniques have been being developed to adopt the rapid increase and evolutionary requirements of WSN applications.

Power consumption of nodes is the major constraint to address in such applications. The RF front end which is equipped in each single node represents a considerable power consumption share, usually no less than 50%, out of the total power [14]. Furthermore, those nodes are intended to operate in a self-powered energy-harvesting scheme to avoid the routine of battery change or recharge. Therefore, many techniques on different layers, starting from the PHY layer up to the very high level layer of application, have been developed and brought up together to save power consumption whenever possible.

2.2. Wireless Sensor Networks (WSN)

Wireless Sensor Networks are a set of tenths to thousands autonomous mesh networks comprised of sensing nodes exchange data through wireless communication at any environment. Multiple standards have been introduced with relaxed specifications to be easily employed in WSN applications and satisfying their requirements. Low data rates, adjacent channel rejection, phase noise, transmission power level, narrowband channels, and short range characterize communication standards adopted by WSN and IoT applications.

2.3. WSN requirements

Individual nodes of the network should satisfy the following main requirements:

1. Size: nodes should be enough compact from the physical area perspective to fit in the diverse hard environments.

2. Cost: the individual nodes of the network should be low-cost because the target systems can deploy very large number of nodes; up to thousands.
3. Power Consumption: the network nodes are supplied either from battery or, preferably, from an energy harvesting source/system. In both cases, the low power consumption operation is the mandatory requirement either to ensure long battery life, several years, or the capacity of energy harvesters under all conditions.
4. Sensitivity: the system power reduction can be obtained through utilizing less count of network nodes and lower levels of transmission power. Therefore, indeed a highly sensitive receiver front ends in each node are required to allow for long distance placement of the network communicating nodes at such low levels of transmission power.
5. Interference rejection: all network nodes are communicating over the same band at low levels of power – for the sake of overall system power consumption – which requires good adjacent channel rejection to ensure coexistence.

2.4. WSN applications

WSN had found its way in too many applications with various domains. In WSN, the main principle operations are 1) monitoring an environment, where the system is deployed, 2) intelligently makes decisions, 3) and takes actions accordingly. The WSN deployment usually depends on the following:

1) physical environment
2) intended ranges to be covered
3) estimated target network lifetime
4) the type of the data to be exchanged between nodes

Following are some of the most common applications for WSN:

1. Health-care monitoring: like medical applications include monitoring of several processes, ex. physiological changes, motion and activity, and mobile patient vital sign [15], [16].
2. Environmental monitoring: environmental monitoring involves many natural physical quantities like volcano activities; forest fire detection; air pollution rates; temperature, humidity, and water levels monitoring; and radiation measurements [17].
3. Smart structures: the flexibility of WSN enables autonomous behavior in a complex structures like smart homes, buildings, and cities.
4. Entertainment: the WSN principally involves smart Body Area Network (BAN) for the applications with high data rates such as video gaming [18].

2.5. Power optimization techniques

Since power consumption of the network nodes is the major constraint to address in such WSN applications, various methodologies have been being explored on all wireless network protocol stack. The developed techniques are aiming to extend power consumption minimization more and more in the already developed wireless standards for ultra-low power applications. Although going up in the protocol stack makes things highly abstracted, effective techniques are being actively developed for power reduction.

2.5.1. Application layer:

Many different techniques can be used at the application layer to reduce power of network nodes. Load partitioning is a well-known, effective, and commonly used technique. Intensive computation of applications can be carried out on the base station – the central node – instead of distributing it among the network nodes. Therefore, the work done by individual nodes in the network is much more relaxed. In this scheme, the nodes send requests to the central node in order to process the required computation on its behalf and wait for the results. There are many various other application specific methodologies. For example, heavy data processing applications use various efficient compression algorithms to decrease the number of the bytes to be transmitted between the network nodes. On the other hand, database applications are currently exploring new algorithms to index and retrieve the data, and perform query operations to reduce the required communication among nodes. Furthermore, power-aware operating systems (OS) have been developed specifically to target WSNs such as Contiki, MANTIS, etc [19].

2.5.2. Transport layer:

At the transport layer, power saving can be addressed through the efficient handling of the necessary retransmission of data due to the packet losses in a faulty links. In the traditional wired networks, the packet losses are used to identify the congestion paths between the network nodes. Therefore, transport layer applies a re-routing mechanism. However, in wireless links, the packet losses do not necessarily happen to occur due to congestion. Taking this fact into consideration, the unnecessary immediate re-routing decisions – which may terribly impact the power performance because of the packets transmission forwarding through longer paths – could be avoided.

2.5.3. Network layer:

Network layer optimization is concerned with the power-efficient routing algorithms along with the employed network topology in the system. Intelligent algorithms should utilize the shortest path between the directly uncontended communicating nodes to reduce the required packets forwarding between communicating nodes while avoiding possible nodes contention or paths congestions.

2.5.4. Data link layer:

A very common technique to decrease the power consumption in a network at the data link layer is the packet scheduling protocol based algorithms. The bundling of multiple packets into a single burst to be transmitted decreases the overhead bytes which is associated with each packet – added by the data link layer – to be individually transmitted. In addition, the packet scheduling may reduce the re-transmission rate due to the packet loss. It defers the packets transmission targeting a specific node to a time when this target node is capable of receiving and processing more packets.

2.5.5. MAC layer:

At MAC layer, the power reduction techniques rely mainly on the sleep scheduling protocols. The network nodes do not have data to transmit and similarly they would not need to receive data continuously all the time. Therefore they could operate under a duty cycling scheme to obtain effective power savings. Three main schemes providing duty cycled wireless communication have been presented in [20]:

2.5.5.1. Synchronous:

All nodes in the network are periodically synchronized. Successful communication is guaranteed, but the power overhead due to the required periodic synchronization and re-transmission may degrade the power performance of the whole system. Moreover, it would not be suitable for the latency-critical applications where the receiving node may keep missing repeated transmissions from another node till it wakes up on the next cycle. On the other hand, many applications utilize heavy duty cycling – 1% duty cycle – of this scheme since their nodes are in sleep mode most of the time.

2.5.5.2. Pseudo-asynchronous:

In this scheme, nodes are in a standby mode – rather than the sleep mode in the synchronous scheme – and they are only waken up

when receiving a target request packet from the transmitting node. This scheme is optimized over the synchronous scheme for applications which have long off periods where no necessary periodic wake-ups and synchronization are needed.

2.5.5.3. Asynchronous:

In this scheme, the network nodes are comprising of two receivers: the main receiver and a wake-up (WuRX) receiver. The main receiver remains off until signaled by the WuRX which remains always on, monitoring the channel for an incoming wake-up packet. The main receiver is waken up to handle main data packets then back to the sleep mode again. This scheme is considered as the most power efficient one. WuRX power consumption should indeed be negligible compared to the main receiver power. Moreover, power could be reduced by duty cycling the WuRX itself; resulting a new hybrid scheme. Therefore, this scheme is divided to two methodologies: always-on mode, and duty-cycled mode. Although duty-cycled mode turns this scheme to synchronous, WuRX duty cycling is much more relaxed than main receiver duty cycling due to the fact it has negligible power – few microwatts or even sub-uW power. As a result, power latency tradeoff could be easily compromised using this scheme. Too many works have been proposing WuRX designs where they are either as simple as power detection circuit [21] – [25] or as capable as main receivers in modulating signals, retrieving data, and securely waking up main receivers without being deceived with a false alarms [2], [3], [26] – [28].

2.5.6. Physical layer:

A lot of smart techniques for power reduction at physical layer can save the significant power consumption portion along with the MAC layer. Since nodes spend most of the time in the idle state, minimizing leakage currents is commonly adopted as a design requirement for circuits either in RF front end

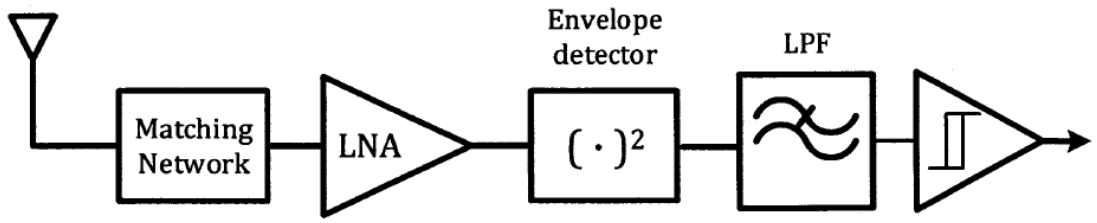


Figure 2.1: Energy-detection receiver architecture [3]

, or digital baseband. Therefore they employ high threshold voltage and FinFET devices offered by the CMOS processes. Technology scaling, CPU voltage scaling, variable clock CPUs, flash memory, and disk spin down techniques can be used to reduce the active power as well [29].

Techniques can be classified into two main categories; First category system level methodologies represented in effective low power receiver architectures, and second category involves innovative circuit techniques for low power implementation of the receiver building blocks.

2.5.6.1. Receiver Architectures:

2.5.6.1.1. Energy-Detection Receivers

Energy-detection receivers are the simplest architectures. Figure 2.1 shows one of the most common architectures of the energy-detection receivers. They are the most power efficient receivers because they include no power hungry building blocks like the LO and mixers. The RF signal is regularly amplified through the LNA. Then it is self-mixed to be down-converted to the baseband. Afterwards the baseband signal is passed through a LPF to perform adjacent channel rejection. Finally, the signal level is compared against a reference voltage to obtain either zero, or one. Although energy-detection receivers can achieve sub-µW power consumption, they are only limited to the OOK modulation schemes. OOK modulation scheme might not be suitable to many applications, and have a small data rates. The power-detection architectures had been widely adopted in WuRX. Sub-µW WuRX have been introduced in [30] – [31] at the cost of the reduced sensitivity.

2.5.6.1.2. Super-regenerative Receivers

Super-regenerative architecture, shown in figure 2.2, is one of the most common low-power receivers, and widely employed in the WSNs. They are mainly based on a super-regenerative oscillator, SRO. The key idea is to use a duty-cycled, quench node, oscillator which starts the oscillation with a build-up time proportional to the received RF signals power level. The SRO then dissipates the stored power in its tank through the baseband blocks, representing a non-linear filter behavior. SROs are usually realized using an external high-Q resonators, like the Bulk Acoustic Wave (BAW), which are consuming large area and costly. In addition, the maximum data rates are limited by the build-up time of the SRO oscillations. Low-power receivers, OOK and BFSK modulation schemes compliant, and achieving high

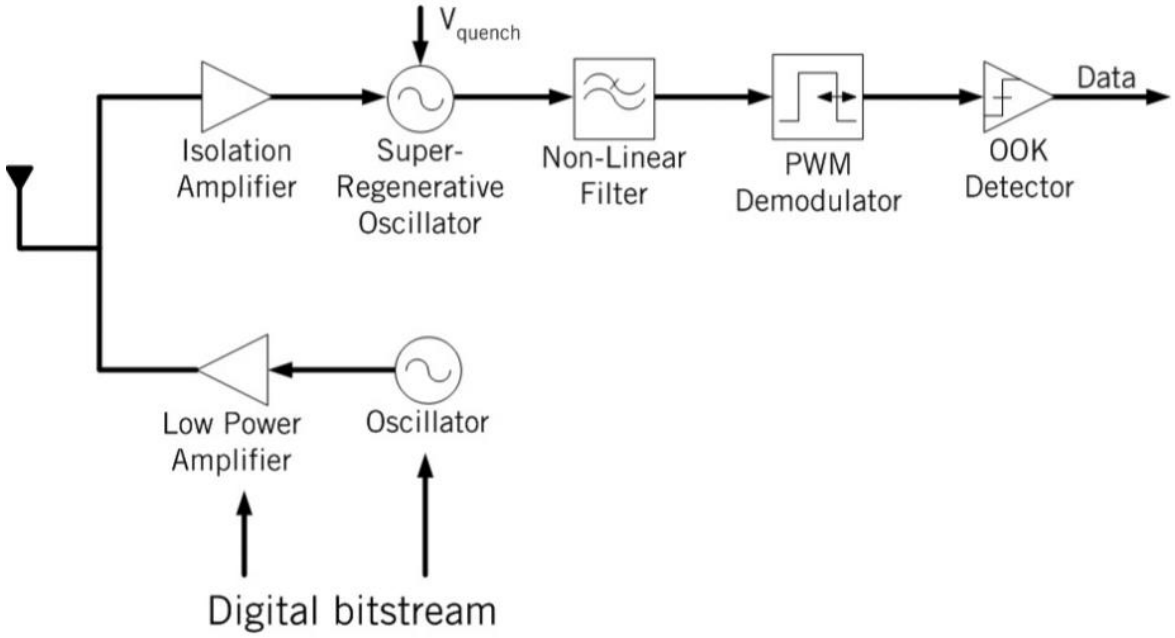


Figure 2.2: Super-regenerative receiver architecture [33]

sensitivity have been proposed in [32] – [33].

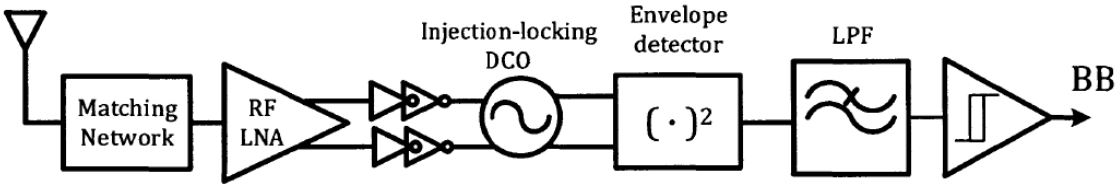


Figure 2.3: Injection-locking receiver architecture [3]

2.5.6.1.3. Injection-locking Receivers

Injection-locking architectures, shown in figure 2.3, have been developed to extend the capability of the very simple energy-detection architectures to modulate a Frequency Shift Keying, FSK, signals while preserving its power efficiency and simplicity.

This architecture adds an injection-locking oscillator, ILO, directly following the LNA, to the energy-detection receiver architecture to convert the FSK modulated signals to an OOK signals. The ILO produces a constant envelope signal when injected by a signal with a frequency in the range of locking. On the other hand, a signal with a frequency outside the locking range causes an injection pulling. Therefore, a time-varying phase will result an amplitude modulated signal. In [34], A 640-µW receiver achieving -87dBm sensitivity was introduced. The receiver utilized the injection-locking architecture.

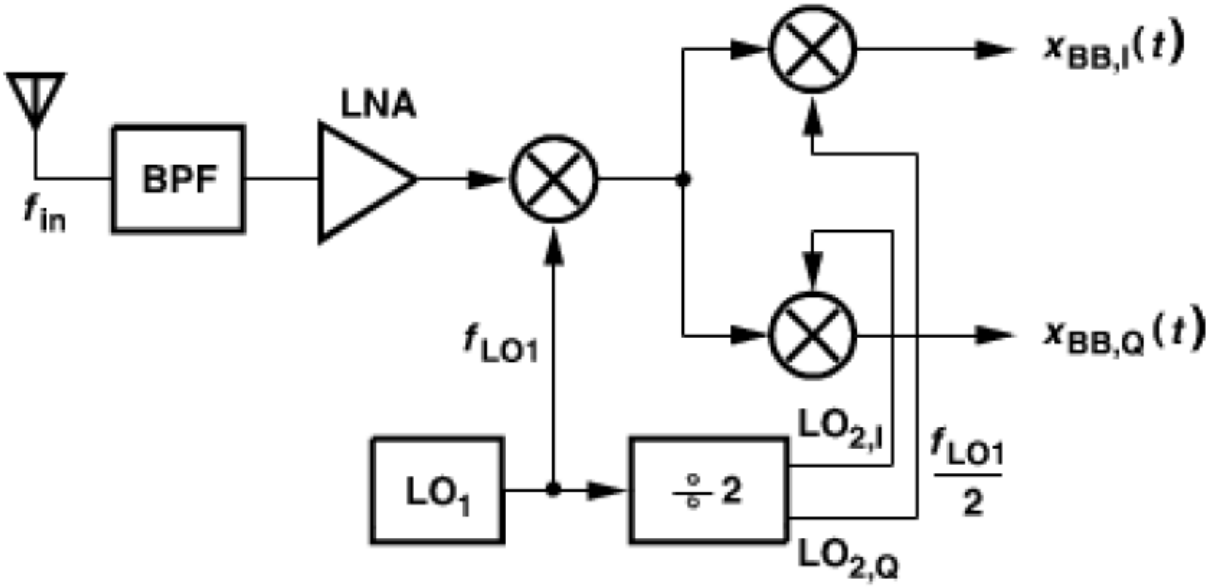


Figure 2.4: Sliding IF receiver architecture [35]

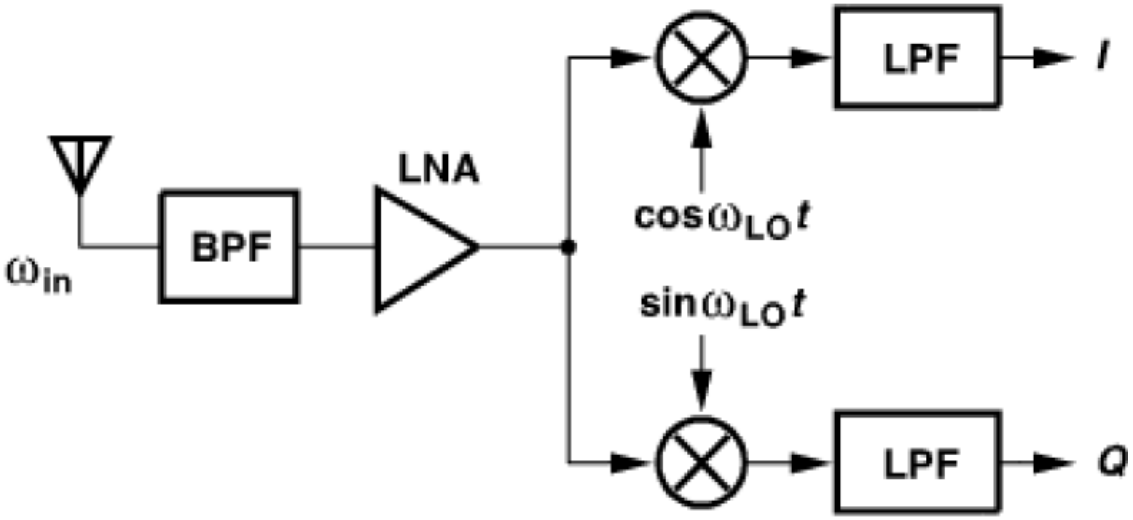


Figure 2.5: Direct conversion receiver architecture [35]

2.5.6.1.4. Sliding IF Receivers

The sliding IF receiver architecture is a dual-conversion super-heterodyne architecture. It employs only single oscillator to realize both LO_1 and LO_2. In the conventional super-heterodyne architecture, each LO was generated from a completely separate oscillator. This approach had a serious drawback that the multiple oscillators on the same chip experience an unwanted coupling. Instead, in the sliding IF architecture, the second local oscillator, LO_2, is derived from the first local oscillator, LO_1, through a frequency dividers.

Figure 2.4 shows a sliding IF receiver with frequency division ratio of two. The first IF, in the sliding IF architecture, is not a constant. It varies, or slides – that's where the naming comes from, as the RF signal frequency varies across the target band. For example, assuming that the receiver, in figure 2.4, has zero second IF, then the f_{LO1} will be $\frac{2}{3}\, f_{in}$ and the f_{IF1} will equal to $\frac{1}{3}\, f_{in}$.

The Sliding IF architecture raises tradeoff between the image rejection and the accuracy of the LO quadrature generation. Higher frequency division ratios result a lower LO_2. Therefore, a smaller mismatches between the LO quadrature phases are indeed required. On the other hand, frequency difference between the RF signal and its image decreases as the LO_2 is reduced which in turn makes it difficult to reject the image, and the thermal noise of both the antenna and the LNA in the image band through the RF filters

2.5.6.1.5. Direct Conversion Receivers

Direct Conversion, Zero-IF or homodyne architecture, shown in figure 2.5, is one of the most common architectures in all wireless applications. The main advantages of direct conversion architecture over traditional heterodyne receivers [34] are:

1. A simpler frequency planning
2. absence of image frequencies
3. Low-pass filters easily realized as an integrated active filter instead of band-pass filters which have stringent tradeoffs between center frequency and quality factor
4. Reduced mixing spurs

In the direct conversion receivers, the RF signals are directly down-converted to the baseband after the low noise amplification. Asymmetrically-modulated signals will be corrupted when they are down-converted to the basebands.

Therefore the typical direct conversion receiver provides two paths, I and Q, to separate the baseband signals through their phases. Although the direct conversion architecture entails some drawbacks, such as DC offset; LO leakage; even-order distortion; flicker noise; and I/Q mismatch, they have been developed over years to overcome these issues. Like the conventional heterodyne receivers, they require band-select filter at the front end which is usually costly and bulky such as: Surface Acoustic Wave (SAW) or Film Bulk Acoustic wave (FBAR) filters. Many works had been reported utilizing direct conversion architecture in [36] – [41] achieving tailored specs of each application.

2.5.6.1.6. Low-IF Receivers

The low-IF architecture is similar to the direct conversion architecture except for RF signal is down-converted to a low intermediate frequency (IF), which is very near to baseband. Therefore two main issues of the direct conversion architecture are avoided; flicker noise and DC offset. On the other hand, the image rejection is required. In the low-IF receivers, image and desired frequencies are in the same band, unlike conventional heterodyne receivers. Most of standards, especially narrowband standards, have much relaxed adjacent channel tolerance compared to out-of-band blocker tolerance. Hence a moderate Image Rejection Ratio, IRR, would be sufficient.

The Low-IF architecture requires both I and Q paths for image rejection which is achieved through either a polyphase or a complex filters. Two receiver chain paths demands 2x of power consumption in the baseband blocks and extra LO power consumption for the I/Q generation in case of single phase RF signal driving the mixers.

2.5.6.2. System power-efficient techniques:

2.5.6.2.1. Mixer first front end

LNAs are usually used as first active block in the receivers to provide a low return loss and essential low-noise voltage gain over entire target RF band. Due to their wide bandwidth and high operational frequency requirements, the LNAs require significant high power consumption. Alternatively, a mixer-first configuration was proposed where the LNA is deferred from the RF band to a much lower IF band, in order to aggressively cut down the power consumption and the effective bandwidth requirements. In this case, the mixers must provide a high linear frequency responses to guarantee wide RF input signal dynamic.

2.5.6.2.2. Harmonic down-conversion

The conventional fundamental-order mixers down-convert RF signal to IF by mixing it with local oscillator frequency. For example; the LO fundamental harmonic is mixed with the RF frequency to generate the IF as explained by

$$\omega_{IF} = \omega_{RF} - \omega_{LO}$$

However, in the sub-harmonic mixer, the LO harmonic frequency is used to be mixed with the RF frequency in order to generate the LO, i.e.

$$\omega_{IF} = \omega_{RF} - n\,\omega_{LO}$$

where n is the n^{th} harmonic of the LO.

Thus, The LO signal is a fractional sub-harmonic of the RF frequency. There are many advantages of using sub-harmonic mixers.

1) Simplified LO generation: it is hard to generate a local oscillator signal with a low-phase noise because of lower quality-factors of passive components and the lower current gain of transistors. In current technologies, the lower frequency oscillators have a better phase noise performance, due to a higher transistor current gain at lower frequencies and a better passive devices in the newer technologies
2) DC offset reduction: direct-conversion receivers highly utilize this advantage. In the fundamental-order mixer, LO signal leaking from oscillator port into RF port will self-mix with the LO to cause DC offsets. Therefore, they could saturate baseband circuits which follow receiver or corrupt baseband signal. To avoid this, using a sub-harmonic mixer is a candidate solution, where self-mixing will not fall at the baseband or cause a DC offsets, because the LO frequency is a fractional harmonic of RF frequency

3) LO buffers power consumption: the consumed power in LO buffer circuitry can be large at the high LO frequencies. If LO frequency is a subharmonic fraction of RF frequency, the required power in the buffers shall be significantly reduced. Moreover, in the future phased-array applications, – where single LO could be imagined to drive a multiple receiver elements – the routing losses hence the LO buffers power consumption could be decreased through using a sub-harmonic mixers.

2.5.6.3. Circuit power-efficient techniques:

2.5.6.3.1. Passive building blocks

The ultra-low power receivers employ a passive building blocks whenever possible in order to reduce the active power consumption. There are many various blocks which can be implemented using completely passive elements.

1) Transformer-based amplification: Transformers have been utilized at the front end of the receivers for a single-ended to a differential conversion. In principle, the 1-to-N transformer could amplify input voltage by N factor and transform impedance seen by its secondary to the value necessary for matching, a 50 Ω. However, the imperfections such as: limited magnetic coupling; power loss, hence noise; and substantial capacitive coupling may degrade performance too much as to defeat the main purpose. In [40], a stacked structure transformer has been investigated to optimally design the front-end transformer which replaces the traditional LNA, with a compromise between the voltage gain, and the capacitive coupling and losses. It achieves a noise figure of 4.5 dB, 12 dB gain, and $|S_{11}|$ > 12 dB using a complete passive front end.

2) Passive mixer: The passive mixer as a first block in receiver chains comes as the very appealing front-ends for the ultra-low power receivers**.** Passive mixer consume no power while directly down-converting the RF input signal to an IF for both amplification and filtering at much lower rate, hence power consumption. However, several implications arise from the mixer switches being as the very first block after the matching network.

The first issue is receiver's input impedance and matching requirements with the antenna. The passive mixer is transparent. Therefore, its input impedance strongly depends on baseband impedance presented to it. In addition, re-radiation back to antenna through mixer switches results in dependence on the impedance at the mixer RF port. Thus, the matching network of the mixer-first architectures must be carefully designed in order to account for both load and source impedances of mixer.

The second issue is the noise figure of the mixer, and its effect on the performance of the overall system. Mainly, this drawback is due to the passive mixers transparency which results in the up-conversion of the baseband signals and the re-radiation, hence signal power loss. Passive mixer-first architecture could be used in both the high-performance receivers as well as the low power nodes. They have been showing a competitive performance metrics against the traditional LNA-first receivers.

3) Polyphase filter: The polyphase filter is a symmetric RC network with both inputs and outputs organized symmetrically in a relative phases as shown in figure 2.6. If the input frequency is $^{1}/_{2\pi RC}$, a two adjacent inputs are shifted by *+45º* and *−45º* to the output. The branches outputs constructively add for the counterclockwise quadrature inputs while destructively add for the clockwise quadrature inputs. Figure 2.7 shows the response of filter to the two sets of phasors. For the image rejection, the desired and image signals are first down-converted by the quadrature LO phases. It maps them to same frequency but into a two opposite sequences. This follows from the trigonometric identities

$$sin(\omega_{LO} \pm \omega_{IF})t \; x \; sin\, \omega_{LO}\, t$$

$$= \frac{1}{2}\,(\, cos\, \omega_{IF}\; t - \; cos(\, 2\omega_{LO} + \; \omega_{IF})\, t\,)$$

$$\rightarrow \frac{1}{2}\; cos\, \omega_{IF}\; t \quad \textit{(Higher order components ae filtered)}$$

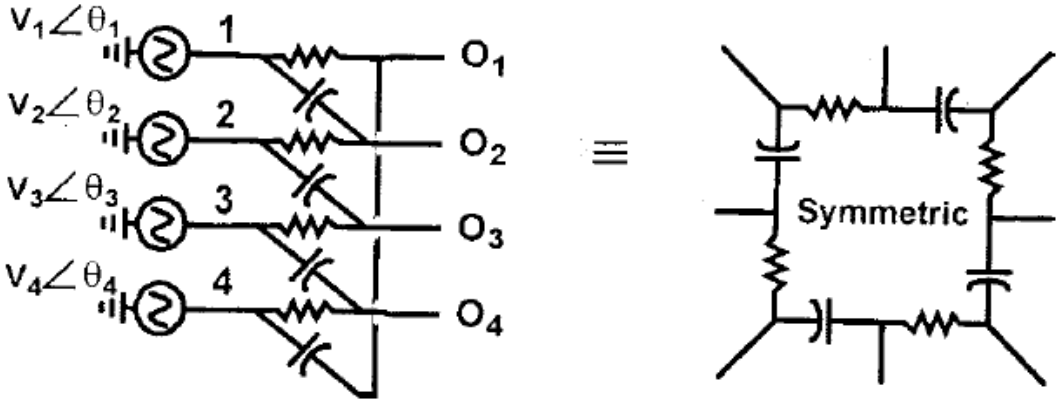


Figure 2.6: Classic *RC* polyphase filter [11]

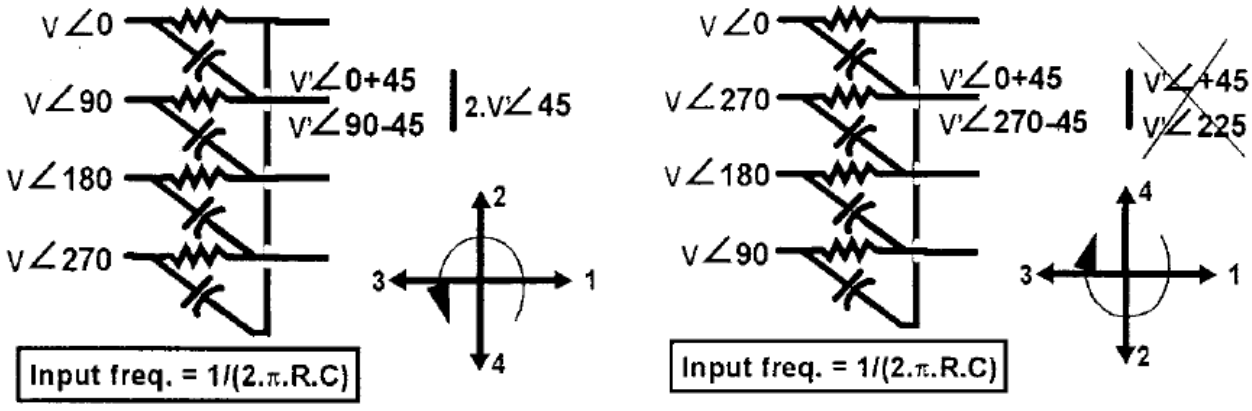


Figure 2.7: Polyphase filter passes one input sequence, counterclockwise, and nulls the other input sequence [11]

$$sin(\omega_{LO} \pm \omega_{IF})t \; x \; cos\, \omega_{LO}\, t$$

$$= \frac{1}{2}\,(\pm sin\, \omega_{IF}\; t \; + \; sin(2\omega_{LO} + \omega_{IF})\, t\,)$$

$$\rightarrow \pm \frac{1}{2}\; sin\, \omega_{IF}\; t \;\; \textit{(Higher order components ae filtered)}$$

There are many practical design considerations for the polyphaser filters as follows:

A. *Bandwidth:*

The polyphase filter rejects an input sequence fully only at the *RC* frequency. Away from this frequency, the image rejection is weaker. Therefore, multiple stagger-tuned stages of polyphase filter must be cascaded if a robust image rejection is required across wide band. Figure 2.8 shows the image rejection

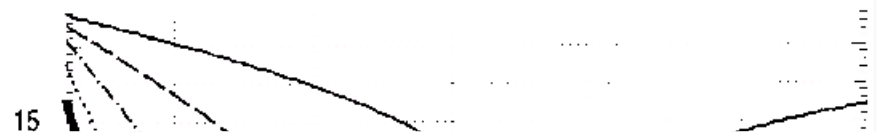
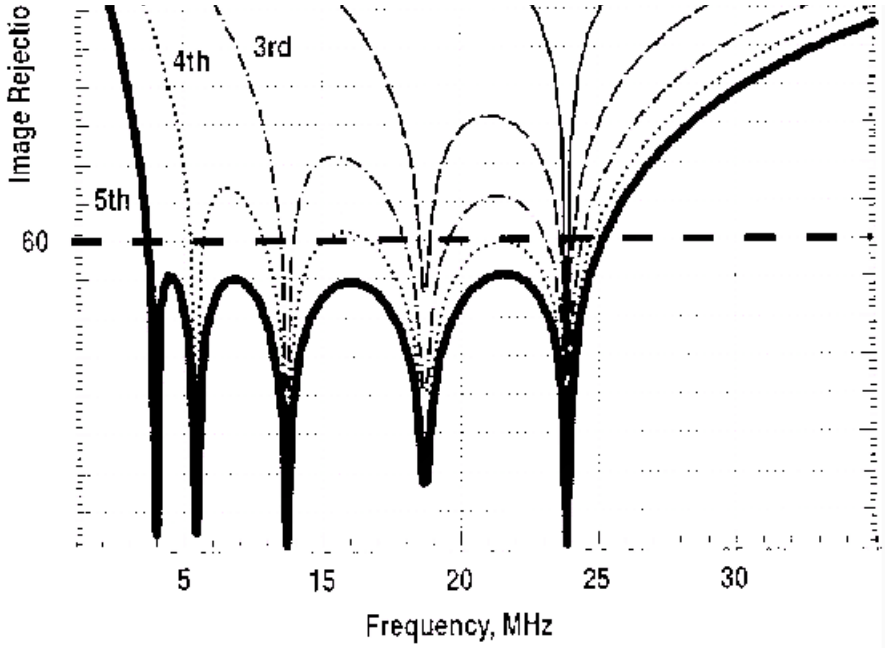


Figure 2.8: Cascade response of five-stage stagger-tuned *RC* polyphase filter [11]



through a five stage polyphase filter, whose pole frequencies are distributed over the desired bandwidth.

The logarithmically-spaced poles is the most common criteria for the poles distribution. In addition, the filter must be

designed in order to attenuate over a wider channel bandwidth – by *25%* - since on-chip *RC* time constant may vary – due to process – with up to a $\pm 25\%$ from the actual value [11].

B. *Component Matching:*

The mismatch in transfer function of each polyphase branch means that phasors which are representing image signal will no longer exactly cancel. The careful layout design and the skillful layout techniques must be followed in order to minimize the mismatches for a better obtained image rejection.

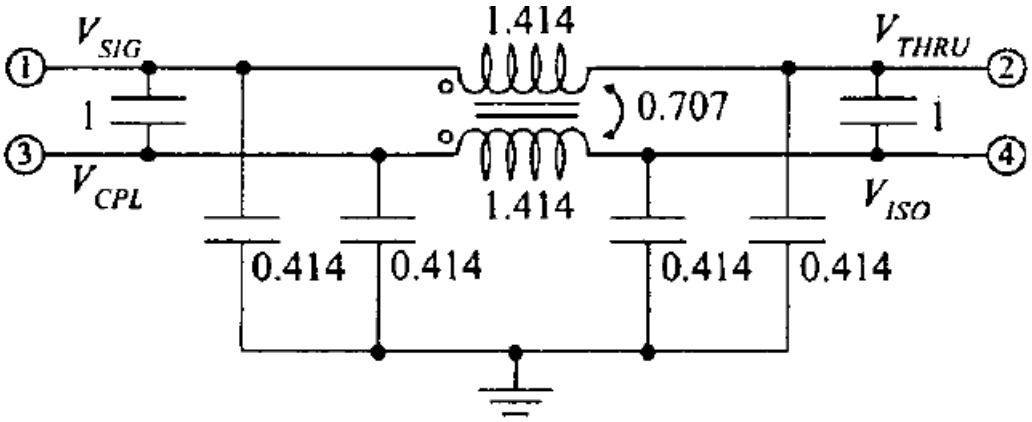


Figure 2.9: Normalized prototype lumped-element circuit for a quadrature hybrid coupler [43]

C. *Noise:*

In the multistage polyphase filter, all resistors contribute noise. However, similarly as the desired signal, the noise originating in first few stages is attenuated while traversing the filter along with desired signal. If all stages use an equal resistors but a different capacitors for the stagger tuning, the voltage noise spectral density, *4KTR*, of the last stage dominates at output. Therefore, the resistance of the last stage defines the whole filter noise and must be lower than the upper limit of the target noise.

D. *Input Impedance:*

The polyphase filter input impedance is strongly frequency dependent. In the multistage polyphase filter which is loaded at output with a capacitance only – no resistive path to the ground – which implies a very high input impedance at the dc. At the first stage pole frequency, input impedance falls. When a mixer with wideband input drives the polyphase filter, its voltage gain at the low frequency will be larger than the gain

to desired signal at pole frequency. A strong adjacent channel interferers may down-convert in the low-IF RX to lower than pole frequency and therefore may saturate the receiver. Therefore, polyphase filter must be driven by a low source impedance, such as the source followers.

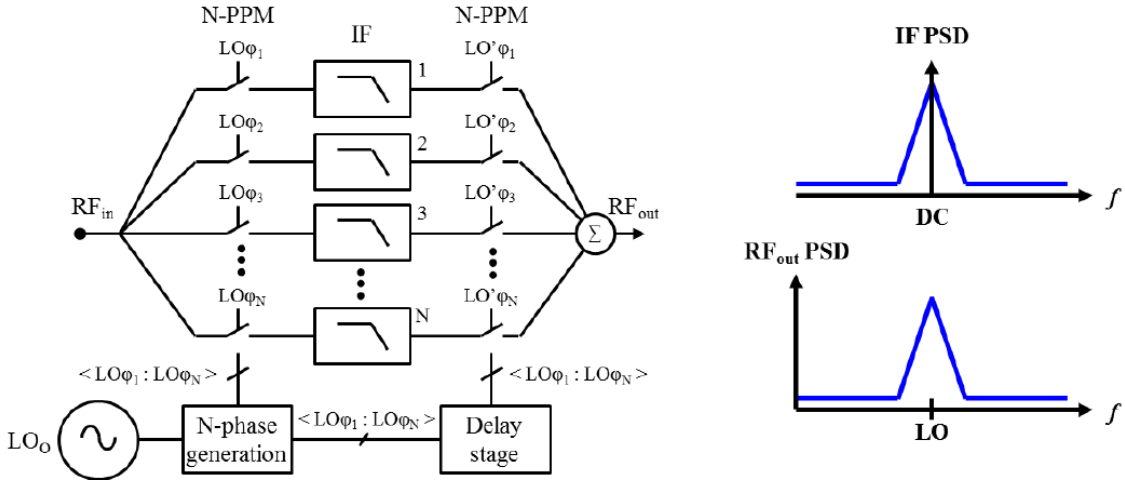
4) Quadrature generation: The simple *RC-CR* pair, adopted by the polyphase filters, is the most common, widely used and the simplest scheme of passive quadrature. They can be employed either in the RF signal path or the LO path. When synthesized in the RF path, the *RC-CR* scheme introduces a signal loss. Moreover, its functionality relies on the resistors and capacitors absolute values – which are prone to the process variations. In principal, a higher-order *RC-CR* structures with more *RC-CR* pairs in cascade could be implemented, which enhances tolerance against the process variations by trading-off a higher signal loss. On the other hand, the *RC-CR* pair realization in LO path minimizes the swing of the LO signal from a VCO which is directly driving the mixers while avoiding an incurred loss in the RF path. In order to compensate for a reduced LO swing, high swing buffers could be used to drive the mixers at expense of the required power consumption of the drivers.

Another approach for the generation of passive quadrature is use of a directional couplers. Typically, they are made using a resonant, quarter-wavelength transmission line elements as the circuit building blocks. Although they are commonly used in the microwave hybrid circuits, they are too large for an on-chip integration in the semiconductor technology at a low RF frequencies. For example, wireless applications in a 1 – 5 GHz frequency range, the lengths of a resonant elements are on order of centimeter or more [42]. Therefore, a lumped circuits have been designed in order to emulate the microwave directional couplers in [42] and [43]. Figure 2.9 shows typical transformer based directional coupler.

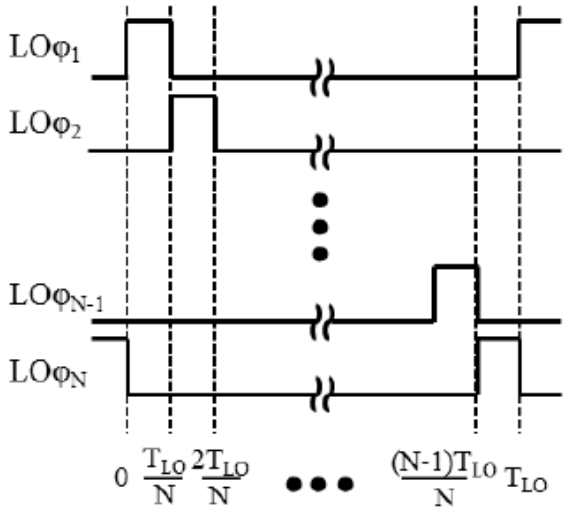
2.5.6.3.2. High-Q filters

The N-path narrow band-pass filters theory was first developed in 1947 [44]. Several years later, revisited in 1960 [45] and 1983 [46]. This theory is based on the double modulation where a Low-Pass Filter (LPF) is placed between a two N-path passive mixers – each one modeled as a simple parallel switch network as shown in figure 2.10.a – driven by the non-overlapping N-phase LO signal which is generated from global clock LO_0. Each LO phase has interval time of on-state duty-cycle equal to the cycle period of the LO (T_{LO}) over the N paths number $\left({}^{T_{LO}}/_{N}\right)$. Figure 2.10.b shows the timing diagram of N non-overlapping clocks. The first mixer down-converts the RF input signal to an IF frequency by mixing with LO ($\omega_{IF} = \omega_{RF,in} - \omega_{LO}$). At IF-band, the signals are low-pass filtered through an identical low-pass filters located in each path. The resulting IF signals are then up-converted back to the RF by mixing with LO through second mixer $\left(\omega_{RF,out} = \omega_{IF} + \omega_{LO}\right)$. To provide an isolation between two switches of each path, delay stage is introduced in the LO signal path in order to drive the second N-path mixer. Therefore, resulting output frequency response presents narrow Band-Pass Filter (BPF) which is centered at LO frequency. This BPF response is IF LPF frequency centered at the DC translated to the RF. This theory could be extended to narrow-band notch filters as well by replacing LPF with High-Pass Filter (HPF) [47] and [48], as shown in figure 2.10.c.

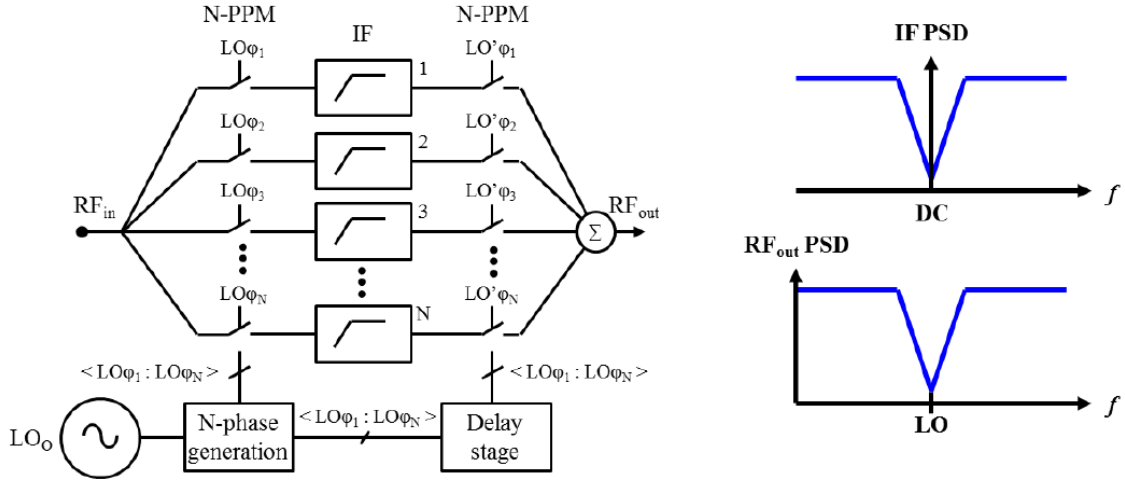
The ideal N-path passive-mixers (N-PPMs) are defined by combination of the N passive paths which are connected in parallel. Paths are composed of an ideal switch which allows the current to flow in both directions: from the input to the output and from the output to the input. The passive mixers transparency offers the bidirectional response between a high-frequency input and a down-converted output. Therefore, the BPF response could be obtained at the input node by single N-PPM as shown in figure 2.11. This effect is explained as an impedance frequency translation from a low-frequency IF mixer output node to a high-frequency RF mixer input node.



(a)



(b)



(c)

Figure 2.10: N-path passive mixer (a) band-pass filter and (b) notch filter configurations. (c) N-path mixer clock distribution [65]

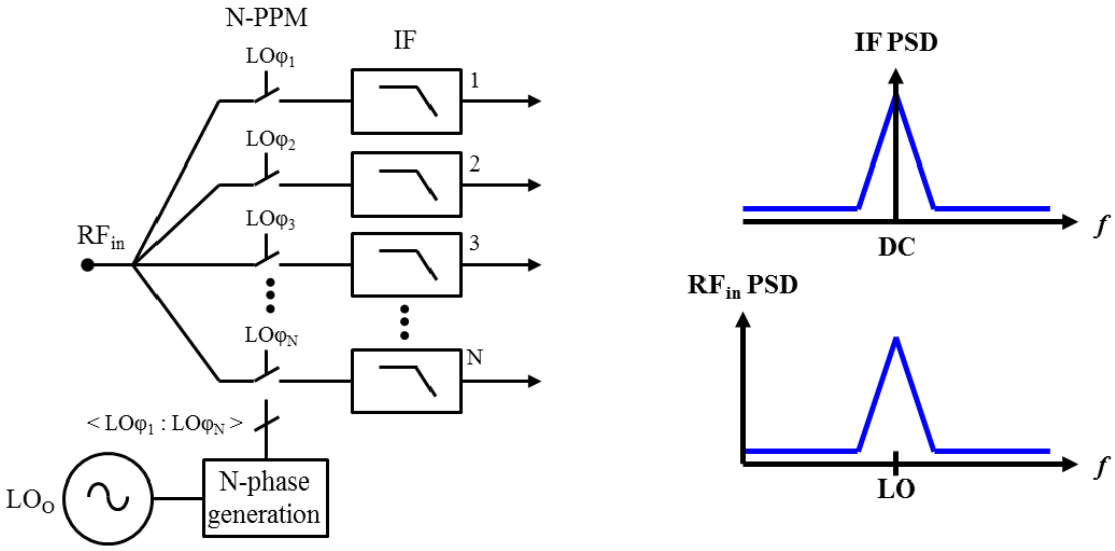


Figure 2.11: Single mixer N-path BPF configuration and respective frequency responses [65]

Recently, the N-Path Passive Mixer (N-PPM) flexibility has been widely, extensively studied through a different architectures for various types of the wireless telecommunication applications. In General, three types of N-path mixer configurations were proposed according to number of paths: 2-PPM, 4-PPM and 8-PPM. These architectures utilize the N-path mixer BPF response in order to provide a high interferer rejection while avoiding any external high-Q resonators. In context of standardized radio communications – addressed so far with such techniques – design effort has been targeted at the linearity and noise optimization. High-IIP3 mixer linearity was obtained by driving passive mixers with a large swing LO signals which are provided from a high voltage supplies [49]. The low noise figure performance was achieved by increasing the paths number and using an active feedback loop Frequency-Translational Noise-Cancelling (FTNC) techniques – implemented by a parallel N-PPM configurations placed at receiver front-end [50]. Despite their performance, these active feedback loops are not convenient for the ULP applications. Moreover, increasing the paths number results in increasing the clock circuitry complexity. Therefore, the overall system power consumption degrades. In IC design, the N-phase LO signal is typically generated from global LO_0 clock by using a digital frequency dividers. In this case, LO_0 frequency is directly proportional to the used paths number $\left(f_{LO,0} = N\, f_{RF}/_2 \right)$. Therefore, for 4-PPM and 8-PPM, the global LO_0 frequency is $2f_{RF}$ and $4f_{RF}$ respectively. This behavior could strongly affect system power consumption, especially in the case of the digital circuits (like ring oscillator), for which power consumption is directly proportional to their operational

frequency. In all these high-performant N-PPM based receivers, power consumption is set above a 10 mW. Taking the generation requirement of a high-frequency LO_0 into account – digital circuitry required to generate N-phase LO and buffer stages required to drive mixer switches – N-PPM power

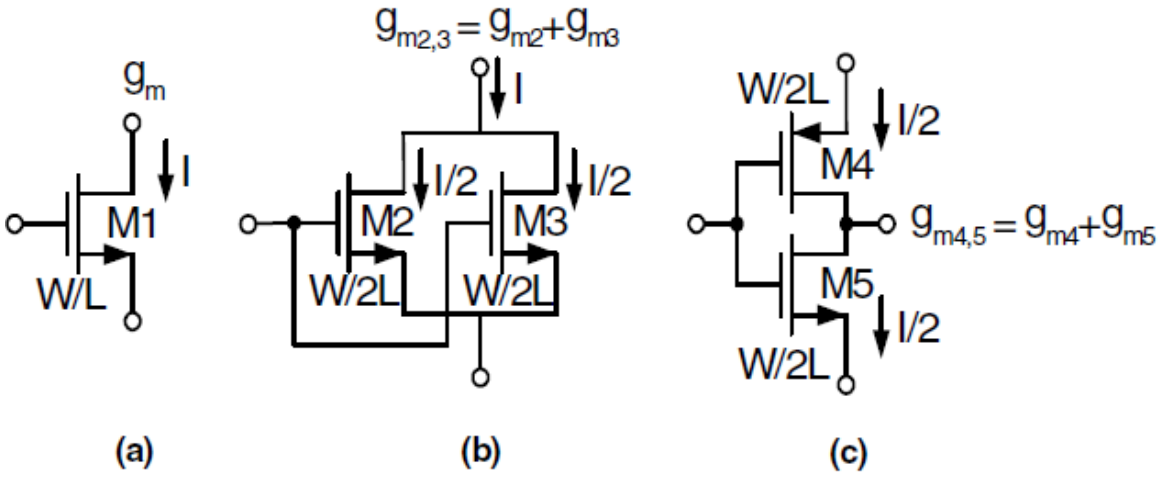


Figure 2.12: Current reuse operation principle [51]

consumption optimization could be obtained by minimizing the paths number.

2.5.6.3.3. Current reuse (recycling) and building blocks stacking

Current reuse is one of the most common and efficient techniques developed and successfully applied to many building blocks like amplifiers, mixers, OTA cells for filters, and VCO.

The basic idea in this technique is to maintain the NMOS transistor transconductance while reducing the drain current by two, as first introduced in [51]. Thus, power consumption of a circuit could be reduced without a compromise to gain, linearity, and other parameters which are directly related to transconductance.

Figure 2.12(a) shows a single NMOS device (M_1) which has an aspect ratio of W/L with drain current I. With these dimensions, M_1 transconductance is gm. On the other hand, drawn in figure 2.12(b) are two NMOS transistors which are connected in parallel (M_2, M_3). Their aspect ratio is half of M_2 hence, half M_1 current flows in each ($I/2$), but total current flowing through the compound is I. In this case, equivalent transconductance of the compound is $g_{m2,3} = g_{m2} + g_{m3} = g_m$. Therefore, both configurations in figure 2.12(a) and figure 2.12(b) are equivalent. In figure 2.12(c) one of the NMOS transistors was substituted by PMOS (device M_4). Both transistors M_4 and M_5 have same dimensions as of figure 2.12(b). The equivalent compound transconductance is the same as in previous cases $g_{m4,5} = g_{m4} + g_{m5} = g_{m2,3} = g_m$, but in this

case total current is half, as the same current flows through both transistors. The input capacitance is nearly equal to M_1 input capacitance.

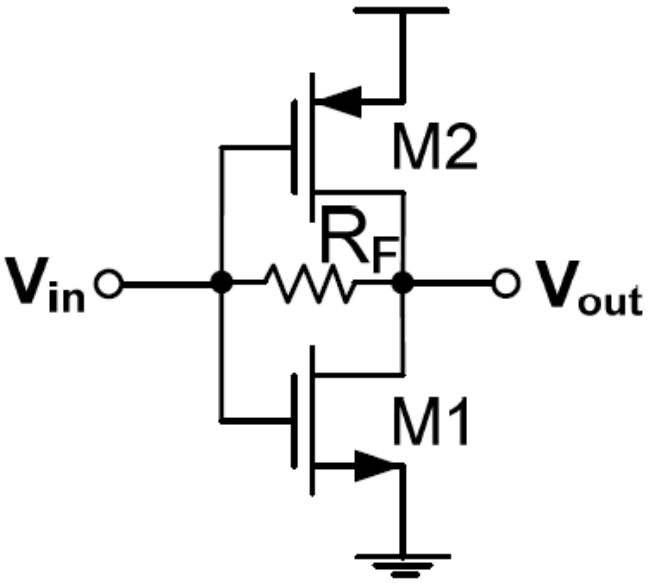


Figure 2.13: Resistive feedback current reuse configuration

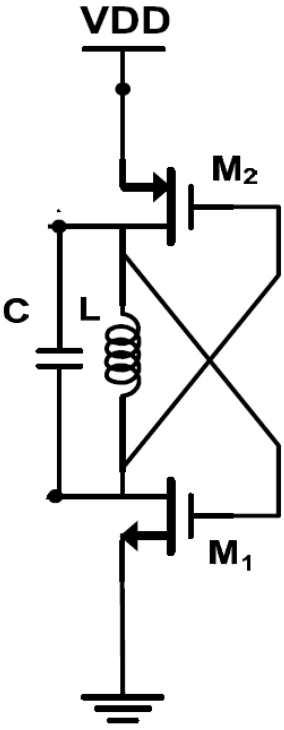


Figure 2.14: Current reuse VCO [53]

The current reuse principle could be applied to any active circuit because of its simplicity. It became popular technique for the power saving. The resistive feedback current reuse configuration, shown in figure 2.13, has been widely used in modern receivers either as front-end LNAs or baseband amplifiers [3], [9], [10], and [52]. The CMOS VCO circuit employs both NMOS and PMOS cross-coupled pairs act as the negative impedance to sustain LC tank oscillation, shown in figure 2.14, is using the current reuse

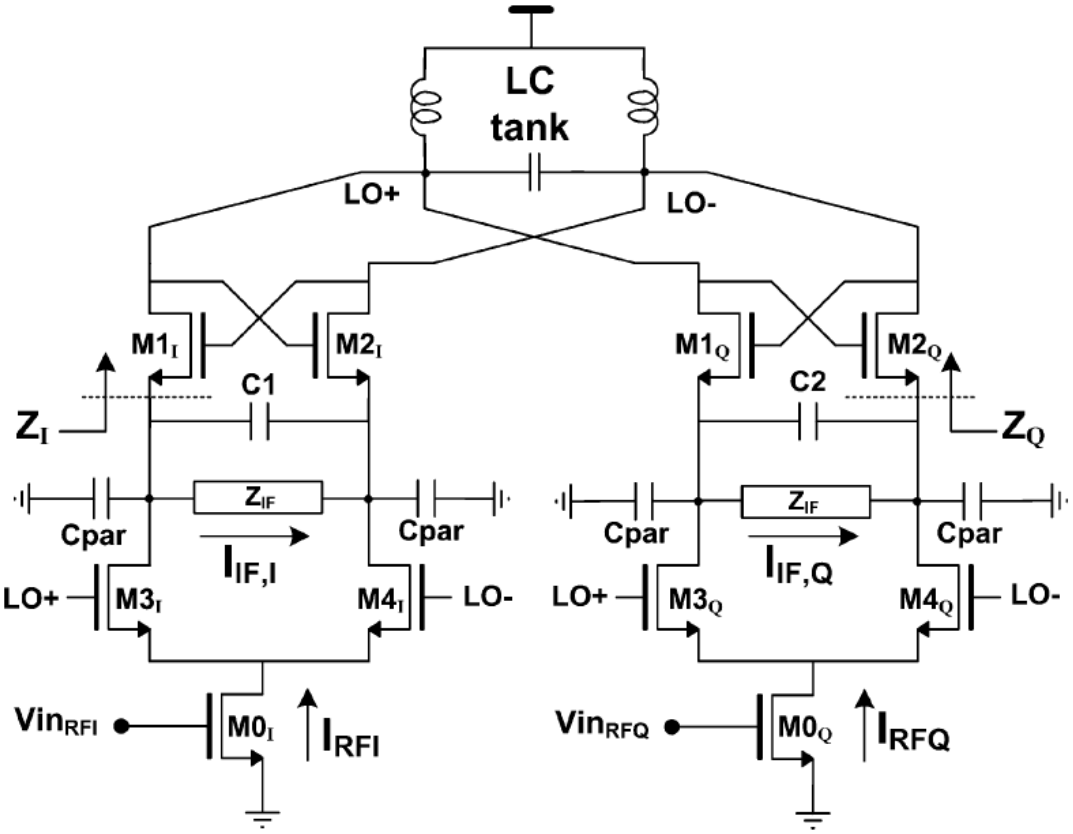


Figure 2.15: Single *LC* tank quadrature LMV cell [54]

technique to achieve a better phase noise at the same power consumption as conventional LC VCO which are employing only either NMOS or PMOS [53].

The current reuse technique has been extended to recycle currents from one building block to another. It also known as blocks stacking or cascoding. A typical, well-known, and popular application is the single stage receiver frontend called LNA-Mixer-VCO (LMV) cell which had been firstly introduced in [54], as shown in figure 2.15. The LNA, mixer and VCO are sharing same devices which play double role, one at the RF and one at the IF, without introducing any conflicts between the two domains. For example, transistors M_0 act as a LNA at RF, while providing a DC bias current to VCO, or similarly M_1 – M_2 perform mixing task while contributing – together with capacitance C_2 – to VCO operation at RF. Therefore, several contradicting tasks have been successfully merged: the current reuse, reduction of device

count, the multiple functionality with no spurious interactions, and compatibility with the low supply voltage.

2.5.6.3.4. Reduced supply voltage

The power consumption is directly proportional to supply voltage ($P = V.I$). Transistors' transconductance is the main circuit parameter affecting the circuit metrics. For a given transconductance value produced through a given current budget which flows into transistors, the supply voltage can be decreased to reduce the power consumption of the circuit while preserving the design requirements.

2.6. Summary

Power consumption of WSN nodes is the major constraint to address in such applications. Continuous research is ongoing to develop efficient energy harvesting units capable of sustaining an independent supply sources for nodes in WSN applications. In parallel, low power radios are investigated to develop a power efficient RF modules can operate from the new harvesters once enabled. Many techniques presented in this chapter on different layers, starting from PHY layer up to the very high level layer of application, can be brought up together to help in developing the next generation of low power radios.

Chapter 3 : System Design

This chapter focuses on the BT5.1/BLE receiver system design based on the literature survey presented in the previous chapter to derive the specs of building blocks.

The proposed BT5.1/BLE receiver operates in two modes; low power, and high performance. In the low power mode, mixer down-converts RF signal using third harmonic of LO to compensate for the impact of I/Q, necessary for low-IF architecture adopted, LO generation on power consumption while normally down-converts RF signal using fundamental LO component in high performance mode. The receiver incorporates a configurable integrated matching circuit to adapt input impedance change between the two modes due to 4-phase passive mixers transparency at the front end. The mixer first architecture allows LNA to operate at IF, unlike conventional LNA first architecture where LNAs are at RF and hence require high power consumption. A configurable complex filter permits both BT5.1 and BLE operation in both receiver modes. Software at the top layer can drive the PHY layer to either mode or wireless standard. The proposed receiver utilizes reduced supply voltage and current reuse which enable achieving required transcondactunce, g_m, to meet specs of building blocks while at effective low power.

3.1. Receiver Architecture

Receiver architecture choice depends on:

1. Radio frequency
2. Modulation scheme
3. Required Signal to Noise Ratio, SNR, and interference ratio
4. Process technology
5. Application

Direct conversion and low-IF architectures are the most common receiver architecture for low power applications while preserving target system specifications. Both architectures offer high level of integration which helps in meeting low cost requirement of WSN applications. Flicker noise has severe impact on direct conversion architecture where its corner frequency falls in the range of tens or even hundreds of megahertz in current CMOS technologies. DC offsets generated by 1) LO leakage and self-mixing, 2) second order nonlinearity, 3) systematic and random process mismatches saturate the baseband circuits and hence prohibit signal detection. Direct conversion receivers have no image frequency.

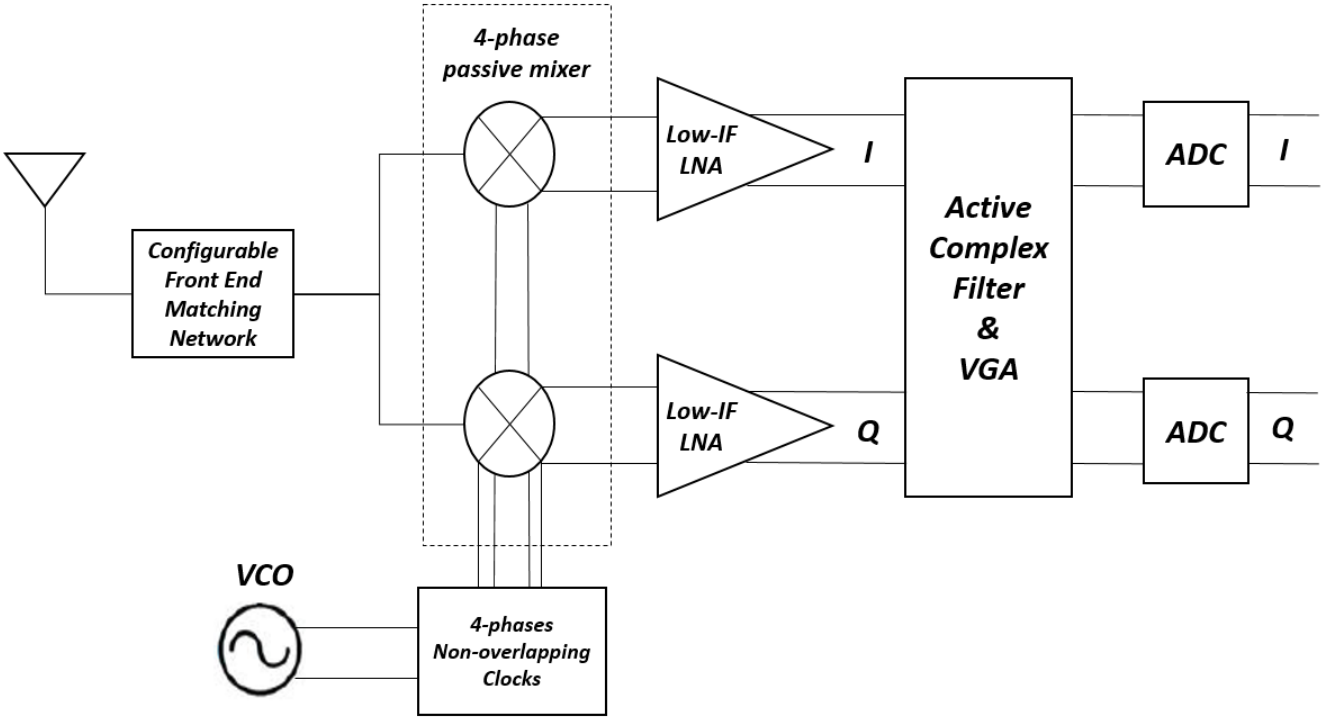


Figure 3.1: Receiver architecture

Low-IF architecture avoids direct conversion architecture issues. Although low-IF architecture has image frequency, it relaxes the required image rejection much more than conventional heterodyne architectures. Moreover, narrowband standards for WSN like Bluetooth, BLE, ZigBee, etc have more relaxed adjacent channel interference tolerance which reduces the image rejection specification.

Therefore low-IF architecture is favored for Bluetooth and BLE standard compliant receivers implemented in CMOS process. Figure 3.1 shows the receiver architecture.

3.2. Receiver system design

Understanding the system and pinpointing the power saving features, is the key to design an optimum low power receiver. A summary of the Bluetooth5.1 and BLE target specifications is shown in Table 3.1. Although Bluetooth/BLE specifications have relaxed sensitivity levels of -70 dBm, earlier research works and industry are pushing this level to much lower values, below -90 dBm.

3.2.1. Noise Figure (NF):

To get the required NF for the receive chain; the required Signal-to-Noise ratio (SNR) at the demodulator input to achieve the Bit Error Rate mentioned in Table 3.1 should be obtained.

Table 3.1: BLUTOOTH5 AND BLE TARGETED SPECIFICATIONS SUMMARY

	Bluetooth5.1	BLE
Frequency band (MHz)	2400 – 2483.5	
Number of channels	79	40
Channel Spacing (MHz)	1	2
Image frequency Interference, C/I_{image} (dB)	– 9	
Data rate (Mbps)	Up to 3	Up to 1
Modulation scheme	GFSK, π/4-DQPSK, 8DPSK	GFSK
Sensitivity (dBm)	– 70	
Maximum Usable Level (dBm)	– 20	– 10
Bit Error Rate (BER)	0.1 %	

K : Boltzmann's constant *T_o : Room Temperature in Kelvin (300k)*

$$\textit{Noise Factor (F)} = \frac{SNR_i}{SNR_o} = \frac{S_i}{N_i} \cdot \frac{N_o}{S_o}$$

$$= \frac{S_i}{K\, T_o\, BW} \cdot \cdot \frac{1}{SNR_o} \qquad (3.1)$$

$$\textit{Noise Figure (NF)} = 10\, log_{10}(F) = S_i\ (dBm) + 174\ (dBm)$$

$$- 10\, log_{10}\, BW - SNR_o\ (dB) \qquad (3.2)$$

where $N_{i_{dBm}} = (K\, T_o\, BW)_{dBm} = -174\ dBm + 10\, log_{10}\, BW$

Ni represents the noise input to the circuit from a 50Ohm antenna, under impedance matching conditions. This is so called *Noise floor*. Thus, for a specific receiver (specific NF), as the input signal power increases, the output SNR increases. Therefore, the worst case output SNR occurs at the minimum input signal power (receiver sensitivity), since the receiver NF is constant versus input power. Noise Figure should be calculated at this worst case scenario.

$$SNR_{o_{min}} = (\frac{S_o}{N_o})_{min} = \frac{G_{RX} \cdot S_{i_{min}}}{N_{generated} + G_{RX} \cdot N_i} \qquad (3.3)$$

As mentioned above, proposed Bluetooth/BLE receivers in the literature had pushed the sensitivity level to values better than *– 90 dBm*, although the standard defines much more relaxed levels, *– 70 dBm.* This work targets sensitivity level of *– 94 dBm.*

For FSK modulation scheme:

$$BER = \frac{1}{2} e^{\frac{-1}{2} SNR} \qquad (3.4)$$

Then the Signal to Noise Ratio, SNR, will be 11 dB for 10^{-3} BER.

On the other hand, according to [55] and [56], the SNR is about 9 dB and 17.5 dB for 10^{-3} BER in case of π/4-DQPSK and 8DPSK modulation schemes respectively.

Substituting into (3.2) to get the required noise figure for BLE and each modulation scheme of BT5.1:

$$NF_{BLE,\ 2M} = -94 + 174 - 10\ log_{10}(2\ x\ 10^6) - 11 = 6\ dB \qquad (3.5)$$

$$NF_{BLE,\ 1M} = -94 + 174 - 10\ log_{10}(1\ x\ 10^6) - 11 = 9\ dB \qquad (3.6)$$

$$NF_{BT5,\ GFSK} = -94 + 174 - 10\ log_{10}(1\ x\ 10^6) - 11 = 9\ dB \qquad (3.7)$$

$$NF_{BT5,\ \pi/4-\mathrm{DQPSK}} = -94 + 174 - 10\ log_{10}(1\ x\ 10^6) - 9 = 11\ dB \qquad (3.8)$$

$$NF_{BT5,\ 8\mathrm{DQPSK}} = -90 + 174 - 10\ log_{10}(1\ x\ 10^6) - 17.5 = 6.5\ dB \qquad (3.9)$$

A noise figure of 6 dB is targeted to achieve up to 2 Mbps data rate and better than *– 94* dBm sensitivity level for BLE, whereas for BT5.1, up to 3 Mbps data rate and *– 90* dBm sensitivity level.

3.2.2. Receiver Gain:

Since the receiver dynamic ranges for BT5.1 and BLE are 70 dB and 84 dB respectively, one receiver gain stage cannot be used. This is the reason a variable gain amplifier, VGA, with multiple gains to relax the dynamic range required from the succeeding block (demodulator). An additional modification to relax the steps of the VGA is to switch off the LNA and replace it with an attenuator at higher input power levels. At such levels, the input SNR is very high reducing the importance of having an LNA or to reduce the overall receiver NF.

Assuming the Analog-to-Digital, ADC, or demodulator input dynamic range ranges from -10 dBm to 2 dBm. This corresponds to 0.4 V_{pp} differential to 0.8 V_{pp} differential in a 50Ohm resistor for a 0.7 V supply system. So the maximum gain and minimum gain can be calculated:

$$G_{min.} = \text{min. Required chain output} - \text{min. Input power}$$

$$= -10 - (-94) = 84 \quad (3.10)$$

$$G_{max.} = \text{max. Required chain output} - \text{max. Input power}$$

$$= 2 - (-20) = 22 \quad (3.11)$$

This wide dynamic input power range requires gain distribution over the receiver chain building blocks. The VGA steps will be exercised across the different input power levels.

3.2.3. Linearity (Third order Input Intercept Point IIP_3):

Bluetooth5.1 and BLE standards define a two tone test to measure the receiver IIP_3. According to the standard, the actual sensitivity performance, BER is less than or equal to 10^{-3}, shall be met under the following conditions:

I. The wanted signal shall be at a frequency f_0 with a power level 6 dB over the reference sensitivity level.
II. A static sine wave signal shall be at a frequency f_1 with a power level of –50 dBm.
III. An interfering signal shall be at a frequency f_2 with a power level of – 50 dBm.

IV. When receiving with 1 Msym/s modulation, frequencies f0, f1 and f2 shall be chosen such that $f_0 = 2f_1 - f_2$ and $|f_2 - f_1| = n * 1$ MHz, where n can be 3, 4, or 5.

V. When receiving with 1 Msym/s modulation, frequencies f0, f1 and f2 shall be chosen such that $f_0 = 2f_1 - f_2$ and $|f_2 - f_1| = n * 2$ MHz, where n can be 3, 4, or 5.

VI. The receiver shall fulfill at least one of the three alternatives (n=3, 4, or 5); different modulation schemes can use different alternatives.

In order to have an output *SNR* larger than $SNR_{o,\ min.}$, the sum of the IM3 product and the $SNR_{o,\ min.}$ must be lower than the sensitivity plus the margin, Δ. This leads to a maximum IM3 given by N_{floor} + Δ; thus the entire chain minimum IIP3 is equal to:

$$IIP_3 = \frac{1}{2}(3P_{\text{interferer}} - IM_3)$$

$$= \frac{1}{2}(3P_{\text{interferer}} - N_{floor} - \Delta)$$

$$= \frac{1}{2}(3(-50) - (-174 + 60 + 6) - 6)$$

$$= -24\ dBm \qquad (3.12)$$

The foregoing IIP_3 derivation is due to adjacent channel interferers specified by Bluetooth5.1 and BLE standards, called out of channel IIP_3. The 1 dB compression point could be derived given the IIP_3, assuming the whole receiver is modeled as a nonlinear system having a transfer function of $y = \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3$ as follows:

$$IIP_3 = \sqrt{0.145\ \left|\frac{\alpha_1}{\alpha_3}\right|} \qquad (3.13)$$

$$A_{1dB} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}$$

$$= -28.82\ dBm \qquad (3.14)$$

Where α_1 is the first order signal component gain and α_3 is the third order signal component gain.

3.2.4. Linearity (Second order Input Intercept Point IIP_2):

Bluetooth5.1 and BLE standards have no definition for a two tone test to measure the receiver IIP_2. However, the worst case scenario could be considered as follows: two in band blockers with a power level of -50 dBm placed at 3 MHz and 6 MHz from the wanted channel with a power level 6 dB over the reference sensitivity level [57]. Thus the entire chain minimum IIP_2 is equal to:

$$\begin{aligned} IIP_2 &= 2P_{\text{interferer}} - IM_2 \\ &= 2P_{\text{interferer}} - N_{floor} - \Delta \\ &= 2(-50) - (-174 + 60 + 6) - 6 \\ &= +2\ dBm \end{aligned} \tag{3.15}$$

The derived value is definitely below the IIP_2 achievable for the whole receiver with any architecture. Differential building blocks can achieve much more than the derived value since the differential signals eliminate second order components except for an amount of mismatch between them resulting from process variations and errors among matched devices.

3.3. Summary

The receiver system design applies for both the two modes of operation and both BT5.1 and BLE standards. Low-power mode relaxes the noise figure requirement at the cost of lower sensitivity levels for various BT5.1/BLE data rates. Table 3.2 summarizes the system level and receiver building blocks specifications.

Table 3.2: RECEIVER SYSTEM LEVEL SPECIFICATIONS

	System Level Specs		Mixer		Low-IF LNA	Filter & VGA	Matching Network	
	Low-power mode	High-performance mode	Low-power mode	High-performance mode	Both modes	Both modes	Low-power mode	High-performance mode
Noise Figure (dB)	12.3	6	12	2	7	10	3	
In Band IIP3 (dBm)	−24		+5		−10	−3	+40	
IIP2 (dBm)	+2		+5		+20	+30	+40	
Power (µw)	600	1200	150 (for VCO, divider, buffers)	750 (for VCO, divider, buffers)	250	200	-	
Gain (dB)	48/81	55/88	3		28	20 to 55	2	10
Sensitivity	−91.5 dBm	−94 dBm						
Data Rate	1Mbps or 2Mbps							
Phase Noise	−102 dBc/Hz @ 2.5MHz							
Image Rejection Ratio	More than 21 dB							
Out Band (OB) IIP3	−30 dBm							
Receiver Architecture	Low IF mixer first receiver							
Standard	BT5.1/BLE							
Technology	65 nm							

Chapter 4 : Receiver Design

This chapter focuses on the receiver circuit design and techniques for low power operation and flexible configurability to operate either in high-performance mode or low-power mode both meeting BT5.1 and BLE standards specifications. In addition, four-phases passive mixer analysis based of Linear Time Variant, LTV, and Linear Time Invariant, LTI, models will be reviewed for fundamental LO component. The analysis is extended to explain harmonic down-conversion properties of passive mixers and discuss the benefits and drawbacks as well.

4.1. Background and motivation

Bluetooth technology is a short range, robust, low power, low cost, and widely customizable communication system aiming to connect various fixed and portable devices. Since earlier Bluetooth specification releases, it has been adopted in many applications due to its key features. Moreover, Bluetooth Low Energy (BLE) has been introduced for the first time in the fourth release of Bluetooth standard. Bluetooth/BLE operates in the same 2.4GHz ISM radio band as *IEEE 802.11b/g/n/ax* (WiFi) and *IEEE 802.15.4* (ZigBee).

Although Bluetooth has relaxed specifications, ultra-low power receivers, achieving sub-mW, are still a challenging task. Power-hungry blocks, like VCO, usually defines a lower limit for power performance.

4.2. Receiver Architecture

Figure 4.1 shows the proposed receiver architecture. It has a configurable front end matching circuit that interfaces the mixer core to the antenna. This provides impedance transformation for both modes since the input impedance of passive mixers depends on the mode of operation. The low-power mode utilizes down-converting the RF signals by the third harmonic component of the LO. The high-performance mode uses the fundamental component of the LO to down-convert the RF signals. In addition, the proposed design offers passive voltage gain to improve the overall sensitivity. A 4-phases passive mixer is directly following the matching circuit driven by 25% duty cycle non-overlapping clocks. The 4-phases passive mixer is chosen as a compromise between the power consumption of the low-power mode operation and the

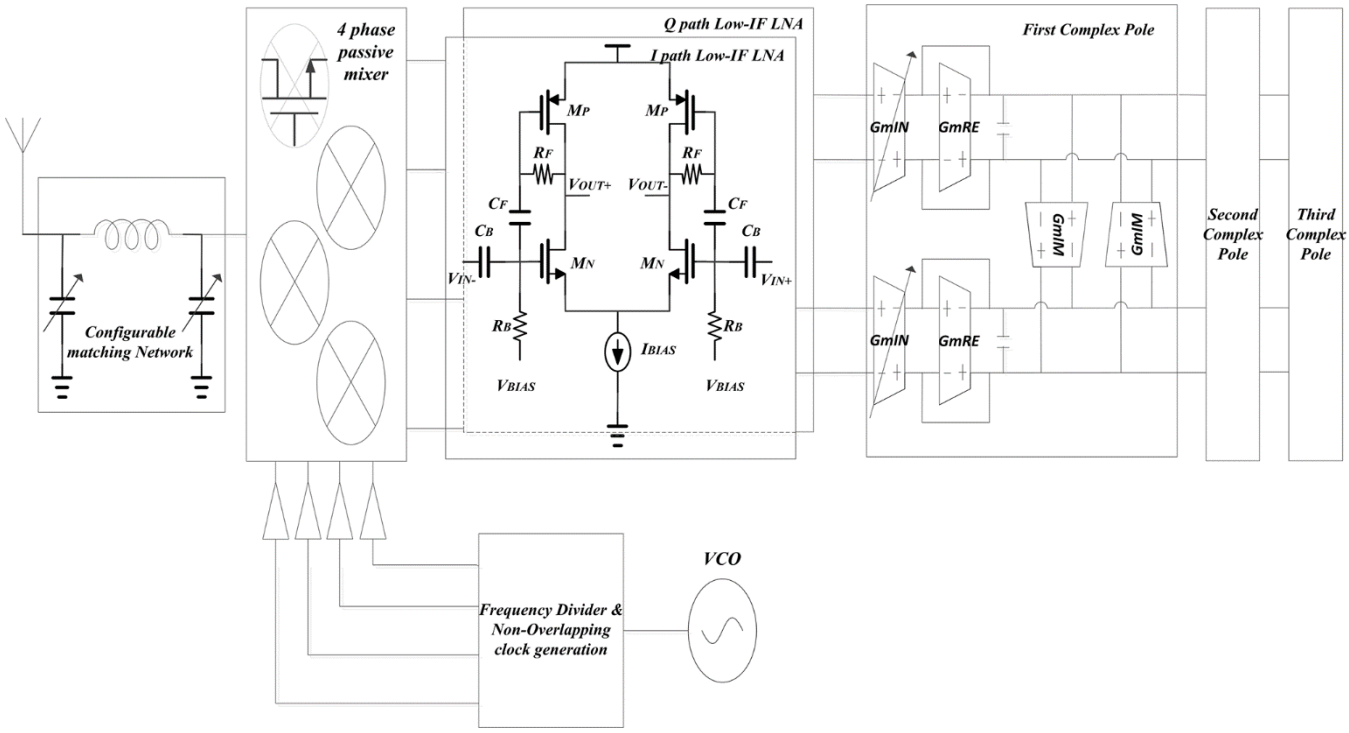


Figure 4.1: Proposed receiver architecture

noise performance of the high-performance-mode operation. Figure 4.2 shows the tradeoffs in terms of the estimated receiver figure of merit (FOM $= -P_{sensitivity} - 10\log\frac{P_{DC}}{Data\ Rate}$) against the number of mixer phases [52].

The simplest 2-phases structure has superior power consumption at the expense of image rejection and poor noise performance. On the other hand, the power consumption dramatically increases as the number of the passive mixer phases increases because:

1) The RX paths following the passive mixer are duplicated.

2) The VCO runs at a higher frequency than the RF signal, 4x and 8x for 8-phases and 16-phases respectively.

3) The higher order and complex frequency dividers following the VCO are operating at high frequencies.

4) The LO drivers are loaded by larger capacitances of the mixers' gates.

The 8 and 16-phases structures provide larger input impedance. Consequently they provide better impedance matching capability for both modes of operation, even with a very low mixer ON resistance, without the need for a matching circuit. In addition, they achieve better NF than the 4-phases structure, although the NF improvement is small in the range of few GHz LO frequencies [58].

The The differential in-phase and quadrature mixer outputs are then applied to a Low-IF LNA. A third-order bandpass complex filter combines the in-phase and quadrature-phase signals to attenuate interferers at adjacent channels and reject the image.

Two controlled VCO cores are used to generate the desired LO signal for each mode of operation separately. One core is operating at almost twice the frequency of the received signal. Then it is followed by a frequency divider by two and non-overlapping clocks generator to provide both the I and Q LO near the received signal frequency, separated by IF of 10 MHz to avoid flicker noise. The wanted RF signal is down-converted normally by fundamental component. The other VCO core on the other hand operates near two-third of the received signal frequency, similarly for the frequency divider to divide the frequency by two. Then the desired RF signal is down-converted by the third harmonic of the LO.

Passive mixer sizing should compromise among different tradeoffs such as: the input impedance seen by the matching circuit at the RF input port of the mixer, the noise generation of the mixer, and the input capacitance seen by the frequency divider and the buffers at the LO port of the mixer.

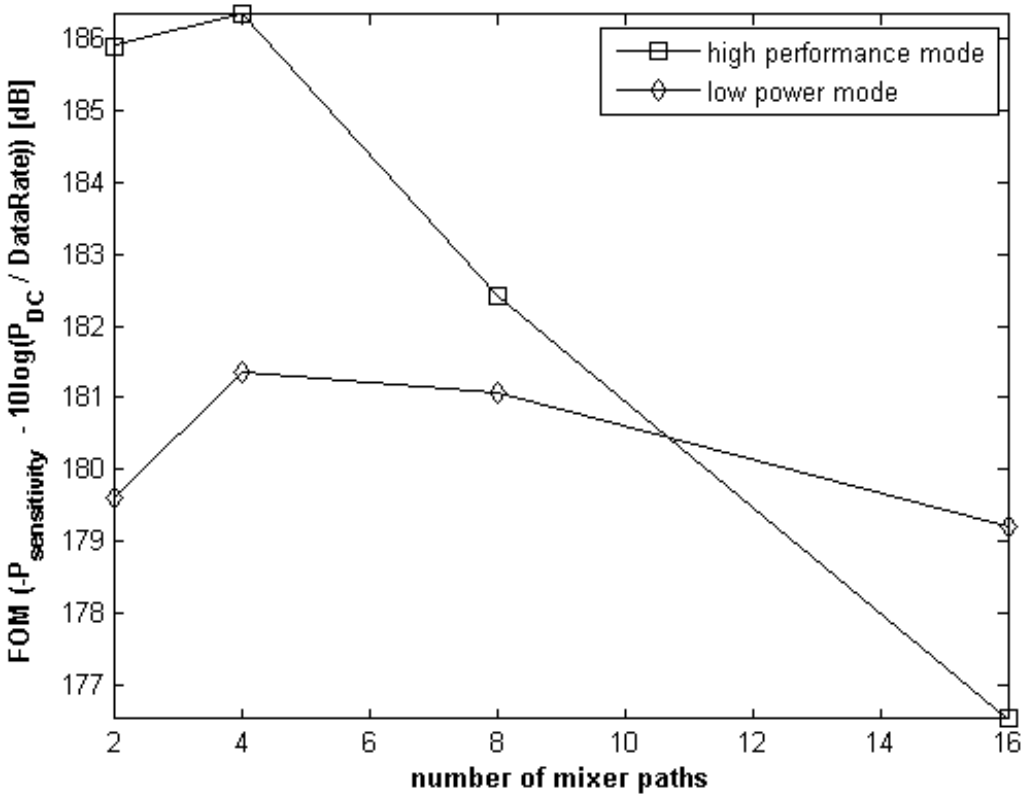


Figure 4.2: Estimated FOM against number of passive mixer phases

4.3. Receiver circuit design

4.3.1. Integrated Front End Matching Circuit

A configurable matching circuit is required to adopt the two modes of operation. As will be discussed in the passive mixer analysis, the impedance transform term, γ, and shunt resistance R_{sh} are highly dependent on the LO harmonic component of interest. Consequently, they change the input impedance seen at the RF port of the mixer in the two modes.

Figure 4.1 shows a pi matching circuit topology used with variable inductor and capacitors to achieve matching in the two operation modes. In the high-performance mode, the matching circuit provides about 6-dB passive voltage gain. Therefore, it helps in improving the overall receiver sensitivity. In the low-power mode, the imaginary component of the input impedance seen at the RF port of the mixer is scaled down to a small term and varies slowly across the band, as will be shown later. Thus, it gives a better opportunity for good matching within the entire band.

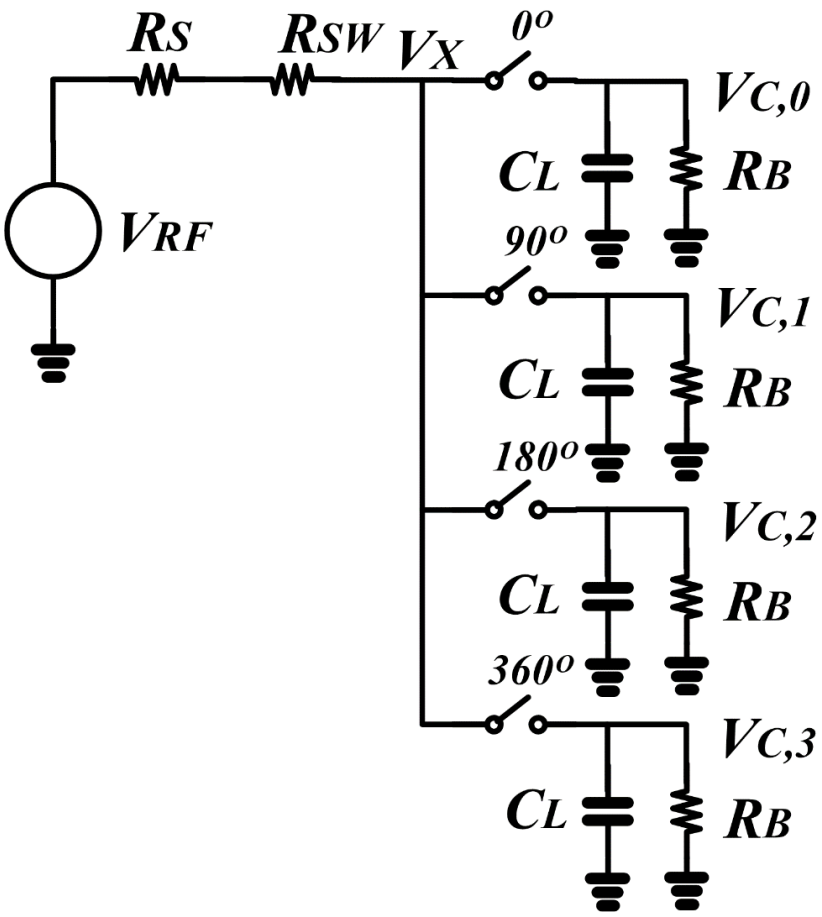


Figure 4.3: Four-phases passive mixer configuration model loaded by sampling capacitors and resistors [61]

4.3.2. Four-Phases Passive Mixer

Traditionally, LNAs were usually used as the first active RF block in receiver chains providing a gain stage with minimum added noise. Operating at high frequency; wide bandwidth; and low noise, LNAs consume considerable power of the total receiver power budget [35]. The mixer-first architecture defers the LNA to an IF, or baseband. Therefore, it reduces the power consumption and bandwidth requirements. The mixer-first architecture has been first introduced in [59].

In the literature, several articles have been done for analyzing, designing, and optimizing passive mixers [40], [41], [58 – 65]. They show competitive noise performance and matching compared to the conventional LNA-first receiver architecture. Moreover, the passive mixer-first receivers provide a high-Q filtering at the front end without the need for external, bulky, and costly RF filters such as Surface Acoustic Wave filters (SAW) [60].

Although they are simple in structure, they have been used along with the baseband amplifiers to realize the complete receiver chain as proposed in [65].

In this work, the same 4-phase passive mixer analysis methodology, presented in [61], is followed to construct the simple Linear Time Invariant (LTI) model at the *n-th* order harmonic frequency of the LO. Figure 4.3 shows the simplified circuit model of the 4-phases passive mixer.

In the Linear Time Variant, LTV, circuit of figure 4.3, starting from the charge conservation law, the accumulated charge during each LO phase through antenna resistance and the mixer switching resistance R_{sw}, $R'_a = R_a + R_{sw}$, equals to the dissipated charge through R_B

$$Q_m = \frac{V_{c,m}\, T_{LO}}{R_B} = \int_{m\frac{T_{LO}}{4}-\frac{T_{LO}}{8}}^{(m+1)\frac{T_{LO}}{4}-\frac{T_{LO}}{8}} \frac{V_{RF}(t)-V_{c,m}}{R'_a}\, dt \qquad (4.1)$$

Given that RF signal is located at any harmonic of the LO, then

$$V_{RF}(t) = \mathrm{A}\cos(\mathrm{n}\omega_{LO}\mathrm{t} + \Phi) \qquad (4.2)$$

And assuming $V_{c,m}$, baseband signals on the output capacitors, is at steady state, A(t) and Φ(t) are varying slowly relative to $R'_a C_L$ and $R_B C_L$ time constants, then substituting (4.2) into (4.1)

$$V_{c,m} = \begin{cases} \frac{2\sqrt{2}}{\pi}\frac{R_B}{R_B+4R'_a}\frac{1}{n}\,\mathrm{A}\cos\left(\frac{mn}{2}\pi + \Phi\right) & n = 1,3,9,11,\ldots \\ -\frac{2\sqrt{2}}{\pi}\frac{R_B}{R_B+4R'_a}\frac{1}{n}\,\mathrm{A}\cos\left(\frac{mn}{2}\pi + \Phi\right) & n = 5,7,13,15,\ldots \end{cases} \qquad (4.3)$$

A virtual voltage for each LO harmonic is defined by $V_{x,n}$. Assuming non-overlapping clocks, $V_{x,n}$ is always connected to only one output capacitor at a

time, thus $V_{x,n}$ could be found by the up-conversion of baseband signals on the output capacitors

$$V_{x,n} = \frac{V_{c,0} - V_{c,2}}{2} V_{LO}(\mathrm{n}\omega_{LO}\mathrm{t}) + \frac{V_{c,1} - V_{c,3}}{2} V_{LO}(\mathrm{n}\omega_{LO}\mathrm{t} + \frac{\pi}{2}) \qquad (4.4)$$

Using Fourier transform of 25% clocks and substituting from (4.3) into (4.4)

$$V_{x,n} = \frac{8}{(n\pi)^2} \frac{R_B}{R_B + 4R'_a} \mathrm{Acos}(\mathrm{n}\omega_{LO}\mathrm{t} + \Phi) \qquad (4.5)$$

To compute the input impedance seen from the RF port of mixer, the input current is first calculated

$$I_{A,n}(\mathrm{t}) = \frac{V_{RF}(t) - V_{x,n}(t)}{R'_a}$$

$$= \frac{4R'_a + (1 - \frac{8}{(n\pi)^2})R_B}{R_B R'_a + 4{R'_a}^2} V_{RF}(t) \qquad (4.6)$$

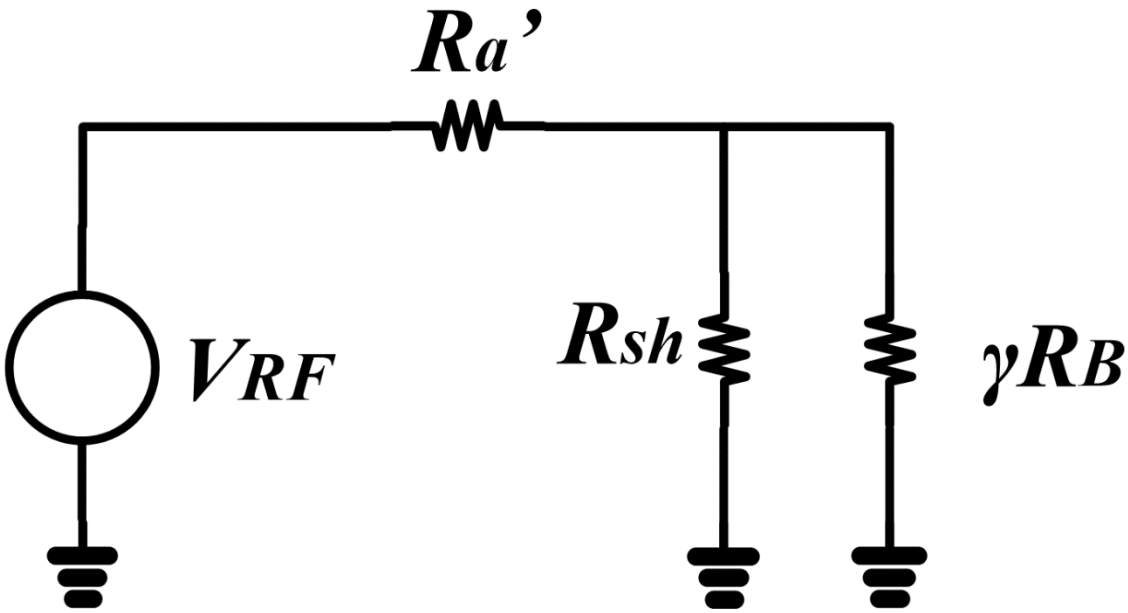
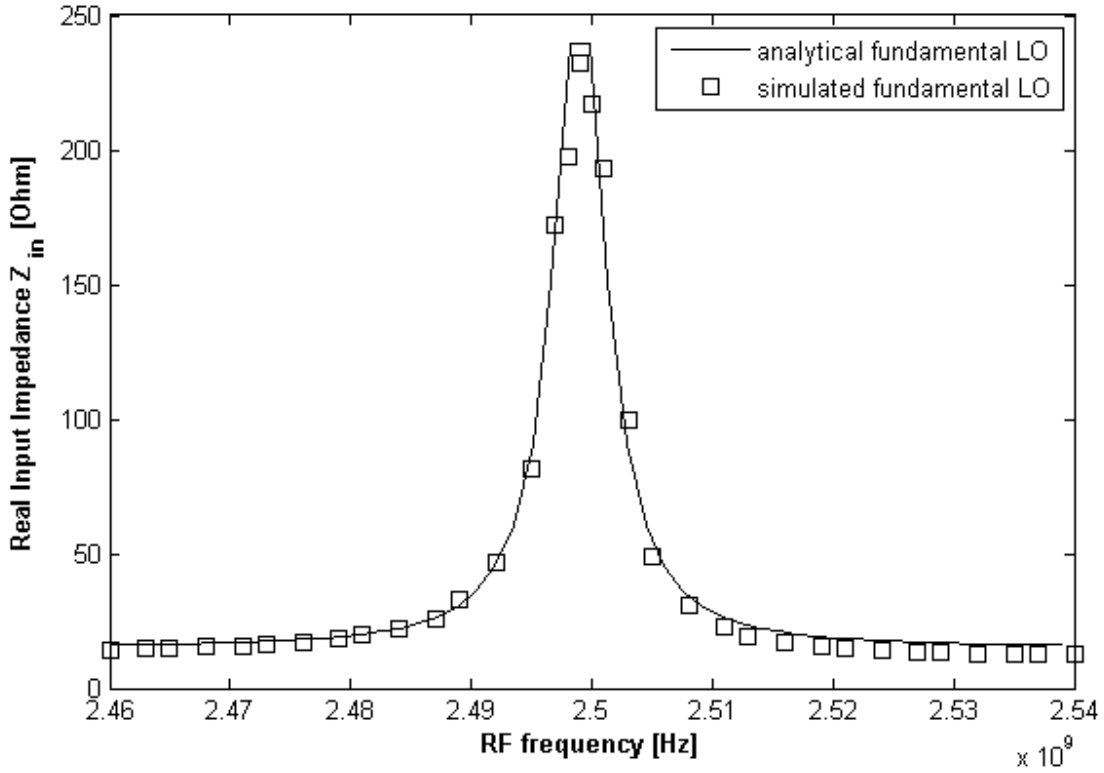


Figure 4.4: Simplified 4-phases passive mixer configuration LTI model

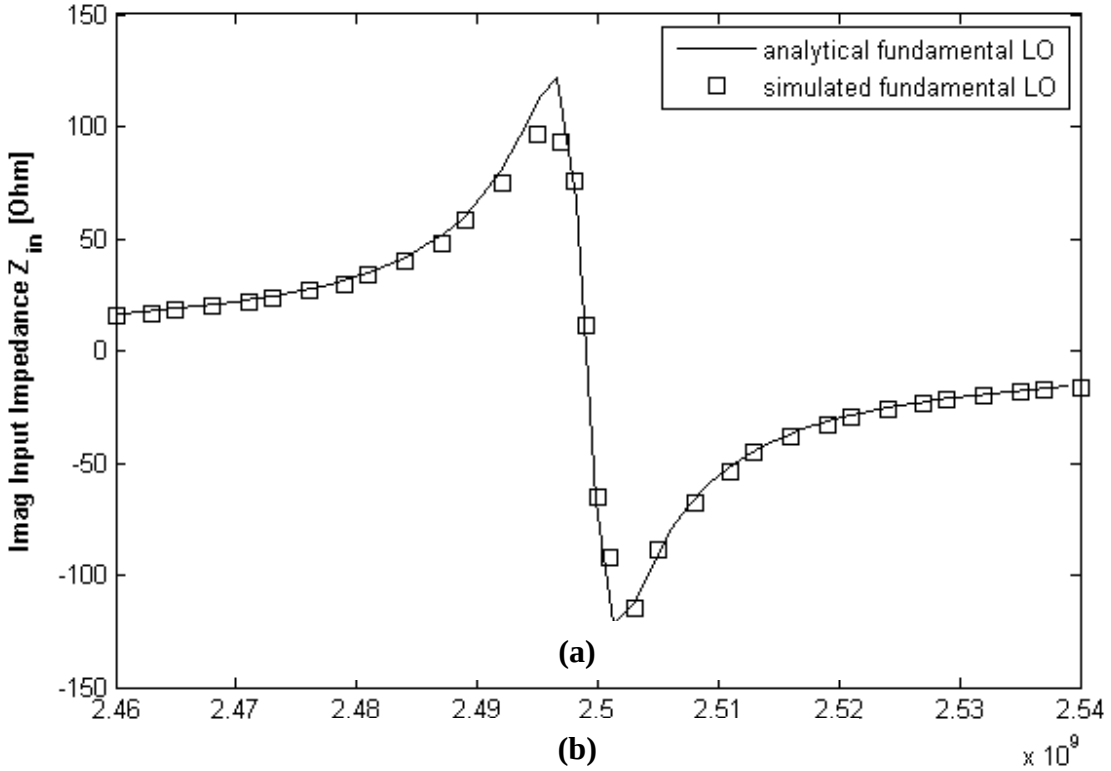
From the LTI model shown in figure 4.4, the current is obtained as

$$I_{A,n} = \frac{\gamma R_B + R_{sh}}{\gamma R_B R'_a + R_{sh} R'_a + \gamma R_B R_{sh}} V_{RF} \qquad (4.7)$$

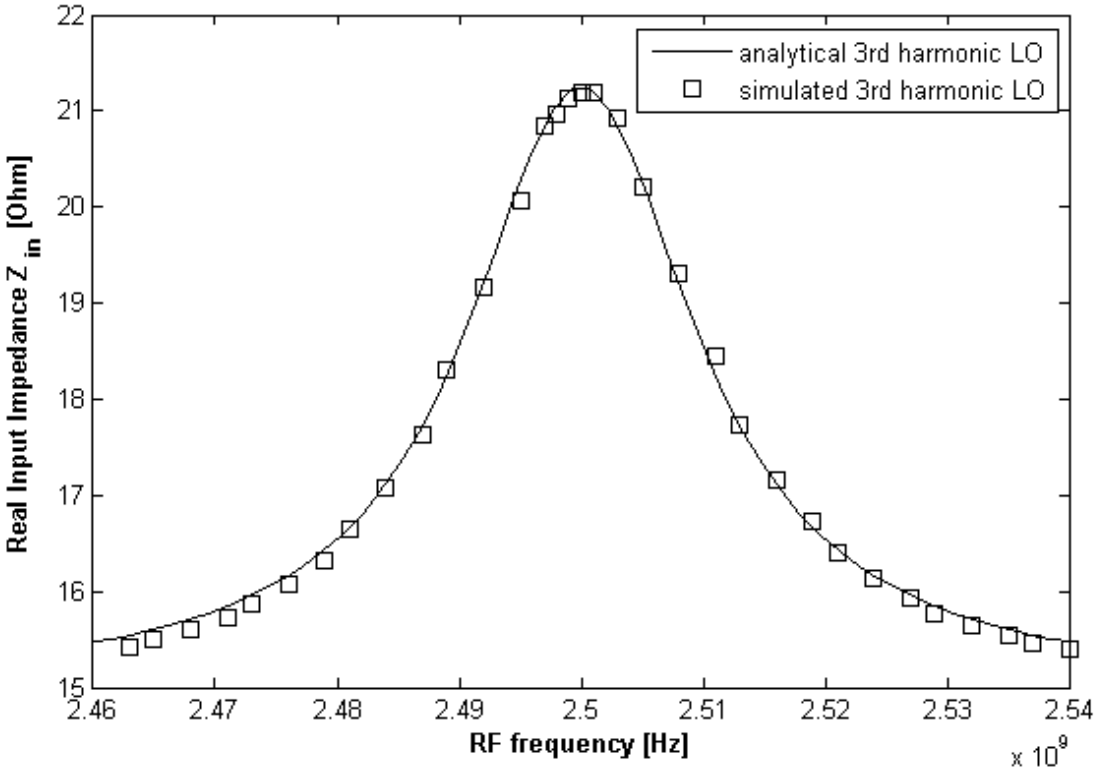
Where R_{sh}, is a virtual shunt resistance γ is a scaling factor.


analytical fundamental LO
simulated fundamental LO
Real Input Impedance Z_{in} [Ohm]
RF frequency [Hz]
x 10^9
250
200
150
100
50
0
2.46
2.47
2.48
2.49
2.5
2.51
2.52
2.53
2.54

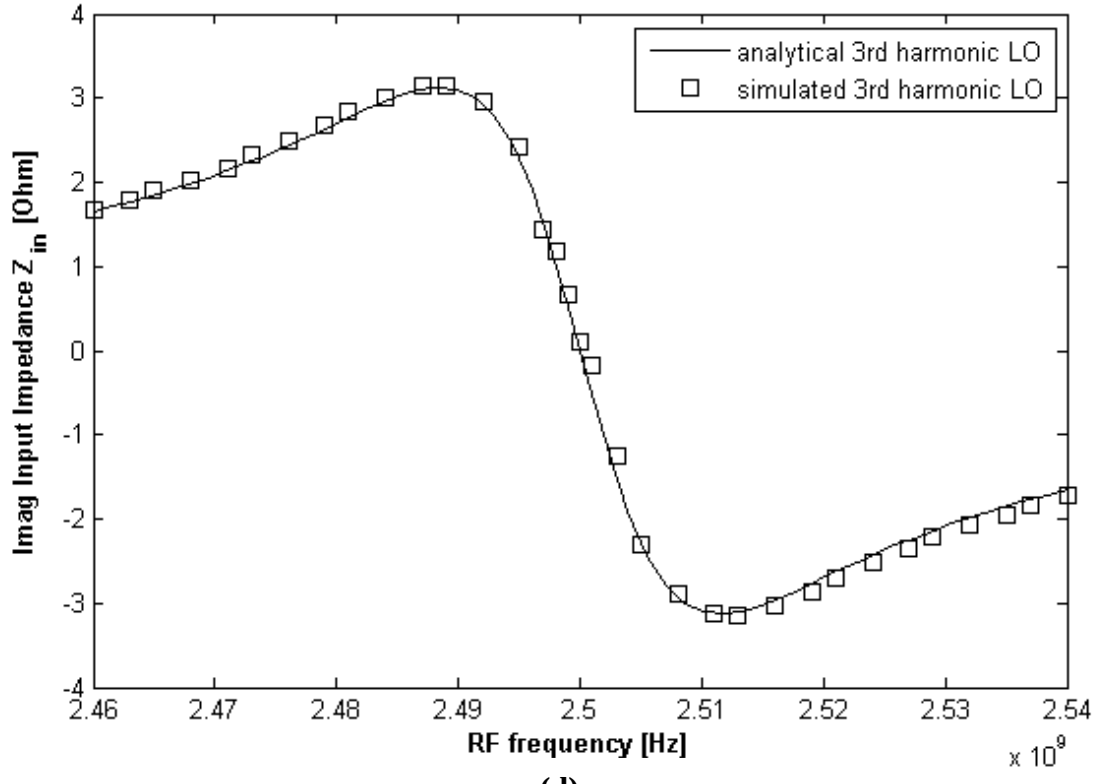
(a)


analytical fundamental LO
simulated fundamental LO
Imag Input Impedance Z_{in} [Ohm]
x 10^9
150
100
50
0
-50
-100
-150
2.46
2.47
2.48
2.49
2.5
2.51
2.52
2.53
2.54

(b)

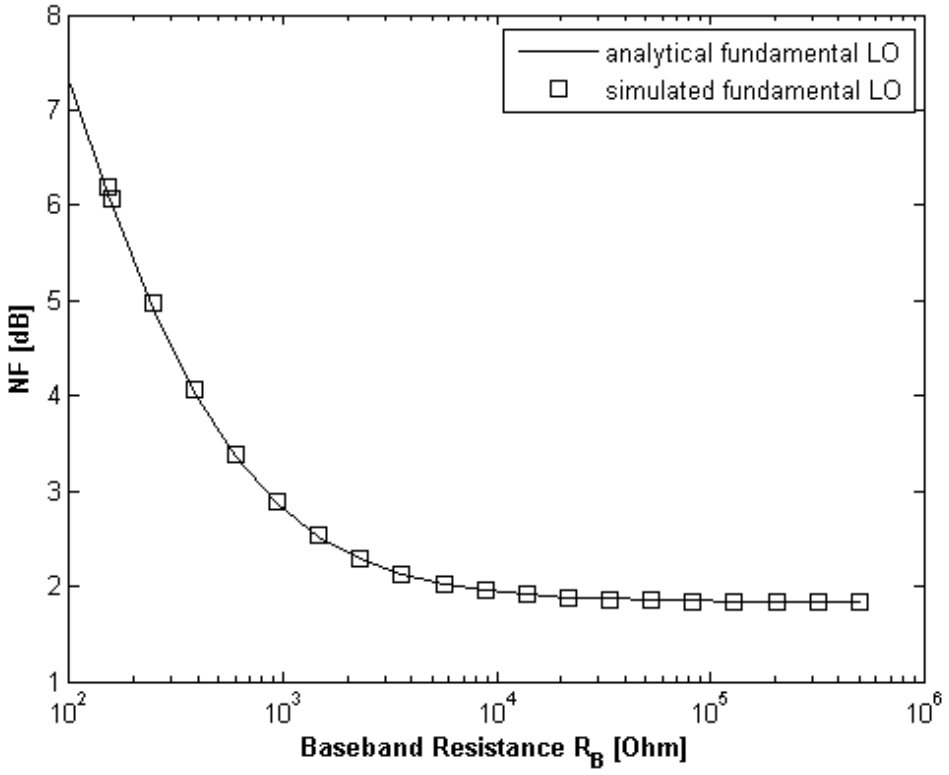


(c)

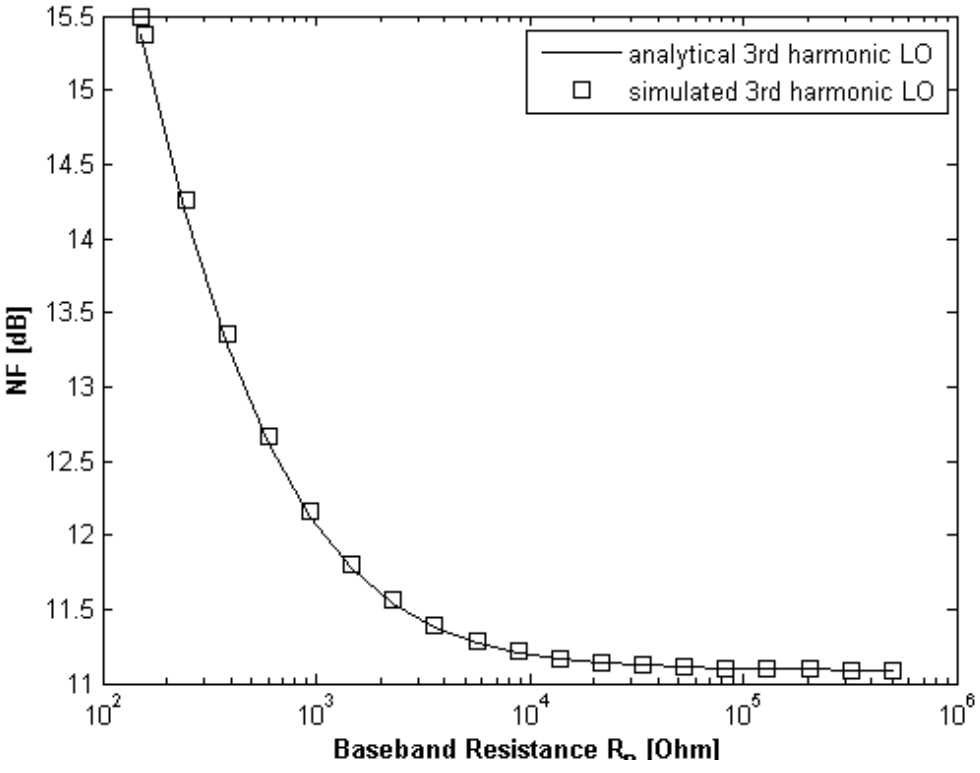


(d)

Figure 4.5. Analytical and simulated 4-phases passive mixer input impedance Z_{in} (a) real and (b) imaginary components when driven by fundamental LO and (c) real and (d) imaginary components when driven by third harmonic LO



(a)



(b)

Figure 4.6. Analytical and simulated noise figure of 4-phases passive mixer against baseband resistance R_B (a) down-conversion by fundamental LO component, (b) down-conversion by third harmonic LO component

The virtual shunt resistance models the power losses due to up-conversion of the baseband signals on the output capacitors through the LO harmonics other than the LO harmonic of interest.

Making the currents obtained from the LTV and LTI models equal

$$\gamma = \frac{2}{(n\pi)^2} \tag{4.8}$$

$$R_{sh} = \frac{4\gamma}{1-4\gamma} R'_a \tag{4.9}$$

Subharmonic mixing at higher LO harmonics has smaller γ and R_{sh}. Smaller shunt resistance introduces more losses of the RF signal power. In addition, it limits the simple baseband impedance tuning capability to achieve matching to the antenna impedance.

In addition, from the LTI model, simplified noise figure expression can be formulated as follows

$$\mathrm{F} = 1 + \frac{1}{{V_{n,R_a}}^2}\left({V_{n,R_{sw}}}^2 + \left(\frac{R_a + R_{sw}}{R_{sh}}\right)^2 {V_{n,R_{sh}}}^2 + \left(\frac{R_a + R_{sw}}{\gamma R_B}\right)^2 {V_{n,\gamma R_B}}^2\right) \tag{4.10}$$

Input impedance, R_{in}, seen at the RF port of the mixer is:

$$R_{in} = R_{sw} + \gamma R_B \,//\, R_{sh} \tag{4.11}$$

Accounting for the mixer output capacitors, similarly;

$$Z_{in} = R_{sw} + \gamma Z_B(j\omega_{IF}) \,//\, R_{sh} \tag{4.12}$$

Figure 4.5 shows the analytical and simulated effective real and imaginary components of the input impedance Z_{in} seen at the RF port of the 4-phases passive mixer using NMOS transistors with $R_{sw} \sim 15\ \Omega$; $R_B = 10\ \mathrm{k}\Omega$; $C_B = 50$ pF; and the LO frequency is 2.5 GHz and 833.33 MHz for the fundamental and third harmonic LO respectively. The output capacitors C_B affect both real and imaginary parts of Z_{in}. For the real components, shown in figure 4.5(a) and (c), the output capacitors realize a low pass filter at baseband which is transformed to a band pass filter at RF frequency. Due to the scaling factor, the effective capacitance at baseband is reduced. Since the scaling factor is smaller for higher harmonic index of the LO, the effective capacitance at baseband in case of fundamental down-conversion is larger than its corresponding in case of third harmonic down-conversion. Therefore, the sharpest band pass filtering behavior is obtained at fundamental LO down-conversion.

Similarly for the imaginary components, shown in figure 4.5(b) and (d). The imaginary components are either inductive for negative IF frequencies, $\omega_{IF} < 0$, or capacitive for positive IF frequencies, $\omega_{IF} > 0$. They are scaled down and slowly varying in the case of third harmonic LO down-conversion due to the scaling factor.

Far away from LO frequency, in case of either fundamental or higher order harmonic mixing, the output capacitors shunt the IF impedance and the input impedance approaches R_{sw}.

Despite Large mixer devices are preferred for better noise figure. In this case, the noise figure is dominated by the last two terms in the noise figure expression. As shown in figure 4.6(a) and (b), as the baseband resistance R_B increases, the noise figure decreases and is dominated by the first two terms, $V_{n,R_{sw}}$ and $V_{n,R_{sh}}$ which determine the minimum noise for the 4-phases passive mixer. For higher LO harmonic mixing, the second term is scaled up by the ratio R_{sh} at fundamental LO to R_{sh} at the third harmonic component of LO – this ration is about 43 – and the last term is scaled up by n^2. For example, assuming a noise figure of 1.8 dB at fundamental mixing and ignoring ${V_{n,\gamma R_B}}^2$ term compared to ${V_{n,R_{sh}}}^2$ and ${V_{n,R_{sw}}}^2$, the noise figure is 11 dB at third harmonic mixing. This degradation is justified due to the increased losses at subharmonic mixing.

Despite impedance tuning limitation and NF degradation drawbacks, subharmonic N-phases passive mixers are still very useful for low power narrowband applications such as Bluetooth/BLE and ZigBee.

4.3.3. Low-IF LNA

When amplifiers operate at low frequency – 10 MHz IF – and small bandwidth – slightly more than 2 MHz – rather than the entire RF Bluetooth band, this significantly reduces the power consumption. The fully differential current reuse low-IF LNA is shown in Fig.1. The differential I/Q mixer outputs are ac-coupled to the low-frequency LNA inputs to reduce flicker noise and provide DC biasing. At very low frequency, the inputs appear only at NMOS gates loaded by diode connected PMOS transistors. Since g_{mn} and g_{mp} are designed to be equal, the amplifier has a unity gain at such low frequencies. At IF, C_F shorts the inputs to PMOS gates. Thus, the amplifier utilizes both the NMOS and PMOS for amplification with the same bias current, and accordingly reduce the current requirement for meeting specific noise and gain. The supply voltage has been selected to be 0.7V as trade-off between the noise and the low-power/high-performance modes power consumption.

4.3.4. Complex filter

The LNA is followed by a complex filter to perform the channel selection and the image rejection. Figure 4.1 shows typical single Gm-C complex pole synthesis. A two Gm-C stages with real transfer function are transformed into a complex one by adding an imaginary part. The imaginary part is obtained by

cross-connecting $g_{m_{IM}}$ transconductance between the I and Q paths [7]. The real component of the pole is synthesized through the $g_{m_{RE}}$ transconductance in shunt with the capacitance C:

$$\omega_{3dB} = \frac{g_{m_{RE}}}{C} \qquad (4.13)$$

On the other hand, the imaginary component is given by:

$$\omega_{shift} = \frac{g_{m_{IM}}}{C} \qquad (4.14)$$

A current-recycling-based topology has been reported in [66] where all the filter's transconductors share their bias currents with the previous stage, Balun-LNA-Mixer (Blixer). However, in this topology, the transistors forming complex load are pseudo-differential. When multiple cells of this topology are cascaded to realize a higher-order filters, the filters exhibit a positive common-mode feedback loop. To maintain stability for this common-mode loop, its gain should be less than unity. This condition sets a constraint on possible filter design space where $g_{m_{IM}}$ should be less than $g_{m_{RE}}$. Therefore, a tightly, limited range of bandpass center frequencies is available for a given bandwidth to preserve stability.

The same topology has been revisited in [67] to enhance this stability issue over a wider design range of $g_{m_{RE}}$ and $g_{m_{IM}}$. It has adopted a fully differential architecture instead of pseudo-differential in the main topology. Fully differential architecture can maintain the common mode gain well lower than the differential mode gain through suitable Common Mode Rejection Ratio (CMRR).

The cross-coupled, M_{NEG}, transistors – create a negative conductance – are seen as a parallel transconductance to $g_{m_{RE}}$ by the common-mode signals and accordingly, reducing the common-mode gain of the cell. For the differential

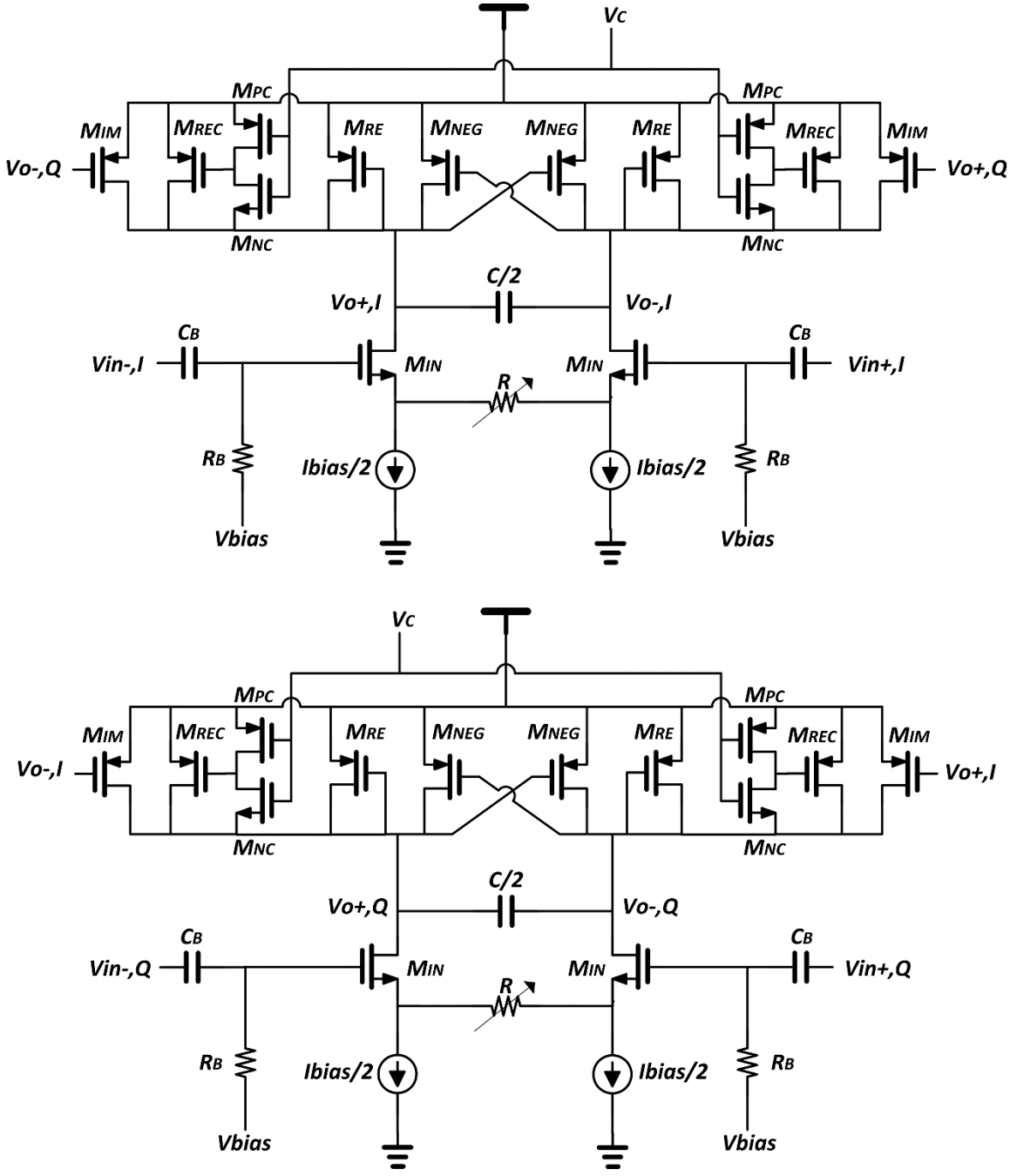


Figure 4.7: Current reuse GM-C complex pole

signals on the other hand, the M_{NEG} pair acts as a negative resistance which in turn reduces the effective real part transconductance, hence the bandwidth, and boosts the differential-mode gain. Figure 4.7 shows the current reuse implementation of a single complex pole.

The complex filter is tuned to have either 1-MHz bandwidth for BT5.1/BLE, or 2-MHz bandwidth for BLE. Therefore, better adjacent channel rejection is obtained in each standard. This is achieved through added controllable $g_{m_{REC}}$ transconductance in parallel with $g_{m_{RE}}$ and controlled by

M_{NC} and M_{PC} control transistors which are connected as an inverter configuration. Therefore, the real part of the complex poles can be controlled by $g_{m_{REC}}$ and accordingly the bandwidth. The inverter's input is a control signal from the baseband, V_c.

Now the Bandwidth and frequency shift relations are:

$$\omega_{3dB} = \frac{g_{m_{eff}}}{C} = \frac{g_{m_{RE}} + D \cdot g_{m_{REC}} - g_{m_{NEG}}}{C} \qquad (4.15)$$

$$\omega_{shift} = \frac{g_{m_{IM}}}{C} \qquad (4.16)$$

Where D is either one or zero.

If V_c is low, D is zero, the M_{REC} transistor's gate is pulled up to the supply voltage through M_{PC} and turning off this PMOS. Consequently, the effective real transcondactance becomes $g_{m_{eff}} = g_{m_{RE}} - g_{m_{NEG}}$ in the 1-MHz bandwidth mode.

If V_c is high, D is one, the M_{REC} transistor's gate is pulled down to V_{out} through M_{NC} and turning on this PMOS. Consequently, it appears in parallel with M_{RE} and the effective real transcondactance is increased by $g_{m_{REC}}$, $g_{m_{eff}} = g_{m_{RE}} + g_{m_{REC}} - g_{m_{NEG}}$ in the 2-MHz bandwidth mode. This increased effective transconductance, reduces the differential-mode gain. Thus, minimum gain requirement shall be designed in this mode. To ensure that the M_{REC} transistor is diode-connected over the entire V_{out} swing range, the M_{NC} transistor should be always on when V_c is high. Therefore, V_c should be slightly higher than the supply voltage and the M_{NC} is chosen to be a low-threshold transistor. The high level of the control signal $V_{c_{high}}$ has a lower limit as follows:

$$V_{c_{high}} >= V_{DD} - V_{DSAT} + V_{th_{M_{NC}}} \qquad (4.17)$$

The input transconductances are utilized to realize a variable gain in the filter. They are made degenerated by a variable resistance *R* in each pole to provide a wide gain tuning range for the overall receiver gain.

4.3.5. VCO and frequency divider

Since the VCO is not directly driving the mixer, a high swing oscillation is not a design requirement, although it helps in the phase noise minimization. The noise associated with the tail current source has a significant contribution in the phase noise. Its flicker noise is directly modulating the output common-mode level and accordingly, modulating the oscillation frequency. The higher-order noise at even harmonics of the oscillation frequency is down-converted, by cross-coupled core transistors, to near the oscillation frequency. Therefore, it results in a phase noise as well. However, removing the tail current source

makes the output common-mode sensitive to the Process; Voltage; and Temperature variations, PVT. Class C VCO shown in figure 4.8, described in [68], has a 3.9-dB phase noise improvement over the standard LC-tank oscillator for the same power consumption.

To minimize the power consumption, the supply voltage is reduced further. However, a lower limit is required for a reasonable swing to avoid operating the cross-coupled transistors in the deep triode region which accordingly reduces the tank quality factor and degrades the phase noise. To design the coupling capacitors C_b equal to the input capacitance seen at the cross-coupled gates, the feedback signal experiences an attenuation by two. Therefore, the lower limit of the supply voltage is derived as follows:

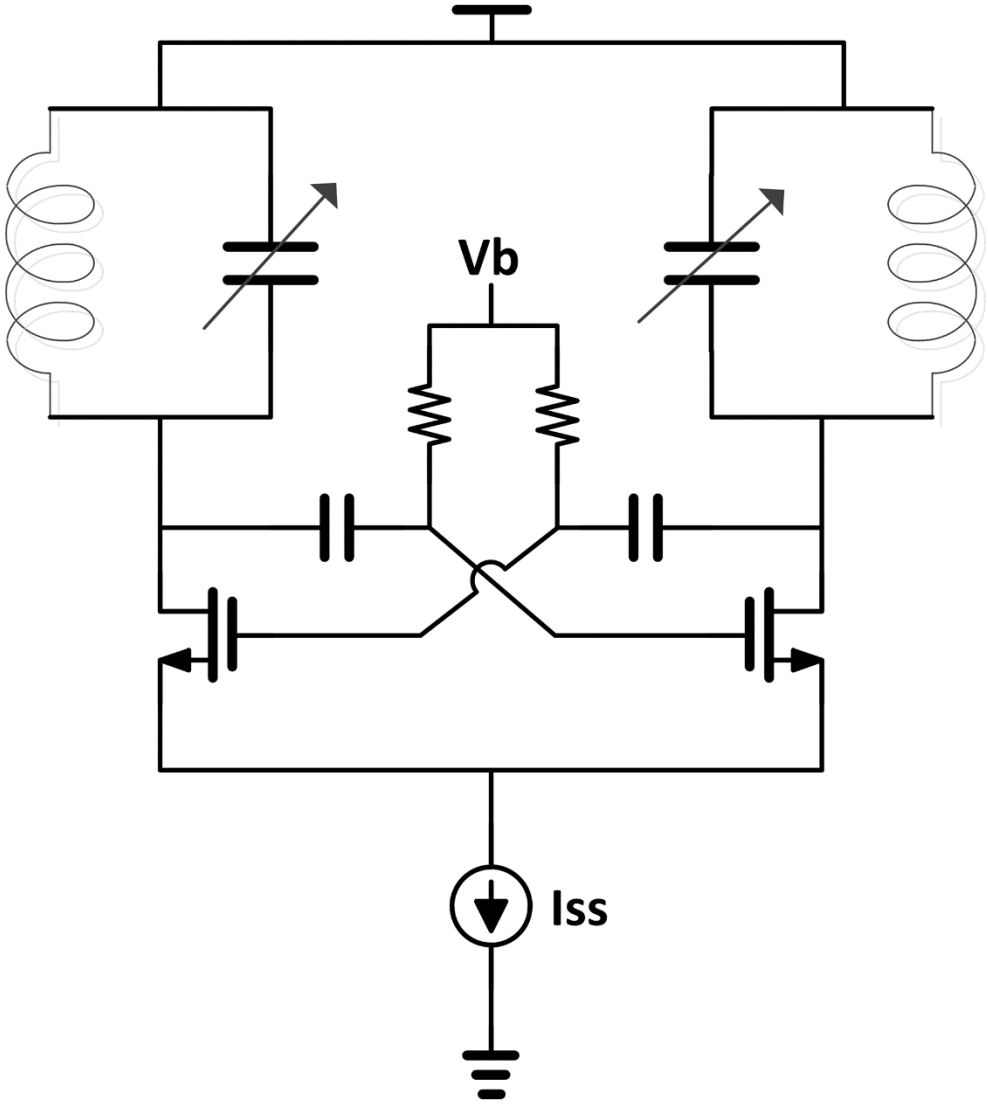


Figure 4.8: Class C VCO core

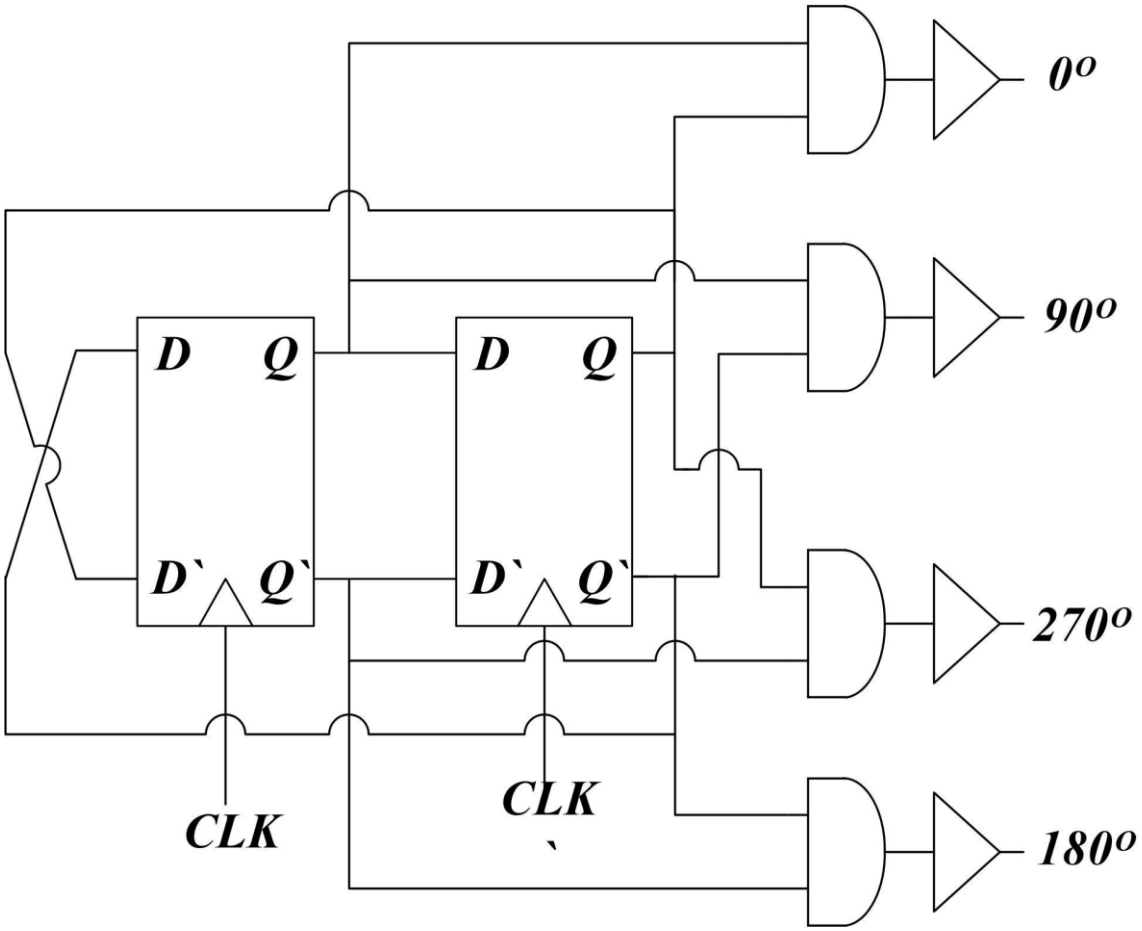


Figure 4.8: 25% non-overlapping clock generation

$$V_b <= V_{DD} - \frac{3}{2} V_p + V_{th} \quad (4.18)$$

$$V_b >= V_{gs} + V_{DSAT} \quad (4.19)$$

Where V_b is the cross-coupled bias voltage and V_p is the oscillation peak voltage.

Combining (18) and (19) and assuming the cross-coupled and the tail transistor to have equal V_{DSAT}, V_{DD} has a lower limit as follows:

$$V_{DD} >= \frac{3}{2} V_p + 2 V_{DSAT} \quad (4.20)$$

For $V_p \approx 200$ mV and $V_{DSAT} \approx 100$ mV, $V_{DD} >= 500$ mV

The dual mode operation places a demand for the LO to have a two well far away frequency ranges, 1.6 GHz in the low-power mode and 4.8 GHz in the high-performance mode. For optimum design at each LO frequency, the operation is divided into two completely separate VCO cores at the expense of extra active area. In fact, the main area concern comes from the need for extra

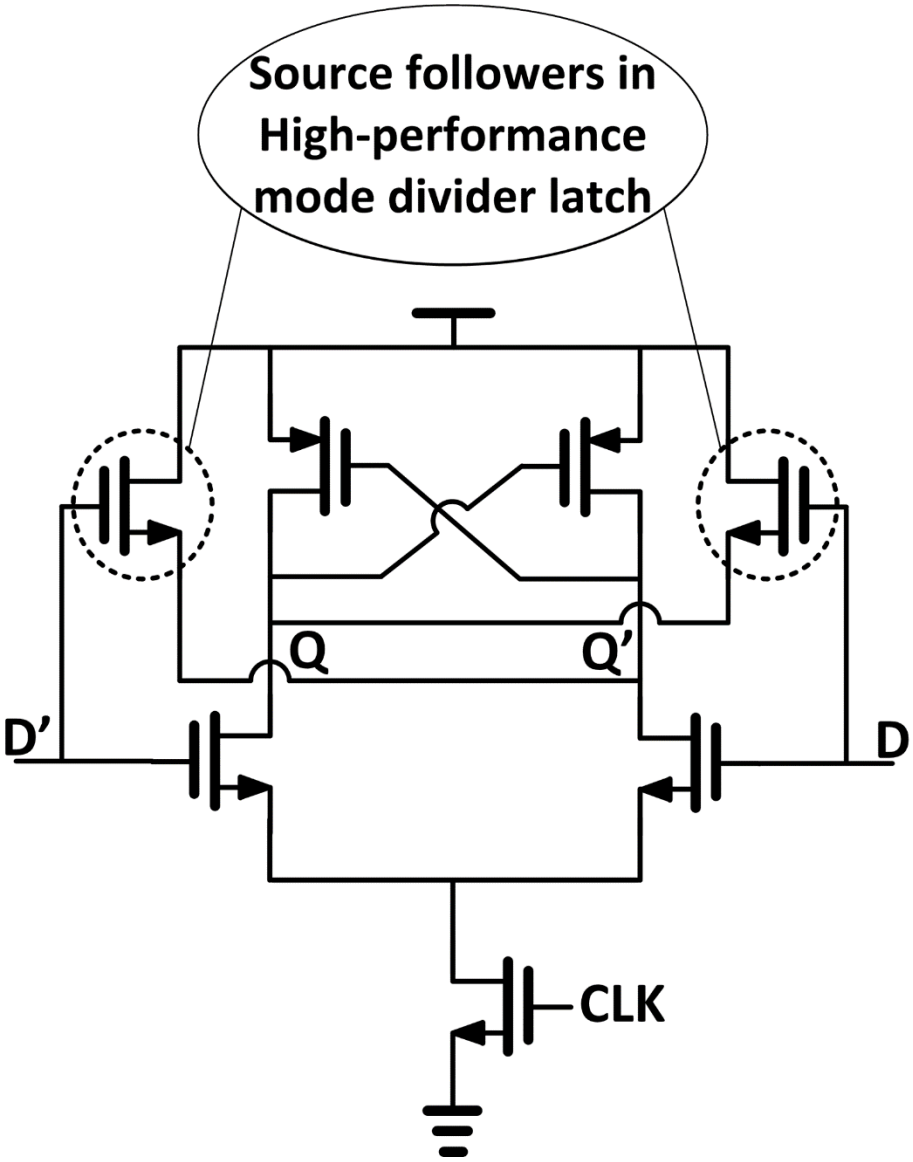


Figure 4.9: Divider latch

inductors for each LC core. However, considering the overall receiver area, the low-IF LNAs eliminated the need for inductors in the conventional LNA-first architecture.

In order to generate 25% duty cycle LO phases, a frequency divider – divide-by-two – circuit and some combinational logic are employed.

Figure 4.8 shows the clock generation circuit driven by the buffered VCO outputs. The latches used in the divider incorporate additional NMOS source followers, over the conventional rail-to-rail latch circuit as shown in figure 4.9. This is to improve the speed and reduce the power consumption [69] in the high-performance mode where the VCO runs at 4.8 GHz. Whereas, in the low power mode, the 1.6-GHz VCO outputs drive the conventional divider latches will consume slightly less power than the modified latches. The NAND gates and chain of inverters following the latches and NAND gates are designed to drive the 20-µm wide mixer switches and ensure non-overlapping LO waveforms to minimize the RX path noise figure.

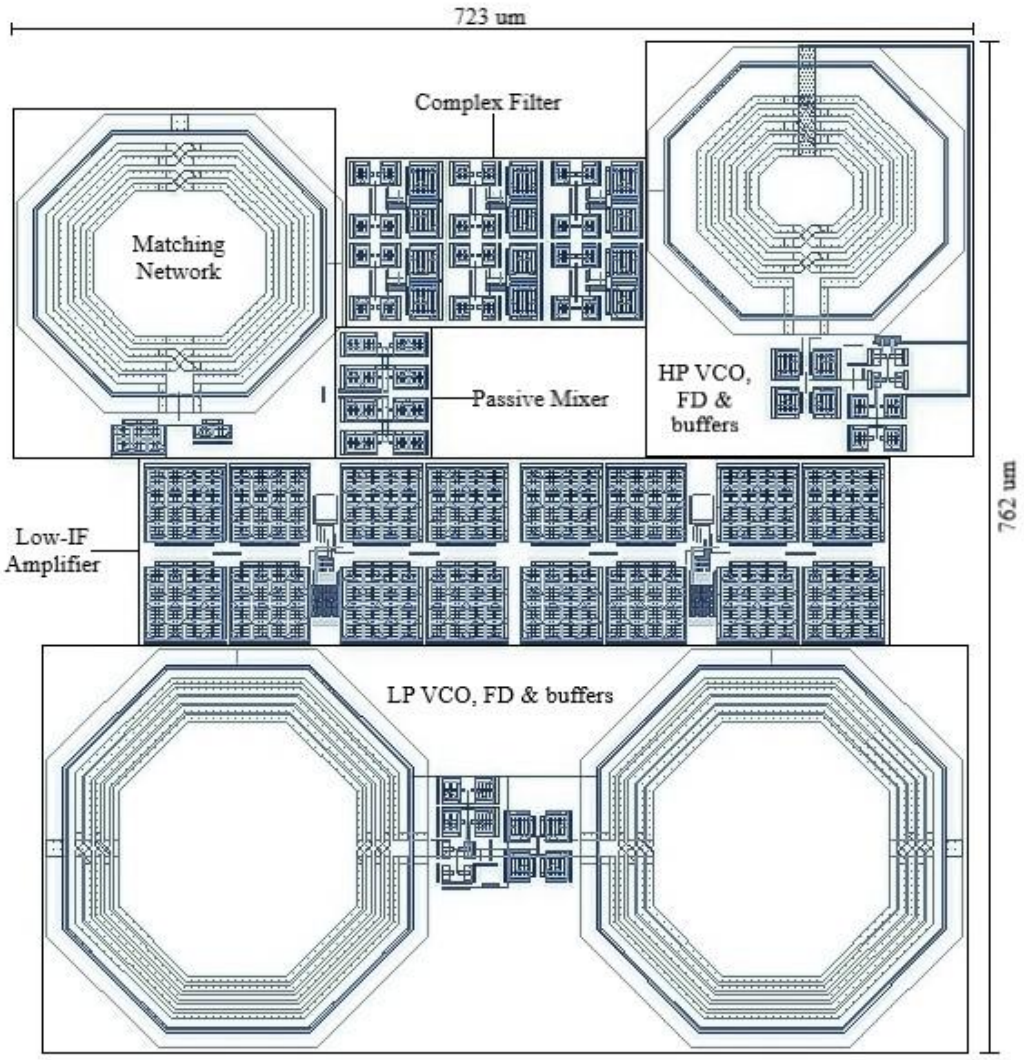


Figure 4.10: Receiver Layout

4.4. Simulation results

The receiver in Figure 4.1 is implemented in 65-nm CMOS technology. It occupies 723 µm x 762 µm. Figure 4.9 portrays the full receiver layout. The receiver operates from 700-mV, for the chain path, and 500-mV, for the LO and frequency dividers supply voltages.

The choice of two separate clock generation circuits, one dedicated for each mode of operation, consumes a significant area due to the two large asymmetric spiral inductors of low-power mode circuit. A larger inductance value is needed for a low- power LC VCO. In addition, a higher quality factor Q_{max} of larger coils occurs at lower frequencies compared to small coils [70].

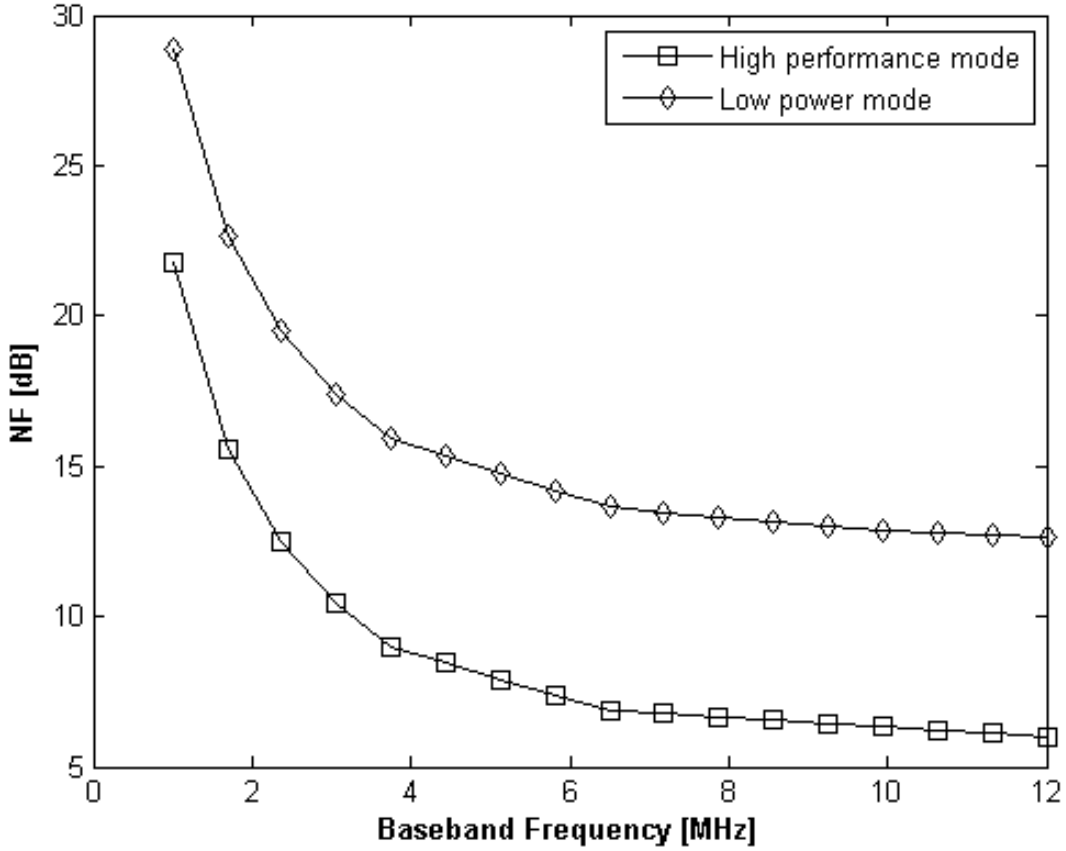


Figure 4.11: Receiver noise figure in the two operation modes

Figure 4.10 plots the noise figure for the whole receiver chain operating in the two modes versus the baseband frequency. At low frequency, the noise figure is significantly high due to the flicker noise. The average noise figure for the low-power and high-performance modes is about 12.82 dB and 6.3 dB at 10 MHz, respectively. As discussed earlier, the power loss – due to up-converting the baseband signals through the passive mixers hence re-radiated – rapidly increases as the LO harmonic index, which is used to down-convert the desired RF signal, increases.

The receiver chain transfer function plots are shown in figure 4.11 with a center frequency of 10 MHz and tuned to either 1-MHz or 2-MHz bandwidth for BT5.1/BLE, or BLE, respectively.

Although the complex filter provides different passband gains at each bandwidth since the effective load seen by the differential signals is higher in case of 1-MHz bandwidth, they are adjusted through the degeneration resistance of the input transconductors and plotted on the same figure. It achieves 65-dB image rejection at least and 17-dB attenuation at the second adjacent channel.

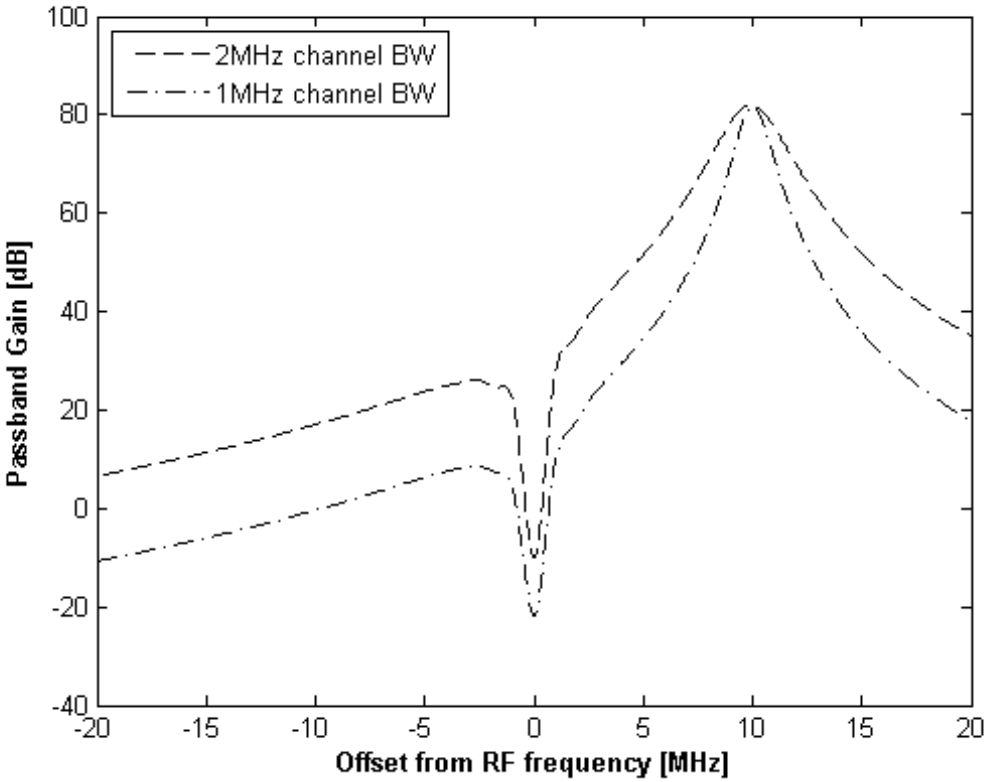


Figure 4.12: Receiver transfer function in the two operation modes

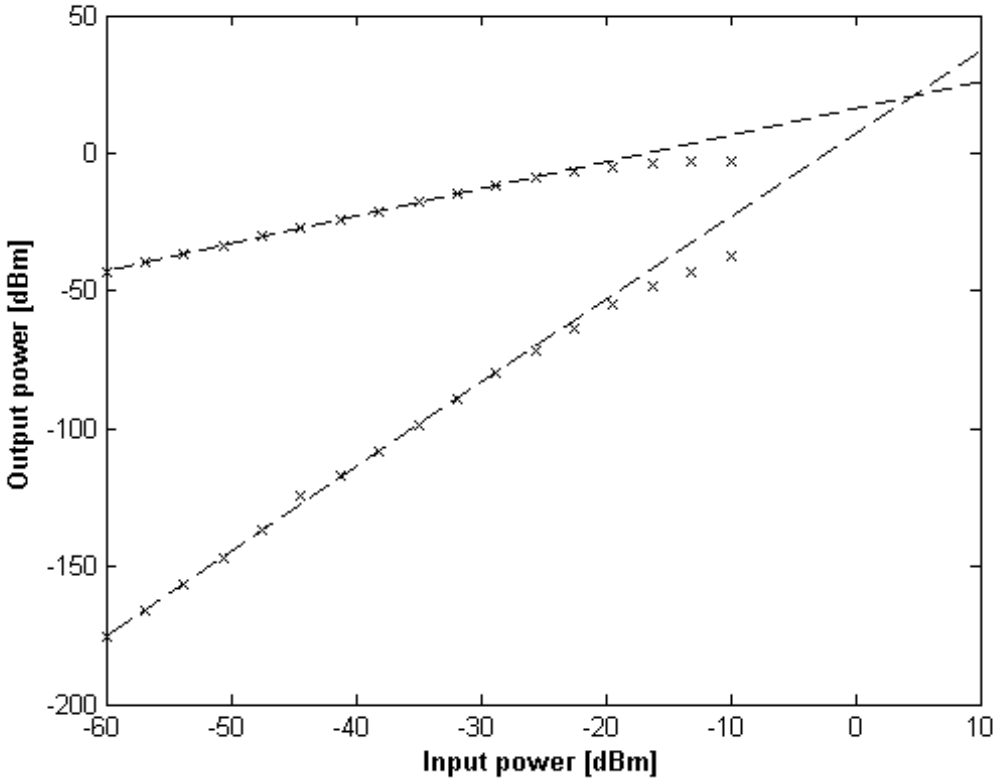


Figure 4.13: Front end out-band IIP3 in the low-power mode

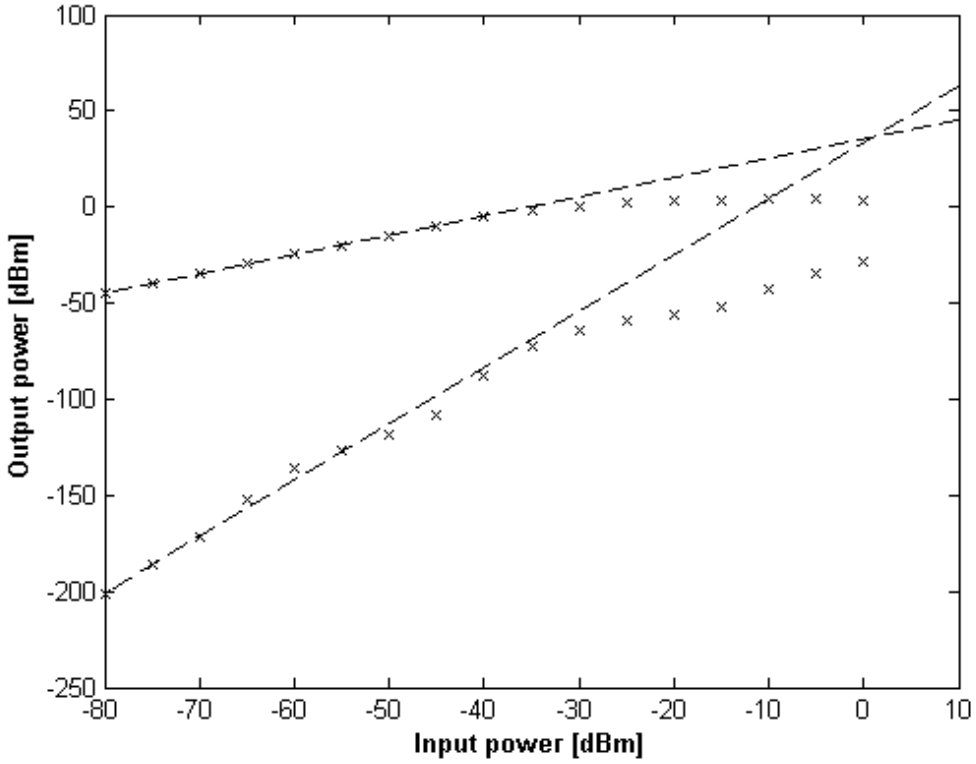


Figure 4.14: Front end out-band IIP3 in the high-performance mode

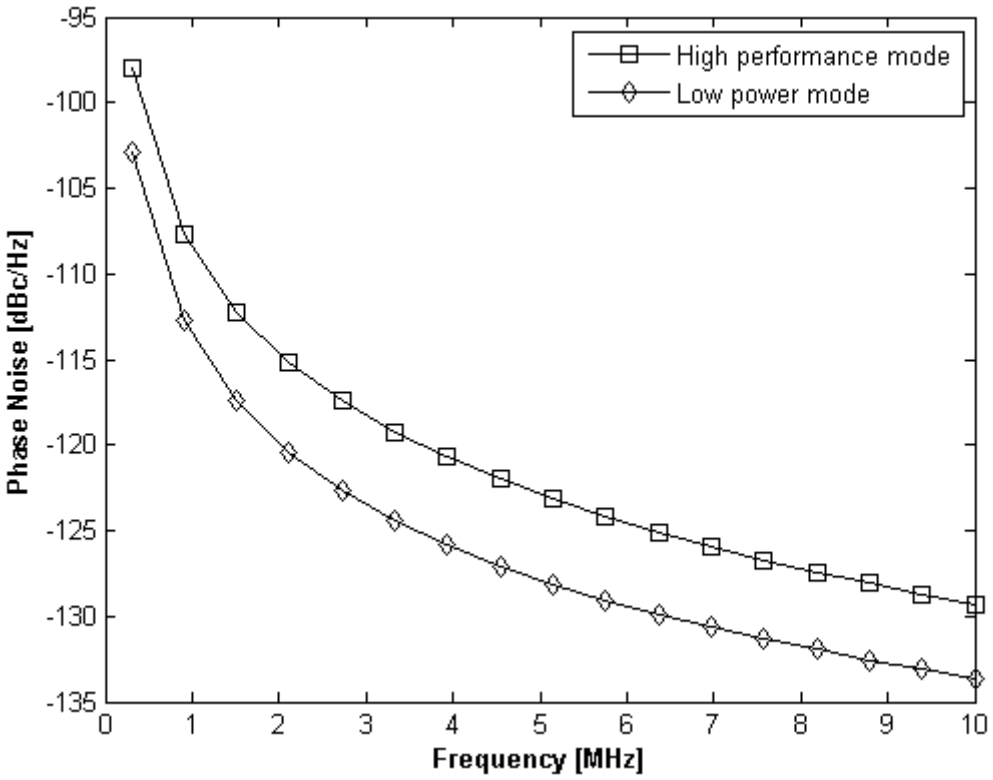


Figure 4.15: VCO phase noise in the two operation modes

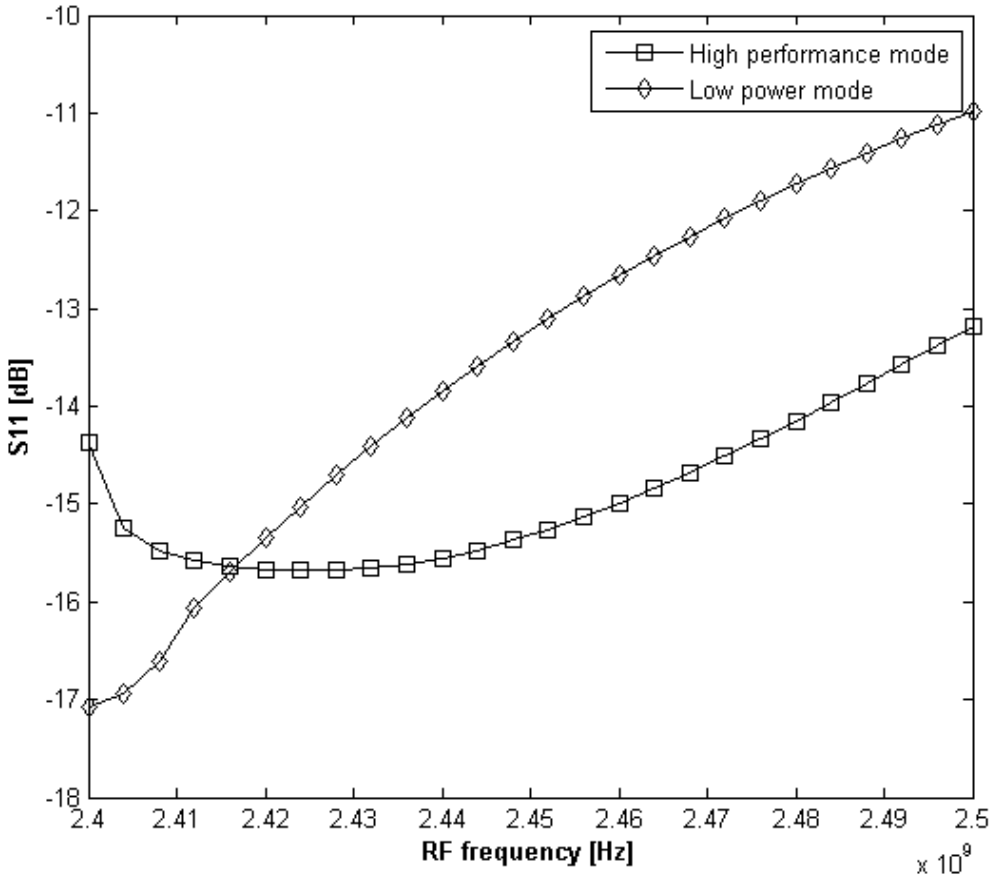


Figure 4.16: S11 in the two modes of operation

The front end Out-Of-Band (OOB) IIP3 in low-power and high-performance modes are shown in figure 4.12 and figure 4.13, respectively. Increased load capacitance of 10pF improves the filtering property of the passive mixers and correspondingly, increases the OOB IIP3 [41]. In the low-power mode, the front end conversion gain is lower than the high-performance mode conversion gain. Therefore compression effect appears at higher input power levels and IIP_3 is better.

Figure 4.14 shows the simulated phase noise versus the frequency offset. At 2.5-MHz offset, phase noise is -122.5 dBc/Hz in low-power mode, whereas it is -117 dBc/Hz in high-performance mode. Since the VCO in the high-performance mode is running at frequency 3x times the frequency of VCO in the low-power mode. Therefore, the phase noise is expected to be higher given that:

1) Q of the inductors in the two modes are within the same range ~ 11.5

2) the output swing is the same of 400 mV

3) the current consumption in the high-performance mode VCO is about 2.5x of the low-power mode VCO

Figure 4.16 plots the input matching response, S11, against RF frequency showing better than -11 dB over Bluetooth band in both operation modes.

PVT variations are simulated in both modes of operation, and presented in the following figures. Some receiver metrics such as the receiver conversion gain in the two operation modes and the noise figure in the low-power mode requires fine calibration in single elements: the complex filter pole capacitors, or output capacitors of passive mixer. The calibration satisfies BT5.1/BLE specifications.

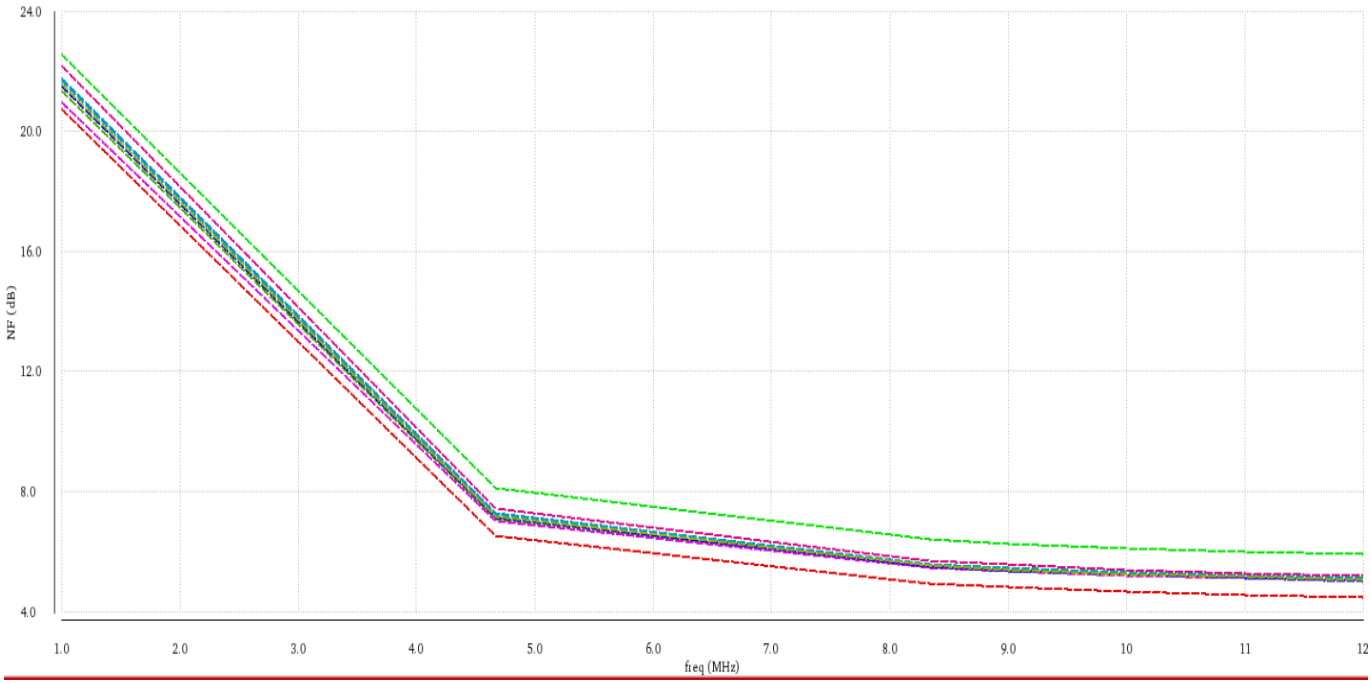


Figure 4.17: Receiver noise figure in the high-performance mode under PVT without calibration

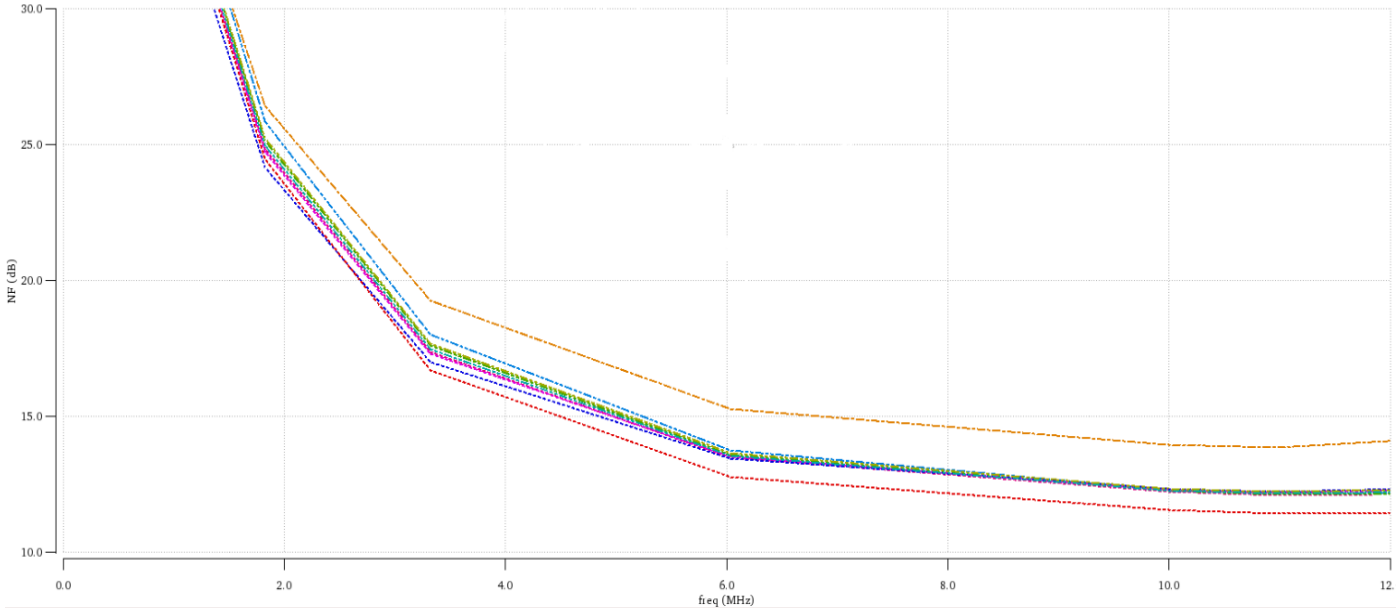


Figure 4.18: Receiver noise figure in the low-power mode under PVT without calibration

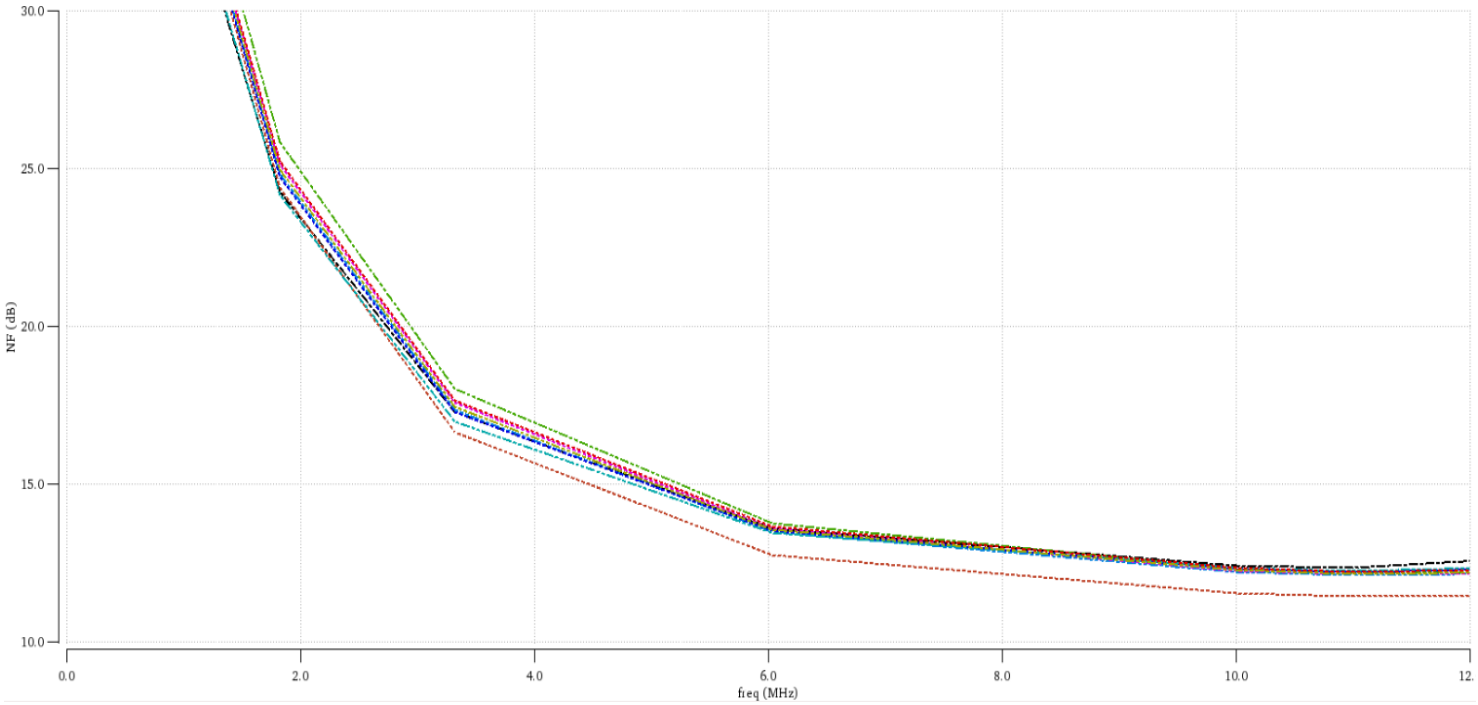


Figure 4.19: Receiver noise figure in the low-power mode under PVT with mixer output capacitors calibration

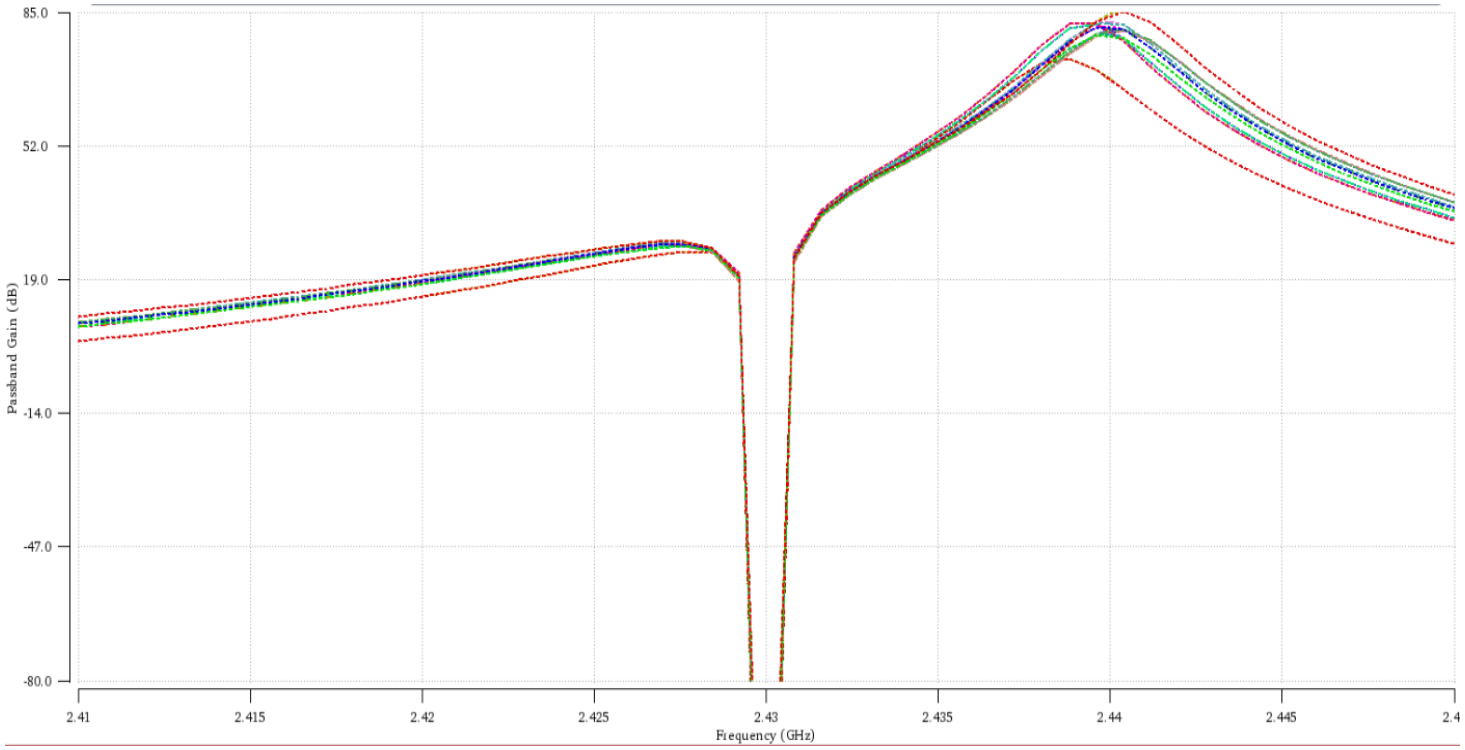


Figure 4.20: Receiver transfer function in the high-performance mode under PVT without calibration

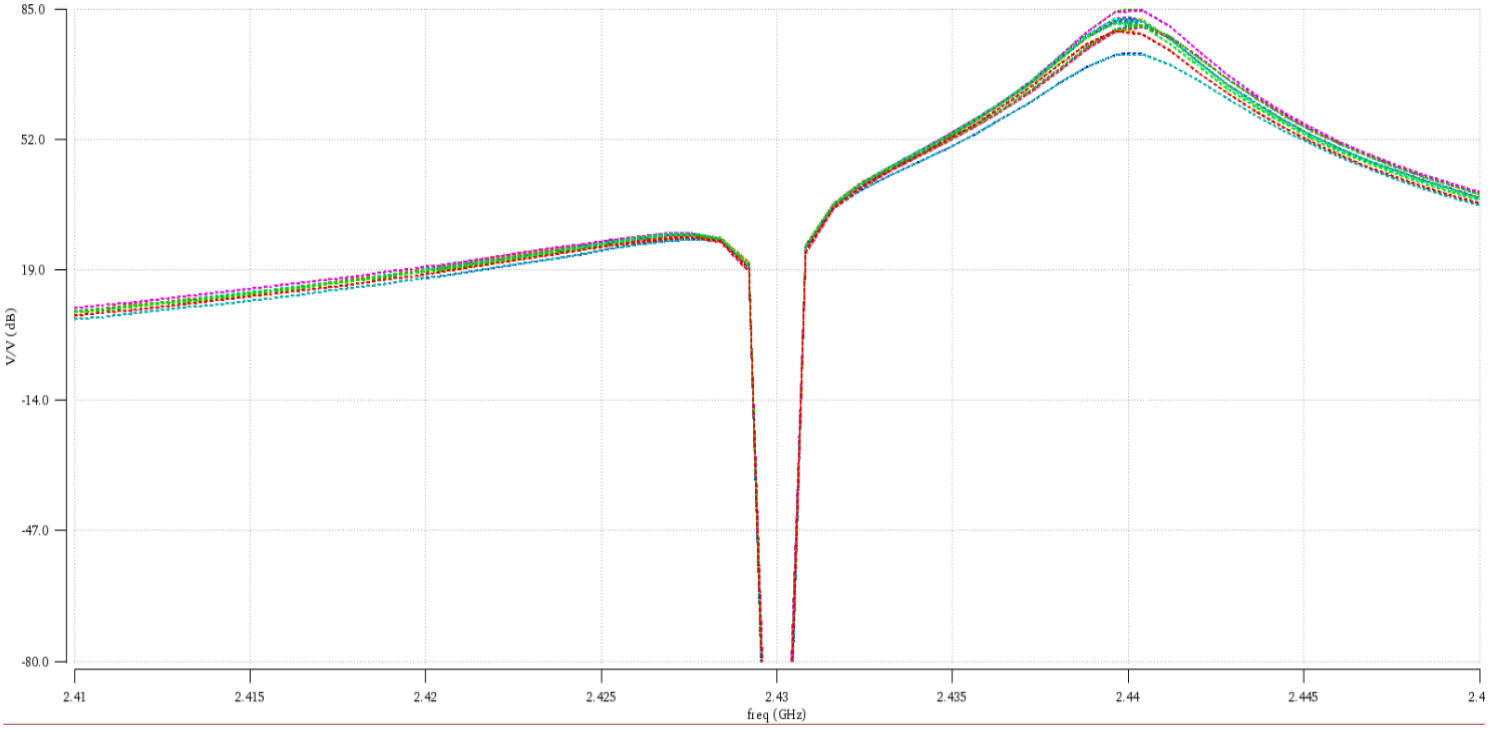


Figure 4.21: Receiver transfer function in the high-performance mode under PVT with complex filter pole capacitors calibration

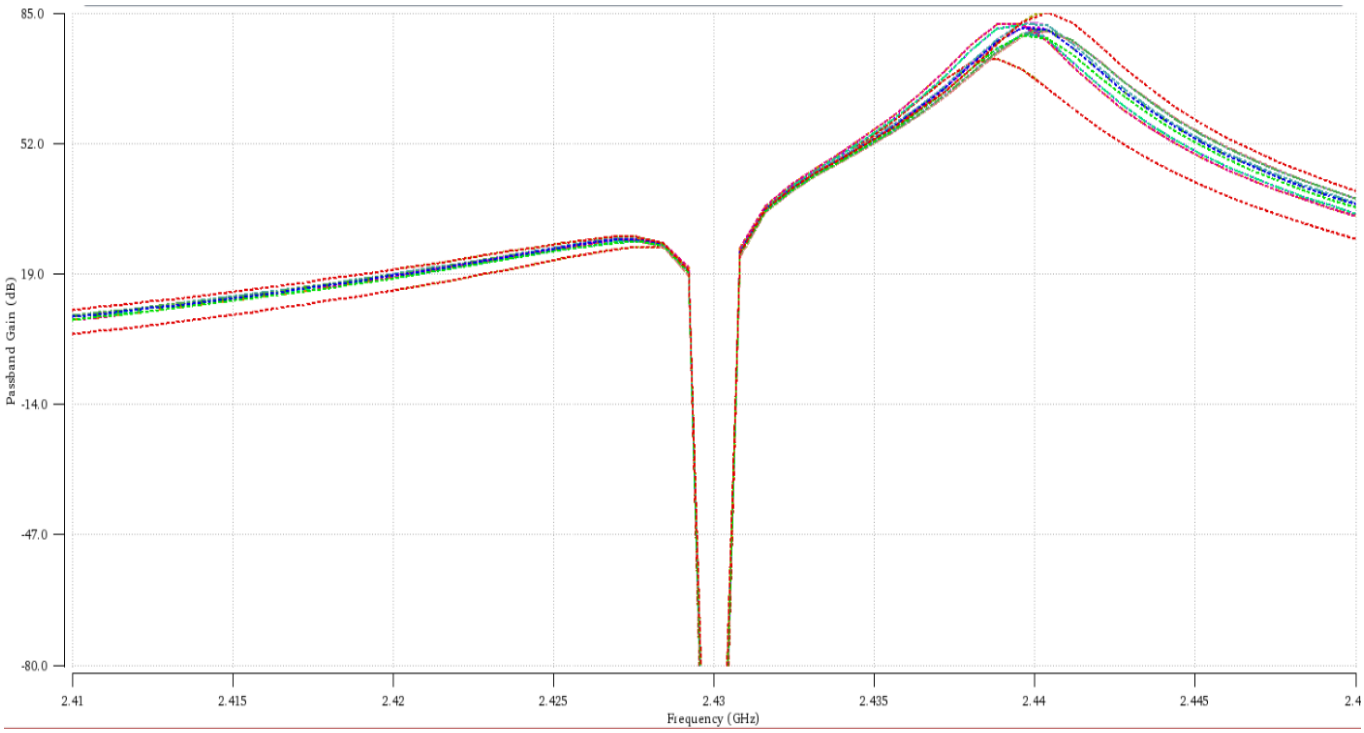


Figure 4.22: Receiver transfer function in the low-power mode under PVT without calibration

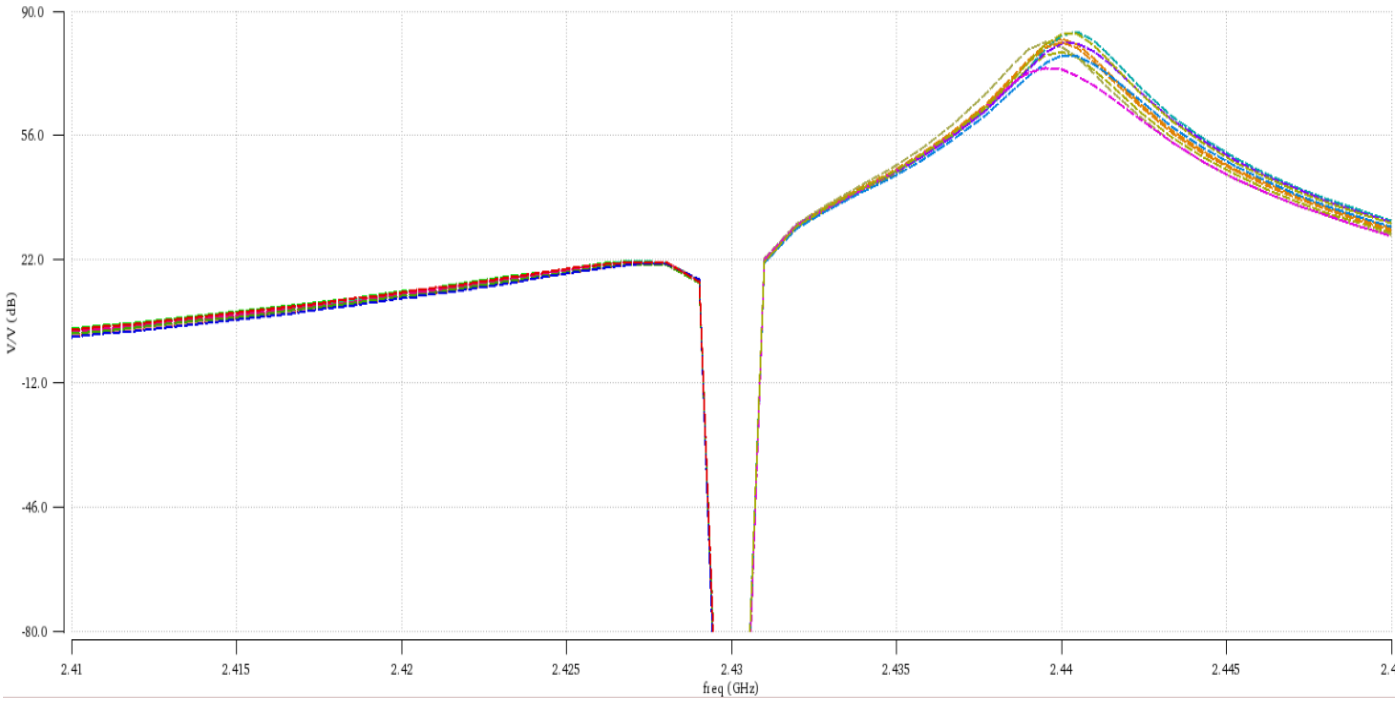


Figure 4.23: Receiver transfer function in the low-power mode under PVT with complex filter pole capacitors calibration

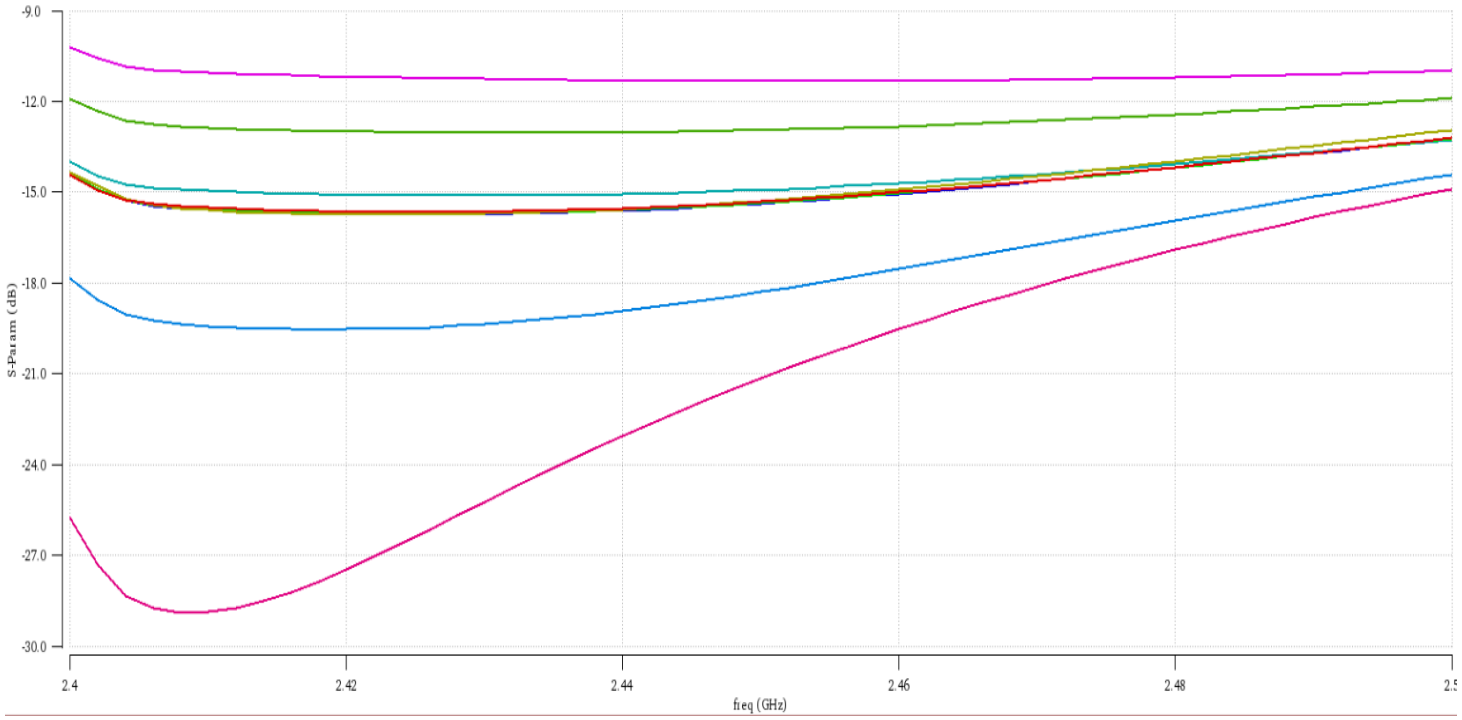


Figure 4.24: S11 in the high-performance mode under PVT without calibration

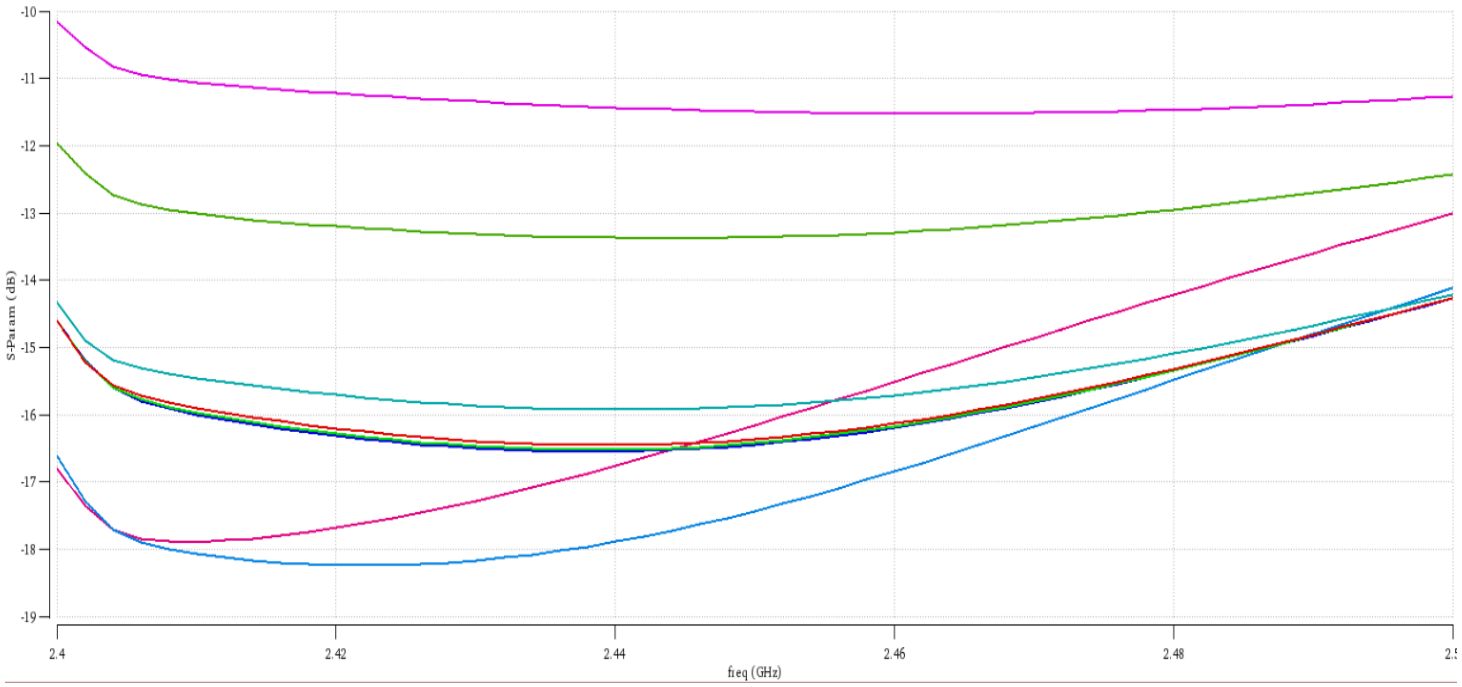


Figure 4.25: S11 in the low-power mode under PVT without calibration

Table 4.1 summarizes the results for both receiver operation modes compared to the state of the art. Thanks to various techniques adopted both on the system level and circuit level, the proposed receiver achieves improved performance metrics at low power dissipation in both modes of operations compared to literature.

4.5. Comparison to receivers state of the art

LMV cell-based receivers in [7], [8] recycled the LNA current to a stacked mixer and VCO. This technique, however, has reduced voltage headroom and block isolation; that's VCO may be pulled by RF blockers and VCO noise will add to the RX noise. Ultra-low voltage supply receivers are popular low power radios approach. A 300mV RX in [9] extensively applies transformer coupling between RF blocks to maximize headroom and lowers transistor threshold voltage through forward body biasing. This comes at the cost of area and increase of leakage currents. Moreover, 180mV RX front end in [10] where I/Q generation is obtained by a passive RC-CR network in the RF path. According to [11], good matching should be preserved through careful layout which complicates both the circuit and physical designs. Also, as the supply voltage is reduced, the IIP3 degrades accordingly. In addition, inductive loaded LNA is divided to two stages, one providing conventional LNA requirements and the second for driving subsequent RC-CR network and passive mixers which imposed extra area.

The work [52] employ passive mixers to avoid the power-hungry active mixers. However, it still have significant power in front end LNA. A new idea has been presented in [40] to realize a fully passive front end receiver where a transformer-based amplification along with 4-phases differential passive mixers to overcome power-hungry RF building blocks.

Table 4.1: PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

	This Work		[8]	[9]	[10]		[52]		[71]
Supply Voltage (V)	Dual supply 0.7V – 0.5V		0.8	0.3	0.18	0.3	0.8		3
Active Power (µW)	697	1250	600	1600	382[1]	1305[1]	2300	2900	6300[2]
NF (dB)	12.82	6.3	15.1/15.8	6.1	11.3	8.8	5.9		6.5
OOB IIP3 (dBm)	+5.58	+2.6	-15.8/-16.8	-21.5	-12.5	+4.8	-17		
Voltage Gain (min/max) (dB)	48/81	55/88	55.5/56.1	83	34.5	41.3	-		-
IRR (min/max) (dB)	65/81		30.5/37.3	-	26.2	25.1	No Image		-
VCO PN (dBc/Hz) @ Offset	-122.5 @ 2.5MHz	-117 @ 2.5MHz	-109 @ 2.5MHz	-112 @ 1MHz	-113 @ 2.5MHz	-116.6 @ 2.5MHz	-		-
Data Rate (Mbps)	1 or 2		1	1	1		1	2	1
FOM[3]	180.87	184.06	178.02/177.32	173.44	183.78	180.94	181.4	180.4	176.41
Technology (nm)	65		130	65	28		40		40
Active Area (mm^2)	0.551		0.25	1.7	1.65		0.8		1.1[4]

[1]Does not include channel selection filters

[2]Includes ADC

[3]FOM = $-P_{sensitivity} - 10\log\frac{P_{DC}}{Data\ Rate}$

[4]Includes both RX and TX

Work Contribution

This work significantly contributes to the literature by bringing up various techniques for low power operation in addition to flexible configurability. For the first time in the literature, a single receiver design compromises two modes of operation in a passive mixer-first architecture based on fundamental LO, and third harmonic LO down-conversion. Proposed receiver configurability provides flexible selection for both the mode of operation, and the wireless standard. A software stack at the top layer adjusts the target receiver wireless standard, and operation mode based on a set of factors. For example, a low-level battery status, or power-saving mode can drive the receiver to operate in the low-power mode. On the other hand, distant communicating devices, or nodes in a noisy environment can make use of the high-performance mode where their receivers are more sensitive. Some applications can utilize the dual mode operation to realize the wake up, and main receiver chains. i.e the low-power mode acts as the wake up receiver chain whereas the high-performance mode represents the main receiver chain. This work highlights the capability of designing dual mode passive mixer-first based receivers. However, it can actually be extended to multiple modes of operation based on the LO harmonic index where complex systems, and complex software can make use of them.

In addition, the proposed receiver design achieves good performance metrics compared to the literature in both modes of operation.

Discussion and Conclusions

A low power, low supply voltage, dual operation mode receiver has been presented. The receiver achieves good performance while consuming only 697 µW/1250 µW through optimizations both at system level and circuit level designs and compromise between its two modes. The proposed receiver is the first one to utilize one receiver chain design realizing two modes of operation through fundamental and harmonic down-conversion based on passive mixers analysis at LO harmonics. The receiver exports control signals to the baseband world for simple mode of operation control and bandwidth adjustment. Each mode is compliant to both BT5.1 and BLE noise figure, linearity, IRR, and phase noise specifications.

Future Work

1. Optimum single VCO core for LO generation in the two receiver modes of operation
2. Design a power Management Unit capable of driving dual supply voltages for the receiver chain, and LO generation circuit. It can be extended to operate the whole receiver from an energy harvester
3. Design a PLL to synthesize a full receiver
4. Design a transmitter to synthesize a complete Bluetooth/BLE transceiver system
5. Get the designs ready for Tape out

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Appendix A: System Architecture Trade-offs Octave Script

```
%% High performance mode

%% VCO power (in micro watts)

% 2 path @ 2.4 GHz, from MIT thesis

% hp_vco_2pp = 95.5

hp_vco_2pp = 100;


% 4 path @ 4.8 GHz, achieved result

hp_vco_4pp = 250;


% 8 path @ 9.6 GHz, estimated from A Low-Voltage Low-Power Wide-Tuning-Range Hybrid Class-AB/Class-B VCO With Robust Start-Up and High-Performance FOM

% estimated by scaling power to achieve -101 @ 1MHz, half power degrades PN by 3dB according to Razavi

hp_vco_8pp = 2000;


% 16 path @ 19.2 GHz, estimated from A Low-Voltage Low-Power Wide-Tuning-Range Hybrid Class-AB/Class-B VCO With Robust Start-Up and High-Performance FOM

hp_vco_16pp = 9000;




%% frequency divider power (in micro watts)

% 2 path @ 2.4 GHz

hp_fd = 0;


% 4 path @ 4.8 GHz, achieved result

hp_fd_by2 = 225;
```

```
% 4 path @ 9.6 GHz, estimated from eScholarship UC item 4vc123z8
graphs, 1 divider @ 9.6GHz + 1 divider @ 4.8GHz

hp_fd_by4 = 400 + hp_fd_by2;


% 4 path @ 19.2 GHz, estimated from A 21-GHz 8-Modulus Prescaler and
a 20-GHz Phase-Locked Loop Fabricated in 130-nm CMOS, 6mA current
consumption under 0.7V

hp_fd_by8 =  0.7*6000;



%% AND gate and Buffering following frequency divider, estimated but
could be more percise from achieved

hp_fd_buf = 20;  % this is per one output (single not differential)

% num of AND gates depends on num of paths

hp_nand = 20;



%%% Buffering following VCO, depens on frequency of operation,
estimation would be based on Pdis = C*f*(Vdd^2) given buffering power
@ 2.4GHz as a reference

hp_lo_buf = 20;

hp_vco_2pp_buf = 2*hp_lo_buf;

hp_vco_4pp_buf = 2*hp_lo_buf * 2;

hp_vco_8pp_buf = 2*hp_vco_4pp_buf * 2;

hp_vco_16pp_buf = 2*hp_vco_8pp_buf * 2;



%% total power consumption

%hp_lo_2pp = hp_vco_2pp + hp_vco_2pp_buf + hp_fd + 0 * hp_nand +
2*hp_fd_buf     + 16*hp_lo_buf

hp_lo_2pp = hp_vco_2pp + hp_vco_2pp_buf + 2*hp_fd + 2*hp_nand +
2*hp_fd_buf + 200;

hp_lo_4pp = hp_vco_4pp + hp_vco_4pp_buf + hp_fd_by2 + 4*hp_nand +
4*hp_fd_buf;
```

```
hp_lo_8pp = hp_vco_8pp + hp_vco_8pp_buf + hp_fd_by4 + 8*hp_nand +
8*hp_fd_buf;

hp_lo_16pp = hp_vco_16pp + hp_vco_16pp_buf + hp_fd_by8 +
16*hp_nand + 16*hp_fd_buf;


hp_lo_power = [hp_lo_2pp hp_lo_4pp hp_lo_8pp hp_lo_16pp];



%% noise figure, estimated from Unified Frequency-Domain Analysis of
Switched-Series-RC Passive Mixers and Samplers, Optimized Design of N-
Phase Passive Mixer-First Receivers in Wideband Operation

hp_nf = [6 3 1.4 1.2];



%% Low power mode

%% VCO power (in micro watts)

% 2 path @ 0.8 GHz, CMOS Technology based LC VCO Review [11] --->
@ 1.85 GHz

lp_vco_2pp = 85;


% 4 path @ 1.6 GHz, achieved result

lp_vco_4pp = 100;


% 8 path @ 3.2 GHz, estimated from CMOS Technology based LC VCO
Review [25] ---> @ 3.88 GHz

% estimated by scaling power to achieve -101 @ 1MHz, half power
degrades PN by 3dB according to Razavi

lp_vco_8pp = 560;


% 16 path @ 6.4 GHz, estimated from CMOS Technology based LC VCO
Review [38] ---> @ 6.85 GHz

lp_vco_16pp = 1790;
```

```
%% frequency divider power (in micro watts)

% 2 path @ 0.8 GHz

lp_fd = 0;


% 4 path @ 1.6 GHz, achieved result

lp_fd_by2 = 100;


% 4 path @ 3.2 GHz, estimated from eScholarship UC item 4vc123z8
graphs, 1 divider @ 3.2GHz + 1 divider @ 1.6GHz

lp_fd_by4 = 200 + lp_fd_by2;


% 4 path @ 6.4 GHz, estimated from eScholarship UC item 4vc123z8
graphs, 1 divider @ 6.4GHz + 1 divider @ 3.2GHz +  1 divider @ 1.6GHz

lp_fd_by8 = 270 + lp_fd_by4;


%% AND gate and Buffering following frequency divider, estimated but
could be more percise from achieved, estimated according to high
performance -scaled by three-

lp_fd_buf = 20/3;  % this is per one output (single not differential)

% estimated according to high performance -scaled by three- num of AND
gates depends on num of paths

lp_nand = 20/3;



%% Buffering following VCO, depens on frequency of operation,
estimation would be based on Pdis = C*f*(Vdd^2) given buffering power
@ 2.4GHz as a reference, estimated according to high performance -scaled
by three-

lp_lo_buf = 20/3;

lp_vco_2pp_buf = 2*lp_lo_buf;

lp_vco_4pp_buf = 2*lp_lo_buf * 2;

lp_vco_8pp_buf = 2*lp_vco_4pp_buf * 2;

lp_vco_16pp_buf = 2*lp_vco_8pp_buf * 2;
```

```
%% total power consumption

%hp_lo_2pp = hp_vco_2pp + hp_vco_2pp_buf + hp_fd + 0 * hp_nand +
2*hp_fd_buf     + 16*hp_lo_buf

lp_lo_2pp = lp_vco_2pp + lp_vco_2pp_buf + 2*lp_fd + 2*lp_nand +
2*lp_fd_buf + 200;

lp_lo_4pp = lp_vco_4pp + lp_vco_4pp_buf + lp_fd_by2 + 4*lp_nand +
4*lp_fd_buf;

lp_lo_8pp = lp_vco_8pp + lp_vco_8pp_buf + lp_fd_by4 + 8*lp_nand +
8*lp_fd_buf + 450;

lp_lo_16pp = lp_vco_16pp + lp_vco_16pp_buf + lp_fd_by8 + 16*lp_nand
+ 16*lp_fd_buf;


lp_lo_power = [lp_lo_2pp lp_lo_4pp lp_lo_8pp lp_lo_16pp];



%% noise figure, estimated

lp_nf = [14 11 4 3.8];



%% FOM

BW1 = 2*10^6;

BW2 = 1*10^6;

snr = 13;

hp_Psens1 = -174 + 10*log10(BW1) + hp_nf + snr;

hp_Psens2 = -174 + 10*log10(BW2) + hp_nf + snr;


lp_Psens1 = -174 + 10*log10(BW1) + lp_nf + snr;

lp_Psens2 = -174 + 10*log10(BW2) + lp_nf + snr;


hp_FOM1 = -hp_Psens1 - 10*log10((hp_lo_power*10^(-6))/BW1);

hp_FOM2 = -hp_Psens2 - 10*log10((hp_lo_power*10^(-6))/BW2);
```

```
lp_FOM1 = -lp_Psens1 - 10*log10((lp_lo_power*10^(-6))/BW1);

lp_FOM2 = -lp_Psens2 - 10*log10((lp_lo_power*10^(-6))/BW2);



%% number of passive mixer paths

num_paths = [2 4 8 16];



%% plot

%plot(num_paths, hp_lo_power)

set(gcf,'color','w');

plot(num_paths, hp_FOM1, '--ks');

hold on;

plot(num_paths, lp_FOM1, '-.kd');

xlabel('number of mixer paths','FontSize',10,'FontWeight','bold');

ylabel('FOM (-P_{sensitivity} - 10log(P_{DC} / DataRate))
[dB]','FontSize',10,'FontWeight','bold');

legend('high performance mode','low power mode');
```

Appendix B: Analytical, and Simulated Noise Figure Plots Octave Script

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Simulated
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


%% Fundamental LO mode noise figure %%

hp_mode_nf = csvread('C:\My Files\Masters\Thesis\Simulations\simulation tables
v0.0\nf_fund_mixer_analysis_1.csv',1,0);


yh = transpose(hp_mode_nf(1,:));

xh = transpose(hp_mode_nf(2,:));

% eliminate first element

yh = yh(2 : length(yh));

xh = xh(2 : length(xh));



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Analatical
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Rsw = 13;

Ra = 50;

Raa = Ra + Rsw;

Rb = xh;

hp_gamma = 2/(pi^2);

hp_Rsh = (4*hp_gamma/(1-4*hp_gamma))*Raa;


Cb = 50 * 10^(-12);

fif = 10 * 10^6;
```

```
wif = 2 * pi * fif;

xb = -i * (1./(wif * Cb));


zb = (Rb * xb)./(Rb + xb);

hp_zbscaled = hp_gamma * zb;



noisefloor = 4 * (1.38*10^(-23)) * (300);

VnRa_power = noisefloor * Ra;

VnRsw_power = noisefloor * Rsw;

VnRsh_power = noisefloor * hp_Rsh;

VnGammaRb_power = noisefloor * hp_gamma*Rb;


%term1 =  Raa./(hp_gamma * abs(zb));

term1 =  Raa./(hp_gamma * Rb);

term2 = term1.^2;

term3 = term2.*VnGammaRb_power;

hp_F = 1 + (1/VnRa_power) * (VnRsw_power + ((Raa/hp_Rsh)^2)*VnRsh_power + term3);

%%hp_F = 1 + (1/VnRa_power) * (VnRsw_power + ((Raa/hp_Rsh)^2)*VnRsh_power);

hp_nf = 10*log10(hp_F);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Simulated
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% 3rd Harmonic LO mode noise figure %%

lp_mode_nf = csvread('C:\My Files\Masters\Thesis\Simulations\simulation tables
v0.0\nf_3rdharm_mixer_analysis_1.csv',1,1);


yl = transpose(lp_mode_nf(1,:));

xl = transpose(lp_mode_nf(2,:));

% eliminate first element

yl = yl(2 : length(yl));

xl = xl(2 : length(xl));



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Analatical
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Rsw = 13;

Ra = 50;

Raa = Ra + Rsw;

Rb = xl

lp_gamma = 2/((3 * pi) ^ 2);

lp_Rsh = (4*lp_gamma/(1-4*lp_gamma))*Raa;


Cb = 50 * 10^(-12);

fif = 10 * 10^6;

wif = 2 * pi * fif;

xb = -i * (1./(wif * Cb));
```

```
zb = (Rb * xb)./(Rb + xb);

lp_zbscaled = lp_gamma * zb;


lp_zin = Rsw + (lp_zbscaled * lp_Rsh)./(lp_zbscaled + lp_Rsh);



noisefloor = 4 * (1.38*10^(-23)) * (300);

VnRa_power = noisefloor * Ra;

VnRsw_power = noisefloor * Rsw;

VnRsh_lpower = noisefloor * lp_Rsh;

VnGammaRb_lpower = noisefloor * lp_gamma*Rb;


%term1 =  Raa./(lp_gamma * abs(zb));

term1_lp =  Raa./(lp_gamma*Rb);

term2_lp = term1_lp.^2;

term3_lp = term2_lp.*VnGammaRb_lpower;

lp_F = 1 + (1/VnRa_power) * (VnRsw_power + ((Raa/lp_Rsh)^2)*VnRsh_lpower + term3_lp);

%%lp_F = 1 + (1/VnRa_power) * (VnRsw_power + ((Raa/lp_Rsh)^2)*VnRsh_lpower);

lp_nf = 10*log10(lp_F);
```

الملخص

يحفز التطور المستمر لشبكة أجهزة الاستشعار اللاسلكية الأنظمة القائمة بشدة الحاجة إلى طاقة منخفضة للغاية وأجهزة راديو حيث تم تجهيز عدد كبير جدًا من الأجهزة والمستشعرات بواسطة جهاز استقبال أو جهاز إرسال أو جهاز إرسال / استقبال. الغرض من هذه العقد هو العمل في مخطط حصاد ذاتي للطاقة و تستخدمه كمصدر طاقة لهل للتشغيل و ذلك لتجنب إجراء تغيير البطارية أو إعادة الشحن. وبالتالي ، فهي مقيدة للغاية لاستهلاك الطاقة.

تستخدم أجهزة الاستشعار اللاسلكية دورة عمل قليلة جدا لأنها لا تحتاج إلى أن تكون نشطة طوال الوقت لتقليل الطاقة التى تستهلكها. هناك تقنية بديلة أخرى وهي استخدام جهاز استقبال مساعد يعمل دائمًا (WuRX) و يستهلك القليل من الوات أو حتى طاقة أقل من ميكرو وات واحد مع الحفاظ على جهاز الاستقبال الرئيسي في وضع السكون حتى يتلقي إشارة تنبيه من جهاز الاستقبال المساعد ذات الطاقة المنخفضة جدا. النهج الثاني مناسب للتطبيقات الحرجة فى وقت الاستقبال و الارسال.

يتم استخدام المعايير اللاسلكية ذات معدلات البيانات المنخفضة والمصممة لتطبيقات الطاقة المنخفضة في شبكة أجهزة الاستشعار اللاسلكية. بما أن أجهزة الاستشعار اللاسلكية تعمل بمعدلات بيانات منخفضة ، فيمكنها أن تحقق استهلاك طاقة منخفض و مستويات حساسية أفضل مما يسمح بخفض طاقة جهاز الارسال عن طريق الإرسال بقدرة أقل. يعد البلوتوث منخفض الطاقة واحد من أفضل المرشحين كمعيار لاسلكي لشبكة أجهزة الاستشعار اللاسلكية نظرًا لأن تقنية البلوتوث ناشئة وتم نشرها واعتمادها على نطاق واسع نظرًا لقوتها وقلة تكلفتها ومرونتها للتخصيص.

تقدم هذه الأطروحة تصميم جهاز استقبال متوافق مع الاصدار الخامس من البلوتوث و البلوتوث منخفض الطاقة. جهاز الاستقبال لديه وضعين للعمل هما وضع الطاقة المنخفضة ، و وضع الأداء العالي. التصميم يستخدم تقنيات مختلفة لاستهلاك منخفض للطاقة على مستوى النظام والدائرة معا.

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تاريخ التسجيل: 2017\3\1
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القسم: هندسة الالكترونيات و الاتصالات الكهربية
الدرجة: ماجستير
المشرفون:
أ.د. أحمد حسين
أ.م.د. حسن مصطفى

الممتحنون:

أ.د. أحمد حسين (المشرف الرئيسي)
أ.د. أحمد نادر محى الدين (الممتحن الداخلى)
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أ.م.د. سامح عاصم ابراهيم (الممتحن الخارجى)
أ.م.د. حسن مصطفى (المشرف الرئيسي)

عنوان الرسالة:

تصميم مستقبل منخفض الطاقة ذو وضعي تشغيل للبلوتوث و البلوتوث منخفض الطاقة

الكلمات الدالة:

البلوتوث ، البلوتوث منخفض الطاقة ، تردد متوسط منخفض ، محول تردد أولا ، واجهة أمامية لترددات الراديو ، ثنائى الوضع ، وضع الأداء العالى ، وضع الأداء منخفض الطاقة ، اعادة استخدام التيار

ملخص الرسالة:

يحفز التطور المستمر لشبكة أجهزة الاستشعار اللاسلكية الأنظمة القائمة بشدة الحاجة إلى طاقة منخفضة للغاية وأجهزة راديو حيث تم تجهيز عدد كبير جدًا من الأجهزة والمستشعرات بواسطة جهاز استقبال أو جهاز إرسال أو جهاز إرسال / استقبال. الغرض من هذه العقد هو العمل في مخطط حصاد ذاتي للطاقة و تستخدمه كمصدر طاقة لهل للتشغيل و ذلك لتجنب إجراء تغيير البطارية أو إعادة الشحن. وبالتالي ، فهي مقيدة للغاية لاستهلاك الطاقة.

تستخدم أجهزة الاستشعار اللاسلكية دورة عمل قليلة جدا لأنها لا تحتاج إلى أن تكون نشطة طوال الوقت لتقليل الطاقة التى تستهلكها. هناك تقنية بديلة أخرى وهي استخدام جهاز استقبال مساعد يعمل دائمًا (WuRX) و يستهلك القليل من الوات أو حتى طاقة أقل من ميكرو وات واحد مع الحفاظ على جهاز الاستقبال الرئيسي في وضع السكون حتى يتلقي إشارة تنبيه من جهاز الاستقبال المساعد ذات الطاقة المنخفضة جدا. النهج الثاني مناسب للتطبيقات الحرجة فى وقت الاستقبال و الارسال.

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تقدم هذه الأطروحة تصميم أول جهاز يستخدم تصميم سلسلة مستقبل واحد يحقق طريقتين للتشغيل من خلال تحويل التردد باستخدام fundamental and harmonic LO متوافق مع الاصدار الخامس من البلوتوث و البلوتوث منخفض الطاقة. جهاز الاستقبال لديه وضعين للعمل هما وضع الطاقة المنخفضة ، و وضع الأداء العالي. التصميم يستخدم تقنيات مختلفة لاستهلاك منخفض للطاقة على مستوى النظام والدائرة معا. بالاضافة الى ذلك تقدم الأطروحة تحليل لمحولات التردد التى لا تستخدم مصدر طاقة (passive mixers) لتردد ال LO الأساسى (fundamental LO) و مضاعفاتها (harmonic LO).

تقدم هذه الأطروحة جهاز استقبال متوافق مع تقنية Bluetooth5.1 و Bluetooth Low Energy. جهاز الاستقبال لديه وضعان للتشغيل ؛ وضع الطاقة المنخفضة ، ووضع الأداء العالي. و هو يقدم تقنيات مختلفة لاستهلاك منخفض للطاقة على مستوى النظام والدائرة. يتم استخدام محول التردد أولا ذو IF منخفض لتحسين استهلاك الطاقة على مستوى النظام. علاوة على ذلك ، يتيح تحويل التردد باستخدام harmonics LO في وضع الطاقة المنخفضة توليد Quadrature LO. استخدام جهد إمداد منخفض ، mV500 لـ VCOs و mV 700 لسلسلة الواجهة الأمامية ، و محولات تردد لا تستخدم مصدر طاقة ، و اعادة استخدام التيار يساعدون فى تقليل الطاقة المستهلكة على مستوى الدائرة. يستخدم المستقبل المقترح دائرة متكاملة. يتم تنفيذ المستقبل المقترح بتقنية 65 CMOS نانومتر ويحتل مساحة تبلغ 0.551 ميللى متر مربع و تستهلك فقط 697 ميللى وات و 1250 ميللى وات عند التشغيل في وضع الطاقة المنخفضة ووضع الأداء العالي على الترتيب.

تصميم مستقبل منخفض الطاقة ذو وضعي تشغيل للبلوتوث و البلوتوث منخفض الطاقة

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كجزء من متطلبات الحصول على درجة
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في
هندسة الالكترونيات و الاتصالات الكهربية

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يناير – 2021

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