Author	Ahmed Lutfi Awad EL-Greatly
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Supervision Committee	Prof. El-Sayed Mahmoud El-Rabaie
	Assoc. Prof. Ahmed Ahmed Shaaban Dessouki
	Assoc. Prof. Hassan Mostafa
	Assistant Prof. Rania Mohamed Abdalla

English Abstract

Time-based Analog-to-Digital Converter (T-ADCs) have gained most of researchers' interest recently for their higher performance than other analog-to-digital converters in terms of operation speed, input dynamic range and power consumption. However, T-ADCs suffer from serious drawbacks which are the output delay non-linearity and the limited dynamic range of the input signal. In this research, two proposed 5 bits voltage-to-time converters are presented for T-ADCs at which the input voltage signal is connected to the body terminal of the starving transistor rather than its gate terminal. These proposed converters exhibit better linearity which is analytically proven in the thesis. The maximum linearity error is reduced to 0.4%. In addition, the input dynamic range of these converters is increased to 800mV for a supply voltage of 1.2V by using industrial hardware-calibrated TSMC 65nm CMOS technology and the proposed ADCs operate at a clock frequency of 500MHz. Moreover, a 3-bit highly linear Time-based Analog-to-Digital Converter (T-ADC) is proposed. This proposed ADC

exhibits high linearity, simple design and low power which make it the best solution for the problems that limit the performance of the Multiple-Input Multiple-Output (MIMO) systems. The proposed ADC exhibits a maximum linearity error of 0.56%, a wide input dynamic range of 800mV and a low power of 2.2mW. The supply voltage used equals to 1.2V in industrial hardware-calibrated TSMC 65nm CMOS technology. The proposed ADC operates at a clock frequency of 4GHz and a maximum input frequency of 2GHz.

Key Words	Body biasing; Time-based analog-to-digital converter; Voltage-to-time converter; MIMO; Low resolution ADC

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Summary

Analog-to-digital converter (ADC) is considered the link between the real world, represented by real-time analog signals and the digitized world, represented by digital integrated circuits, microprocessors and microcontrollers. ADCs are the key components in most recent electronic devices especially in software-defined radio (SDR), biomedical devices and low-power electronic devices.

Recent ADC architectures are facing many serious limitations due to CMOS technology scaling. One of these limitations is the degradation of the signal-to-noise ratio (SNR) due to the reduction of the supply voltage. Moreover, the dynamic range of analog input signal is reduced as the threshold voltage is not affected by the continuous scaling of CMOS transistors.

These limitations led to the design of the time-based analog-to-digital converter (T-ADC). In this ADC, the input voltage signal is converted to a delay signal first where the delay is proportional to the input signal value. Following that, this delay signal is converted to a digital code. This allows the processing of the signal to be in the time domain. However, the performance of the Voltage-to-Time Converter (VTC) circuit in the T-ADC is limited by two major drawbacks. These drawbacks are the output delay non-linearity and the limited dynamic range of the input signal.

In this Thesis, two proposed 5 bits voltage-to-time converters are presented for T-ADCs at which the input voltage signal is connected to the body terminal of the starving transistor rather than its gate terminal.

These proposed converters exhibit better linearity which is analytically proven in the thesis. The maximum linearity error is reduced to 0.4%. In addition, the input dynamic range of these converters is increased to 800mV for a supply voltage of 1.2V by using industrial hardware-calibrated TSMC 65nm CMOS technology and the proposed ADCs operate at a clock frequency of 500MHz.

Thanks to their simple design, the proposed VTC circuits occupy a small area of 26.67 μm^2 for the first proposed VTC and 11.16μm^2 for the second proposed VTC, while consuming very small power of 18μW for the first proposed VTC and 15μW for the second proposed VTC. The effect of PVT variations on the proposed designs is discussed. In addition, calibration circuits are proposed to overcome the limitations in the VTC circuits' performance due to these variations. Moreover, Time-to-Digital Converter (TDC) is proposed as the performance of the VTC is limited by the design of the time-to-digital converter (TDC) circuit that follows it. The TDC affects the linearity of the whole ADC and its performance should be investigated. Differential non-linearity (DNL) and integral non-linearity (INL) for the whole ADC are calculated as they are the most important parameters that represent the linearity in the whole ADC.

Since the proposed designs are suitable for applications with limited power budget, such as internet of things (IoT) and wearable devices, the proposed VTC circuits can be applied for low-resolution ADCs for wireless communication receivers in Multiple-Input Multiple-Output (MIMO) systems as the power consumption is a much more important factor than resolution.

Hence, a 3-bit highly linear Time-based Analog-to-Digital Converter (T-ADC) is proposed. This proposed ADC exhibits high linearity, simple design and low power which make it the best solution for the problems that limit the performance of the MIMO systems. The proposed ADC exhibits a maximum linearity error of 0.56%, a wide input dynamic range of 800mV and a low power of 2.2mW. The supply voltage used equals to 1.2V in industrial hardware-calibrated TSMC 65nm CMOS technology. The proposed ADC operates at a clock frequency of 4GHz and a maximum input frequency of 2GHz.

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List of Abbreviations

ADC	Analog-to-Digital Converter
BER	Bit Error Rate
BD	Block Diagonalization
BS	Base Station
CTC	Current-to-Time Converter
D-FF	D Flip Flop
DAC	Digital-to-Analog Converter
DNL	Differential Non-Linearity
DU	Delay Units
ENOB	Effective Number Of Bits
EOC	End Of Conversion
FBB	Forward Body Bias
FFT	Fast Fourier Transform
FOM	Figure Of Merit
INL	Integral Non-Linearity
IoT	Internet of Things
LSB	Least Significant Bit
MIMO	Multiple Input Multiple Output
MMSE	Minimum Mean Square Error
MSB	Most Significant Bit
MSE	Mean Square Error
PVT	Process-Voltage-Temperature
PWM	Pulse Width Modulation
RBB	Reverse Body Bias
SAR	Successive Approximation Register

SD	Sigma Delta
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SQNR	Signal-to-Quantization Noise Ratio
T-ADC	Time based Analog to Digital Converters
TDC	Time-to-Digital Converters
THD	Total Harmonic Distortion
TSMC	Taiwan Semiconductor Manufacturing Company
VCO	Voltage-Controlled Oscillator
VFC	Voltage-to-Frequency Converter
VTC	Voltage-to-Time Converter
ZF	Zero Forcing

Chapter 1

Introduction

Analog-to-Digital Converter (ADC) is considered the bridge that links the real world represented in real-time signals, which are analog signals, with the digitalized world represented in modern digital integrated circuits. Since all the input signals are analog in nature, ADCs are found in all modern electronic devices such as microprocessors, biomedical devises and all cellular devices.

ADC is the key metric that defines the performance of the whole system in terms of the power consumption, resolution and output speed.

Technology scaling is considered the main problem that affects the design of the ADC. With continuous technology scaling, the supply voltage is reduced which reduces the dynamic range of the analog input signal that is processed by the ADC. Moreover, reducing the supply voltage results in degradation of the Signal-to-Noise Ratio (SNR) as the thermal noise doesn't scale with technology [1, 2].

1.1 ADC Design Trends

In order to improve power efficiency, speed and cost along with technology scaling, there are three design trends for ADCs as shown below [1, 3]:

1.1.1. Minimalistic Design

The main goal in this approach is to simplify the analog sub-circuits in the ADC to improve the overall power dissipation although this will affect the accuracy in measuring the input voltage. An example of this trend is to remove or simplify the op-amp blocks in ADC as in op-amp-less implementation of pipeline ADCs [4] in which the op-amp is replaced with open-loop amplifiers. Another example is to replace op-amps with comparators in switched capacitor circuits as shown in Fig 1.1 and Fig. 1.2 [5].

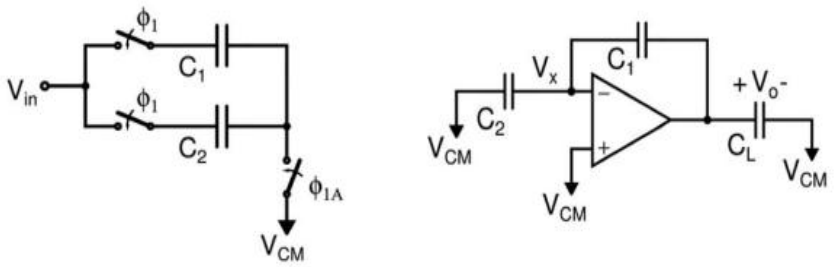


Figure 1.1. Conventional switched capacitor gain stage [5].

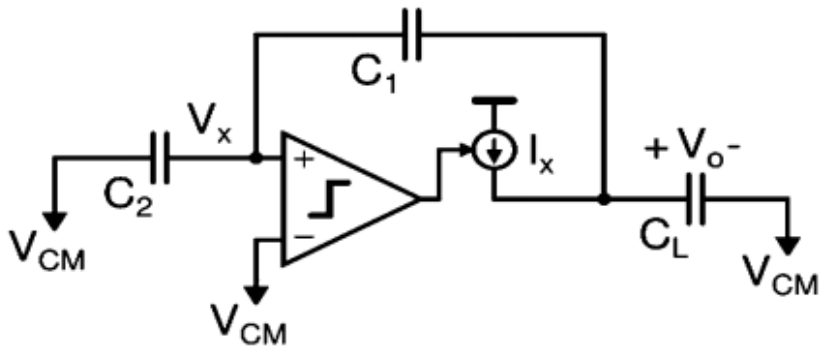


Figure 1.2. Comparator-based switched capacitor gain stage [5].

1.1.2. Digitally-Assisted Analog Design

In this approach, the main idea is to reduce the accuracy of measuring the analog input signal in the analog circuitry while adding digital calibration circuits to correct imperfections in the input analog signal in the digital domain. This approach results in lower power consumption and higher operation speed.

One example of this approach is the use of open-loop amplifiers in pipeline ADCs while correcting the nonlinearities caused by open-loop amplifiers in the digital domain [4]. Figure 1.3 shows the conventional pipeline stage while Fig. 1.4 shows the usage of open-loop amplifier in the pipeline stage [4]. Figure 1.5 shows the digital non-linearity compensation circuit that makes the back-end conversion error (ε_r) very small [4].

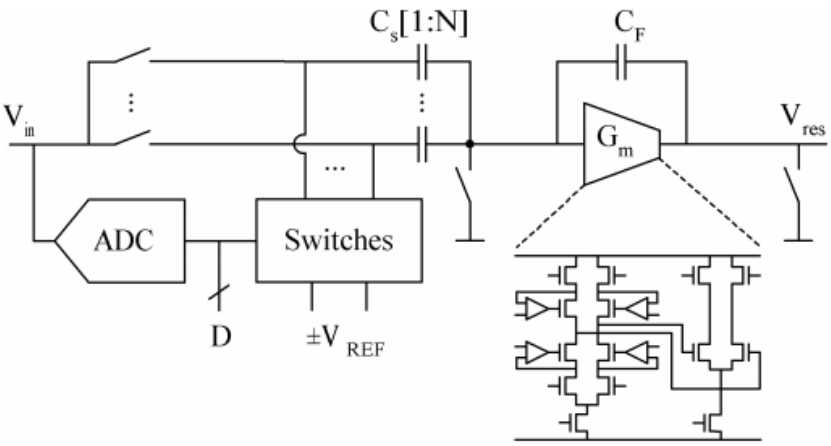


Figure 1.3. Conventional pipeline stage [4].

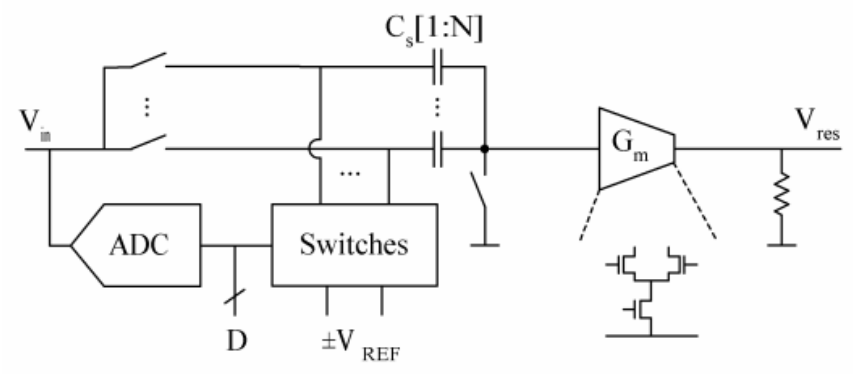


Figure 1.4. Pipeline stage with open-loop amplifier [4].

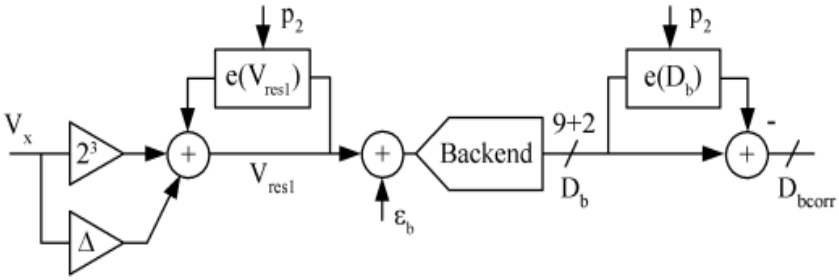


Figure 1.5. Digital non-linearity compensation [4].

1.1.3. Time Domain Analog Signal Processing

The main idea of this approach is to convert the input signal from voltage domain to time domain first before processing it because processing the analog signal can be done using digital circuitry instead of the analog one. Thus, this approach can benefit from the advantages of technology scaling in reducing power consumption and the area at the same time.

Many designs have been introduced as a result using this approach such as the design of Time based Analog to Digital Converters (T-ADC).

In T-ADC, the input voltage signal is converted to a delay signal first before processing.

The analog input signal can be converted into frequency instead of time using the voltage-to-frequency converter [6] or Voltage-Controlled Oscillators (VCOs), where the VCO frequency is linearly proportional to the analog signal amplitude. Then, frequency is converted to digital code using phase detectors [7, 8].

1.2 Time-Based Analog-to-Digital Converters

The design of time-based ADCs has got more attention by researchers as it is proven by recent studies that time-based ADCs can overcome the limitations of technology scaling that were previously stated.

In time-based ADC, the analog input voltage signal is converted to a delay signal. This delay is proportional to the amplitude of the analog input signal. Following that, this delay signal is processed by digital circuitry and converted to a digital code. This allows reducing the analog circuitry which minimizes the impact of technology scaling on the ADC design. Moreover, processing the signal in time domain is an important advantage due to the reduction of gate delay as a result of technology scaling. This improves time resolution in nanometer-scale devices, despite the reduction in supply voltage.

1.3 Problem Statement

Despite the significant improvement in performance of the time-based ADCs, these ADCs are facing serious limitations which need to be

taken in consideration and more research should be directed toward overcoming these limitations. These limitations are the output delay non-linearity and the limited dynamic range.

The output delay non-linearity results from the non-linear response of the sub-circuitry that converts the analog signal into delay signals. This non-linearity results in inaccurate conversion of the input signal to digital code. More research should be done to design new sub-circuits to maintain the linearity of the output delay response. Moreover, new digital calibration algorithms may be implemented to reduce the non-linearity error.

Limited dynamic range is considered a major drawback in the design of time-based ADCs. This limitation appears as a result of reducing the supply voltage while the threshold voltage of the CMOS devices is kept unchanged. New design techniques should be done to reduce the effect of the threshold voltage value on the input signal dynamic range.

1.4 Thesis Objectives

The main objectives of this thesis are:

- Design new circuits that can reduce the non-linearity of the output delay signal at higher input values.
- Perform detailed analytical analysis for the proposed designs to prove that the linearity has improved.
- A full performance analysis should be done using Cadence Virtuoso simulator program to study the proposed circuits' performance against

second order effects such as process variations, supply voltage variations, temperature variations, and jitter.

1.5 Thesis Organization

The rest of the thesis is organized as follows:

Chapter 2 introduces a literature review on the most common ADC architectures and their performance. It provides a detailed discussion about time-based ADCs especially the Voltage-to-Time Converter (VTC) and Time-to-Digital Converters (TDC). Moreover, novel trends in the design of VTC circuits are discussed in details.

Chapter 3 introduces the proposed VTC circuits providing a strong analytical analysis to proof the improvement in the performance of the proposed circuits in terms of the output delay non-linearity, power consumption and dynamic range. Moreover, a discussion is included about the effect of some important factors on the performance of the proposed VTC circuits such as Process-Voltage-Temperature (PVT) variations.

Chapter 4 introduces the Time-to-Digital Converter (TDC) circuit for the proposed VTC as the TDC affects the linearity of the whole ADC. Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are also introduced.

Chapter 5 presents using the first proposed ADC in the Base Station (BS) in Multiple Input Multiple Output (MIMO) systems.

Chapter 6 includes the conclusions and future work followed by the list of references.

Chapter 2

A Literature Review on Common ADC Architectures

In this chapter, we discuss the most common ADC architectures including the theory of operation and performance analysis. Moreover, a detailed survey is presented on the common commercial ADC architectures. The data in this survey are collected from major integrated circuits companies such as Texas Instruments and Analog Devices for about 1500 commercial ADCs. This chapter aims to help researches to choose from the most common architectures the ADC that fits their desired application.

Performance metrics and design specifications for the ADC are discussed first. Then, a detailed description of ADC architectures is discussed.

2.1 Performance Metrics

The overall dynamic performance of ADCs can be identified by five important metrics as follows [9]:

2.1.1. Signal to Noise Ratio (SNR)

It is defined by the ratio between the signal power to noise power as shown below:

$$\text{SNR} = 10\ \log_{10}\left[\frac{\text{Signal Power}}{\text{Noise Power}}\right] \quad (2.1)$$

2.1.2. Total Harmonic Distortion (THD)

It is defined as the ratio between the signal power to harmonic distortion power as shown below:

$$\text{THD} = 10\ \log_{10}[\frac{\text{Signal Power}}{\text{Distortion Power}}] \quad (2.2)$$

2.1.3. Signal to Noise and Distortion Ratio (SNDR)

It is defined by the ratio between the signal power to the sum of distortion and noise power as shown below:

$$\text{SNDR} = 10\ \log_{10}\left[\frac{\text{Signal Power}}{\text{Distortion Power+Noise Power}}\right] \quad (2.3)$$

2.1.4. Effective Number Of Bits (ENOB)

It represents the actual resolution of the ADC when taking in consideration the circuit noise as follows:

$$\text{ENOB} = \frac{\text{SNDR(dB)}-1.76}{6.02} \quad (2.4)$$

2.1.5. Figure Of Merit (FOM)

Figure Of Merit (FOM) is considered the reference parameter that can be used to compare the efficiency of different ADC topologies regardless of their design. There are two common equations that describe FOM in terms of ENOB, sampling frequency and power consumption as shown below [10]:

$$FOM1 = \frac{DR^2 F_S}{P} \quad (2.5)$$

$$FOM2 = \frac{P}{2^{ENOB} F_S} \quad (2.6)$$

Where DR is the input dynamic range, P is the power consumption and F_S is the sampling frequency.

2.2 Design Specifications

There are important parameters that should be taken in consideration during selecting the appropriate design of ADC for a specific application. These parameters are:

2.2.1 Resolution

It is a measure of how accurately the ADC can detect very small changes in the input signal. Resolution can better described as the minimum required change in the input signal in order to change the corresponding digital output by 1 Least Significant Bit (LSB) and can be described as follows [9]:

$$\text{LSB} = \frac{V_{in\_FR}}{2^N} \quad (2.7)$$

Where N is the number of bits of the ADC and Vin_FR is the full range of the input signal.

2.2.2 Dynamic Range

It represents the maximum range of the input signal that can correctly detected by the ADC. It represents an important metric during the appropriate ADC architecture for a specific application.

2.2.3 Latency (Output Delay)

It represents the time required by the ADC to convert the analog signal to the digital code. As the latency decreases, the ADC becomes more efficient. Some applications requires high speed ADCs such as pipeline ADCs at the cost of power consumption while other applications requires lower power consumption at the cost of operation speed. These applications are discussed later in details.

2.2.4 Power Consumption

Although reducing the power consumed is a main goal in all ADC architectures especially in mobile devices, this power reduction comes at the cost of higher output speed in specific applications. In sum, there is a trade-off between the power consumption and the operation speed. Choosing between power consumption and latency is decided based on the type of application the ADC is used for.

2.3 ADC Architectures

In this section, the most popular ADC architectures are discussed in details at which the input voltage signal is directly converted to a digital code such as flash ADC, Successive Approximation Register (SAR) ADC, pipe-lined ADC and sigma-delta ADC.

Other types of ADCs convert the input voltage signal to intermediate signal (time or frequency signals) first before converting it to digital code such as single slope ADC, dual slope ADC, Pulse Width Modulation (PWM) ADC and a Voltage-to-Time Converter (VTC) circuit followed by a Time-to-Digital Converter (TDC) circuit. These ADCs will be

discussed separately in details as they represent the main interest of this thesis.

2.3.1 Flash ADC

An N-bit flash ADC is shown in Fig. 2.1. It consists of 2^N resistors that form a ladder voltage divider in order to divide the reference voltage into 2^N equal intervals. This reference voltage represents the maximum value for the input voltage signal. The 2^N comparators compare the input voltage with each value of the voltage intervals resulting in logic '1' if the input voltage value is greater than the reference voltage of the corresponding bit. The output of these comparators is a thermometer code that needs a decoder to convert it to a digital code.

This ADC does not need a clock. In other words, the conversion time is set when accessing the comparators and the decoder.

The advantage of this design is its high speed as it is only limited by the delay of comparators and the decoder [9, 11]. However, this architecture has low resolution [9, 11]. For higher resolution, the speed of the flash ADC is affected by the loading of the large number of comparators. Moreover, the area and the power consumption increase due to using many comparators.

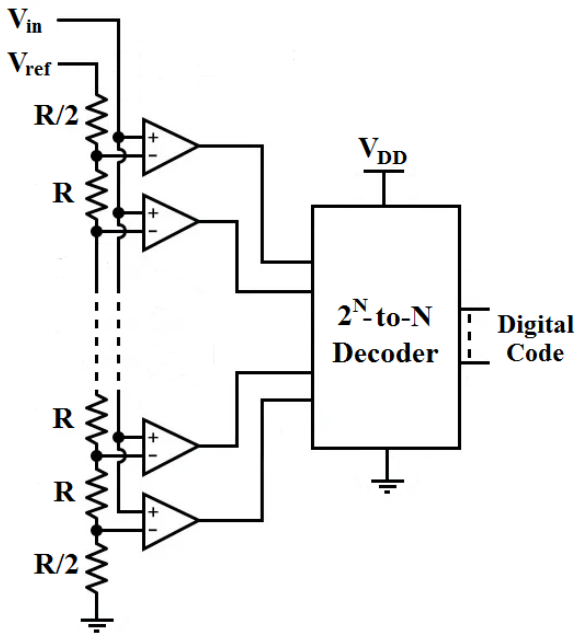


Figure 2.1. N-bit Flash ADC.

2.3.2 Successive Approximation Register (SAR) ADC

SAR-ADC is one of the most commonly used architectures because it gives better resolution with no more silicon area or more consumed power. This high resolution comes at the cost of the operation speed.

An N-bit SAR-ADC is shown in Fig. 2.2. It consists of a comparator, N-bit DAC and SAR. Its theory of operation depends on iteration process for the output bits starting from the Most Significant Bit (MSB) to the LSB.

First, the MSB is initialized by logic '1'. Then, the input voltage after being sampled is compared with the DAC output ($V_{ref}/2$) using the comparator. If the input voltage is greater than the DAC output the output

of the comparator will be “1”, the MSB remains “1” and the next bit will be executed by comparing the sampled input with the new DAC output ($V_{REF}/2 + V_{REF}/4$) at the next edge of the clock signal. Else, the output of the comparator will be ‘0’ and the MSB will be set to ‘0’. Then, the sampled input will be compared with the DAC output in this case at the next edge of the clock signal to determine the value of the next bit. This iteration process will be repeated until the LSB is executed and the End Of Conversion (EOC) signal becomes ‘1’. The operation procedure of this ADC is explained in the flowchart shown in Fig. 2.3.

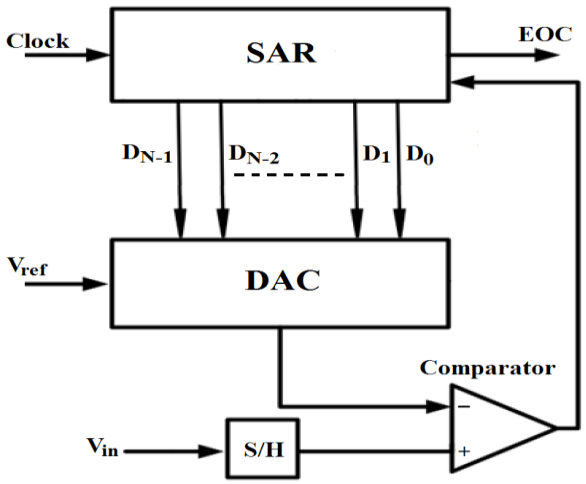


Figure 2.2. N-bit SAR-ADC.

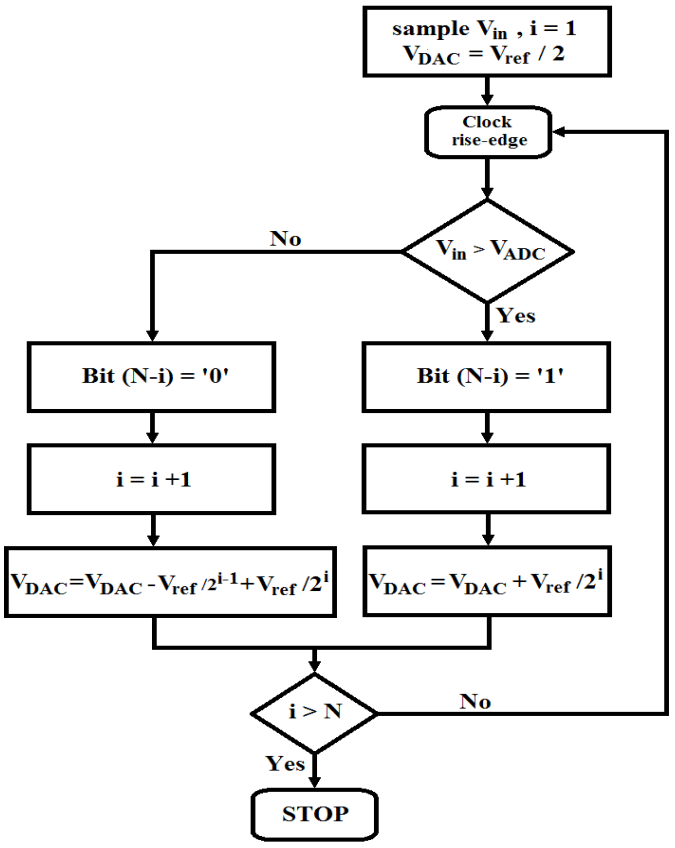


Figure 2.3. Operation flow chart for N-bit SAR-ADC.

For further illustration, take the input voltage range equals to 1volt (V_{ref} = 1), V_{in} = 0.6v and the SAR-ADC is a 4-bit ADC. The solution procedure is as follows:

Since $V_{in} > V_{ADC}$ ($V_{ref}/2$); (0.6 > 0.5), then the MSB (bit 3) is '1'. Since $V_{in} < V_{ADC} + V_{ref}$ /4; (0.6 < 0.5+0.25), then the next bit (bit 2) is '0'. Since $V_{in} < V_{ADC} + V_{ref}$ /8; (0.6 < 0.5+0.125), then the next bit (bit 1) is '0'. Since $V_{in} > V_{ADC} + V_{ref}$ /16; (0.6 > 0.5+0.0625), then the next bit (bit 1) is '1'.

Hence, the final digital output that represents the input voltage of 0.6 volts is '1001' which equivalent to 0.5 + 0.0625 = 0.5625V. This error difference decreases by increasing the number of bits (increasing resolution). Table 2.1, shows the voltage that corresponds to each bit.

Table 2.1. Equivalent voltage for each bit in SAR ADC.

Bit	Voltage (V)
3	0.5
2	0.25
1	0.125
0	0.0625

2.3.3 Pipeline ADC

Its theory of operation based on obtaining higher resolution by cascading many lower resolution ADCs together. This helps in reducing the complexity of the circuit and reducing the chip area used. As an example, when using 8-bit flash ADC, 255 comparators are needed. By using Pipeline ADC of 4 stages each stage is a 2-bit flash ADC; we can obtain the same resolution with only 12 comparators instead of 255 ones.

However, this simple architecture will be at the cost of latency. In another words, the delay time of pipeline ADC equals the sum of the delay time of each stage

Figure 2.4 shows a single stage of an (N×M)-bit pipeline ADC. First, the input signal is sampled then converted to a digital code using an N-bit ADC, then the N-bits digital code is reconverted into an analog signal using an N-bit DAC. This analog signal is then subtracted from the sampled input signal to produce the residue signal. This residue signal is

amplified by a gain of 2^N to convert it back to a full-scale signal to make it available for the next stage ADC. The shown stage is one of M- stages that form the (N×M) overall resolution.

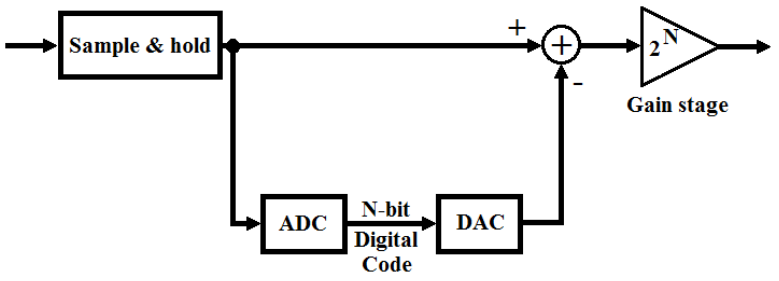


Figure 2.4. An N-bit single stage of (N×M) bit pipeline ADC.

2.3.4 Sigma Delta (SD) ADC

Its idea is based on oversampling for the input signal and reducing the error by the feedback system. Figure 2.5 shows a first order Sigma-Delta ADC. It consists of a summing node, integrator, ADC and a DAC feedback branch [12, 13].

First, the input voltage is summed with the output of the DAC feedback branch. This summing can be represented by a switched capacitor [12, 13].

Second, an integrator is used to add the present output value of the summing node with the previous value obtained at the previous integration step. After that a comparator converts the integrator output to a logic bit. The output of the comparator is “1” if the integrator output voltage is greater than or equal zero and vice versa. If the input signal is increasing, the comparator generates a greater number of "1" and vice versa if the input is decreasing [12, 13].

Finally, the 1-bit DAC at the feedback branch produces "+V_{ref}" value if the output of the comparator is "1" and "-V_{ref}" value otherwise. The loop is executed many times which results in high resolution but at the cost of latency. Further details about SD ADCs and their different architectures can be found in [14, 15].

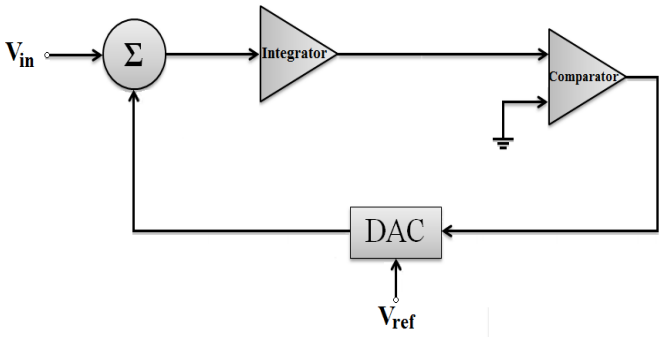


Figure 2.5. First order Sigma Delta (SD) ADC.

2.4 Performance Analysis

A study is made on about 1500 commercial ADCs to compare the performance of different architectures of ADCs in terms of sampling frequency, resolution, SNR, power consumption and FOM. These commercial ADCs are from the most popular integrated circuits' companies such as Texas Instruments and Analog Devices.

Figure 2.6 shows the resolution of ADCs versus the sampling frequency. It is obvious that sigma delta ADCs offer higher resolution than the other architectures while flash ADCs have the lowest resolution. Moreover, pipeline ADCs can be used for applications that need high sampling rates.

Figure 2.7 shows SNR of ADCs versus the sampling frequency. It is obvious that sigma delta ADCs have the highest SNR value. Figure 2.8 shows the power consumption of ADCs versus the sampling frequency. It can be concluded that pipeline ADCs consume higher power compared with other ADCs. Figure 2.9 shows FOM for ADCs. It indicates that SAR ADCs have the worst performance while pipeline ADCs have the best performance.

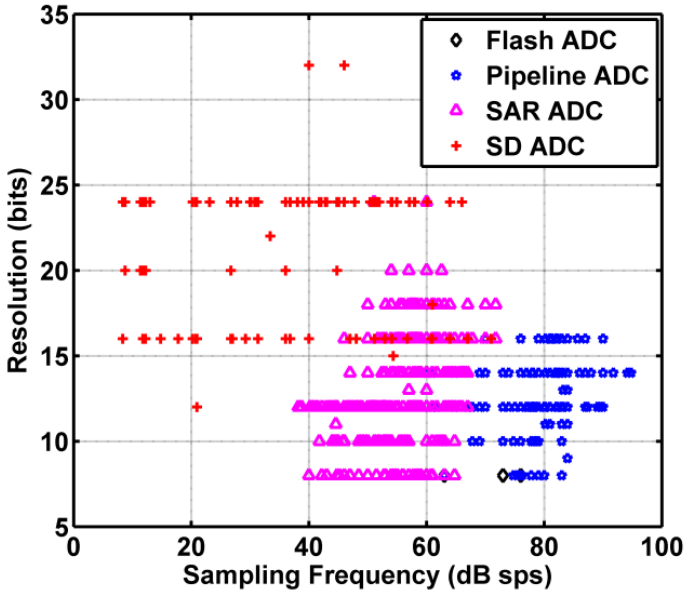


Figure 2.6. Resolution versus sampling frequency.

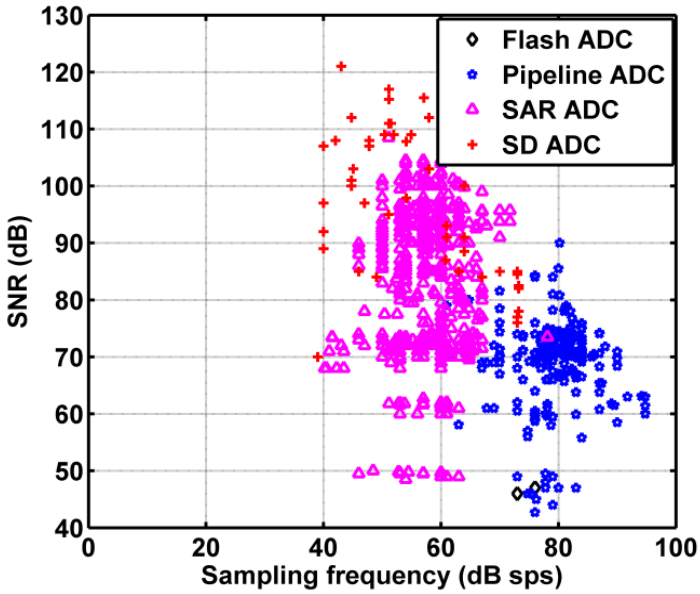


Figure 2.7. SNR versus sampling frequency.

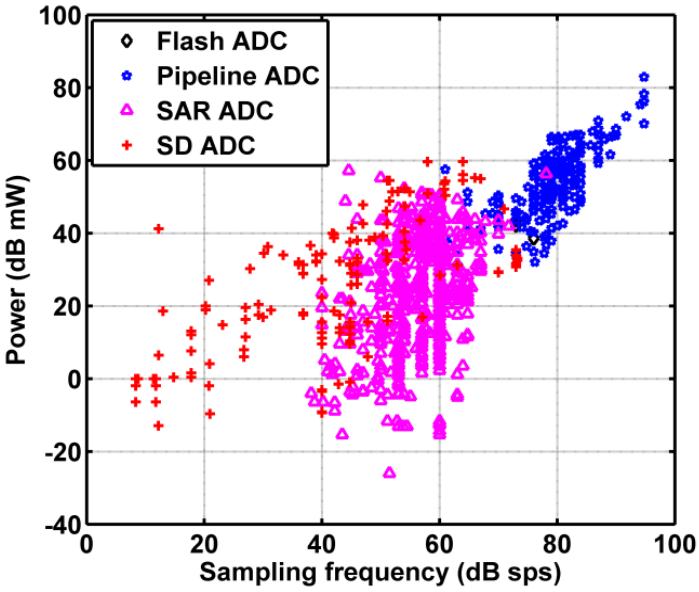


Figure 2.8. Power versus sampling frequency.

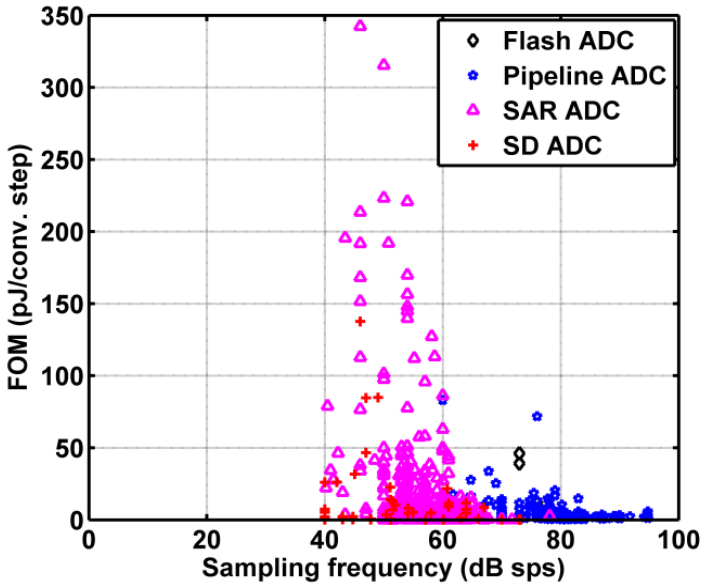


Figure 2.9. FOM versus sampling frequency.

Table 2.2 shows performance comparison for the commercial ADC architectures in terms of sampling rate, resolution, SNR, power consumption and FOM. It is concluded from the previous analysis that sigma delta ADCs have a promising performance in terms of resolution, SNR and power consumption. However, they suffer from low sampling frequencies. In the other hand, pipeline ADCs have high sampling rate but consume high power and have low SNR values.

Each of the previous four architectures has the best performance that fits specific application. In other words, sigma delta ADCs can be used for low power applications that require high precision at high latency while SAR ADCs can be used for low power, high speed applications. Moreover, pipeline ADCs are the most popular ADCs for applications that need high sampling rates but at the cost of power consumption and latency.

Table 2.2. Performance Comparison for the recent commercial ADC architectures.

Architecture	Sampling rate	Resolution	SNR	Power consumption	FOM
Flash	Moderate high	Low	Low	High	Moderate
SAR	Low	Moderate	Moderate high	Low	High
SD	Low moderate	High	High	Moderate	Moderate
Pipeline	High	Moderate	Low moderate	High	Moderate

2.5 Time-Based Analog-to-Digital Converters

Time-based Analog-to-Digital Converter (T-ADC) has gained researchers' interests nowadays as it represents an effective solution to the limitations that resulted from technology scaling.

In time-based ADC, the conversion process of the analog signal to a digital code is done in two steps. First, the input voltage signal is converted to a time signal which is proportional to the input signal value. Then, this delay signal is converted to a digital code. This conversion procedure helps the processing of the analog signal to be done in the time domain which is a great advantage because as a consequence of technology scaling, time resolution has been improved in nanometer-scale devices due to the reduction of gate delay.

Moreover, the delay signal can be processed using digital circuitry instead of the analog circuitry which results in reducing the area and the power consumption significantly. As an example, one of the most common time-based ADCs, the Voltage to Time Converter (VTC) based T-ADC, does not need a sample and hold circuit for the input voltage

signal which results in reducing the overall power consumption and the chip area by a great amount.

2.5.1 Time-Based ADC Architectures

The most common time-based ADC architectures are integrating ADC, Voltage-Controlled Oscillator (VCO) based ADC, Pulse Width Modulation (PWM) ADC and Voltage to Time Converter (VTC) ADC. These architectures are discussed below in details.

2.5.1.1 Integrating ADC

In this type of ADC, the input signal is integrated in time domain and a ramp signal is generated at the output terminal of the integrator. A counter is used to count the ramp signal edges and stops counting when the ramp signal goes to zero. Integrating ADC can be a single slope ADC [1] or a dual slope ADC [9]. Figure 2.10 shows a single slope integrating ADC. Although this design is robust, it operates at low speed and consumes high power.

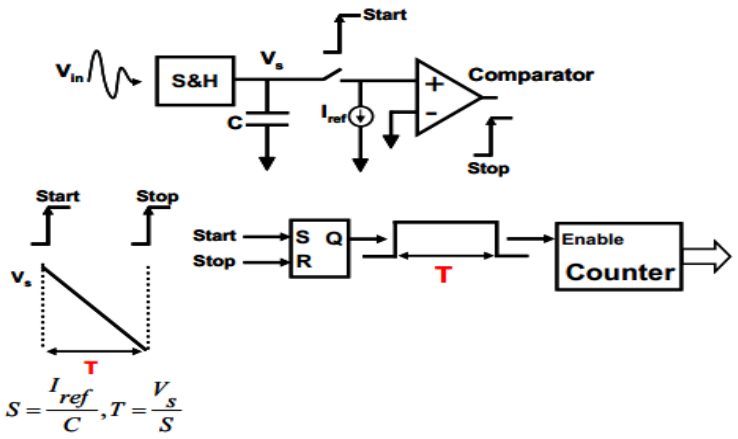


Figure 2.10. Single slope integrating ADC [1].

2.5.1.2 Voltage-Controlled Oscillator (VCO) Based ADC

In this ADC, the input analog signal is converted to a frequency signal using a VCO at which its output frequency is controlled by the input signal amplitude. Then, the frequency signal can be converted to a digital code using numerous techniques [16-19] such as using a counter and D-flip flops for the conversion [1]. Figure 2.11 shows a simple model of VCO-based ADC. The main advantage of this ADC is that digital circuits can be used along with the VCO and no analog circuitry required. However, this design faces two challenging limitations that affect its performance. These limitations are the VCO non-linearity and the sensitivity of this design to Process, Voltage and Temperature (PVT) variations [1, 9].

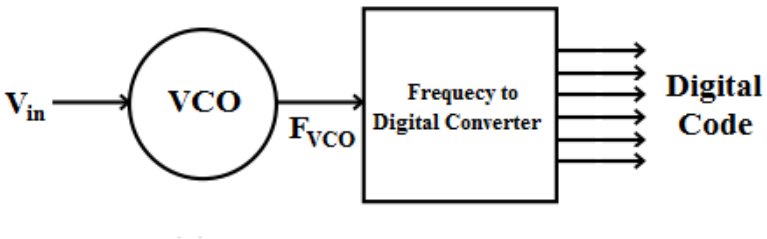


Figure 2.11. VCO based ADC.

2.5.1.3 Pulse Width Modulation (PWM) ADC

In this ADC, the analog input signal is pulse width modulated to a time domain signal. Then the time signal can be quantized using a counter [20]. The non-linearity of the PWM results in a distortion in the time signal. This distortion can be reduced by using a modulating frequency of at least eight times the bandwidth [21]. Figure 2.12 shows a simple block diagram of PWM ADC.

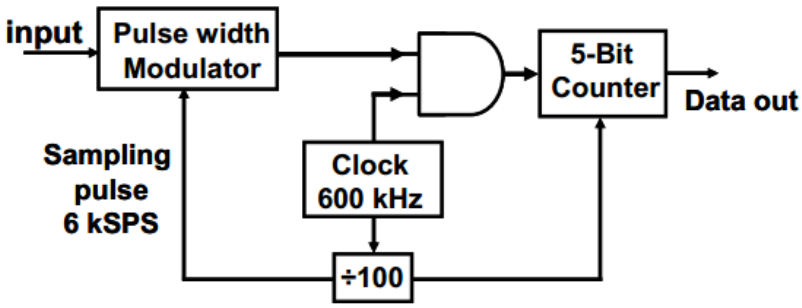


Figure 2.12. PWM ADC [20].

2.5.1.4 Voltage to Time Converter (VTC) Time Based ADC

VTC based T-ADC consists of two stages as shown in Fig. 2.13. The first stage is a Voltage to Time (VTC) converter that converts the input signal to delay pulses. The delay in each pulse is proportional to the input voltage signal value. The second stage is a Time-to-Digital Converter (TDC) that converts these delay pulses to a digital code. The VTC theory of operation is discussed below and the recent research that is done to improve its performance specifically increasing the output linearity.

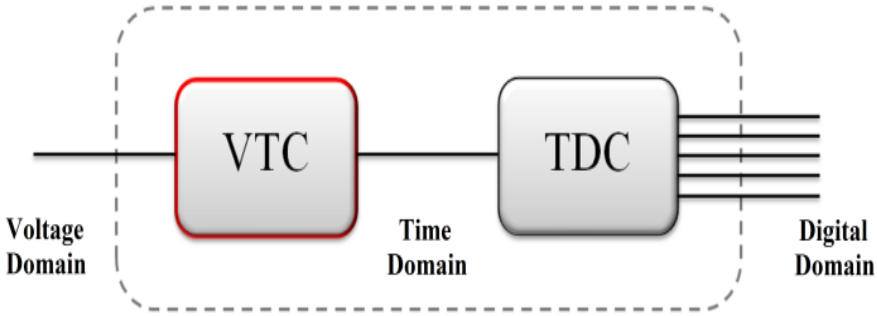


Figure 2.13. VTC based T-ADC.

A. Voltage to Time Converter (VTC)

There are numerous circuits that convert the voltage signal to delay-time signals. One of these circuits is the Ramp-and-Comparator-Based VTC explained in [9]. But, the most common circuit used is the current starving inverter circuit shown in Fig. 2.14. It consists of a CMOS inverter with an NMOS starving transistor connected to the driver branch which is controlled by the analog input signal (V_{in}) [22].

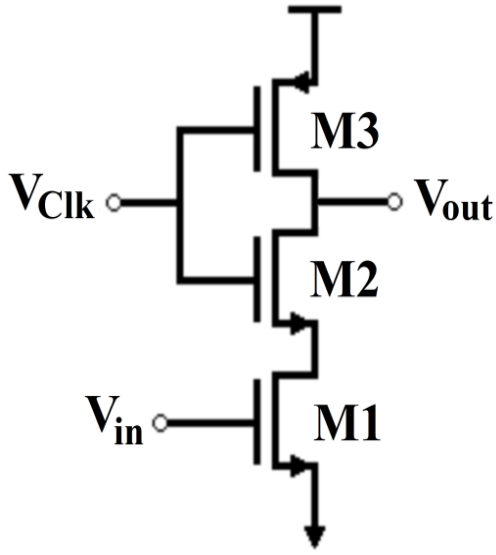


Figure 2.14. The current starving inverter circuit.

The input signal which is connected to the gate of the starving NMOS transistor controls the current of the driver branch during fall time. In other words, the fall time of the output voltage of the inverter is proportional to the input voltage signal. When the value of the input signal increases, the fall time of the output signal increases and vice versa. Figure 2.15 shows the fall time of the inverter for different input voltages. The rise time of the inverter output can be also controlled

instead of the fall time by connecting a PMOS transistor with the load branch of the inverter as shown in Fig. 2.16 [2].

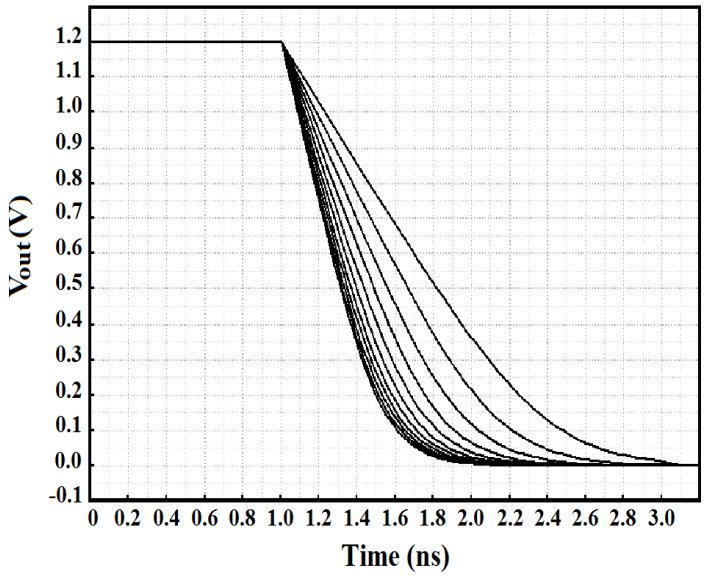


Figure 2.15. Fall-time of the output voltage of the conventional VTC for input voltage range from 0.7V to 1.2V at supply voltage of 1.2V.

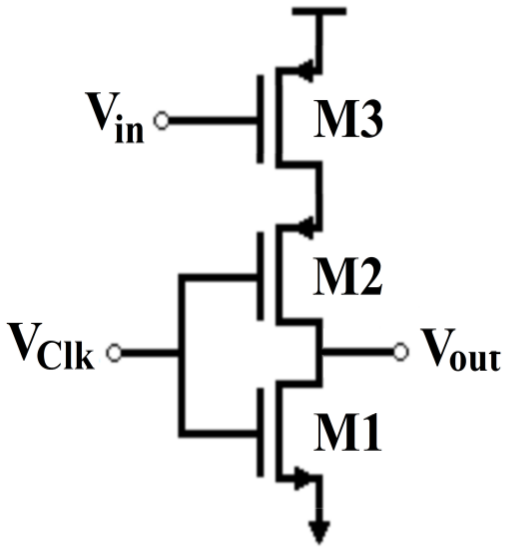


Figure 2.16. Rise-time current starving inverter VTC.

B. VTC Performance Limitations

The current starved inverter VTC suffers from severe limitations that affect the conversion process of the input signal. These limitations are listed as follows:

1. Limited Dynamic Range

The input signal can't have small values because it is connected to the gate of the starving NMOS transistor. Thus, its value must be greater than the threshold voltage of the transistor for the transistor to be 'ON' to create a path for the output to ground.

In order to overcome this problem, a weak transistor (with small aspect ratio) is connected in parallel with the starving transistor at which its gate is connected to the supply voltage [2, 23]. This weak transistor is always 'ON' to guarantee that there is a path for the output to ground even for small values of the input voltage. Figure 2.17 shows the addition of a weak transistor M4 for the VTC to operate at small input values.

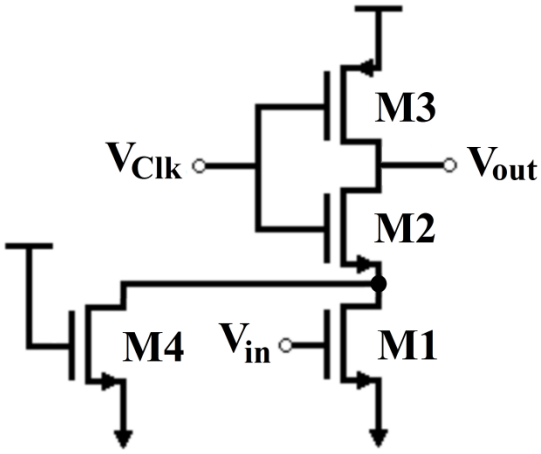


Figure 2.17. VTC with weak transistor M4.

Moreover, the upper limit of the dynamic range is limited as it affects the linearity of the circuit response. In other words, the fall time of the output signal becomes more non-linear with respect to the input signal when the value of the input voltage increases. This point will be discussed below in details and how to overcome it.

2. Non-Linearity Effects

One of the biggest challenges in the design of VTC circuit is the non-linearity that appears in the fall time delay of the output response for high input values [23]. It is obvious from Fig. 2.15 that when the input voltage increases, the delay curves for the output becomes more non-linear which results in inaccurate conversion of the input signal to digital code.

This non-linearity happens because during the fall time of the output signal, the starving transistor will be operating in saturation mode with a current of:

$$I_D = \frac{K'}{2} \times \frac{W}{L} (V_{GS} - V_{th})^2 \quad (2.8)$$

Where $V_{GS} = V_{in}$, W/L is the aspect ratio of the transistor, k' is a constant and V_{th} is the threshold voltage of the starving transistor.

Also,

$$I_D = C \frac{dV}{dt} \quad ==> \quad dt = C \frac{dV}{I_D} \quad (2.9)$$

Where C is the parasitic capacitance at the output node, dV is the voltage change at the output during discharging from '1' to '0' and dt is the delay fall time of the output.

From the two previous equations we can conclude that the relation between the input voltage and the output delay time is non-linear and this non-linearity increases by increasing the input voltage.

C. Time to Digital Converter (TDC)

Time-to-Digital Converter (TDC) converts the delay signal that produced by the VTC into a digital code for a complete analog to digital conversion process. The performance of the TDC should be investigated as it limits the performance of the whole ADC in terms of linearity, resolution and power consumption.

The most important parameters that represent the linearity in the whole ADC are Differential Non-Linearity (DNL) and Integral Non-Linearity (INL). DNL is defined by the conversion step deviation from its ideal value (1LSB) in ADCs. INL is defined by the deviation of the whole transfer function of the ADC from its ideal value [24]. The maximum value of DNL should not exceed 1LSB to avoid missing codes [24].

There are many TDC architectures that have been proposed to improve the resolution without affecting the linearity of the ADC. The most common types of TDCs are discussed below in details. The advantages and disadvantages of each type are also discussed.

1. Delay Line Based TDC (Flash TDC)

Flash TDC architecture is shown in Fig. 2.18. It consists of cascaded buffer stages with a delay unit before each stage [9]. The buffer consists of a D-flip flop with two inputs; the start and the stop signals. The start signal represents the input delay signal that comes from the VTC. The

difference between the start and the stop signal represents the time range of the input delay signal. Each delay unit has more delay than the previous one by t_d which represents the resolution of the TDC or LSB (the minimum delay time that can be detected by the TDC).

The start signal which represents the input delay signal passes through the buffer stages. It activates the number of flip-flops that resembles its delay value. Then the stop signal arrives and the activated flip-flops record logic '1' as their current states. The output of the flip-flops is a thermometer code which is converted to a digital code using a decoder.

The most important drawback of this architecture is the trade-off between the speed and resolution [9]. For higher resolution, the number of buffer stages is increased (as t_d decreases) which reduces the speed of operation for the TDC.

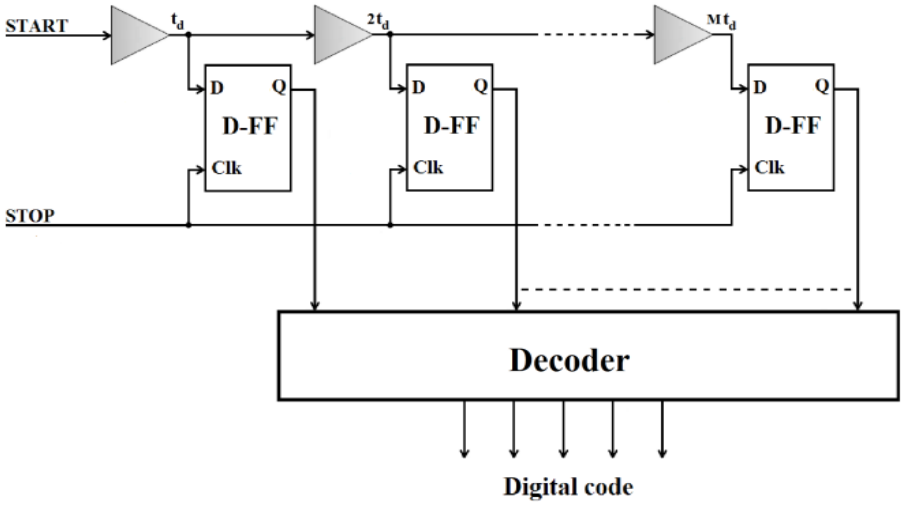


Figure 2.18. Flash TDC.

2. Vernier Delay-Line Based TDC

This architecture has solved the problem of having a small resolution less than the minimum gate delay in the technology used. Its architecture is shown in Fig. 2.19. Both the start and stop signals have delay units in their path but with different values making the stop signal path faster than the other. The difference between the delay units of the two paths equals to the resolution of the TDC (LSB).

The stop signal comes after the start signal with a delay time chosen to be equal to the maximum delay of the input signal ((M+1) × LSB).

As the start signal starts to pass through the buffer stages, the output of the D flip-flop is set as "High" if the start signal comes before the stop signal. Once the stop signal reaches the start signal, the output of the flip-flops which is a thermometer code is converted to a digital code using a decoder.

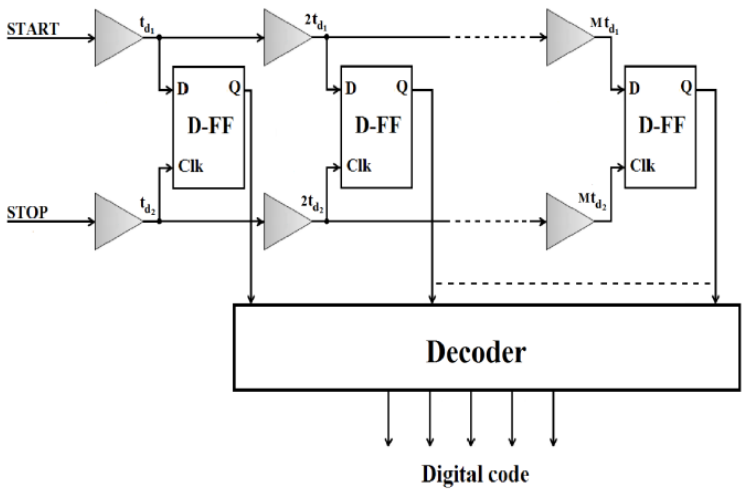


Figure 2.19. Vernier delay-line TDC.

Vernier delay-line TDC has the advantage of its high resolution that can be less than the minimum gate delay in the technology used. However, this architecture suffers from significant drawbacks such as transistors' mismatch, noise and delay line physical length [25]. Many research is done [26-31] to achieve higher resolution that can reach 2ps [31].

3. Hybrid TDC

In the Vernier Delay-line based TDC, we can only measure short time range with high resolution. With the hybrid TDC, we can measure large time range with high resolution. This can be achieved by using a counter with the delay line to increase the time range used. The delay line TDC is employed as a fine quantizer to resolve the residual error of the counter measurement. More details about the structure and architecture of hybrid TDCs are available in [32].

D. Novel Trends in VTC Design

Research now is focusing on improving the performance of the VTC circuit rather than the TDC circuit as the non-linearity of the VTC is much large and affects the linearity of the following TDC stage. Hence, this thesis focuses on the novel trends in the design of VTC circuits.

A lot of research is done to improve the performance of the VTC circuit. Circuits in [23], [33-41] and [6] are proposed to overcome the previously mentioned limitations of the conventional VTC circuit. In [23], a linearization circuit is proposed to achieve a maximum linearity error of 2%. However, it has a limited input dynamic range of only 200mV.

A VTC circuit is proposed in [33] which operates at a high sampling rate of 5GS/s but consumes high power of 3.6mW and has only 100mV input dynamic range. The VTC proposed in [34] is a modification to the VTC circuit in [33] in order to increase the input dynamic range to 140mV which is still insufficient.

In [35], the theory of operation of the proposed VTC circuit is modified at which the input signal is compared with a voltage ramp signal. This design has the advantage of low power consumption but operates at a small sampling frequency of 1MHz. In [36], a differential input is applied to the proposed VTC circuit to achieve a maximum linearity error of 3%. However, the input dynamic range is still very small (172 mV).

In [6], a Voltage-to-Frequency Converter (VFC) is proposed and a 3% maximum linearity error is achieved. However, this design suffers from small input dynamic range of 320mV and consumes high power of 477μW. In [37], the linearity of the VTC is improved by adding track-and-hold circuit, level shifter and a pulse shape restorer. However, the improved linearity is not sufficient and the proposed VTC consumes high power. In [38], a VTC with a two-step transition inverter delay line is proposed which consumes 180μW of power. However, the proposed VTC has very low sensitivity of 0.1ps/mV.

In [39], a current-to-time converter (CTC) is proposed which achieves a maximum linearity error of 2.1%. However, the sampling rate is very small (50MS/s). In [40], although the proposed VTC achieves a better dynamic range of 400mV, the power consumption of this design is

relatively high (3.35mW). In [41], a fully digital time-based ADC is proposed to reduce the chip area at which the power consumption is reduced to 380μW.

Chapter 3

Proposed VTC Circuits

The theory of operation for the proposed circuits is based on the body biasing technique at which the input signal is connected to the body terminal of the starving transistor. The body biasing technique results in a highly linear drain current with respect to the body-to-source voltage of the starving transistors, as proven below.

The body biasing technique can be applied on a falling-time starving inverter at which the starving transistor is NMOS. In addition, it can be applied on a rise-time starving inverter at which the starving transistor is PMOS. Both cases are discussed below in detail.

3.1 First Proposed VTC

The proposed circuit is introduced as shown in Fig. 3.1. The input signal is applied to the body terminal of the NMOS starving transistor. The output load capacitance C_L equals to 30fF (for FO4).

In this VTC, the threshold voltage of the starving transistor, V_T, is a function of the body-to-source voltage (which represents the input signal) and is given by:

$$V_T = V_{To} + \gamma\left(\sqrt{|2\emptyset_f - V_{BS}|} - \sqrt{|2\emptyset_f|}\right) \quad (3.1)$$

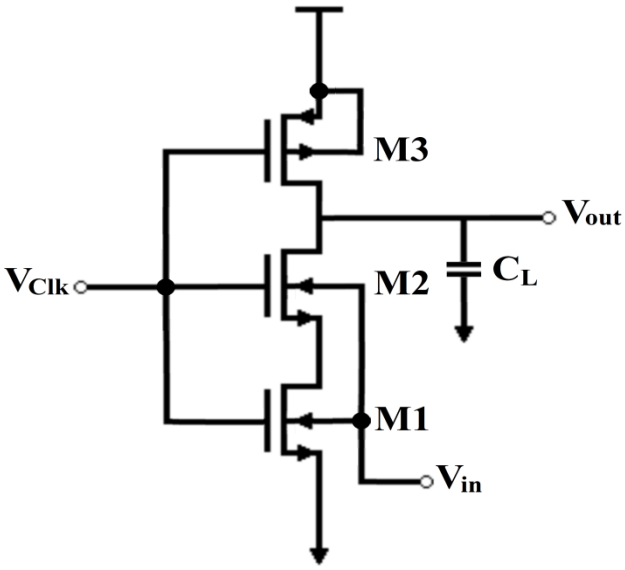


Figure 3.1. First proposed voltage-to-time converter (VTC) circuit.

Where V_{To} is the zero-bias threshold voltage, γ is the body effect factor, V_{BS} is the body-to-source voltage and $\emptyset_f$ is the Fermi potential.

The following analytical proof shows that the body biasing provides a linear relation between the drain current of the starving transistor (which represents the discharging current of the output load capacitance) and the body-to-source voltage. The proof is derived as follows:

$$\because\ I_D = \frac{K_n}{2}\ (V_{GS} - V_T)^2 \tag{3.2}$$

$$\therefore I_D = \frac{K_n}{2}\left({V_{GS}}^2 - 2V_{GS}V_T + {V_T}^2\right) \tag{3.3}$$

$$\because V_T = V_{To} - \gamma\sqrt{\left|2\emptyset_f\right|} + \gamma\sqrt{\left|2\emptyset_f - V_{BS}\right|} \tag{3.4}$$

$$\therefore V_T = V_{To} - \gamma\sqrt{\left|2\emptyset_f\right|} + \gamma\sqrt{\left|2\emptyset_f\right|}\sqrt{\left|1 - \frac{V_{BS}}{2\emptyset_f}\right|} \tag{3.5}$$

$$\because \sqrt{1+x} \cong 1 + \frac{x}{2} \quad , for\ x < 1 (Taylor\ series\ expansion) \tag{3.6}$$

$$\therefore V_T = V_{TO} - \gamma\sqrt{|2\emptyset_f|} + \gamma\sqrt{|2\emptyset_f|}\left(1 - \frac{V_{BS}}{2|2\emptyset_f|}\right) \tag{3.7}$$

$$\therefore V_T = V_{TO} - \gamma\sqrt{|2\emptyset_f|}\left(\frac{V_{BS}}{2|2\emptyset_f|}\right) \tag{3.8}$$

$$\therefore V_T = V_{TO} - \left(\frac{\gamma}{2\sqrt{|2\emptyset_f|}}\right)V_{BS} \tag{3.9}$$

$$\therefore {V_T}^2 \cong {V_{TO}}^2 - \left(\frac{V_{TO}\gamma}{\sqrt{|2\emptyset_f|}}\right)V_{BS} \tag{3.10}$$

Substitute (3.9) and (3.10) into (3.3):

$$\therefore I_D \cong K_1 + K_2 V_{BS} \tag{3.11}$$

Where,

$$K_1 = \frac{K_n}{2}(V_{GS} - V_{TO})^2 \tag{3.12}$$

$$K_2 = \frac{K_n\gamma}{2\sqrt{|2\emptyset_f|}}(V_{GS} - V_{TO}) \tag{3.13}$$

From (3.11) and (2.9):

$$dt = \frac{C\ dV}{K_1 + K_2 V_{BS}} \tag{3.14}$$

Multiplying both numerator and denominator by the factor $(k_1 - k_2 V_{BS})$, the fall time delay will be equal to:

$$dt = \frac{K_1 C\ dV}{{K_1}^2 - {K_2}^2 {V_{BS}}^2} - \frac{K_2 C\ dV\ V_{BS}}{{K_1}^2 - {K_2}^2 {V_{BS}}^2} \tag{3.15}$$

Since V_{BS} is dominant over V_{BS}^2 for values below 1, it is clear that the fall time delay (discharging time) of the output signal is linearly proportional to the input signal voltage which is applied to the body terminal.

Adding more series-identical NMOS transistors to the starving transistor helps in improving the performance of the circuit in two ways. First, the overall (W/L) of the series NMOS transistors is decreased as follows:

$$\left(\frac{W}{L}\right)_{total} = \left(\frac{W}{L}\right)/N \tag{3.16}$$

Where N is the number of NMOS series transistors. This results in decreasing the discharge current which means that the delay time for the fixed voltage step of the input signal increases. Hence, the resolution of the proposed VTC circuit increases. Second, adding more series NMOS transistors decreases the gate-to-source voltage of the driver transistor M1. This guarantees that the driving transistor is kept in saturation to maintain linearity during all the discharging period of the output load capacitor.

Figure 3.2 shows the output delay of the proposed VTC circuit for different number of series starving transistors (N). It is obvious that when the number of series starving transistors increases, the output delay range increases and the sensitivity (the rate of change of the output delay with respect to the input voltage) increases as well. The number of series starving transistors cannot exceed six for a clock frequency of 500MHz as the output voltage will not have enough time to go logic ‘0’. For more

series starving transistors, the clock frequency should be reduced for proper operation.

Figure 3.3 shows the sensitivity of the proposed VTC circuit versus the number of series starving transistors (N). For N having the values of four, five and six, the resolution of the proposed VTC will be 5 bits (for a least significant bit (LSB) of 5ps). Four starving transistors are used for the final architecture of the proposed VTC circuit as it has a lower quantization error than having more starving transistors. Figure 4.3 shows the final architecture of the proposed VTC circuit.

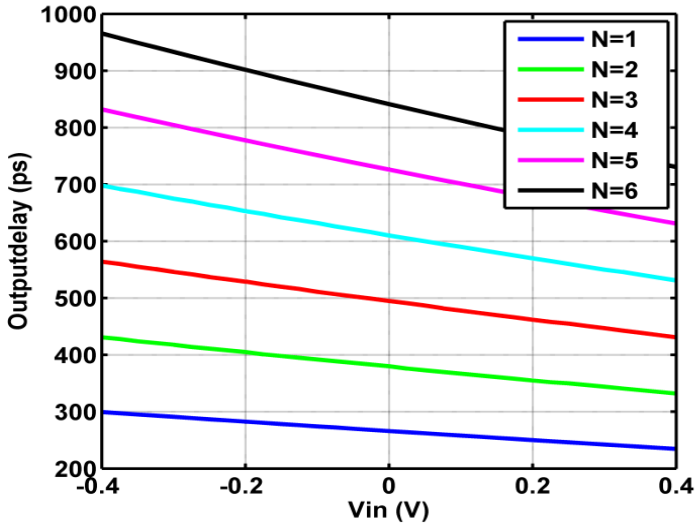


Figure 3.2. Output delay for different number of series starving transistors (N).

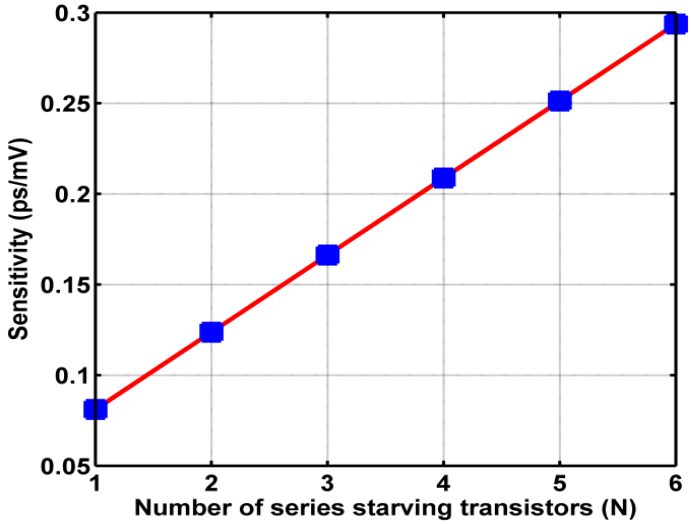


Figure 3.3. Sensitivity versus the number of series starving transistors (N).

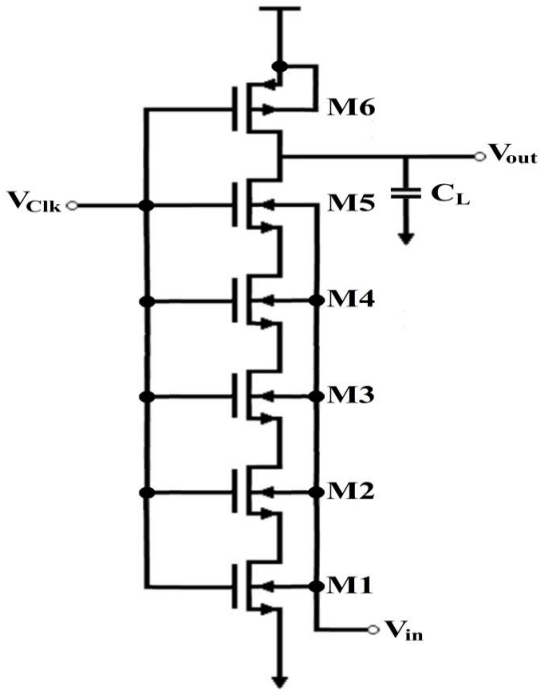


Figure 3.4. Final architecture of the first proposed VTC circuit.

The Forward Body Bias (FBB) voltage is limited by the forward biasing of the drain-bulk junction (the positive bound of the input voltage connected to the p-Well in case of NMOS and the negative bound of it below the supply voltage connected to the n-Well in case of PMOS). The FBB is also limited by the sub-threshold leakage current [42]. Moreover, the Reverse Body Bias (RBB) voltage bound is determined by the junction leakage current. In case of NMOS, the RBB voltage bound is the negative bound of the input voltage, connected to the p-Well, and the positive bound of over the supply voltage, connected to the n-Well in case of PMOS [42].

The upper limit of the FBB voltage is 0.6V for latch-up free operation in 65nm CMOS technology with a supply voltage that ranges from 0.9 to 1.2V [42–44]. SPICE simulations are done by sweeping the FBB voltage of the PMOS transistor. These simulations show that the upper limit of the FBB voltage equals 0.59V in order to prevent latch-up triggering for the NMOS transistor. Thus, the maximum FBB voltage is chosen to be equal to 0.4V to avoid latch-up in case of FBB voltage fluctuations around 0.4V. Moreover, the RBB voltage is also selected to be equal to 0.4V. Hence, the FBB and the RBB maximum body voltages are chosen to be equal to ±0.4V for NMOS devices and 1.2 ± 0.4V for PMOS devices [42, 45].

Thus, the input signal range is taken form −0.4 to 0.4V, resulting in a full range of 800mV. The maximum value of the input signal is 0.4V to avoid latching up [42, 45, 46]. In other words, a short circuit path occurs between the supply voltage and ground when the body-to-source voltage

exceeds 0.4V in BULK-CMOS technology. This leads to a high current to pass, which results from parasitic bipolar devices in the CMOS circuits.

Latch-up can be avoided during the fabrication process by isolating NMOS and PMOS devices using an oxide trench along with a buried oxide layer. In addition, it can be avoided by increasing the spacing between CMOS devices, although this reduces packing density.

3.2 Second Proposed VTC

The second proposed VTC circuit has the same theory of operation as the first proposed VTC. However, the body biasing technique is applied on a rise-time starving inverter at which the starving transistor is PMOS. As it was proven before in the first proposed VTC, it is concluded that the rise time delay (charging time) of the output signal is linearly proportional to the input signal voltage which is applied to the body terminal.

Figure 3.5 shows the second proposed VTC circuit. Adding more series-identical PMOS transistors to the starving transistor helps in improving the performance of the circuit. The output delay of the proposed VTC circuit for different number of PMOS series starving transistors (N_P) is shown in Fig. 3.6. The maximum number of series PMOS transistors that can be used is four for a clock frequency of 500MHz. The sensitivity of the proposed VTC is shown in Fig. 3.7. For a 5-bit resolution VTC, four series PMOS starving transistors are used for better sensitivity and lower quantization noise.

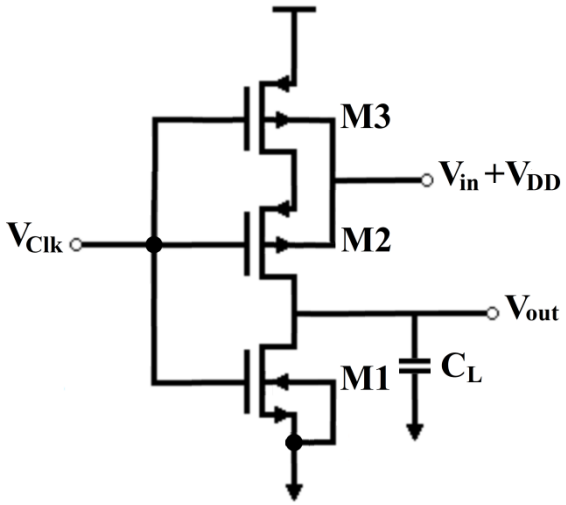


Figure 3.5. Second proposed VTC circuit.

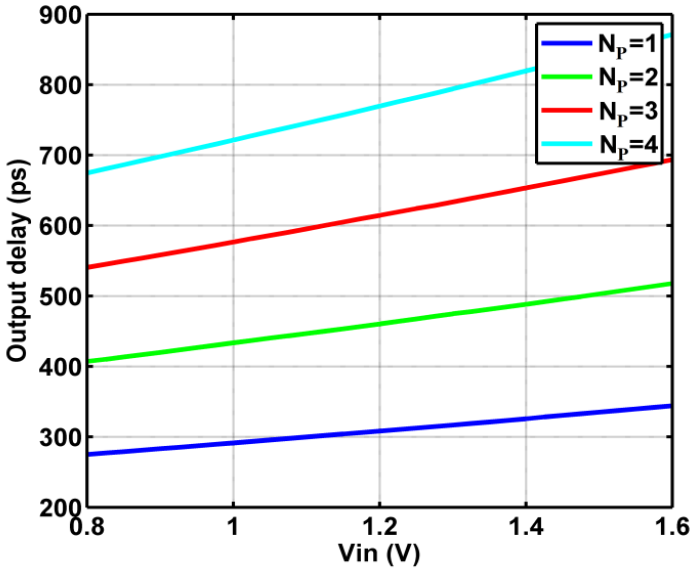


Figure 3.6. Output delay for different number of series starving transistors (N_P).

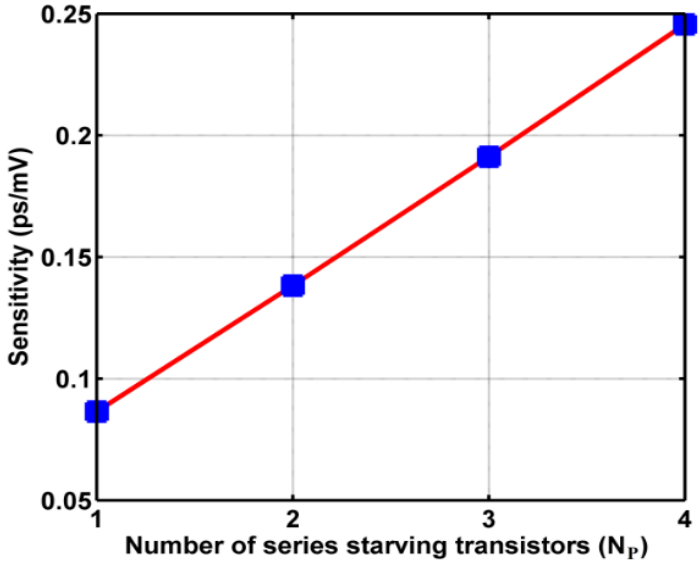


Figure 3.7. Sensitivity versus the number of series starving transistors (N_P).

Figure 3.8 shows the final architecture of the second proposed VTC circuit. The input signal (V_{in}) in the second proposed VTC ranges from −0.4 to 0.4V with an offset voltage of V_{DD}. This offset voltage is added as the source of the starving PMOS transistor is connected to V_{DD} keeping the body-to-source voltage (V_{BS}) equal to V_{in}. This input dynamic range ensures that the body-to-source voltage does not exceed 0.4V to avoid latching-up [42, 45, 46].

There are several circuits that can be used to add the supply voltage (V_{DD}) to the input signal (V_{in}). One of these circuits is the non-inverting summing amplifier shown in Fig. 3.9. In this circuit, the input signal (V_{in}) and the supply voltage (V_{DD}) are connected to the positive port of the operational amplifier. The resistors used in this circuit are identical to make the output of the amplifier equal to (V_{in} + V_{DD}). This circuit is implemented off-chip on the PCB (Printed Circuit Board).

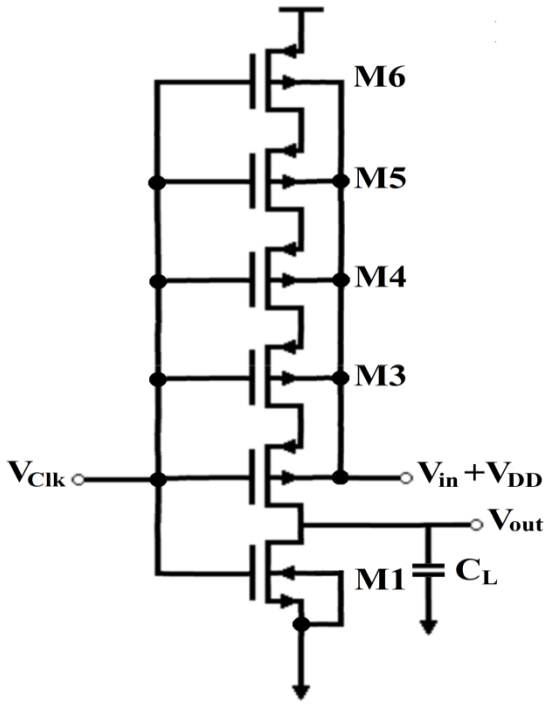


Figure 3.8. Final architecture of the second proposed VTC circuit.

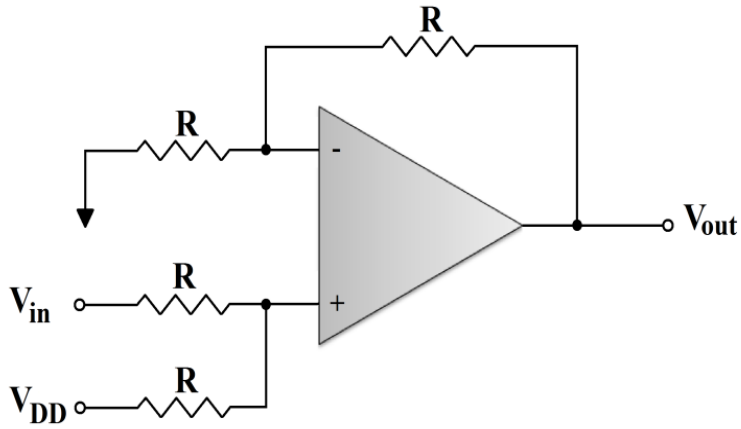


Figure 3.9. Non-inverting summing amplifier circuit.

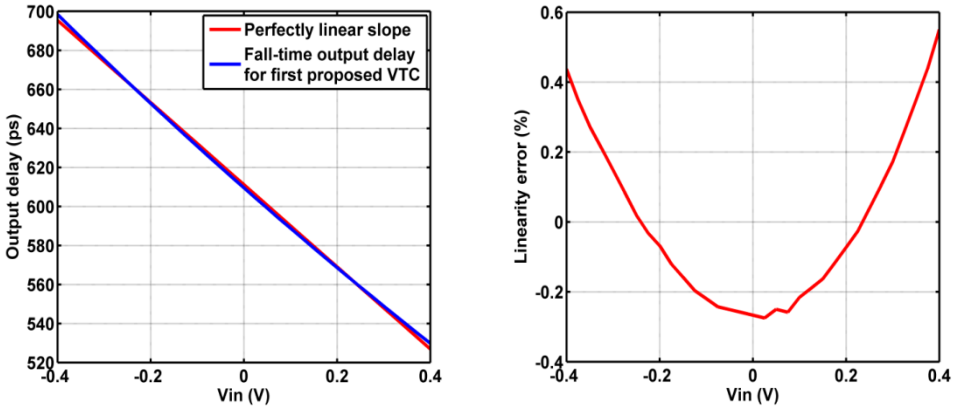
3.3 Simulation Results

The proposed VTC circuits are simulated using Cadence Virtuoso with industrial hardware-calibrated 65nm transistor device models provided by TSMC. The simulation is performed using a supply voltage of 1.2V. The Least Significant Bit (LSB), which is mainly dependent on the TDC block, is assumed to be equal to 5ps, resulting in a resolution of 5 bits for the proposed VTC circuits. The clock frequency equals to 500MHz and the frequency of the input signal equals to 72.75MHz. The size of all NMOS transistors used in the two proposed designs is identical and equal to (120 nm/60 nm). This is the minimum allowable size to achieve high output delay range for better resolution. The size of all PMOS transistors is twice that for the NMOS transistor and equals to (240 nm/60 nm). We are discussing below the simulation results for the most important parameters that affect the performance of the VTC circuit.

3.3.1 Linearity

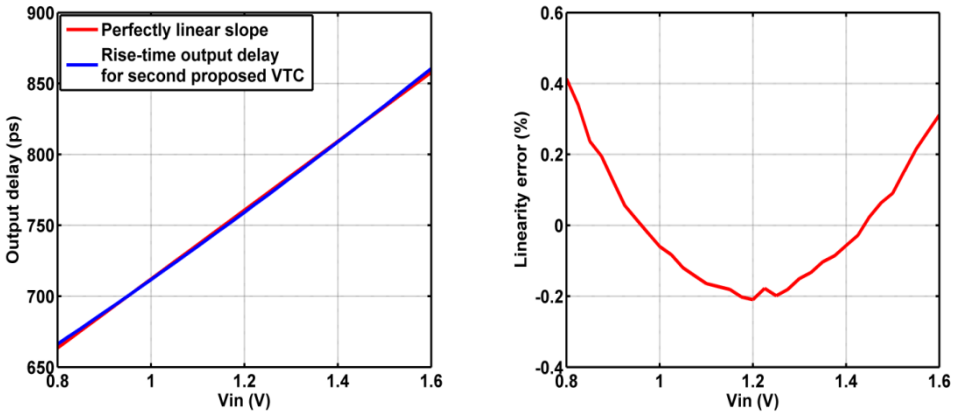
For the first proposed VTC, the fall time of the output delay is plotted and compared with a perfectly linear slope as shown in Fig. 3.10a. The linearity error percentage is shown in Fig. 3.10b. It is obvious that the maximum linearity error significantly decreased to about 0.55% which shows a great improvement in reducing the linearity error.

For the second proposed VTC, the rise time of the output delay is plotted and compared with a perfectly linear slope as shown in Fig. 3.11a. The linearity error percentage is shown in Fig. 3.11b. It is obvious that the maximum linearity error significantly decreased to about 0.4% which is the minimum reported linearity error up to the authors' knowledge.



(a) (b)

Figure 3.10. (a) Output delay versus a perfect linear slope for the first proposed VTC; (b) Linearity error percentage for the first proposed VTC.



(a) (b)

Figure 3.11. (a) Output delay versus a perfect linear slope for the second proposed VTC; (b) Linearity error percentage for the second proposed VTC.

3.3.2 Signal-to-Quantization Noise Ratio (SQNR)

SQNR is a very important parameter that affects the ADC performance as it represents the effect of noise on how the input signal is correctly processed. SQNR is calculated as follows:

1- A sinusoidal input signal (with a peak-to-peak voltage equals to the input dynamic range) is applied to the VTC. The clock signal applied represents the sampling frequency.
2- The output delay at the sampling points is calculated using cadence calculator.
3- 1024 sampling points are taken and coherent sampling is applied to evaluate accurate results.
4- An ideal TDC circuit is evaluated to convert the output delay to a digital code using MATLAB program. .
5- Then an ideal DAC circuit is applied to evaluate the output voltage signal using MATLAB program.
6- Fast Fourier Transform (FFT) is applied to the output signal and SQNR is calculated.

Figure 3.12 shows the SQNR for different input frequencies. It is obvious that for the effective number of bits (ENOB) to be greater than four, the maximum input frequency is equal to 105MHz for the first proposed VTC and 95MHz for the second proposed VTC.

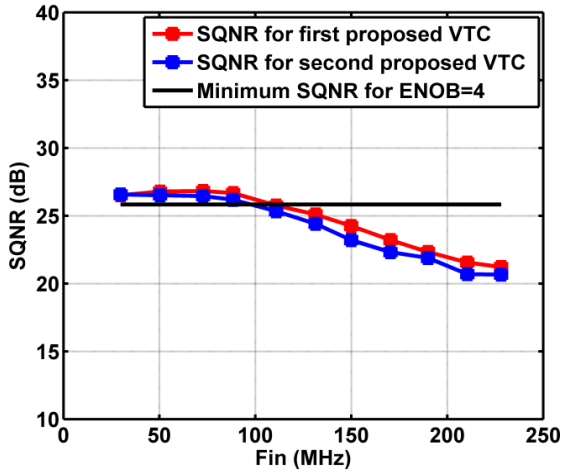


Figure 3.12. SQNR for different input frequencies.

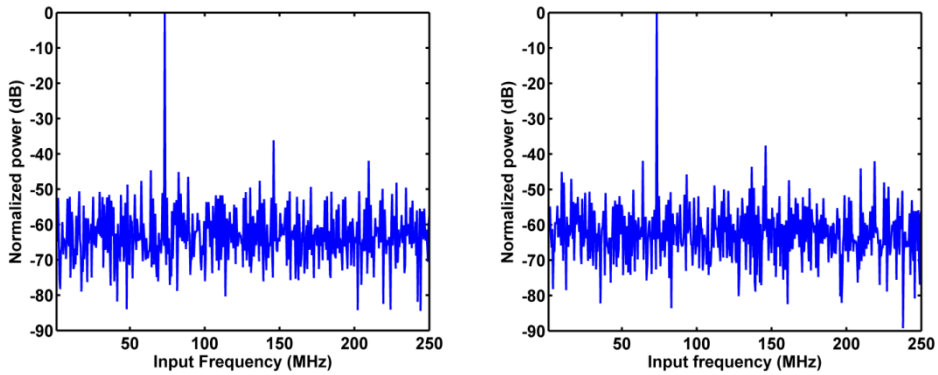
3.3.3 ENOB

Effective number of bits (ENOB) is calculated from SQNR using Eq. 2.4 for an input sinusoidal signal at a frequency of 72.75MHz and clock frequency of 500MHz. This specific value for the input frequency is chosen to ensure coherent sampling is achieved for more accurate results [22]. ENOB equals 4.1637 for the first proposed VTC and 4.1017 for the second proposed VTC. The frequency spectrums of the first and second proposed circuits are shown in Fig. 3.13.

3.3.4 Power Consumption

Figure 3.14 shows the power consumption for the proposed VTCs at different input frequencies. It is obvious that the second proposed VTC circuit exhibits lower power consumption than that for the first proposed VTC circuit. The proposed circuit provides very low power consumption, due to its novelty in using the body terminal as an analog input terminal to improve the linearity. This is because usually, the body terminal carries

very low current and accordingly, adds insignificant power consumption [42, 45]. At an input signal frequency of 72.75MHz, the proposed VTCs consume very small power of 18µW for the first proposed VTC and 15µW for the second proposed VTC.



(**a**) (**b**)

Figure 3.13. (a) Frequency spectrum for the first proposed VTC at F_{in} = 72.75MHz; (b) frequency spectrum for the second proposed VTC at F_{in} = 72.75MHz.

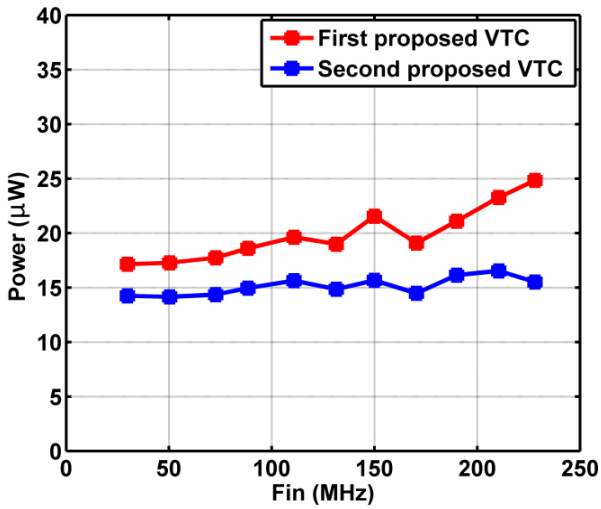


Figure 3.14. Power consumption for different input frequencies.

3.3.5 FOM

Figure of merit (FOM) represents the efficiency of the VTC in terms of the power consumption, sampling frequency and the input dynamic range. It is expressed by Eq. 2.5 and Eq. 2.6. Table 3.1 shows a comparison between the proposed VTC designs and other modified VTCs [7, 8, 47–54]. It indicates that both proposed VTCs have the minimum power consumption while having a wide dynamic input range and better FOM values.

3.4 Process-Voltage-Temperature (PVT) Variations

PVT variations are considered the most important factors that affect the performance of the proposed VTC circuits. These variations are discussed below in details.

3.4.1 Process Variations

Process variations are very important factors that measure the performance of the VTC circuit. They affect the output delay of the circuit. Hence, the linearity of the VTC and ENOB are also affected. The performance of the proposed circuits is investigated in terms of maximum linearity error, sensitivity and ENOB for the three main process corners TT, FF and SS. Figure 3.15 shows the change in the maximum linearity error due to process variations for the proposed circuits and Fig. 3.16 shows the change in the output sensitivity of the proposed circuits. It is obvious that the sensitivity at SS corner increases to 0.405ps/mV for the first proposed VTC and 0.424ps/mV for the second proposed VTC.

Table 3.1. Performance comparison for the two proposed VTCs with other modified VTCs.

	First proposed	**Second proposed**	**[7]**	**[8]**	**[47]**	**[48]**	**[49]**	**[50]**	**[51]**	**[52]**	**[53]**	**[54]**
technology	**65nm**	**65nm**	65nm	65nm	40nm	65nm	65nm	65nm	65nm	65nm	65nm	65nm
supply Voltage (V)	**1.2**	**1.2**	0.6	1.2	0.7	1	1.2	1.0	1.0	1.2	1.05	1.2
dynamic Range (mV)	**800**	**800**	600	--	700	--	1200	200	800	600	360	1420
resolution (bits)	**5**	**5**	9	--	8	--	8	4	8	4	5	14
sampling Frequency (MHz)	**500**	**500**	205	205	0.0028	4000	500	5000	950	1200	5000	250
input Frequency (MHz)	**72.75**	**72.75**	7	2	$30*10^{-6}$	65	250	400	10	602	2500	100
ENOB	**4.1637**	**4.1017**	8.1	10.4	6.4	9.2	-	3.5	7.25	3.1	4.1	12.8
max. DNL (LSB)	**±0.08**	**±0.08**	--	--	-2.3	--	+0.38	+0.34	+0.6	+0.54	--	--
INL (LSB)/max. INL (LSB)	**0.28/-0.44**	**-0.08/+0.52**	--/+1.5	--	--/+2.2	--	--/+0.6	--/+0.38	--/+0.8	--/+0.78	--	--
power (mW)	**0.018**	**0.015**	3.3*	1*	0.0031*	49.7*	0.48	4.1	1.66	0.96	4	0.25
area (mm^2)	**$26.67*10^{-6}$**	**$11.16*10^{-6}$**	0.026*	0.06*	0.003*	0.244*	0.012	0.08	0.007*	0.01*	0.17*	$2*10^{-4}$
FOM1 ($x10^{-12}$)	**17.78**	**21.33**	0.0224	--	$44*10^{-5}$	--	1.5	0.049	0.366	0.45	0.162	2.1
FOM2(Pj/step)	**0.002**	**0.0017**	0.235*	0.1509*	30.9*	0.2148*	-	0.62*	0.016*	0.196*	0.17*	0.00007
simulated/measured	**simulated**	**simulated**	measured	measured	measured	measured	measured	measured	measured	measured	measured	simulated

* These numbers are calculated for the whole ADC.

However, the maximum linearity error at SS corner increases to 1.3% for the first proposed VTC and 0.961% for the second proposed VTC.

Figure 3.17 shows ENOB of the proposed VTC circuits for the process corners. The clock frequency used at process corners is reduced to 400MHz as the output delay at SS corner exceeds 1ns. Moreover, the input signal frequency is chosen to be nearly equal to 61.33MHz to ensure coherent sampling is achieved. Coherent sampling guarantees that FFT results are accurate for proper calculation of ENOB. ENOB decreases to 3.5bits at SS corner for the first proposed VTC and decreases to 3.6bits for the second proposed VTC. As a result, calibration for the proposed circuits is needed to improve the linearity and ENOB for the proposed circuits at SS corner.

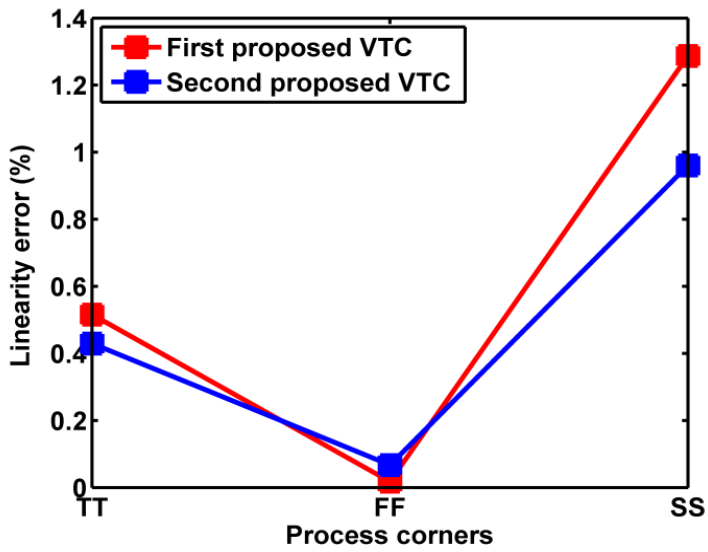


Figure 3.15. Maximum linearity error versus process corners for the proposed VTCs.

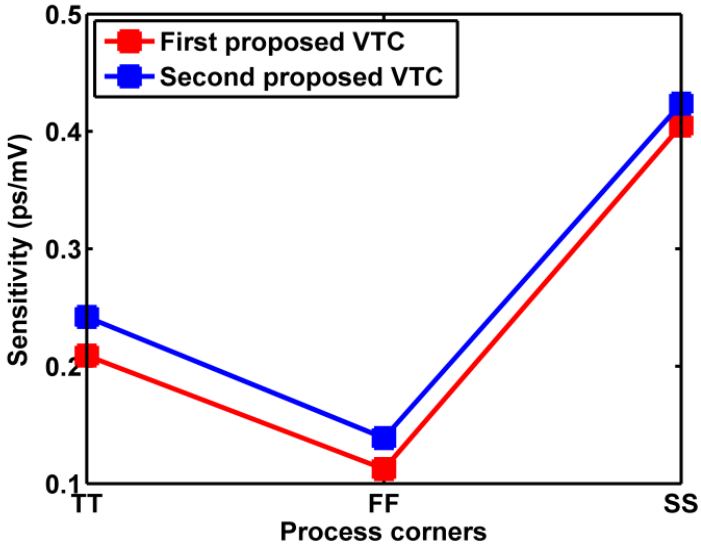


Figure 3.16. Sensitivity versus process corners for the proposed VTCs.

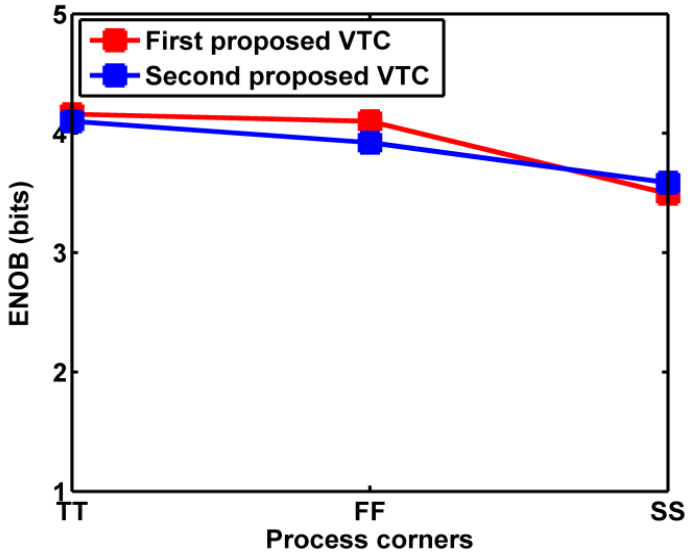


Figure 3.17. ENOB versus process corners for the proposed VTCs.

A calibration circuit for the first proposed VTC is proposed to improve the performance of the VTC at SS corner. The first proposed VTC and the calibration circuit are shown in Fig. 3.18. The calibration circuit consists of a detection circuit and a stack of eight identical NMOS transistors connected between the output node of the VTC and the ground node. The function of the detection circuit is to detect the occurrence of SS corner.

The detection circuit is shown in Fig. 3.19. It consists of two inverters with different load capacitors and a D Flip-Flop (D-FF). The values of the load capacitances are adjusted such that the START signal edge comes before the STOP signal edge only when the circuit operates at SS corner. In this case, the inverted output of the D-FF (Q-bar) will be "1" (D-FF circuit is discussed in details in ch. 4).

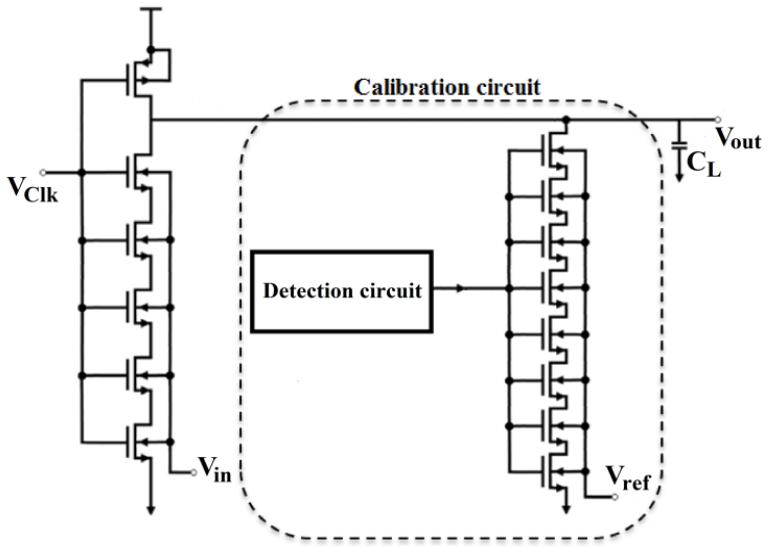


Figure 3.18. The first proposed VTC with the calibration circuit.

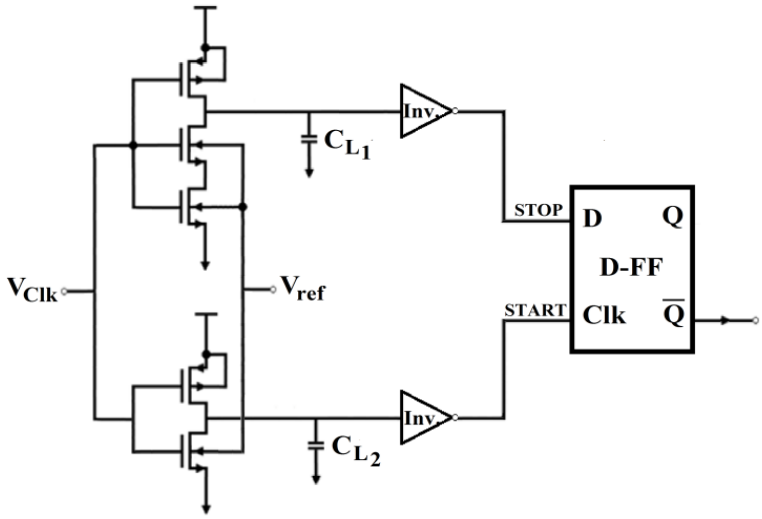


Figure 3.19. The detection circuit for calibration of the first proposed VTC.

The output of the D-FF activates the stack of NMOS transistors which results in increasing the discharging current of the load capacitance at the output node. This leads to a significant decrease in the output delay range at SS corner to be near the range obtained at the nominal corner TT. The value of the reference voltage (V_{ref}) is set to −0.4V, which is the minimum allowed voltage. This allows the stack to drive a small current to keep the output sensitivity at acceptable levels at SS corner.

The detection circuit detects only SS corners and the inverted output of the D-FF keeps its state at ‘0′ for TT and FF corners. Moreover, the values of the load capacitances are adjusted such that the state of the inverted output of the D-FF is ‘0′ even if the circuit is subjected to temperature variations. This can be easily achieved as the additional delay produced from temperature variations is less than that at SS corner.

Figure 3.20 shows the maximum linearity error calculated at process corners before and after calibration for the first proposed VTC. The maximum linearity error at SS corner improved after calibration to be equal to 0.38% for the first proposed VTC. ENOB is also improved to be equal to 4.38 at SS corner after calibration. Figure 3.21 shows ENOB for the first proposed VTC at process corners before and after calibration. Although sensitivity is decreased at SS corner after calibration as shown in Fig. 3.22, it becomes near to that value at nominal process corner. The value of the load capacitance C_{L1} equals to 30fF and the value of the load capacitance C_{L2} equals to 55fF.

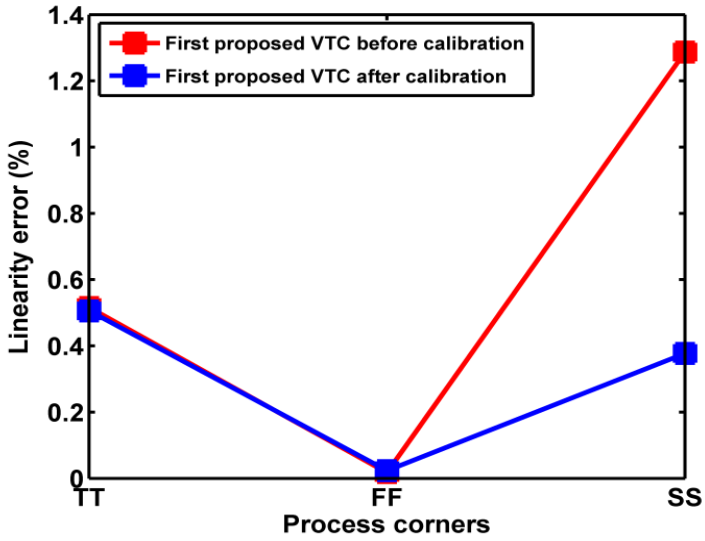


Figure 3.20. Maximum linearity error versus process corners for the first proposed VTC before and after calibration.

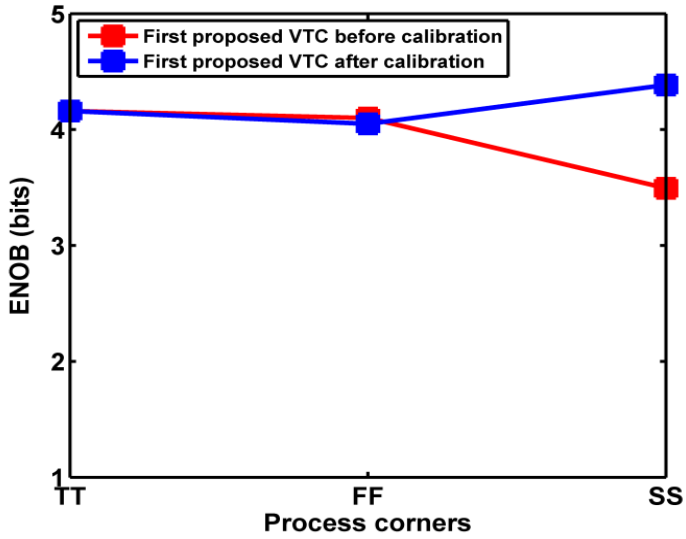


Figure 3.21. ENOB vs. process corners for the first proposed VTC before and after calibration.

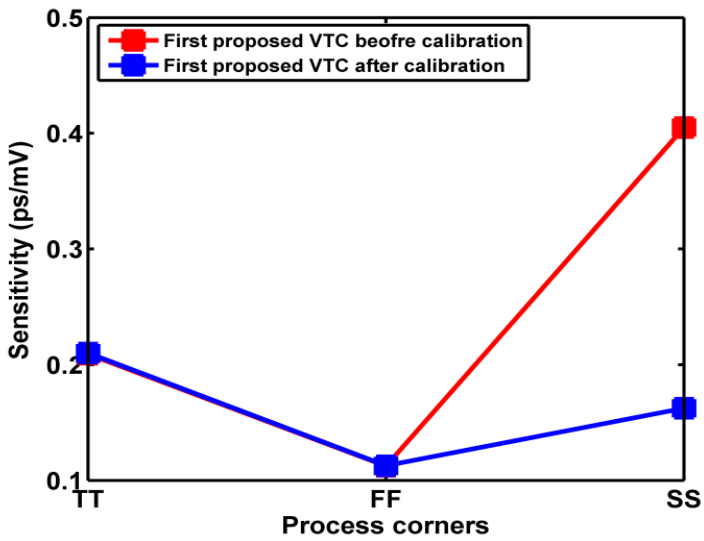


Figure 3.22. Sensitivity versus process corners for the first proposed VTC before and after calibration.

The second proposed VTC circuit is calibrated by the same technique. Figure 3.23 shows the calibrated second proposed VTC circuit. The calibration circuit consists of a detection circuit and a stack of eight identical PMOS transistors connected between the supply voltage and the output node of the VTC.

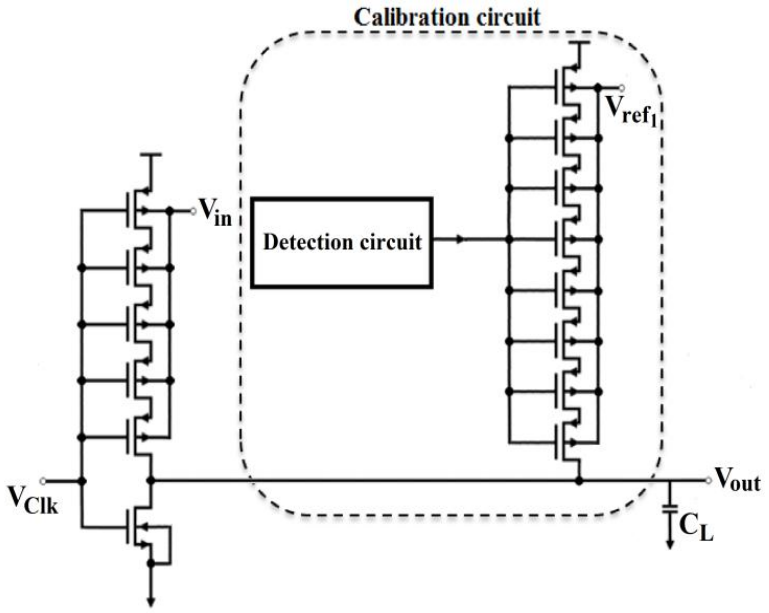


Figure 3.23. The second proposed VTC with the calibration circuit.

Figure 3.24 shows the detection circuit. It has the same theory of operation as in the detection circuit of the first proposed VTC. It detects the occurrence of SS corner at which the output of D-FF will be '0' at this corner only. This activates the stack to increase the charging current of the load capacitance at the output node. Similarly, the value of the reference voltage (V_{ref1}) is set to 1.6V. This allows the stack to drive a small current to keep the output sensitivity at acceptable levels at SS

corner. The value of the load capacitance C_{L1} equals to 60fF and the value of the load capacitance C_{L2} equals to 30fF. The value of the reference voltage (V_{ref2}) is set to 0.8V.

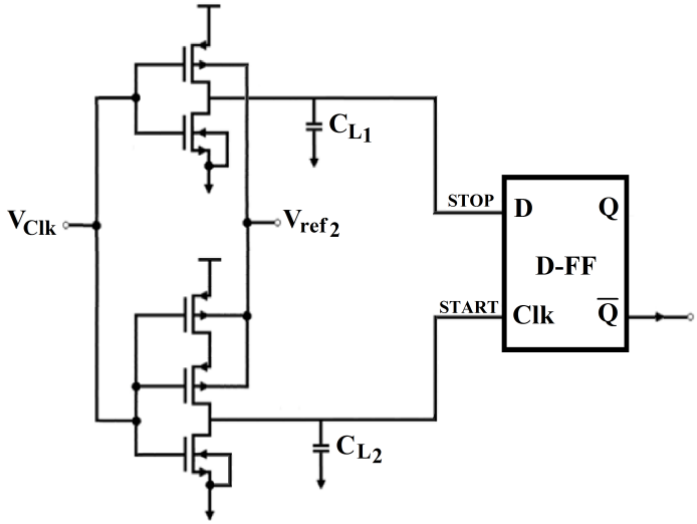


Figure 3.24. The detection circuit for calibration of the second proposed VTC.

Figure 3.25 shows the maximum linearity error for the second proposed VTC before and after calibration at process corners. The maximum linearity error at SS corner improved after calibration to be equal to 0.26%. ENOB is also improved to be equal to 4.35 at SS corner after calibration. Figure 3.26 shows the improvement in the values of ENOB at process corners for the second proposed VTC. The sensitivity of the second proposed VTC after calibration is shown in Fig. 3.27. It becomes near to that value at TT process corner. All the NMOS transistors used in the calibration circuits are identical to each other having the size of (120nm/60nm). In addition, all the PMOS transistors used are identical to each other having the size of (240nm/60nm).

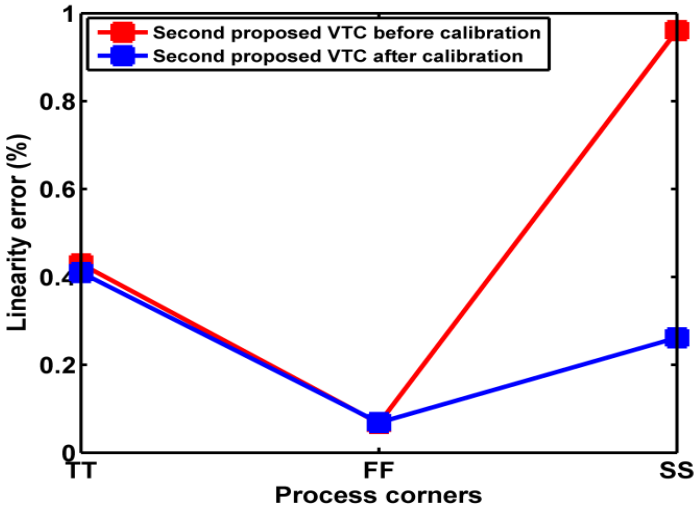


Figure 3.25. Maximum linearity error versus process corners for the second proposed VTC before and after calibration.

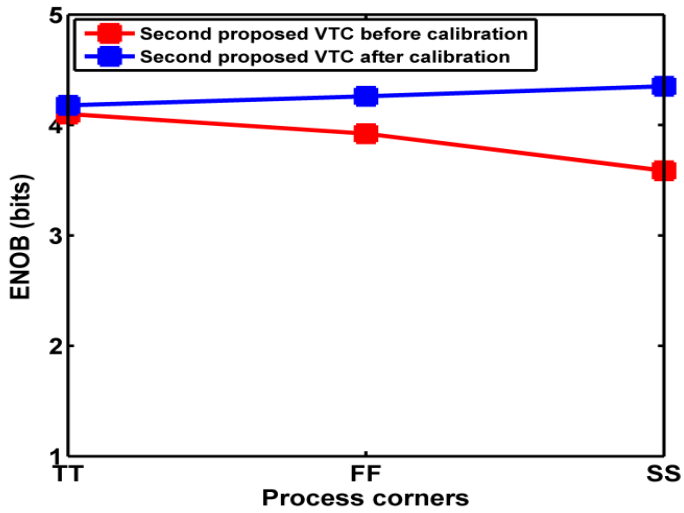


Figure 3.26. ENOB versus process corners for the second proposed VTC before and after calibration.

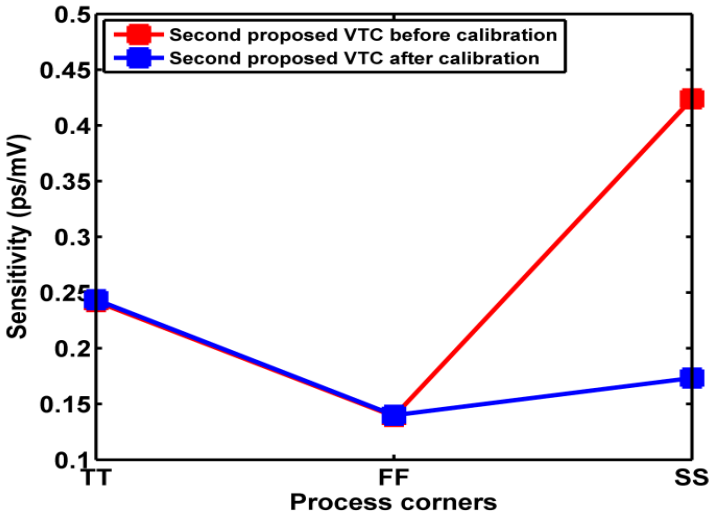


Figure 3.27. Sensitivity versus process corners for the second proposed VTC before and after calibration.

3.4.2 Supply Voltage Variations

The supply voltage is one of the most important factors that affect the performance of the VTC circuit. The VTC output delay is calculated for different supply voltages for the two proposed VTC circuits as shown in Fig. 3.28a and Fig. 3.28b.

As the supply voltage decreases, the output delay range increases which results in increasing the sensitivity of the proposed VTC circuits as shown in Fig. 3.29. However, reducing the supply voltage results in degradation in the SNR that limits the performance of the whole ADC circuit [2].

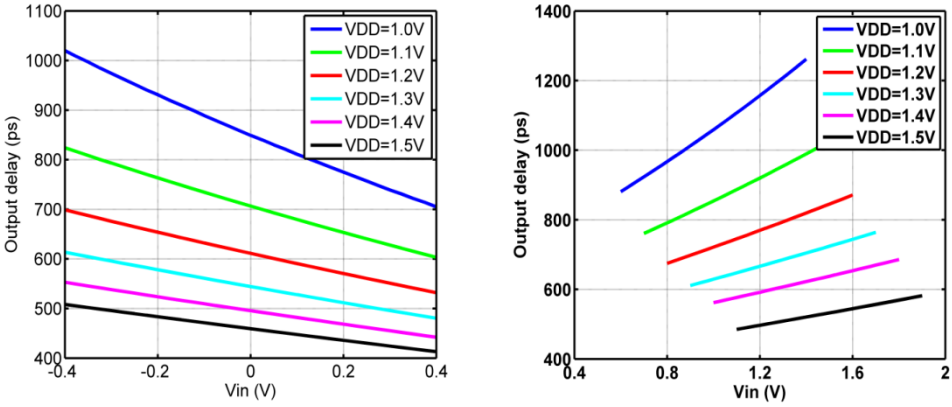


Figure 3.28. (a) Output delay of the first proposed VTC for different supply voltages. (b) Output delay of the second proposed VTC for different supply voltages.

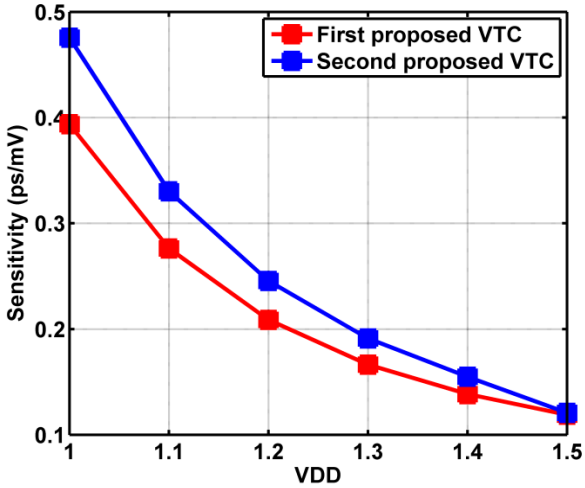


Figure 3.29. Sensitivity versus supply voltage for the two proposed VTC circuits.

3.4.3 Temperature Variations

Temperature variations have a significant effect on the operation speed of integrated circuits. As the temperature increases, the current driven by transistors decreases, causing additional latency to the output of the circuit. The effect of temperature variations on the linearity,

sensitivity and ENOB of the proposed VTC circuits is investigated for a temperature range from −40 to 85°C. Figure 3.30 shows the maximum linearity error versus temperature variations for the two proposed circuits. It is obvious that although the maximum linearity error increases with temperature, it does not exceed 1% for the given temperature range.

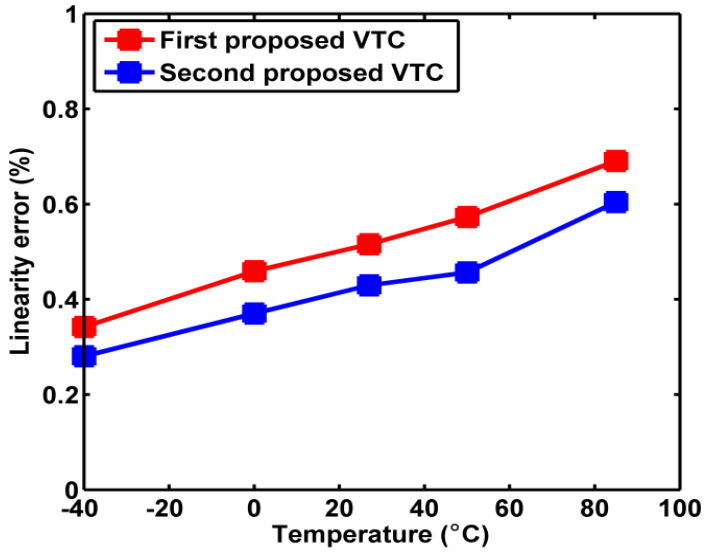


Figure 3.30. Maximum linearity error versus temperature for the proposed VTCs.

The sensitivity of the proposed VTC circuits shows a slight increase by increasing the temperature, as shown in Fig. 3.31. Moreover, ENOB for the proposed VTC circuits keeps its value at an acceptable level for the given temperature range, as shown in Fig. 3.32. The input signal frequency is chosen to be nearly equal to 61.33MHz at a clock frequency of 400MHz. In sum, it is obvious that the two proposed VTC circuits show immunity in terms of linearity, sensitivity and ENOB against temperature variations and do not need calibration.

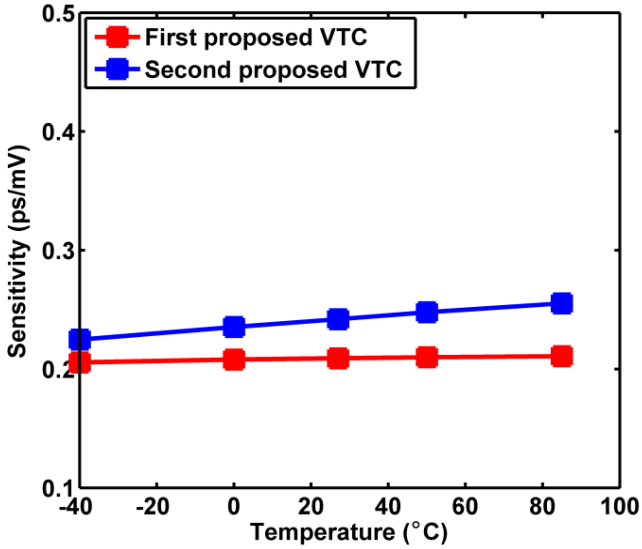


Figure 3.31. Sensitivity versus temperature for the proposed VTCs.

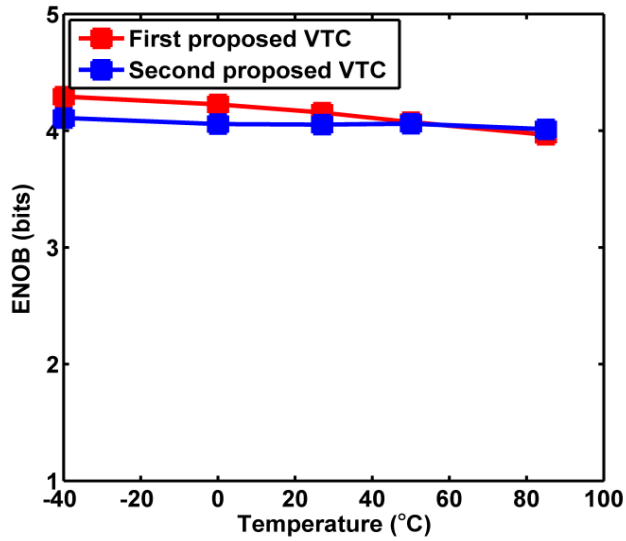
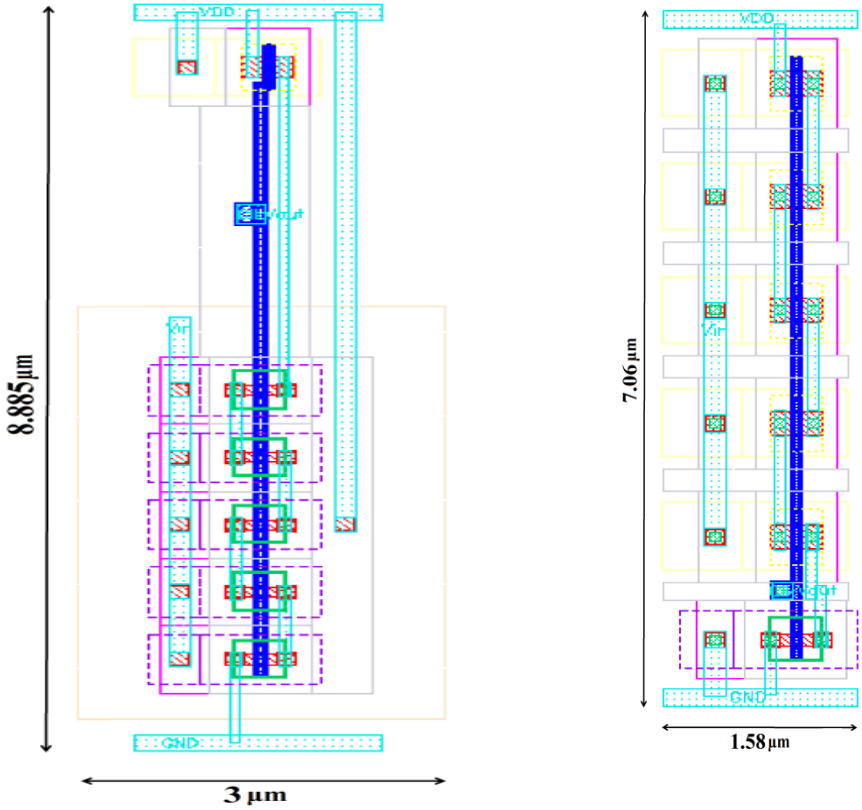


Figure 3.32. ENOB versus temperature for the proposed VTCs.

3.5 Layout Design

The layouts for the proposed VTCs are designed using Cadence Layout tool. Both areas for the proposed VTCs are very small compared to other VTC circuits (as shown in Table 1) thanks to their simple design (one-stage circuit). For the first proposed VTC, triple-well technology is used in order to avoid connecting the Bulk terminal with ground while controlling the voltage of the body terminals of NMOS devices. In other words, a deep N-well layer is used to isolate the p-well from the p-substrate. However, using triple well technology results in a higher layout area. Figure 3.33a shows the layout of the first proposed VTC which occupies a small area of 26.67μm^2. For the second proposed VTC, no triple-well technology is needed for the PMOS body control. Thus, the second proposed VTC occupies smaller area of 11.16μm^2 as shown in Fig. 3.33b.



(**a**) (**b**)

Figure 3.33. (a) Layout of the first proposed VTC circuit; (b) Layout of the second proposed VTC circuit.

Chapter 4

Proposed TDC Circuits

The performance of the VTC is limited by the design of the time-to-digital converter (TDC) circuit that follows it. The TDC affects the linearity of the whole ADC and its performance should be investigated.

In this chapter, two 5-bit standard Vernier delay-line TDCs are used in this work. They are most commonly used as they have the advantage of having very high resolution that can be less than the minimum gate delay in the technology used. The novelty in the design of these TDC circuits is using body biasing technique to control the step delay difference between the delay units of the delay lines in the TDC circuit.

4.1 TDC Circuit Design for The First Proposed VTC

For the first proposed VTC, an interface circuit is proposed after the VTC in order to drive STOP and START signals to the TDC. Figure 4.1 shows the interface circuit that is used for the first proposed VTC. The output of the VTC is inverted to produce the START signal while the STOP signal is a delayed version of the clock signal. The delay unit for the STOP signal is the VTC circuit with a reference voltage equivalent to the maximum delay that can be produced from the VTC ($V_{ref} = -0.4V$).

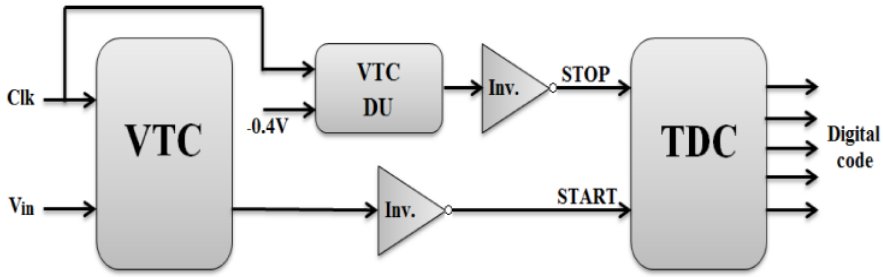


Figure 4.1. Interface circuit for the first proposed VTC.

Figure 4.2 shows a 5-bit Vernier delay-line. The Delay Units (DUs) are CMOS buffers which are controlled by controlling the body-to-source voltage, as shown in Fig. 4.3. Each of the DUs at the STOP line provides lower delay than that at the START line by an amount that is equivalent to one LSB. This delay difference is obtained by applying certain voltages to the bodies of the NMOS devices in the DUs.

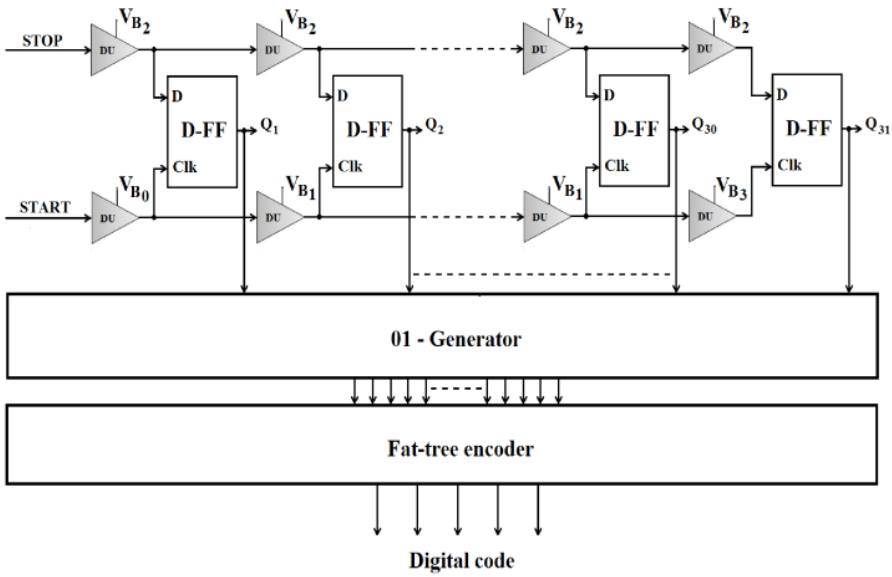


Figure 4.2. Vernier delay-line time-to-digital converter (TDC).

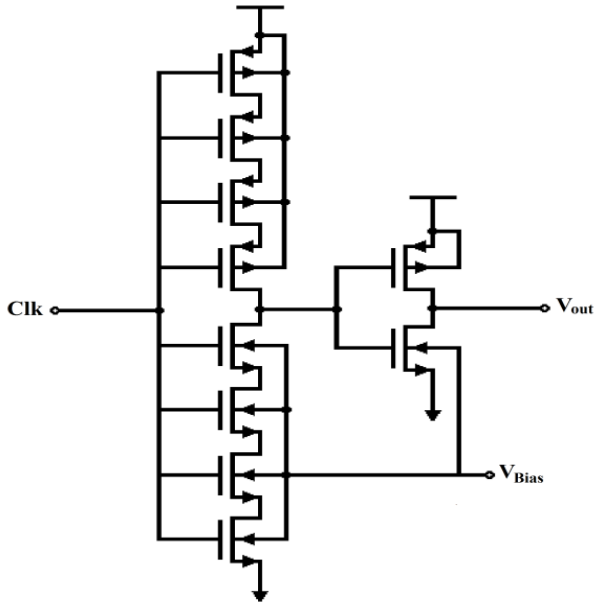


Figure 4.3. Delay unit for the first proposed ADC.

A timing diagram for the START and STOP signals is shown in Fig. 4.4. When the value of the input signal is minimum (-0.4V), the START signal comes with the STOP signal at the same time. Thus, the START signal comes after the STOP signal at all the D-FFs in the TDC and the output of all the flip-flops equals '1'.

On the other hand, when the input signal value is maximum (0.4V), the START signal comes before the STOP signal with a delay difference of (Δ) which is equivalent to the maximum output delay range obtained from the VTC. This makes the START signal to come before the STOP signal at all the D-FFs in the TDC and the output of all the flip-flops equals '0'. By varying the input signal, the output of the flip-flops will also vary. The delay difference in the START signal for the whole input dynamic range equals Δ.

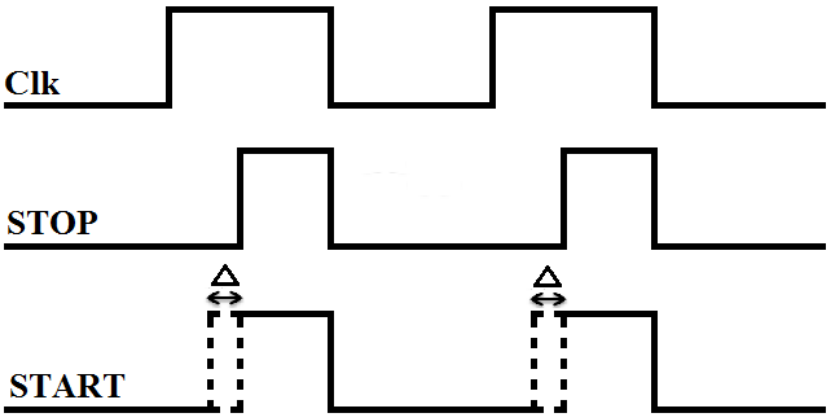
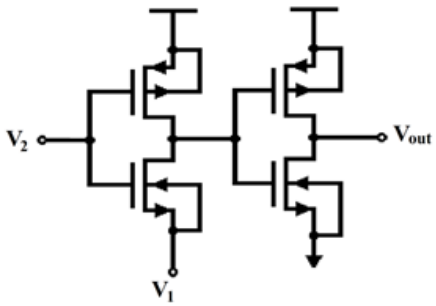


Figure 4.4. Timing diagram for the first proposed TDC.

The output of the flip-flops is an inverted thermometer code. The thermometer code is first converted to a one-hot code using 01-generator circuits [55]. The 01-generator circuit is shown in Fig. 4.5.



V_1	V_2	V_{out}
0	0	0
0	1	1
1	0	0
1	1	0

Figure 4.5. The 01-generator circuit.

Finally, a fat tree encoder [56] is used to convert the one-hot code to a digital code. It is constructed using OR logic gates. The fat tree encoder provides a high speed output. However, it consumes very large chip area. The equations of the output digital bits (D_0, D_1, D_2, D_3 and D_4) are shown below (where (A_0, .., A_{31}) represent the one-hot code):

$$D_4=A_{16}+A_{17}+A_{18}+A_{19}+A_{20}+A_{21}+A_{22}+A_{23}+A_{24}+A_{25}+A_{26}+A_{27}+A_{28}+A_{29}+A_{30}+A_{31} \quad (4.1)$$

$$D_3=A_8+A_9+A_{10}+A_{11}+A_{12}+A_{13}+A_{14}+A_{15}+A_{24}+A_{25}+A_{26}+A_{27}+A_{28}+A_{29}+A_{30}+A_{31} \quad (4.2)$$

$$D_2=A_4+A_5+A_6+A_7+A_{12}+A_{13}+A_{14}+A_{15}+A_{20}+A_{21}+A_{22}+A_{23}+A_{28}+A_{29}+A_{30}+A_{31} \quad (4.3)$$

$$D_1=A_2+A_3+A_6+A_7+A_{10}+A_{11}+A_{14}+A_{15}+A_{18}+A_{19}+A_{22}+A_{23}+A_{26}+A_{27}+A_{30}+A_{31} \quad (4.4)$$

$$D_0=A_1+A_3+A_5+A_7+A_9+A_{11}+A_{13}+A_{15}+A_{17}+A_{19}+A_{21}+A_{23}+A_{25}+A_{27}+A_{29}+A_{31} \quad (4.5)$$

The TDC is manually calibrated by adjusting the biasing voltages for the delay units. The values of the biasing voltages after calibration are V_{B2} = 0.4V, V_{B1} = 0.075V, V_{B0} = 0.39V and V_{B3} = 0.2V.

Differential non-linearity (DNL) and integral non-linearity (INL) are the most important parameters that represent the linearity in the whole ADC. DNL and INL are calculated for the ADC with accuracy of 1mV (800 points are calculated for 800mV input range). This means each digital code has 25 calculated points (LSB = 25mV). Figure 4.6 shows the DNL for the first proposed ADC while Fig.4.7 shows the INL for the first proposed ADC. The maximum DNL equals ±0.08LSB and INL equals 0.28LSB (maximum INL equals −0.44LSB).

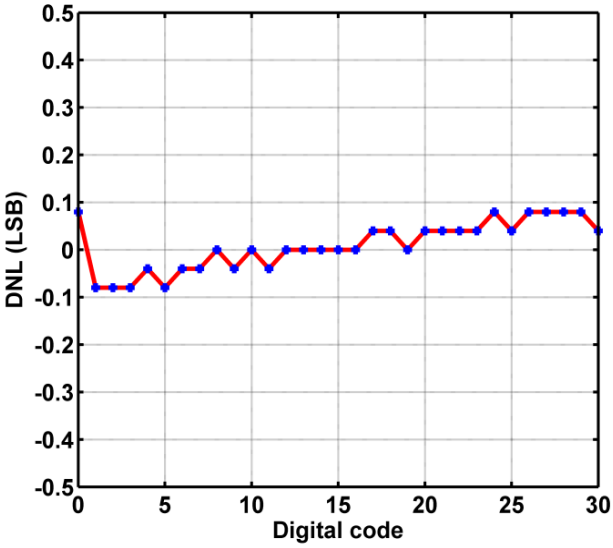


Figure 4.6. Differential non-linearity (DNL) for the first proposed ADC.

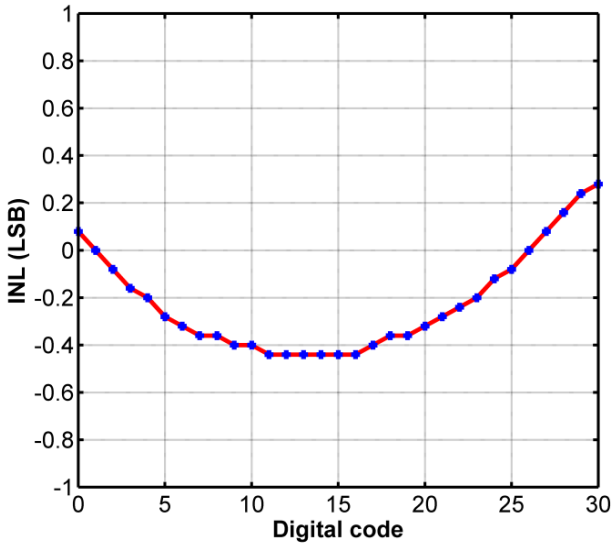


Figure 4.7. Integral non-linearity (INL) for the first proposed ADC.

4.2 TDC Circuit Design for The Second Proposed VTC

For the second proposed VTC, the interface circuit is modified, at which the START and STOP signals are replaced by each other. Moreover, the inverters are replaced by buffers as the output delay of the VTC is a rise time. In addition, the reference voltage used equals 0.8V, which is equivalent to the minimum output delay of the second proposed VTC. The interface circuit for the second proposed VTC is shown in Fig. 4.8.

The same TDC is used for the second proposed VTC and the delay units are controlled by controlling the body-to-source voltage, as shown in Fig. 4.9. The theory of operation is the same as previously discussed for the first proposed circuit. After calibration, the values of the biasing voltages are V_{B2} = 1V, V_{B1} = 1.45V, V_{B0} = 0.95V and V_{B3} = 1.6V.

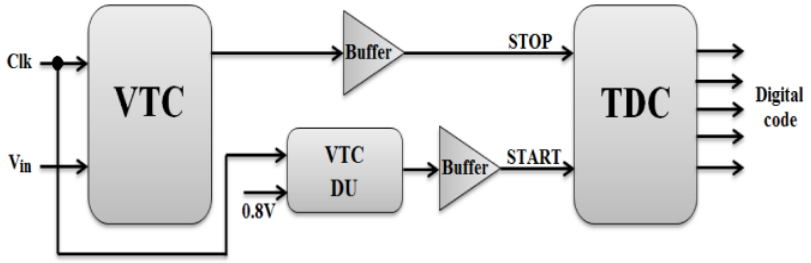


Figure 4.8. Interface circuit for the second proposed VTC.

Figure 4.10 shows the DNL for the second proposed ADC while Fig. 4.11 shows the INL for the second proposed ADC. They are calculated with accuracy of 1mV. The maximum DNL equals ±0.08LSB and INL equals −0.08LSB (maximum INL equals 0.52LSB).

In sum, the two proposed VTC circuits exhibit high performance when implemented with Vernier delay-line TDC to construct the whole ADC circuit. DNL and INL for the proposed designs are compared with other modified designs as previously shown in Table 3.1 in Ch. 3. It is obvious that the proposed designs have better DNL and INL results. All the NMOS transistors used in the interface circuit and the TDC are identical to each other, having the size of (120nm/60nm). In addition, all the PMOS transistors used are identical to each other, having the size of (240nm/60nm).

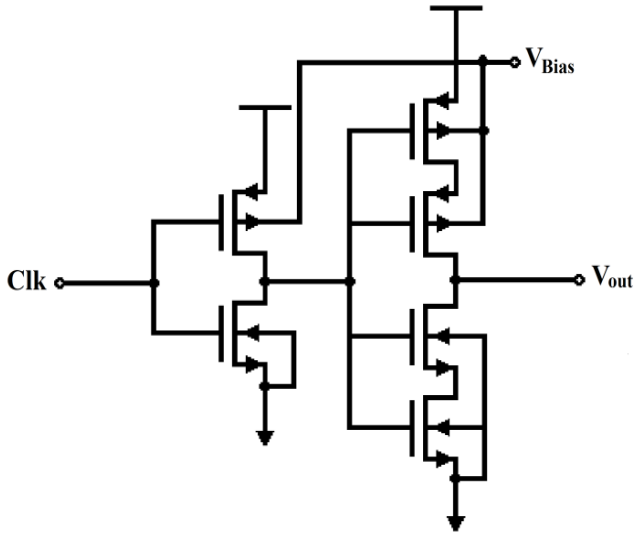


Figure 4.9. Delay unit for the second proposed ADC.

Figure 4.12 shows the layout of the two proposed ADCs. The layout includes the two proposed VTCs, the calibration circuits, the interface circuits and the TDC circuits. The first ADC occupies an area of 0.0092mm2, while the second ADC occupies an area of 0.0067mm2. The first ADC occupies a higher area than the second ADCs due to using triple-well technology (deep N-well layer) for the NMOS body control.

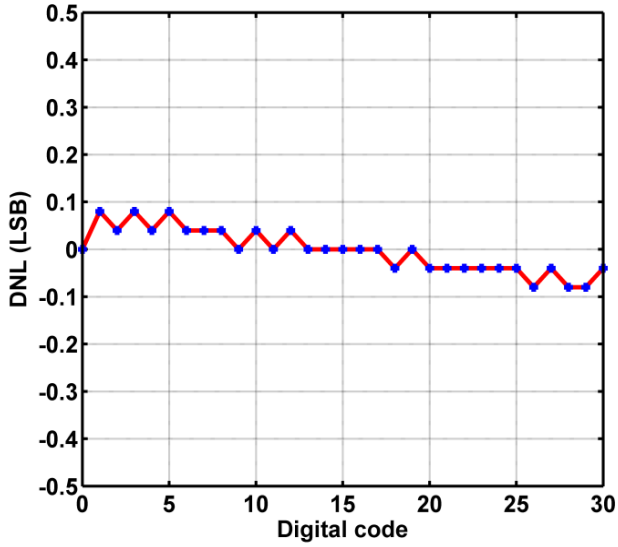


Figure 4.10. Differential non-linearity (DNL) for the second proposed ADC.

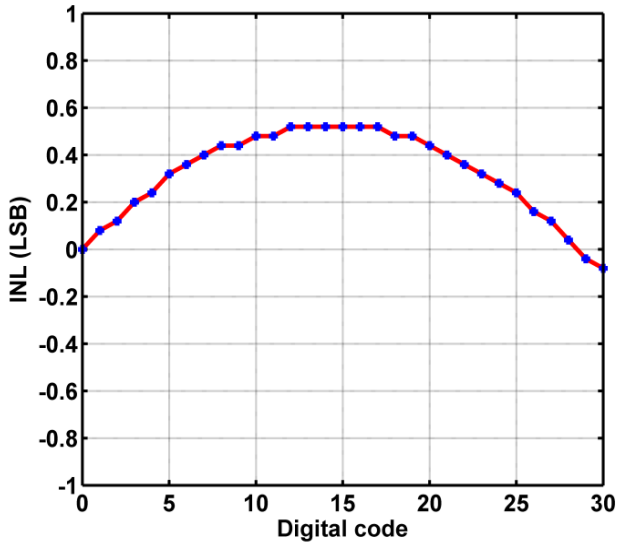


Figure 4.11. Integral non-linearity (INL) for the second proposed ADC.

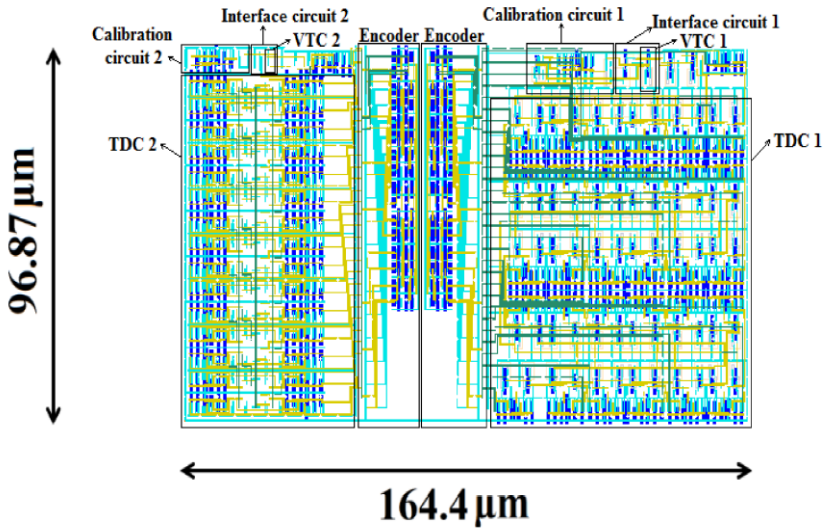


Figure 4.12 Layout of the two proposed ADCs.

Chapter 5

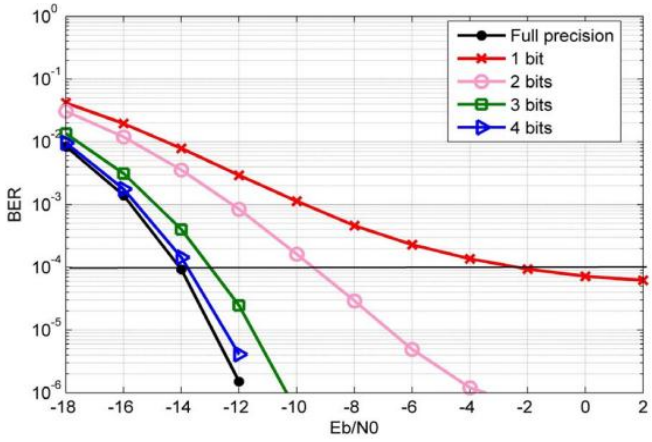
Proposed ADC in MIMO Systems

Massive Multiple-Input Multiple-Output (MIMO) is considered a promising technology for future wireless communications systems and 5G. However, using high resolution ADCs for the antennas at the Base Station (BS) causes high power consumption and high cost. Reducing the resolution of the ADCs at the BS causes severe non-linearity errors in the received signals due to additional quantization noise [57]. Thus, the demand for high linear, low power and low resolution ADCs arises for high performance MIMO systems.

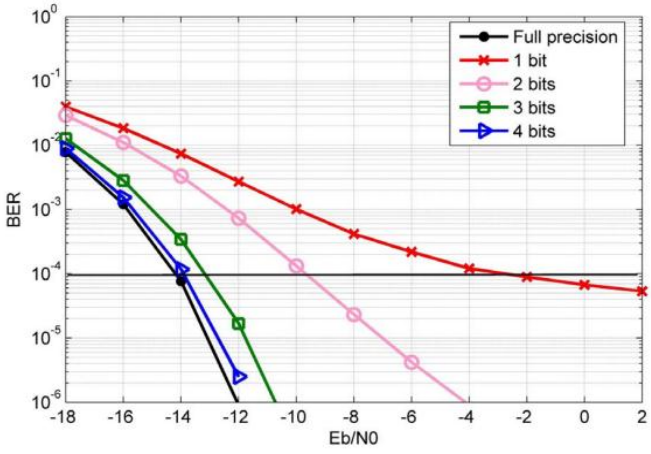
Many studies have been held to compensate between the non-linearity of low resolution ADCs and the high power consumption along with hardware costs of high resolution ADCs. Mixed-ADC architectures are proposed in [58-60] at which some high resolution ADCs are used along with low resolution ADCs. This results in enhanced Bit Error Rate (BER). However, the complexity of the circuits at the receiver increases. Other studies focus on improving channel estimation techniques to overcome the non-linearity that results from using 1-bit ADCs in MIMO systems [61].

Many studies are held to investigate the performance of MIMO systems using low resolution ADCs [62-65]. These studies conclude that low resolution ADCs can bring acceptable performance in terms of BER and system throughput at low power levels.

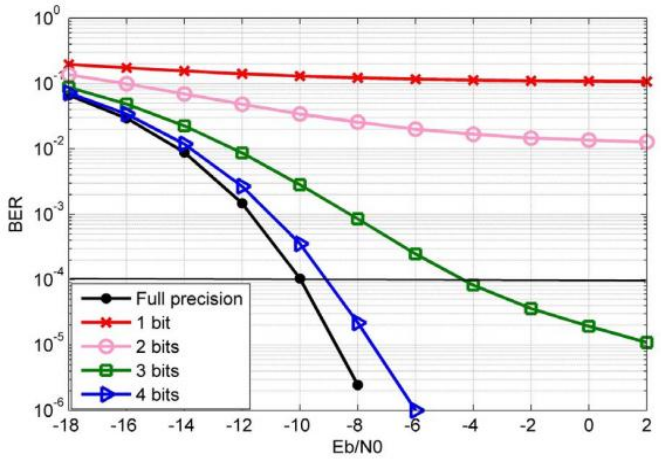
In [64], a study is made on BER performance of uplink massive MIMO with low-resolution ADCs. Figure 5.1 shows the effect of low resolution ADCs on the BER performance of uplink massive MIMO systems versus SNR per bit (E_b/N_0 in dB) [64]. Two transmission modulation schemes of QPSK and 16-QAM are employed by the K-users and the BS uses Zero forcing (ZF) and Minimum Mean Square Error (MMSE) detection techniques. Simulations are performed with 100 antennas at the BS while serving 10 users [64].



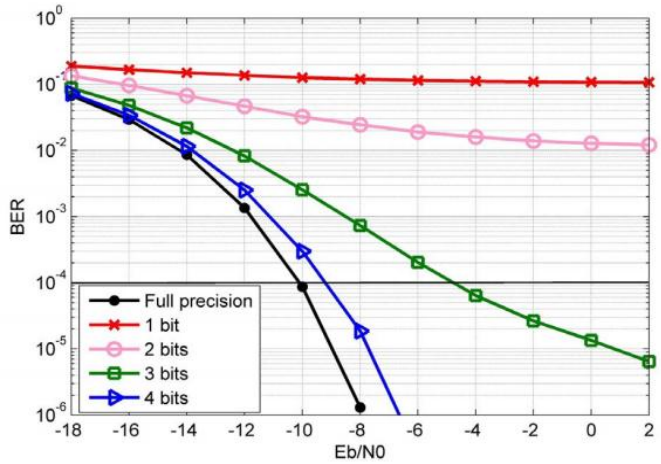
(a)



(b)



(c)



(d)

Figure 5.1. BER versus SNR per bit (E_b/N_0) for M = 100, K = 10 and different ADC resolutions (a) using ZF detector for QPSK; (b) using MMSE detector for QPSK; (c) using ZF detector for 16 QAM; (d) using MMSE detector for 16 QAM [64].

In [65], a study is held for downlink performance in multi-user massive MIMO with low resolution ADCs. Figure 5.2 shows the Mean Square Error (MSE) performance of channel estimation versus SNR [65]. It is obvious that the performance of 4-bit ADC is close to that for full precision ADC. Figure 5.3 shows the system throughputs of the downlink

with the Block Diagonalization (BD) scheme [65] that proves that the 3-bits ADCs can achieve 90% of the throughput realized by infinite resolution at low signal power condition while increasing the ADC resolution beyond 4-bits seems unnecessary [65].

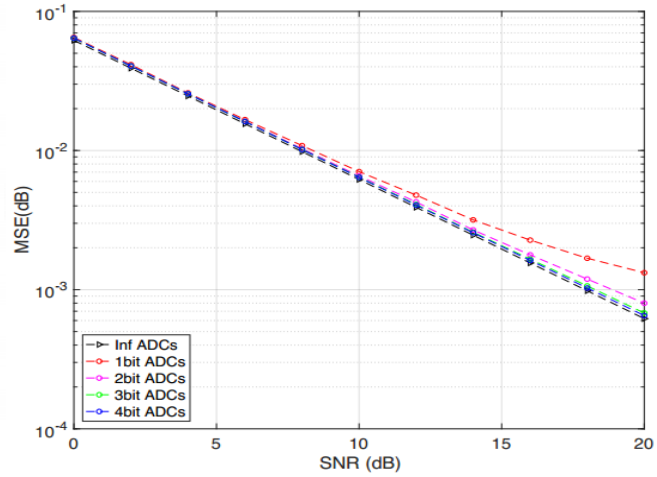


Figure 5.2. MSE performance comparison between infinite and low-resolution ADCs [65].

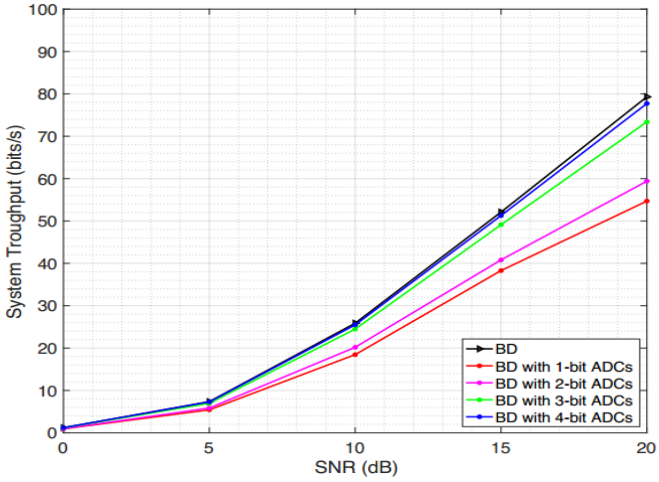


Figure 5.3. Performance of downlink with conventional BD scheme (No. of Antennas =128) [65].

Choosing the appropriate design for the ADC is very crucial in order to obtain high linearity with lower cost in recent technologies. CMOS technology scaling has a significant effect on the design of ADCs. Due to technology scaling, the supply voltage is reduced which causes degradation in the SNR. Moreover, the threshold voltage remains constant by the continuous scaling of CMOS transistors. This results in reducing the dynamic range of the analog input signal.

Due to these limitations, recent research is focused on the design of T-ADC at which the input analog signal is processed in the digital domain to reduce the analog circuitry. Reducing the analog circuitry decreases the circuit complexity by a great amount. Hence, the power consumption and hardware cost are significantly reduced.

In this chapter, a 3-bit VTC is proposed at 4GS/s and maximum input frequency of 2GHz. The theory of operation of this VTC is based on body biasing technique which is described previously in details in Ch. 3. The maximum linearity error is reduced to 0.56% and the input dynamic is increased to 800mV.

5.1 The Proposed Circuit Design and Analysis

5.1.1 Proposed VTC

The theory of operation for the proposed VTC is based on connecting the input signal to the body terminal of the starving transistor instead of its gate terminal as shown in Fig. 5.4. It is previously proven in Ch. 3 that there is a linear relation between the body-to-source voltage (V_{BS}) of the starving transistor and the fall-time delay of the VTC output.

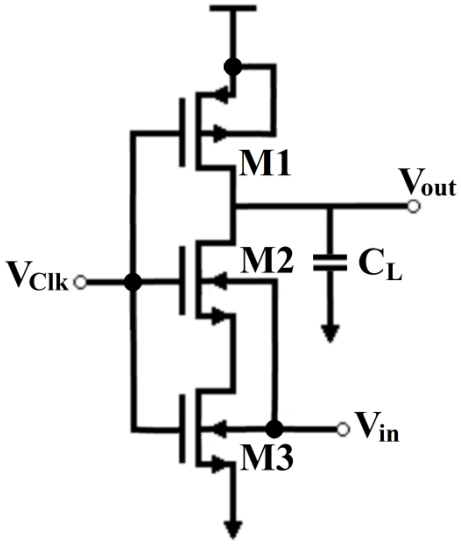


Figure 5.4. The proposed VTC circuit.

The value of the input signal can range from -0.4 to 0.4V resulting in a wide input dynamic range of 800mV. Using values out of this range can cause latch-up. The resolution of the proposed VTC is 3bits. The clock frequency is chosen to be equal to 4GHz which is suitable for ultra-high frequency ranges.

5.1.2 Proposed 3-Bit Vernier Delay-Line TDC

The TDC circuit converts the output delay signal from the VTC to a digital code. The TDC circuitry is more complicated than the VTC and consumes more chip area. There are several architectures for the TDC. The most commonly used is the Vernier delay-line TDC for its high resolution that can be less than the gate delay of the used technology.

A 3-bit Vernier-delay line TDC is introduced in order to calculate the DNL and the INL. These parameters represent a measure for the linearity of the whole ADC.

Figure 5.5 shows the interface circuit that generates the START and STOP from the output delay of the VTC. The START signal is an inverted version from the output delay. The STOP signal is a delayed version of the clock signal at which its delay is the maximum delay that can be produced from the proposed VTC circuit (V_{in}=-0.4V). This delay is generated by another VTC circuit as shown in Fig. 5.5. The interface circuit ensures that the delay between the START and STOP signals is zero when the input signals is at its minimum value (-0.4V).

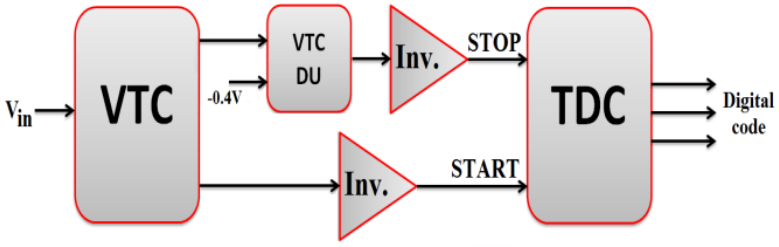


Figure 5.5. The interface circuit.

Figure 5.6 shows a 3-bit Vernier delay-line TDC. It consists of two delay paths for the START and STOP signals, D flip-flops (D-FF), 01 generator circuits and a fat-tree encoder. The DU circuit used in the delay paths is shown in Fig. 5.7. Its output delay is controlled by the value of the bias voltage that is connected to body terminal of the NMOS transistors.

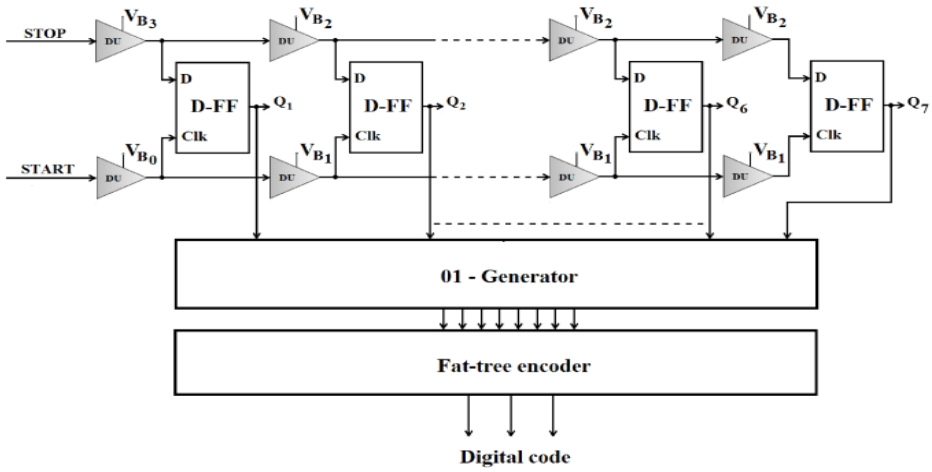


Figure 5.6. 3-bit Vernier delay-line TDC.

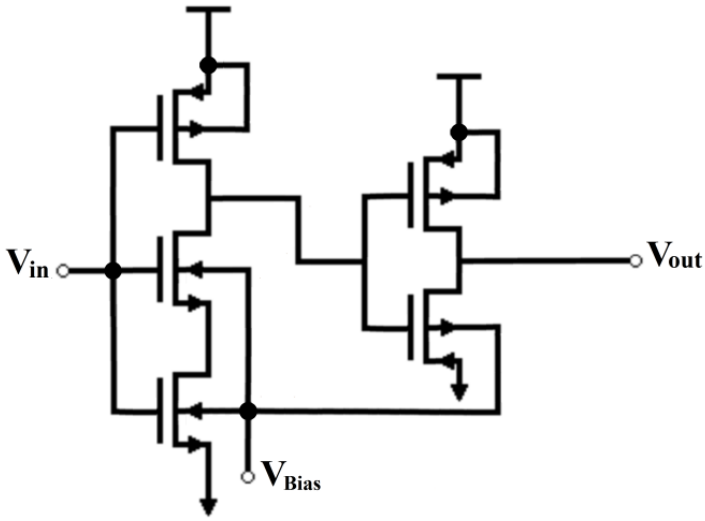


Figure 5.7. The delay unit circuit.

The value biasing voltages is chosen such that the delay of the DU in the START signal path is slightly greater than that in the STOP signal path by 1 LSB (2.87ps). When the input signal is at its minimum value (-0.4V), the START signal comes after the STOP signal at all the flip-flops and their output is '1'. By increasing the value of input signal, the START

signals starts to come before the STOP signal and the first flip-flop produces a ‘0’ output. When the input signal is at its maximum value (0.4V), the output of all flip-flops gives ‘0’.

The output of the seven flip-flops represents an inverted thermometer code. In order to convert this code to a digital code, 01-generator circuits are used to convert this thermometer code into a hot-one code. Then this code is converted to a digital code using a NAND-NOR fat-tree encoder.

5.2 Simulation Results and Discussions

The proposed ADC is simulated using Cadence virtuoso with industrial hardware-calibrated 65nm transistor device models by TSMC. The clock frequency equals to 4GHz and the maximum input frequency is 2GHz. The input dynamic range equals to 800mV for a supply voltage of 1.2V. In the proposed VTC circuit, the size of the PMOS transistor equals to (900nm/60nm). The size of each of the two NMOS transistors equals to (360nm/60nm).

Figure 5.8 shows the output delay of the proposed VTC versus a perfectly linear slope and Fig. 5.9 shows the linearity error percentage versus the input voltage. It is obvious that the maximum linearity error equals to 0.56% for an input dynamic range of 800mV.

ENOB is calculated for the proposed using FFT with 1024 samples to calculate the SQNR. Coherent sampling is achieved for more accurate results [22]. Figure 5.10 shows ENOB for the proposed VTC at different input signal frequencies. The frequency spectrum of the proposed VTC at an input frequency of 1.496GHz is shown in Fig. 5.11.

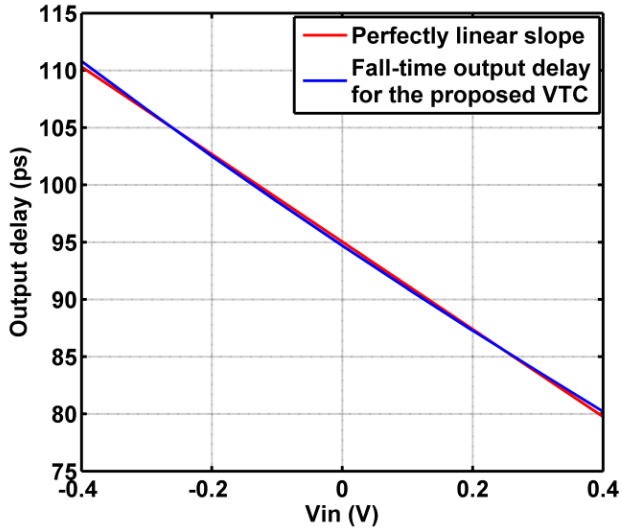


Figure 5.8. Output delay versus perfect linear slope for the proposed VTC.

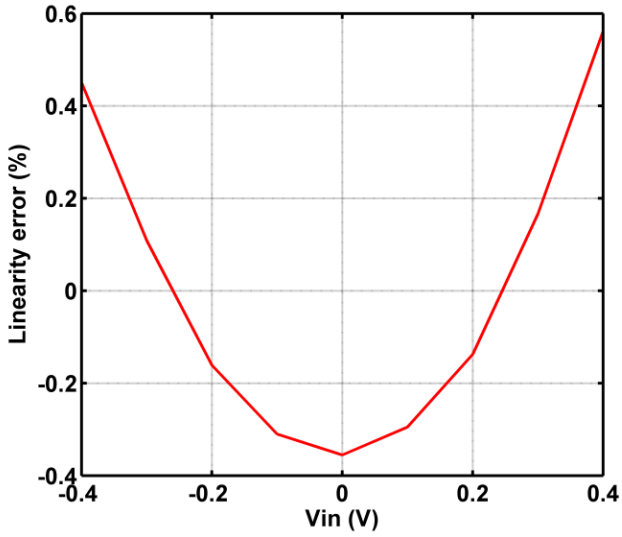


Figure 5.9. Linearity error percentage versus input voltage.

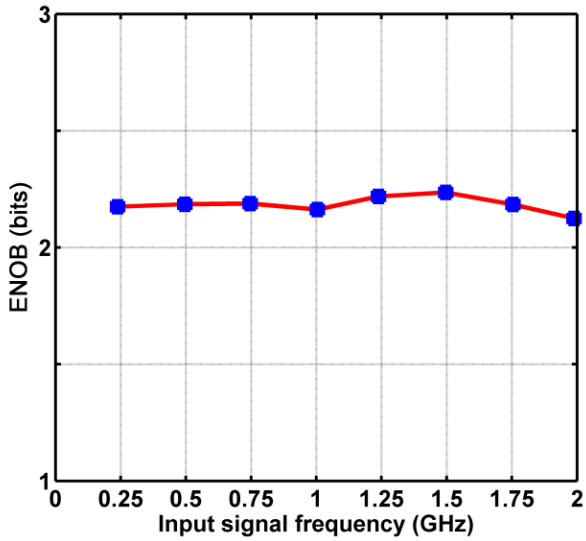


Figure 5.10. ENOB for the proposed VTC versus input signal frequency.

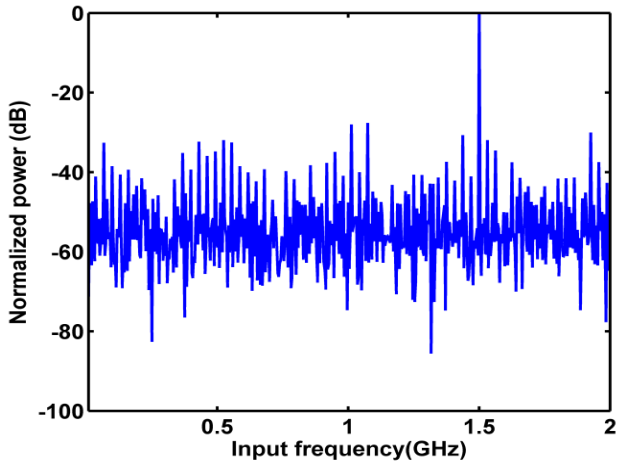


Figure 5.11. The frequency spectrum of the proposed VTC at an input frequency of 1.496GHz.

The power consumption for the proposed VTC at Nyquist frequency equals to 149μW while the overall power consumption of the ADC equals to 2.2mW. Figure Of Merit (FOM) is one of the most important metrics that measures the performance of the ADC. FOM for the proposed VTC

is calculated and compared with other modified VTCs as shown in Table 5.1.

Table 5.1 Performance comparison for the proposed ADC in MIMO systems with other low resolution ADCs.

	Proposed work	**[34]**	**[52]**	**[53]**
Technology	**65nm**	90nm	65nm	65nm
Supply voltage (V)	**1.2**	-	1.2	1.05
Dynamic range (mV)	**800**	140	600	360
Resolution (bits)	**3**	3	4	5
Sampling frequency (GHz)	**4**	2.5	1.2	5
Maximum input frequency (Nyquist) (GHz)	**2**	1.3	0.6	2.5
ENOB at Nyquist frequency (bits)	**2.1247**	2.1	3.1	4.1
Max. DNL (LSB)	**+0.07 LSB**	±0.04	+0.54	-
INL/max. INL (LSB)	**+0.28/+0.28**	-/±0.04	-/+0.78	-
VTC power (at Nyquist)(mW)	**0.148**	6.4	-	4
Max. ADC Power (at Nyquist) (mW)	**2.219**	13	2	21
FOM1 ($x10^{12}$)	**1.15**	0.0038	0.216	0.031
FOM2(Pj/step)	**0.127**	1.1	0.196	0.17

Temperature and process variations are crucial factors that affect the performance of the proposed VTC circuit in terms of linearity error and ENOB. Figure 5.12 shows the effect of temperature variations on the maximum linearity error for a temperature range from -40 to 85°C. It is obvious that the maximum linearity error increases slightly with the increase of temperature but at acceptable limits. The maximum linearity error increases to about 0.67% at 85°C which is still at a low level.

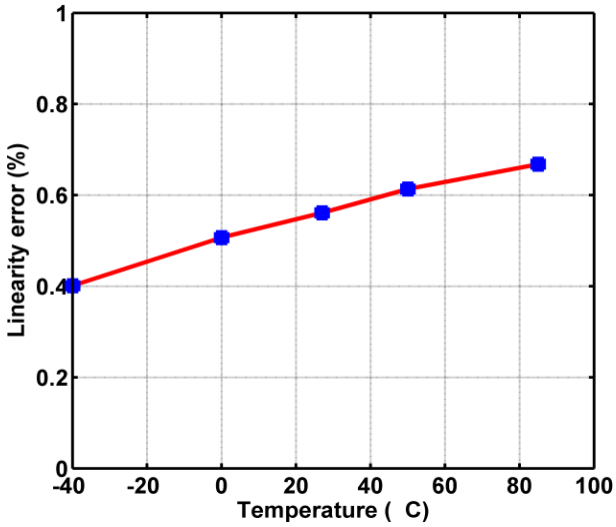


Figure 5.12. Maximum linearity error for the proposed VTC versus temperature.

The effect of temperature variations on ENOB is shown in Fig. 5.13. It is obvious that the change in ENOB in the given temperature range is negligible. ENOB is calculated at an input signal frequency of 1.496GHz and clock frequency of 4GHz. In sum, the proposed VTC circuit shows robustness against temperature variations.

The effect of process variations on the maximum linearity error for the proposed VTC is shown in Fig. 5.14. The clock frequency is reduced to 2.5GHz as the output delay increases at SS corner. The maximum linearity error increases significantly at SS corner and equals to 1.2%. Hence, calibration is required for the proposed VTC to reduce the linearity error at SS corner. In contrast, the proposed VTC circuit shows more robustness against process variations in terms of ENOB. Figure 5.15 shows ENOB for the main process corners at an input frequency of 0.9985GHz. It is obvious that ENOB is nearly constant.

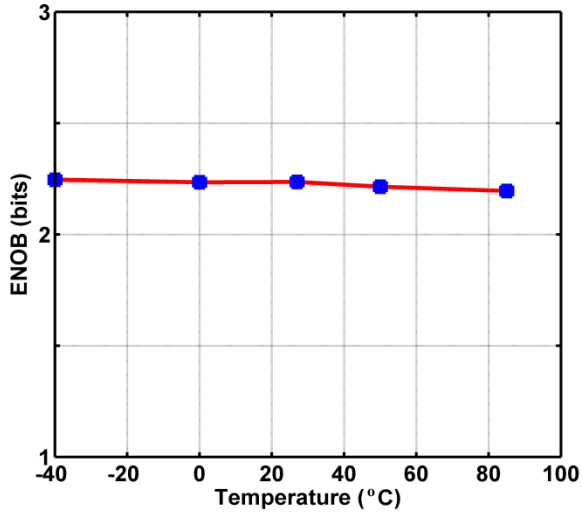


Figure 5.13. ENOB for the proposed VTC versus temperature.

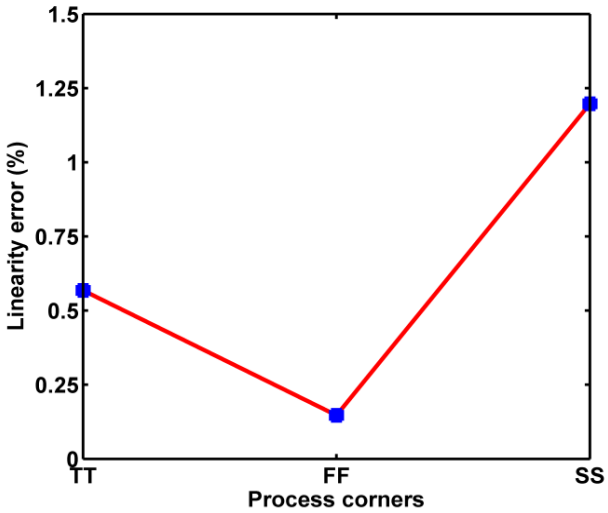


Figure 5.14. Maximum linearity error for the proposed VTC versus process corners.

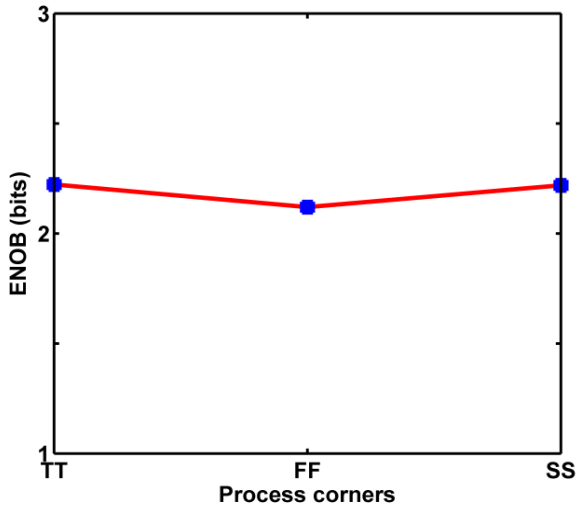


Figure 5.15. ENOB for the proposed VTC versus process corners.

DNL and INL are calculated after manually calibrating the TDC by adjusting the values of the biasing voltages in the delay paths. The values of the biasing voltages after calibration are V_{B2}=0.4V, V_{B1}=0.05V, V_{B0}=0.4V, V_{B3}=0.3V. DNL and INL are calculated using a ramp input signal with resolution of 1mV (800 points for the input dynamic range of 800mV). Each digital code has 100 calculated points as the LSB equals to 2.87ps. Figure 5.16 shows the DNL for the proposed ADC while Fig. 5.17 shows the INL. The maximum value of DNL equals to +0.07LSB while INL has the value of +0.28LSB (which equals to its maximum value as well).

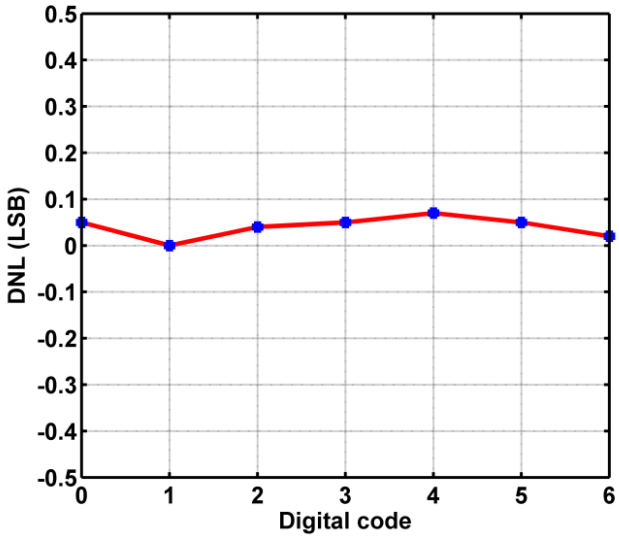


Figure 5.16. DNL for the proposed ADC.

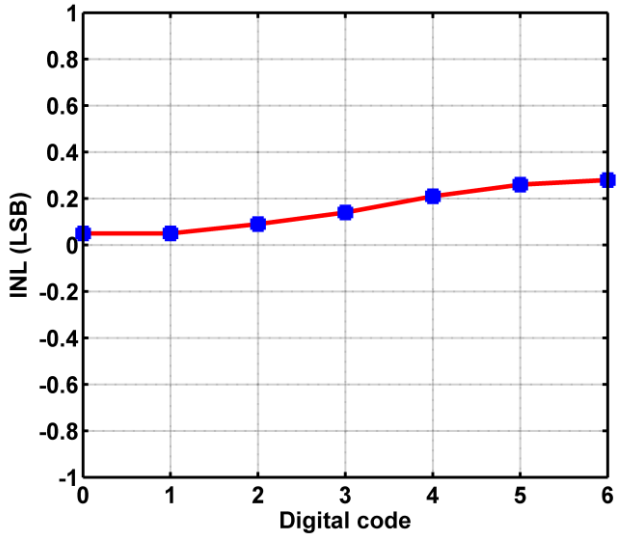


Figure 5.17. INL for the proposed ADC.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this thesis, two proposed VTC circuits were presented achieving better linearity with wide input dynamic range. The input signal was connected to the body terminal of the starving transistor instead of its gate terminal. The maximum linearity error was 0.55% for the first proposed VTC and 0.4% for the second proposed VTC, with an input dynamic range of 800mV for a supply voltage of 1.2V. The proposed VTCs can be used for a 5-bit time-based ADC at a maximum sampling frequency of 500MHz in 65nm CMOS technology.

Thanks to their simple design, the proposed VTC circuits occupy a small area of 26.67μm^2 for the first proposed VTC and 11.16μm^2 for the second proposed VTC, while consuming very small power of 18μW for the first proposed VTC and 15μW for the second proposed VTC.

The effect of PVT variations on the proposed designs was discussed. In addition, calibration circuits were proposed to overcome the limitations in the VTC circuits' performance due to these variations. Moreover, time-to-digital converter (TDC) and the jitter effect were discussed.

The proposed VTCs suffer from low resolution and quite low sampling frequencies. The proposed designs are suitable for applications with limited power budget, such as Internet of Things (IoT) and wearable devices. In addition, the proposed VTC circuits can be applied for low-

resolution ADCs for wireless communication receivers in multiple-input multiple-output (MIMO) systems as the power consumption is a much more important factor than resolution.

Hence, a highly linear VTC circuit was proposed that can be used to increase the linearity of low resolution ADCs in MIMO systems. The proposed VTC exhibits maximum linearity error of 0.56% with a wide input dynamic range of 800mV. The supply voltage used equals to 1.2V in industrial hardware-calibrated TSMC 65nm CMOS technology. The maximum power consumption for the proposed VTC at Nyquist frequency equals to 149μW while the overall power consumption of the ADC equals to 2.2mW. The proposed VTC shows high performance against temperature and process variations. The whole ADC exhibits maximum DNL of +0.07LSB while having INL of +0.28LSB.

6.2 Future Work

Our future work in this research is to fabricate the proposed ADCs and report measurement results. This was postponed due to lack of funding.

Moreover, the future plan of this research is to use the proposed ADCs in other applications that require very low power consumption at quite acceptable resolution such as sensors in biomedical wearable devices and electronic textiles [66] as this technology is emerging and became the trend nowadays.

Publications

[1] A. Elgreatly, A. Dessouki, H. Mostafa, R. Abdalla, and E. El-Rabaie, "A Novel Highly Linear Voltage-To-Time Converter (VTC) Circuit for Time-Based Analog-To-Digital Converters (ADC) Using Body Biasing," *Electronics*, vol. 9, no. 12, pp. 2033, Dec. 2020.

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ملخص الرسالة

يعتبر محول الإشارة التناظرية إلى الرقمية (ADC) هو الرابط بين العالم الحقيقي ، الذي يتمثل في الإشارات التناظرية الواقعية وبين العالم الرقمي ، الذي يتمثل في الدوائر المتكاملة الرقمية والمعالجات الدقيقة والميكروكونترولر. محول الإشارة التناظرية إلى الرقمية يعتبر من المكونات الرئيسية في أحدث الأجهزة الإلكترونية وخاصة في دوائر نظم الراديو المعرفة برمجيا (SDR) ، والأجهزة الطبية الحيوية والأجهزة الإلكترونية منخفضة الطاقة.

تواجه التصميمات الحديثة لمحول الإشارة التناظرية إلى الرقمية (ADC) العديد من القيود الخطيرة بسبب التحجيم المستمر لتقنية "CMOS". أحد أهم هذه القيود هو تدهور نسبة الإشارة إلى الضوضاء (SNR) بسبب انخفاض جهد المصدر. علاوة على ذلك ، يقل النطاق الديناميكي لإشارة الدخل التناظرية نظرا لأن جهد العتبة لا يتأثر بعملية التصغير المستمرة لترانزستورات "CMOS".

أدت هذه القيود إلى تصميم محول الإشارة التناظرية إلى الرقمية المعتمد على الوقت (T-ADC). في هذا النوع من المحولات ، يتم تحويل إشارة جهد الدخل التناظرية إلى إشارة تأخير أولاً حيث يتناسب التأخير مع قيمة إشارة جهد الدخل. بعد ذلك ، يتم تحويل إشارة التأخير هذه إلى رمز رقمي. هذا يسمح بمعالجة الإشارة في المجال الزمني. ومع ذلك ، فإن أداء دائرة تحويل الجهد إلى الوقت (VTC) في " T-ADC " محدود بسبب عدم خطية إشارة التأخيرعند الخرج مع قيمة إشارة جهد الدخل وكذلك بسبب النطاق الديناميكي المحدود لإشارة جهد الدخل.

قدمت الرسالة تصميمين جديدين لدائرة تحويل الجهد إلى الوقت (VTC) المستخدمة في "T-ADC" حيث يتم توصيل إشارة جهد الدخل بطرف جسم الترانزستورمن نوع "starving" بدلاً من طرف البوابة الخاصة به. تظهر هذه التصميمات الجديدة تحسنا ملحوظا في خطية إشارة التأخيرعند الخرج حيث تم تقليل أقصى خطأ في إشارة التأخير ليصل إلى 0.4٪. بالإضافة إلى ذلك ، زاد النطاق الديناميكي لإشارة جهد الدخل ليصل إلى "800" ميللي فولت باستخدام تقنية " TSMC 65nm CMOS" وتردد يبلغ 500 ميجاهرتز.بفضل تصميمها البسيط ، تشغل التصميمات الجديدة المقترحة مساحة صغيرة حيث تبلغ 26.67 ميكرومتر مربع للتصميم الأول و 11.16 ميكرومتر مربع للتصميم الثاني ، بينما تستهلك طاقة صغيرة جدًا تبلغ 18 ميكروواط للتصميم الأول و 15 ميكروواط للتصميم الثاني. قدمت الرسالة أيضا مناقشة لتأثير تغيرات "PVT" على التصميمين الجديدين. بالإضافة إلى ذلك ، تم اقتراح دوائر جديدة للمعايرة للتغلب تأثير هذه التغيرات على أداء التصميمين الجديدين المقترحين.

علاوة على ذلك ، تم اقترح دائرة جديدة لتحويل الوقت إلى رمز رقمي (TDC) نظرًا لأن أداء هذه الدائرة يؤثر على أداء التصميمين الجديدين لدائرة تحويل الجهد إلى الوقت (VTC)التي تسبقها من حيث خطية الدائرة الكلية لمحول الإشارة التناظرية إلى الرقمية المعتمد على الوقت (T-ADC). تم حساب اللاخطية التفاضلية (DNL) و اللاخطية المتكاملة (INL) لأنهما من أهم المعاملات التي تمثل الخطية في الدائرة الكلية لمحول الإشارة التناظرية إلى الرقمية المعتمد على الوقت (T-ADC).

نظرًا لأن التصميمات الجديدة المقترحة مناسبة للتطبيقات التي تتطلب استهلاك محدود للطاقة مثل إنترنت الأشياء (IoT) والأجهزة القابلة للارتداء ، يمكن تطبيق التصميمات الجديدة المقترحة لتصميم دوائر محول الإشارة التناظرية إالى الرقمية منخفضة الدقة لأجهزة استقبال الاتصالات اللاسلكية في أنظمة "مدخلات متعددة مخرجات متعددة" (MIMO) لأن استهلاك الطاقة يعد عاملا أكثر أهمية من الدقة في هذه الأنظمة.

ومن ثم ، تم تطويرالتصميم الأول الجديد لدائرة تحويل الجهد إلى الوقت (VTC) بحيث زاد التردد المستخدم إلى 4 جيجا هرتزولكن على حساب الدقة التي قلت من 5 إلى 3 بت. تقدم الدائرة الجديدة خطية عالية لإشارة التأخيرعند الخرج وتصميمًا بسيطًا واستهلاك طاقة منخفض مما يجعله أفضل حل للمشاكل التي تحد من أداء أنظمة "MIMO". تقدم الدائرة المقترحة أقصى خطأ في إشارة التأخير بحد أقصى يصل إلى 0.56٪. بالإضافة إلى ذلك ، نطاق الديناميكي لإشارة جهد الدخل يصل إلى "800" ميللي فولت باستخدام تقنية "TSMC 65nm CMOS" وتردد يبلغ 4 جيجاهرتز وأقصى تردد لإشارة الدخل يبلغ 2 جيجاهرتز.

وتتكون الرسالة من ستة فصول كالتالي:

الفصل الأول :

تناول مقدمة موجزة عن محول الإشارة التناظرية إلى الرقمية (ADC) ومحول الإشارة التناظرية إلى الرقمية المعتمد على الوقت (T-ADC) وانتهى هذا الفصل بايضاح مشكلة وأهداف الرسالة ومحتويات باقى الفصول.

الفصل الثاني :

شمل بالشرح والتفصيل التصميمات الحديثة لمحول الإشارة التناظرية إالى الرقمية (ADC) وكذلك محول الإشارة التناظرية إلى الرقمية المعتمد على الوقت (T-ADC) مع عرض دراسة مفصلة ومقارنة لأداء هذه التصميمات والتطبيقات الملائمة لكل نوع من هذه المحولات.

الفصل الثالث :

قدم دراسة نظرية وتحليلية للتصميمين الجديدين لدائرة تحويل الجهد إلى الوقت (VTC) المستخدمة في "T-ADC " مع عمل محاكاة كاملة للدوائرالجديدة المقترحة باستخدام برنامج "Cadence Virtuoso" باستخدام تقنية "TSMC 65nm CMOS". كماعرض أيضا مناقشة لتأثير تغيرات "PVT" على التصميمين الجديدين المقترحين.

الفصل الرابع :

قدم دائرة جديدة لتحويل الوقت إلى رمز رقمي (TDC) لكل تصميم من التصميمين الجديدين مع حساب اللاخطية التفاضلية (DNL) و اللاخطية المتكاملة (INL) للدائرة الكلية للمحول.

الفصل الخامس :

وصف كيفية تطويرالتصميم الأول الجديد لدائرة تحويل الجهد إلى الوقت (VTC) لكي يكون مناسبا للاستخدام في أجهزة استقبال الاتصالات اللاسلكية في أنظمة "مدخلات متعددة مخرجات متعددة" (MIMO).

الفصل السادس :

شمل مستخلصات الرسالة مع تقديم للتوصيات المقترحة للأبحاث المستقبلية لهذا الموضوع.

وقد ذيلت الرسالة بقائمة المراجع.