Low Power, Dual Mode Bluetooth 5.1/Bluetooth Low Energy Receiver Design

Ahmed Magdy[1], Sameh Ibrahim[2], A. H. Khalil[1], Hassan Mostafa[3]
[1]Electronics and Electrical Communications Engineering Department, Cairo University, Cairo, Egypt
[2]Electronics and Electrical Communications Engineering Department, Ain Shams University, Cairo, Egypt
[3]University of Science and technology, Nanotechnology Department Zewail, October Gardens, 6th of October, Giza, Egypt

Abstract—**This paper presents a low-power Bluetooth 5.1 (BT5.1) and Bluetooth Low Energy (BLE) compliant receiver (RX). The receiver has two modes of operation: a low-power mode, and a high-performance mode. It utilizes various techniques for low power consumption at both system and circuit levels. For example, it uses a Low-IF mixer-first architecture to optimize power consumption at system level. In addition, it uses harmonic down-conversion in the low-power mode to enable quadrature local oscillation generation. Circuit-level power minimization techniques include using reduced supply voltages, 500 mV for the VCOs and 700 mV for the front end, using passive mixers, and reusing the biasing currents. The proposed receiver utilizes an integrated configurable matching circuit. The proposed receiver is implemented in 65-nm CMOS technology and occupies an active area of 0.55 mm^2 consuming only 697 μW and 1250 μW in low-power mode and high-performance mode, respectively. The low-power RX mode achieves a noise figure of 12.82 dB and an IIP3 of +5.58 dBm. The high-performance RX mode achieves a 6.3-dB noise figure and +2.6-dBm IIP3. The proposed receiver achieves better than 65 dB image rejection.**

Keywords — **Bluetooth, BLE, low-IF, mixer-first, RF front end, dual mode, high performance mode, low power mode, passive mixer, harmonic down-conversion, current reuse, complex pole, Gm-C filter.**

I. Introduction

Bluetooth technology is a short-range, robust, low-power, low-cost, widely used, and flexibly customizable communication system aiming to connect various fixed and portable devices [1]. Since earlier Bluetooth specification releases, it has been adopted in many applications due to its key features. Moreover, Bluetooth Low Energy (BLE) has been introduced for the first time in the fourth release of Bluetooth standard. Bluetooth/BLE operates in the same 2.4-GHz Industrial Scientific Medical (ISM) radio band as *IEEE 802.11b/g/n/ax* (WiFi) and *IEEE 802.15.4* (ZigBee).

As the demand for ultra-low power (ULP) radios; like in wireless Sensor Networks (WSN), wearable devices, medically implanted devices, wireless payment tags, etc; is rapidly increasing, BLE offers one of the best candidates as a wireless communication standard. Furthermore, BLE has been employed in wake-up receivers (WuRX) in prior work achieving less than 250 μW of power consumption [2].

Although Bluetooth has relaxed specifications, ultra-low power receivers, achieving sub-mW, are still a challenging design task. Power-hungry blocks, such as the voltage-controlled oscillator (VCO), usually defines a lower limit for power performance.

Various techniques have been used to realize ultra-low power radios in the literature. An LNA-Mixer-VCO (LMV) cell-based receiver has been introduced in [3], [4] where LNA current is recycled by stacked mixer and VCO. This technique, however, has reduced voltage headroom and lacks block isolation. Correspondingly, the VCO might be pulled by RF blockers and

VCO noise adds up to the RX noise. Ultra-low supply voltage receivers are a popular low power radios approach. A 300-mV RX in [5] extensively applies transformer coupling between RF blocks to maximize headroom and lowers transistor threshold voltage through forward body biasing. This comes at the expense of area and increase of leakage currents. Moreover, a 180-mV RX front end was introduced in [6] where I/Q generation is obtained by a passive RC-CR network in the RF path. According to [7], good matching should be preserved through careful layout. In addition, as the supply voltage is reduced, IIP3 degrades. In addition, an inductive-loaded LNA is divided into two stages, one providing conventional LNA requirements and the second for driving subsequent RC-CR network and passive mixers which imposes extra area.

The proposed BT5.1/BLE receiver operates in two modes: low-power, and high-performance modes. The proposed receiver uses several techniques for low power consumption at both system and circuit levels. For example, the passive mixer first architecture allows LNA to operate at IF, unlike the conventional LNA first architecture where LNAs are at RF and correspondingly, require high power consumption. A configurable complex filter permits both BT5.1 and BLE operation in both receiver modes. A software stack at the top layer drives the PHY layer to select which wireless standard (i.e BT5.1 or BLE) and which operation mode (i.e low-power or high-performance). The proposed receiver utilizes a reduced supply voltage and current reuse to be capable of achieving the required transcondactunce g_m to meet the required building blocks specifications with low power consumption.

This paper is organized as follows. Section II discusses the RX system architecture. Section III discusses the design of the VCO and the RX building blocks. Section IV discusses the simulation results, and finally, the conclusions are drawn in Section V.

II. Receiver Architecture Overview

Fig. 1 shows the proposed receiver architecture. It has a configurable front end matching circuit that interfaces the mixer core to the antenna. This provides impedance transformation for both modes since the input impedance of passive mixers depends on the mode of operation. The low-power mode utilizes down-converting the RF signals by the third harmonic component of the LO. The high-performance mode uses the fundamental component of the LO to down-convert the RF signals. A 4-phases passive mixer is directly following the matching circuit driven by 25% duty cycle non-overlapping clocks.

The differential in-phase and quadrature mixer outputs are t hen applied to a Low-IF LNA. A third-order bandpass complex filter combines the in-phase and quadrature-phase signals to attenuate interferers at adjacent channels and reject the image.

Two controlled VCO cores are used to generate the desired
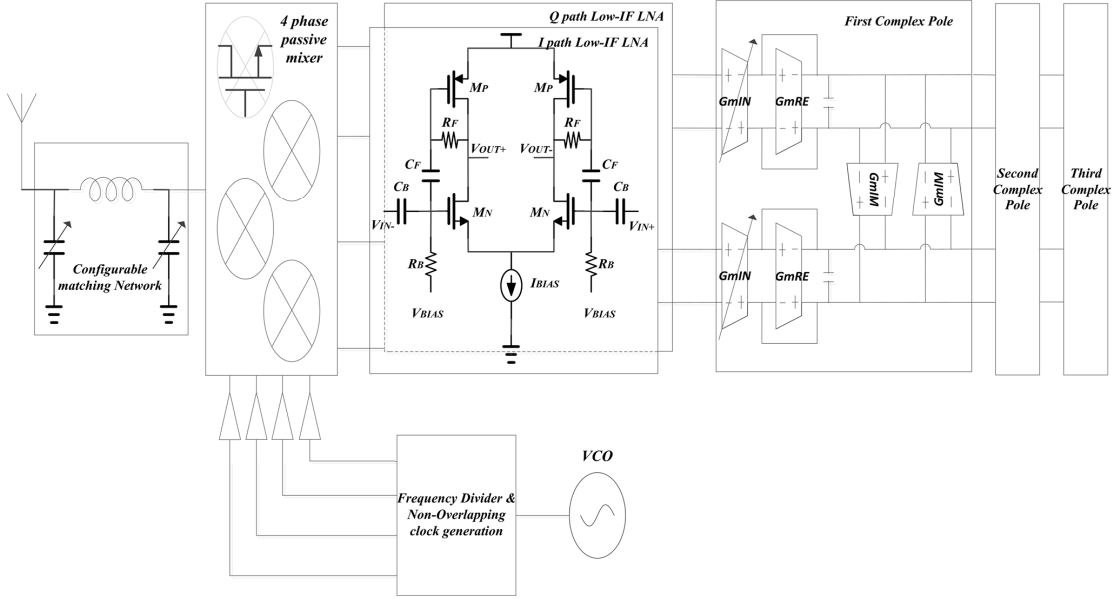
Fig. 1. Proposed receiver architecture

LO signal for each mode of operation separately. One core is operating at almost twice the frequency of the received signal. Then it is followed by a frequency divider by two and non-overlapping clocks generator to provide both the I and Q LO near the received signal frequency, separated by IF of 10 MHz to avoid flicker noise. The wanted RF signal is down-converted normally by fundamental component. The other VCO core on the other hand operates near two-third of the received signal frequency, similarly for the frequency divider to divide the frequency by two. Then the desired RF signal is down-converted by the third harmonic of the LO.

III. CIRCUITS DESIGN

A. Integrated Front End Matching Circuit

A configurable matching circuit is required to adopt the two operation modes since the input impedance seen from the RF port of the passive mixer is highly dependent on the LO frequency [8], and the LO harmonic component of interest. Fig.1 shows a tunable pi matching circuit achieving 6-dB passive voltage gain in the high-performance mode. Therefore, it helps in improving the overall receiver sensitivity.

B. Four-Phases Passive Mixer

The 4-phases single-ended passive mixer with a 20μm/65nm sizing compromise among different tradeoffs in both operation modes such as: the input impedance seen by the matching circuit at the RF input port of the mixer, the noise generation of the mixer, and the input capacitance seen by the frequency divider and buffers at the LO port of the mixer.

C. Low-IF LNA

The fully differential current reuse low-IF LNA is shown in Fig.1. The differential I/Q mixer outputs are ac-coupled to the low-frequency LNA inputs to reduce flicker noise and provide DC biasing. g_{mn} and g_{mp} are designed to be equal. At IF, C_F shorts the inputs to PMOS gates. Thus, the amplifier utilizes both the NMOS and PMOS for amplification with the same bias current, and accordingly reduces the current requirement for meeting specific noise and gain. The supply voltage has been selected to be 0.7V as a compromise between the noise and the low-power/high-performance modes power consumption.

D. Complex Filter

Fig.1 shows a typical single Gm-C complex pole synthesis. A two Gm-C stages with real transfer function are transformed into a complex one by adding an imaginary part. The imaginary part is obtained by cross-connecting $g_{m_{IM}}$ between the I and Q paths [3]. The real component of the pole is synthesized through the $g_{m_{RE}}$ in shunt with the capacitance C.

A current-recycling-based topology has been reported in [9] where all the filter's transconductors share their bias currents with the previous stage, Balun-LNA-Mixer (Blixer). The same topology has been revisited in [10] to enhance a stability issue over a wider design range of $g_{m_{RE}}$ and $g_{m_{IM}}$. It has adopted fully differential architecture. The Fully differential architecture can maintain common-mode gain well lower than the differential-mode gain through suitable Common Mode Rejection Ratio (CMRR).

Fig. 2 shows the current reuse implementation of a single complex pole; inputs and outputs for both I and Q paths are shown combined. The complex filter is tuned to have either 1-MHz bandwidth for BT5.1/BLE, or 2-MHz bandwidth for BLE. Therefore, better adjacent channel rejection is obtained in each standard. This is achieved through added controllable $g_{m_{REC}}$ transconductance in parallel with $g_{m_{RE}}$ and controlled by M_{NC} and M_{PC} control transistors which are connected as an inverter configuration. Therefore, the real part of the complex poles can be controlled by $g_{m_{REC}}$ and accordingly the bandwidth. The inverter's input is a control signal from baseband, V_c.

Now the bandwidth and frequency shift relations are:

$$\omega_{3dB} = \frac{g_{m_{eff}}}{C} = \frac{g_{m_{RE}} + D \cdot g_{m_{REC}} - g_{m_{NEG}}}{C} \quad (1)$$

$$\omega_{shift} = \frac{g_{m_{IM}}}{C} \quad (2)$$

Where D is either one or zero.

If V_c is low, D is zero, the M_{REC} transistor's gate is pulled up to the supply voltage through M_{PC} and turning off this PMOS. Consequently, the effective real transcondactance becomes $g_{m_{eff}} = g_{m_{RE}} - g_{m_{NEG}}$ in the 1-MHz bandwidth mode.
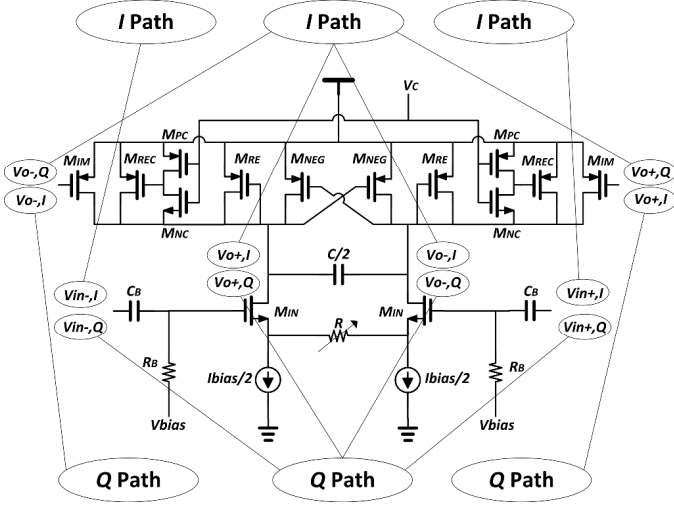
Fig. 2. Current reuse GM-C complex pole

If V_c is high, D is one, the M_{REC} transistor's gate is pulled down to V_{out} through M_{NC} and turning on this PMOS. Consequently, it appears in parallel with M_{RE} and the effective real transcondactance is increased by $g_{m_{REC}}$, $g_{m_{eff}} = g_{m_{RE}} + g_{m_{REC}} - g_{m_{NEG}}$ in the 2-MHz bandwidth mode.

The input transconductances are utilized to realize a variable gain in the filter. They are made degenerated by a variable resistance R in each pole to provide a wide gain tuning range for the overall receiver gain.

E. VCO and Frequency Divider

Since the VCO is not directly driving the mixer, a high swing oscillation is not a design requirement, although it helps in the phase noise minimization. The noise associated with the tail current source has a significant contribution in the phase noise. However, removing the tail current source makes the output common-mode sensitive to the process; voltage; and temperature variations (PVT). Class C VCO, described in [11], has a 3.9-dB phase noise improvement over the standard LC-tank oscillator for the same power consumption.

To minimize the power consumption, the supply voltage is reduced further. However, a lower limit is required for a reasonable swing to avoid operating the cross-coupled transistors in the deep triode region which accordingly reduces the tank quality factor and degrades the phase noise. To design the coupling capacitors C_b equal to the input capacitance seen at the cross-coupled gates, the feedback signal experiences an attenuation by two. Therefore, the lower limit of the supply voltage is derived as follows:

$$V_b <= V_{DD} - \frac{3}{2} V_p + V_{th} \qquad (3)$$
$$V_b >= V_{gs} + V_{DSAT} \qquad (4)$$

Where V_b is the cross-coupled bias voltage and V_p is the oscillation peak voltage.

Combining (3) and (4) and assuming the cross-coupled and the tail transistor to have equal V_{DSAT}, V_{DD} has a lower limit as follows:

$$V_{DD} >= \frac{3}{2} V_p + 2 V_{DSAT} \qquad (5)$$

For $V_p \approx 200$ mV and $V_{DSAT} \approx 100$ mV, $V_{DD} >= 500$ mV

The dual mode operation places a demand for the LO to have a two well far away frequency ranges, 1.6 GHz in the low-power mode and 4.8 GHz in the high-performance mode. For optimum design at each LO frequency, the operation is divided into two completely separate VCO cores at the expense of extra active area. In order to generate 25% duty cycle LO phases, a frequency divider – divide-by-two – circuit and some combinational logic are employed. Fig. 3 shows the clock generation circuit. It is driven by the buffered VCO outputs. The latches used in the divider incorporate additional NMOS source followers, over the conventional rail-to-rail latch circuit as shown in Fig. 4. This is to improve the speed and reduce the power consumption [12] in the high-performance mode where the VCO runs at 4.8 GHz. Whereas, in the low-power mode, the 1.6-GHz buffered VCO outputs drive the conventional divider latches which consume slightly less power than the modified one. The NAND gates and chain of inverters following the latches are designed to drive the 20-μm wide mixer switches and ensure non-overlapping LO waveforms. Thus, it minimizes the RX path noise figure.

IV. SIMULATION RESULTS

The receiver in Fig. 1 is implemented in 65-nm CMOS technology. It occupies 723 μm x 762 μm active area. Fig. 5 portrays the full receiver layout. The receiver operates from a 700-mV supply, for the chain path, and a 500-mV supply, for the LO and frequency dividers.

The choice of a two separate clock generation circuits – one dedicated for each mode of operation – consumes a significant area due to the two large asymmetric spiral inductors of the low-power mode circuit. A larger inductance value is needed for a low-power LC VCO. In addition, a higher quality factor Q_{max} of larger coils occurs at lower frequencies compared to small coils [13].

Fig. 6 plots the post-layout noise figure for the whole receiver chain in the two modes versus baseband frequency. At low frequency, the noise figure is significantly high due to the flicker noise. The average noise figure for the low-power and high-performance modes is about 12.82 dB and 6.3 dB at 10 MHz, respectively.

The post-layout receiver chain transfer function plots are shown in Fig. 7 with a center frequency of 10 MHz and tuned to either 1- MHz, or 2-MHz bandwidth (BW) for BT5.1/BLE or BLE, respectively. The receiver achieves 65-dB image rejection at least and 17-dB attenuation at the second adjacent channel.

Fig. 8 plots the post-layout input matching response, S11, against RF frequency showing better than -11 dB over Bluetooth band in both operation modes.

The front end post-layout Out-Of-Band (OOB) IIP3 in the high-performance and low-power modes are shown in Fig. 9 and Fig. 10, +2.6 dBm and +5.58 dBm, respectively. Increased load capacitance of 10 pF improves the passive mixers filtering property and correspondingly, increasing the OOB IIP3 [14]. In the low-power mode, the front end conversion gain is lower than the high-performance mode conversion gain. Therefore compression effect appears at higher input power levels and the IIP_3 is better.

Fig. 11 shows the post-layout simulated phase noise versus the frequency offset. At 2.5-MHz offset, the phase noise is -122.5 dBc/Hz in the low-power mode, whereas it is -117 dBc/Hz in the high- performance mode. The VCO in the high-performance mode is running at a frequency 3x times the phase noise is expected to be higher given that: 1) Q of the inductors
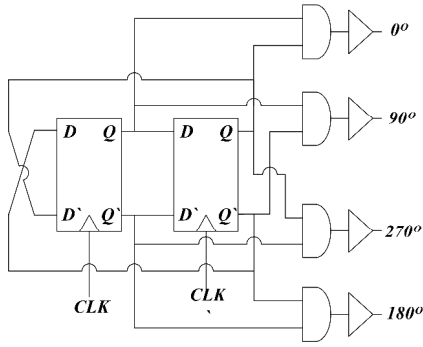
Fig. 3. 25% non-overlapping clock generation
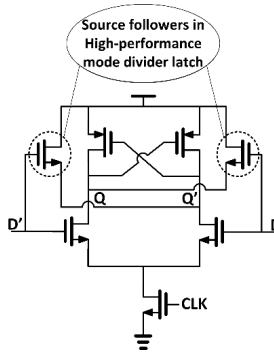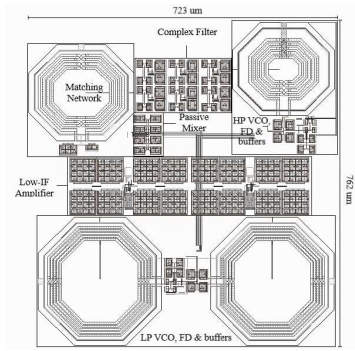

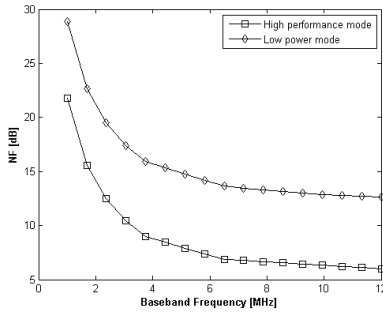Fig. 4. Divider latch

Fig. 5. Receiver Layout

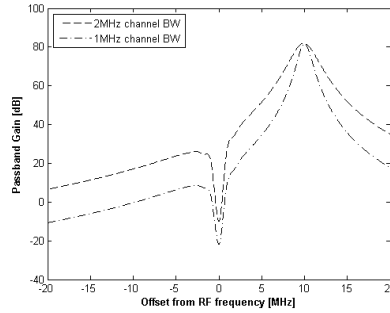Fig. 6. Receiver noise figure in two modes

Fig. 7. Receiver transfer function in two modes
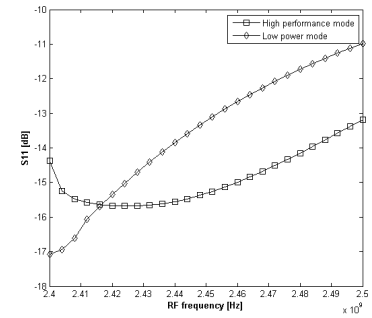

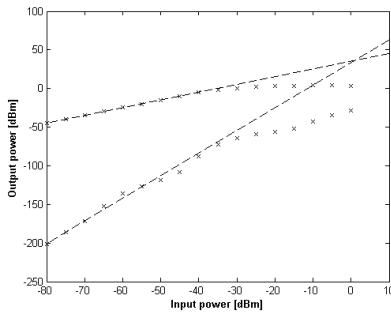Fig. 8. S11 in two modes

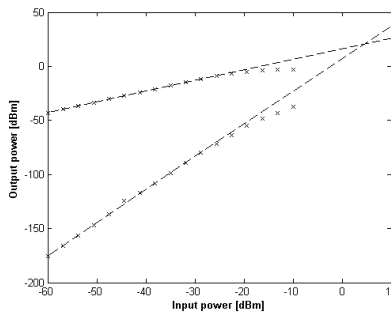

Fig. 9. Front end OOB IIP3 in high-performance mode
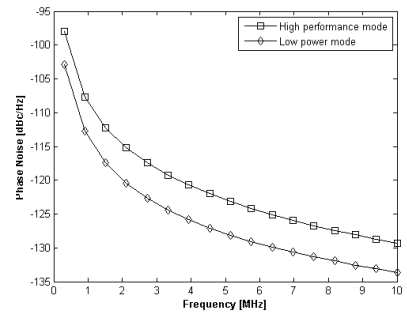

Fig. 10. Front end OOB IIP3 in low-power mode

Fig. 11. VCO phase noise in two modes

in the two modes are within the same range ~ 11.5, 2) the output swing is the same of 400 mV, and 3) the current consumption in the high-performance mode VCO is about 2.5x of the low-power mode VCO.

Table I summarizes the post-layout simulation results for both the receiver operation modes compared to the state of the art. Thanks to various techniques adopted both on the system level and circuit level, the proposed receiver achieves improved performance metrics at low power dissipation in both modes of operations.

V. CONCLUSION

A low power, low supply voltage, dual operation mode receiver has been presented. The receiver achieves good performance while consuming only 697 µW/1250 µW through optimizations both at system level and circuit level designs and compromise between its two modes. The proposed receiver is the first one to utilize one receiver chain design realizing two modes of operation through fundamental and harmonic down-conversion passive mixer first architecture. The receiver exports control signals to the baseband world for simple mode of operation control and bandwidth adjustment. Each mode is compliant to both BT5.1 and BLE noise figure, linearity, IRR, and phase noise specifications.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

	This Work[1]		[4]	[15]		[16][1]
Supply Voltage (V)	Dual supply 0.7V – 0.5V		0.8	0.8		0.8
Power (µW)	697	1250	600	2300	2900	550[2]
NF (dB)	12.82	6.3	15.1/15.8	5.9		14
OOB IIP3(dBm)	+5.58	+2.6	-15.8/-16.8	-17		-16
Voltage Gain (min/max)(dB)	48/81	55/88	55.5/56.1	-		42
IRR (min/max) (dB)	65/81		30.5/37.3	No Image		No Image
VCO PN (dBc/Hz)	-122.5 @ 2.5MHz	-117 @ 2.5 MHz	-109 @ 2.5 MHz	-		-112 @ 1MHz
Data Rate (Mbps)	1 or 2		1	1	2	1
FOM[3]	181.75	184.06	178.02/177.32	181.4	180.4	181.6
Technology(nm)	65		130	40		180
Area (mm^2)	0.551		0.25	0.8		1

[1]Post-layout simulated results   [2]Excluding the filters

[3]FOM $= -P_{sensitivity} - 10\log\frac{P_{DC}}{Data\,Rate}$

VI. ACKNOWLEDGMENT

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