A 10 Gb/s SerDes Transceiver

Abdelrahman M. Sawaby[1], Abdelrahman M. Elshorbge[1], Omar T. Abdelhalim[1], Mahmoud A. Farghaly[1], Mahmoud Sherif Taha[1], Yehia Hamdy Yehia[2], Salma El-Sawy[2], Mohamed Samir Fouad[2], and Hassan Mostafa[1,3].
[1]Electronics and Electrical Communications Engineering Department, Cairo University, Giza, Egypt.
[2]ICpedia, Cairo, Egypt.
[3]University of Science and technology, Nanotechnology and Nanoelectronics Program, Zewail City of Science and Technology, October Gardens, 6th of October, Giza , Egypt.
Emails : amsawaby@gmail.com, elshorbgeabdelrahman@gmail.com, omarazklany97@gmail.com, ma7moudfarghly1998@gmail.com, mahmoudsherif2305@gmail.com, yehia.hamdy@ic-pedia.com, salma.elsawy@ic-pedia.com, mohamed.fouad@ic-pedia.com, hmostafa@uwaterloo.ca

***Abstract*—This paper presents a Serial Data Link Transceiver, which supports data rate transfer up to 10 Gbit/s designed with 65-nm CMOS technology. The Transmitter is modeled with Verilog-A with 3-taps Finite Impulse Response Filter (FIR) and Current Mode Logic (CML) drivers. The Receiver is DC-coupled and driven by Power Management Units (PMU), Band Gab Reference (BGR) and Low Drop Out regulator (LDO). The equalization in the receiver is achieved using Continuous Time Linear Equalizer (CTLE) with channel loss compensation up to 7.5 dB, Variable Gain Amplifier (VGA) and programmable 3-taps Decision Feedback Equalizer (DFE). The sampling clock is acquired using Clock and Data Recovery block (CDR). Both the transmitter and the receiver use supply voltage of 1.2V generated from voltage supply of 1.8V using PMU. The receiver average power consumption is 9.57 mW at 10 Gbit/s rate.The Transceiver's equalization is tested over 30-inches of FR4 channel and achieved compensation up to 27 dB loss at the Nyquist frequency (5 GHz).**

***Index Terms*—Clock and Data Recovery, Continuous Time Linear Equalizer, Decision Feedback Equalizer, Finite Impulse Response Filter, SerDes Transceiver, Variable Gain Amplifier .**

I. Introduction

The growth development of modern communication technologies such as cloud computing and social networking has led to an ultra-high bandwidth demand on data communication. According to Cisco forecast, the global average IP traffic will reach 1 Pbps by 2022, and busy hour traffic will reach 7.2 Pbps [1]. In order to support the dramatic growth in global IP traffic, a high-speed links are used. Among the variety of high-speed links, Serializer/Deserializer (SerDes) transceivers play an important role. In addition to bandwidth requirement, the power efficiency and area need to be taken into account in the design process.

In this work, a 10 Gb/s SerDes transceiver is modeled using Verilog-A and the receiver (RX) is designed with 65-nm CMOS technology including the power management unit, clock data recovery and termination calibration. The receiver consumes around 9.58 mW with termination calibration included. All blocks are designed to be configurable to compensate the attenuation of different wireline channels and support different communication standards. The main consideration for all clocks is to achieve bandwidth requirement (5 GHz in case of 10 Gb/s data rate) and minimize the power consumption. The rest of this paper is organized as follows.In Section II, the transceiver blocks details are described. In Section III, the simulation results and comparison to prior art are presented .In Section IV, the conclusion are presented.

II. Design and Implementation

This section presents an architectural overview of the transceiver and the circuit implementation of TX and RX Blocks. The transceiver block diagram is shown in Fig. 1.

A. Transmitter

The TX used in this work is modeled using a Verilog-A. The TX is composed of 3 stages as shown in Fig. 1. A 8:1 MUX It converts the data from serial data (8 lines, each line with rate of 1.25 Gb/s) to parallel data with rate of 10 Gb/s. The FIR model is composed of 3 taps for equalization (1 main-cursor, 2 post-cursors). Taps coefficient value is determined and calculated depending on the response of 30 inch FR4 channel using zero forcing algorithm [2]. The model of the FIR filter, shown in Fig. 2, is implemented with (GM cell and Flip-Flops). The driver Gm cell model is based on the CML driver. It works with digital input data of two levels (0 and 1) and it steers a current in the termination resistance with the specific value determined based on the output swing desired and multiplied by the taps coefficients. The delay unit (D flip flop) is supposed to give a delay time equal to the Unit Interval (UI).

B. Receiver

The receiver is composed of Termination Calibration Circuit, Power Management unit (BGR, LDO), CTLE , VGA, DFE and CDR. The transceiver is based on DC coupling signal and DC common mode around 0.8 V.

1) Termination Calibration Circuit:

This circuit is used to calibrate on-chip slices to external off-chip 50 Ω resistance for channel termination to improve matching to have no reflection on the channel. As shown in Fig. 3, the chosen design of this circuit is as in [3]. An off-chip resistance (50 Ω) with high precision is used as a reference. To

978-1-6654-2157-7/21/$31.00 ©2021 IEEE

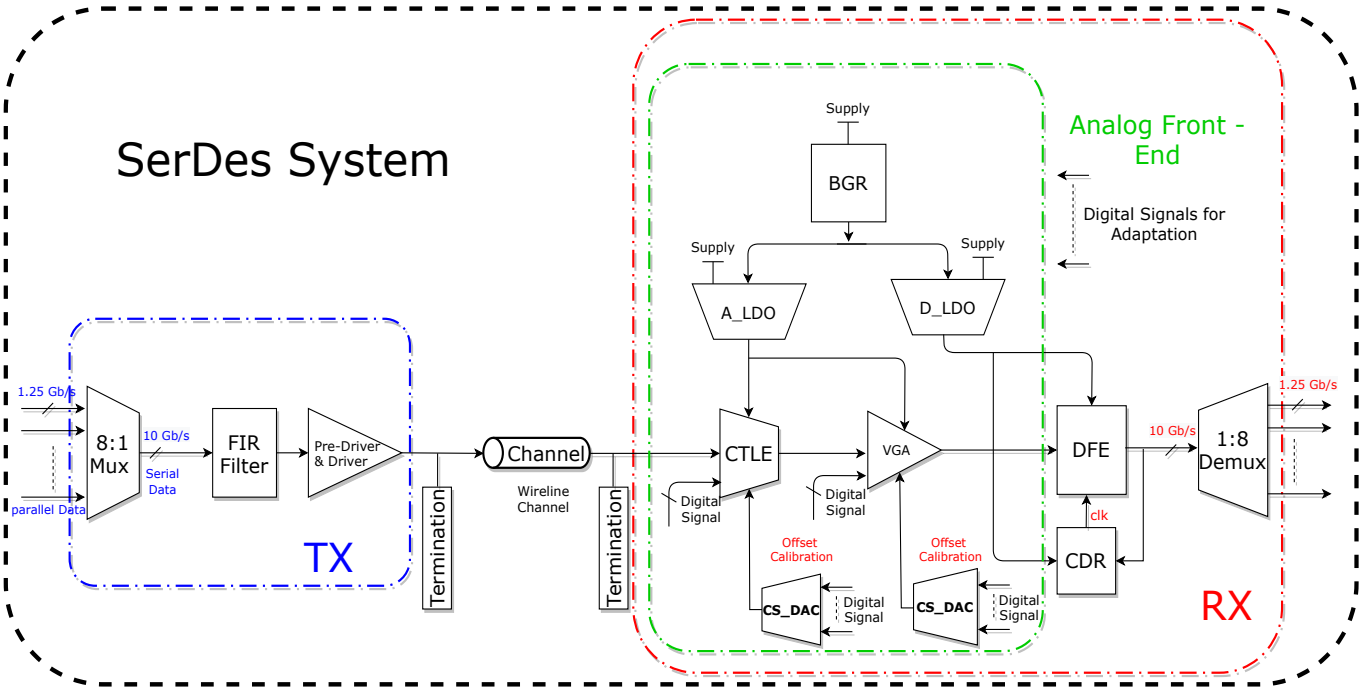

Fig. 1. SerDes transceiver high-level block diagram.

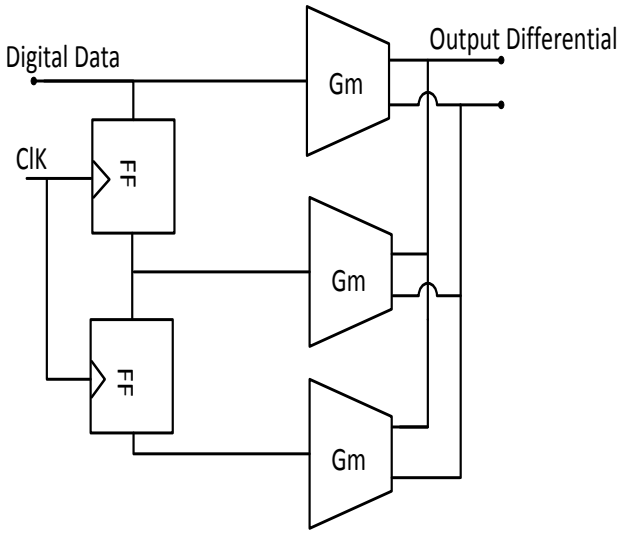

Fig. 2. Circuit Model of The FIR.

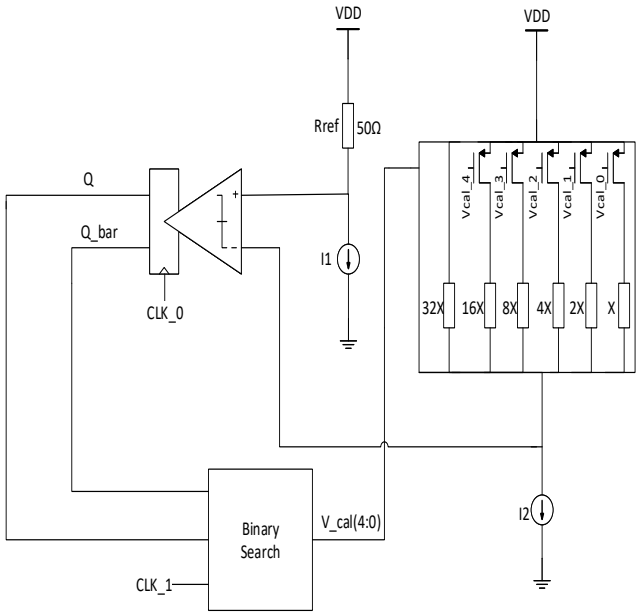

Fig. 3. Termination Calibration Circuit.

control the on-chip resistance value there are five PMOS slices with on-chip resistances and one resistance which is always on, and a current mirror is used to push the same current to the reference resistance and the slices. The Latched Comparator (Double tail latched comparator) followed by SR latch is the comparing unit in the architecture. All the calibration process is controlled and managed by a binary search block, which is a Verilog-A module designed to calibrate the slices.

2) Bandgap Reference:

Bandgap voltage references are an essential block in any analog/mixed-signal (AMS) and digital systems [4]. The BGR used in this work is based on [5] with some modification to meet the new specs. The specifications of the BGR in this work are an output voltage of 0.6 V, a maximum supply current of 10 μA, a temperature coefficient of 16 PPM over a temperature range from -40 °C to 100 °C, and the supply voltage of 1.8 V.

3) Low Dropout Voltage Regulator (LDO):

LDO circuit Function is to generate a stable supply voltage for the RX blocks. There are two LDOs, one for AFE Blocks and the other for Digital blocks. The LDO used is Cap less LDO. The advantage of the Cap Less LDO is that it is suitable for System on chip (SoC) applications. The design of this LDO is based on Cap less LDO with damping factor (based on Miller Compensation) topology with some modification [6]. Output voltage of the LDO equals 1.2 V with steady state error of 1 % and overshoot of 10 %, its Maximum current is 1 mA and its supply voltage is 1.8 V.

4) Continuous Time Linear Equalizer (CTLE):

CTLE Function is performing boosting gain at high frequency and lower gain at DC to cancel the channel response as it adds higher attenuation at high frequency. The CTLE, shown in Fig. 4, consists of a differential pair amplifier with degeneration with variable resistance R_S and capacitance C_S (as parallel slices with digital signals) which have direct control over the DC gain and the gain of high frequency components to add the ability to adapt the circuit response. A bandwidth extension technique, which is implemented with a shunt inductor, is used to obtain bandwidth of 5 GHz which is limited by load Capacitance and load resistance R_D.

The Common Mode Feedback is used to control the output common mode by using parallel slices of Resistance R_D with PMOS switches to control the value of R_D and directly adapt the common mode level.

The offset cancellation circuit is used to solve the shift in the output common mode because of the mismatch of the input differential by using current steering DAC. The current steering DAC is composed of one differential pair to decide which branch to correct its common mode and parallel slices of current tails controlled digital signals. The CTLE can compensate channel Loss from 1.5 dB up to 7.5 dB.

5) Variable Gain Amplifier (VGA):

VGA is a single stage common source amplifier with degeneration variable resistance R_S (as parallel slices with digital signals) to control the gain. The Gain Range is from 4 up to 9 dB. The same technique of Common mode feedback and offset cancellation used in the CTLE is used in the VGA.

6) Decision Feedback Equalizer (DFE):

The function of DFE is canceling the post cursor ISI and decision-making of the system as its output is a Digital signal. The proposed DFE Architecture is 3 Taps Direct Half rate DFE as its principal advantage is to relax the design of the DFE blocks more than full rate DFE. The number of taps is 3 taps to have the flexibility to equalize the transmitted data for a different channel. The DFE is composed of two identical loops for the even and the odd data. Each loop starts with a Gm-cell, which is assorted as a buffer to have a clean digital input without notches because the differential pairs of the taps are very sensitive to the output of the flip flop and slicer. For sampling the data on the summing node a slicer is used, it Slicer is a double tail latched comparator followed by SR latch with AND-OR implementation [7] and using Clocked NMOS Capacitors in the input of slicer to solve kickback noise of the dynamic comparator [8]. The D-flip-flop is used as a delay unit and built by a sense amplifier-based flip-flop which is composed of a sense amplifier and modified SR latch [9]. For the feedback, taps are used and are composed of one differential pair to steer current in the summing node and 5 parallel slices of current tails controlled digitally to control the tap coefficient.

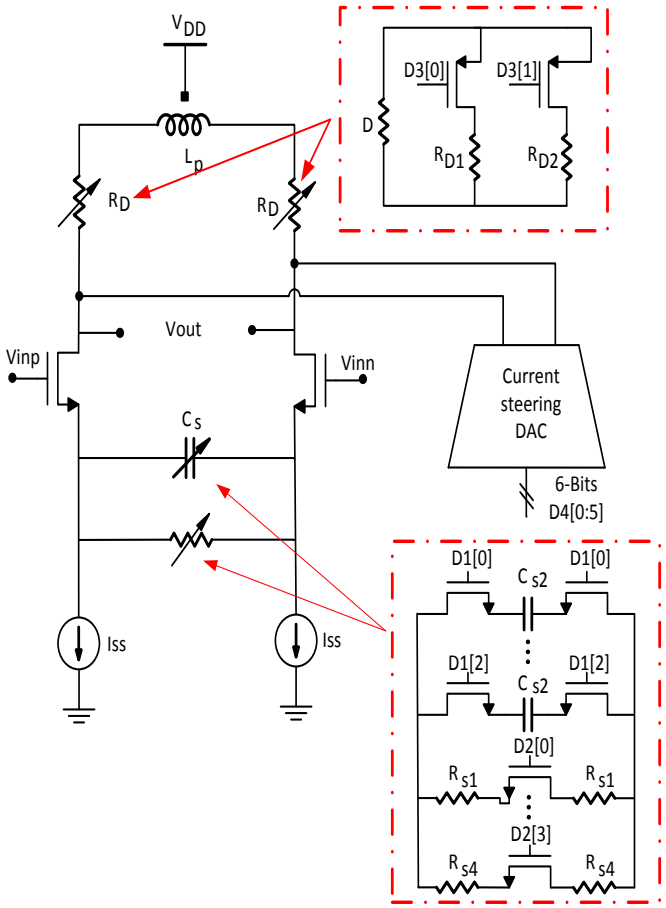

Fig. 4. Full CTLE Schematic with Offset Cancellation Circuit.

7) Clock and Data Recovery (CDR):

The CDR function is to extract the clock used in the RX part from the data [10].The CDR architecture is as in fig. 5. The Bang-Bang Phase Detector [11] is composed of four Dual Edge Triggered Flip Flops (DETFF) which is composed of 6 transmission gates [12] and 4 inverters, two symmetric XOR gates. Its outputs are early and late signals which are the input of the charge pump. The VCO used in this design is a Current Starved Ring Oscillator [13]. A typical Charge pump is used as in [14]. The VCO consists of delay units or inverters, a controlling circuit, and buffering circuit. The controlling circuit shown in Fig. 6 is responsible for controlling the current flows through the delay unit by controlling $V_{Bias,N,P}$. The controlling has two types of tuning, V_{ctrl} is used for fine-tuning and V_{b1} to V_{b8} are used for coarse tuning. In coarse tuning, thermometer code is used instead of binary code because it has an increasing function, unlike binary code. The range of frequency of the VCO is 4 to 6.2 GHz.

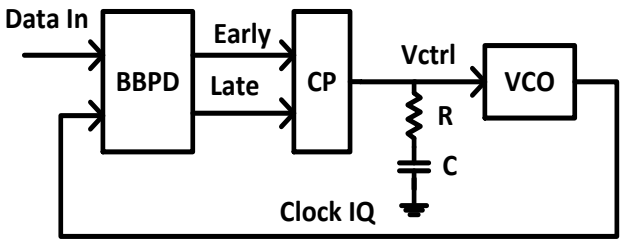

Fig. 5. Block Diagram of The CDR.

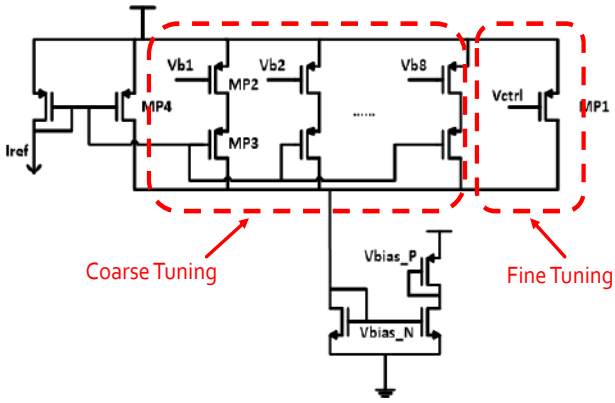

Fig. 6. The Schematic of The Controlling Circuit of The VCO.

III. Simulation Results

The 10 Gb/s receiver is designed in a 65-nm CMOS technology. The schematic simulated eye diagram of the transmitted 10 Gb/s is shown in Fig. 7. The transmitter swing is around 100 mVpp differential. The simulated eye diagram of the input of the even slicer at typical is shown in Fig. 8. The figure shows one eye opened and the other one is partially distorted. The swing is around 200 mVpp differential. The system is also simulated across process variation and temperature .The programmable equalization blocks are used to overcome the variation and achieve the best possible eye-opening, The gain of equalization blocks can be increased by changing Digital codes to adjust the equalization in SS-PV and the same in FF-PV to decrease the gain. To test the system, a BER tester is designed using Verilog-A. The results from the BER tester show that the transceiver is operating error free ($BER < 10^{-12}$).

Fig. 9 Shows the relationship between the BER and the phase of the slicer clock.

The simulated average power consumption of the different blocks is shown in Table I. The supply voltage in this case is 1.2 V and the transmission rate is 10 Gb/s. The total average power consumption is 9.58 mW. Also a comparison between this work and the previous art is shown in Table II.

IV. Conclusion

A 10 Gb/s SerDes transceiver was presented in this paper that is designed using a 65-nm CMOS technology, the entire

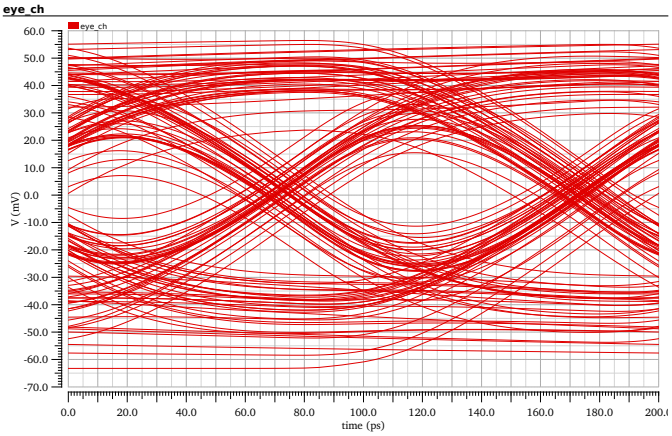

Fig. 7. Simulated transmitted eye diagram.

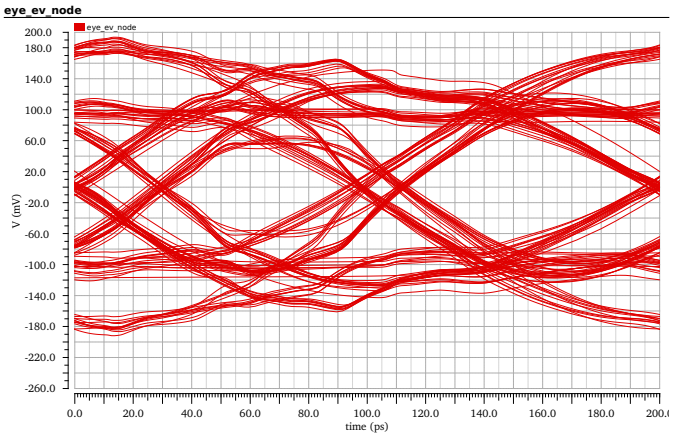

Fig. 8. Simulated even slicer input eye diagram.

transceiver uses 1.2 V supply voltage and the receiver consumes only 9.58 mW which is low compared to the published work. The designed receiver is tested with modeled transmitter using Verilog-A to show the BER of the whole transceiver with different sampling points. [20].

Acknowledgement

This work was partially funded by ONE Lab at Zewail City of Science and Technology and Cairo University, ICpedia, ASRT, NTRA, and ITAC.

TABLE I
Simulated Average Power Consumption.

Block	Average Power Consumption
PMU	0.031 mW
AFE	2.04 mW
DFE	3.6 mW
CDR	3.91 mW
Total	9.58 mW

TABLE II
COMPARISON TO PRIOR ART.

Specification	[15]	[16]	[17]	[18]	[19]	This Work
Technology	28-nm	65-nm	40-nm	65-nm	65-nm	65-nm
Data Rate	5-28.2Gb/s	16 Gb/s	16 Gb/s	1.62-10 Gb/s	32 Gb/s	10 Gb/s
Supply Voltage	0.92 V	1.2V TX, 1V RX	1.5V TX, 0.9V RX	1V	1.1V and0.9V	1.2V
Equalization	2-taps FFE, AFIR, and 2-taps DFE	4-taps FFE, 1-tap FIR, and 2-taps DFE	3-taps FFE, CTLE, and 14-taps DFE	CTLE, 2-taps data DFE, and 1-tap edge DFE	CTLE, 15-taps FFE, and 2-taps DFE	3-taps FIR, CTLE, and 3-taps DFE
Losses at Nyquist	15 dB at 28.2 GHz	27.6 dB	34 dB	23 dB	-	Over 27 dB at 5 GHz
Modulation	NRZ	NRZ	NRZ	NRZ	PAM-4	NRZ
Power Consumption (mW)	243 (TX/RX)	173.7 (TX/RX)	235 (TX/RX)	24.4 (TX/RX)	264 (TX/RX)	9.57 (RX)
BER	10^{-12}	10^{-12}	10^{-15}	10^{-12}	10^{-12}	10^{-12}
Energy per Bit (pJ/bit)	8.617	10.856	14.687	2.44	8.25	0.957

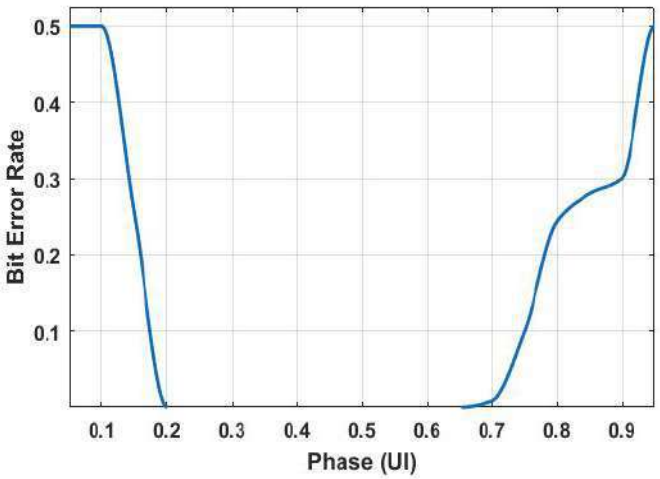

Fig. 9. BER versus the phase of the slicer clock.

REFERENCES

[1] G. Forecast, "Cisco visual networking index: Global mobile data traffic forecast update 2017–2022," *Update*, vol. 2017, p. 2022, 2019.

[2] S. S. Abeysekera, "Implementation of a zero-forcing residue equalizer using a laguerre filter architecture," in *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No. 04CH37512)*, vol. 3. IEEE, 2004, pp. III–385.

[3] V. Melikyan, A. Balabanyan, A. Hayrapetyan, and N. Melikyan, "Receiver/transmitter input/output termination resistance calibration method," in *2013 IEEE XXXIII International Scientific Conference Electronics and Nanotechnology (ELNANO)*. IEEE, 2013, pp. 126–130.

[4] A. H. Hassan, M. A. ElBadry, Y. Ismail, and H. Mostafa, "A low-power self-startup bandgap circuit for energy efficient applications," in *2017 New Generation of CAS (NGCAS)*. IEEE, 2017, pp. 29–32.

[5] H. Omran, M. H. Amer, and A. M. Mansour, "Systematic design of bandgap voltage reference using precomputed lookup tables," *IEEE Access*, vol. 7, pp. 100 131–100 142, 2019.

[6] K. N. Leung and P. K. Mok, "A capacitor-free cmos low-dropout regulator with damping-factor-control frequency compensation," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, 2003.

[7] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia, J. K.-S. Chiu, and M. M.-T. Leung, "Improved sense-amplifier-based flip-flop: Design and measurements," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 876–884, 2000.

[8] K.-M. Lei, P.-I. Mak, and R. P. Martins, "Systematic analysis and cancellation of kickback noise in a dynamic latched comparator," *Analog Integrated Circuits and Signal Processing*, vol. 77, no. 2, pp. 277–284, 2013.

[9] D. Anoop, N. K. YB, and M. Vasantha, "High performance sense amplifier based flip flop for driver applications," in *2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*. IEEE, 2017, pp. 129–132.

[10] K. Ismail, T. Ismail, and H. Mostafa, "Design and implementation of cdr and serdes for high speed optical communication networks using fpga," in *2016 18th International Conference on Transparent Optical Networks (ICTON)*. IEEE, 2016, pp. 1–3.

[11] S.-H. Lin, C.-L. Hsieh, and S.-I. Liu, "A half-rate bang-bang phase/frequency detector for continuous-rate cdr circuits," in *2007 IEEE Conference on Electron Devices and Solid-State Circuits*. IEEE, 2007, pp. 353–356.

[12] M. Pedram, Q. Wu, and X. Wu, "A new design of double edge triggered flip-flops," in *Proceedings of 1998 Asia and South Pacific Design Automation Conference*. IEEE, 1998, pp. 417–421.

[13] S. Suman, K. Sharma, and P. Ghosh, "Analysis and design of current starved ring vco," in *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*. IEEE, 2016, pp. 3222–3227.

[14] W. Rhee, "Design of high-performance cmos charge pumps in phase-locked loops," in *1999 IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 2. IEEE, 1999, pp. 545–548.

[15] M. Mahani, R. Zavari, S.-T. Lim, D. Hong, K. Scheffer, P. Graumann, H. Ransijn, T. Dusatko, S. Ho, P. Snyder *et al.*, "Multi-standard 5 gbps to 28.2 gbps adaptive, single voltage serdes transceiver with analog fir and 2-tap unrolled dfe in 28nm cmos," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, 2017, pp. 23–26.

[16] A. Roshan-Zamir, O. Elhadidy, H.-W. Yang, and S. Palermo, "A reconfigurable 16/32 gb/s dual-mode nrz/pam4 serdes in 65-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 9, pp. 2430–2447, 2017.

[17] A. Agrawal, J. F. Bulzacchelli, T. O. Dickson, Y. Liu, J. A. Tierno, and D. J. Friedman, "A 19-gb/s serial link receiver with both 4-tap ffe and 5-tap dfe functions in 45-nm soi cmos," *IEEE journal of solid-state circuits*, vol. 47, no. 12, pp. 3220–3231, 2012.

[18] J. Lee, K. Park, K. Lee, and D.-K. Jeong, "A 2.44-pj/b 1.62–10-gb/s receiver for next generation video interface equalizing 23-db loss with adaptive 2-tap data dfe and 1-tap edge dfe," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 10, pp. 1295–1299, 2018.

[19] S. Kiran, S. Cai, Y. Luo, S. Hoyos, and S. Palermo, "A 32 gb/s adc-based pam-4 receiver with 2-bit/stage sar adc and partially-unrolled dfe," in *2018 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2018, pp. 1–4.

[20] H. ElGemmazy, A. Helmy, H. Mostafa, and Y. Ismail, "High cmrr and wideband current-mode instrumentation amplifier using fully differential operational floating conveyor," in *2017 Japan-Africa Conference on Electronics, Communications and Computers (JAC-ECC)*. IEEE, 2017, pp. 45–48.