FPGA Utilized Implementation of Epileptic Seizure Detection System Based on Wearable Devices using Dynamic Partial Reconfiguration

Mohamed Fawzy
Siemens Digital Industries Software
Cairo, Egypt
mohamed.el-kholy@siemens.com

Ahmed Hussien
Electronics and Electrical Communications Engineering Department
Cairo University, Giza, Egypt
ahmed.hussien60@gmail.com

Hassan Mostafa
University of Science and technology, Nanotechnology and Nanoelectronics Program
Zewail City of Science and Technology, October Gardens, 6th of October, Giza 12578, Egypt.
hassanmostafahassan@gmail.com

***Abstract*— Unplanned seizures are caused by a disorder in the central nervous system known as epilepsy. Although significant advancements have been made in the realm of non-EEG wearable devices, there is still much room for improvement in the field of EEG-based seizure detection and prediction using ML. The management of epilepsy has a lot of promise to be aided by non-invasive wearable technology. The suggested study intends to design and implement a support vector machine (SVM) classification-based epileptic seizure detection system based on various wearable devices. The proposed technique for detecting seizures accomplishes According to data for seizure detection, our system consistently achieves a sensitivity of 100% and an accuracy of 97%. High level MATLAB model creation is part of the design cycle. Despite the fact that high performance cannot be achieved with just one signal. Although a high performance detection system cannot achieve the requisite sensitivity and accuracy with a single signal, we presented various combining techniques. RTL modelling, design optimization, FPGA implementation, and functional verification are all included in the implementation cycle. The capacity of the FPGA's partial dynamic reconfiguration is suggested for implementation in order to make better use of the available resources. Comparing the proposed implementation to relevant earlier work, it demonstrated improved utilization.**

Keywords—Epilepsy, FPGA, Implementation, seizure, detection, wearable, SVM, DPR

I. INTRODUCTION

More than 50 million people worldwide cannot live a normal life because they have epilepsy. Unplanned seizures caused by a disorder in the patient's neurological system are known as epilepsy. Only 66% of patients are successfully treated with epileptic medications. When medications are unable to treat an epileptic case, surgery is the next possible choice. Due to the need to localise the epileptogenic zone, not all epileptic cases are surgical candidates. A 60% success rate for lobe surgery is possible, compared to a 35% success rate for extratemporal lobe surgery. [1]
A number of surveys assessing patients' preferred seizure detection techniques are mentioned in [2-5]. All of them have a bias in favour of detachable, non-invasive, and low-visibility gadgets. Contrarily, patients have a difficult time accepting devices that could include wearing a helmet or that could have patch electrodes on the face, neck, or head [3]. Therefore, the patients' preferences are unmistakably in favour of non-EEG-based detection technologies. These gadgets might be wearable, such a wristband, purse, necklace, or a system for intelligent clothing or a belt, or they could correlate to patch electrodes worn on the chest, shoulder, or arm [3].

There is still tremendous need for development in the area of non-EEG wearable devices, despite significant advancements in EEG-based seizure detection and prediction utilizing machine learning. The management of epilepsy has a lot of potential to benefit from non-invasive wearable technology. The patients must be willing to wear these devices for extended periods of time and they must have strong signal quality.

The problem of seizure prediction and detection has been studied in the past using a variety of methods, including machine learning models [6], deep learning models [7], statistical models [8], and other methods [9]. Support vector machine classifiers, which have a history of success, are one of the most widely used machine learning techniques.

The structure of the paper is as follows. A background on the evaluated dataset of wearable devices is given in Section II, and an example of the best seizure detection system is shown in Section III. Section IV provides a summary of the hardware setup. Section V demonstrates the use of dynamic partial reconfiguration to optimize resource consumption, and Section VI compares the results of the syntheses with earlier research.

II. DATASET OF WEARABLE DEVICES

The dataset evaluated during this work is attained from the Epilepsy Foundation of America - My Seizure Gauge Public Dataset. These data collected by non-invasive wearable biosensors and devices [10], [11] and provides long-term recordings (Between 3-5 days) of epilepsy patients which implies there are more seizures per patient. Recordings from nineteen patients are provided together with seizure times and metadata about the recordings. Data are provided from three devices: Empatica E4, ByteFlies Sensor Dots and Epilog. These devices are recording following signals: Limb accelerometry in three axes (ACCX,ACCY,ACCZ,ACCMAG), Blood volume pulse (BVP), Electrodermal activity (EDA), Heart rate (HR),Temperature (TEMP), Electromyography (EMG), Photoplethysmography (PPG).

978-1-6654-6463-5/22/$31.00 ©2022 IEEE

Summary of each device and corresponding recorded signals is mentioned in table 1. Machine learning algorithm in this paper evaluated on patient "MSEL_01097" which having all recorded signals.

Table 1 - Summary of Wearable devices

Device	*Location*	*Signals*
Empatica E4	Wrist	ACC,BVP,EDA,HR,Temp
ByteFlies Sensor	Variable (patch)	ACC,PPG or EMG
Epilog	Forehead	Single-channel EEG

III. SEIZURE DETECTION SYSTEM

The block diagram of the 4-stage seizure detection system utilized in this work is depicted in Fig 1

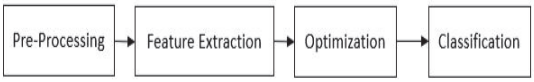

Figure 1 – Block Diagram of Seizure Detection System

This Paper is extension to self-work published in [12] where described the different blocks of system. starting with the different stages of data pre-processing, then described the feature extractor phase along with the different exercised features in time and frequency domains and the optimum selected features based on different performance metrics, results proved that some signals achieved high sensitivity results. However, one signal is not enough to achieve good results in both sensitivity and accuracy (>95%) and need more optimization of the model. Previous published paper also explained the proposed different combining methods of bio signals which lead to achieving desired both sensitivity and accuracy. Paper also discussed the selection of optimum window length. Seizure detection is considered a classification problem between two classes, the ictal period when a true seizure happens and the non-ictal period including postictal, pre-ictal and inter-ictal periods. Support vector machine (SVM) is one of the most popular classification techniques. SVM is chosen in binary classification problems as proven excellent accuracy in seizure detection as stated in [13-15]. Three performance metrics are exploited in this work: sensitivity, specificity, and accuracy. Sensitivity is the ability of a test to correctly identify those with the disease which is also known as true positive rate. Specificity is the ability of the test to correctly identify those without the disease which is also known as true negative. Accuracy refers to how close a sample statistic is to a population parameter

$$Sensitivity = \frac{TP}{TP + FN} \times 100 \quad (1)$$

$$\text{Specificity} = \frac{TN}{TN + FP} \times 100 \quad (2)$$

$$\text{Accuracy} = \frac{TP + TN}{TP + TN + FP + FN} \times 100 \quad (3)$$

Table 2 shows a summary for the final three proposed models using different signals, window length and signals combining algorithm along with their performance measurements. Hardware complexity implementation of related extracted features can be metric for model selection.

Table 2 - Proposed Seizure Detection System

Signals	*Features*	*Window*	*algorithm*	*Sensitivity*	*Accuracy*
EMG, BVP, ACCY	Approximate Entropy root mean square Fluctuation Index	4	assumed weights	100	95.9
TEMP, EMG, ACCX	Fractal Dimension Approximate Entropy Fluctuation Index	1	Machine learning	100	96.9
EMG, BVP, EDA	Approximate Entropy root mean square Shannon Entropy	4	Machine learning	100	96.5

IV. HARDWARE IMPLEMENTATION OF SEIZURE DETECTION SYSTEM

A. Field Programmable Gate Arrays (FPGA)

FPGAs are integrated circuits that are frequently available off-the-shelf. Configurable logic blocks (CLBs) and a set of programmable interconnects found in FPGAs enable the designer to join blocks and set them up to carry out anything from straight forward logic gates to intricate operations. FPGAs are more energy-efficient than CPUs and GPUs and are perfect for embedded applications. The flexibility, configurable parallelism, and adaptability of an FPGA make them particularly well-suited for boosting machine learning and deep learning operations.

B. General optimization techniques

The main challenge in hardware implementation is optimizing the complexity of original algorithm to fit the hardware limitations to achieve optimum area and power. Following are some general techniques used in the optimization trials and performance comparison used to validate them as there must be acceptable impact on the sensitivity and accuracy results.

Many steps having division by a particular constant, as seen in the feature equations. Because it is simply linearly scaling all the data, removing multiplication and division by constants has no impact on the classification outcome. The classifier adjusts the hyper-plane it creates by the corresponding scaling amount. Figure 2 depicts the outcome of eliminating division or multiplication by a constant and linearly scaling data points.

Approximating complex functions into simpler ones which have most similar curve and accordingly having acceptable performance degradation in the favor of saving power and area. Figure 2 showing example for the analogy between Ln function and SQRT function. The approximated feature extractor prioritizes area and power requirements over maintaining the original sensitivity. The approximate design aims for a performance loss of 1-2 percent in favor of power and area savings.

Using Logarithm Properties as target algorithms having different logarithm operations. Following Example for one the logarithm transformations

$$\sum_{i=1}^{M} \log\left(P(x_i)\right) = \log\left(\prod_{i=1}^{M} P(x_i)\right) \quad (4)$$

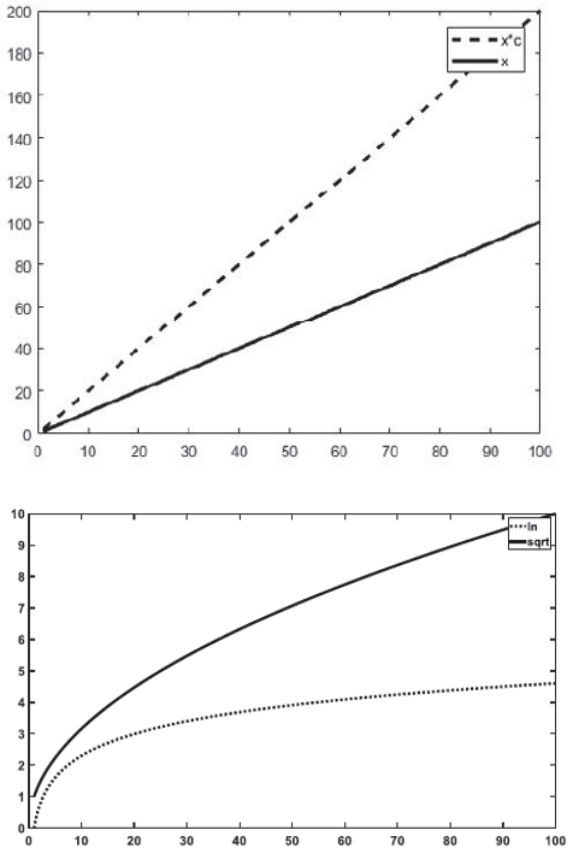

Figure 2 - General optimization techniques

C. Implementation of Shannon Entropy Extractor

Signals' continuous values are quantized. The frequency of each level is then determined. Input values from a big set (typically a continuous set) are mapped to output values in a countable smaller set, frequently with a finite number of elements, in a process known as quantization.

$$H(x) = -\sum_{i=1}^{M} P(x_i) \cdot \log\big(P(x_i)\big), P(x_i) = \frac{\text{Frequency}}{N} \quad (5)$$

Where M is the number of levels and N is the length of symbol

Exercised different optimization techniques as mentioned above like: Removal of division by constant, Logarithm transformation, Approximation of complex functions. Compared the performance of different proposed optimizations with the performance of original algorithm. Selected following configuration as the optimum approximation performance

$$H(x) = -\sum_{i=1}^{M} \text{sqrt}\big(P(x_i)\big) \ , P(x_i) = \text{Frequency} \quad (6)$$

Quantization block having different configurations: the input signal can be configured as the input signal as it is or normalized by subtraction from the minimum value, number of quantization levels, the value of minimum level can be configured as zero or the global minimum value, the value of minimum level can be configured as zero or the global minimum value and finally the value of maximum level can be configured as local or global or variable maximum value. Exercised different configurations and performance measurements proved using 5-levels quantization with zero as the minimum value and using the input signal as it is and using variable max value. Using variable maximum complicating the Hardware implementation so instead of finding maximum value, tried to get relation between maximum and first values and calculate the average of difference between them. results proving this correlation and accordingly calculated the average bias.

Figure 3 showing the block diagram of Shannon entropy which starting by adders and dividers for calculating the values of the levels. Dividing by 2 is simply executed by simple shifter. Then using absolute subtraction and minimum block for the quantization operation. Then using counters for calculating the frequency of each level and finally using the root mean square and summation for calculating the entropy.

Based on following statistics, Input is always decimal so fractional part for input is zero and integral part selected based on the maximum value which is 34 bits. Output is floating number, Integral part selected to 5 bits based on the maximum value and fractional part selected based on performance experiments and comparing with the results of floating number.

Input	decimal	Output	decimal
min	75311776	min	11.3137085
max	10415661056	max	20.97902707

Following is summary of the synthesis results of Shannon entropy extractor on FPGA Xilinx Artix-7.

Site Type	Used
Slice LUTs	312
Register as Flip Flop	76
Bonded IOB	52
BUFGCTRL	1
Total On-Chip Power: 8.139 W	
Frequency: 110 MHz	

D. Implementation of Approximate Entropy Extractor

The output value shows if the input signal is regular. Approximate entropy has been used in literature to categorize EEG in mental disorders such schizophrenia, epilepsy, and addiction. The dataset is separated into overlapping subsequent, where r designates a filtering threshold and m determines the length of each subsequent. Following are the calculations for the correlation between these events and approximate entropy.

$$\phi^m(r) = \frac{1}{N-m+1} \sum_{i=1}^{N-m+1} \log C_i^m(r) \ , ApEn = \phi^m(r) - \phi^{m+1}(r) \quad (7)$$

Exercised different optimization techniques as mentioned above and selected following configuration as the optimum approximation performance

$$ApEn = log\phi^m(r) - log\phi^{m+1}(r) \ , \ \phi^m(r) = \sum_{i=1}^{N-m+1} C_i^m(r) \quad (8)$$

The main configuration of approximate entropy block is selecting the window size (m). Experiments showed that window size is not affecting only the performance but

also the latency of algorithm which conclude that less window size leads to increase in latency and better performance so selected window size(m) as 2. The block diagram of basic implementation of approximate entropy which starting with storing all the data into memory then reading each cycle specific addresses to create the subsequent windows then using the comparators and counters to calculate the correlation and finally using the logarithm and subtraction to calculate the approximate entropy. To overcome the long latency issue of previous implementation, applied the parallelism to be able to calculate the correlation of multiple windows at same time. Figure 4 showing the block diagram of this parallel implementation of approximate entropy. The main change in implementation is the parallel usage of the comparators which mainly used to calculate the correlation and accordingly the memory write/read addresses used to create the subsequent windows. Using Parallelism is tradeoff between the latency and area of the design. The latency mainly affected by the number of iterations for calculation the correlation and the area mainly impacted by the number of comparators. The memory read and write sequences also impacted as in non-parallelism design, read operation from the memory can be started just after three cycles as in first read operation we need only to access the first three elements while in full parallelism design, read operation should be started after completely writing the data into the memory as first read operation need to access the whole memory. Parallelism implementation can be configured by the number of stages to balance between the latency and the area of design. Table 3 summarizing the latency, number of comparators and memory write/read sequences for the different implementations: non-parallelism, full parallelism and semi parallelism which having Parallelism factor which is number of stages (k). Generalized equations for latency and number of comparators calculation based on the number of stages(k) as following

$$Latency = \frac{(\mathrm{N} - \mathrm{m} + 1)^2}{(\mathrm{K} - 1)} \quad (9)$$

$$Number\ of\ comparators = [K * m] + (k-1)(m+1) \quad (10)$$

Table 3 - Parallelism Impact for Approximate Entropy

Implementation (m = 2)	Latency	#Comparators	Memory Read/Write sequences
Non-Parallelism	(N-m+1)^2 =58564	=m+(m+1) = 2m+1 = 5	Read is delayed 3 cycles as in first read operation, we need to access first 3 elements
Full Parallelism (#stages = k = N-1=242)	=N+N-m+1 = 2N-m+1=485	=[m*(N-1)] + [(m+1)*(N-2)] = [2*242]+[3*241] = 484 + 723 = 1207	Read is started after completely write in the memory
Semi Parallelism (Parallelism factor = #stages = k)	(N-m+1)^2/(K-1) =(242)^2 / (K-1)	[K*m] + (k-1)(m+1) =2K+3K-3=5K-3	Read is started after partially write in the memory based on the papalism factor

Based on following statistics, Input is always decimal so fractional part for input is zero and integral part selected based on the maximum value which is 34 bits, Output is floating number, Integral part selected to 2 bits based on the maximum value and fractional part selected as 3 bits based on performance

Input	Decimal	Output	decimal
min	-282645623734272	min	0.004141
max	288304008265728	max	1.046617

Following is summary of the synthesis results of Shannon entropy extractor on FPGA Xilinx Artix-7.

Site Type	Used
Site Type	Used
Slice LUTs	5934
Register as Flip Flop	4015
F7/F8 Muxes	1440

Total On-Chip Power: 17.2 W

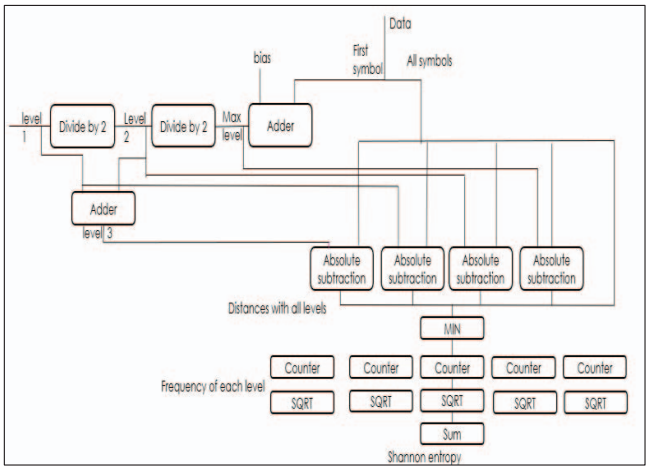

Figure 3 - Block Diagram of Shannon Entropy

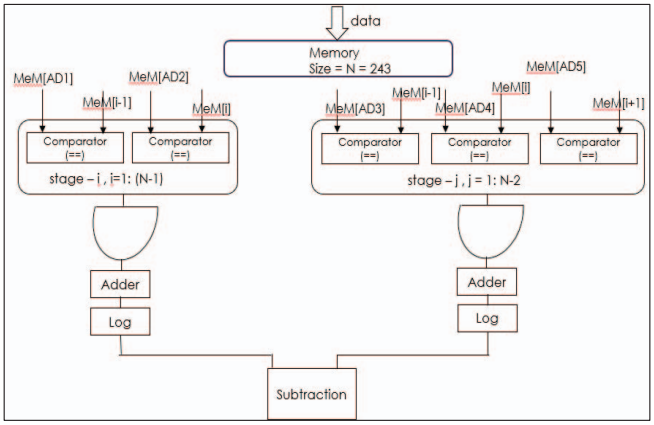

Figure 4 - Block diagram of parallel approximate entropy design

E. *Implementation of Fluctuation Index extractor*

Implementation of SVM classification, Fluctuation Index extractor and Fractal Dimension extractor is discussed in [16] and used same architecture.

V. Dynamic Partial Reconfiguration

SRAM-FPGAs have the capability of dynamic partial reconfiguration (DPR), which provides the freedom to change a portion of the FPGA while using the same hardware resources [17]. The Xilinx DPR design flow requires that the design be divided between a dynamic part and a static part [18]. The system's dynamic component is made up of the reconfigurable modules (RMs), whereas the static component is made up of the static modules that remain unchanged after reconfiguration.

The following are the primary benefits of reconfigurable systems:

1. Resource utilization: When a typical design is implemented, the majority of the hardware resources are not used until after it has been turned on and has been running for a while. By just implementing the active part of the design in the allocated period and time multiplexing the resources between the design hardware modules in accordance with the activity schedule, reconfigurable hardware and DPR will increase resource usage.

2.Scalability: using reconfigurable hardware allows upgrading system to accommodate freshly defined tasks to handle the growth in technology and features. It also enables the deploying of bug fixing in hardware, which decreases the cost of re-deploying new hardware and increase the time-to-market for products.

3. Reusability: reusing the resources for different design implementations is enabled, where a system can be customized for adaptability.

4. Power reduction: considered the most important detail, where power dissipated in the system although most of the parts are not working. In the Integrated Circuits (IC) design, the leakage power is the power consumed by the device, while it is even not active. FPGA reconfiguration helps in delaying the implementation of a specific part until the time of operation, which decreases the consumed power over time and though the battery lifetime.

5. Area: instead of implementing a full system in a horizontal way, which consumes area, a system can be optimized by vertical implementation idea which uses programming in space and time, where a stack of blocks is stored and loaded at the time of operation. This will save the area used by the same blocks in the horizontal design.

A. *Proposed Implementation*

The main challenge in hardware implementation for wearable devices-based seizure detection system is using multiple extractors for the different bio signals and accordingly proposed improving the hardware utilization by using the FPGA partial dynamic reconfiguration capability of Xilinx where we consider each feature extractor as configurable module. First step in applying the partial dynamic reconfiguration is unifying the interface to create the common interface for all configurable modules. Figure 5 showing the block diagram of the basic implementation without using the partial dynamic reconfiguration where using four different feature extractor blocks and accordingly four different SVM classiffiation blocks and finally the majority decision block while Figure 6 showing the block diagram for the proposed implementation using the partial dynamic reconfiguration. This implementation having the different feature extractor as the configurable module and using one common svm classification block. This needs additional blocks, starting with mode selection counter which select the configurable module to specific feature extractor , four FIFOs for storing the signals of the de-activated extractors, Multiplixer for the SVM configuration to switch to the proper feature classification and finally FIFO for storing the classification output of each signal to enable the decision block once this FIFO is full.

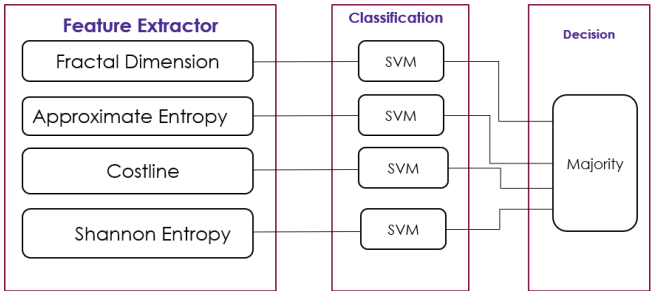

Figure 5 - Block diagram of the basic implementation

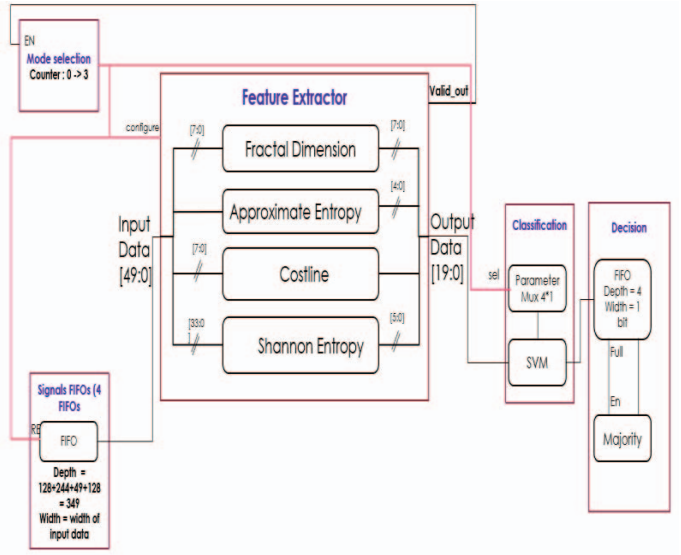

Figure 6 - Block diagram for the proposed implementation using the partial dynamic reconfiguration

This Propsed implementation aims for improving the hardware utilization and accordingly compared the utilization of proposed implementation with the utilization of basic implementation. Table 4 summarizing the utilization comparison for the prposed implementation with considering also the overhead of DPR implenation due to the extra modules like FIFOs,Multiplixers,Counters which proving reducation gain 0.68x

Table 4 – DPR Utilization (feature Extraction + SVM)

Implementation	Slice LUTs	Slice Registers	F7 Muxes	F8 Muxes	Total
Basic Implementation	11571	5270	1100	416	18357
DPR Implementation	6614	4211	1040	416	12281
Overhead	127	55	16	0	198
Reduction Percentage ((DPR+Overhead)/Basic)	0.582577	0.809488	0.96	1	0.679795

VI. COMPARISON WITH RELATED WORK

The suggested design excels earlier works in the literature in terms of sensitivity and specificity. Additionally, Table 5 shows a comparison between the proposed methods and other seizure detection systems at the FPGA-system level.

The highest achieved sensitivity by the proposed design is higher than that in [19-22],[16],[24]. Moreover, the utilization of the design is better than the mentioned previous work.

Table 5 - Implementation comparison with other work

Model	FPGA	LUTs	Registers	Sensitivity	Specificity	Accuracy
[19]	Virtex - 5	2583 0.3KB memory		95.24%		
[20]	Zynq-7000 XC7Z02	9202	10579	98.4%	0.35 6/h	
[21]	Microsemi Igloo	1237 5.56 KB memory		92.51%	80.1 %	
[22]	Pynq-Z1	17492	16685	92.9%	96%	95.8%
[24]	Virtex-7			77.95%	95%	
[16]	Virtex-7	7611	2342	96.7%	90%	90.4%
Proposed Implementation	Artix-7	6741	4266	100%	96%	97%

VII. CONCLUSION

This experiment demonstrated that wearable devices have significant potential to be employed in high accuracy epileptic seizure detection systems. They fulfil the needs and preferences of seizure patients. Although a high-performance detection system cannot provide the requisite sensitivity and accuracy with a single signal, many combination techniques have been presented [23]. The FPGA platform is used to develop this seizure detection system with high sensitivity resources.

The implemented system exploits Approximate Entropy, Fluctuation Index, Fractal Dimension and Shannon Entropy for feature extraction after exercising 23 different features with all their possible combinations, in addition to support vector machine training and classification after comparison with other different classifiers. The maximum achieved accuracy of the proposed system is 97%, while the highest achieved sensitivity obtained is 100% at 100 MHz operating frequency.

Dynamic Partial Reconfiguration capability in FPGAs is used to improve the utilization of resources and achieved gain 0.68x.

REFERENCES

[1]P. Boon, T. Vandekerckhove, E. Achten, E. Thiery, L. Goossens, V. K, D. M, G. Van Hoey, B. Vanrumste, B. Legros and e. al., "Epilepsy surgery in Belgium, the experience in gent," Acta Neurologica Belgica, no. 99, p. 256, 1999.

[2]Bruno E, Simblett S, Lang A, Biondi A, Odoi C, Schulze- Bonhage A, et al. Wearable technology in epilepsy: the views of patients, caregivers, and healthcare professionals. Epilepsy Behav 2018;85:141–9.

[3]Hoppe C, Feldmann M, Blachut B, Surges R, Elger CE, Helmstaedter C. Novel techniques for automated seizure registration: patients' wants and needs. Epilepsy Behavior 2015;52:1–7.

[4]Janse SA, Dumanis SB, Huwig T, Hyman S, Fureman BE, Bridges JFP. Patient and caregiver preferences for the potential benefits and risks of a seizure forecasting device: a best-worst scaling. Epilepsy Behav 2019;96:183–91.

[5]Tovar Quiroga DF, Britton JW, Wirrell EC. Patient and caregiver view on seizure detection devices: a survey study. Seizure 2016;41:179–81.

[6]I. Alaa, N. Ahmed, M. Nader, A. Magdy, M. Ibrahim, M. Khalil, M. H.Zakhari, and H. Mostafa, "Seizure Prediction & Segmentation Merge Yielding a Boosted Low Power Model", IEEE International Conference on Microelectronics (ICM 2019).

[7]Khan H, Marcuse L, Fields M, Swann K, Yener B. Focal onset seizure prediction using convolutional networks. IEEE Trans Biomed Eng 2018.

[8]Myers MH, Padmanabha A, Hossain G, de Jongh Curry AL, Blaha CD. Seizure prediction and detection via phase and amplitude lock values. Front Human Neurosci 2016.

[9]Zandi AS, Tafreshi R, Javidan M, Dumont GA. Predicting epileptic seizures in scalp EEG based on a variational Bayesian Gaussian mixture model of zerocrossing intervals. IEEE Trans Biomed Eng 2013.

[10]Kuhlmann, L., Karoly, P., Freestone, D.R., et al., (2018) Epilepsyecosystem.org: Crowd-Sourcing Reproducible Seizure Prediction with Long-Term Human Intracranial EEG, Brain, awy210, https://doi.org/10.1093/brain/awy210

[11]Nasseri, M, Nurse, E, Glasstetter, M, et al. Signal quality and patient experience with wearable devices for epilepsy management. Epilepsia. 2020; 00: 1– 11. https://doi.org/10.1111/epi.16527.

[12] M. Fawzy and H. Mostafa, "High Accuracy Epileptic Seizure Detection System Based on Wearable Devices Using Support Vector Machine Classifier," 2021 International Conference on Microelectronics (ICM), 2021, pp. 124-127, doi: 10.1109/ICM52667.2021.9664898.

[13]Y. Liu, W. Zhou, Q. Yuan, and S. Chen, "Automatic seizure detection using wavelet transform and SVM in long-term intracranial EEG," IEEE Trans. Neural Syst. Rehabil. Eng., vol. 20, no. 6, pp. 749–755, Nov. 2012.

[14]H. Elhosary, M. H. Zakhari, M. A. Elgammal, M. A. Abd El Ghany, K. N. Salama and H. Mostafa, "Low-Power Hardware Implementation of a Support Vector Machine Training and Classification for Neural Seizure Detection," in IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 6, pp. 1324-1337, Dec. 2019, doi:10.1109/TBCAS.2019.2947044.

[15]M. A. Elgammal, H. Mostafa, K. N. Salama and A. Nader Mohieldin, "A Comparison of Artificial Neural Network(ANN) and Support Vector Machine(SVM) Classifiers for Neural Seizure Detection," 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS), Dallas, TX, USA, 2019, pp. 646-649, doi: 10.1109/MWSCAS.2019.8884989.

[16]H. Elhosary, M. H. Zakhari, M. A. Elgammal, K. A. H. Kelany, M. A. Abd El Ghany, Khaled N. Salama, and H, Mostafa, " Hardware Acceleration of High Sensitivity Power-Aware Epileptic Seizure Detection System Using Dynamic Partial Reconfiguration," IEEE Access, vol. 9, pp. 75071-75081, 2021.

[17]D. Koch, "Partial Reconfiguration on FPGAs: Architectures, Tools and Applications", Springer Publishing Company, 2013 .

[18]Xilinx Inc., "Partial Reconfiguration User Guide UG909", 2016.

[19]]A. Page, C. Sagedy, E. Smith, N. Attaran, T. Oates and T. Mohsenin, "A Flexible Multichannel EEG Feature Extractor and Classifier for Seizure Detection," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 2, pp. 109-113, Feb. 2015 .

[20]H. Wang, W. Shi and C. Choy, "Hardware Design of Real Time Epileptic Seizure Detection Based on STFT and SVM," in IEEE Access, vol. 6, pp. 67277-67290, 2018

[21]T. Zhan, S. Z. Fatmi, S. Guraya and H. Kassiri, "A Resource-Optimized VLSI Implementation of a Patient-Specific Seizure Detection Algorithm on a Custom-Made 2.2 cm^2 Wireless Device for Ambulatory Epilepsy Diagnostics," in IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 6, pp. 1175-1185, Dec. 2019 .

[22]D. Serasinghe, D. Piyasena and A. Pasqual, "A Novel Low-Complexity VLSI Architecture for an EEG Feature Extraction Platform," 21st Euromicro Conference on Digital System Design (DSD), Prague, 2018, pp. 472-478, 2018 .

[23] Mohamed Fawzy, Hassan Mostafa. "High Accuracy Epileptic Seizure Detection System Based on Wearable Devices Using Support Vector Machine Classifier", 2021 International Conference on Microelectronics (ICM), 2021

[24] Z. Taufique, A. Kanduri, M. A. Bin Altaf and P. Liljeberg, "Approximate Feature Extraction for Low Power Epileptic Seizure Prediction in Wearable Devices," 2021 IEEE Nordic Circuits and Systems Conference (NorCAS), 2021, pp. 1-7