Multi Energy Harvesters For Biomedical

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List of Symbols and Abbreviations

ILPS	Inductive link power supply
IMDs	Implantable medical devices
PCE	Power conversion efficiency
RFID	Radio-frequency identification
VD	Voltage doubler
OTA	Operational trans conductance amplifier
EA	Error amplifier
PM	Phase margin
GBW	Gain bandwidth
LDO	Low dropout regulator
V_{REF}	reference voltage
PSRR	Power supply rejection ratio
CTAT	Complementary-to-absolute-temperature
PVT	Process Variables Temperature.
PTAT	Proportional-to-absolute-temperature
Rout	Stage Equivalent Resistance
Vout	Output Voltage Of The charge Pump
ŋ	power Efficiency Of The charge Pump
MPPT	Maximum Power Point Tracking
VCO	Voltage Control Oscillator
TEG	Thermoelectric generator

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Abstract

This project will investigate the problem of ENERGY. An energy crisis is a significant bottleneck in the supply of energy resources. Industrial development and population growth have led to a surge in the global demand for energy in recent years. The energy problem is the most irritating problems nowadays in the field of electronics and communication.

The project has two branches:

- The first branch is bio-medical interfacing which is implementation of biomedical interfacing circuit that receives the analog signal from an electrode implanted in the brain and provides it in a digital format for further processing.
- The second branch is micro-scale energy harvesting which is implementation of micro-scale energy harvesting system capable of delivering the required power to a brain biomedical interfacing circuit using piezoelectric, thermal, RF, Inductive link, or infrared energy harvesting system.

Our project is the second branch; it is the part responsible for providing the sufficient amount of energy to the bio-medical interfacing circuit and the processing unit to try to treat the epilepsy cases by knowing the signal reaches the brain.

The whole system is consisting of: the transducer of any kind mentioned above, then the rectification and regulation stage, and at last there is the rechargeable battery that feeds the bio-medical interfacing circuit and the processing unit with energy.

Through the survey about energy harvesting systems, we are implementing three kinds of interfacing circuits to three transducers. They are thermal, which has output voltage DC, and inductive link, and piezo-electric, which has output voltage AC.

The DC voltage needs to be regulated before it can charge the battery. However, the AC voltage needs to be rectified first, and then it is regulated before charging the battery.

Chapter 1 Introduction

In a new class of miniaturized electronic systems (e.g. Smart dust sensors, biomedical implants that enable new application domains. Despite the stringent constraints on size (and hence battery capacity), these systems are often required to operate for several months to years without the need for battery replacement, because frequent battery replacement may be either infeasible or prohibitively expensive. Environmental energy harvesting represents an attractive approach to alleviate the energy supply challenge in these systems and has the potential to result in self-powered, perpetual system operation. While the basic idea of environmental energy harvesting has been extensively explored and applied at the macro-scale in the context of large systems such as solar farms, windmills, etc., designing micro-scale energy harvesting systems involves several new challenges. Most of these challenges stem from the fact that the form-factor constraint in these systems mandates the use of miniature energy transducers (a few cm3). As a result, the maximum power output of these micro-scale transducers is extremely small, often only a few mW. Therefore, the harvesting subsystem should be carefully designed to extract as much power as possible from the transducer and transfer it to the electronic system with minimal loss, which requires extremely energy efficient design. This paper presents an Overview of the various system-level tradeoffs and design considerations involved in designing such highly efficient micro-scale energy harvesting systems.

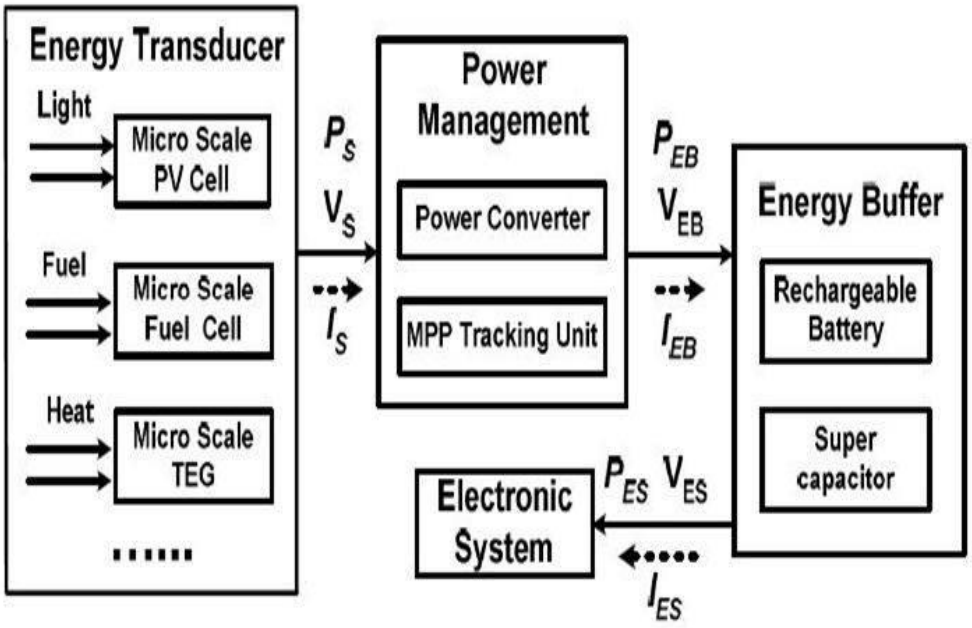


Figure 1.1: Block diagram of a micro- scale harvesting system

Energy harvesting devices generate electric energy from their surroundings through direct energy conversion. Currently, implanted batteries provide the energy for implantable biomedical devices. However, batteries have fixed energy density, limited lifetime, chemical side effects, and large size. Devices powered by harvested energy have longer lifetime and provide more comfort and safety than conventional devices.

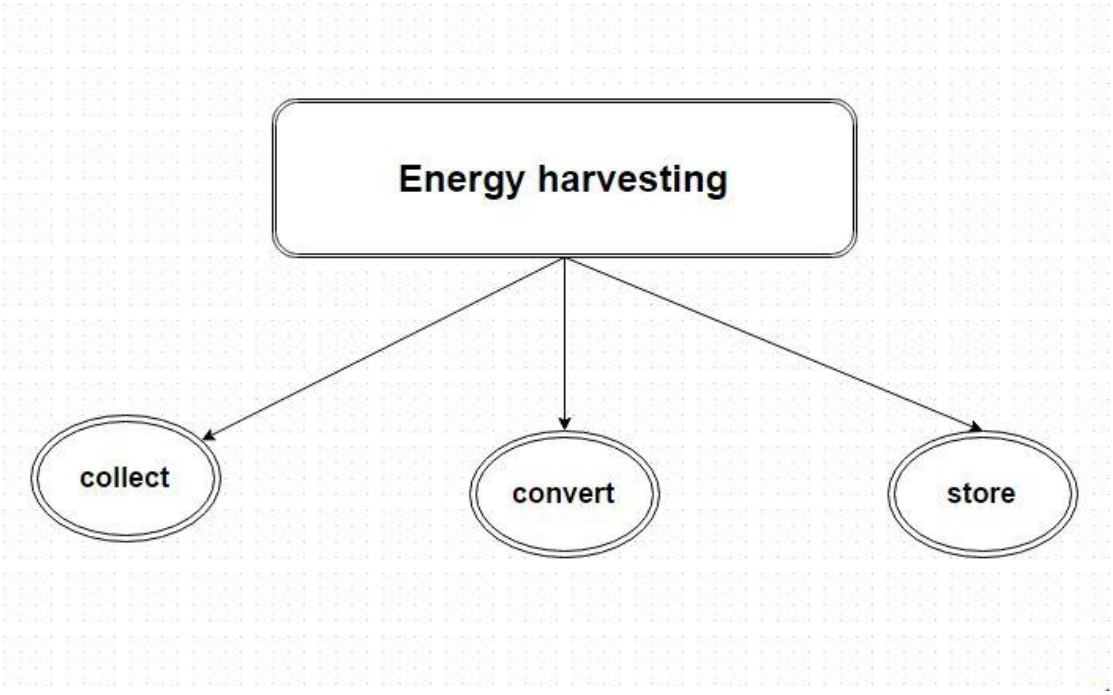


Figure 1.2: Energy harvesting tree

In the above figure we show the three main blocks for any type of energy harvesting system:

i. Collect: which collect all types of different sources of energy like (inductive, capacitive, thermal, solar and kinetic….etc.).
ii. Convert: which convert all this types of energy to electric energy to use it to operate the biomedical application.
iii. Store: which store the electric energy in buffer like small battery or super capacitor to use it later in any application we need.

Advanced technical developments have increased the efficiency of devices in capturing trace amounts of energy from the environment and transforming them into electrical energy. In addition, advancements in microprocessor technology have increased power efficiency, effectively reducing power consumption requirements. In combination, these developments have sparked interest in the engineering community to develop more and more applications that utilize energy harvesting for power.

Energy harvesting from a natural source where a remote application is deployed, and where such natural energy source is essentially inexhaustible, is an increasingly attractive alternative to inconvenient wall plugs and costly batteries. This essentially free energy source, when designed and installed properly, is available maintenance-free and is now available throughout the lifetime of the application. Such systems can be more reliable than wall plugs or batteries.

In addition, energy harvesting can be used as an alternative energy source to supplement a primary power source and to enhance the reliability of the overall system and prevent power interruptions.

So energy harvesting has many advantages:

- Avoid battery chemical reaction.
- Avoid battery large size.
- Avoid battery limited life.
- Provides natural energy sources.
- Provides mobility.
- Allow for charging in applications.

Many real life applications using energy harvesting system power are now practical. Wireless sensor network systems such as ZigBee systems often benefit from energy harvesting power sources. For example, when a wireless node is deployed at a remote site where a wall plug or a battery is either unreliable or unavailable, energy harvesting can augment or supply power. In another example, a remote control node running on energy harvesting can be implemented as a self-powered electronic system. And in yet other situations, multiple energy sources can be used to enhance the overall efficiency and reliability of any system. Figure 1.3 shows the different types of energy harvesting techniques used in biomedical applications.

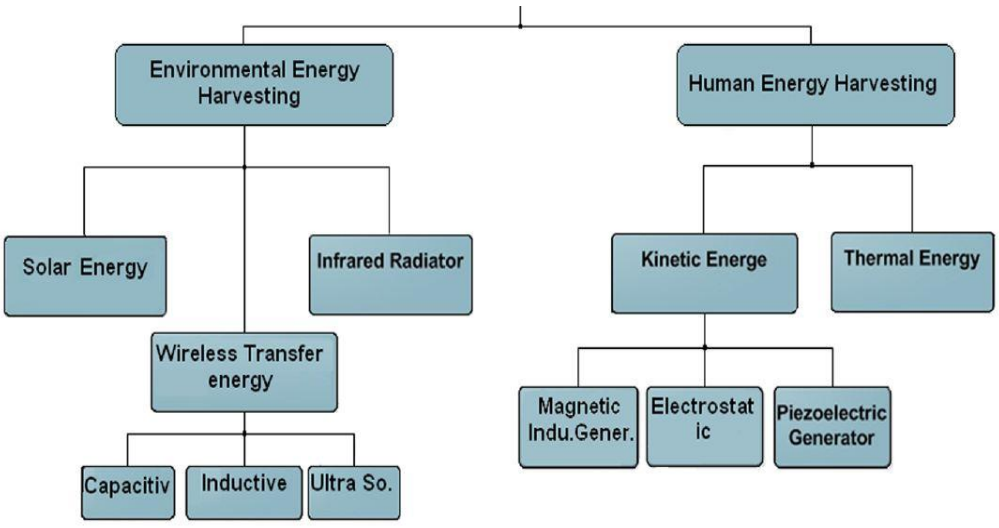


Figure 1.3: Energy harvesting methods used in biomedical applications

Chapter 2 System Overview

2.1 Inductive Link Harvesting System

In this chapter, a 13.56 MHz CMOS near-field inductive link power supply (ILPS) for Implantable medical devices (IMDs) is proposed. IN RECENT years, implantable medical devices (IMDs) have become more and more important in the treatment of intractable diseases or disorders, especially neurological ones. Such neural prosthetic IMDs utilize electrical pulses to stimulate neural cells and restore neural functions. Several examples are cochlear implants, retinal prostheses, and closed-loop epilepsy control.

These IMDs usually have high power consumption greater than several milli Watts. Since they are implanted into the human body, a long-term reliable power supply is required to avoid the frequent surgery for the battery replacement. However, current battery technology cannot sustain for an enough long time. Therefore, wireless power transfer can be a useful solution for IMDs. The near-field inductive energy transfer has become the most widely used method for the neural prosthetic IMDs to recharge the chargeable battery or directly provide the required power from medium to high levels.

A near-field inductive link power supply (ILPS) can be divided into three different parts as: power amplifier, near-field coils, and power regulator. The power amplifier amplifies the RF signal to drive the near-field coils. The near-field coils transmit the RF signal through the skin. The coil size which could be confined by the physical sizes of IMDs is an important design factor that mainly determines both power conversion efficiency (PCE) and maximum transmission distance.

The power regulator which converts the received signal into DC voltage to supply the IMD consists of low-dropout regulators (LDOs) and active rectifier or passive rectifier. In the reported CMOS ILPSs, active rectifiers with power MOS devices, comparators and control circuits are adopted to convert AC power into DC power. Since the power MOS devices has both turn-on and turn-off delay times, the comparators should accurately control switch timing to obtain proper forward current conduction and avoid reverse current conduction. Thus the efficiency can be increased.

The demand for low drop-out regulators has been driven by the portable electronics market as well as industrial and automotive applications. Most recently, the increasing demand for portable and battery operated products have forced these circuits to operate under lower voltage conditions. Furthermore, high current efficiency has also become necessary to maximize the lifetime of the battery. Battery life is determined by the total current drain composed of quiescent current and load current. A series low drop-out regulator is a circuit that provides a well specified and stable dc voltage whose input to output voltage is low. The drop-out voltage is

defined as the value of the input/output differential voltage where the control loop stops regulating. The term series comes from the fact that a power transistor (pass transistor) is connected in series between the input and output terminals of the regulator. The operation of the circuit is based on feeding back an error amplifier signal to control the output current flow of the power transistor driving the load. Low drop-out regulators can be categorized as either low power or high power. Low power LDOs are typically those with a maximum output current of less than 1 A, exhibited by most portable applications. On the other hand, high power LDOs can yield currents that are equal to or greater than 1 A to the output, which are commonly demanded by many automotive and industrial applications. They are widely used in present electronic industry, since they are one of the subsystems of the power management unit.

2.2 Thermal Energy Harvesting System

Thermal energy harvesting has many key challenges, its relatively low output power, efficiency, how to deliver maximum power to application load by reducing the amount of dissipated power. This paper is facing these challenges presenting a new approach of control unit technique for Maximum power point tracking of thermal energy harvesting systems. The thermo electric generator (TEG) output is modelled to be 250 mV out from the temperature difference between its layers; Pelliconi charge pump is used to step up the output voltage level of the TEG. The control unit consists of voltage controlled oscillator (VCO) and non-overlapping clock generator. A prototype is implemented using UMC 130nm technology process, where it achieves 61 % power efficiency, with output voltage level approximately 3V at maximum load current 50 uA.

Energy harvesting is collecting ambient energy in different forms i.e. thermal, piezo, solar, etc. Then, the harvested energy is transformed into electrical energy through certain energy transducers, then this electric energy has to been step up to maintain its use, then we need to store these ambient of energy in super capacitor or chargeable battery to meet the application they provided for. The most important part in the design of the system is the part of the design of the maximum power point tracking (MPPT) circuit. In this paper, a new MPPT circuit is proposed to achieve high power efficiency with maximum load current.

This system is composite of voltage source which is the equivalent to TEG, TEG is the device which convert thermal energy to electric energy, the out power level of TEG is proportional to the difference in temperature on its plate, and then this voltage source is being an input to the selected charge (pelliconi charge pump) pump as the power management for the system which need MPPT control unit to operate it, after that the output voltage from charge pump will store in a small battery or a super capacitor then use this stored energy in biomedical devices.

Chapter 3 AC to DC Converter

3.1 Introduction

In this part, we present a fully integrated active voltage doubler in 0.13µm CMOS technology using offset-controlled high speed comparators for extending the range of inductive power transmission to implantable microelectronic devices (IMD) and radio-frequency identification (RFID) tags. This active voltage doubler provides considerably higher power conversion efficiency (PCE) and lower dropout voltage compared to its passive counterpart and requires lower input voltage than active rectifiers, leading to reliable and efficient operation with weakly coupled inductive links.

It is known that the input voltage of a full-wave active rectifier must be larger than its output DC voltage. As compared with that of a full-wave active rectifier, the input voltage of an active voltage doubler rectifier (VD) can be lower than its output DC voltage, leading to more reliable operation in the weakly coupled inductive link environment. The offset-controlled functions in the comparators compensate for turn-on and turn-off delays to not only maximize the forward charging current to the load but also minimize the backward current, optimizing PCE in the high frequency (HF) band.

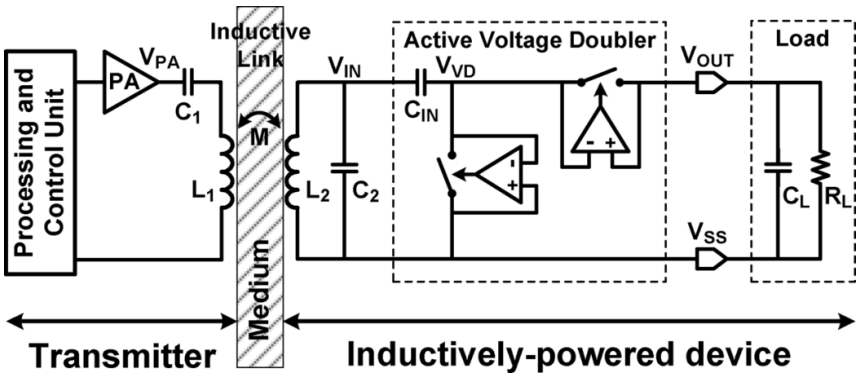


Figure 3.1: Block diagram of an inductively-powered device (e.g., an IMD) with emphasis on the inductive power transmission through the proposed active voltage doubler

Fig. 3.1 shows the block diagram of an inductively-powered IMD with emphasis on the inductive power transmission that consists of three main components: power transmitter (Tx), inductive link, and IMD (Rx). On the Tx side, the primary coil,L_1, is driven by a power amplifier (PA) at the carrier frequency,f_c . This signal induces power in the secondary coil,L_2, and the active voltage doubler converts the AC voltage in tank $L_2\ C_2$ to a DC voltage (V_{out}) at higher levels than the peak input voltage.

The size of L_2 is significantly constrained when it is meant to be implantable in the human body or embedded in a small RFID tag, resulting in small L_2 value and lowV_{in}. There are also IMDs under development, in which the secondary coil has to be embedded in the stimulator package (e.g., to be injectable) or directly implemented on the backside of the microelectrode array to facilitate the system micro-assembly and packaging by eliminating the flex cable that would otherwise be needed to place L_2 under the skin.

In such cases, the distance between L_1 and L_2 can be considerably larger than the size of L_2, significantly limiting V_{in}. This condition renders even the most efficient rectifiers either ineffective or highly inefficient. A viable solution could be using voltage doublers which can operate at lower $V_{in,peak}$ while providing sufficient V_{out}. This can also increase the read range in the RFID tags that operate in the HF band.

3.2 ACTIVE VOLTAGE DOUBLER ARCHITECTURE

3.2.1 Operating Principle of the Voltage Doubler

Both rectifiers and voltage doublers have been widely used for inductively-powered applications. Passive rectifiers and voltage doublers using diode-connected transistors suffer from large forward voltage drops and power losses because of their threshold voltages.

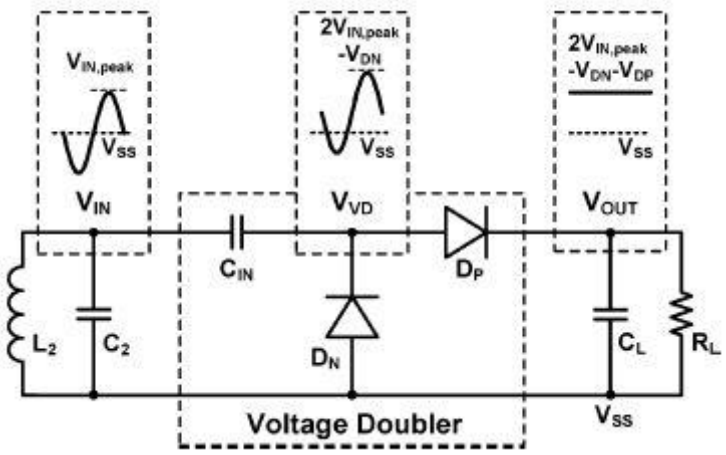


Figure 3.2: Schematic diagram of the passive voltage doubler using diodes or diode connected Transistors

Fig. 3.2 shows the topology of the conventional passive voltage doubler using either diodes or diode-connected transistors. It consists of one capacitor,C_{IN}, and two diodes,D_N and D_P, with forward dropout voltages of V_{DN} and V_{DP}, respectively. Rectified output voltage, V_{out}, is low pass filtered by C_L, and supplies the load resistor, R_L. The sinusoidal input voltage, V_{IN}, generated across the secondary resonance circuit, L_2C_2, has a peak amplitude of $V_{in,peak}$, which depends on the inductive link parameters and V_{PA} at the output of the power amplifier (PA), shown in Fig. 3.1.

When V_{IN} goes below $-V_{DN}$, V_{VD} is connected to V_{SS} through D_N, and C_{IN} is charged to $V_{in,peak} - V_{DN}$, with V_{VD} as the positive node. When V_{IN} increases above $-V_{in,peak}$, D_N turns off again and the isolated V_{VD} increases by the following $V_{in,peak} - V_{DN} + V_{IN}$. When $V_{VD} > V_{out} + V_{DP}$, D_P turns on and current flow from V_{IN} to V_{out} to charge $R_L C_L$ load. In this step, the charge stored in C_{IN} decreases by the amount of charge delivered to the load, but C_{IN} is charged again to $V_{in,peak} - V_{DN}$ in the next cycle. Due to the dropout voltage across D_P, V_{out} can reach a maximum voltage of $2V_{in,peak} - V_{DN} - V_{DP}$, The total dropout voltage of the voltage doubler,V_{Drop}, can be calculated from:

$$V_{Drop} = 2V_{in,peak} - V_{out} = V_{DN} + V_{DP}$$

This equation shows that the diode dropout voltages, V_{DN} and V_{DP}, directly affect the voltage doubler output voltage and consequently its PCE. Thus, substituting them with fast MOS switches with low on-resistance and leakage would be an effective way of reducing V_{Drop} and improving the PCE.

3.2.2 Implementation of the Active Voltage Doubler

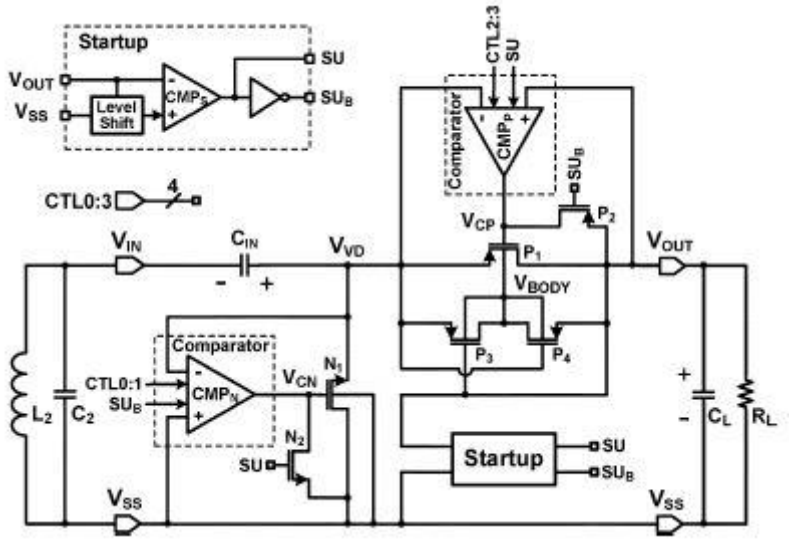


Figure 3.3: Schematic diagram of the proposed active voltage doubler employing high speed offset-controlled comparators,CMP_N and CMP_P, to drive N_1 and P_1 pass transistors, respectively, and achieve higher PCE

Fig. 3.3 shows a simplified schematic diagram of the proposed active voltage doubler, in which two pass transistor switches, N_1 and P_1, are driven by high-speed comparators, CMP_N and CMP_P, respectively. When $V_{VD} < V_{SS}$, CMP_N output goes high, N_1 turns on with a low dropout voltage, $V_{DS(N1)}$, and C_{IN} is charged to $V_{IN,peak} - V_{DS(N1)}$ in the shown polarity. When $V_{VD} > V_{out}$, CMP_P output goes low, P_1 turns on with a low dropout voltage, $V_{SD(P1)}$, and current flows through P_1 to charge $R_L C_L$ in the shown polarity. Therefore, after a few cycles, V_{out} is charged up

to $2V_{IN,peak} - V_{DS(N1)} - V_{SD(P1)}$ and the total dropout voltage, $V_{Drop} = V_{DS(N1)} + V_{SD(P1)}$ which results from the instantaneous input current flowing through the on-resistance of N_1 and P_1, will be much smaller than that of the passive voltage doubler in Fig. 3.2.

To drive N_1 and P_1 at high frequencies in the order of 13.56 MHz, comparators are equipped with internal offset-control functions and four signals (CTL0:3) to reduce the effects of the comparators' delay. These four signals are generated by comparing V_{IN} with 0V. The signals CTL1 and CTL2 are connected to the comparator output and the signals CTL0 and CTL3 are connected to the inversion of the comparator output. The comparator we are talking about here is an ordinary common-gate comparator with +ve terminal connected to V_{IN} and -ve terminal connected to ground.

Also, the separated N-well body terminal of P_1 needs to be connected to the highest potential on the chip to prevent latch-up and substrate leakage problems. Therefore, in Fig. 3.3 we have adopted the dynamic body biasing technique from with auxiliary transistors, P_3 and P_4, automatically connecting to the highest potential between V_{VD} and V_{out}.

Since the comparators are supplied from V_{out}, which is initially at 0 V, it is necessary for the active voltage doubler to have startup capability. The startup block in Fig. 3.3, which will be described later in this part. The startup circuit generates a complementary pair of startup enable signals, SU and SU_B, depending on the V_{out} level to control the startup switches, N_2 and P_2, as well as the comparators. When V_{out} is too lowto operate the comparators, the startup circuit sets $SU = high$ and $SU_B = low$, which turn N_2 and P_2 on, respectively, while disabling the comparators. In this condition, both, N_1 and P_1 are diode-connected to form a passive voltage doubler, which starts charging V_{out} regardless of the comparators' status. When V_{out} exceeds a certain level that is sufficient to operate the comparators, SU and SU_B toggle and turn N_2 and P_2 off, while enabling the comparators to normally run the active voltage doubler.

3.3 CIRCUIT DETAILS AND DESIGN CONSIDERATIONS

3.3.1 Offset-Controlled High Speed Comparator

CMP_N and CMP_P need to drive large gate capacitances of N_1 and P_1 at high frequencies, respectively. Thus, key design parameters are drive capability and short delay. Comparator delay can reduce the PCE by either decreasing the input power that could otherwise be delivered to the load or allowing instantaneous back currents that flow from C_L back to L_2C_2 tank. When $V_{IN} < V_{OUT}$ To reduce such delays, we have designed high-speed comparators with adjustable internal offsets, which basic concept was introduced in. These built-in offset control functions help

comparators turn their pass transistors on and off at proper times, leading to higher PCE.

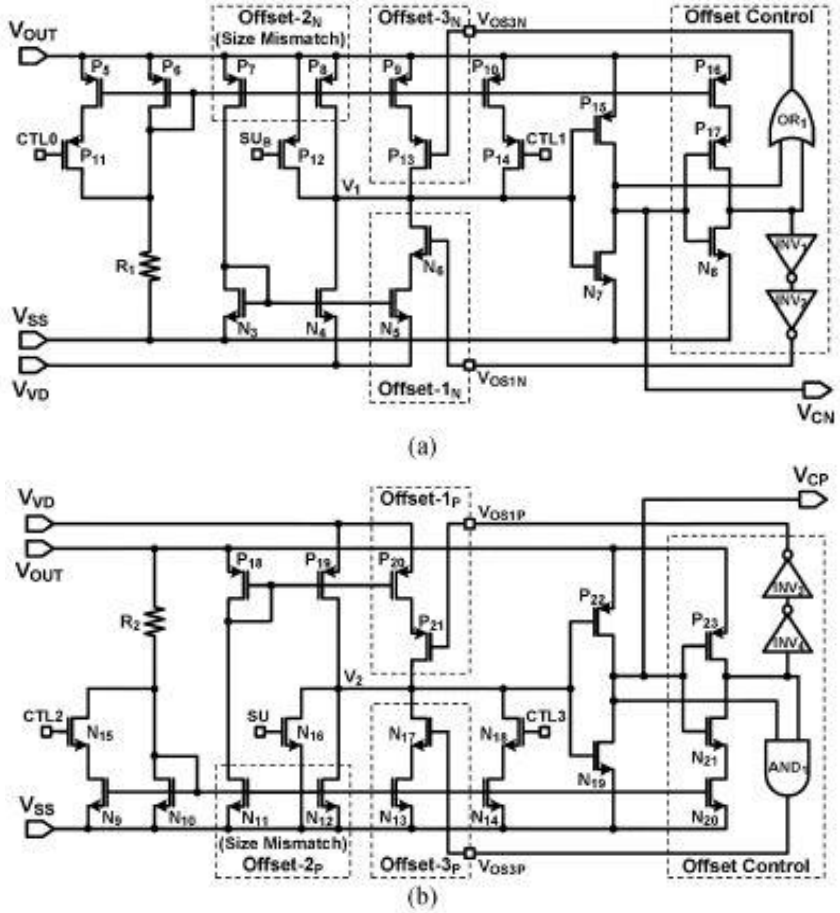


Figure 3.4: Schematic diagram showing three offset-control functions built-in our high speed comparators, (a) $\mathbf{CMP_N}$ and (b) $\mathbf{CMP_P}$ Offset-1 for turn-on delay, Offset-2 for turn-off delay, and Offset-3 for reliable turn-off operation

Fig. 3.4 shows the schematic diagram of two symmetrical high speed comparators, in Fig. 3.4(a) CMP_N and in Fig. 3.4(b) CMP_P, each of which is equipped with three built-in offset-control functions. In Fig. 3.4(a), $P_7 - P_8$, $N_3 - N_4$and $P_{15} - N_7$ form a common gate comparator, which input terminals at the sources of N_3 and N_4 are connected to V_{SS} and V_{VD}, respectively. P_6 and R_1 form a biasing branch, which is mirrored on to P_7 and P_8. Thus, the comparator requires a minimum supply voltage of $V_{TH(P6)}$ in order to start its operation. Since the gate of the diode-connected N_3 is coupled with N_4, currents flowing through N_3 and N_4 depend on their source voltages, V_{SS} and V_{VD}, respectively. When $V_{VD} < V_{SS}$, the current flowing through N_4 tends to be larger than that of N_3, P_7, and P_8. Hence, V_1, the input of the $P_{15} - N_7$ inverter rapidly drops, leading to a high comparator output voltage, V_{CN} , which turns on N_1.

We added Offset-1_N and Offset-2_N inside CMP_N (and their duals in CMP_P) in order to compensate for the turn-on and turn-off delays, respectively. Offset-1_N block is implemented using current source N_5, controlled by switch N_6, which can pull additional offset current from CMP_N output branch, leading, V_1 to start dropping earlier when this offset mechanism is activated by $V_{OS-1N} = high$. Constant Offset-

2_N has been implemented using the size mismatch between $P_7 - P_8$, the larger W/L ratio of P_8 pushes additional offset current into the comparator output branch to increase, V_1 early.

The offset control signal, V_{OS-1N}, is provided by an offset control block that consists of the current-starved inverter, $P_{16} - P_{17} - N_8$, and other logic gates in Fig. 3.4(a). when $V_{VD} > V_{SS}$, $V_{CN} = low$, and $V_{OS-1N} = high$. Thus, N_6 turns N_5 on to pull offset current in parallel with N_4 at a level that is higher than the additional current that is pushed in P_8 by Offset-2_N. Therefore, V_{CN} starts to increase earlier to turn N_1 on a bit before V_{VD} falls below V_{SS} to compensate for the comparator turn-on delay. Once $V_{CN} = high$, Offset-1_N block turns off, and the offset current pushing through P_8 becomes dominant. As a result, V_{CN} starts to decrease earlier to turn N_1 off a bit before V_{VD} exceeds V_{SS} to compensate for the comparator turn-off delay.

Sudden variations in V_{VD} may occur with rapid changes in the forward current due to interconnect parasitic inductance between L_2C_2 tank and the voltage doubler. These variations may disrupt proper switching of the pass transistors and should be avoided. To protect the comparators against such effects, we have added a 3rd offset branch, Offset-3_N. which consists of P_9 current source, controlled by P_{13} switch. When V_{CN} goes low, it takes a while before the current-starved inverter output goes high. During this time, $V_{OS-3N} = low$, activating the Offset-3_N branch to inject additional current into V_1 node and prevent V_{CN} from undesired changes due to V_{VD} variations. This will keep N_1 off until the next carrier cycle.

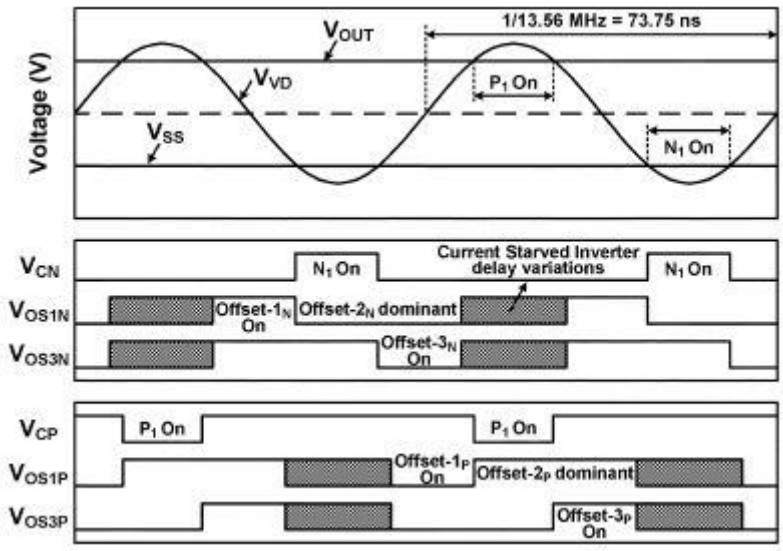


Figure 3.5: Timing diagram showing the relationship between the operating voltages of the active voltage doubler and the offset control signals of each comparator

Fig. 3.5 shows the timing relationship between the input, output, and comparator voltages of the voltage doubler and the offset control signals of each comparator. All transitions of the offset control signals occur fast with negligible rising and falling times.

3.3.2 Self-Startup Capability

The active voltage doubler is cable of starting up before its supply rail, V_{OUT}, is charged up to the level that is needed for the comparators to operate.

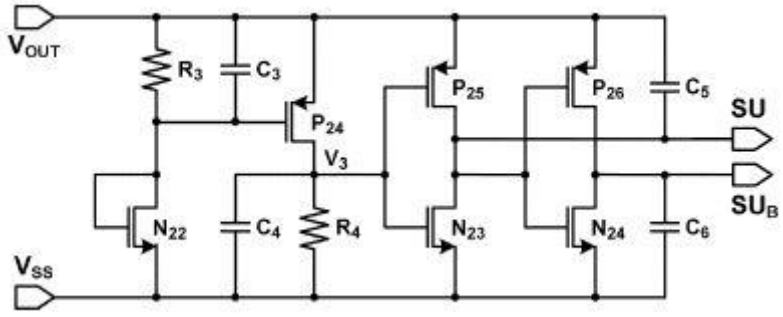


Figure 3.6: Schematic diagram of the startup circuit, which generates the startup enable signals, SU and SU_B

The startup circuit in Fig. 3.6 reconfigures the doubler circuit as a diode-connected passive voltage doubler by generating SU and SU_B signals based on V_{out}. When $V_{out} = 0V$ comparator outputs, V_{CN} and V_{CP}, in Fig. 3.3, are also at 0 V. In this condition, N_1 and P_1 are diode-connected and conduct when $V_{VD} > V_{TH(P1)}$ and $V_{VD} < -V_{TH(N1)}$, respectively, and V_{OUT} starts to charge up.

In fig. 3.6, when $V_{OUT} < V_{TH(N22)} + V_{TH(P24)}$, P_{24} stays off and V_3 remains 0V through R_4. SU and SU_B follow V_{OUT} and V_{SS} and result in N_1 and P_1 to stay diode-connected. During the same period, N_{16} and P_{12} in Fig. 3.4(a) and (b) force V_{CN} and V_{CP} to be low and high, respectively, further supporting N_1 and P_1 to be diode-connected.
when $V_{OUT} > V_{TH(N22)} + V_{TH(P24)}$ N_{22} turns on creating sufficient voltage across R_3 to turn on P_{24} and pull V_3 up. This, SU and SU_B become V_{SS} and V_{OUT}, respectively, turning N_2 and P_2 off releasing the comparator outputs, and allowing N_1 and P_1 operate as switches.

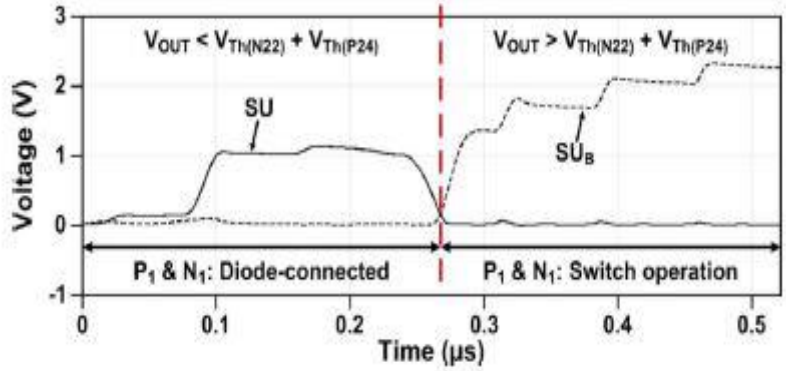


Figure 3.7: Shows the simulated waveforms for the self-startup process of the active voltage doubler SU and SU_B

3.4 SIMULATION AND MEASUREMENT RESULTS

Fig. 3.8 shows the measured output waveform of the active voltage doubler under the condition of $V_{IN,peak} = 2V$, getting an output voltage level equals 3.379V, @ $R_L = 1K\Omega$, $C_{IN} = C_L = 1\mu F$, and $f_c = 13.56\ MHz$.

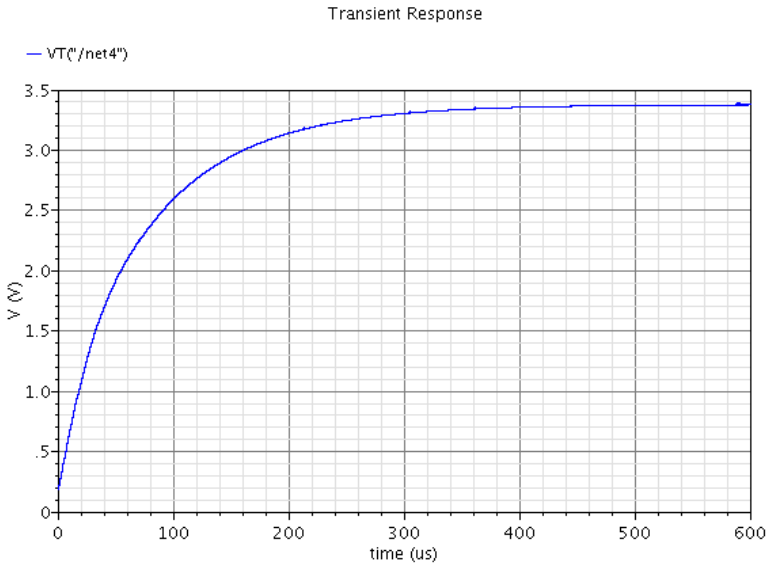


Figure 3.8: Simulated waveform of the output node of the active voltage doubler for $\mathbf{R_L = 1K\Omega}$, $\mathbf{C_{IN} = C_L = 1\mu F}$, and $\mathbf{f_c = 13.56\ MHz}$.

In fig. 3.9 measured waveforms of key nodes in the active voltage doubler, showing V_{VD}, V_{CN}, and V_{CP}, which are the sine wave that enters both comparators at frequency 13.56 MHz, the output signal of the CMP_N that drives the large gate capacitance of the N_1 pass transistor, the output signal of the CMP_P that drives the large gate capacitance of the P_1 pass transistor.

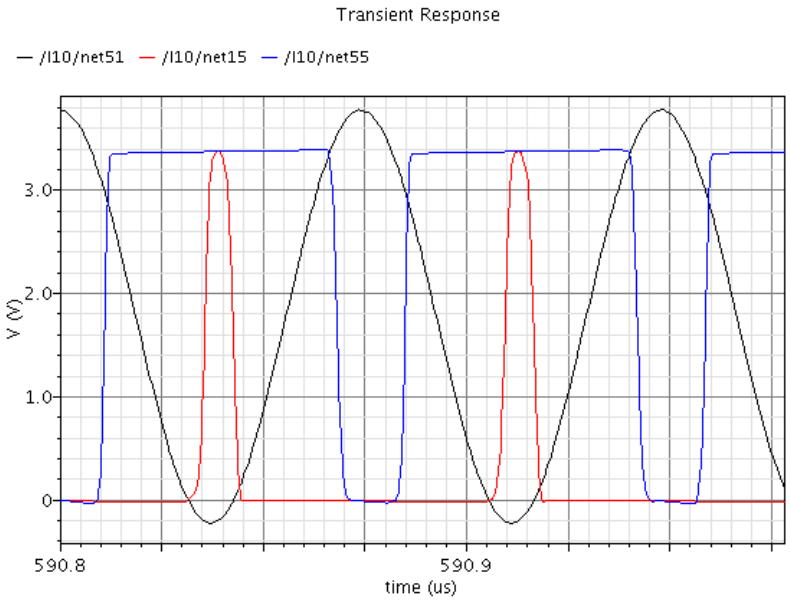


Figure 3.9: measured waveforms of key nodes in the active voltage doubler, showing $\mathbf{V_{VD}}$, $\mathbf{V_{CN}}$, and $\mathbf{V_{CP}}$

$-V_{VD}$ $-V_{CN}$ $-V_{CP}$

The most important issue we have here is the power consumption, as the presence of the comparators, which are very hungry for power. So the resistance of the biasing branch R_1 and R_2 in CMP_N and CMP_P, respectively, is increased to $100\ K\Omega$. In order to suffocate the current entering the common-gate topology and do not mess with the operating point of the transistor. Also, the two resistances $R_3$and R_4 in the start-up circuit are placed with a value of $1M\Omega$. In order to reduce the static power consumption.

The power consumption of each relevant component in the circuit like the two comparators CMP_N and CMP_P, the two pass transistors switching power:

$$P_{Tr,sw} = W_P * C_{gp} * {V^2}_{OUT} * f_c + W_n * C_{gn} * {V^2}_{OUT} * f_c$$
$$= 0.0225 * 10^{-6} + 0.0185 * 10^{-6}$$
$$= 0.041 * 10^{-6}\ watts$$

Which is neglected.

P_{CMP} is obtained from the simulator to be:

$$P_{CMP_N} = 0.6\ mwatts$$
$$P_{CMP_P} = 0.5\ mwatts$$

The total input power is $15.52\ mwatts$.
With the output power equals $11.42\ mwatts$.
Therefore,

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{11.42}{15.52} = 75\%$$

3.5 LAYOUT

Since, the pass transistors have a relatively large widths compared with the remaining transistors in the whole schematic. Its layout will be a bit different, it has to be divided into multipliers and fingers, in order to match the design response and reduce the wasted area through the whole layout. The widths of the pass transistors are $350\ \mu m$, it is divided into 12 multipliers, each multiplier has 12 fingers, each finger has $2.4\ \mu m$ width per finger.

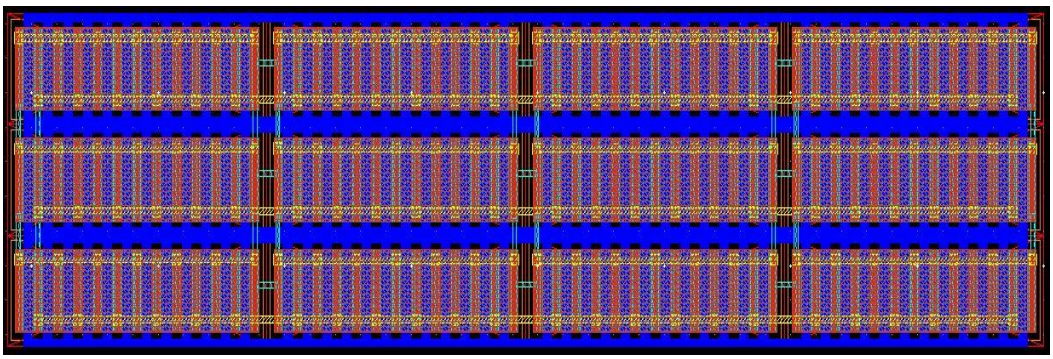


Figure 3.10: The layout of the N_1 pass transistor

Fig. 3.10 shows the complete layout of the N_1 pass transistor with the complete interconnection between the gates, sources, and drains of the 12 multipliers.

Fig. 3.11 shows the complete layout of the P_1 pass transistor with the complete interconnection between the gates, sources, and drains of the 12 multipliers.

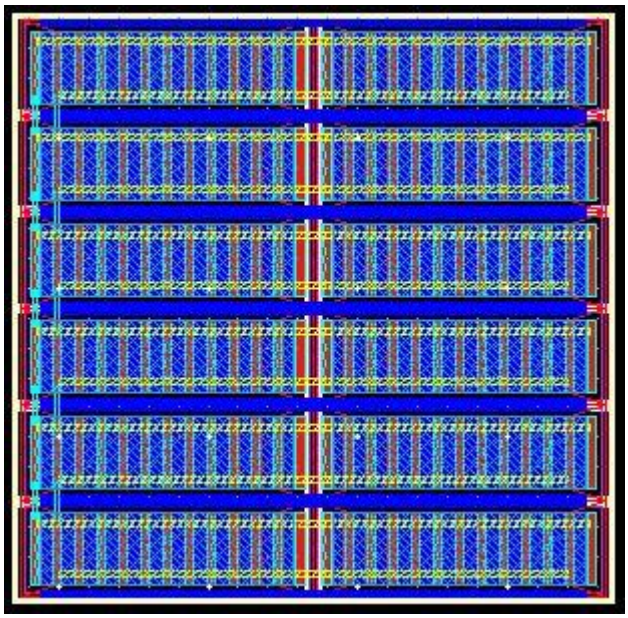


Figure 3.11: The layout of the $\mathbf{P_1}$ pass transistor

With the presence of four control signals CTL0:3, these signals are generated from comparing the input AC voltage (for example: sine wave) with the ground. So, we used an ordinary common-gate topology to implement the comparator and its layout will be presented by fig. 3.12.

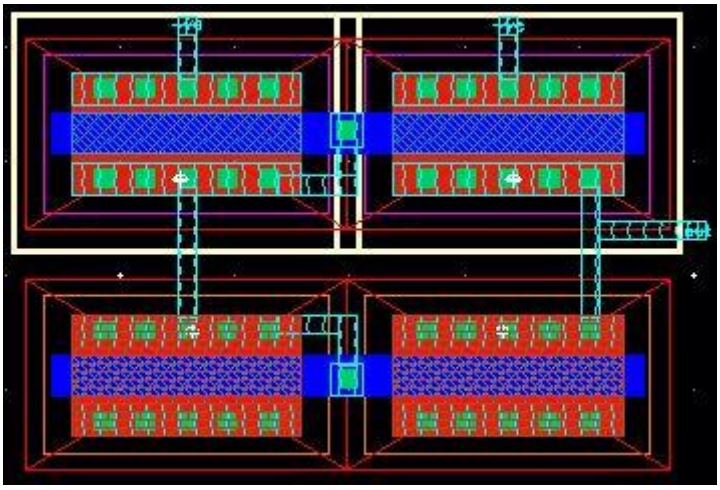


Figure 3.12: The layout of the common-gate comparator

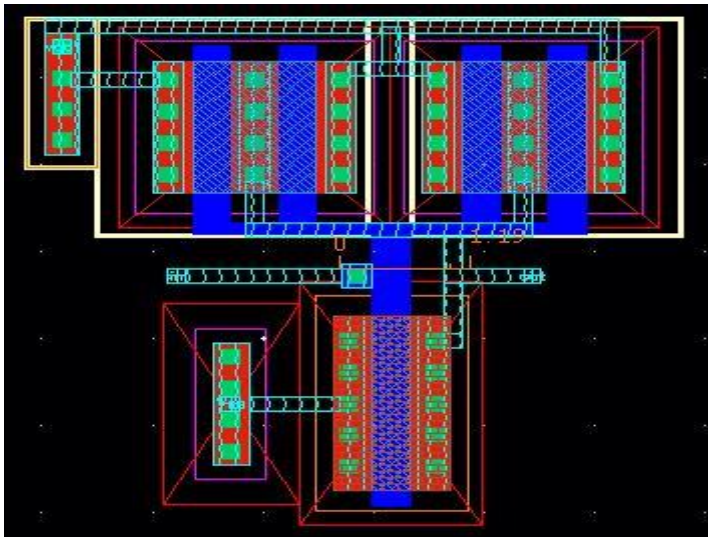
The two resistances in the start-up have a very large value, so, to match it. There is a configuration of:

A A B B A A

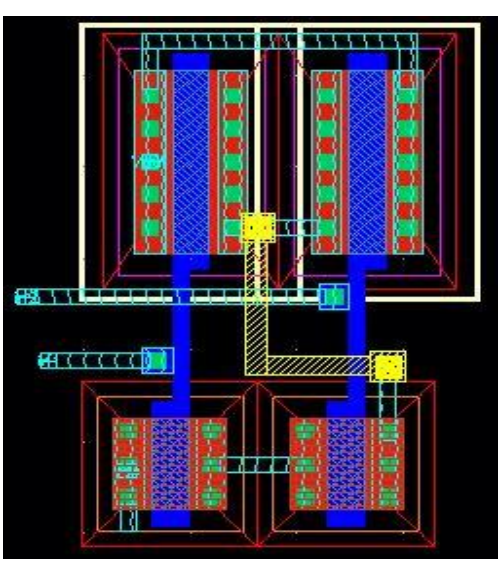
B B A A B B

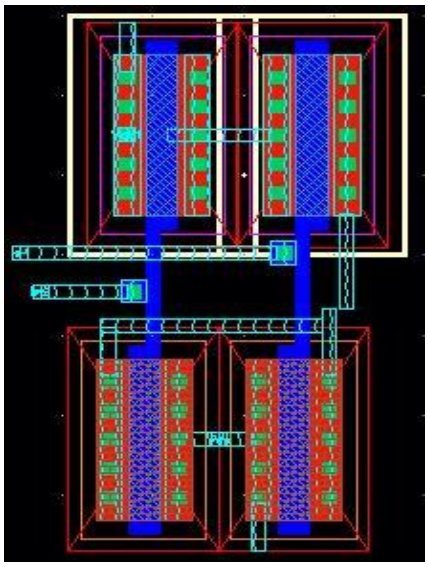
A A B B A A

The last part of the layout was the comparators, the logic gates used in compensating the turn-on and turn-off delays in Offset-1_N, Offset-2_N, and Offset-3_N. As shown in fig. 3.13.



(a)





(b) **(c)**

Figure 3.13: The layout of the logic gates used in the high speed comparators: (a) inverter, (b) NAND, and (c) NOR

Chapter 4 LDO

4.1 Block Level configuration

A linear regulator mainly consists of a control loop which senses the output voltage and maintains a constant output voltage within a specific tolerance regardless of its operating conditions. Figure 4.1 illustrates the conventional LDO architecture. The circuit comprises of a voltage reference, an error amplifier, a power transistor and a feedback network.

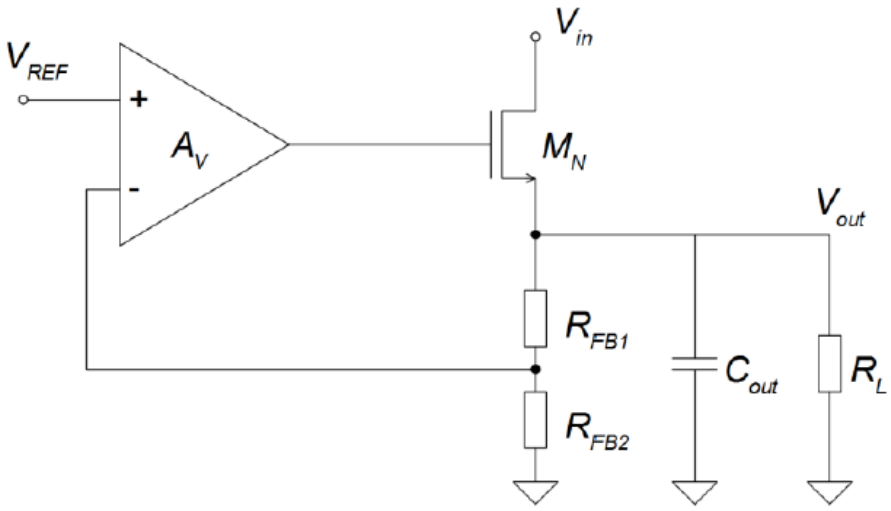


Figure 4.1: The conventional LDO architecture

The feedback network senses the output voltage, delivering a fraction of it to the error amplifier input. The error amplifier compares the voltage sample to the reference and generates an error signal which is used to drive the gate of the power transistor. The output voltage of the regulator is determined by the reference voltage and the ratio of the output resistors R_{FB1} &R_{FB2} as

$$\mathbf{V_{out} = (1+ \frac{RFB1}{RFB2}) VREF},$$

Where V_{REF} is the reference voltage and R_{FB1} &R_{FB2} are the voltage sensing resistors. The physical dimensions of the pass device determine the maximum amount of current which the regulator can source to the load. Since the size of a transistor is directly proportional to the current, the pass device has to be relatively large on order to deliver enough current. The width and length of the channel of a MOS transistor are determined by

$$\mathbf{\frac{W}{L} = \frac{2ID}{\mu n\ Cox\ (VGS - VT)^2}}$$

Where I_D is the drain current, μ_n is the mobility of electrons near the silicon surface, C_{ox} is the oxide capacitance, V_{GS} is the gate to source voltage and V_T is the threshold voltage.

4.2 REGULATION PERFORMANCE

Regulation performance in LDOs is determined by line and load regulation.

i. Load Regulation

Load regulation is a defined as the capability of the regulator to maintain output voltage with varying DC changes in load current.

$$L_R = \frac{\Delta Vout}{\Delta Iload} = \frac{Ro-pass}{1+AOL\beta.} \quad \rightarrow (4.1)$$

Where ΔV_{out} and ΔI_{load} are the changes in output voltage and load current, $R_{o\text{-}pass}$ is the AC output resistance of the pass transistor, A_{OL} is open loop gain of the system and β is the feedback factor.

ii. Line Regulation

Line regulation is a measure of the LDO'S ability to maintain the specified output voltage with varying input voltage. Line regulation is defined as,

$$L_R = \frac{\Delta Vout}{\Delta Vin} \approx \frac{1}{gmn*ro-n*(AV*\frac{RFB2}{RFB1+RFB2})}, \rightarrow (4.2), \text{Apt} = g_m r_{op}$$

Where A_{EA} is the gain of the error amplifier, g_m and $r_{o\text{-}pass}$ are the transconductance and output resistance respectively of pass element and β is the result of voltage divider feedback network.

4.3 POWER SUPPLY REJECTION RATIO (PSRR)

PSRR is defined as the linear regulator's ability to eliminate output ripple caused by input variations. Therefore, PSRR is strongly related to line regulation. The difference between the two is that line regulation specifies only the DC variation while PSRR is specified on wide range of frequencies. PSRR can be defined as the complement of supply injection, or correspondingly as the reciprocal of supply gain A_{in}. The supply gain refers to the small signal variation in output voltage caused by small signal changes in input supply. It is defined as, PSRR=$1/A_{in} = \partial V_{in}/\partial V_{out}$, where A_{in} is the supply gain, ∂V_{in} and ∂V_{out} are the small signal changes in input and output voltages. PSRR of LDO essentially depends on the open loop gain and bandwidth of the regulator. Good PSRR characteristics require a wide bandwidth because PSRR decreases as the frequency response rolls off. Also, signal paths from the supply to the output of the error amplifier should be minimized since AC variation at the gate

of the pass device is directly seen in the output voltage. The PSRR of a linear regulator is determined by three factors:

I. The PSRR of the band gap voltage reference, whose output ripple affects the output ripple of the linear regulator up to the roll-off frequency of the band gap.

II. The open loop gain of the feedback loop(Av),which is roughly equal to the open loop gain of the error amplifier, up to 0dB(unity gain)crossover frequency of the linear regulator.

III. The open loop gain from Vin to Vout (Avo), which is determined by the parasitic parameters of the pass element and values of external components (especially the output capacitor) along the Vin to Vout path, from 0dB crossover frequency (GBW) .High PSRR values are desirable over the frequency range that is critical to the linear regulator, typically 10HZ to 10MHZ.Mathematically, PSRR is the reverse gain of the output ripple over the input ripple at a particular frequency. For LDO'S, specifically, the PSRR is given as:
PSRR (dB) =20log (lAv/Avo), where Av is the open loop gain of the feedback loop, and Avo is the gain from VIN to Vout when feedback loop is open. To achieve the required PSRR, we use RC filter as shown in the below figure.

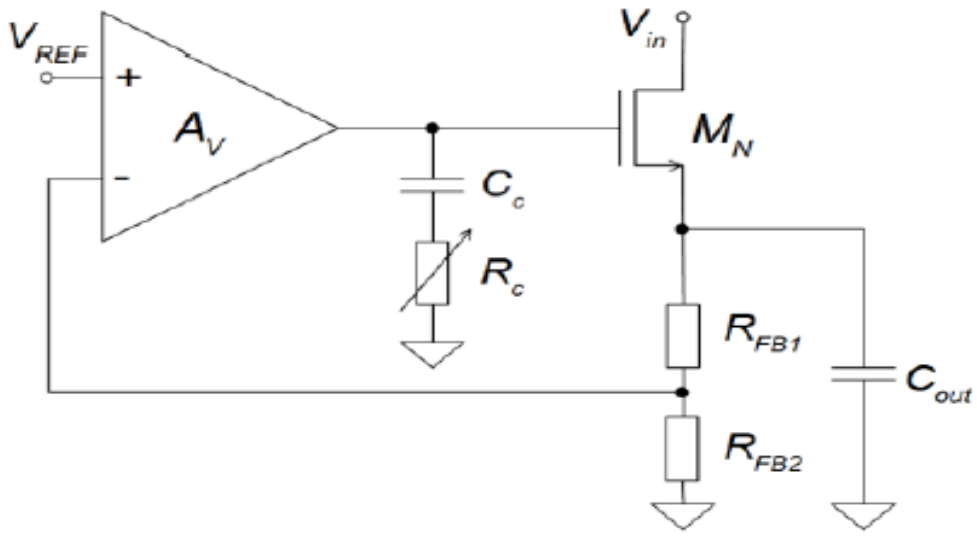


Figure 4.2: LDO compensation method to improve PSRR

4.4 STABILITY

First we will get poles and zeros of LDO to see stability of LDO. For the below figure, we get poles and zeros. The dominant pole of the system is associated with the high impedance output node of the error amplifier.

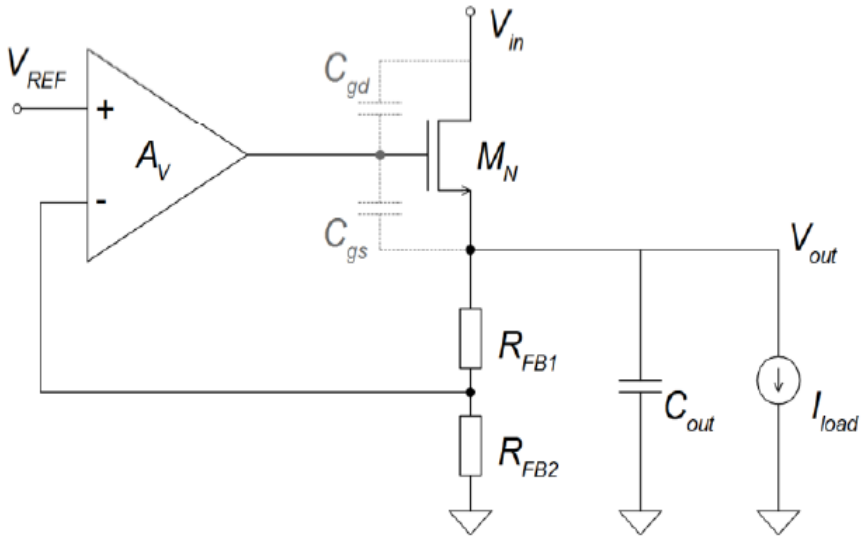


Figure 4.3: NMOS regulator in loading conditions

$$\mathbf{Fp1} = \frac{\mathbf{1}}{\mathbf{2\pi Ro,ea\ Cpar}}$$

Where $R_{o,ea}$ is the output resistance of error amplifier and C_{par} is the parasitic capacitance at the gate of the power transistor, mostly consisting of the gate-source capacitance C_{GS} of M_N. The second major pole is formed at the output of regulator.

$$\mathbf{F_{p2}} = \frac{\mathbf{gmn}}{\mathbf{2\pi Cout}} = \frac{\sqrt{2\mu nCox\frac{w}{l}ID}}{\mathbf{2\pi Cout}}$$

Where g_{mn} is the transconductance of the pass device and C_{out} is the output capacitance. In addition, the gate-source capacitance of M_N creates a feed-forward zero.

$$\mathbf{F_{z1}} = \frac{\mathbf{gmn}}{\mathbf{2\pi Cgs}} = \frac{\sqrt{2\mu nCox\frac{w}{l}ID}}{\mathbf{2\pi Cgs}}$$

For the above poles and zero the system unstable, so to make it stable we use the following circuit.

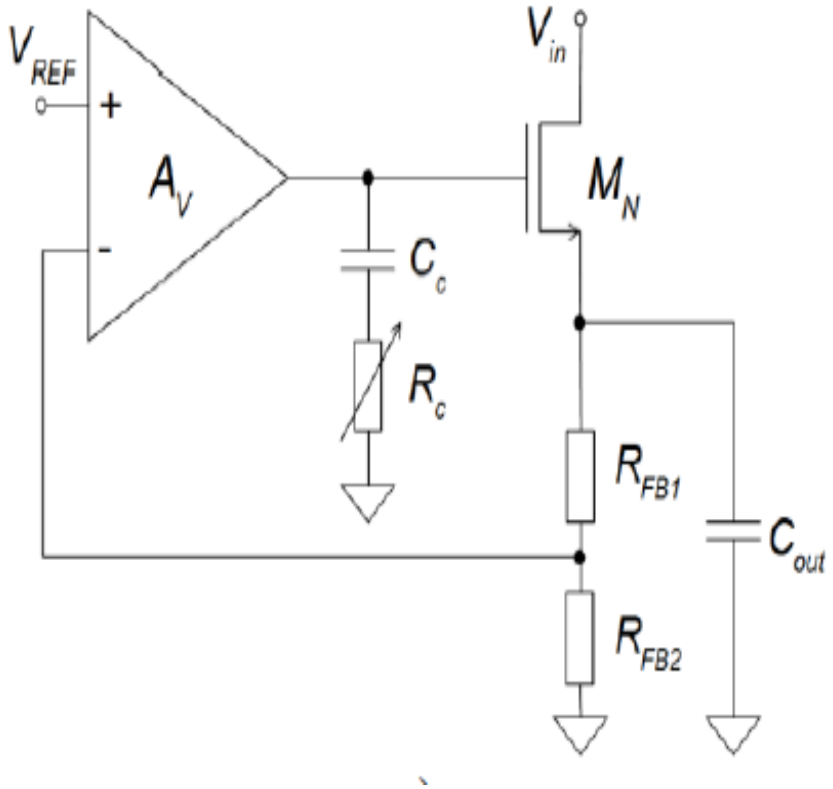


Figure 4.4: LDO compensation method to improve stability

A series RC network is added into the output node of the error amplifier. It essentially creates a zero on a frequency

$$\mathbf{F= \frac{1}{2\pi Rc\ Cc}}$$

Where C_C and R_C are the capacitance and resistance in the compensation network. This compensation network is quite effective if the zero can be made to track the output pole, hence canceling the output pole throughout its movement range. The values of C_c and Rc are 800f F and 500 ohm respectively.

4.5 Pass Transistor

The configuration of the output stage in linear regulators has a significant effect on circuit performance and power efficiency. There are two major topologies used in linear regulators: common-source and common drain configuration.

i. Common drain NMOS pass device

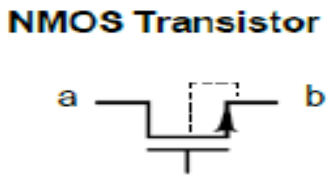


Figure 4.5: Common drain NMOS pass device configuration

The drop-out voltage of common drain NMOS pass device is determined by the below equation. Where drop-out voltage is the minimum voltage across resistor terminals to keep it working properly.

$$V_{D\text{-}O} = V_{sat} + V_{gs}$$

Load regulation is equivalent to the open loop output impedance of the regulator as indicated by equation (4.2). The NMOS LDO has intrinsically higher load regulation characteristics due to the low impedance nature of the source follower. In addition, the feedback loop essentially decreases the output impedance further which results in improved load regulation. Ideally, the output voltage would stay constant regardless of the input but since the loop gain is finite, a change in the input voltage (ΔVin) causes a variation in the output voltage (ΔVout). From the figure (4.1)

$$\frac{\Delta Vout}{\Delta Vin} \approx \frac{1}{gmn * ro{-}n * \left(AV * \frac{RFB2}{RFB1+RFB2}\right)}$$

Where g_{mn} and $r_{o\text{-}n}$ are the transconductance and output resistance of M_N respectively and $(AV * \frac{RFB2}{RFB1+RFB2})$ is the loop gain of the amplifier. This equation also defines the PSRR of a NMOS regulator. The difference is that PSRR is measured over a wide range of frequencies, so the frequency behavior of M_N and the amplifier.

ii. Common source PMOS pass device

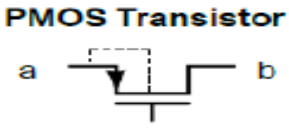


Figure 4.6: Common source PMOS pass device configuration

The drop-out voltage of common drain NMOS pass device is determined by the below equation. Where drop-out voltage is the minimum voltage across resistor terminals to keep it working properly.

$$V_{D\text{-}O} = V_{SD\ (SAT)}$$

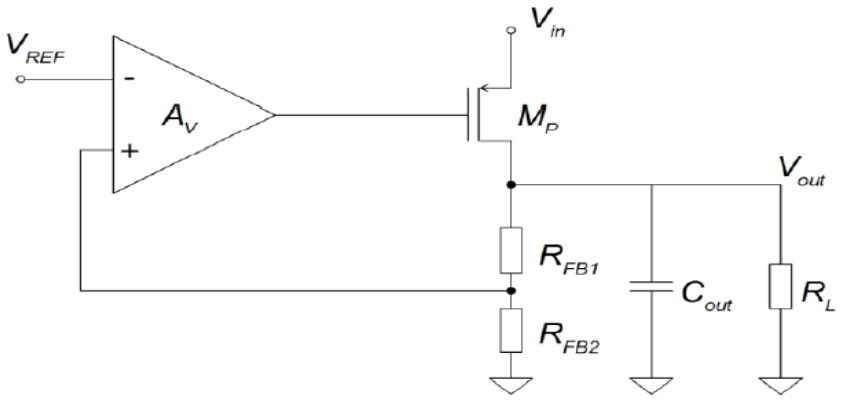


Figure 4.7: PMOS regulator topology

By solving the transfer function for line regulation,

$$\frac{\Delta \mathbf{Vout}}{\Delta \boldsymbol{Vin}} \approx \frac{\mathbf{1}}{(\boldsymbol{AV} * \frac{\boldsymbol{RFB2}}{\boldsymbol{RFB1}+\boldsymbol{RFB2}})}$$

Which implies that line regulation and PSRR is determined only by the loop gain of the amplifier. The most significant drawback for the PMOS topology is the large size of the power transistor. In order to achieve similar performance as the NMOS regulator, M_p has to be roughly two or three times larger due to slower mobility of charge carriers in PMOS transistor.

iii. Comparison of the pass device configuration

Table 4.1: Comparison between pass device configurations

	NMOS	**PMOS**
Dropout voltage	High intrinsically, can be reduced with a charge pump	Low
Open loop output impedance	$\frac{1}{gm}$	r_{ds}
Load regulation	High	Low to medium
Line regulation	High	Inferior
Size	Small	Large

4.6 Error amplifier

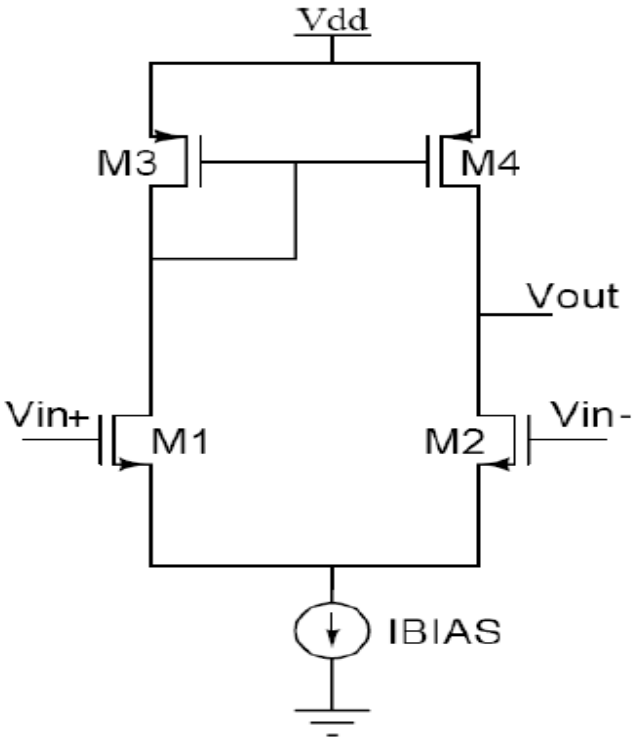


Figure 4.8: Architecture of OTA

Gain of this error amplifier=g_{m2} (r_{o2}//r_{o4}).

4.7 Power Consumption

The actual power consumption across the device can be represented by the following equation.

$$P_C = (I_{DD}-I_L)*V_{DD}$$

Power consumption is 19 µw at load current=1 mA (average current=1.00634mA) and 20 µw at load current=10 mA (average current=10.0063mA) and 20 µw at load current=20 mA (average current=20.0063mA).

4.8 Schematics

i. Schematic of Error Amplifier

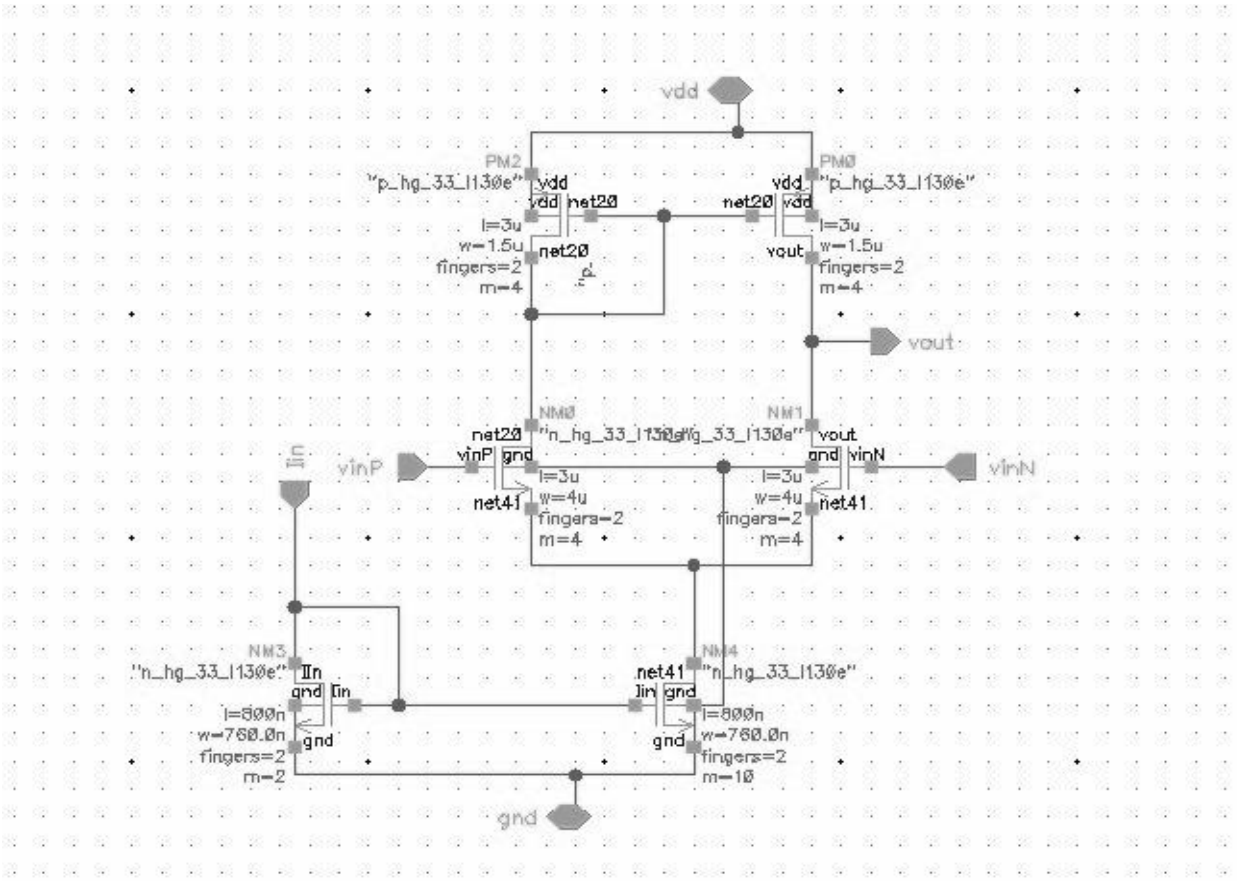


Figure 4.9: Schematic of error amplifier

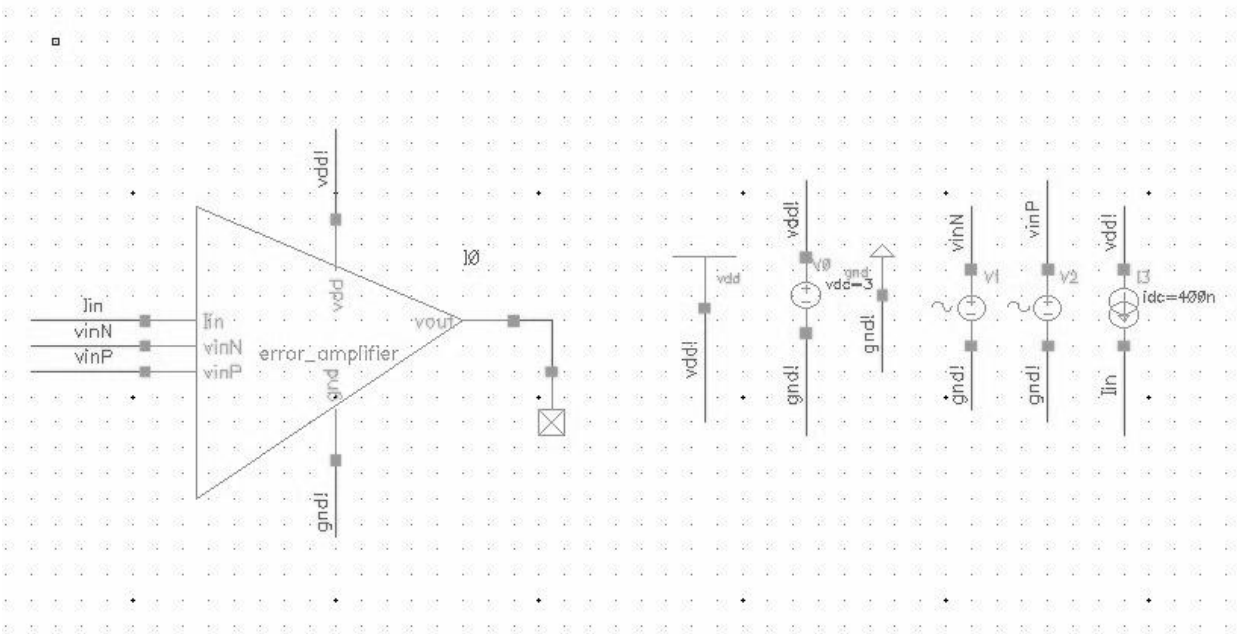


Figure 4.10: Test bench of error amplifier

ii. Schematic of LDO

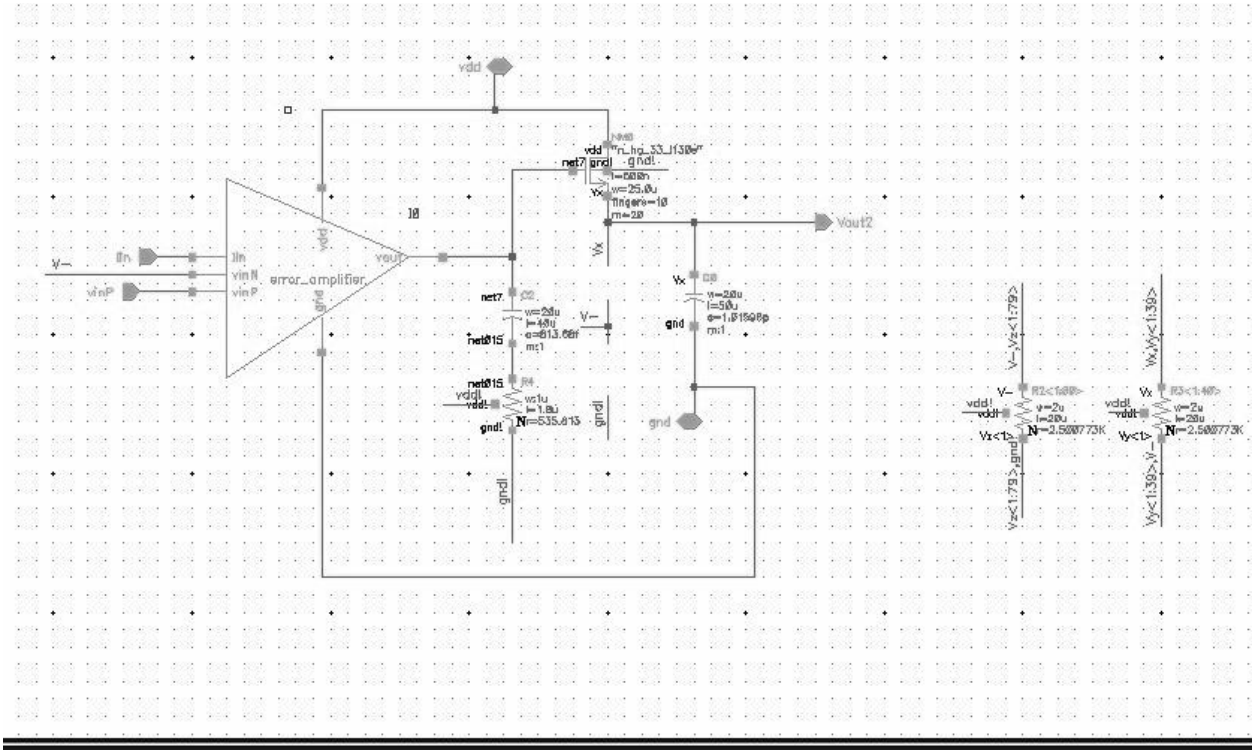


Figure 4.11: Schematic of LDO

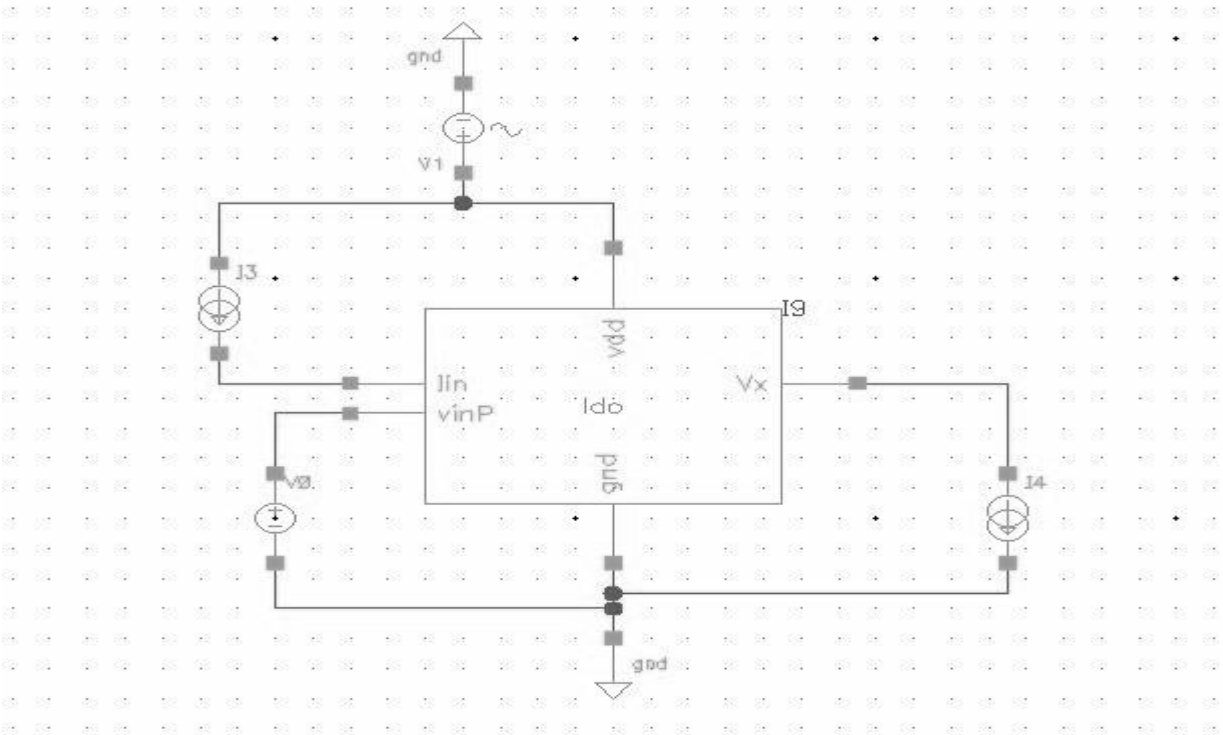


Figure 4.12: Test bench of LDO

We use Ibias=400n and mirror it to 2u, Error amplifier take Iref from band gap circuit and also Low drop-out voltage (LDO) take Vref (800 mV) from band gap circuit.

4.9 SIMULATION AND MEASUREMENT RESULTS

i. Simulation of error amplifier

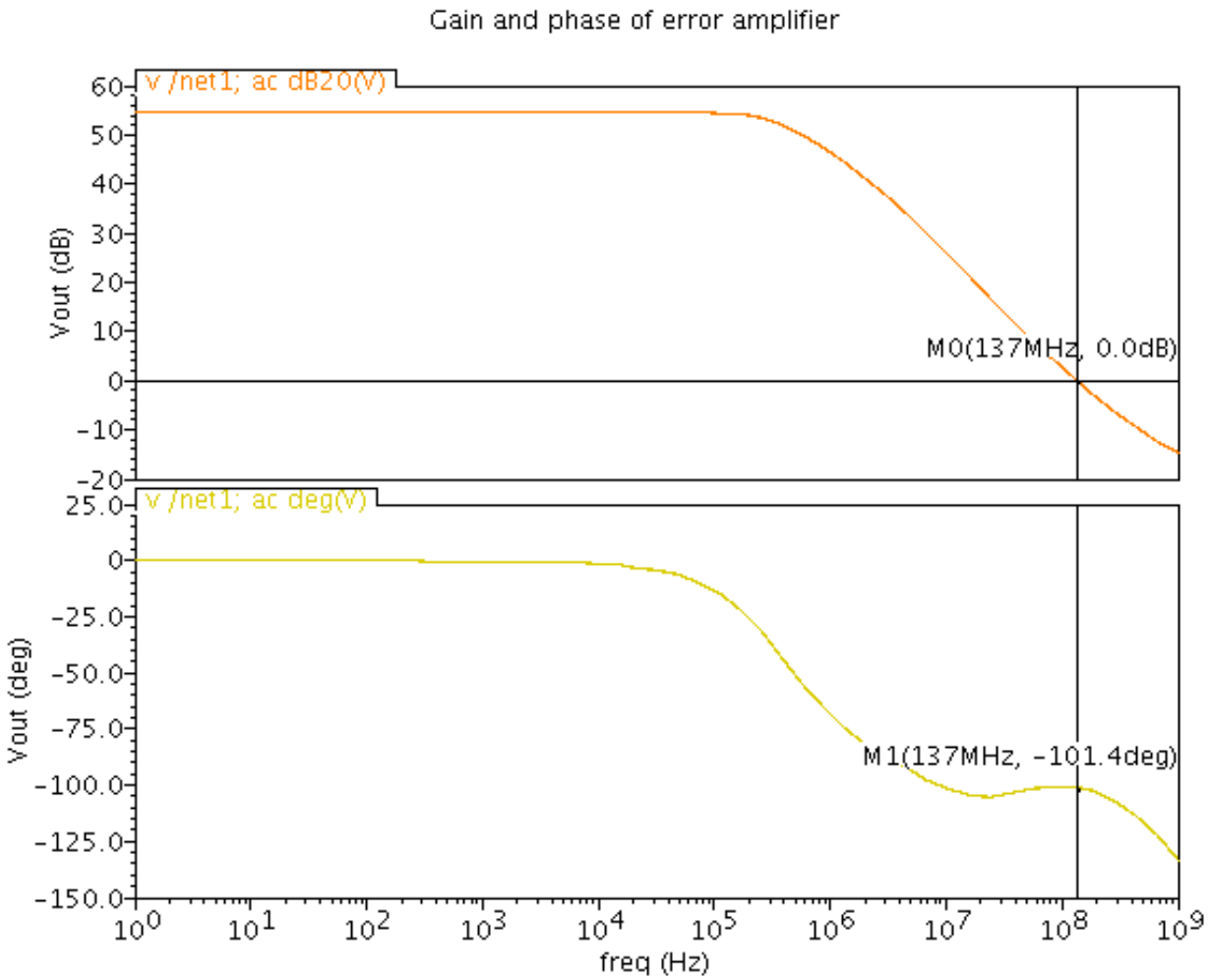


Figure 4.13: Gain and phase response of error amplifier

The above figure shows both gain and phase response of error amplifier. It is shown that gain of EA approximately equals 55db and GBW equals 137 MHz and PM=180-101.4=79.6 db. Definition of PM is, (PM=180+Phase at 0 dB).

ii. Simulation of LDO

- Line Regulation

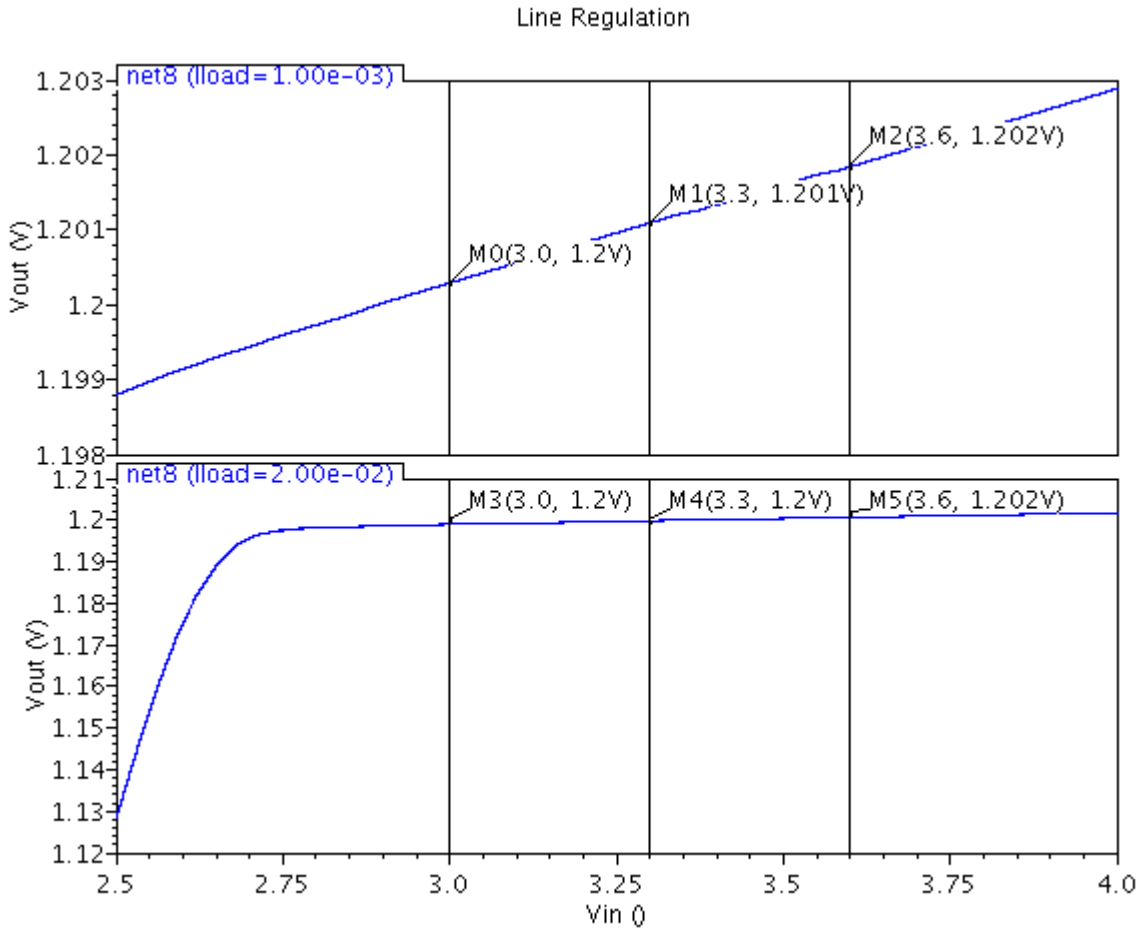


Figure 4.14: Output voltage versus input voltage under load variations

The above figure shows the output voltage of LDO vs. input voltage under load variations. . It is shown that output voltage at load current=1 mA (input voltage=3v) and load current=20 mA (input voltage=3 and 3.3 v) is approximately equal 1.2v. Output voltage at load current=1 mA (input voltage=3.3v) is approximately equal 1.201v. Output voltage at load current=1 mA (input voltage=3.6v) and output voltage at load current=20 mA (input voltage=3v) is approximately equal 1.202v.

- Load Regulation

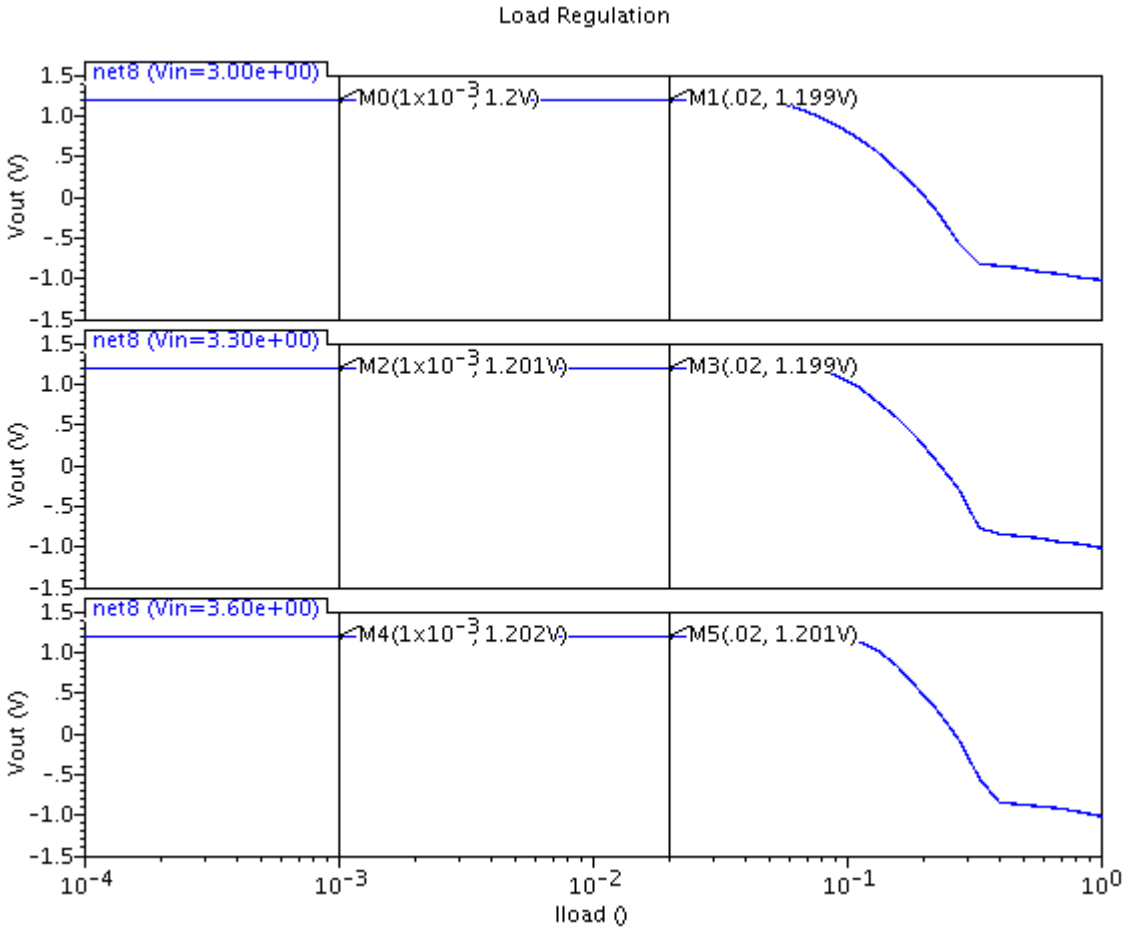


Figure 4.15: Output voltage versus load current

The above figure shows the output voltage of LDO vs. load current under input variations. . It is shown that output voltage at load current=1 mA (input voltage=3v) is approximately equal 1.2 v. Output voltage at load current=1 mA (input voltage=3.3v) and load current=20 mA (input voltage=3.6 v) is approximately equal 1.201v. Output voltage at load current=1 mA (input voltage=3.6v) is approximately equal 1.202 v. And output voltage at load current=20 mA (input voltage=3 and 3.6 v) is approximately equal 1.199v.

- PSRR

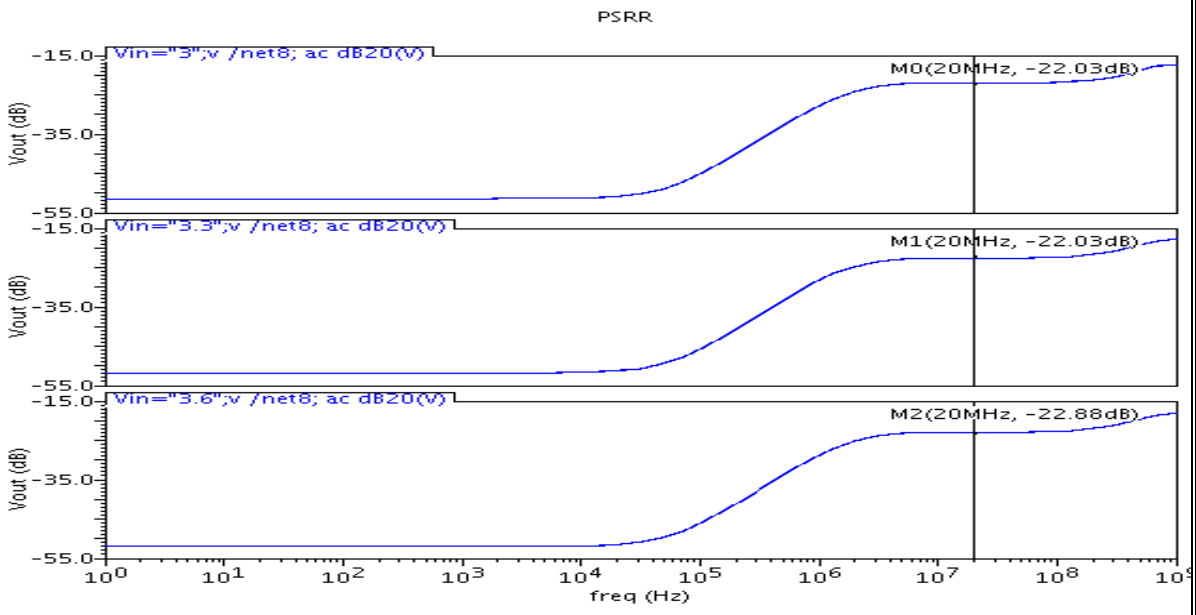


Figure 4.16: Power supply rejection ratio at load current equals 1 mA

The above figure shows the response of power supply rejection ratio at load current equals 1mA. It is shown that PSRR at load current equals 1 mA, input voltage equals 3v and 20 MHz is equal 202.03 db. PSRR at load current equals 1 mA, input voltage equals 3.3v and 20 MHz is equal 22.03 db. PSRR at load current equals 1 mA, input voltage equals 3.6v and 20 MHz is equal 22.88 db.

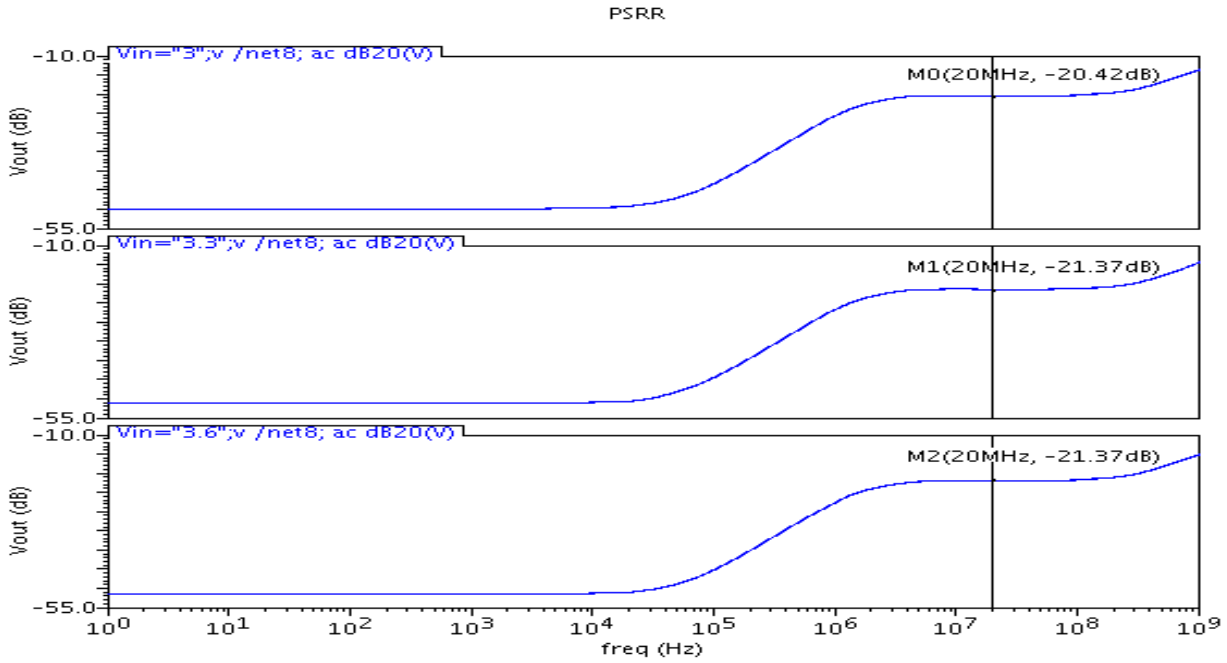


Figure 4.17: Power supply rejection ratio at load current equals 20 mA

The above figure shows the response of power supply rejection ratio at load current equals 20 mA. It is shown that PSRR at load current equals 20 mA, input voltage equals 3v and 20 MHz is equal 20.42 db. PSRR at load current equals 20 mA, input voltage equals 3.3v and 20 MHz is equal 21.37 db. PSRR at load current equals 20mA, input voltage equals 3.6v and 20 MHz is equal 21.37 db.

- Stability

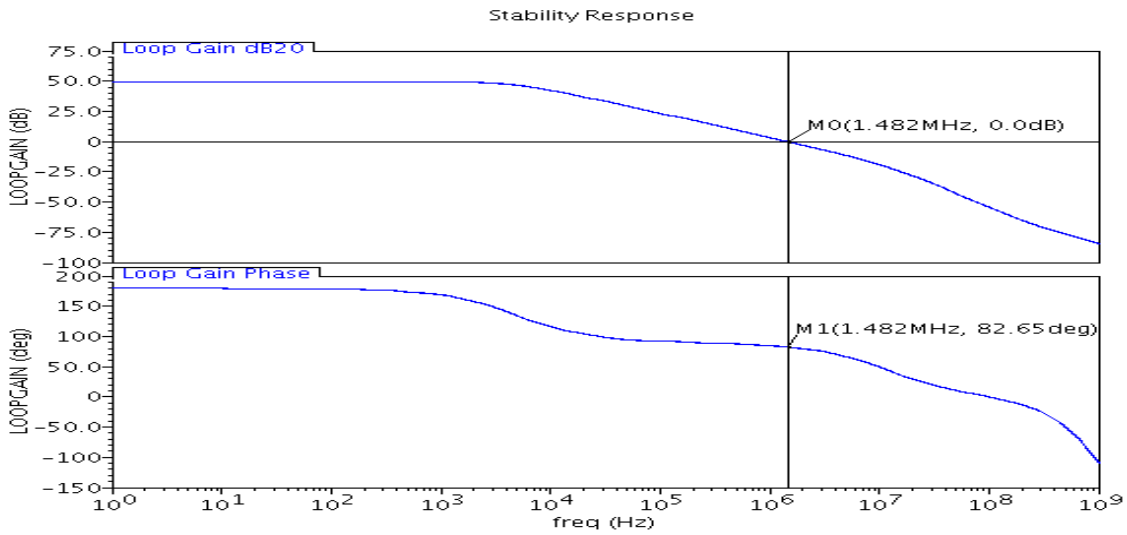


Figure 4.18: Stability response of LDO at load current 1 mA

The above figure shows loop gain of LDO at load current equals 1 mA. It's shown that gain of LDO is approximately 50db, Phase margin equals 82.65db at gain bandwidth equals 1.482MHz.

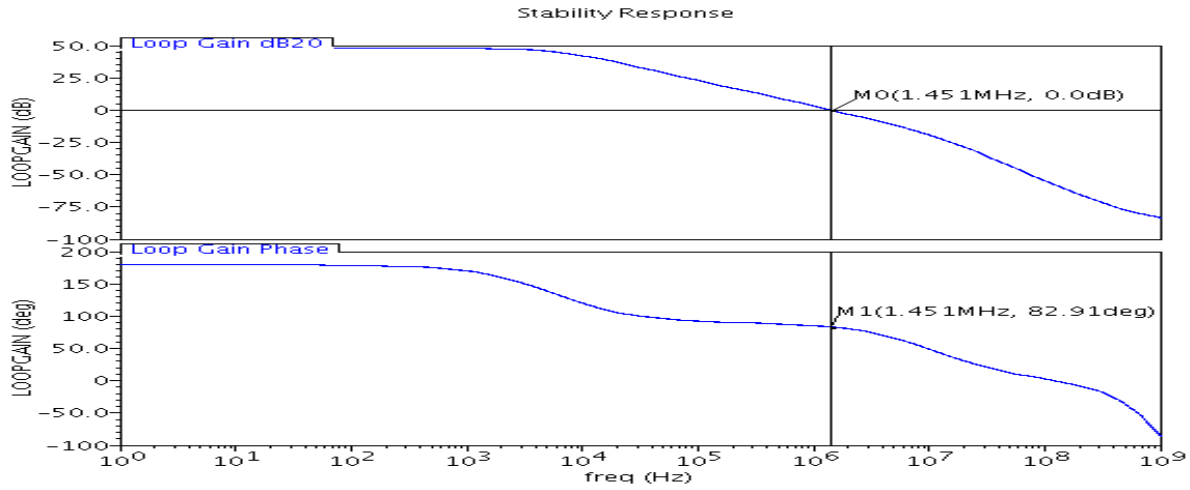


Figure 4.19: Stability response of LDO at load current 20 mA

The above figure shows loop gain of LDO at load current equals 1 mA. It's shown that gain of LDO is approximately 50db, Phase margin equals 82.91db at gain bandwidth equals 1.451MHz.

Table 4.2: Final results of LDO

Specification	Target	Achieved results
Technology process	UMC 130nm	UMC 130nm
Supply voltage variation	+/-10%	3.3 +/-10%
Variations in output voltage	+/-0.5%	Variation in output voltage at load current=1 mA is (1.20029-1.2) 0.029% & Variation in output voltage at load current=20 mA is (1.19903-1.2) -0.097%
PSRR	20 dB at 20 MHz	PSRR=22.03dB (at load=1 mA & Vin=3.3v) PSRR=21.37 dB(at load=20 mA & vin=3.3v)
Load current variation	1mA-20mA	1 mA-20 mA
Load capacitance minimum	1 pF	1 pF
V(reference)	800 mV	800 mV
Output voltage	1.2 v	1.20029 v at load current=1 mA & 1.19903v at load current=20 mA
Loop PM with the supply, and load current	>60 deg	PM>60def for load current variations(1mA-20mA)
Power consumption max	50 uW	20 uW
Resistances	R1=100K ,R2=200K	R1=100K ,R2=200K

4.10 LAYOUT

i. Layout of error amplifier

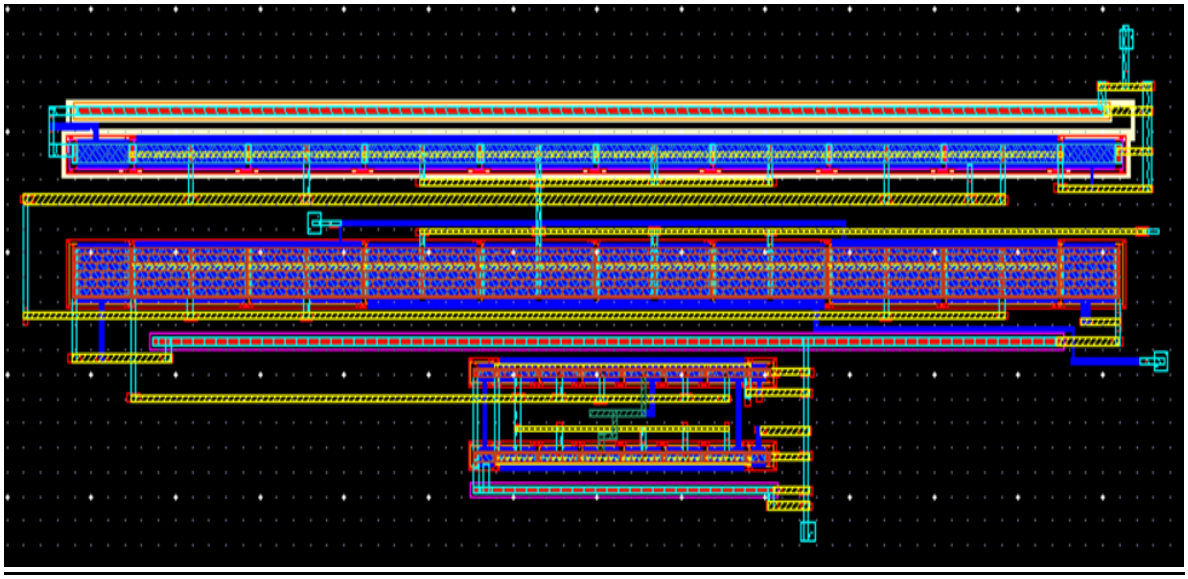


Figure 4.20: Layout of error amplifier

ii. Layout of Pass transistor

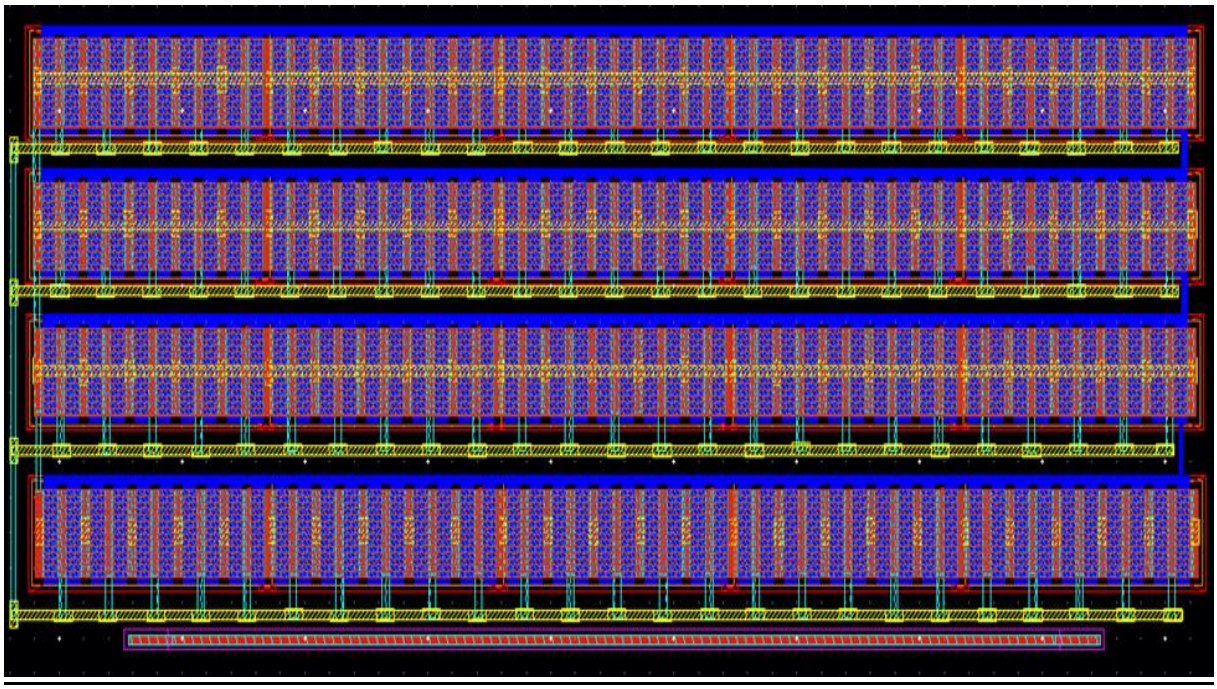


Figure 4.21: Layout of error pass transistor

iii. Layout of LDO

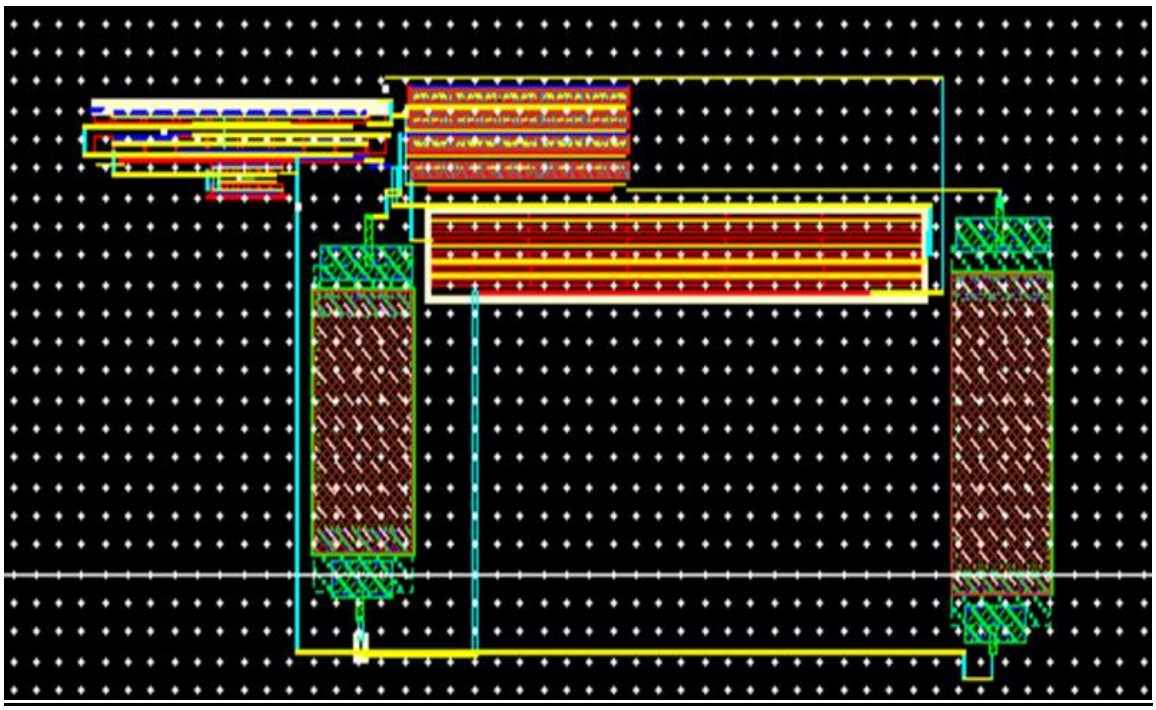


Figure 4.22: Layout of LDO

Chapter 5 BANDGAP REFERENCE CIRCUIT

5.1 Introduction

First of all, we have to look at what voltage references are actually used for. They are used in Analog to-digital converters. They can also be used in both voltage and current regulators. A voltage regulator locks the output voltage to the reference voltage by use of a resistor ratio. Actually it is a two-stage feedback amplifier, with the reference voltage Vref as an input. The first stage is the opamp, whereas the second stage is a source follower. This follower can deliver a large current to the load, depending on its W/L ratio.

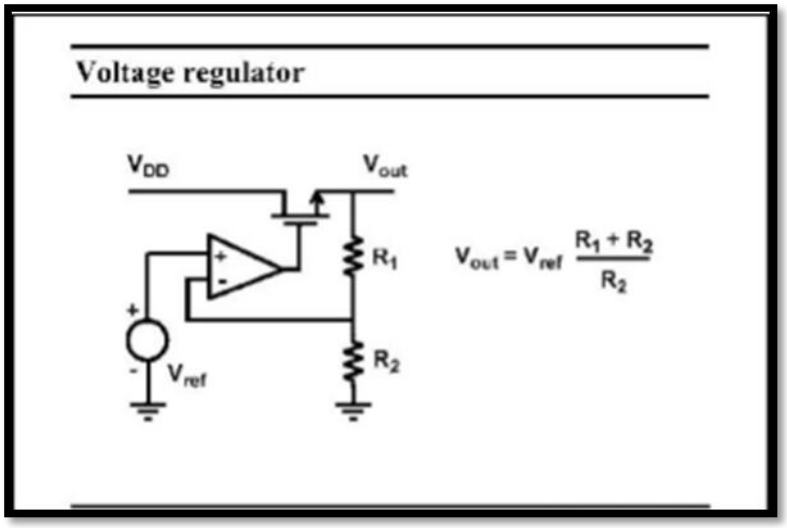


Figure 5.1: The Voltage Regulator

A bandgap voltage reference is a temperature independent voltage reference circuit widely used in integrated circuits. It produces a fixed (constant) voltage regardless of power supply variations, temperature changes and circuit loading from a device.

An accurate voltage or current reference is an important component of most integrated circuits. As its name suggests, a reference establishes a stable point (either a voltage or current) that the rest of the circuits in the system can utilize for generating reliable and predictable results. Whether used with a regulator to build a power-supply , in an operational amplifier to set up a bias point ,or to supply reference voltage for the low dropout voltage (LDOs) ,or in an analog-to-digital converter (ADC) to establish a standard to compare voltages against, the accuracy of the reference directly impacts and often dictates the overall performance of a system.

Since supply voltage is scaling down with the reducing thickness of gate oxide in modem CMOS technology and the increasing demand for low power portable devices, the dynamic range of system is becoming much smaller. Spurious coming from the noisily power supply without adequately rejected will seriously degrade system performances, especially in RF applications. So, LDOs with high accuracy low temperature-coefficient have been used widely in noise sensitive wireless transceivers and ADCs. The power supply rejection (PSR), which is a merit of LDOs' immunity against power spurious, is most important. The maximum achievable PSR of LDOs is mostly limited by the PSR of voltage reference. Thus, the design of low-power low temperature-coefficient high PSR bandgap voltage reference is becoming more and more important.

The bandgap reference circuit has been the most elegant way to fashion an integrated circuit (IC) voltage reference. The circuit operates on the principle of adding a voltage that decreases linearly with temperature to one that increases linearly with temperature to produce a reference voltage that is stable with respect to temperature to the first order. Barring a small curvature, the base-emitter voltage of a bipolar transistor in the active region decreases linearly with temperature, i.e., it has a complementary-to-absolute-temperature (CTAT) dependence. The voltage that increases linearly with temperature, i.e., the proportional-to-absolute-temperature (PTAT) voltage, is produced through the difference in the base-emitter voltages of two bipolar transistors operating under different current densities (a manifestation of the well-known Gilbert principle). A bandgap reference circuit adds these CTAT and PTAT voltages to produce a temperature-independent voltage VREF, as shown in Fig. 5.2. Conventionally, since the CTAT component is generated from a diode or base-emitter voltage.

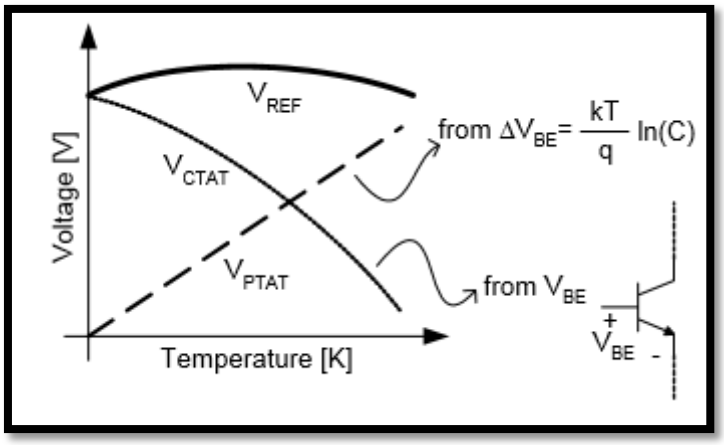


Figure 5.2: Temperature behaviour of a typical bandgap reference circuit

The reason for this is that the diode voltage has various temperature dependent terms and its zero-order or temperature-independent component is the bandgap voltage.

5.2 Bandgap Voltage Reference Principles

The principle of the bandgap voltage reference is to balance the negative temperature coefficient of a pn junction with the positive temperature coefficient. The physics of a bipolar transistor is reviewed to examine where the absolute accuracy and temperature coefficient are coming from. A correction circuit is added to equalize the output voltage over temperature. For a constant current, the voltage VBE across the diode-connected transistor decreases with temperature in a linear way with negative slope coefficient. If we now find a way to add a voltage to this diode voltage VBE, which is Proportional To the Absolute Temperature (PTAT) with the same positive slope coefficient , then we obtain a reference voltage Vref which is independent of temperature. Moreover, we will find that this reference voltage is the bandgap voltage itself.

5.3 Different Topologies for Bandgap reference circuits

One of the first bandgap references is shown in this slide. The PTAT current generator Q1-Q2-R2 provides a PTAT voltage across resistor R1. This voltage is added to the VBE1 of transistor Q1, towards a bandgap reference voltage indeed. Again, the output impedance is low, because an emitter follower is used to close the feedback loop at the output.

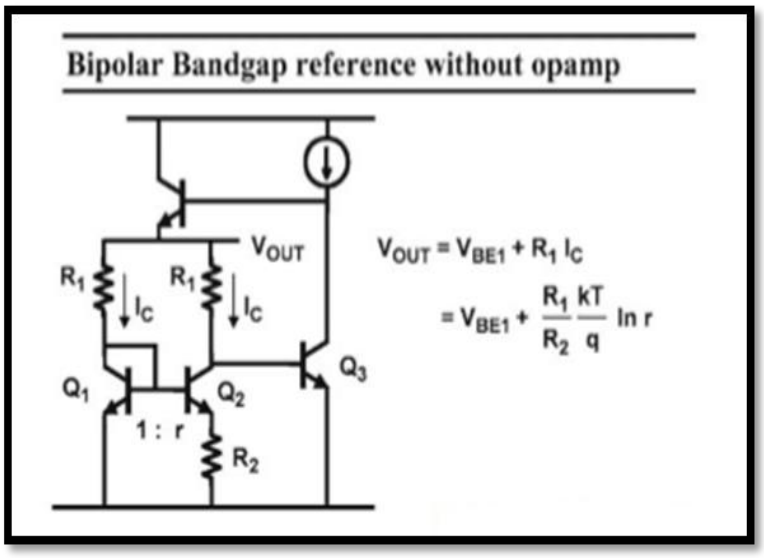


Figure 5.3: Bipolar Bandgap reference without opamp

Operational amplifiers can provide much more loop gain than a transistor pair. In this bandgap reference, the opamp finds an output voltage such that the differential input zero becomes zero. If the resistors R are chosen such that they take up about 0.6 V, then the output voltage is about 1.2 V. The output impedance is obviously very low, at least at low frequencies. The same applies to the bandgap reference on the

right. Its PSRR is worse however because transistors are used, with their collectors connected to the power supply**.**

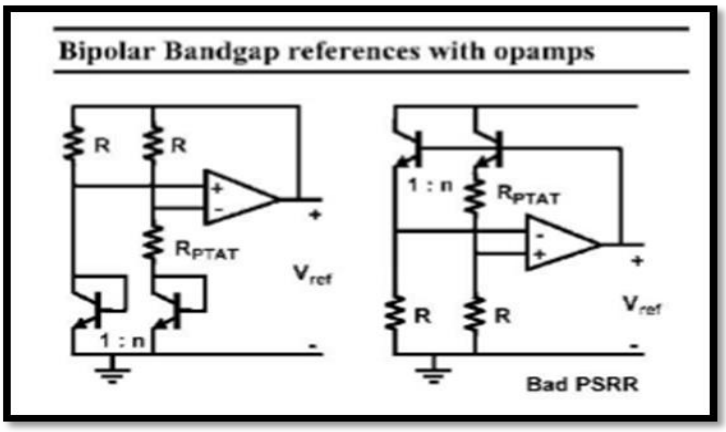


Figure 5.4: Bipolar Bandgap references with opamps

There is one important difference however. CMOS opamps have a larger offset. This means that they are only self-starting if the offset is right. Moreover, the offset gives a much larger error in the current equalization and therefore in the output voltage. The circuit on the right has again a worse PSRR.

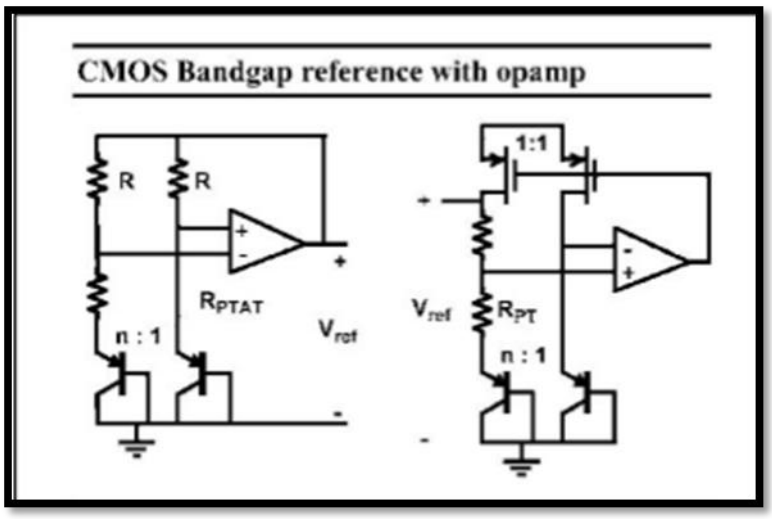


Figure 5.5: CMOS Bandgap reference with opamp

Sometimes a voltage reference is required which is not referred to ground or supply voltage. It is floating. This necessitates a full-differential opamp. The principle is shown in Fig. 5.6. Two pairs of substrate pnp's are used to generate a double bandgap voltage of about 2.4 V on the right. For this purpose, transistors Q1 and Q2 must be biased by a PTAT current, which is not shown here.

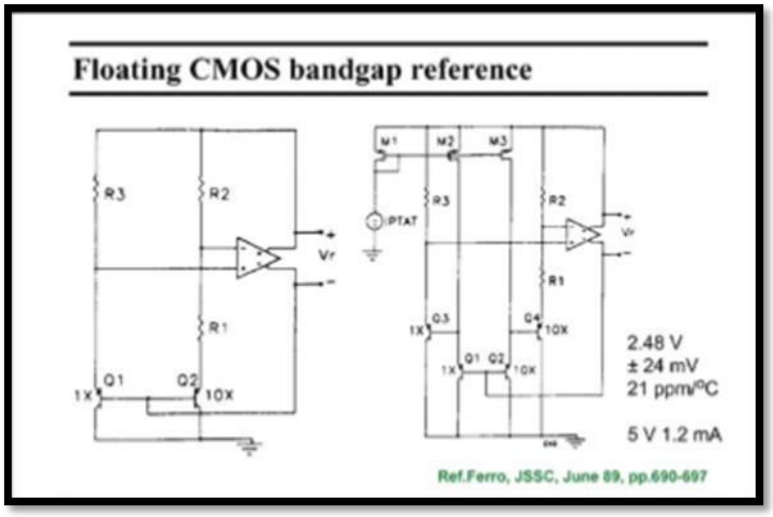


Figure 5.6: Floating CMOS bandgap reference

It is possible to realize a bandgap reference without resistors. Actually, different sizes of MOSTs are used to amplify differences between diode voltages. Two diodes are present. A ten times larger current is pushed through the eight times smaller diode D2 to develop a voltage difference DVD, which is PTAT. This difference is then amplified by a differential pair M3/ M4 and mirrored to the output by M7/M5. Another differential pair M1/M2 then converts this current into a voltage again. The output voltage is a result of many scaling factors A, B and G such that an appropriate PTAT voltage is added to the voltage across diode D2. The output voltage is little less than 1.12 V with a variation of only 9 mV over a 70°C temperature range.

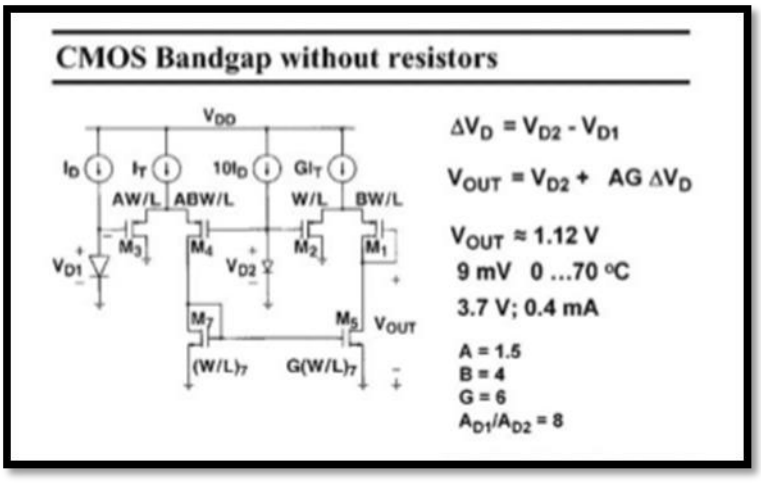


Figure 5.7: CMOS Bandgap without Resistors

The PTAT current generator Q1-Q2-R2 provides a PTAT voltage across resistor R1. This voltage is added to the VBE1 of transistor Q1, towards a bandgap reference voltage indeed. Again, the output impedance is low, because an emitter follower is used to close the feedback loop at the output.

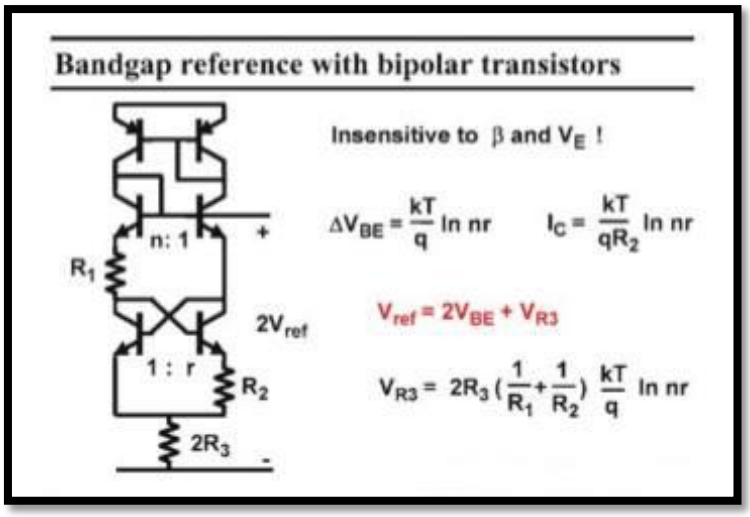


Figure 5.8: Bandgap reference with bipolar transistors

One of the problems of bipolar current mirrors is that some of the precision is lost because of base currents and output resistances. Moreover, mismatch between the bipolar device sizes leads to offset, and causes error voltages. In this realization, these errors are avoided. The pnp current mirrors on top are in series with npn devices. Also, a double reference voltage is taken to reduce the effect of mismatch. Its output voltage is therefore about 2.4 V.

**All the above bandgap reference circuits require startup circuit.

5.4 Different Topologies for Start-up circuit

Some topologies of bandgap circuits can't start by themselves so they need a start-up circuit to initialize the start-up nodes of the design.

The operating points are fund by drawing the two currents versus the common voltage V_{BE1}.The operating points are found at the crossings of the lines.

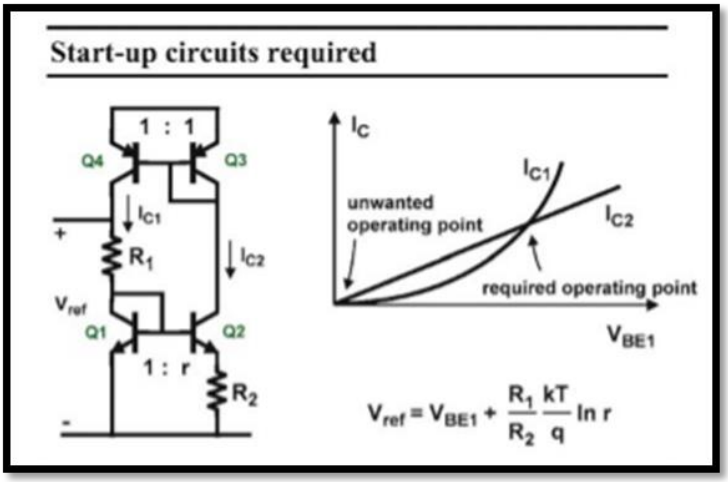


Figure 5.9: Start-up circuit idea

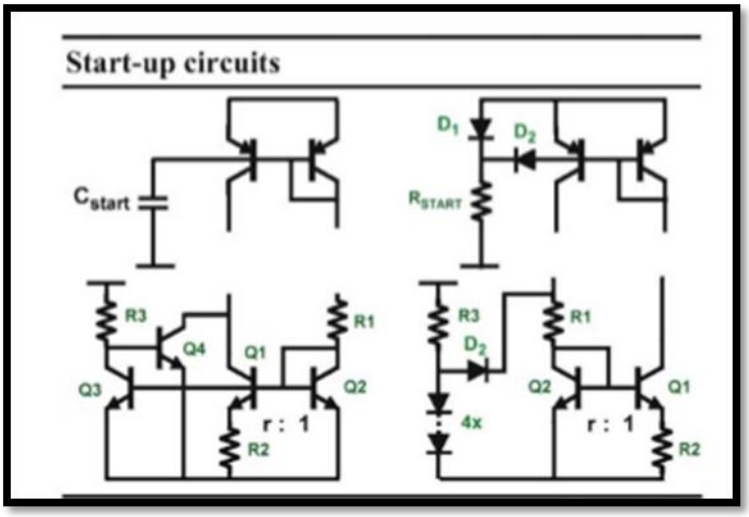


Figure 5.10: Different Start-up circuits

A capacitance at the base of the pnp current mirror draws a current when the supply voltage is switched on. This current flows through the pnp transistors and starts injecting a current in the bottom npn transistors as well, biasing up the bandgap reference circuit. However, if for some other reason the current drops to zero, then the supply voltage has to be switched on and off again.

The other circuit is better with this respect. When the supply voltage is switched on, diode D2 is forward biased, drawing current through the pnp transistors, and biasing up the total circuit. However, the current also starts flowing through resistor Rstart. .The voltage across this resistor increases until about 0.7 V below the supply voltage. Diode D2 is then reverse biased, and disconnected from the actual bandgap circuit. In this way the currents in the bandgap are not disturbed.

A similar arrangement with diodes is shown below in the above figure. The startup circuit below left is different. When the supply voltage is turned on, transistor Q4 starts drawing current, biasing up the bandgap reference. This circuit on its turn drives Q3, which switches Q4 off again. As a result transistor Q4 does not influence the current balance in the bandgap circuit.

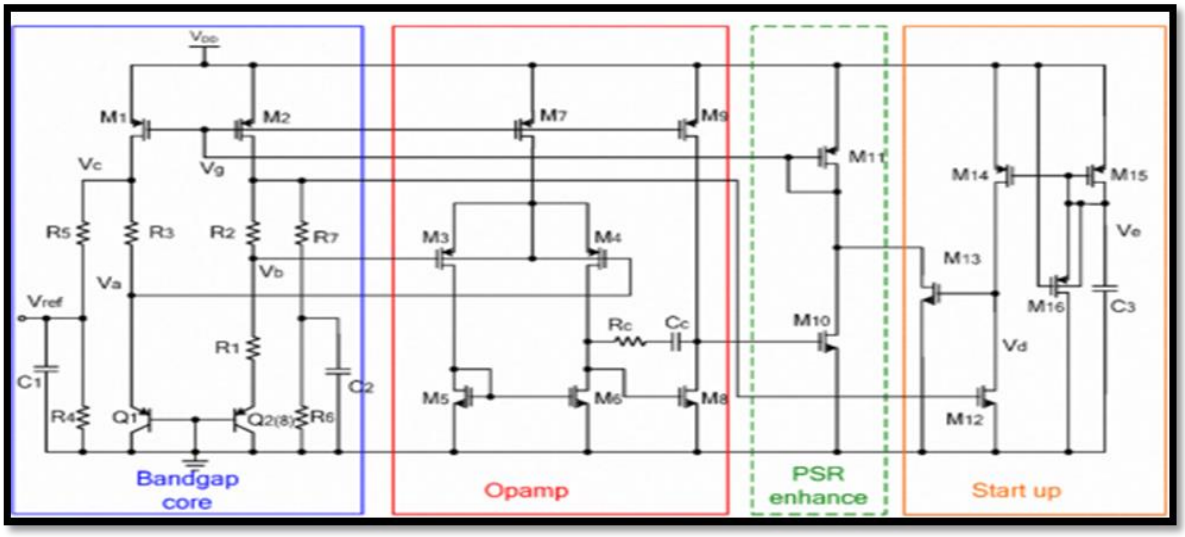


Figure 5.11: Start-up circuit from a Bandgap system already used in applications

-During power on, a current start to charge C3, current mirror of MI4 charges the gate of Ml3 , and turned Ml3 on to pull down node vg, injecting current into the bandgap core to guarantee successfully startup. After startup, MI2 is turned on then Ml3 cutoff.

-When C3 is charged to a threshold voltage below the supply voltage, both MI4 and MI5 are cutoff, thus, the power consumption of the startup circuits is zero after startup.

-MI6 is inserted to discharge C3 when supply is turned down, in order to make sure properly startup next time **[7]**.

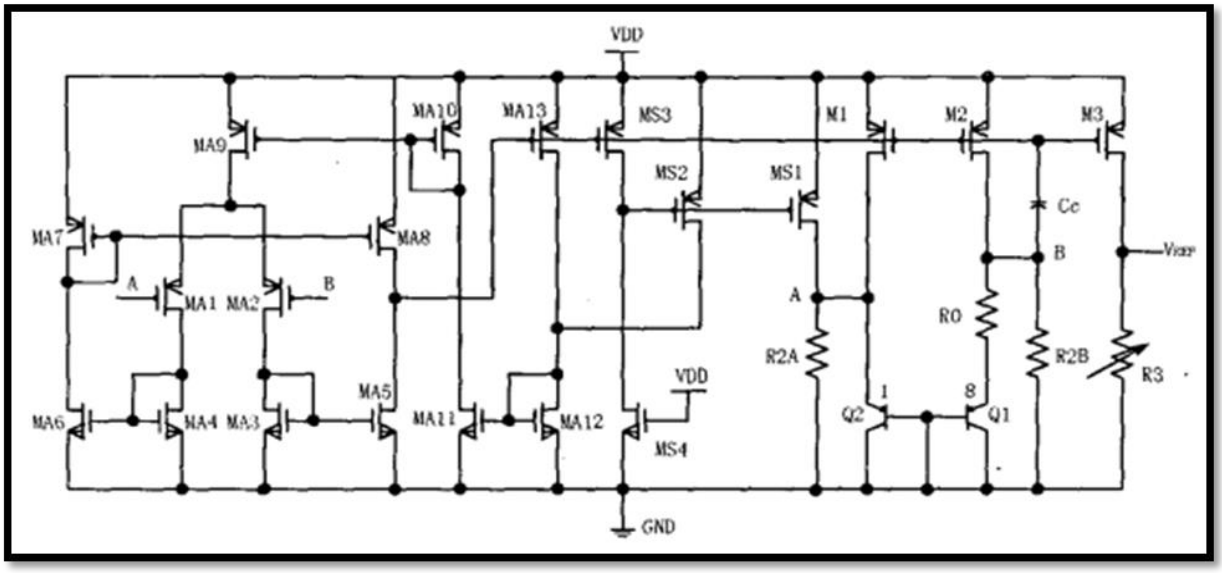


Figure 5.12: Start-up circuit used in applications

The start-up circuit is composed of MSI, MS2, MS3 and MS4. It will provide start-up current for Q2 and op amp. When the circuit operates in zero-current state, the gate voltages of M1-M3 the same as that of MS3. are pulled high and close to supply VDD.

-The drain voltage of MS3 or MS4 is pulled low and this tums on MSI and MS2 to inject current to the bandgap core circuitry by MSI and to the amplifier by MS2. Then the amplifier starts to operate and gradually pulls down its output voltage **[6]**.

5.5 Different Topologies for self-startup Bandgap reference circuit

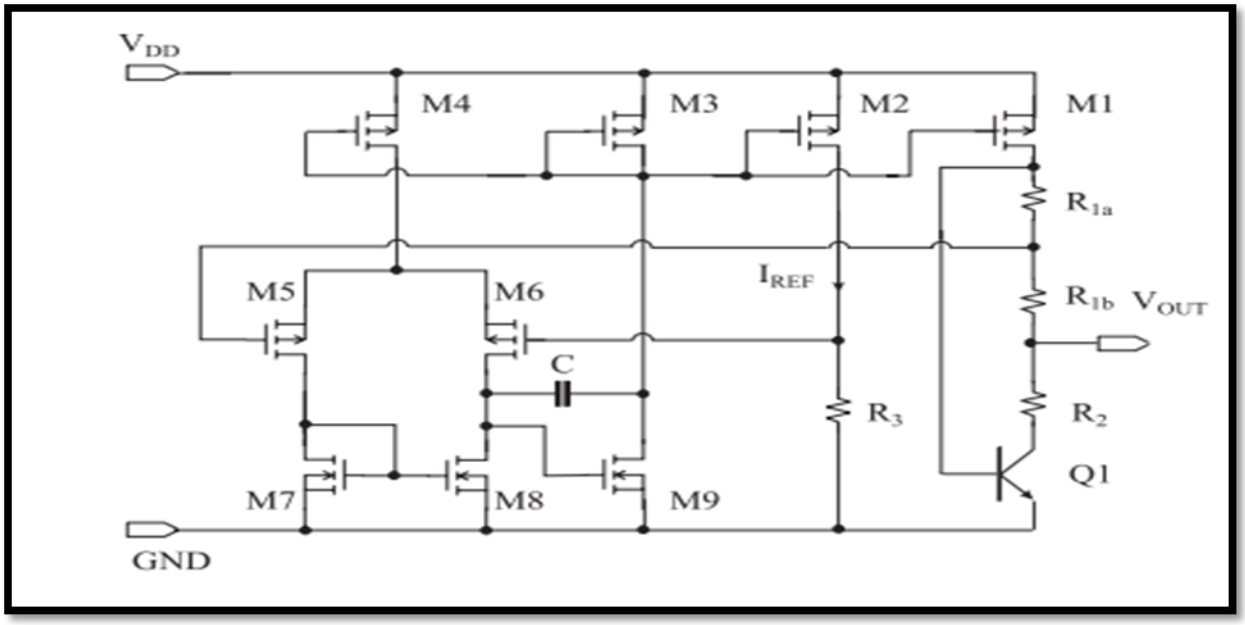


Figure 5.13: Self-startup Bandgap reference circuit

From Kirchhoff's voltage law:-

$-V_{DD} = V_{SG3} + V_C + V_{GS9}$.

At start-up:-

-when the initial voltage across C is zero, the power supply voltage VDD is divided between VSG3 and VGS9 and transistors $M_3 \& M_9$ $are\ turned\ on$, making the bias current flow in each branch of the circuit. The pMOS-input opamp circuit is biased as soon as the power supply is switched on and it provides the negative feedback which is necessary to the circuit for its correct operation **[4]**.

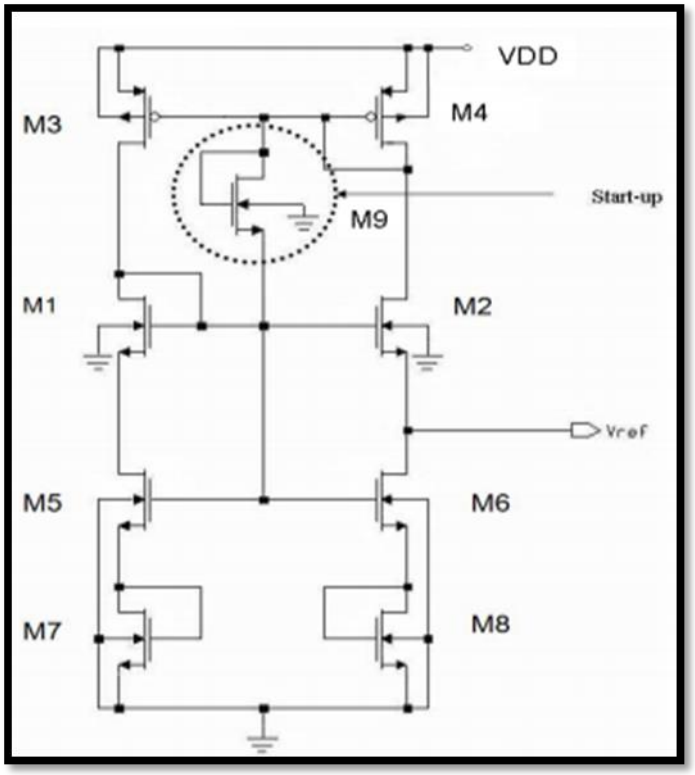


Figure 5.14: Self-Start-up Bandgap used in biomedical applications

When the supply is turned on, all the transistors carry a zero current through the branches as this is one of the operating points of loop formed by M1, M2, M3 and M4.Transistor M9 act as "start-up" circuit to remove this problem.
-When current through the branches is zero that means gate potential of M1 and M2 is at ground and that of M3 and M4 is at VDD. This makes M9 ON and it supplies charges to the gate of M1 and M2 from the gate of M3 and M4. As soon as the gate node of M1 and M2 charges up to the gate voltage of M3 and M4, M9 goes to cut off and thus start up device switches OFF **[5].**

5.6 The Bandgap reference circuit used in the Energy Harvesting system

In the realization shown in Fig. 5.15, an opamp is used which operates on supply voltages below or above 1 V. As a result, a real sub-1V or sub-3V bandgap reference emerges. BiCMOS is used, however, rather than standard CMOS. The principle is similar to the one previously mentioned. The opamp equalizes its input voltages by use of feedback. This voltage is simply VBE. All pMOSTs have again equal currents. The current through resistor R0 is thus PTAT. It is added to a current VBE/R2. This sum also flows through the output transistor. Resistor R3 then sets the output reference voltage **[3].**

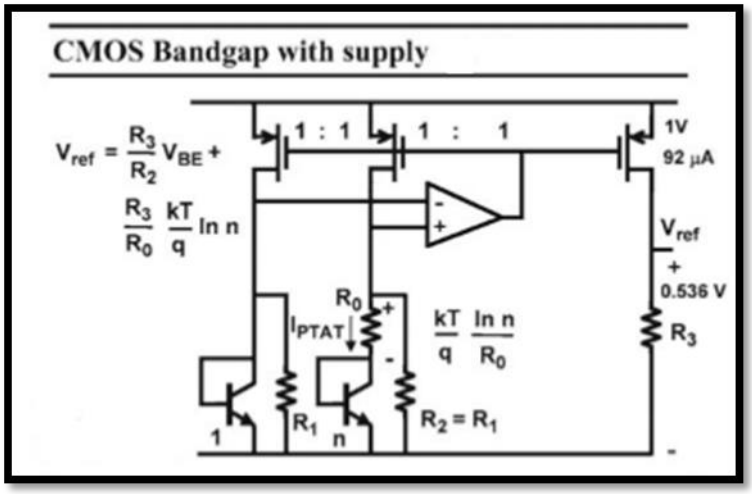


Figure 5.15: The circuit design of the Bandgap circuit used in the Energy Harvesting system

$$\boldsymbol{V_{ref} = I_{ref} * R_3 = \frac{R_3}{R_0} V_T \ln n + \frac{R_3}{R_1} V_{BE}} \text{ .} \qquad \textbf{(5.1)}$$

By solving the reference voltage equation (5.1) and taking into account that $R_1 = R_2$ and n=8.

We found that to have the output voltage equal to 800mV, The Ratio

Between R_1 *or* R_2 and R_0 is between 9 and 11.

$$\therefore \quad \boldsymbol{9 < \frac{R_2}{R_0} < 11}$$

5.7 The Start-up circuit used with the above circuit design

The shown Start-up circuit is used to bias the bandgap circuit with the required current and voltage to enable it to start its operation at the beginning.

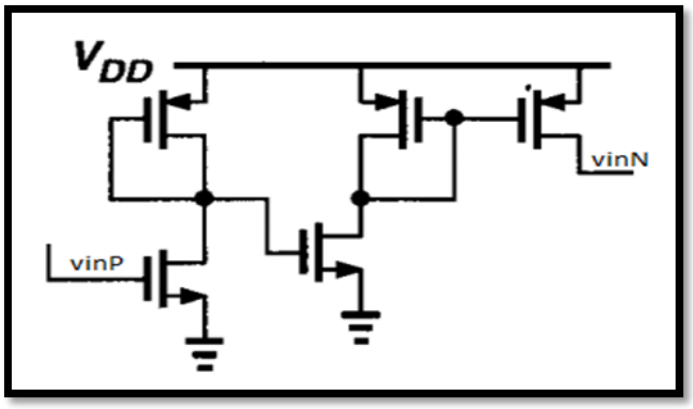


Figure 5.16: The Start-up Circuit design

5.8 The Error amplifier used in the Bandgap circuit

This is the used simple operational amplifier in the design of the Bandgap reference circuit. Its gain is around 55dB with bias current equals to 400 nano ampere. This OTA is stable with phase margin (PM) =81° and this shown in Fig. 5.27.

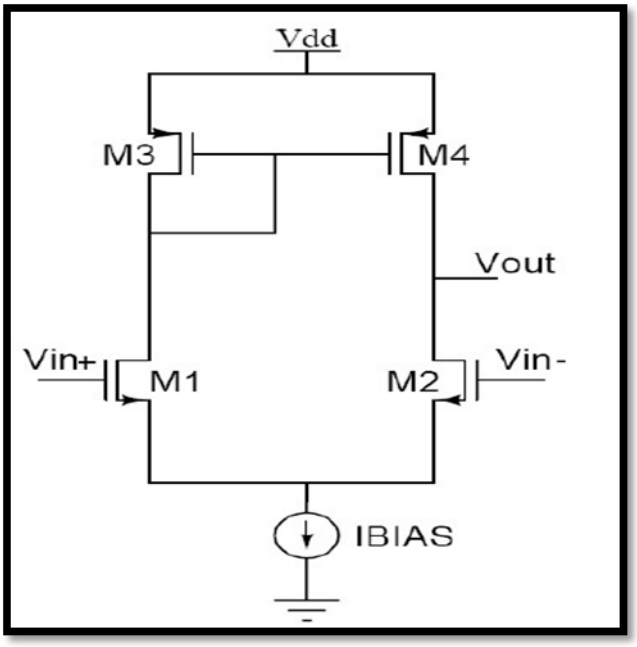


Figure 5.17: The Architecture of the OTA

Table 5.1: Transistors sizing of the OTA

$(\frac{W}{L})M_1,M_2$	*30/3*
$\frac{W}{L})M_3,M_4$	*6/3*

5.9 Schematics from Cadence

i. Schematic of the Error amplifier

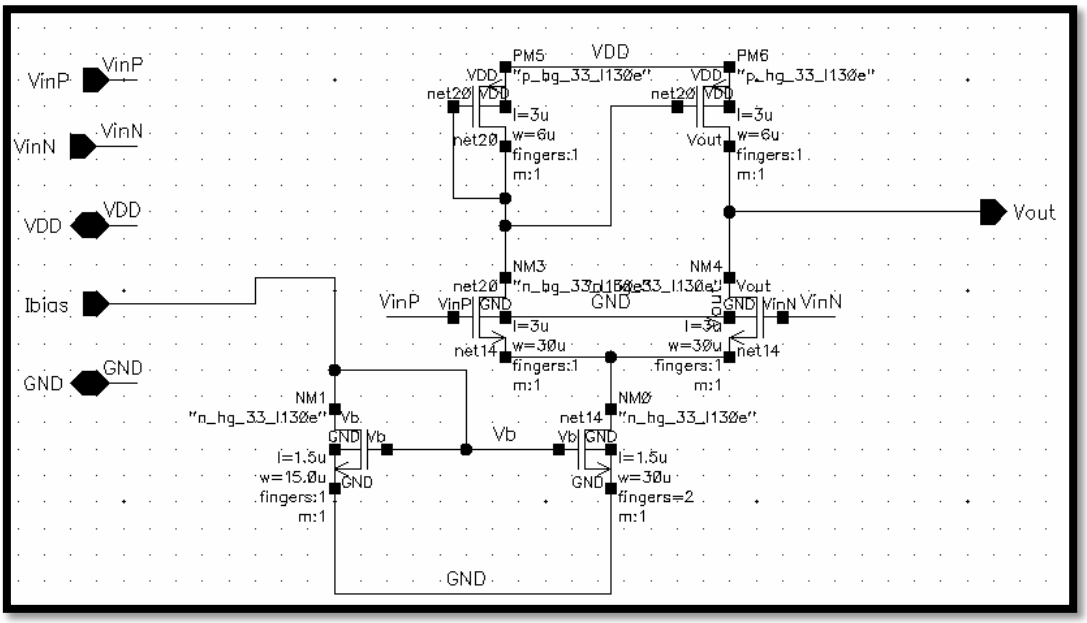


Figure 5.18: The Schematic of the Error amplifier

ii. Schematic of the Start-up circuit

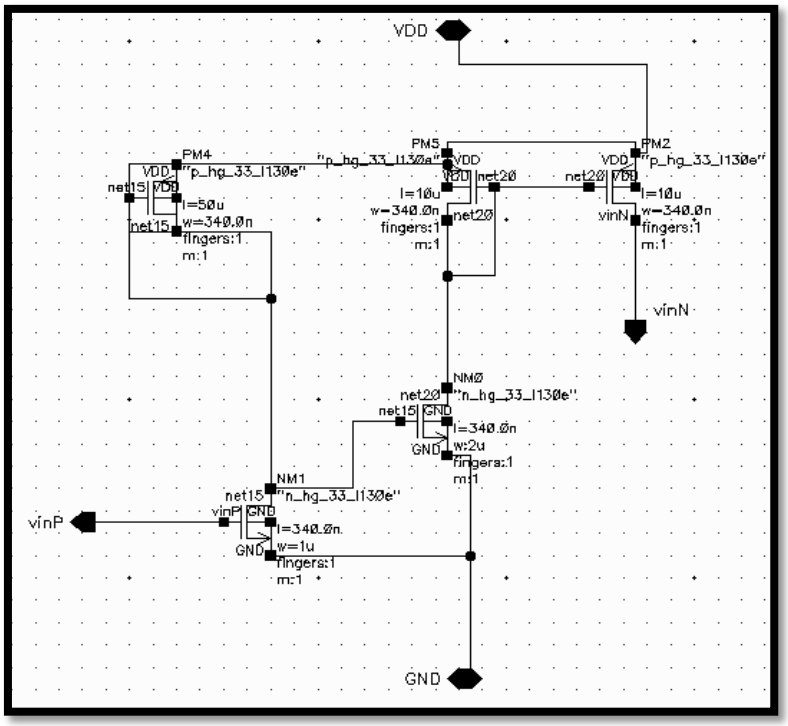


Figure 5.19: The Schematic of the Start-up circuit

iii. Schematic of the Total Bandgap circuit

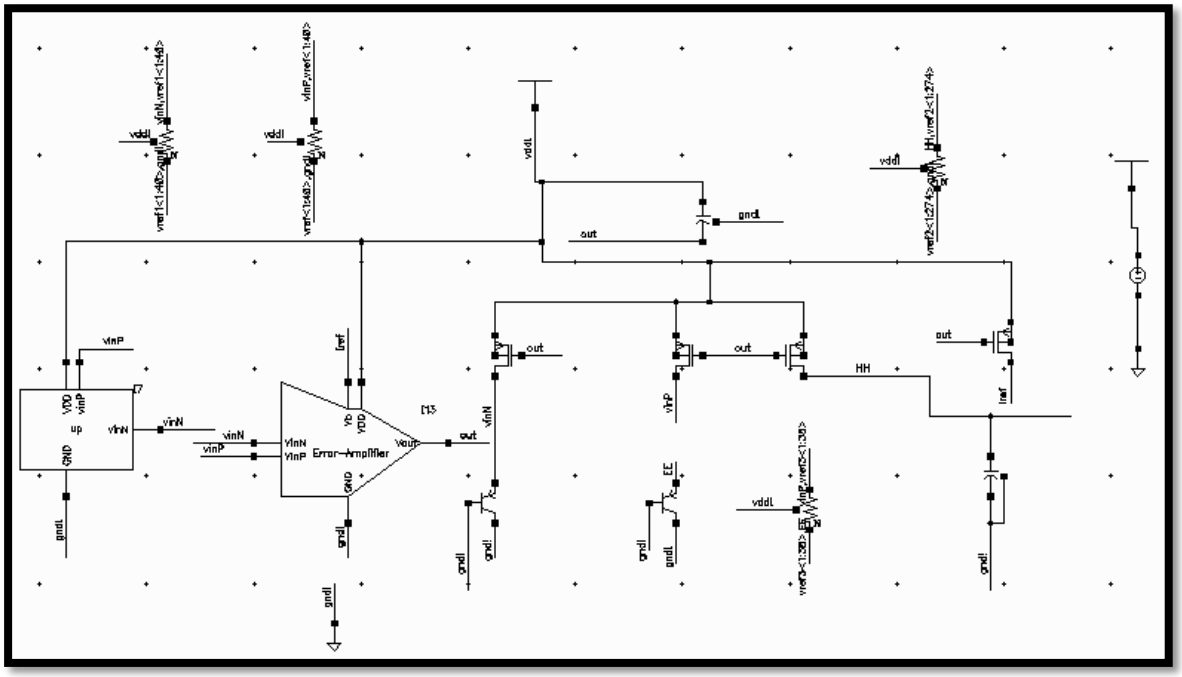


Figure 5.20: The Schematic of the Bandgap reference circuit

iv. Schematic of the Total Bandgap circuit in Blocks

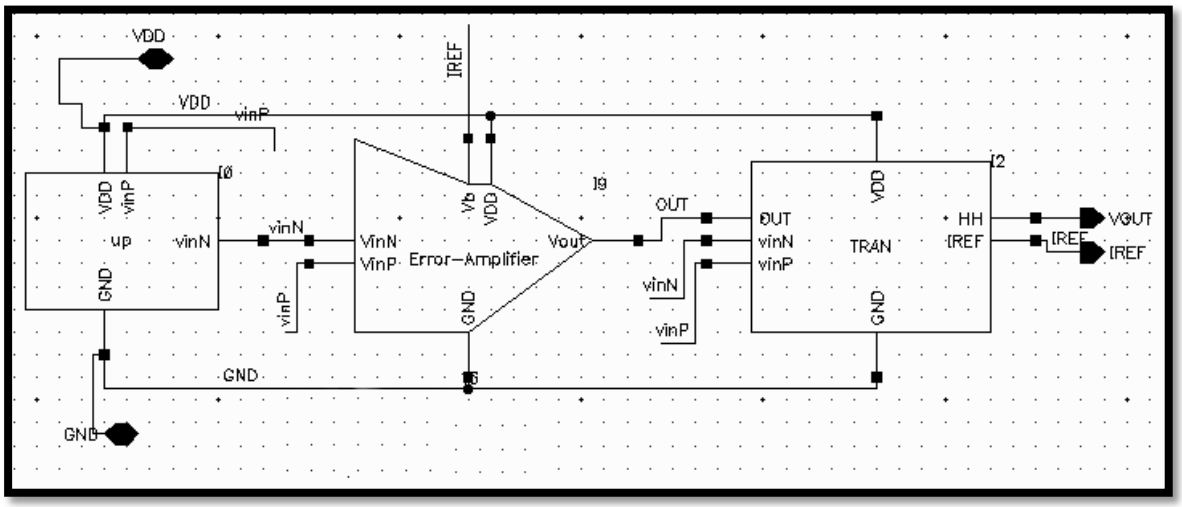


Figure 5.21: The Schematic of the Bandgap circuit in Blocks

v. Schematic of the test bench of the Bandgap

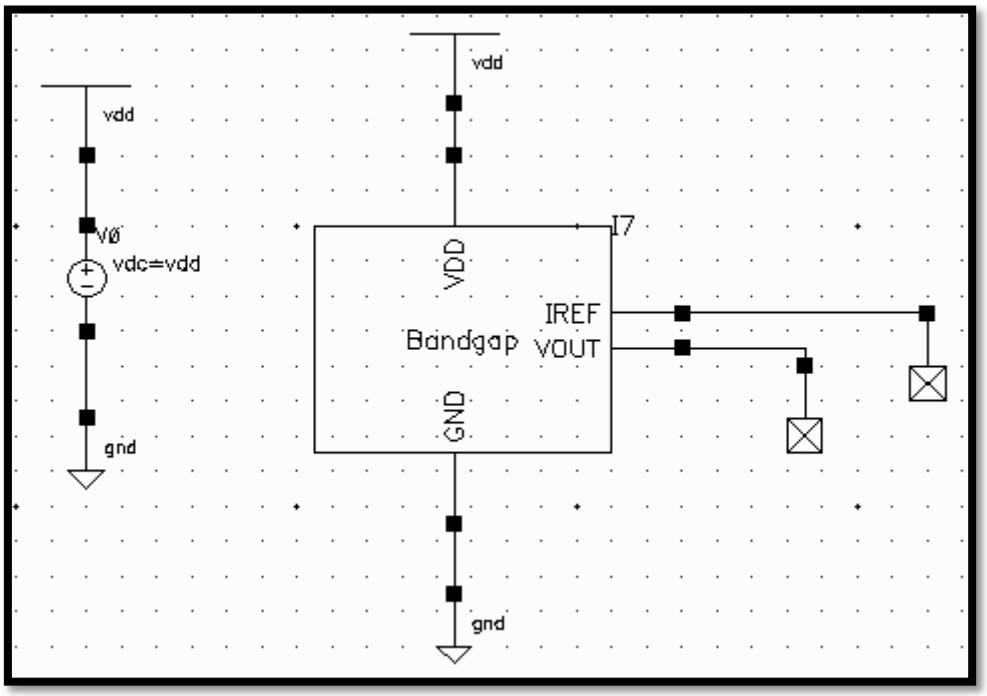


Figure 5.22: The Schematic of the test bench of the Bandgap circuit

5.10 SIMULATION AND MEASUREMENT RESULTS

5.10.1 The Transient Analysis

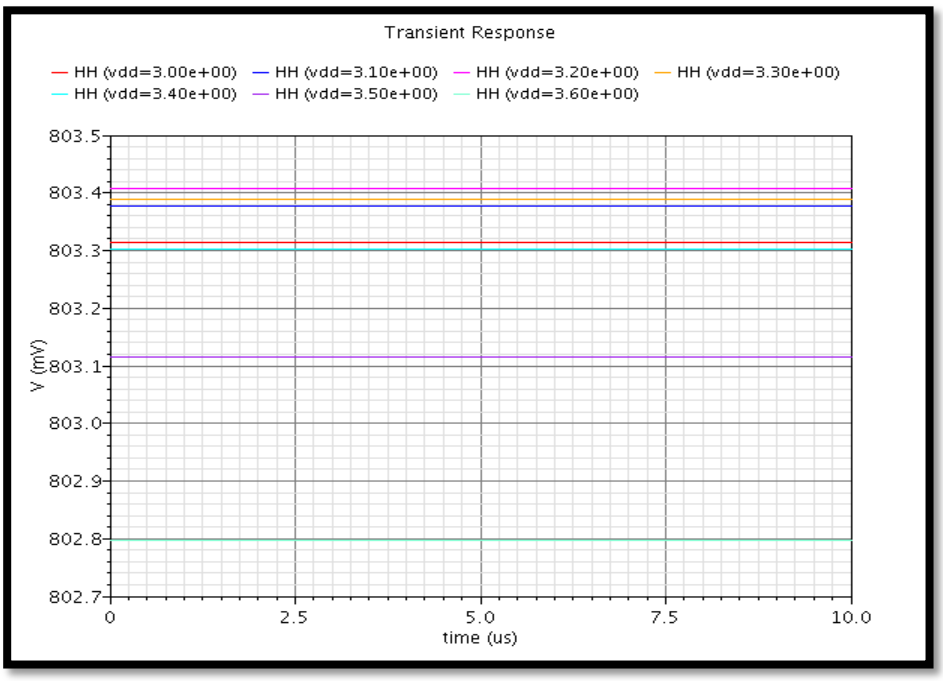


Figure 5.23: The Transient response analysis results of the Bandgap circuit

**As shown from the above results the output voltage variations with the supply voltage vary from802.7973 mV to 803.4085 mV with supply variations from 3:3.6 V.

5.10.2 The DC Analysis

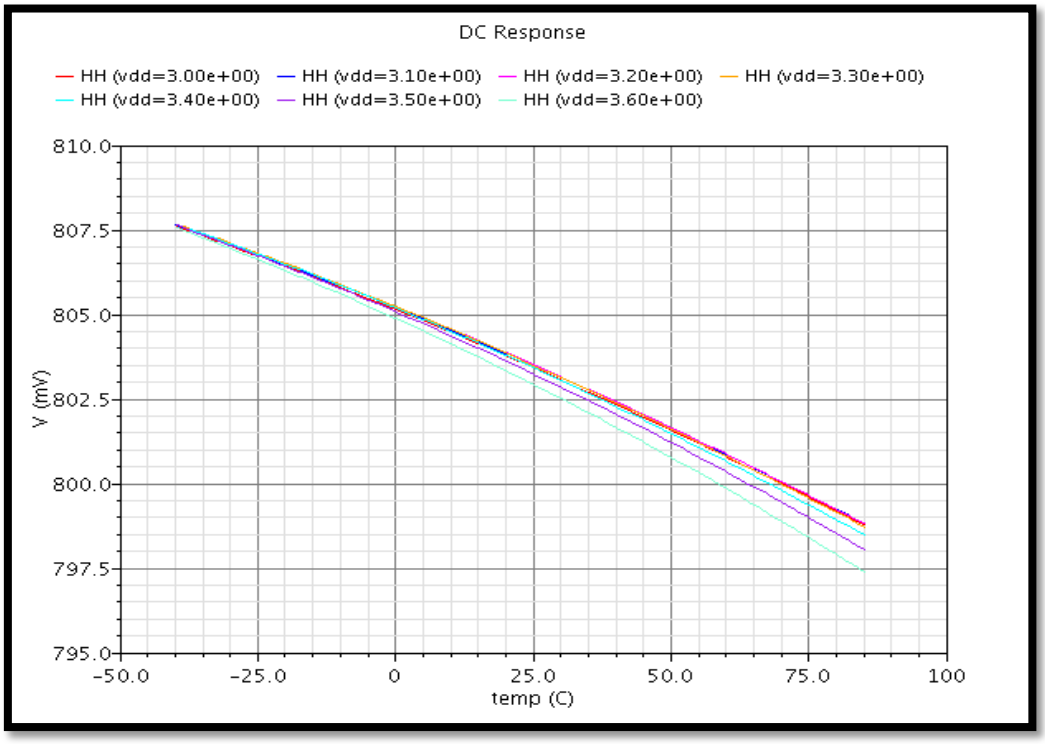


Figure 5.24: The DC response analysis results of the Bandgap reference circuit

**COMMENT:

From the results of the DC analysis shown above, the temperature dependency isn't cancelled at all, but there exist negative temperature dependency. In our Energy Harvesting system this small negative dependency doesn't affect our system as well as all results from this bandgap circuit design is within ranges and as required. So these results are accepted.

5.10.3 The Corners simulation results (PVT)

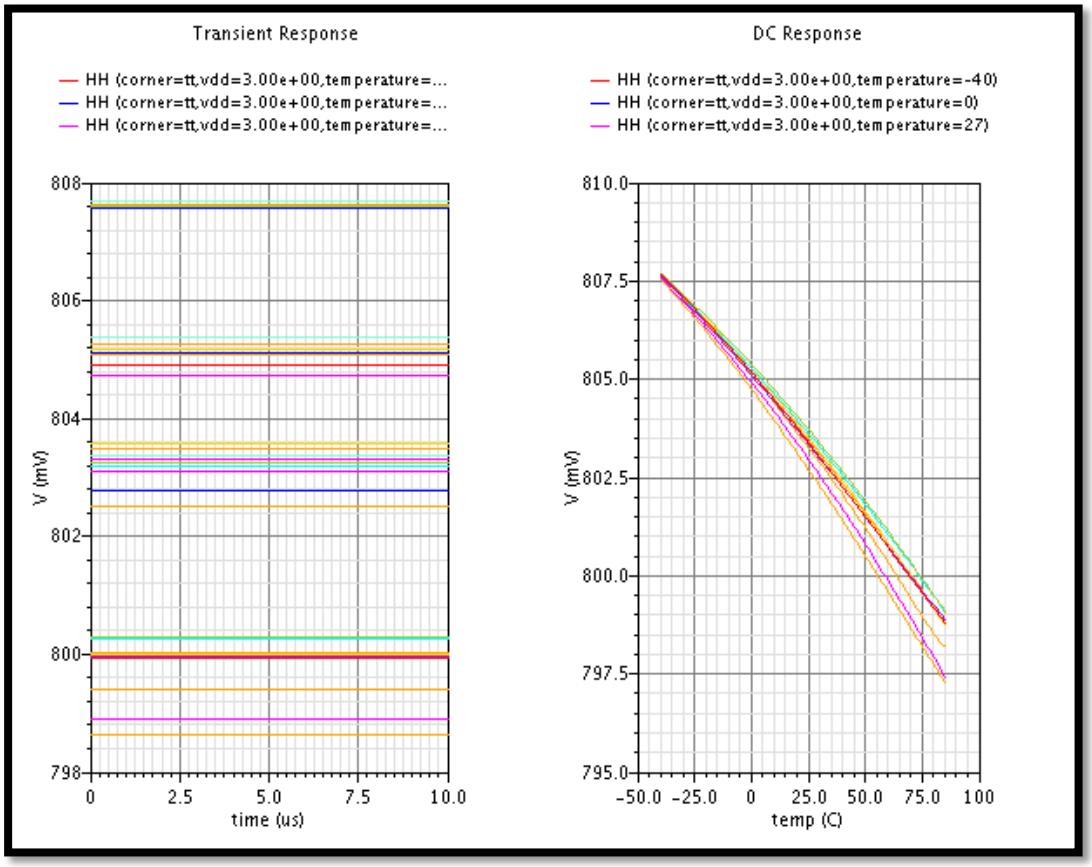


Figure 5.25: Corners simulation results of the Bandgap reference circuit

** As shown from corners simulations and as we have limits to the reference voltage resulted from the Bandgap reference circuit to be between 794 mv and 816 mV. So the results are still within the limits.

5.10.4 The Specifications of The Bandgap circuit

Table 5.2: shows the targeted and achieved specifications from the Bandgap reference circuit

Specification	Target	Achieved
Technology Process	UMC 130 nm	UMC130nm
Supply Variation	+/- 10 %	3:3.6V
Temperature Range	-40: 85 degree	-40:85 degree
PSRR	20 dB at 20MHz	20.67 dB at 20MHZ
Output Voltage Variation with Supply	+/- 0.5 %	From 802.7973: 803.4085 mV (From0.2%:0.455%)
Output Voltage	800mV	800mV
Minimum capacitance used	100 fF	2.99pF
Power Consumption Maximum	50 µW	30 µW

** **power supply rejection ratio** or **PSRR** is a term widely used in the electronic amplifier (especially operational amplifier) or voltage regulator datasheets; used to describe the amount of noise from a power supply that a particular device can reject.

The PSRR is defined as the ratio of the change in supply voltage in the op-amp to the equivalent (differential) output voltage it produces.

$$\textbf{PSRR[dB]=20log}_{10}\left(\frac{\Delta V_{supply}}{\Delta V_{out}}.Av\right)dB.$$

5.11 LAYOUT

i. The Layout of the OTA

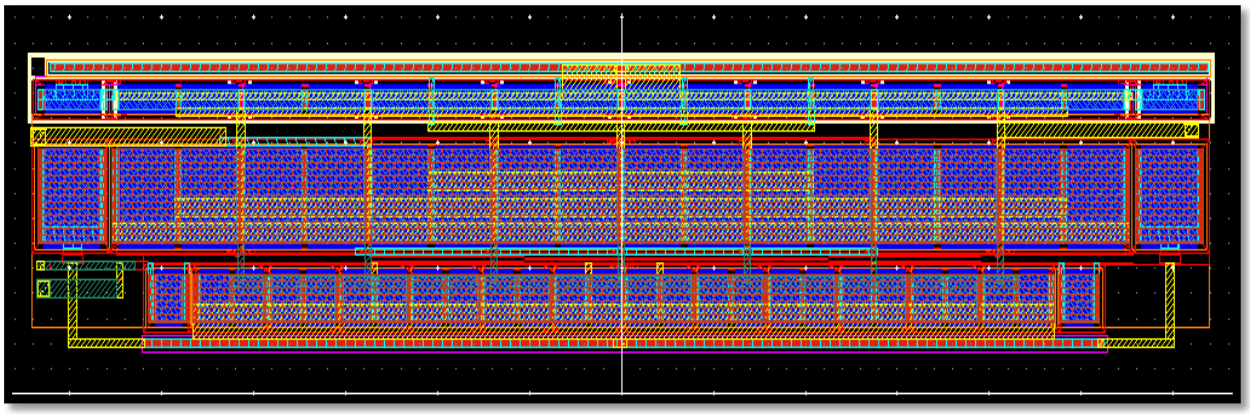


Figure 5.26: The layout of the operational amplifier used in the Bandgap circuit

ii. Pre and Post Layout simulations of the Error Amplifier

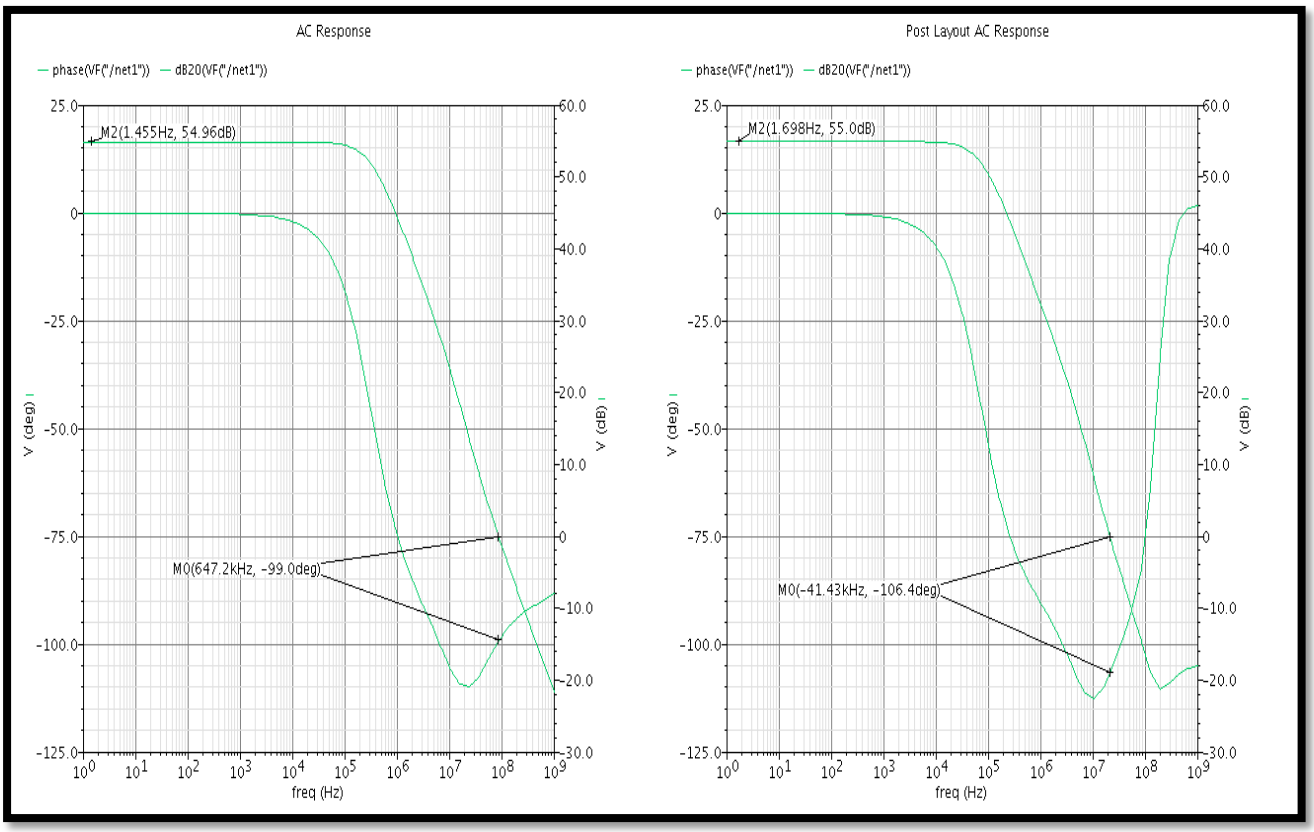


Figure 5.27: Pre and Post Layout simulations of the Error amplifier

iii. The Layout of the Resistors, Capacitors and BJTs

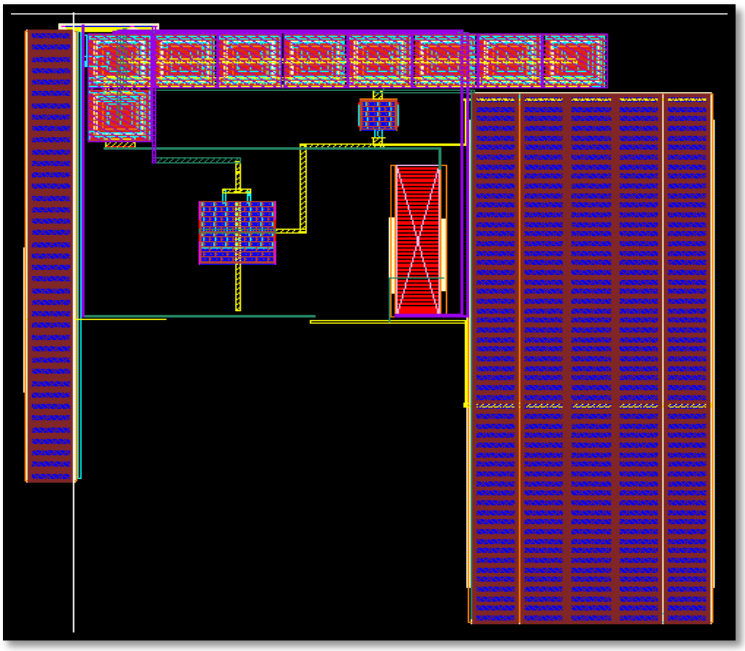


Figure 5.28: The layout of the Resistors, Capacitors and BJTs used in the Bandgap circuit

iv. The Total Layout

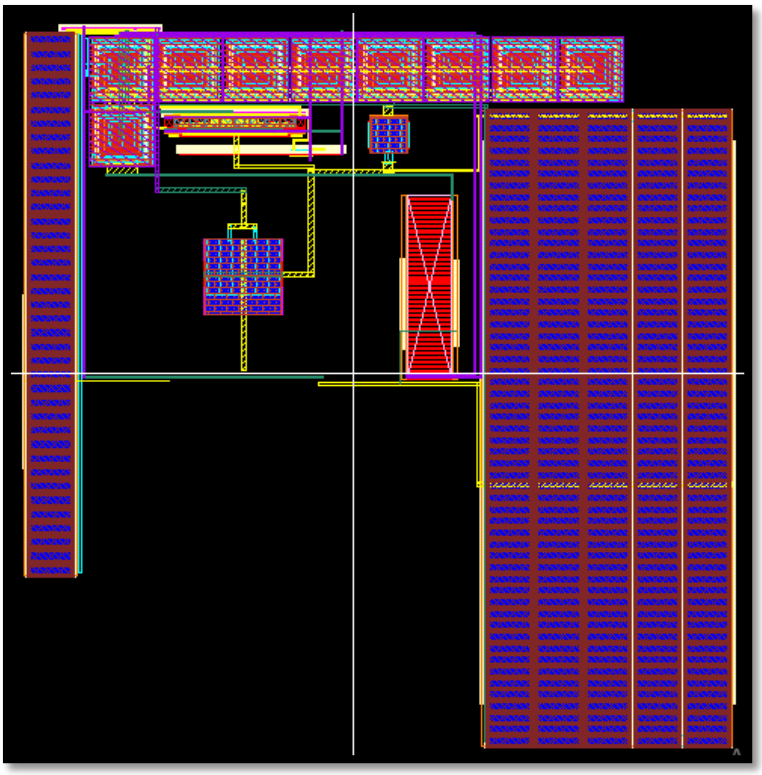


Figure 5.29: The Total layout of the Bandgap reference circuit used in Figure 2-15

The Above layout is the total layout of the Bandgap reference circuit shown in Fig. 5.15 which is used in the Energy Harvesting system as part of the DC to DC converter.

Chapter 6 Charge Pump

6.1 Introduction

There are worldwide efforts on going on development of micro generators that should eliminate the necessity of wiring and batteries in autonomous and stand-alone devices or in devices that are difficult to access. Thermal Energy harvesters are being developed for that purpose, but the human body is not a perfect heat supply for a wearable TEG. The body has high thermal resistance; therefore, the heat flow is quite limited so the most important part in the design of the system shown in Fig. 6.1 is the part of the charge pump design and the maximum power point tracking (MPPT) circuit. A new MPPT circuit is proposed to achieve high power efficiency with maximum load current.

6.2 Thermal Energy Harvesting

The thermoelectric effect is the fact that a temperature gradient in a conducting material results in heat flow; this results in the diffusion of charge carriers. The flow of charge carriers between the hot and cold regions in turn creates a voltage difference Electric power is produced by a temperature difference on the sides of the thermoelectric module TEM heated by a waste heat which can come from industrial processes or even human warmth. After that, the generated low voltage is boosted up in a DC/DC converter or a charge pump CP. Next, in power management unit we used Maximum Power Point Tracking is a method used for extracting maximum available power from any module under certain conditions.

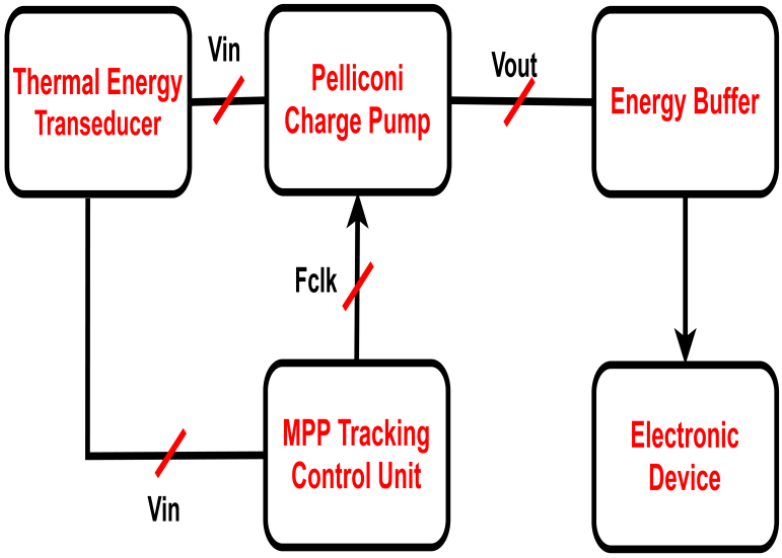


Figure 6.1: thermal Energy harvesting block diagram

6.3 Basics of thermoelectric generators

Thermoelectric generator TEG is a solid-state device as shown in Fig. 6.2 capable of converting heat into electrical energy. Conversation between heat and electricity are described by three thermoelectric effects. These effects are the Seebeck effect, the Peltier effect, and the Thomson effect

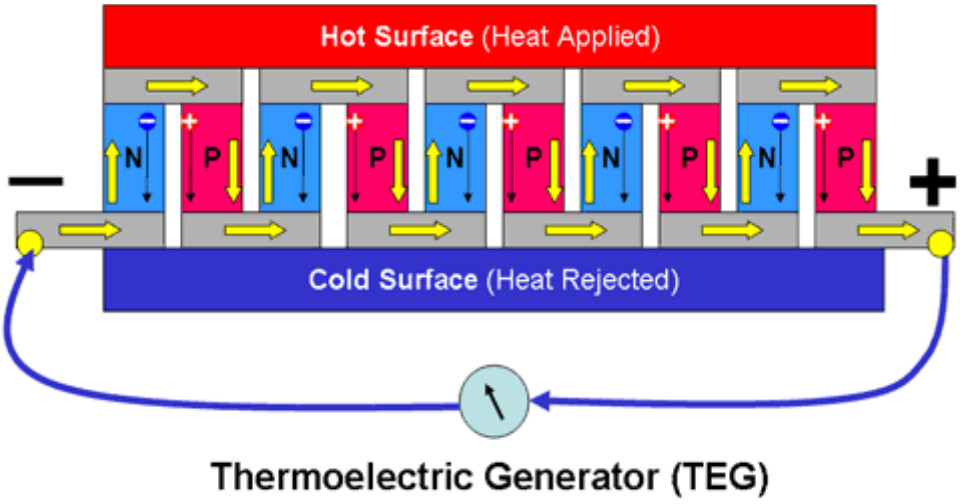


Figure 6.2: thermoelectric generator

6.3.1 Seebeck effect

Seebeck Effect describes the case of conversion from heat to electricity. Circuit consisting of two different conducting materials, whose connections are at different temperatures. This will produce an output voltage.

6.3.2 Peltier effect

This effect is opposite in principle to the Seebeck effect. at the junction of two different conducting materials in the presence of a flowing electrical current. Depending on the direction of current flow the junction absorbs or dissipates heat to the surroundings. The amount of absorbed or dissipated heat is proportional to the electrical current and the absolute temperature *T*.

6.3.3 Thomson Effect

Unlike Seebeck effect and Peltier effect, Thomson effect can be existed in
A single material heat absorption or dissipation can occur along the material when the material is subjected to a temperature difference and electric current.

6.4 Step-up DC-DC Converter

Thermal energy harvesting has many key challenges as its relatively low output voltage which around 0.2 volt which cannot power any electronic circuit. Step-up DC-

DC converters are used after the TEG to generate a higher voltage from the low voltage.

6.4.1 Charge pump

Charge pump is a type of DC-DC converter. The operation of the Charge pump depends on the concept of charge conservation. In the charging and discharging of the used capacitors till the charge reach final load during successive phases.

6.4.2 Charge Pump Design Criteria

Charge pump has many design criteria which are taken into consideration by the designer. Depending on these criteria, the one can determine best charge pump to meet the desired application. Some of these criteria are power efficiency, output voltage ripples, current drivability and layout area.

i. Charge Pump Power Efficiency

Charge pump power efficiency is the significant factor in charge pump design. It is defined as the ratio between the output power and the power supplied from the DC input voltage and the clock sources. The efficiency can't be 100% because the whole circuit consumes power from the input power and not all the input power can be delivered to the load.

ii. Output Voltage Ripple

The ripple at the output node is due to charging and discharging the output node by the load resistance RL.

iii. Layout area

The area of the charge pump on silicon is one of the most important criteria in charge pump design. The capacitors can be considered the element which consumes much more area than transistor's sizes on silicon, but it much better than coil area which almost preferred to be off chip.

6.5 Pelliconi Charge Pump

The operation of pelliconi charge pump shown in Fig.3 is as follows, during the first half cycle Φ1 is high and Φ2 is low, M1 and M2 are on and M0 and M3 are off, C0 is charged to V_{TEG} through M1 so V0 is set to V_{TEG} and C1 is charged to VDD+V_{TEG} and discharge it to $Vout$ through M2. During the second half cycle, Φ1 is low and Φ2 is high, M0 and M3 are on and M1, and M2 are off, C1 is charged to V_{TEG} through M0

so v1 is set to V_{TEG} and C0 is charged to VDD+V_{TEG} and discharge it to $Vout$ through M3 So the output is always VDD+V_{TEG} after first stage **[8], [9].**

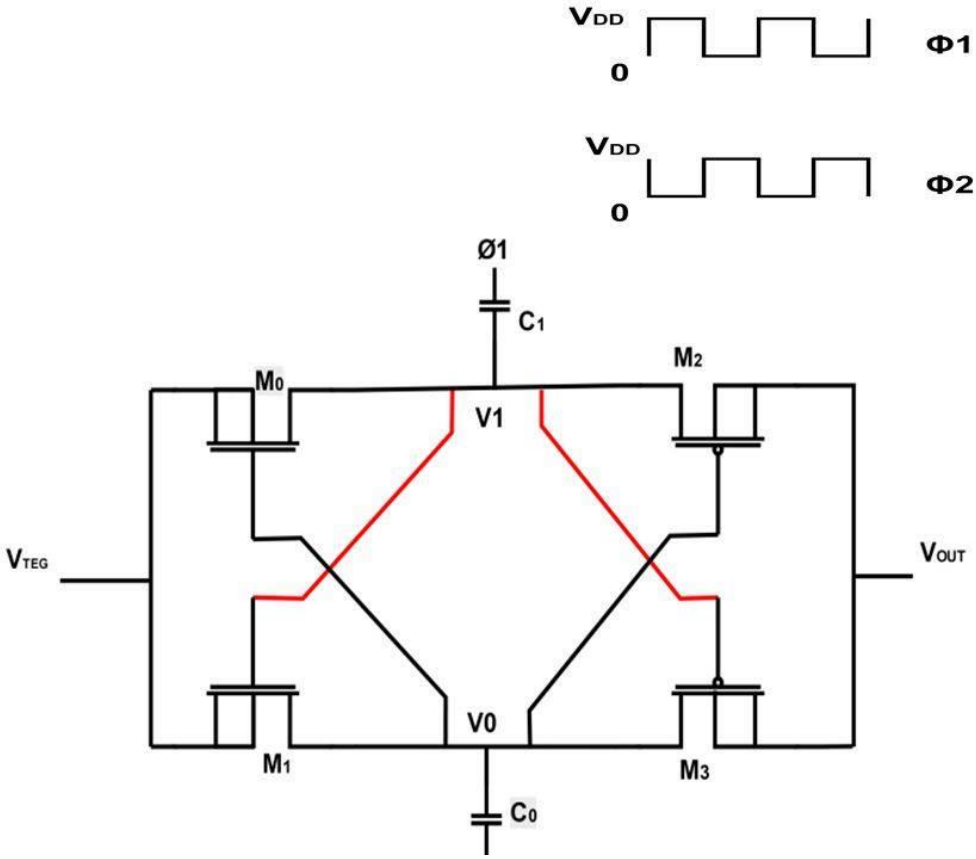


Figure 6.3: Pelliconi charge pump

More than one stage may be cascaded to produce an output voltage larger than VDD+V_{TEG} many several order of magnitude. Pelliconi charge pump has many advantages. First, its gain is large. It also uses very simple non-overlapping clocking scheme. In addition, it has a completely symmetrical scheme and no specific output stage is needed the output voltage for N stages can be expressed as **[13].**

Vout= VDD + NΔV (6.1)

ΔV = VDD.C/ (C + Cs) – Iout.Rout (6.2)

Where C0=C1=C, Cs is the parasitic capacitance

Where the output resistance Rout can be expressed as:

Rout = N.f/ (C + Cs) (6.3)

Where f is the operating frequency of the used clocks. It is clear that Pelliconi is more suitable for low voltage applications. But at very low voltage levels, cascading a many number of stages is necessary to obtain the desired output voltage e.g.; to obtain an output voltage of 3V from a 0.25V input, at least three stages are needed.

Pelliconi power efficiency is the significant factor in charge pump design. It is defined as the ratio between the output power and the power supplied from the DC input voltage and the clock sources.

To evaluate the power efficiency of pelLiconi charge pump we have used the following expression **[13].**

Efficiency=η=$\frac{Pout}{Pin} * 100 = \frac{Pout}{Pout+Ploss}$ (6.4)

But the efficiency can't be 100% because the whole circuit consumes power from the input power and not all the input power can be delivered to the load.

The consumed power can take places in many forms, first, form is the power dissipated in the charge pump output resistance. This resistive power consumption is Equal to **[13]**:

$Pres = Iout^2 . Rout$ (6.5)

Where Rout is the output equivalent resistance of the charge pump. Second the charging and discharging of the capacitance at each node gives a rise to dynamic power dissipation. Dynamic power consumption is frequency dependent and can be calculated as follows **[13]:**

$Pdyn = N. VDD^2 . C + Cs . f$ (6.6)

6.6 SIMULATION AND MEASUREMENT RESULTS

6.6.1 Simulations Results for one stage charge pump

i. Minimum Input Voltage

The TEG module is modelled to have output voltage 250mv. The maximum allowed value for the clock amplitude is 1.2V, design is running at operating frequency 6MHZ with charge pump capacitor of 25pf which normally can be integrated on chip.

ii. Output Voltage

Fig. 6.4 shows the simulation of Vout of the whole thermal energy harvesting system design one stages of charge pump.

iii. Voltage Gain

It is observed that the used charge pump circuit has the capability to pump supply voltage of 250mv to1.226v using one stage only.

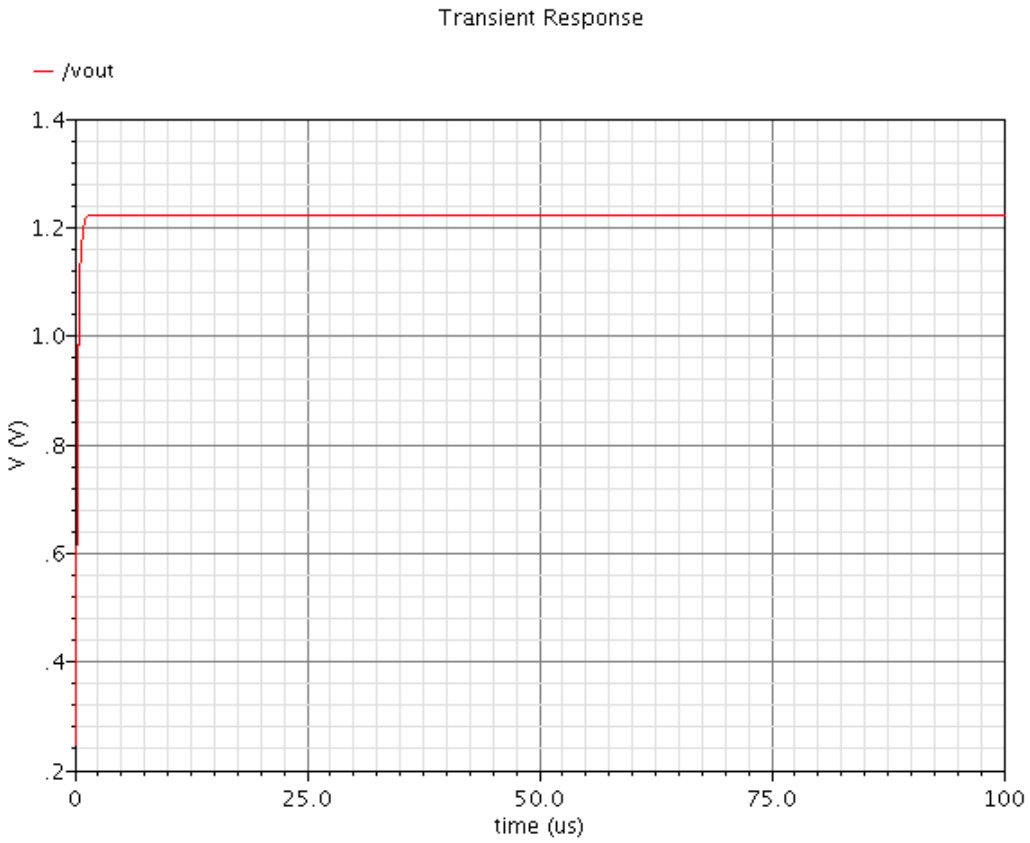


Figure 6.4: output voltage of charge pump (One-Stage, VTEG=0.25V, VDD=1V, f=6MHz)

6.6.2 Simulations Results for three stages charge pump

i. Minimum Input Voltage

The TEG module is modelled to have output voltage 250mv. The maximum allowed value for the clock amplitude is 1.2V, design is running at operating frequency 6MHZ with charge pump capacitor of 25pf which normally can be integrated on chip**.**

ii. Output Voltage

Fig. 6.5 shows the simulation of Vout of the whole thermal energy harvesting system design one stages of charge pump**.**

iii. Voltage Gain

It is observed that the used charge pump circuit has the capability to pump supply voltage of 250mv to3.177v using three stages only.

iv. Power efficiency

It is defined as the ratio between the output power and the power supplied from the DC input voltage and the clock sources.it reaches to 84.1% under condition (Three-Stages, V_{TEG}=0.25V, VDD=1V, f=6MHz).

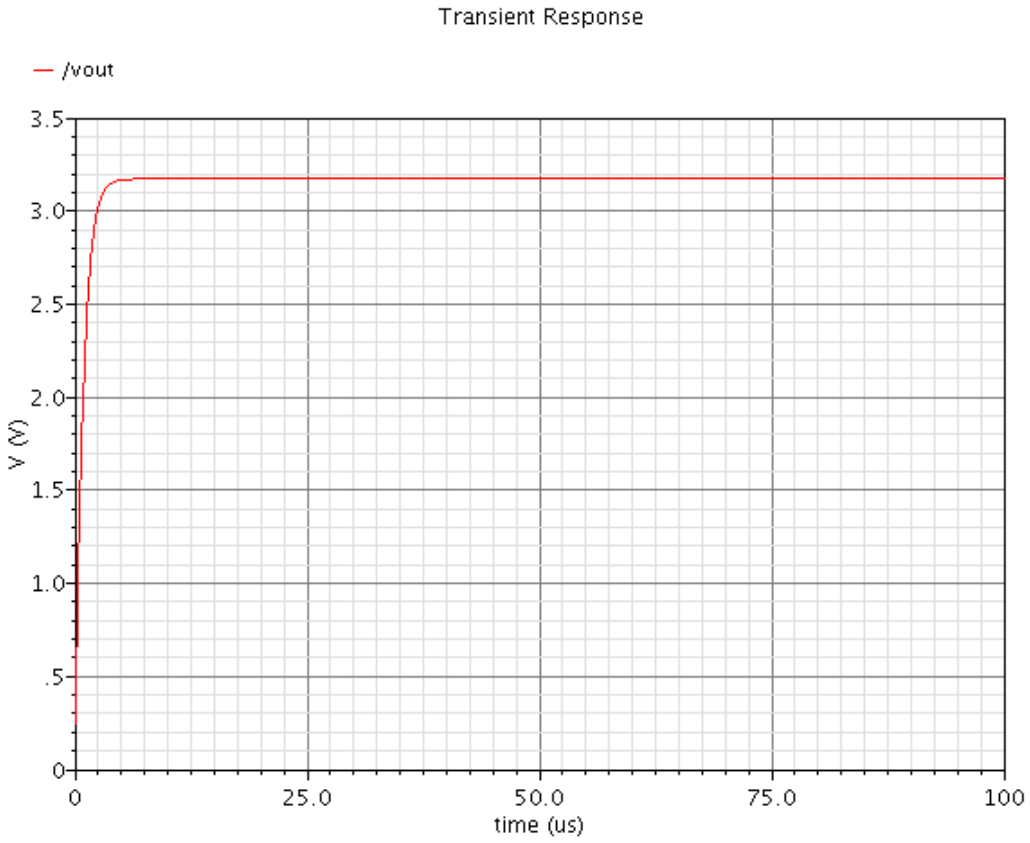


Figure 6.5: output voltage of charge pump (Three-Stages, V_{TEG}=0.25V, VDD=1V, f=6MHz)

6.6.3 Simulations Results for three stage charge pump and MPPT (of whole thermal Energy harvesting system)

i. Minimum Input Voltage

The TEG module is modelled to have output voltage 250mv. The maximum allowed value for the clock amplitude is 1.2V, design is running at operating frequency 6MHZ with charge pump capacitor of 25pf which normally can be integrated on chip.

ii. Output Voltage

Fig. 6.6 shows the simulation of Vout of the whole thermal energy harvesting system design three stages of charge pump.

iii. Voltage Gain

It is observed that the used charge pump circuit has the capability to pump supply voltage of 250mv to3.071v using three stage on and MPPT circuit.

iiv. Power efficiency

It is defined as the ratio between the output power and the power supplied from the DC input voltage and the clock sources.it reaches to 61.1% under condition (Three-Stages, VTEG=0.25V, VDD=1V, f=6MHz).

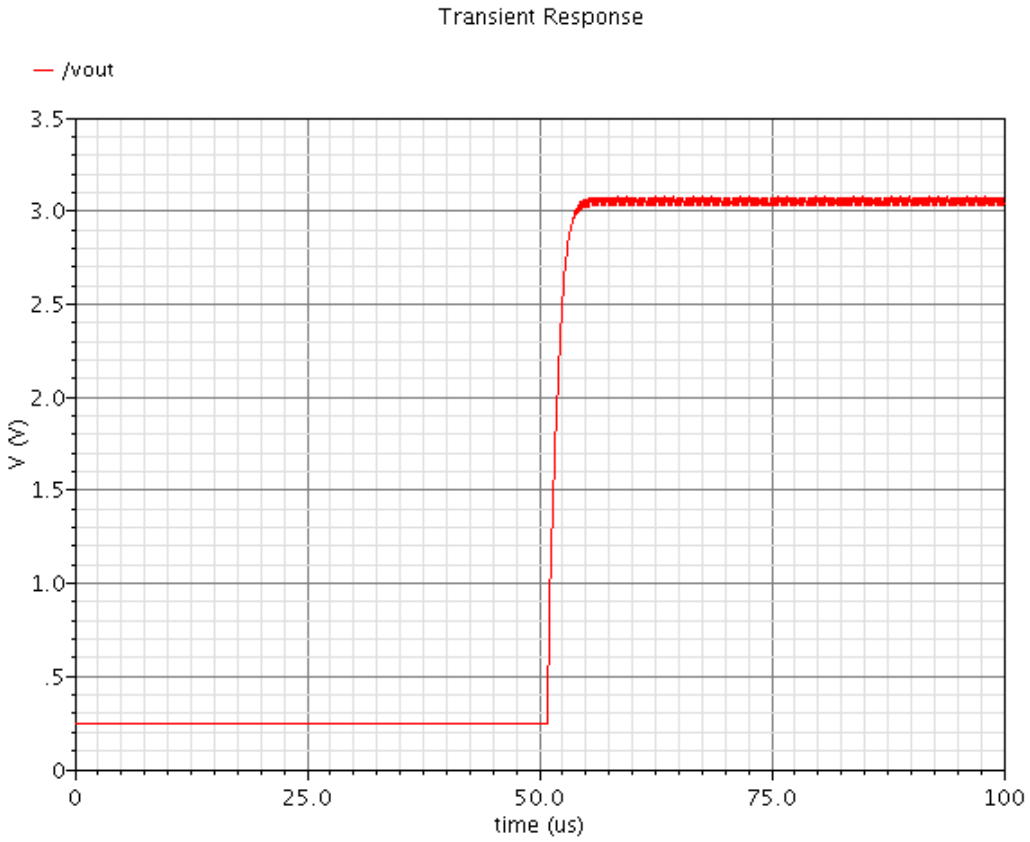


Figure 6.6: output voltage of whole thermal Energy harvesting system(Three-Stages, V_{TEG}=0.25V, VDD=1V, f=6MHz)

6.7 Comparison with other references

We will present in table 6.1 some comparisons among this work and other thermal harvesting to examine the performance obtained from our proposed system and this comparison shows that this system is an efficient thermal energy harvesting.

TABLE 6.1: show A PERFORMANCE COMPARISON BETWEEN THE PROPOSED SYSTEM, AND THE STATE-OF-THE ART ENERGY HARVESTING SYSTEMS

Specification	This work	Ref [8]	Ref [9]	Ref [10]	Ref [11]	Ref [12]
Input voltage	0.25v	0.3V	1.8v	0.2v	0.278V→0.32v	1.2v
Output voltage at load current	2.61v	2.72	5v	_____	_____	6.24V to 7.44V
Operating frequency	6MHZ	1MHz	100MHZ	250kHz	2.3 MHz→ 7MHz	250kHz
Max efficiency	61%	57%	54%	52%	47% → 63%	56 %
I_{out} at max efficiency	50µA	2.8µA	350 µA	30µA	_____	55nA
Control unit	Used	Not used	Not used	Not used	Used	Not used
Numer of stages	3stages	Six stages	3stages	_____	3stages	7stages

6.8 LAYOUT

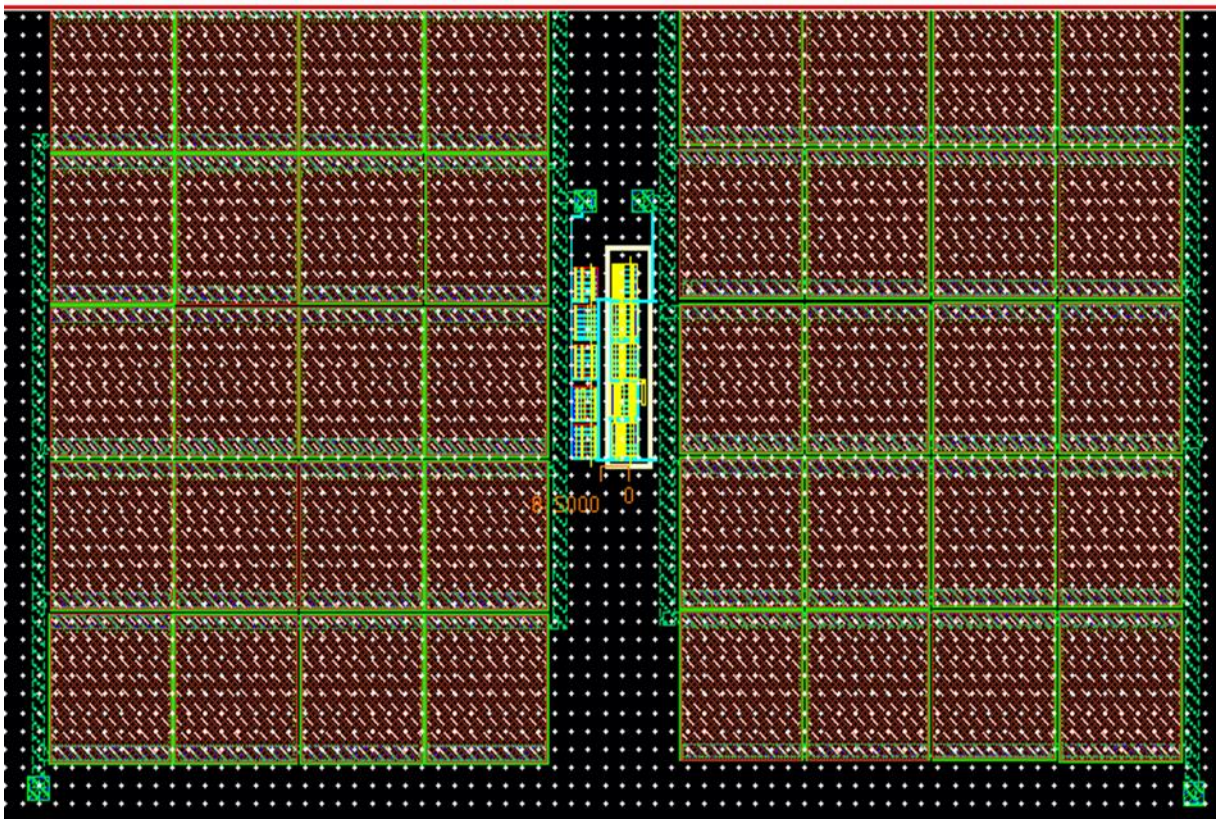


Figure 6.7: pelliconi charge pump Layout

Chapter 7 Maximum Power Point Tracking

7.1 Maximum Power Point Algorithms

In this chapter it is desirable to ensure that energy harvesting systems operate at the maximum power point of energy transducers at any time, in order to maximize the amount of energy extracted. The most important design consideration for MPP tracking in micro-scale energy harvesting systems is to ensure that minimal power overhead is introduced. This is because the output power from a micro-scale energy transducer is very limited to begin with (in the range of tens of µW to a few mW), as much of this power as possible should be delivered for use by the output loading. In this part we make overview of low overhead MPP tracking schemes that are well suited for micro-scale energy harvesting systems.

7.1.1 Reference Voltage Tracking

This maximum power point tracking method originated from empirical data analysis [**14**]. Experimental measurements on some energy transducers have found an approximately linear relationship between the MPP voltage of an energy transducer and its open circuit voltage (V_{oc}). This voltage ratio is about 0.75 for solar cells and 0.5 for thermoelectric generators. Based on the straightforward linear relationship, a simple method to estimate V_{MPP} at runtime is to momentarily disconnect the energy transducer from the load (causing an open circuit for the energy transducer) and senseV_{oc}, from which V_{MPP} can be computed. The energy transducer is made to operate at V_{MPP} by the interface circuit connected to it, which presents the appropriate load impedance to the energy transducer. This method is suitable for micro-scale energy harvesting systems because it involves simple open-loop control and does not require any intensive computations like hill climbing algorithms. The drawback of this approach is that the energy transducer is periodically disconnected from the load, which causes temporary power loss to the load. Further, there is a hardware cost (switches and control generation circuitry) involved in time multiplexing between normal operation and the open circuit mode of operation. Figure 7.1 shows a generic block diagram for the reference voltage tracking system.

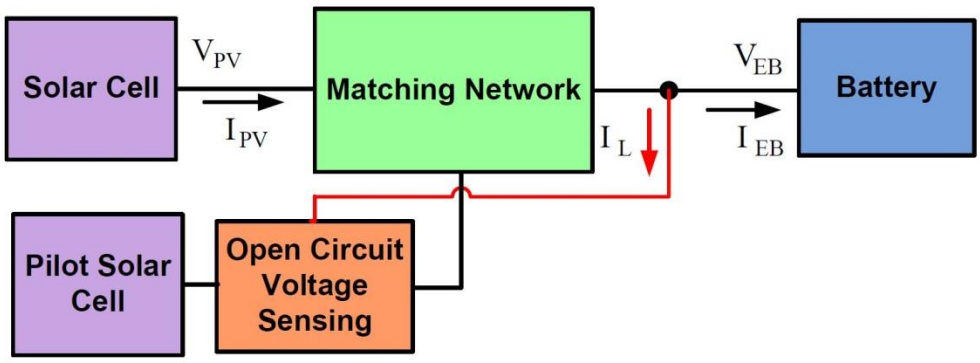


Figure 7.1: Reference Voltage Tracking System Block Diagram

To address these disadvantages, an additional energy transducer is used in the system as a pilot cell. The open circuit voltage of the pilot cell is used in place of the open circuit voltage of the main energy transducer. This eliminates the necessity for doing any open circuit voltage sensing on the main energy transducer. However, with this approach, the pilot cell should be carefully chosen to ensure that its feature is close to that of the main energy transducer. More importantly, this approach is hard to implement for system-level MPP tracking, since the system MPP voltage is no longer linearly dependent on the open circuit voltage, when the impact of a power converter is considered. Figure 7.2 shows a generic block diagram for the pilot-based reference voltage tracking system.

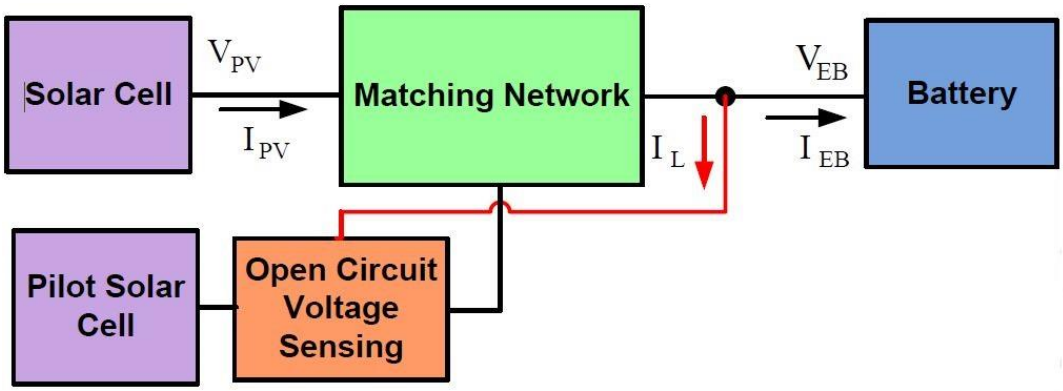


Figure 7.2: Pilot-Based Reference Voltage Tracking System Block Diagram

7.1.2 Hill-Climbing / Perturb-and-Observe

Hill-climbing and Perturb & Observe methods [**14**] essentially have the same operating principle. Both methods adopt an iterative trial-and-error approach to track the MPP. During normal system operation, an MPP tracking procedure is periodically initiated. This procedure involves applying a small perturbation to the interface circuit either by varying the duty cycle of a boost/buck converter or the switching frequency of a charge pump. This perturbation results in a small change in the operating point of the energy transducer as well as its output power. Assume, for illustration, that the perturbation results in an increase in the terminal voltage of the energy transducer. The output power is recorded and compared to the power

output before the perturbation. If the perturbation results in a power increase, another perturbation in the same direction is performed. If the perturbation results in a power decrease, a perturbation in the opposite direction is performed that results in a decrease in terminal voltage. The process is continuously repeated until the MPP is reached. In steady state, the system oscillates around the MPP. There is a trade-off in the perturbation step size. A large step size corresponds to a rapid response to the environmental energy variation and faster convergence, but oscillates with a large swing near the MPP. A small step size can minimize the oscillation swing, but slow down the tracking speed and increase the tracking time. The iterative control procedure is usually implemented in software running on a micro-controller. To minimize the power and cost overhead introduced by a micro-controller, the researchers implement the P&O algorithm using a dedicated decision generation circuit. Figure 7.3 shows a generic block diagram for the Hill-Climbing / Perturb-and Observe System. It can be shown that the control unit consists of three main blocks. The current/voltage sensing block is used for power sampling. The decision generation block is used for forcing the direction of perturbation towards the MPP. The voltage controlled oscillator is used for controlling the power converter for power matching in case of using a charge pump based power converter.

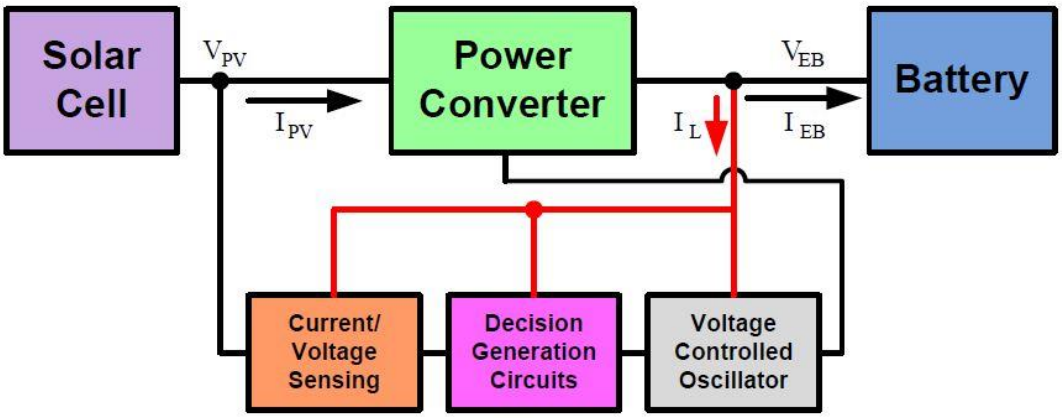


Figure 7.3: A Generic Block Diagram for Hill-Climbing / Perturb-and-Observe System

7.1.3 Analog Control Unit

The Control Unit designed in [**15**] approaches the ideal frequency-voltage relationship mentioned above. To understand how that happens; we can see that since the Op-Amp has a high open loop gain the phase voltage approximately equals the feedback voltage node. From the schematic we can also see that transistors M1, M2 and M3 in the design work as potential dividers that deliver M6 and M7's gate voltages the role of the first 3 transistors is to guarantee the sub threshold operation mode and thus consume very little power. The current Id will be mirrored to the digital side of the control unit. The right side is a ring oscillator with a frequency control M8. And the D-flip flop is used to generate a 50 percent clean square wave.

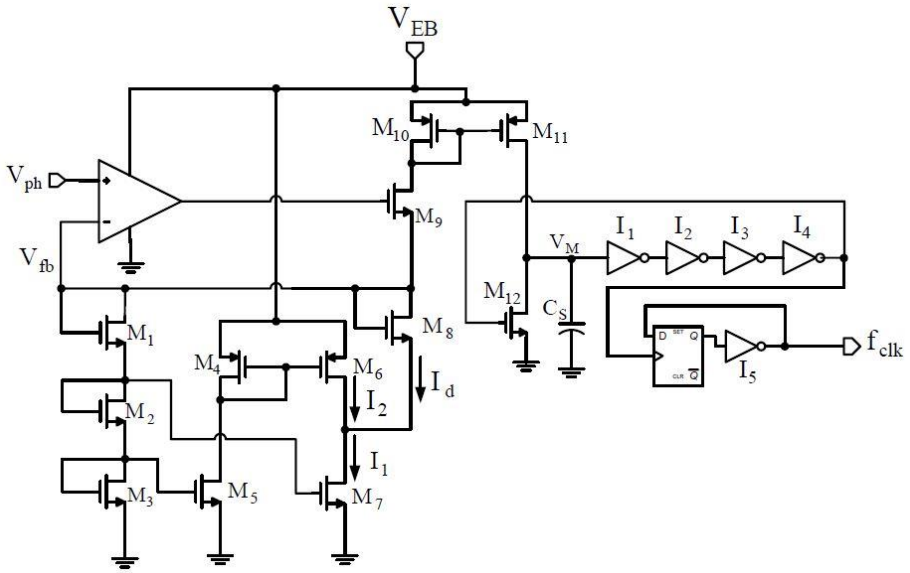


Figure 7.4: Analog control unit schematic

7.2 Maximum Power Point Tracking For Thermal Transducer

7.2.1 Circuit Mechanism

Maximum Power Point Tracking is a method used for extracting maximum available power from any module under certain conditions, as we talked about using charge pump to set up the output voltage we have found that we need to use two non-overlapping clocks to operate this charge pump therefore we need to use maximum power point control unit to make a compact relation between voltage supplied from TEG and charge pump clocks. In Figure 7.5, the proposed MPPT circuit is shown. It consists of three main blocks: voltage controlled oscillator (VCO), voltage buffer, and non-overlapping clocks circuit generator.

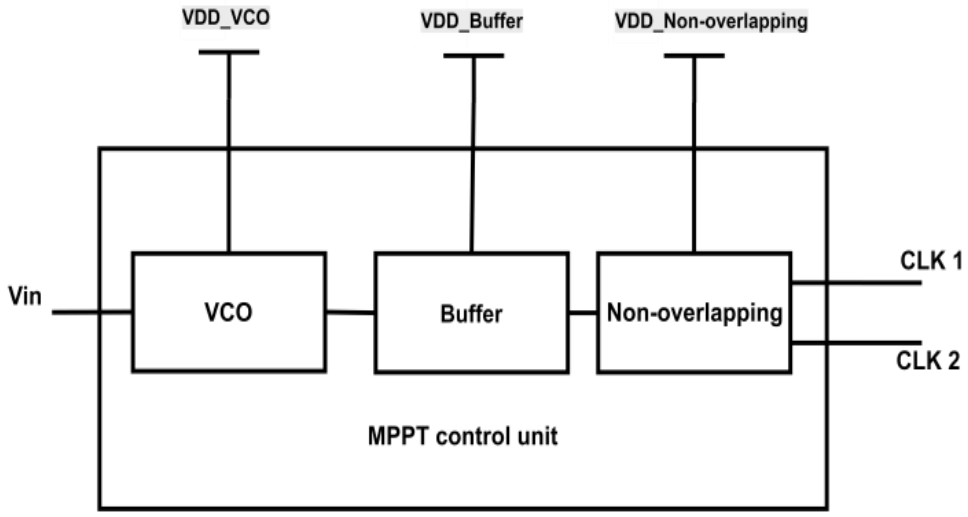


Figure 7.5: MPPT control unit block diagram

A. Voltage Control Oscillator:

As shown in Figure 7.6 the voltage control oscillator is used to sense the input voltage and generate clock which change its frequency as the change in the input voltage, the input voltage come from transducer go through the PMOS transistor gate, Therefore the output current from transistor [**16**].

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{w}{L} ((V_{SG} - V_{th})V_{SD} - \frac{{V_{SD}}^2}{2}) \quad (\mathbf{7.1}).$$

So we get that there is a relation between input voltage and output current and ratio between width and length of the PMOS transistor, when input voltage increases the output current decreases, as we use a constant input voltage equal 250 mv so the output current is directly proportional with the ratio between width and length of this transistor, Since the output frequency from voltage controlled Oscillator equal [**17**]:

$$F_{clk} = \frac{1}{2N\, t_p} \quad (\mathbf{7.2}).$$

N: no. of inverters must be odd
t_p: Average propagation delay for each inverter Therefore,
$t_p \uparrow \Rightarrow L \uparrow \Rightarrow I_D \downarrow \Rightarrow F_{clk} \downarrow$ (trade-off) [**17**]

So from equation (**7.2**), as we use this circuit in biomedical application so we want low frequency to avoid the harmful side effects of high frequencies, therefore we want to decrease the frequency and this reaches by decrease the ratio between width and length of PMOS transistor to decrease the current and increase the propagation delay or we get that when we increase number of inverters so we decrease the output frequency but we increase the power consumption and manufacturing cost.

We use buffer after VCO circuit to control the voltage level of clock oscillation.

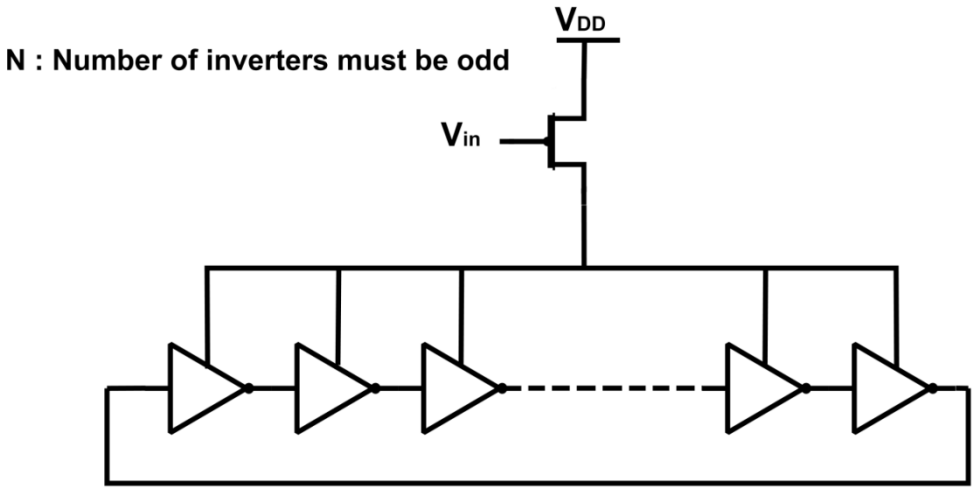


Figure 7.6: VCO circuit

B. Non Overlapping Circuit:

We used non overlapping circuit as shown in Figure 7.7 to control the charging and discharging of the capacitors used in the charge pumping circuits and prevents the switching leakage in the charge pump [**18**]. The two capacitors are alternately charged through a delay circuit connected to an oscillator with two MOSFET switches controlled by the non-overlapping signals instead of two MOS diodes.

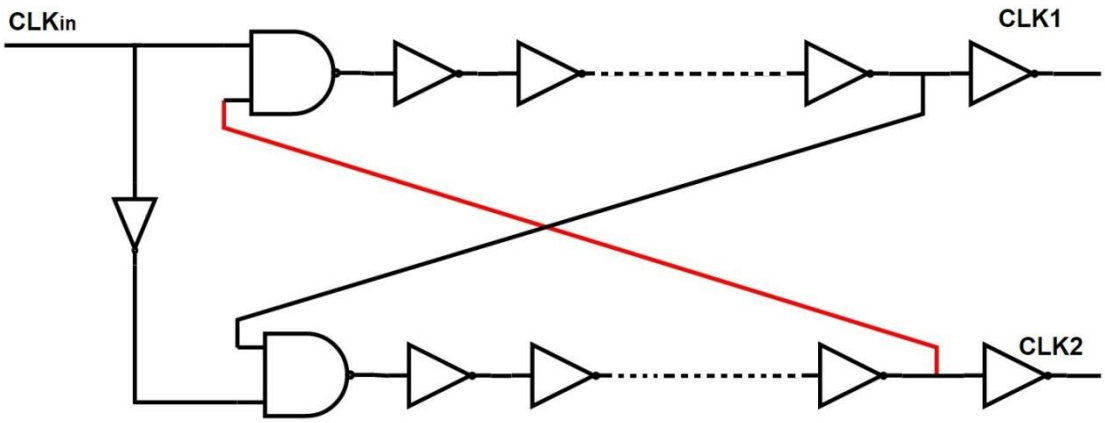


Figure 7.7: Non-Overlapping circuit

From the figure above CLK_{in} is the clock which come out from the voltage control oscillator it will enter to the non-overlapping circuit and we get two non-overlapping clocks (CLK_1 ,CLK_2) which enter to the charge pump to operate it.

7.2.2 Circuit schematics

i. VCO schematic:

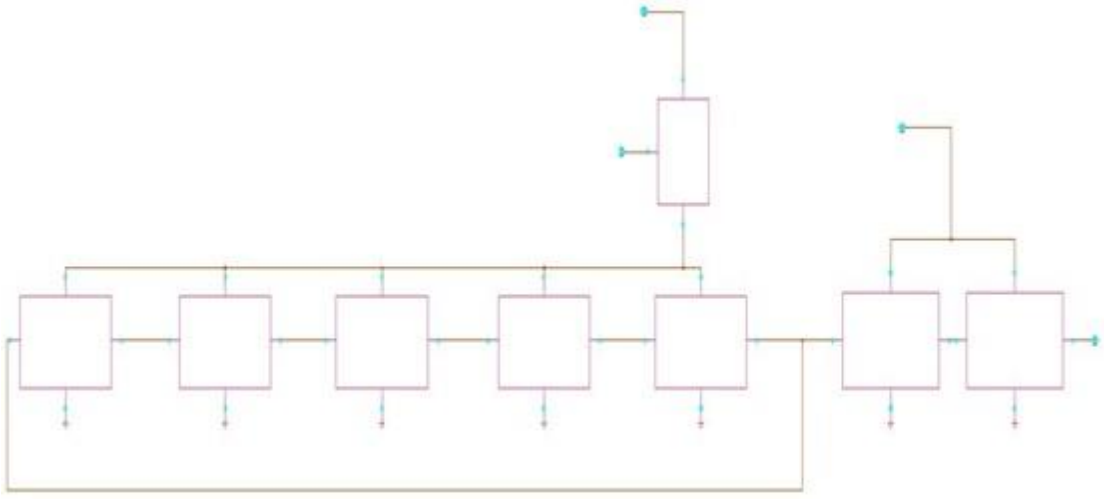


Figure 7.8: VCO circuit schematic

ii. Non-Overlapping circuit schematic:

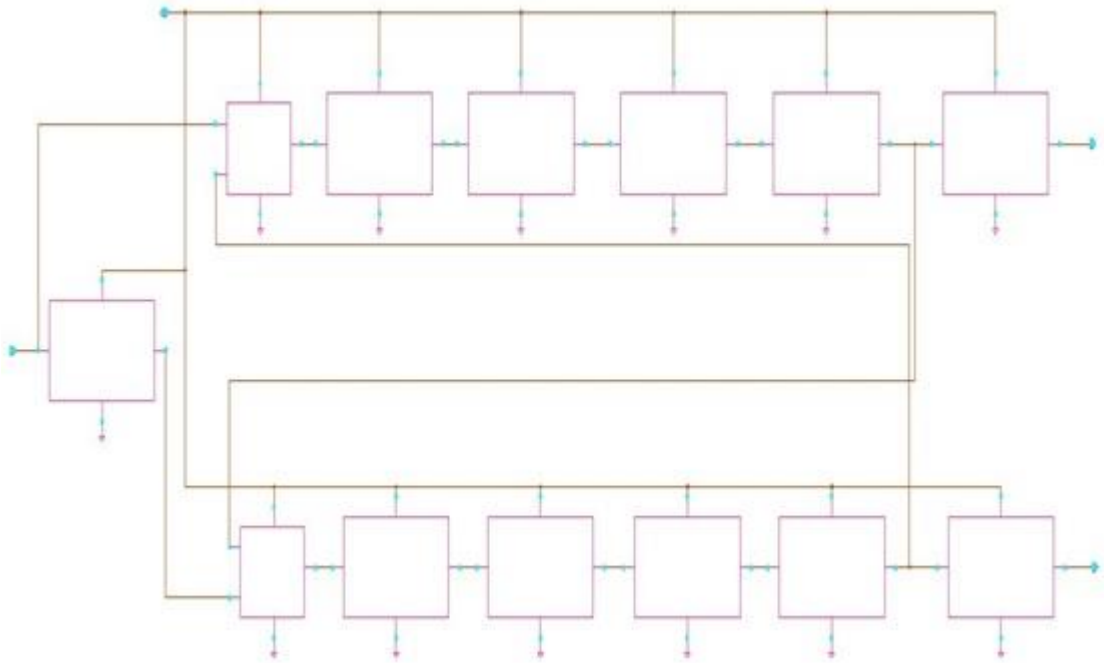


Figure 7.9: Non-Overlapping circuit schematic

iii. Control unit schematic:

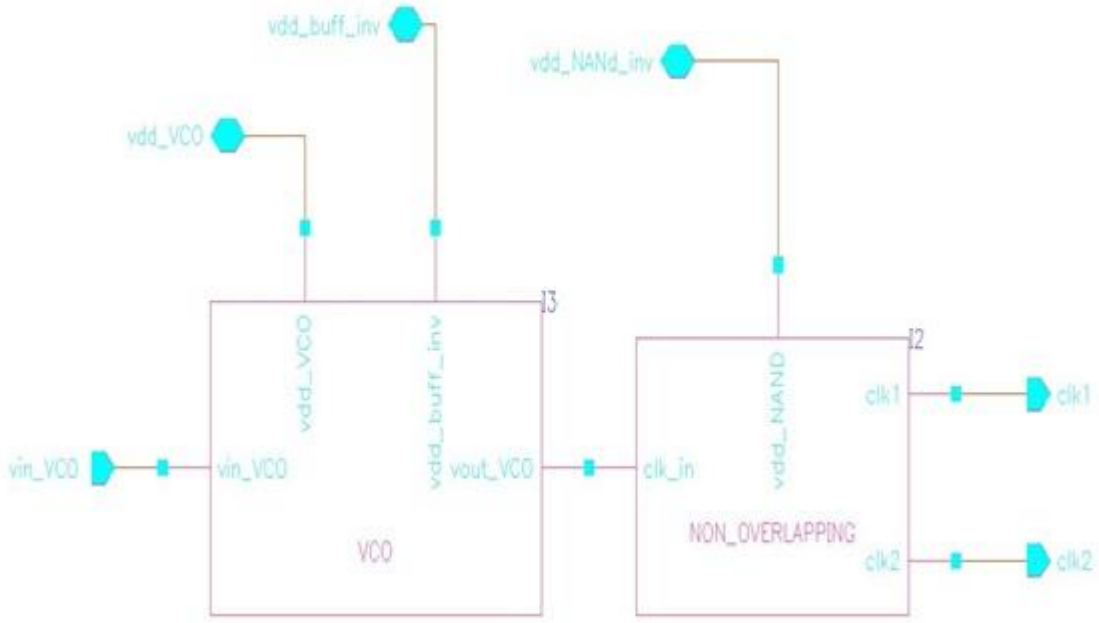


Figure 7.10: control unit schematic

7.2.3 Simulation Results

All simulation results have been done in a 0.13UMC CMOS technology. The TEG module is modeled to have output voltage 250mv:

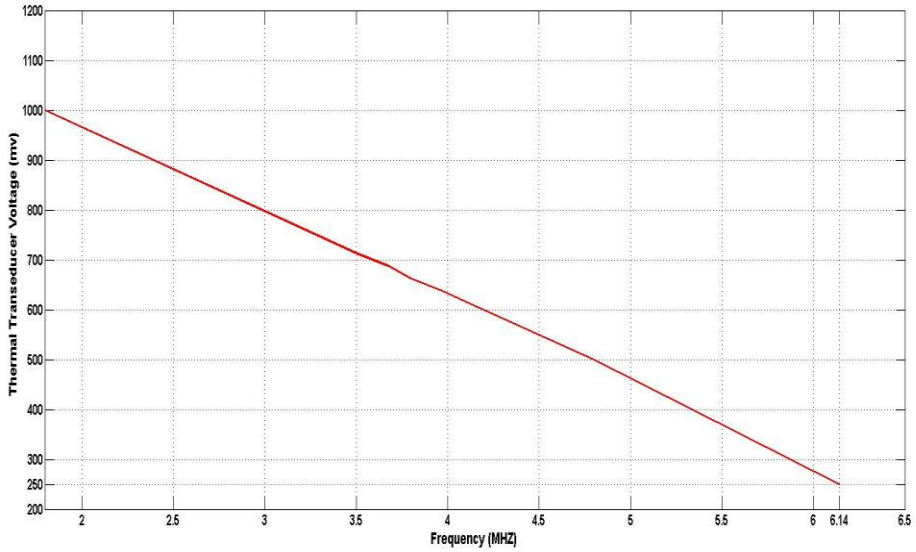


Figure 7.11: Thermal Transducer Voltage versus Output Frequency

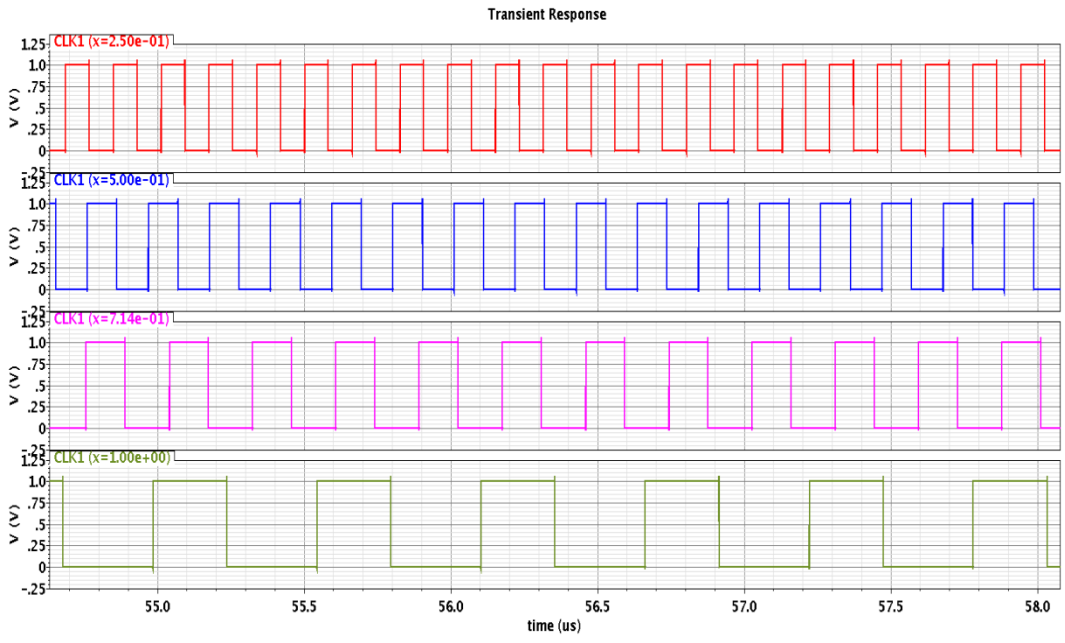


Figure 7.12: Relation between Input Voltage and Output Frequency

The above figures shows the inversely relation between the thermal transducer input voltage and the output frequency from VCO circuit.
Table 7.1 shows the relation between input voltage and output frequency and power consumed in VCO and output current from PMOS transistor. It can be shown the

inversely relation between input voltage and the output current, and the inversely relation between input voltage and output frequency from VCO.

Table 7.1: The relation between input voltage and output frequency and power consumed in VCO and output current from PMOS transistor

Input Voltage	Output Frequency	Average Current	Power Consumption
250mv	6.14 MHz	112.8µA	28.2 µw
500mv	4.8MHz	9.257µA	18.514µw
613mv	4.12MHz	7.289µA	14.578µw
638mv	3.97MHz	6.89µA	13.78µw
663mv	3.8MHz	6.484µA	12.968µw
689mv	3.67MHz	6.057µA	12.114µw
714mv	3.5MHz	5.686µA	11.372µw
1v	1.8MHz	2.08µA	4.16µw

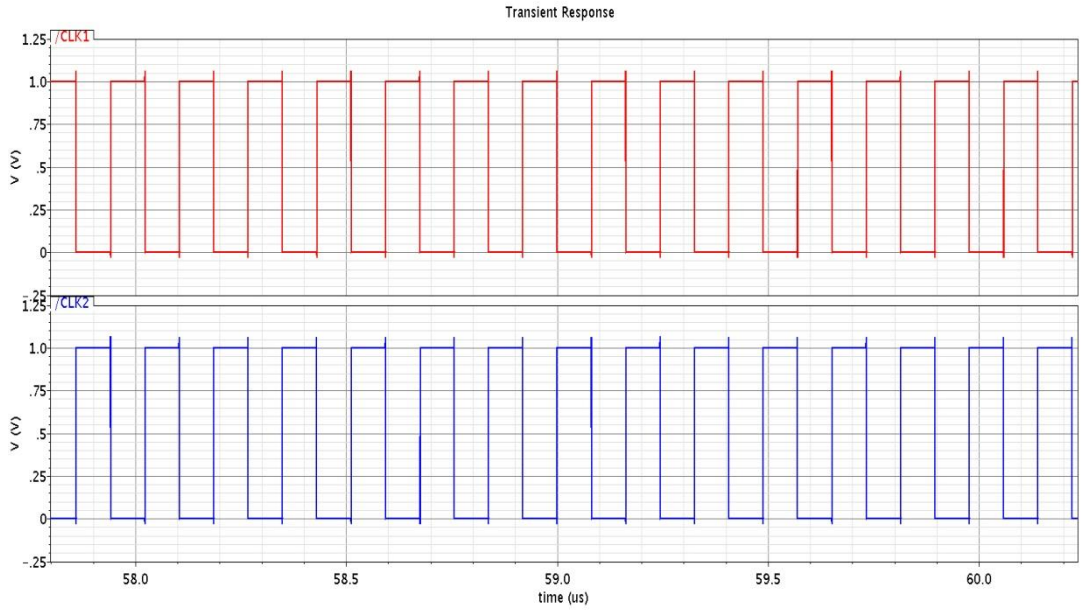


Figure 7.13: Non overlapping clocks

The above figure shows the Non-Overlapping clocks which use to operate the charge pump.

Table 7.2 shows the specifications of the MPPT control unit when TEG module is modeled to have output voltage 250mv.

Table 7.2: The specifications of the MPPT control unit

parameter	Value
V_{in}	250 mv
F_{clk}	6.14 MHz
VDD_{vco}	2 v
VDD_{buffer}	1 v
$VDD_{non-overlapping}$	1 v
P_{vco}	28.2 µw
P_{buffer}	0.118 µw
$P_{non-overlapping}$	65 µw
P_{in}	4.98 µw
PMOS transistor sizing	$\frac{610n}{600n}$
VCO inverter PMOS transistor sizing	$\frac{10\mu}{5\mu}$
VCO inverter NMOS transistor sizing	$\frac{5\mu}{5\mu}$

7.2.4 Circuit layouts

i. PMOS transistor:

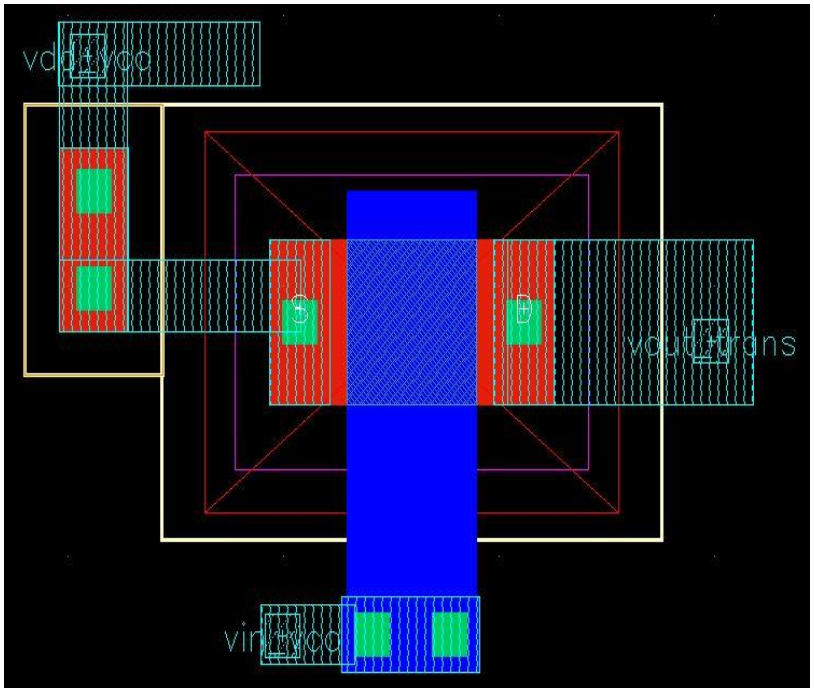


Figure 7.14: PMOS transistor layout

ii. VCO inverter:

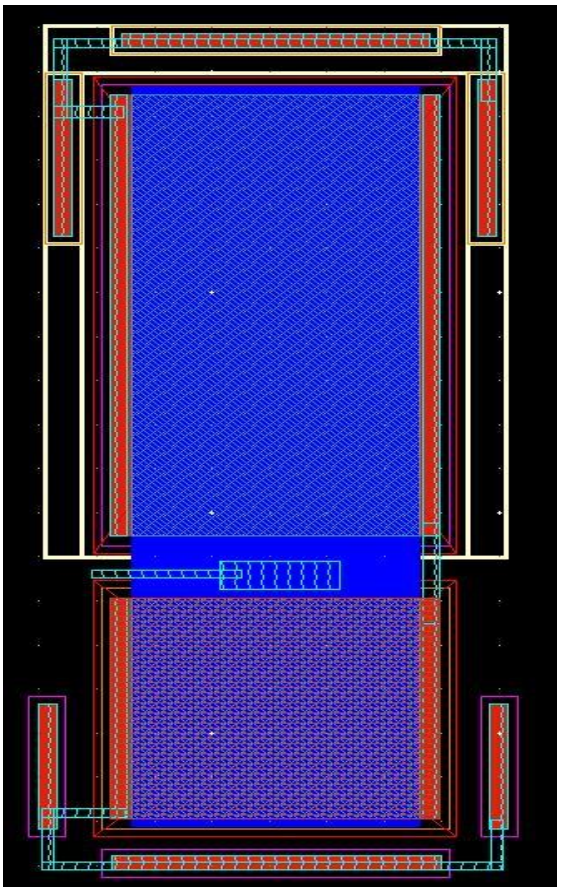


Figure 7.15: VCO inverter layout

iii. Buffer inverter:

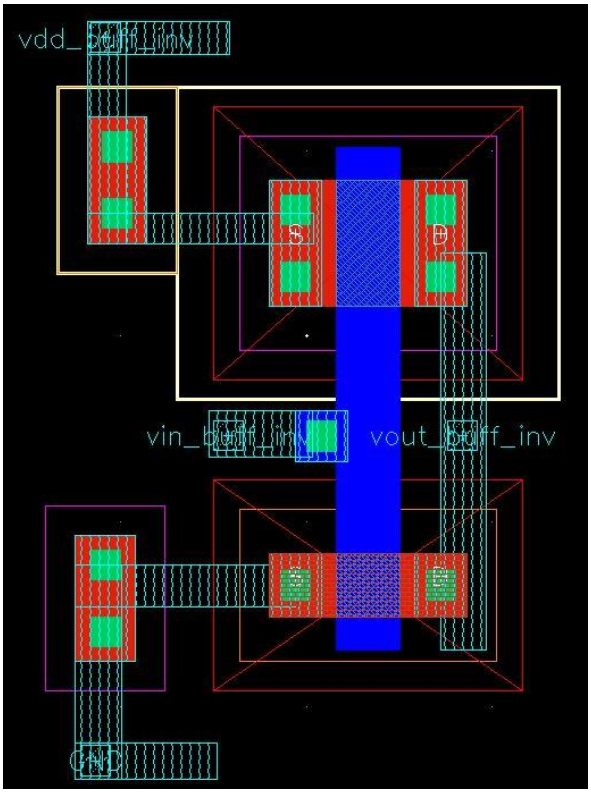


Figure 7.16: Buffer inverter layout

iv. NAND gate:

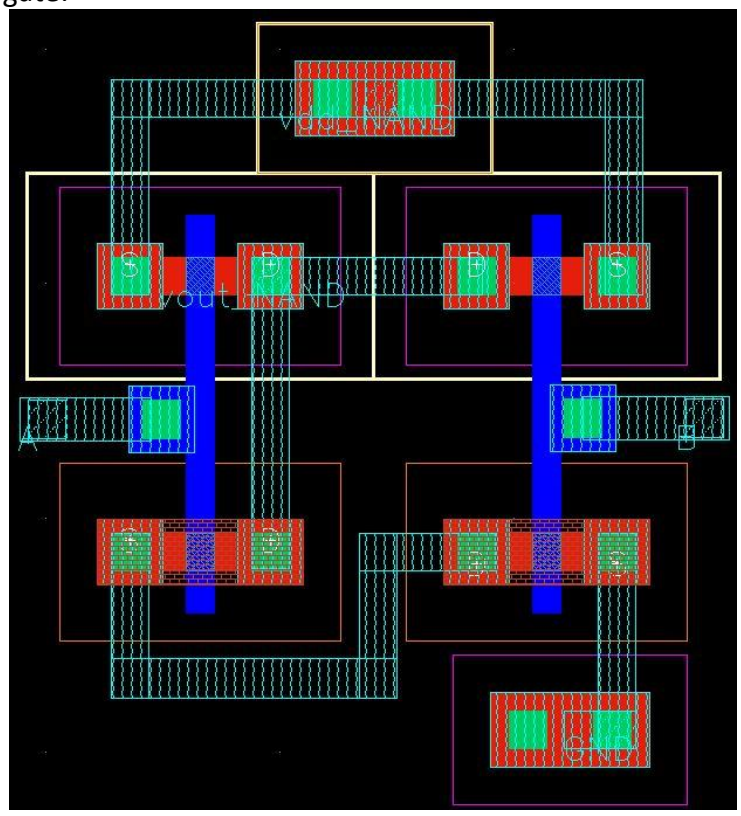


Figure 7.17: NAND gate layout

v. Non-overlapping inverter:

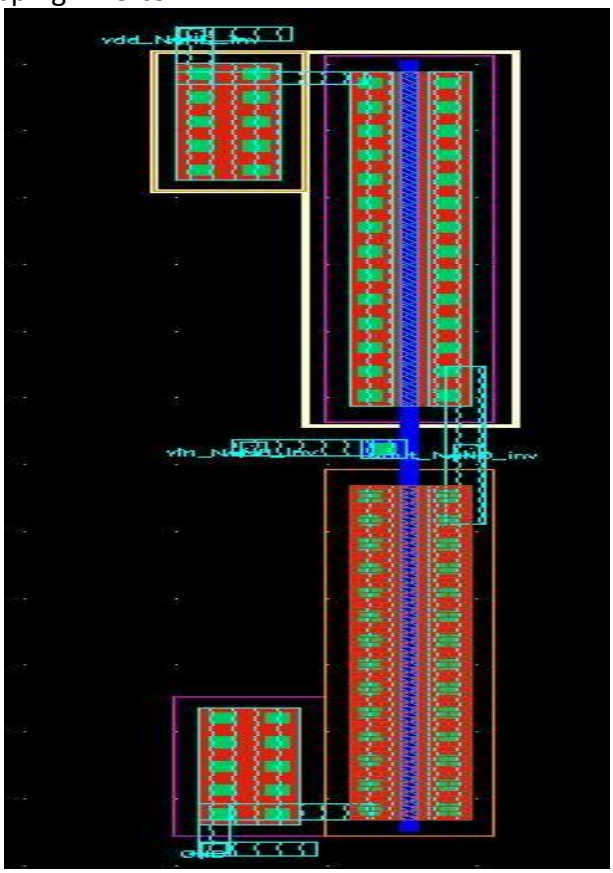


Figure 7.18: Non-overlapping inverter layout

HILL CLIMBING ALGORITHM MAXIMUM POWER TRACKING CONTROL:

To maximize power extraction from power source under all conditions and effective improve the energy conversion efficiency we have to use maximum power point tracking (MPPT) control. There is a Different efforts were done on the maximum power tracking control, (MPPT) perturb and observe algorithm is proposed here, it provided that a proper predictive and adaptive hill climbing strategy. We implement the hill climbing technique found in [20], it present an inductor-less power management system. A charge pump is used to step the voltage up output from power source to a reasonable value to charge a battery. In order to maximize the regulated output power to the battery. Based on the analysis, the system control strategy is proposed which is based on the generic hill climbing algorithm. Circuit design and low power techniques for realizing the hill climbing control is discussed which tracks the system output power value and tunes the system operating parameter to the optimal point. Where the design is mainly based on increasing the output current of the charge pump. So a current sensor is placed at the output to sample the current, then a decision generation circuit is used to find the next step whether to increase the voltage controlled oscillator (VCO) frequency or decrease it. This architecture is good in terms of tracking efficiency, as it‘s a tracking system that adapts itself to the new operating point.

7.3 OVERALL CIRCUIT DESCRIPTION

The block diagram of the proposed system is shown in Fig. 7.19. The optimal power tracking unit monitors the charge pump output power and generates the decision to adjust the system operating parameter. Based on the decision, the control unit tunes the operating frequency of the charge pump in order to maximize the system power output.

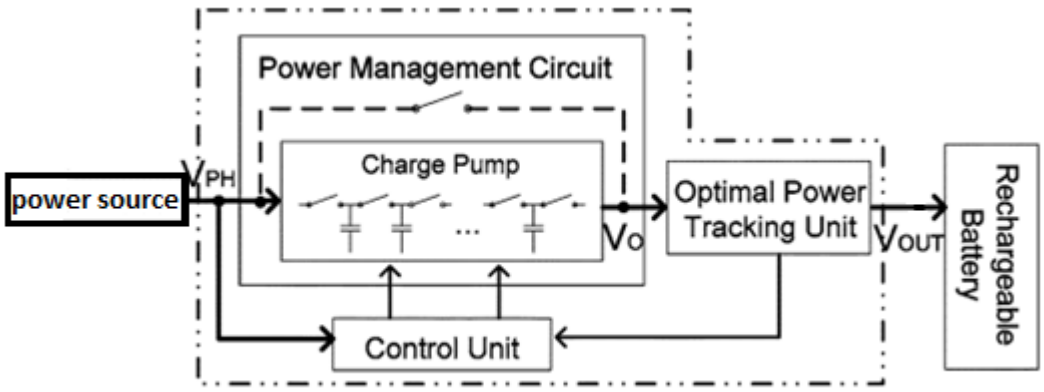


Figure 7.19: Block diagram of the power management system.

7.3.1 Optimal Power Tracking Unit

In order to obtain the maximum output power from the system, the optimal power-tracking unit is used to monitor the amount of power flowing out of the charge pump and determine how to adjust the system operating parameters to operate the system at the MPP. Here a generic hill climbing algorithm is implemented and the detail circuit design will be discussed in 7.4 [20].

7.3.2 Control Unit

The control unit is used to tune the system operating parameters based on the adjusting decision from the optimal power tracking unit. The charge pump switching frequency has a profound impact on the charge pump input impedance and the system power loss, and hence the system output power is directly related to it. Thus, a VCO is used to generate a variable clock frequency for the charge pump. The circuit is shown in Fig. 7.21. Vvco is the adjusting decision signal from the optimal power tracking unit which determines the switching frequency to be outputted through the inverter chain $I_1 \sim I_6$. An edge-triggered D-flip-flop readjusts the duty cycle of the clock and then sends it to the charge pump [20].

7.3.3 Battery

The battery acts as a voltage clamper which clamps the charge pump output voltage to the battery voltage. Here, the battery voltage can be considered to be constant in a short window of time when comparing to the power sampling period of the tracking unit. As a result, maximizing the system output power is equivalent to maximizing the charge pump output current. Based on this, our control strategy is to maximize the charge pump output current [20].

7.4 OPTIMAL OUTPUT POWER CONTROL

Fig. 7.20 shows the circuit of the optimal power tracking unit. The unit monitors the charge pump output current and generates the adjustment signal to the control unit to change the switching frequency so that the system operates around the maximum output power point. The optimal power tracking unit contains two parts. Since the main objective is to maximize the system output current, a current sensor is used to sample the charge pump output current. By comparing the current sample with the previous sample, the decision generation circuit can decide whether the sampled value is the maximum and then generates the corresponding voltage to the VCO to adjust the charge pump switching frequency accordingly [20].

7.4.1 Current Sensor Circuit

The current sensor proposed in [21] is used in the tracking unit and the circuit is shown in Fig. 7.20 (a). With a small biasing current flowing through the transistors MN1 and MN2, the drain voltages of MP1 and MP2 are clamped to the same value. Due to the size ratio of the transistors MP1 and MP2, about 1/N of the total charge pump output current flows to the resistor Rs. Hence the charge pump output current level is reflected by the voltage (Vs) across the resistor Rs. The rest of the output current would flow to the battery through MP2 at node Vout. Since the output current from the charge pump is in pulse shape, a smoothing capacitor is connected to the node Vo to obtain a smooth current profile for the accurate measurement of the average value of the output current through the current sensor [19].

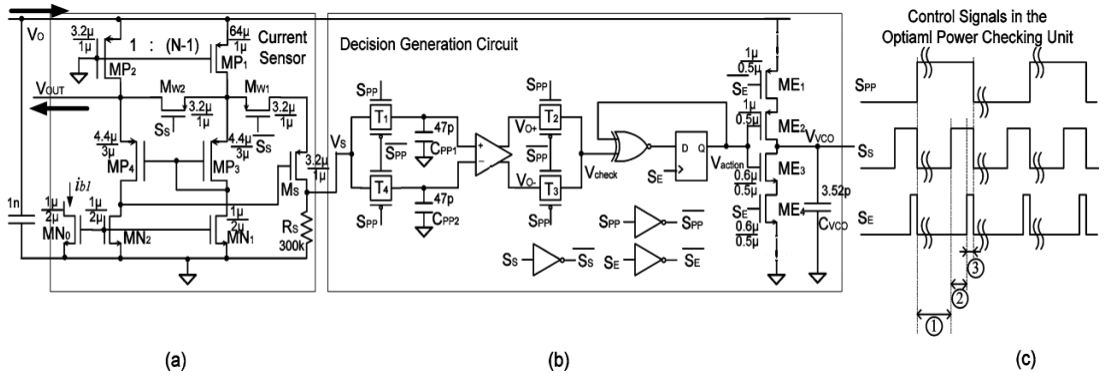


Figure 7.20: Circuit and control signals of the optimal power tracking unit. (a) Current sensor circuit. (b) Decision generation circuit. (c) Control signals in the optimal power tracking unit [normal working phase (1), current sensing phase (2), evaluation phase (3)].

7.4.2 Decision Generation Circuit

In the decision generation circuit shown in Fig. 7.20 (b), the current sensed Vs value and the previous value are stored in the sample capacitors, CPP1 and CPP2, alternatively. If CPP2 holds the previous value, the transmission gates T3 and T4 are off while T1 and T2 are on. The current sensed Vs will be stored in CPP1, and Vcheck will output the comparison results from Vo+ of the comparator. Vcheck is equal to logic '1' if the current sample value (the new sample) is larger than the previous one (the old sample). In the next sample period, T1 and T2 will be turned off while T3 and T4 are on, and CPP1 holds the old sample while CPP2 stores the current Vs value (the new sample). Vcheck will output the comparing results from Vo- for this sample period. This value is XNORed with the previous adjustment decision which is stored in a D-flip-flop and the new decision value Vaction will be updated at the rising edge of the control pulse SE. The logic value of the decision signal Vaction indicates whether we should increase or decrease the charge pump switching frequency. Depending on the Vaction logic value, the capacitor Cvco is either charged through transistor ME1, or discharged through transistor ME4, during the control pulse interval of SE. In this way, the voltage of Vvco is either increased or decreased and it is then sent to the control unit to adjust the switching frequency through the VCO. Usually, the power source not changes very rapidly and the system output current will not change so quickly. At the same time the power tracking unit consumes some power when the system is operating. To reduce the power overhead,

we can reduce the tracking sampling rate. During each sampling period, the current flowing though the sensing resistor Rs and the comparator will become useless after the Vvco adjustment decision is made and this current loss should be avoided. Here, transistors MW1, MW2 are used to disable the current sensor when no sensing is needed. When we sample the charge pump output current, MW1 is on, MW2 is off. The current sensor is enabled and the comparator outputs the checking results of the sensed current value. After the decision is made at Vaction, the power tracking unit is disabled by turning off MW1. The transistor MW2 is on and the sensing current through transistor MP1 will flow to Vout instead of Rs. Thus the charge pump output current can be almost totally transferred to the battery [19].

7.4.3 Timing Diagram

The optimal power tracking unit operation can thus be divided into 3 phases during each sample period, which is shown in Fig. 7.20(c). Here, the sample period means the time interval between 2 consecutive frequency adjustments. During each period, the transmission gate control signal SPP is either high or low, which determines whether the previous sampled Vs or the current one is stored in CPP1 or CPP2, and whether Vo+ or Vo- of the comparator will output the checking results. After each frequency adjustment, the tracking unit is disabled so that all the charge pump output current can flow to Vout. We denote this as the normal working phase. At the end of the normal working phase, sensor control signal SS will activate the optimal power tracking unit where the charge pump output current is sensed and the current changing is checked at node Vcheck. We denote this as the sensing phase. After some delay, the tracking unit enters the evaluation phase in which a pulse SE is generated. Decision signal is updated in the D_flipflop and the capacitor Cvco is charged or discharged during the SE pulse interval according to the generated decision. After that, the operation goes back to normal working phase again. With a lower sample rate, longer time will be occupied by the normal working phase in each sample period, and the average power overhead of the tracking unit is reduced. [19].

7.5 CONTROL UNIT

The output current of charge pump is proportional to operating frequency, the equivalent input impedance Rin of the power converter is the input impedance of the charge pump is inversely proportional to the operating frequency. It should be noted also that this impedance is matched to the power source, so as power source has a corresponding matched impedance value for maximum power. This impedance value has a corresponding frequency value, so the goal of the control unit is to search for the optimum frequency value that delivers maximum power at a given input power from source [14].

7.5.1 Control Unit Circuit Description

The Control Unit circuit shown in Figure 7.21. It translates the Vvco voltage change into a current change through the feedback Amplifier (i.e., the OTA), OTA is force it's two terminals to be equal, so the voltage drop on the resistance Rf is equal Vvco and current flow through resistance Rf is equal Vvco over Rf, that current is mirrored by the current mirror to the right side. The right part is the digital section, it is a current controlled ring oscillator. The frequency tuning is controlled by the charging current of the capacitor (*Cf*), value of capacitor and resistance Rf. Since the output of the ring oscillator has a very small duty cycle (<10%), the output D-flip flop and the inverter are used to produce a 50 % duty cycle clock.

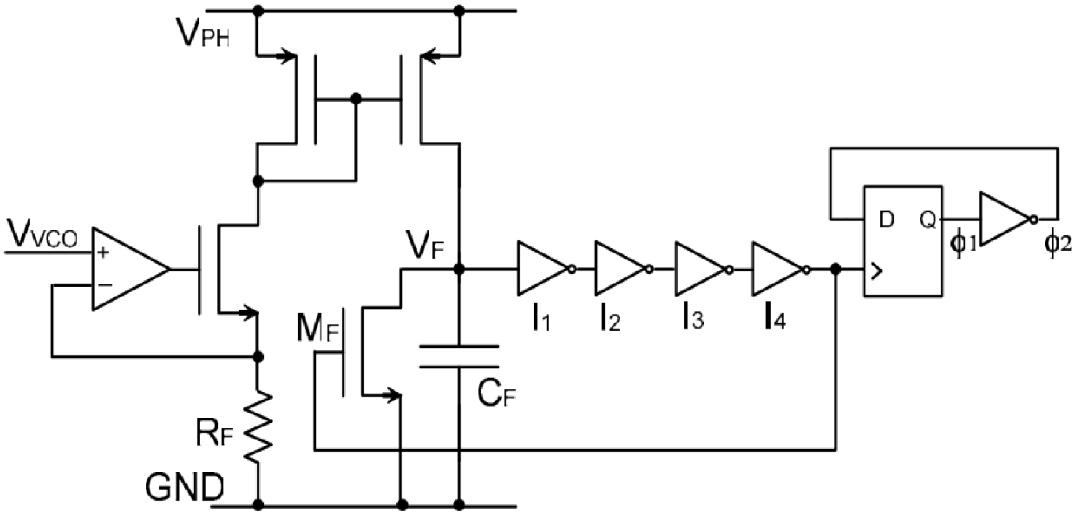


Figure 7.21: control unit for the charge pump

7.5.2 OTA Design

The Op-Amp used in the design is a typical single stage common source amplifier shown in Figure 7.22. The design of the amplifier is targeting large open loop gain and phase .as the power is critical we decrease the bias current which result in reduction in unity gain bandwidth but this decreasing does not effect on our circuit as it work on low frequency .

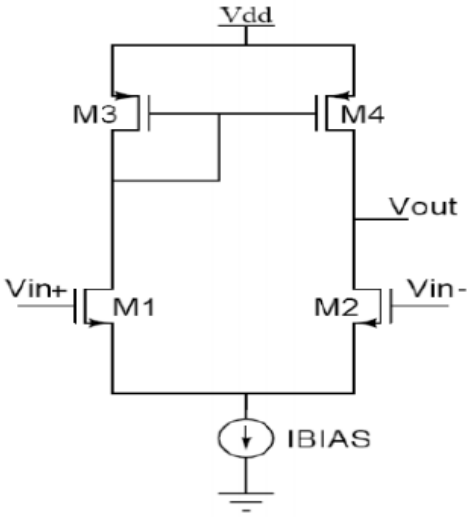


Figure 7.22: Architecture of OTA.

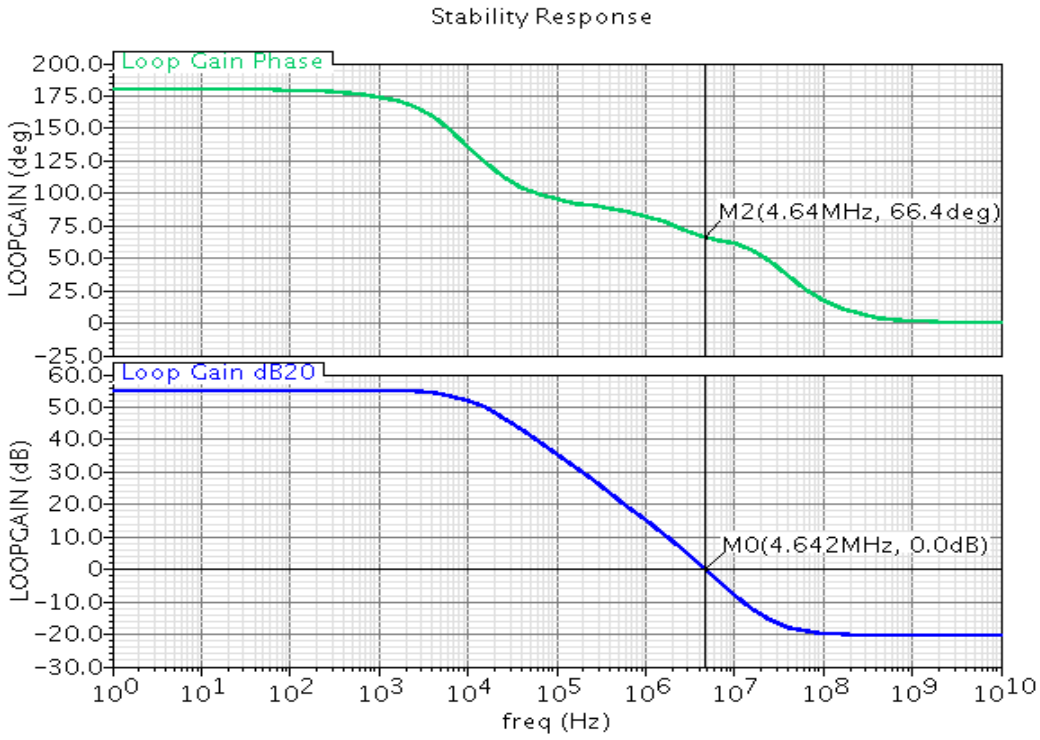


Figure 7.23: Gain Response and Phase Response of the (OTA) used in the

Figure 7.23 shows the gain response and phase response of the (OTA) architecture used. The voltage gain is around 55*dB*, unity gain bandwidth is equal 4.64*MHz*, phase margin is equal to 66.4 degree◦ I bias used is equal 300nA , average current from voltage source is equal to 600nA and 3.3V voltage source is used . and the power consumption is equal to P avg = VDD * Avg current = 3.3V * 0.6uA = 2uW , It can be illustrated that the loop is stable, since the loop phase margin is equal to 66.4**.**

7.5.3 Flip-flop Design

The flip-flop adopted in the design is the true single phase clock based flip flop (TSPC). The design is based on [22]. True Single Phase Clocked (TSPC) register is implemented for the D-flip flop in order to reduce the number of transistors and also its power consumption. So this topology has many advantages, it works at high speeds, and it occupies small area and it consumes low power. The sizing of the pull up network is almost double the size of the pull down network .The design of the TSPC flip flop is shown in Figure 7.24 [14].

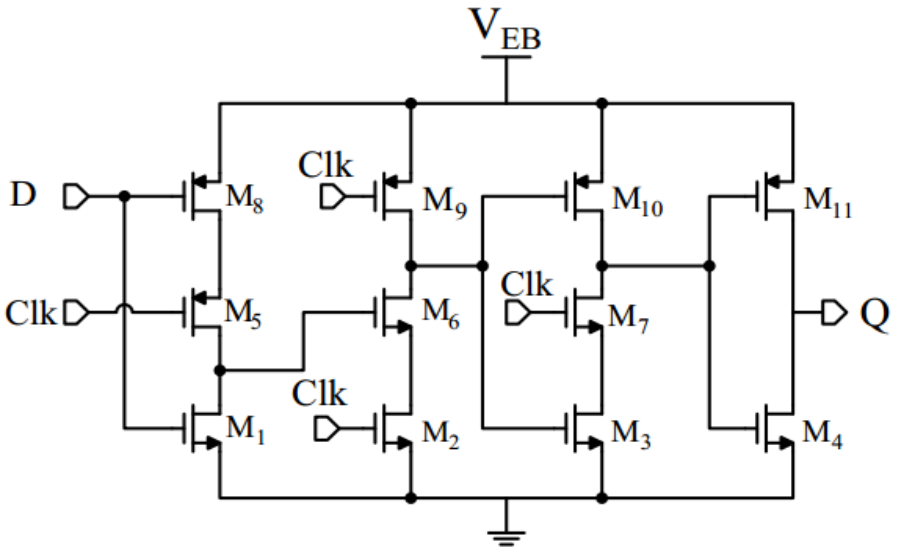


Figure 7.24: True Single Phase Clock based D-flip flop used in the Design

7.6 SIMULATION AND RESULTS

The most important metric in the design of the energy harvesters is the power consumption of the MPPT control, as this metric greatly affects the efficiency.

Current Sensor Circuit Results

First we use design parameter N equal 8, N the size ratio of the transistors MP1 and MP2, about 1/8 of the total charge pump output current flows to the resistor Rs, 25nA biased current used, resistance Rs equal 100K ohm. Obtained result is shown in figure , when we increased input current Vs is increased.

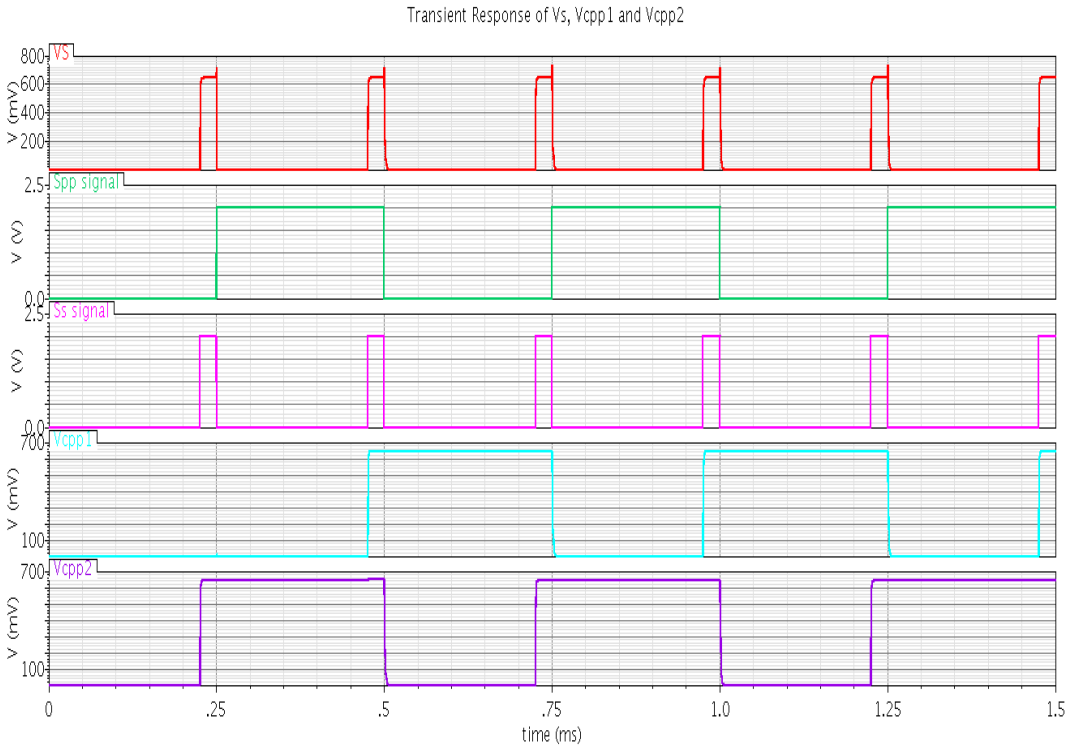


Figure 7.25: voltage drop on resistance RS with Vcpp1 and Vcpp2

Figure 7.25 show the output of current sensor 1st shape in figure is voltage drop Vs (red color line) on resistance Rs, 2nd shape is Spp signal, 3rd shape is Ss signal (the signal that we sample the current during it), 4th shape is voltage drop on capacitor Cpp1 on decision generation circuit, 5th shape is voltage drop on capacitor Cpp2 on decision generation circuit.

We reduced power consumption , 1st by increasing sizing ratio between transistors MP1 and MP2, 2nd by decreasing sampling time of current to 10% of time, there is a constrains on this techniques time of sample must be large enough to capacitor can charge and discharge and comparator can compare between two signal of Vcpp1 and Vcpp2, and sizing ratio have to be enough to differ between two sample as if input current is increase slightly and sizing ratio is large different between two sample will

be very small and comparator result will not be accurate, if we decrease sizing ratio that has a bad effect on Vs voltage as Vs can increase to supply voltage and we can't see increasing of input current and comparator result will be false.

7.6.1 Decision Generation Circuit Results

We change the applied input current flowing through current sensor as shown in figure the curve of red color from 50uA to 100uA.

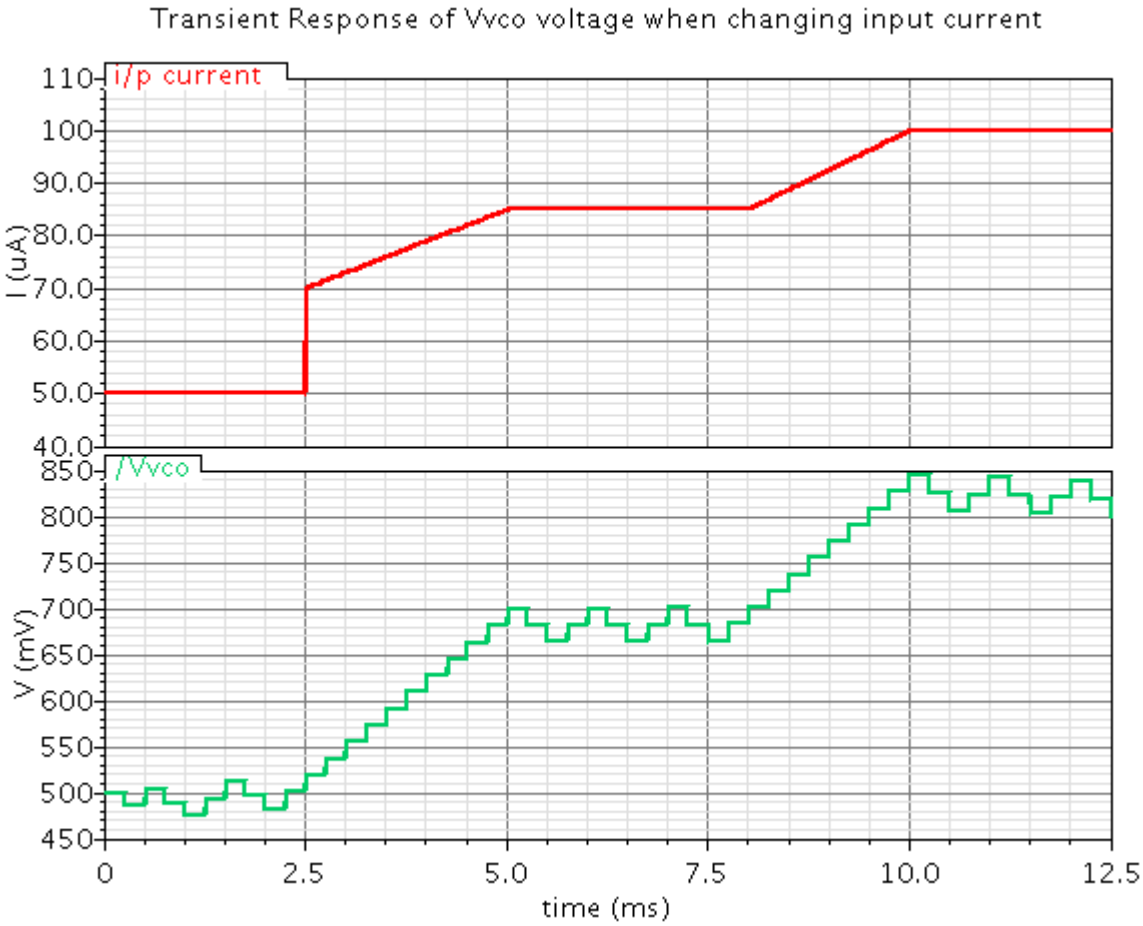


Figure 7.26: output voltage Vvco from decision generation circuit when changing input current of the current sensor

Figure 7.26 show changing in Vvco voltage (green line) when the input current is changed (red line), changing input current corresponding to changing of input power.

TABLE.7.3: The power consumption and efficiency of current sensor and decision generation circuits

Input current	Supply voltage	Input power	Output current	Output power	Power consumption	Efficiency η $\frac{\textbf{power output}}{\textbf{power input}}$
51.56uA	2.3	118.58	50uA	115uW	3.58uW	96.98%
102.9uA	2.3	236.67	100uA	230uW	6.67uW	97.18%
153.4uA	2.3	352.82	150uA	345uW	7.82uW	97.78%
173.6uA	2.3	399.28	170uA	391uW	8.28uW	97.926%

Table 7.3 show that efficiency is around 97%-98% and efficiency increased with increasing input power, current sensor can work with current range from 10uA to 180uA, if we want to increase this range we have to change some design parameter we discussed before, input current range depend on your power source, as you have to design the MPPT control circuit according to your source, you have to know your range of power you can get from source and the range of current to design the design parameter discussed before resistance Rs , sizing ratio between the transistors MP1 and MP2, sampling time and capacitors values.

7.6.2 Control Unit Circuit Results

The most important metric in the design of the energy harvesters is the power consumption of the control unit, as this metric greatly affects the efficiency. Decreasing the frequency range of operation and the supply voltage leads to significant reduction of the dynamic power, in return the whole power consumption decreased. The power consumed in the control circuit is divided into two portions, static power comes from the left side (i.e. analog part), which is responsible for voltage to current conversion, dynamic power comes from the right side (i.e. digital part), which is responsible for current to frequency conversion.

To get low power consumption in control unit, some techniques used to achieve that, 1^{st} reducing biased current of op-amp that affect on unity gain bandwidth but that is no matter on our circuit as it work on low frequency, 2^{nd} increasing the value of the resistance to decrease current taken from supply as I = V/R, when we increasing R

and voltage is equal Vvco current will reduced, 3rd increasing length of first inverter in the chain of inverters used to generate frequency as the first one work on threshold phase not as an inverter, it consume much power as I = V/R and r0 resistance of transistor increasing with increasing of transistor length but that affect on frequency as it decrease it so compromising between them we can get best sizing .

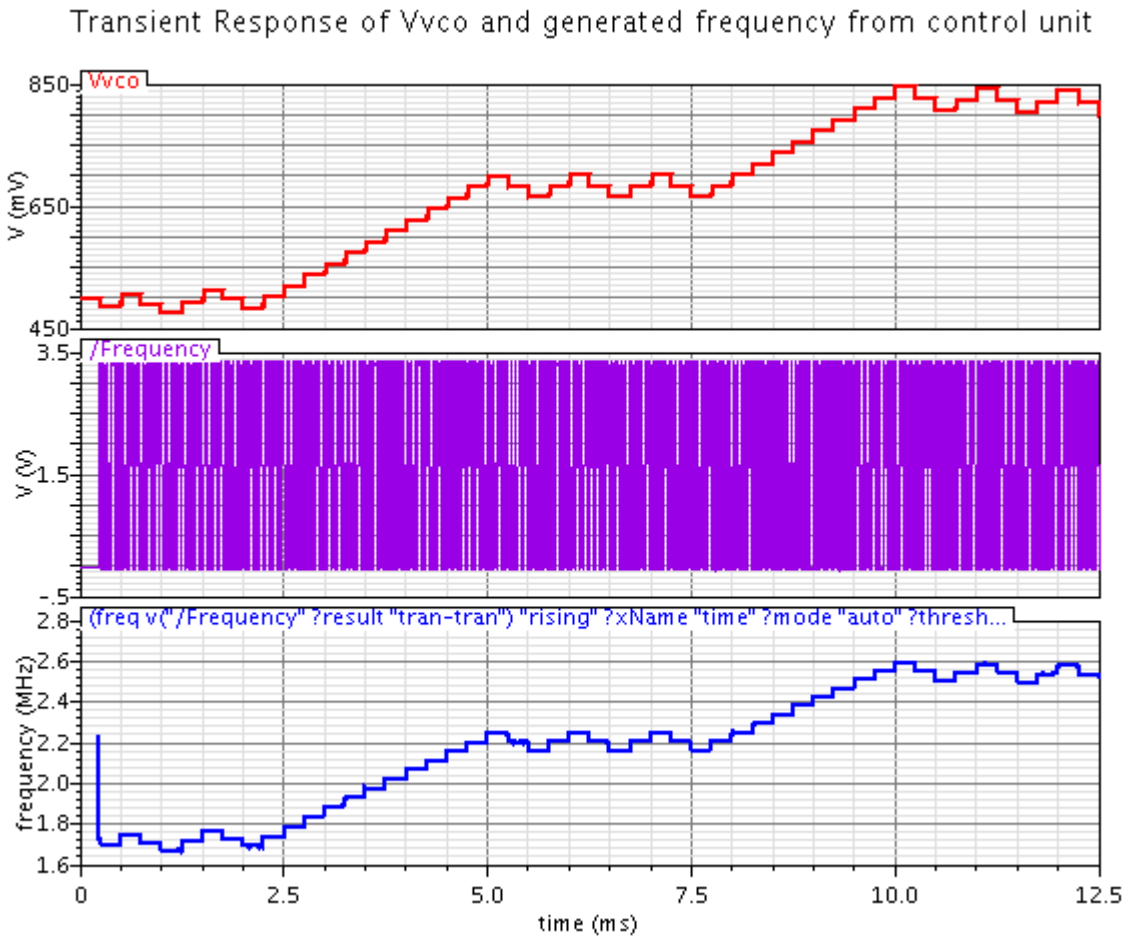


Figure 7.27: generation frequency corresponding to changing in VCO voltage

Red line in figure 7.27 is the Vvco voltage, blue one is the generated frequency from control unit and red one is the generated frequency in time domain.

Table.7.4: Vvco voltage and corresponding generated frequency, power consumption of control unit.

Vvco	Generated frequency	Supply voltage	Current taken from supply	Power consumption
0.1 v	516 kHz	3.3 V	12.3uA	40.59uW
0.2 V	858.1 kHz	3.3 V	13.6uA	44.88uW
0.3 V	1.17 MHz	3.3 V	14.94uA	49.3uW
0.4 V	1.47 MHz	3.3 V	16.38uA	54.05uW
0.8 V	2.498 MHz	3.3 V	21.33uA	70.39uW
1 V	2.954 MHz	3.3 V	23.7uA	78.21uW
1.2 V	3.39 MHz	3.3 V	26.11uA	86.16uW
1.5 V	4 MHz	3.3 V	29.67uA	97.91uW

Table.7.4 show that the power consumption is proportional to frequency generated which is corresponding to Vvco voltage. power consumption can be reduced by using low supply voltage. Due to high power consumption of control unit it reduced the efficiency of the overall system it is preferable to use it with high power sources to get sufficient efficiency.

7.6.3 Process Corner Simulation Results

Process corner simulation done to show how performance of the system in case of variation of fabrication process, current sources, voltage sources, temperature and show how this variation affect on expected output. Figure show the simulation output after applied corners. We change voltage and current sources by ±10%, temperature form -40 to 70 degree, tt, ss and ff processes. By changing biased current of matched current source (22 , 25 , 28) nA, changing biased current of op-amp (270 , 300 ,330) nA, changing voltage source (2.1 ,2.3, 2.5) V , temperature (-40 , 0, 27 , 70) degree .

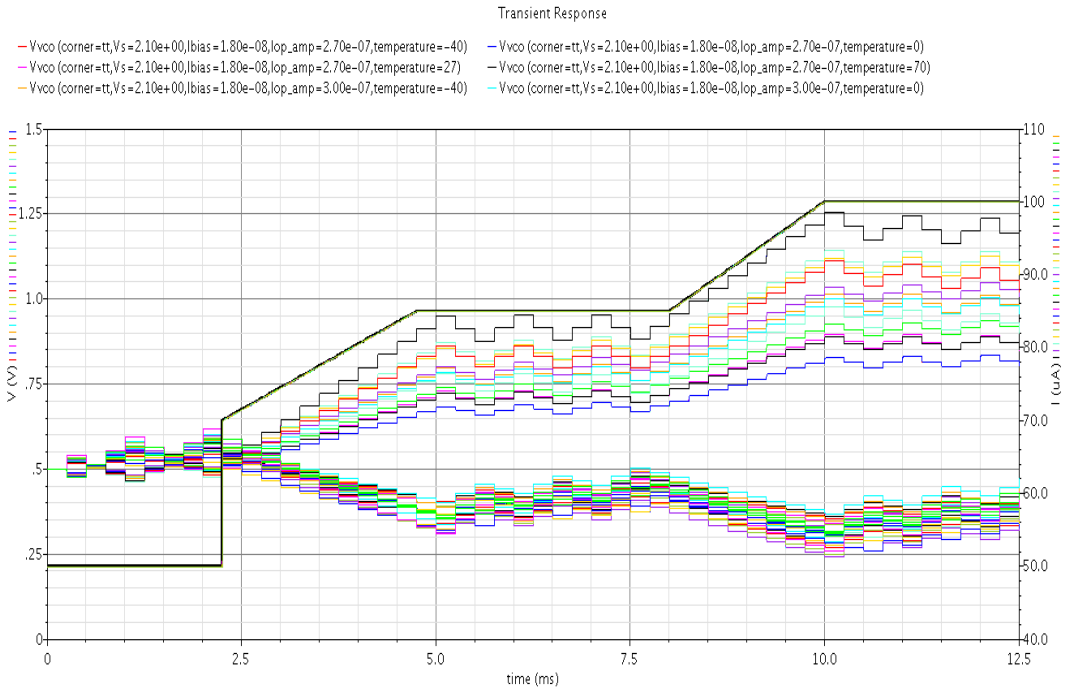


Figure 7.28: output voltage Vvco from decision generation circuit when changing input current of the current sensor in different corner variation

As shown in figure 7.28 curve with black color is the input current to current sensor and other curves is the Vvco voltage, all output is right, according to hill climbing algorithm the new decision is taken dependent on the previous decision as discussed in 7.4.2 if the new decision is '1' mean that the power is increased than the old value the D-F-F keep its output so in the above figure curves that Vvco discharge to ground the last decision taken before input current increase is to discharge capacitor, so when it sample the new value of comparator output is high mean the new value is larger than the old mean that power is increased so it is closed to MPP, so D-F-F keep it's old value which is discharging capacitor and the next sample is larger than the old one so it keep discharging and this is the idea of hill climbing algorithm. But what make that different between above curves? the time when there is any change in input current the output of the comparator cannot be determined because it's two terminals is equal so this is the reason that make difference between above curves as the MPPT control circuit not integrated with charge pump so there is no feedback to show the effect of changing of Vvco on the input power.

7.7 SCHEMATICS

7.7.1 Schematic Of Current Source Circuit

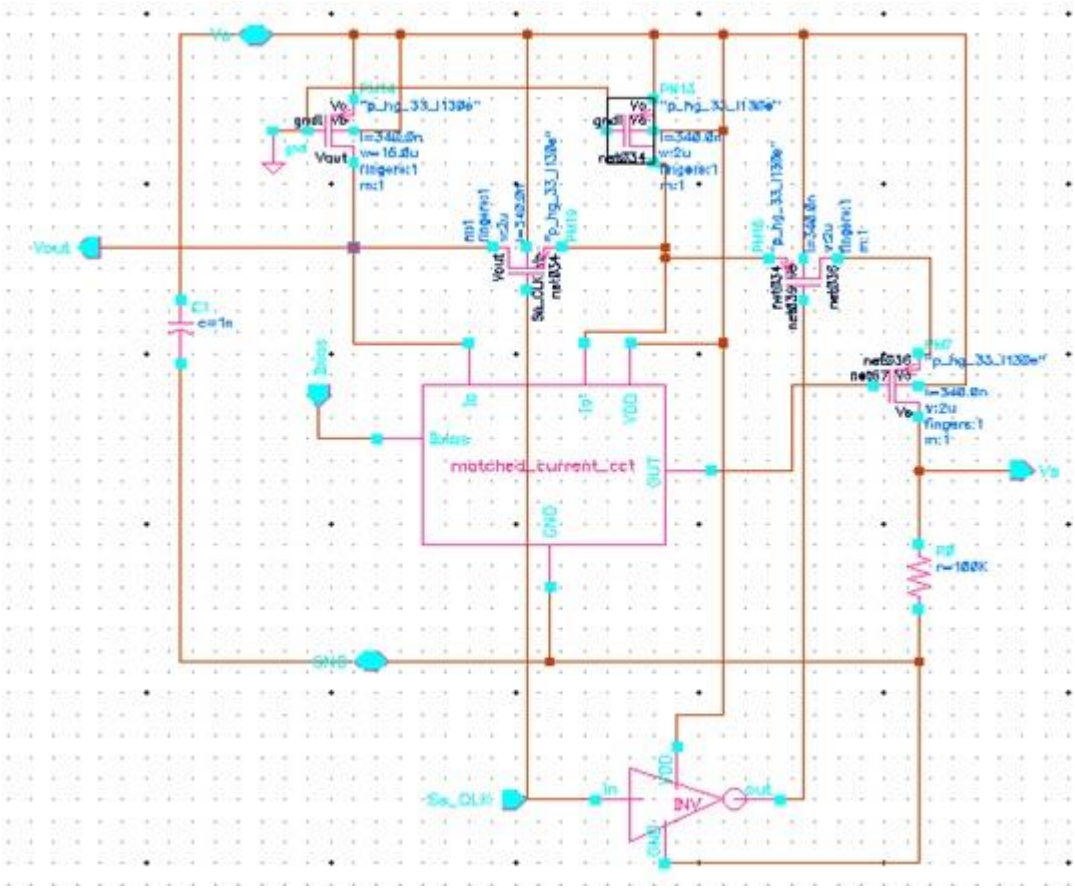


Figure 7.29: Schematic of Current Source Circuit

7.7.2 Schematic Of Decision Generation Circuit

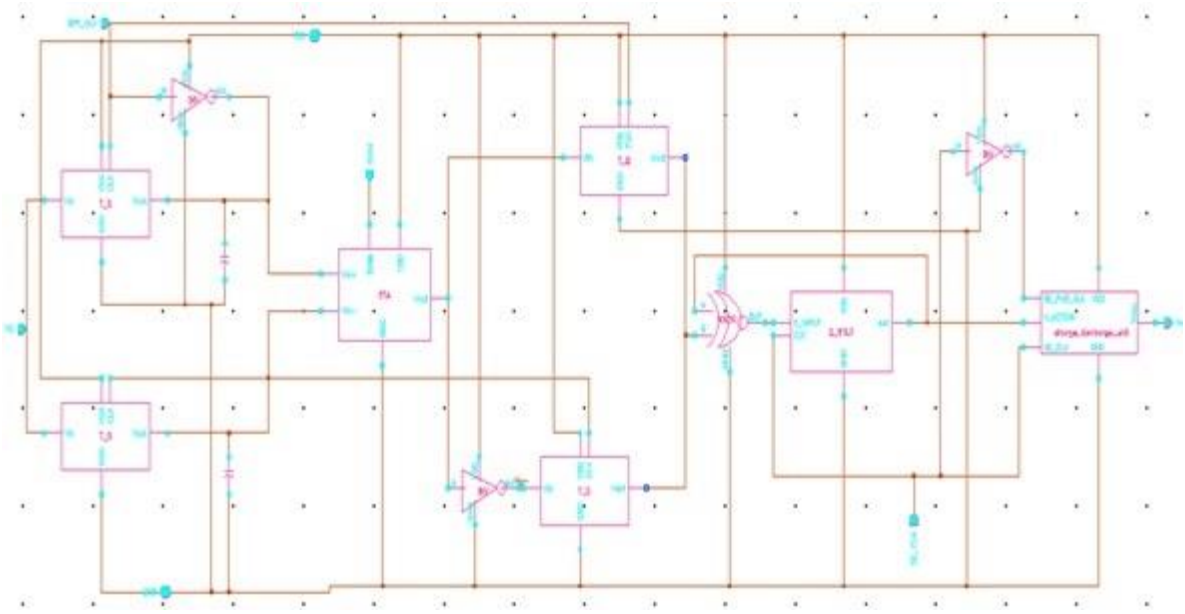


Figure 7.30: Schematic of Decision Generation Circuit

7.7.3 Schematic Of Control Unit Circuit

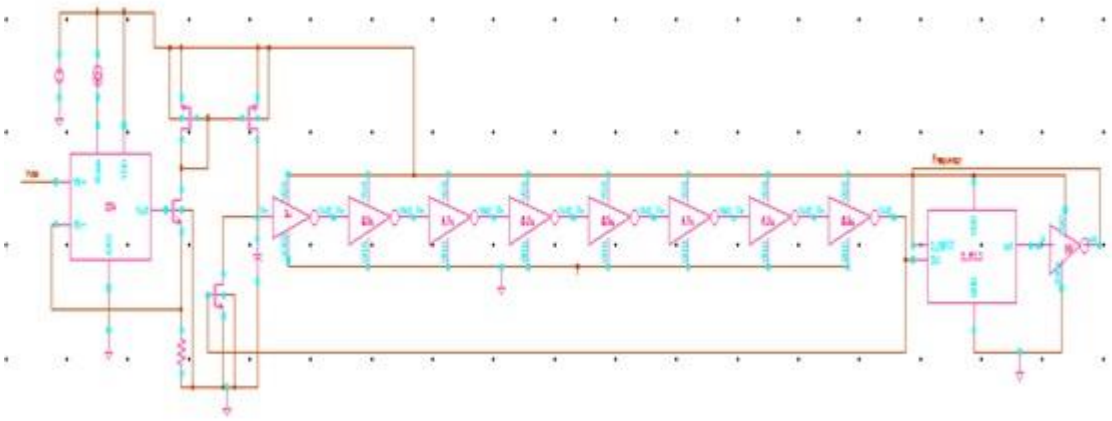


Figure 7.31: Schematic of Control Unit Circuit

7.8 LAYOUT

7.8.1 Layout of firs inverter in control unit ring oscillator

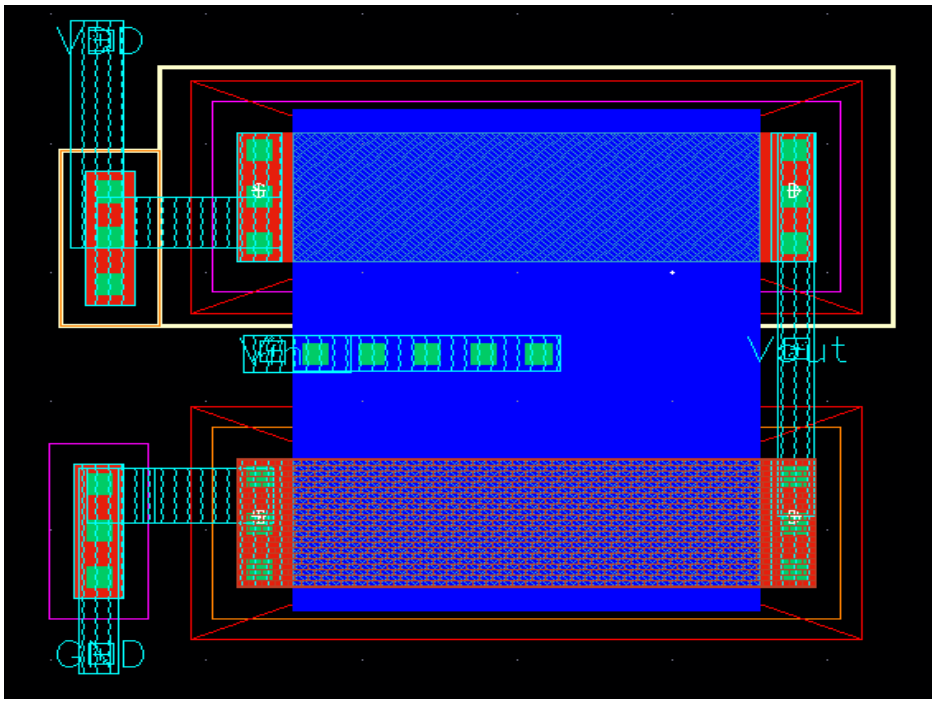


Figure 7.32: Layout of firs inverter in control unit ring oscillator

Inverter shown in figure 7.32 has big length L = 3um and W= 1um to decrease power consumption in this inverter since VF varies around the threshold of the inverter I1, the short circuit current of I1 is significant. Here we use smaller size MOSFETs to implement I1 in order to reduce the current loss.

7.8.2 Layout of other inverters in control unit ring oscillator

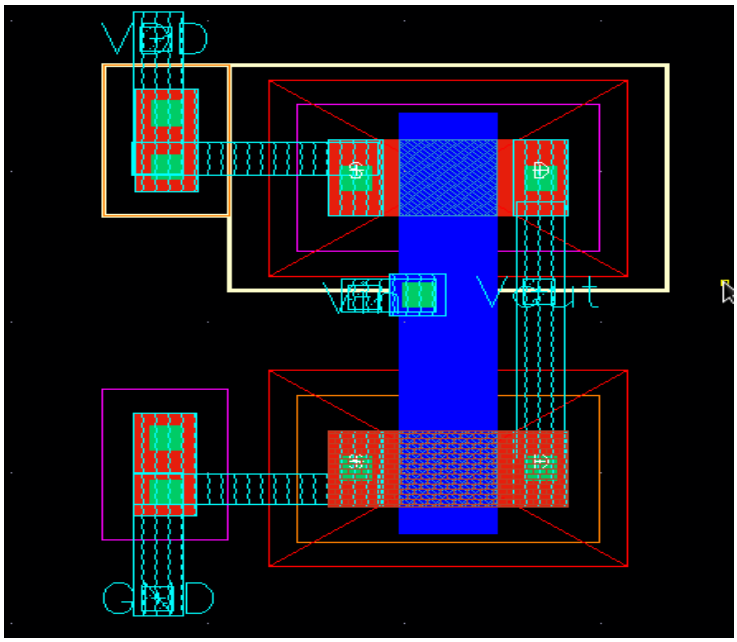


Figure 7.33: Layout of other inverters in control unit ring oscillator

Figure 7.33 show other inverters used in ring oscillator of the control unit it has L equal 0.5um and W equal 0.5um also to reduce current losses in this inverters .

7.8.3 Layout of normal inverter used in all circuits

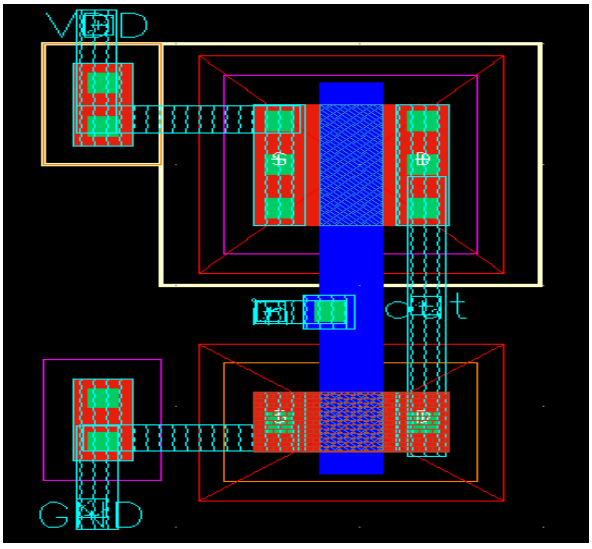


Figure 7.34: Layout of normal inverter used in all circuits

7.8.4 Layout XNOR gate

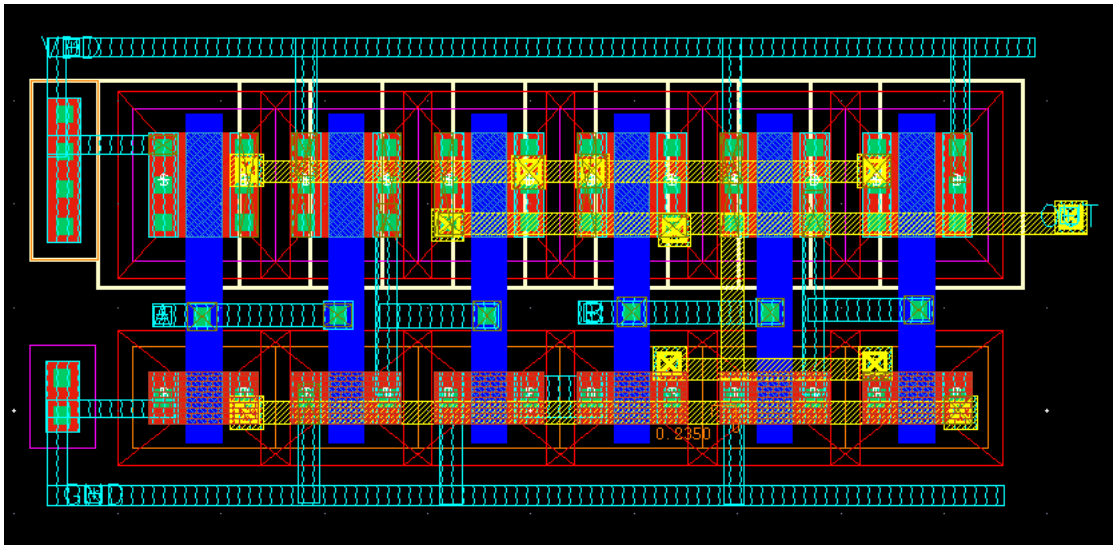


Figure 7.35: Layout XNOR gate

7.8.5 Layout of transmission gate

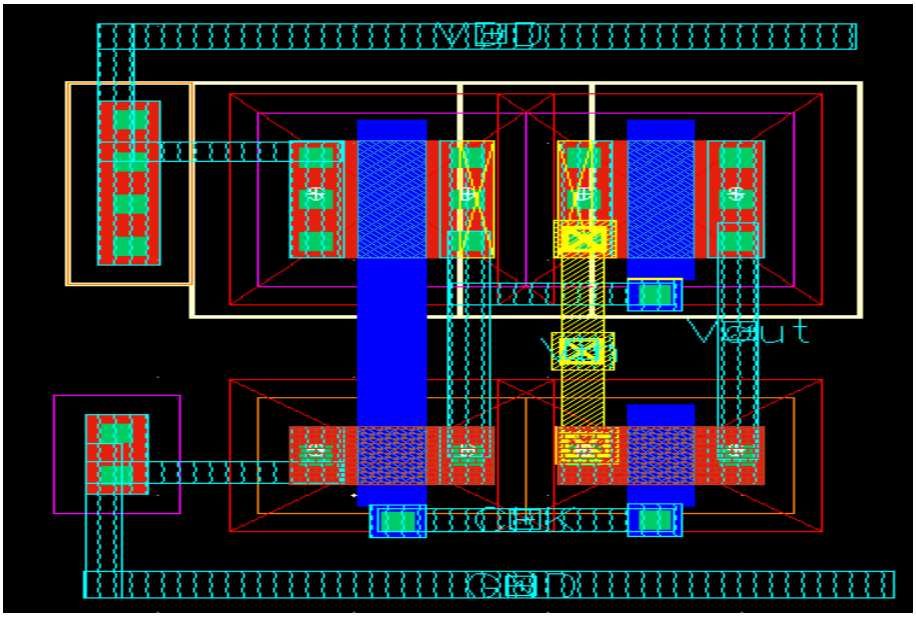


Figure 7.36: Layout of transmission gate

Figure 7.36 shown layout of transmission gate, it is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 but poor 1. It composed of PMOS and NMOS work simultaneously, it takes both advantage of them strong 1 and strong 0.

7.8.6 Layout of charging & discharging circuit

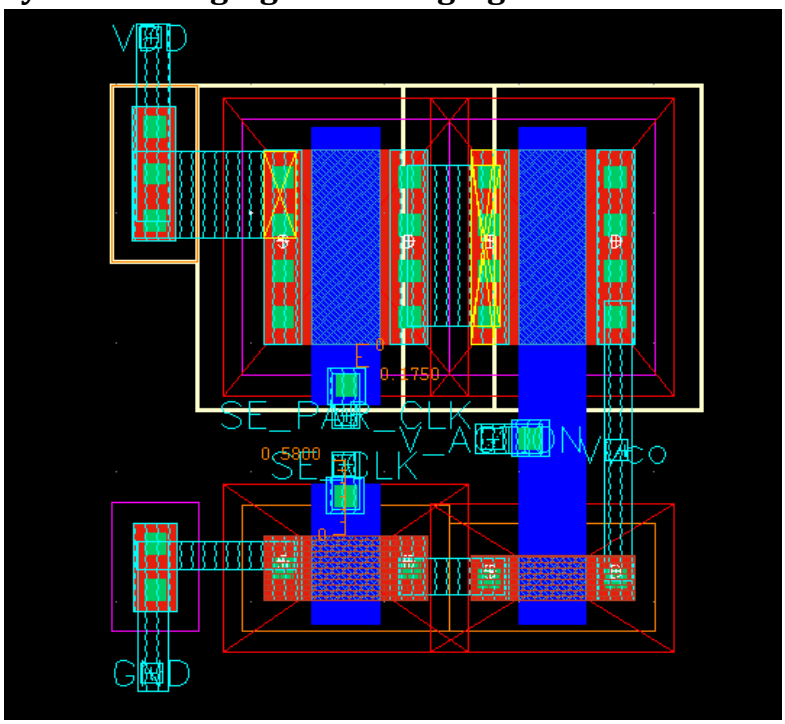


Figure 7.37: Layout of charging & discharging circuit

Figure 7.37 shows charging & discharging circuit, this circuit is the last four transistors in the decision generation circuit responsible for charging and discharging capacitor.

7.8.7 Layout of matched current source in current sensor

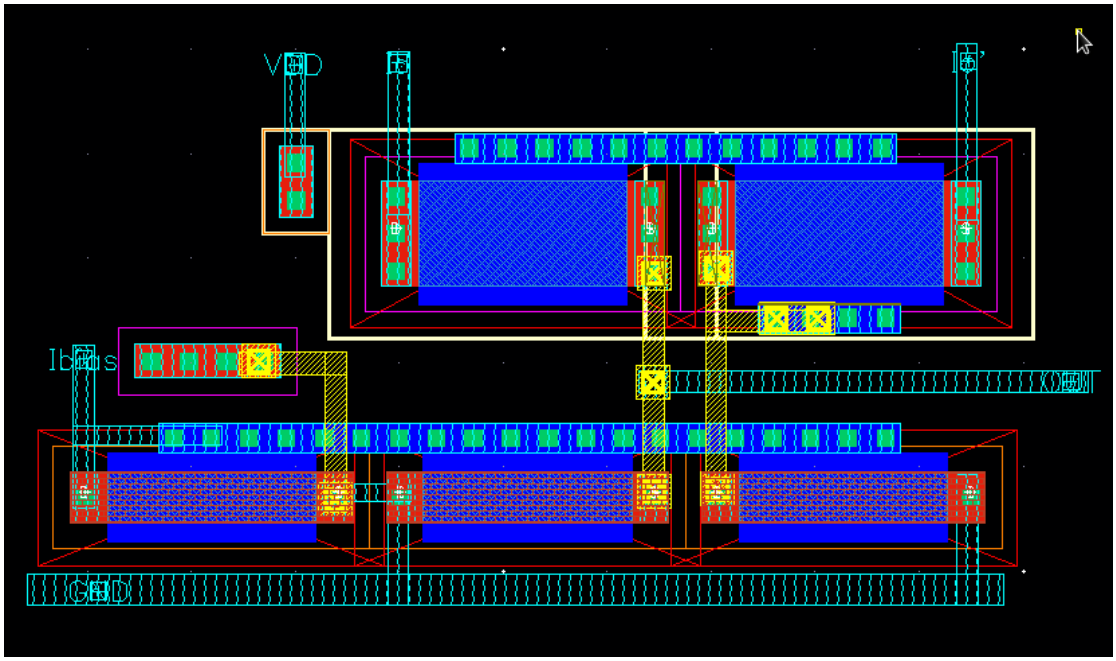


Figure 7.38: Layout of matched current source in current sensor

7.8.8 Layout of current mirror of control unit

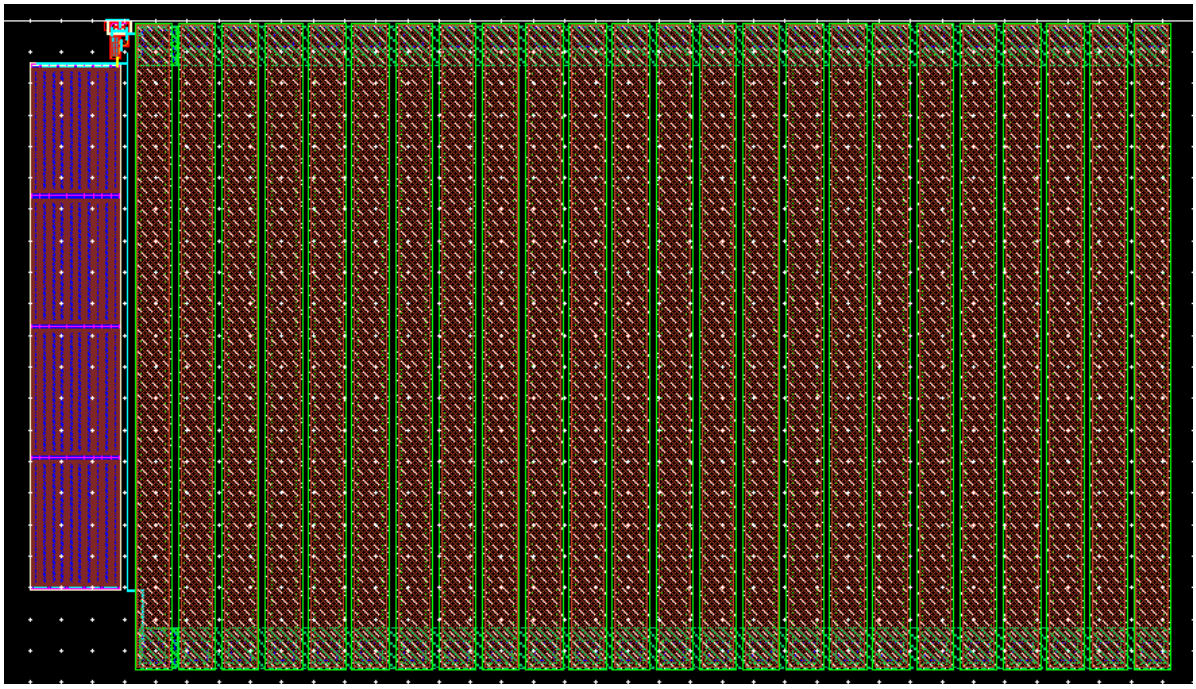


Figure 7.39: Layout of current mirror of control unit

Chapter 8 Conclusion

The field of implantable biomedical is attracting more research interest by offering wide applications for the near future implantable devices. As we discussed previously Energy harvesting, whose main function is to provide clean sources of energy for biomedical applications to overcome the disadvantages of the chemical battery. An energy harvesting system design presents a considerable challenge because of its simultaneous requirement for high efficiency, low power consumption, small input voltage and required high output voltage and low frequency for biomedical application.

In thermal energy harvesting system we used a charge pump is used to set up voltage as well as a simple maximum power point tracking circuit so the power consumption is less than other methods, Therefore our proposed system has a high efficiency and it operate at low frequency which suitable for human body for biomedical applications, Despite this we try to develop the circuit to operate at lower frequency and decrease the channel length of the inverter to decrease the manufacturing cost.

The two systems that were designed for energy harvesting that is inductive link energy harvesting system and the thermal energy harvesting system, table 8.1: shows the technology used is simulation for both systems equal 130 nm and show that inductive link system used ac to dc converter and used LDO as dc to dc converter and not use MPPT, while thermal energy system used MPPT circuit and used charge pump as dc to dc converter and no need for ac to dc converter.

Table 8.1: Shows the inductive and thermal harvesting system specifications

	Inductive link system	**Thermal energy system**
Technology	130 nm	130 nm
MPPT circuit	Not used	Used
AC to DC converter	Used	Not used
DC to DC converter	LDO	Charge pump (one stage)
Input voltage	2 v (peak to peak)	250 mv
Output voltage	1.2 v	1.2 v
Operating frequency	13.56 MHz	6 MHz

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