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A High-Frequency Buck Converter Design Using Mixed Signals Control System

A Graduation Project Submitted in Partial Fulfillment of B.Sc. Degree Requirements in Nanotechnology and Nanoelectronics Engineering

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Abstract

A buck converter (step-down converter) is a DC-to-DC power converter which steps down voltage (while stepping up current) from its input (supply) to its output (load). DC-DC converters are used in nearly every electronic device. Buck converters are crucial in battery powered devices where they are used to generate supply voltages for analog, digital, and radio-frequency ICs. A multitude of challenges are involved in designing control systems for such converters that achieve a wide range of output voltages and load currents needed to drive different loads, also, high frequency, low power systems, small area along with the high efficiency are also desired. In this project a novel mixed-signal control system for a high frequency buck converter is designed in TSMC 0.18µm technology, laid out and fabricated.

Acknowledgement

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List of Abbreviations

ADC	**A**nalog to **D**igital **C**onverter
CCM	**C**ontinuous **C**onduction **M**ode
CP	**C**harge **P**ump
DCM	**D**iscontinuous **C**onduction **M**ode
DCO	**D**igitally **C**ontrolled **O**scillator
DFF	**D**-**F**lip **F**lop
DTC	**D**ead **T**ime **C**ontrol
EA	**E**rror **A**mplifier
LPF	**L**ow-**P**ass **F**ilter
PFD	**P**hase **F**requency **D**etector
PLL	**P**hase **L**ocked **L**oop
PWM	**P**ulse **W**idth **M**odulator

1. Introduction and Literature review

1.1. Introduction

Managing to convert DC voltage from one value to another (DC-DC conversion) is of great significance in the electronic industry, especially in power management units as it is crucial in almost all electronic devices [1, 2]. For instance, decreasing or increasing the available input voltage can reduce battery space, saves certain blocks in the system from damage or breakdown, and facilitates obtaining optimum operating conditions. Also, DC-DC conversion is important in generating supply voltages for analog, digital, and radio-frequency ICs. Moreover, the development of cell phones, PCs, and different applications at the forefront of the electronics industry involves scaling to smaller sizes while providing more diverse functionalities. For instance, Consumers demand Smaller Phones, Maximum battery life and reduced battery charge time. This Diversity in Functionality requires Numerous Components with different power rails. Thus, comes the necessity of DC-DC conversion as an efficient way of meeting different power demands in a single system [3, 4].

One of the aspects where DC-DC conversion is mostly needed is along with the Li-Ion rechargeable battery. It is considered a strong power source for portable electronics for now and into the near future because it provides more power for its size and weight than other types due to its high gravimetric and volumetric energy densities [4]. Moreover, its operating voltage is higher than the primary high current power rails, which enhances DC-DC conversion efficiencies, and by turn the battery lifetime because bucking (stepping down) a higher voltage rail to a lower one proved to be more efficient than boosting (stepping up) to a higher voltage rail [3, 4].

Another aspect is Dynamic voltage scaling. Two of the most power-hungry components in a mobile phone are the RF power amplifier (PA) and the baseband processor. PA is designed to have highest efficiency at maximum transmit power. However, to maintain quality communication, most cell phones reduce transmit power to the minimum required. That is why it is critical to dynamically adjust the power rail voltage of the PA to maintain efficient performance. Similarly, since the dissipated power in a processor is directly proportional to V2, it is preferred to operate the processor at a reduced voltage and a lower frequency when in standby to limit power dissipation and reach longer battery life and higher efficiency. Consequently, it is important to link the PA or processor to a DC-DC converter that can dynamically scale the power rail voltage as required through proper control loops [4, 5].

Another important application is in Automotive Battery Recharge using Solar energy, which causes electrical consumption to be reduced. Nevertheless, when the solar panel absorbs the solar energy, unregulated DC output is generated. Thus, the output voltage needs to be regulated using DC-DC converters to be suitable for further applications. Also, charging time can be reduced by employing a boosted (stepped up) voltage to the battery.

Other applications include Communication Systems, audio systems, Mobile AMOLED Display, in computer peripheral equipment and industrial applications especially for

high output voltage projects, PV applications (MPPT Algorithms), regulated DC power supplies and highly efficient white LED drives [5, 6].

1.2. DC-DC Converters

1.2.1. Overview

The DC-DC power conversion is defined as the process of producing a wanted dc voltage from another level generated from a dc source. This could be realized using a linear regulator, which is a circuit where the resistance of the regulator changes depending on both the input voltage and the load, leading to maintaining a fixed voltage at the output. This regulator behaves as a variable resistor that continues to adjust a voltage divider network to keep the output voltage constant while any excess voltage is dissipated as heat, on the other hand, a better and more efficient alternative is switching regulator, which uses a power switch (active devices) that turns off and on to maintain an average output value, in addition to a diode and an inductor to transfer energy from input to output [7]. Furthermore, advantages of Switching regulators over linear regulators for dc-to-dc power conversion include less energy loss during the transfer, smaller components, less thermal management, and high efficiency (80 to 95%) depending on the load. Also, efficiency of a linear regulator is limited since its regulated voltage must always be less in value than input voltage, whereas the input voltage must be sufficiently high to allow the active device to drop a certain amount of voltage. furthermore, the energy stored by an inductor in a switching regulator is not only capable of being transformed to a reduced (bucked) output voltage, but it can also be increased (boosted), inverted (reverse polarity) or be transferred (through a transformer) to the output that is now electrically isolated from the input [8].

DC-DC converters, which are switching regulators, can be classified into two main stages: the power stage and controller. The power stage accepts an arbitrary input voltage and produces a predetermined output voltage using different circuit components, while the controller produces signals for the power stage to function properly [7, 8]. The power stage is of great significance of the dc-to-dc power conversion technology because most of the requirements need to be met during its design. For instance, a dc-to-dc converter's load current should not be too limited as it needs to meet an arbitrary load requirement. Also, the Input-to-output voltage ratio should be determined to be either considerably small or large. In addition, dc-to-dc converters are regularly required to provide electrical isolation between the input source and the load [7 -9].

For power stage, a DC-DC converter uses semiconductor devices, like MOSFETs and Diodes (for switching), reactive components, like capacitors and inductors (for filtering), and transformers (for altering the current and voltage levels of circuit variables during electrical energy transfer). The semiconductor devices are considered lossless switches that turn on and off at a very high frequency. Consequently, other power stage components are exposed to constantly-changing voltage and current

excitations because of this switching activity. This switching activity and periodicity define the features of the power stage components of dc-to-dc converters [7, 8].
A DC-DC converter load might be any electronic device that needs a constant dc voltage to operate. Thus, the DC-DC converter provides the necessary amount of current for the load to gain sufficient power. This means the load current is subjected to fluctuations in accordance with the load operational conditions. These changes could be rapid and frequent, especially with high-frequency digital systems as a load, which requires the power stage design to be flexible regarding abrupt and wide variations in current level. Furthermore, the DC-DC converter is not only required to accept any voltage and provide a fixed dc voltage for the load, but also to keep the output constant in case of any variations, abrupt change in the input voltage or ac ripple component [8, 9].

1.2.2. Types of DC-DC Converters

DC-DC converters come with various configurations of their power stage. Most conventional DC-DC converters have a DC path from input to output and they differ from each other as explained below:

- Buck converters: Voltage step down, output is the same polarity as input.
- Boost converters: Voltage step up, output is the same polarity as input.
- Luo converters: Voltage step up, output is the same polarity or reverse polarity as input.
- Buck-Boost & Cuk converters: Voltage step-up or step-down, output is reverse polarity as input.
- Zeta converters: Voltage step-up or step-down, output is the same polarity as input.
- Flyback converters: They have no DC path from input to output (Isolated Architectures) [7, 8].

The following subsections will give a brief introduction on each type, its principle of operation, advantages, and disadvantages.

1.2.2.1. Boost converters

The conventional topology of Boost converters is illustrated in Figure 1, its main function is to Convert lower voltage value into higher ones.

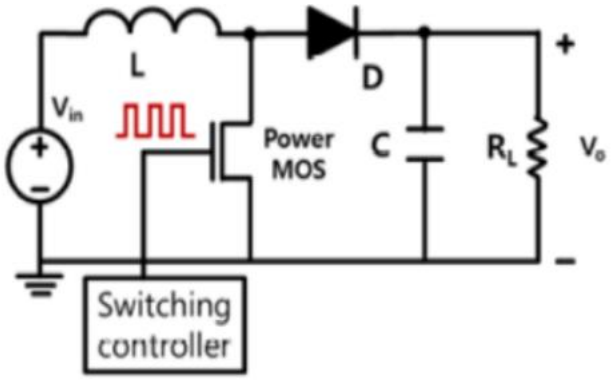

Figure 1: Basic Boost converter topology

Principle of operation is as follows: when the power MOS is switched on, the diode is off, and the inductor current is collected. Also, output capacitor C begins to discharge through RL. Second, when the power MOS is switched off, the collected current in the inductor begins to discharge to the output through the diode.[10].
Advantages of this type of converters are it can step up the voltage with minimal number of components possible in addition to continuous input current. Additionally, the output voltage is positive, which facilitates the control process. In contrast, the discontinuous charging current of the output capacitor leads to larger capacitor size. Additionally, its highest efficiency is limited to duty cycle of 0.5 and the transfer function has a zero in the right half plane which causes control complexity. Also, it is not capable of stepping down the voltage and lacks isolation from input to output [11].

1.2.2.2. Luo converters

Luo Converters are new DC-DC boost conversion circuits that produce an output with the same polarity as the input. Also, they are known for simple circuitry, high efficiency, and small output current and voltage ripples. The most basic topology of the Luo converter is the positive output topology shown in Figure 2. Other known topologies are negative output, self-lift, super-lift, ultra-lift, and combinations of these configurations [12].

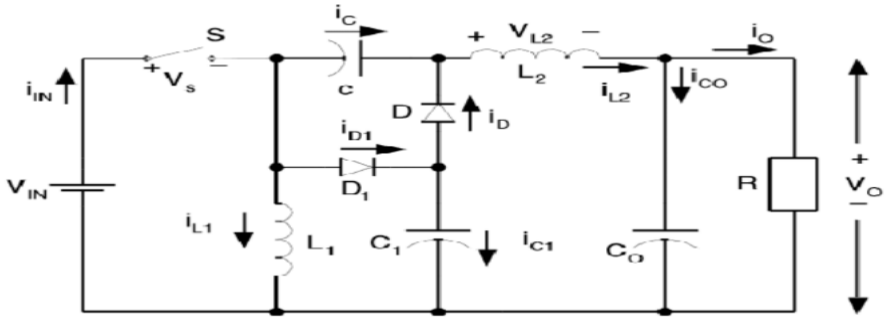

Figure 2: Basic Luo converter topology

Principle of operation is as follows: when switch S is turned on, the source current i_{IN} is the sum of both inductors' currents. First, Inductor L1 collects energy from the source while inductor $L2$ collects it from both the source and capacitor C. As a result, both inductors currents begin to increase. Then, when switch S is turned off, source current

i_{IN} becomes zero, which causes current i_{L1} to charge capacitor C through the free-wheeling diode D. At the same time, current i_{L2} attempts to stay continuous by flowing through the (C_O - R) circuit and freewheeling diode D. Consequently, both inductors currents iL1 and iL2 begin to decrease [12, 13].

Advantages of this type of converters are large voltage transfer gain, high output voltage with small ripples, inexpensive components, and high efficiency. Nevertheless, some topologies have the problem of Output voltage increase in arithmetic progression [14].

1.2.2.3. Buck-Boost converters

The Buck-Boost converter is the DC-DC converter that can both increase and decrease the voltage at its input [15]. The most basic topology of the Buck-Boost converter is the inverting topology shown in Figure 3 [16].

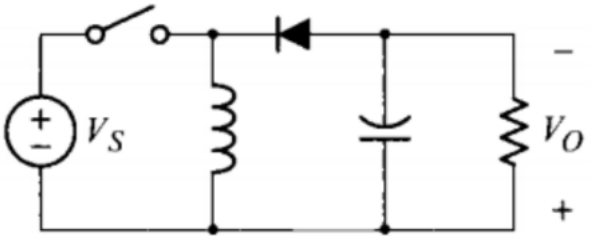

Figure 3: Basic Buck-Boost converter topology

Principle of operation is as follows: when the switch is on, the diode (which acts as a passive switch) is reverse biased (acts as open circuit) leading to charging the inductor (increasing the inductor current IL) while the capacitor discharges to keep Vo's value, The output voltage has an opposite polarity to that of the input voltage Vs and hence the name inverting [16, 17]. When the switch is off, the Inductor current charges the capacitor, and the diode becomes forward biased (acts as a short circuit). The theoretical range that a Buck-Boost converter can cover spans from 0 to infinity [16].

The main advantage of Buck-Boost converters is the fact they can function both ways as a step-up or a step-down converter, however, single switch buck-boost converters are relatively unstable due to the existence of a right half plane zero [18, 19]. This paves the way for introducing two and four switch buck-boost topologies to help overcome these limitations [20, 21].

1.2.2.4. Cuk converters

A Cuk converter is a boost-converter cascaded to a buck-converter to make use of both of their strengths. The buck-converter has a smooth output due to the large output capacitance and the boost-converter has a smooth input voltage. The energy is being stored in a capacitor and it can step up or down the output voltage. The transfer of energy is due to the coupling capacitor (C) shown in Figure 4. The capacitor is large enough to produce almost a DC signal, but it is not as large as the output capacitance,

while the inductors ensure that the current is smooth at the output. Also, the Cuk converter usually works in the KHz frequency range with hundreds of Watts power range [22]. Furthermore, Cuk converters have two major topologies: isolated and non-isolated. The only difference is that the isolated topology design must take high power into consideration. The non-isolated topology is an inverting converter and is depicted in Figure 4 [23].

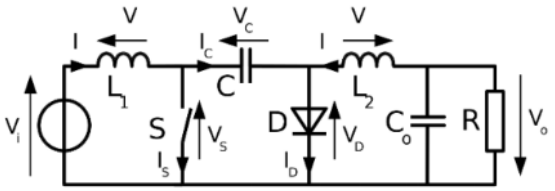

Figure 4: Basic Cuk converter topology

Principle of operation is illustrated in Figure 5, and it consists mainly of two states: First, the on state "Diode in reverse bias", where L1 current and power rises as it draws from the input source. L2 current also rises as it draws power from C. Second, the Off state "Diode in forward bias", where L1 current decreases since the energy is being released to C. L2 current also decreases since the energy is released to C0 [23, 24].

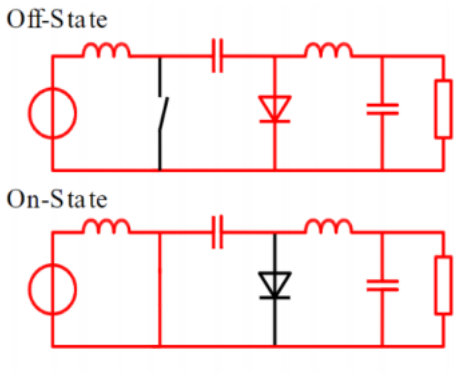

Figure 5: Operation modes of Cuk converter

The major advantages of the Cuk converters are smooth input and output, and the capability of both increasing or decreasing the voltage. However, the negative output voltage and the complex control system makes their design more challenging [24].

1.2.2.5. Zeta converters

Zeta converter is considered a fourth-order DC-DC converter that can operate in either step-up or step-down mode, with four passive components (two capacitors and two inductors). The basic (non-inverting) topology is shown in Figure 6 [25].

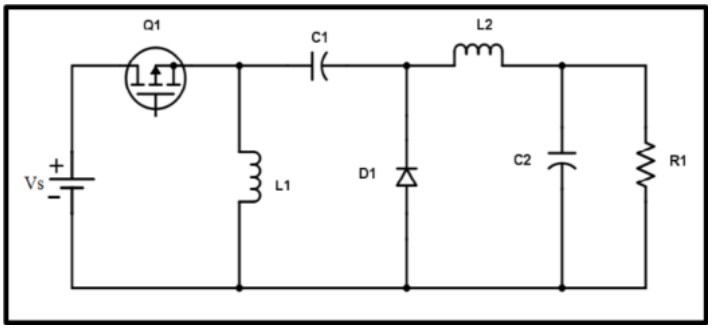

Figure 6: Basic Zeta converter topology

Principle of Operation of the Zeta converter is described by two modes of operation as shown in Figure 7, and Figure 8: First, operation Mode 1 (Switch Q1 is closed and diode is off), where both Inductors currents as they are being charged from the source. Also, discharging of C1 and charging of C2 occur simultaneously. Second, Operation Mode 2 (Switch Q1 is open and diode is on), where inductor currents $iL1$ and $iL2$ discharge gradually through capacitors $C1$ and $C2$ [25, 26].

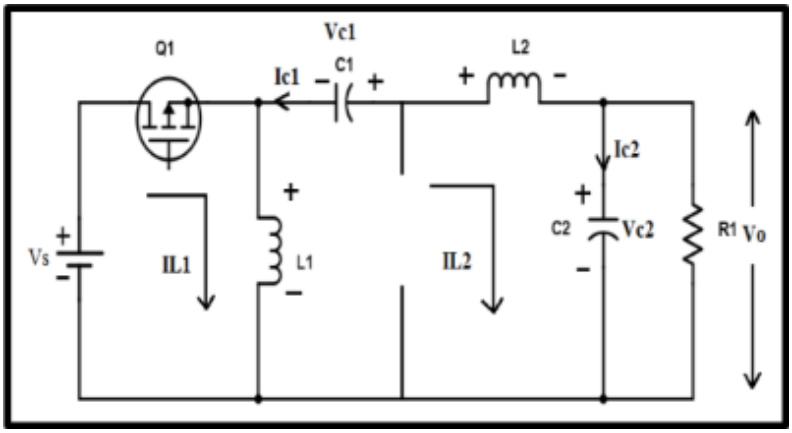

Figure 7: Operation Mode 1 of Zeta Converter

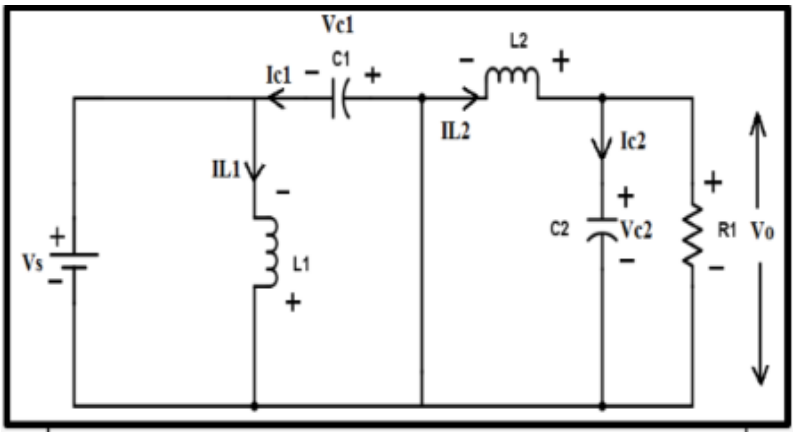

Figure 8: Operation Mode 2 of Zeta Converter

The main advantages of Zeta converters are input to output DC insulation, Buck-boost capability, continuous output current and uniformity of input current. Also, they are easy to compensate due to the absence of zeros in the right-half plane. This facilitates achieving a broader loop bandwidth, better load-transient response, and smaller output

capacitance values. However, they are difficult to control and have high area and power consumption [27].

1.2.2.6. Flyback converters

The flyback configuration is the most plausible among other low-power dc-dc converters due to its relative simplicity [28, 29]. It is considered a modification of the conventional Buck-Boost converter by substituting the inductor with a transformer as indicated by Figure 9, and Figure 10. It is convenient for low wattage applications less than 200Watt [30, 31]. Flyback transformers are normally utilized for output power range of 50-100W. They are also used in high-voltage power supplies for televisions and computers with output current less than about 10 Amps [32].

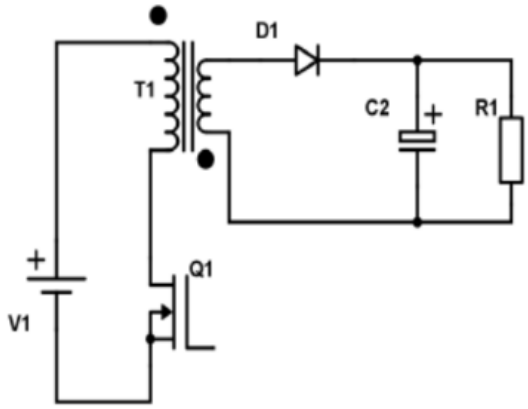

Figure 9: Basic Flyback converter topology

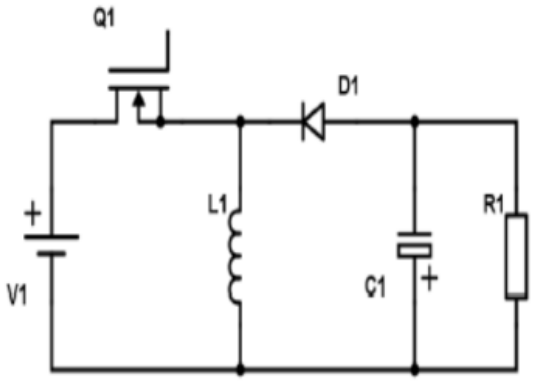

Figure 10: Basic Buck-Boost converter topology

Flyback converter consists of a MOSFET for switching, Clamp circuit for clamping the overshoot voltage resulted from leakage inductance, and a transformer for electrical isolation, energy storage and transfer. Additionally, the capacitor used at the output decreases the ripples [33]. Figure 11 shows the working principle of flyback topology in three main stages: First, MOSFET is turned on and the primary current rises to the highest possible value, and meanwhile, energy is being stored in airgap of a ferrite core transformer. During this stage, the output capacitor is the only source of energy to the output. By the end of this stage, the MOSFET is switched off and the current is at its

peak value. Second, energy begins to transfer from the left side of the transformer to the right side. This happens since the dotted end becomes more negative than the undotted end once the MOSFET is off, which forces the diode on the right side to turn on and leakage inductance attempts to resist this change. This results in a voltage overshoot at the drain of the MOSFET, and ringing with MOSFET parasitic capacitance. Finally, all energy is now transferred to the right side, and the parasitic component of MOSFET in the left side is resonating with the magnetizing inductance as they form an LC circuit. Thus, the next switching can start at any time [32- 34].

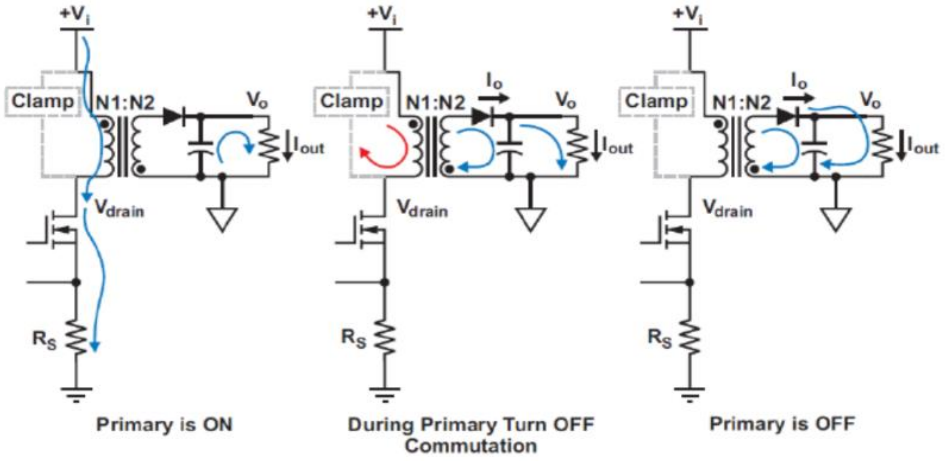

Figure 11: Operation Modes of Flyback Converter

Flyback topology has advantages of multiple outputs, better isolation, and low number of components. Additionally, the transformer suppresses the ripple and avoids electric shocks which enhances reliability of the consumer product. the output voltage can be stepped up or down depending only on turns ratio. Whereas its limitations are the low efficiency, poor cross regulation, the voltage overshoot problem. Also, the only limitation on the number of outputs is transformer pins count [34, 35].

1.3. Buck Converter

As shown in the previous section, there are numerous DC-DC converters with different power stage designs. One of them is the buck converter whose output voltage is lower than the input voltage at all times. The Buck converter is the simplest in both the structure and operation without lacking any of the fundamental features that exist in other converter types. [7, 8]. That is why the buck converter was our selection in this project.

1.3.1. Definition

The buck converter is the simplest circuit that can step-down the voltage while stepping-up the current which is known as step-down dc-to-dc power conversion. As shown in Figure 12, buck converter consists of two main functional parts: a single-pole double-throw (SPDT) switch and ideal low pass filter [8].

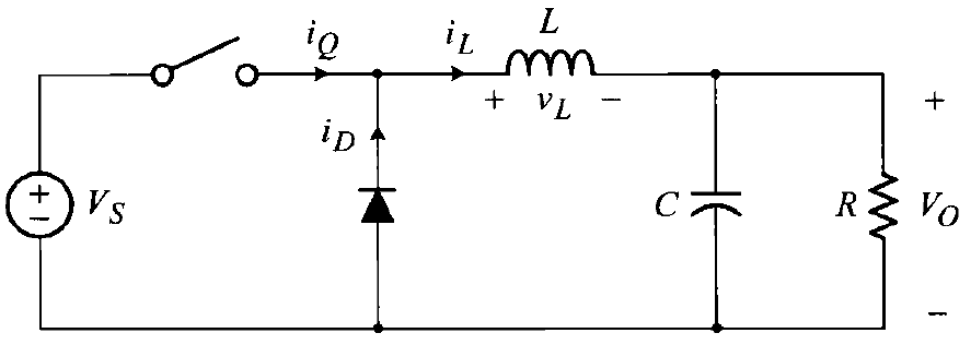

Figure 12: Buck Converter

1.3.2. Theory of Operation

Buck converter has two modes of operation in continuous conduction mode (CCM) according to the switch state:

As indicated in Figure 13, switch is closed (ON-State), so the diode is an open circuit and can be removed as indicated and the voltage source is connected to the loop filter and the load resistance. While in Figure 14, switch is open (OFF-State) so the diode is a short circuit and the voltage source is disconnected and can be removed as shown.

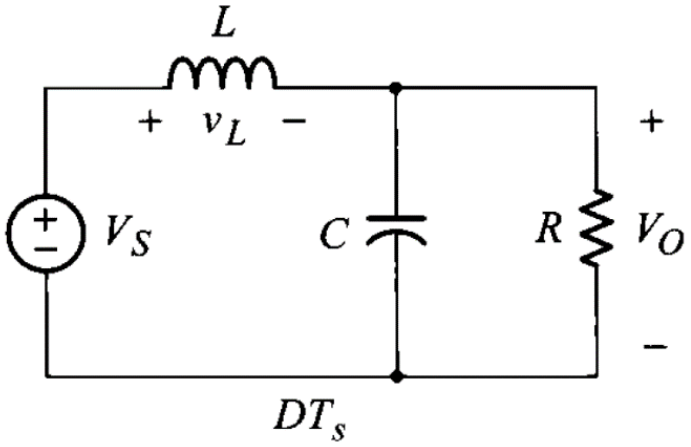

Figure 13: Buck Converter ON-State

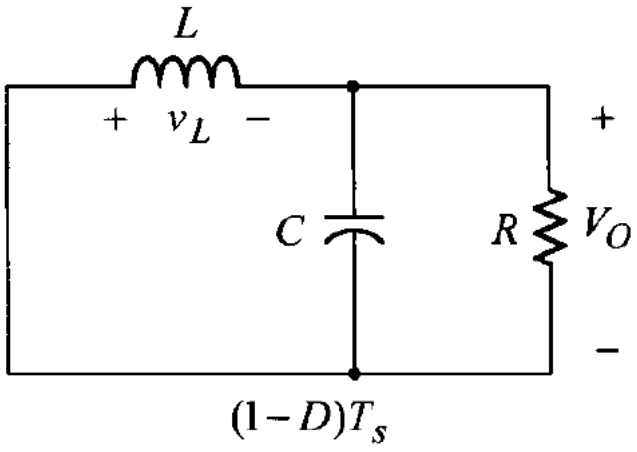

Figure 14: Buck Converter OFF-State

1.3.3. CCM Analysis

In both states, the output voltage is to be considered as constant V_0 according to the small-ripple approximation.
Inductor voltage v_L (as shown in Figure 15) is:

$$v_L = \begin{cases} V_S - V_0 & for\ ON - State \\ -V_0 & for\ OFF - State \end{cases} \quad (1.3.1)$$

Where:

- V_S is the source voltage.
- V_0 is the output voltage.

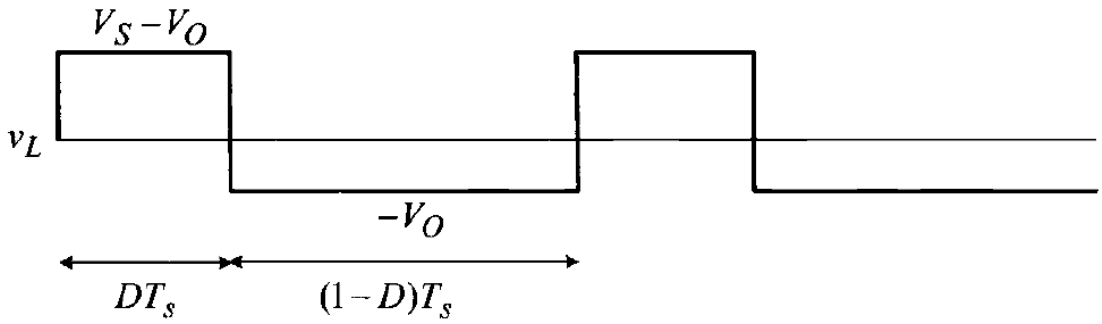

Figure 15: Inductor voltage in CCM

Using the condition of volt-second balance on the inductor gives:

$$(V_S - V_0)DT_S = V_0(1 - D)T_S \quad (1.3.2)$$

And that gives: $V_0 = DV_S$
While D is always ≤ 1, and hence output voltage is always smaller than the input voltage (voltage stepping down).
Where:

- D is the duty cycle ratio (the ratio of sampling time or one-cycle time in which the circuit is in ON-State)
- T_S is the sampling time or the one-cycle time.

Inductor current equation is:

- For ON-State:
  $i_L(t) = \frac{v_L(t)}{L}t = \frac{V_S - V_0}{L}t \quad for\ 0 \leq t \leq DT_S \quad (1.3.3)$

- For OFF-State:
  $i_L(t) = \frac{v_L(t)}{L}t = \frac{-V_0}{L}t \quad for\ DT_S \leq t \leq T_S \quad (1.3.4)$

This means that inductor current is going up in the ON-State while going down in the OFF-State as shown in Figure 16.

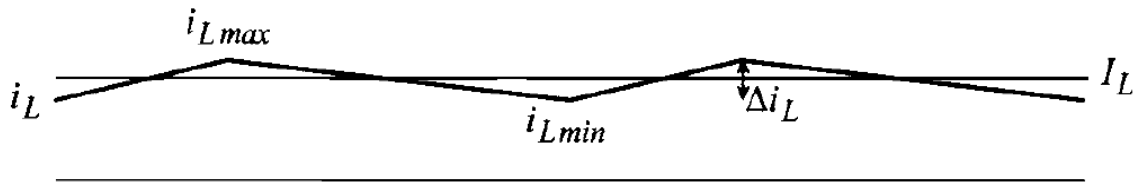

Figure 16: Inductor current in CCM

1.3.4. Current Ripples Analysis

The average current through the capacitor = 0 according to the condition of charge balance. So, the average current through the inductor is the same average load resistor current.

$$\therefore \bar{\imath}_L = I_L = \frac{V_0}{R} \qquad (1.3.5)$$

From (1.3.3) and (1.3.4) we can get that:

$$\Delta i_L = \frac{v_L}{L}\Delta t = \frac{V_S - V_0}{L} D T_S = \frac{-V_0}{L}(1-D)T_S \qquad (1.3.6)$$

As shown in Figure 16:

$$i_{L\,max} = I_L + \frac{1}{2}\Delta i_L \qquad (1.3.7)$$

$$i_{L\,min} = I_L - \frac{1}{2}\Delta i_L \qquad (1.3.8)$$

As shown in Figure 17 and Figure 18

- Current flowing through the switch in the ON-State I_Q is:

$$\bar{\imath}_Q(t) = I_Q = D I_L \qquad (1.3.9)$$

- Current flowing through the diode in the OFF-State I_D is:
-

$$\bar{\imath}_D = I_D = (1-D) I_L \qquad (1.3.10)$$

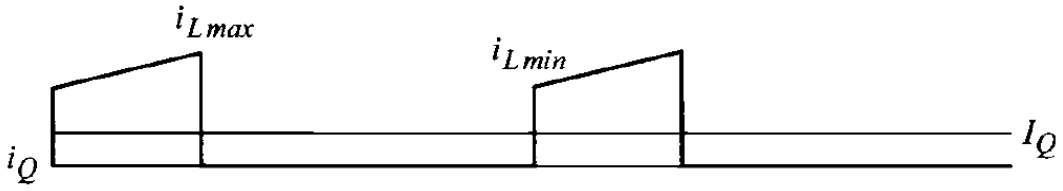

Figure 17: Switch current in CCM

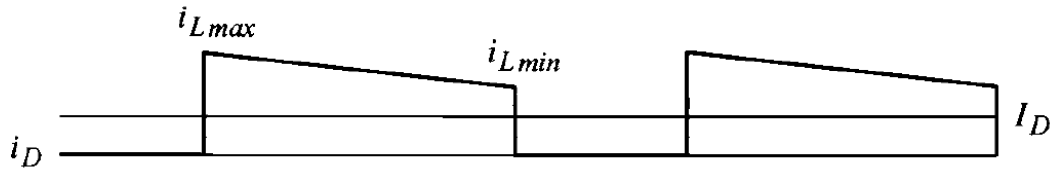

Figure 18: Diode current in CCM

1.3.5. Voltage Ripples Analysis

Due to non-ideal filtering of the LC loop filter, voltage ripples exist in output voltage.

As shown before in Figure 16, inductor current increases and decreases according to the state. This current consists of two components:

- DC component: that flow completely in the load resistor as the capacitor is assumed to be an open circuit in the DC analysis.
- AC component: due to using large capacitors for efficient filtering, the capacitor reactance in AC analysis is much smaller than load resistance. So, this component is assumed to be flowing entirely in the capacitor i_C as shown in Figure 19.

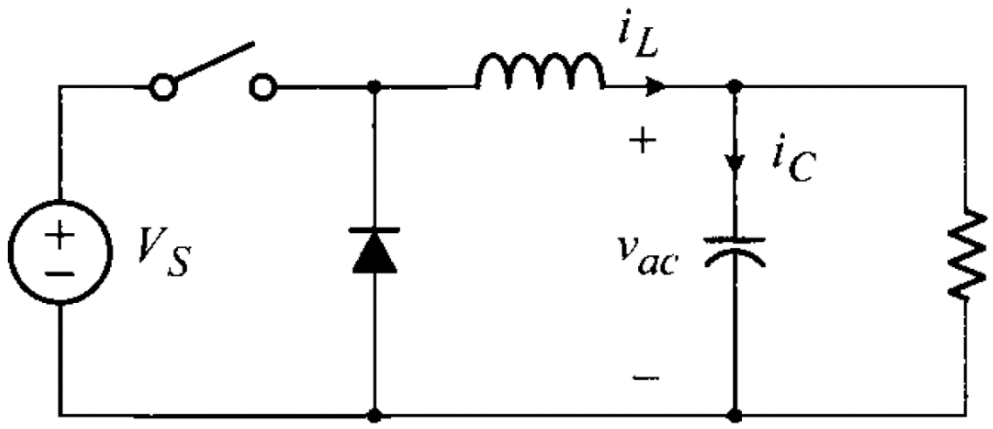

Figure 19: Circuit diagram in AC mode

The triangular AC current component flowing in the capacitor makes a voltage difference v_{ac} across the capacitor as shown in Figure 19, which make a ripple component to be added to the DC output voltage as shown in Figure 20.

$$v_{ac}(t) = \frac{1}{C}\int i_C(t)\,dt \qquad (1.3.11)$$

Where:

- i_C is the current flowing through the capacitor.

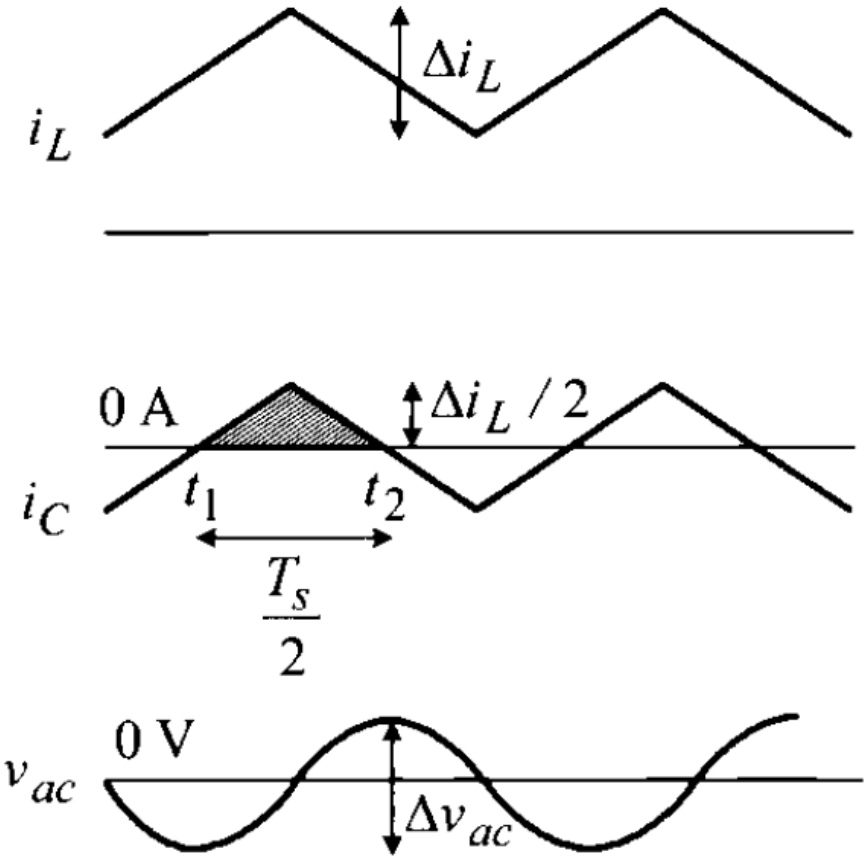

Figure 20: Ripples of Inductor Current, Capacitor Current and Capacitor Voltage respectively.

From (1.3.11) we can see that v_{ac} is positive whenever i_C is positive. For example, between t_1 and t_2 as shown in Figure 20.

$$\therefore \Delta v_{ac} = \frac{1}{C}\int_{t_1}^{t_2} i_C(\tau)\, d\tau \qquad (1.3.12)$$

$$\text{And } i_C = \frac{1}{2}\Delta i_L \qquad (1.3.13)$$

$$t_2 - t_1 = \frac{T_S}{2} \qquad (1.3.14)$$

But as shown in Figure 20**Error! Reference source not found.**, v_{ac} is the area of the s haded triangular area. So, the integration result can be given by the area of this triangular area:

$$\Delta v_c = \frac{1}{C}\left(\frac{1}{2}\right)\left(\frac{T_S}{2}\right)\left(\frac{\Delta i_L}{2}\right) \qquad (1.3.15)$$

- From (1.3.6) and (1.3.14) we can get that:
  $$\Delta v_c = \frac{1}{C}\left(\frac{1}{2}\right)\left(\frac{T_S}{2}\right)\left(\frac{\frac{V_0}{L}(1-D)T_S}{2}\right) = \frac{1}{8}\left(\frac{V_0}{LC}\right)(1-D)T_S^2$$

- Δv_c is the ripples component that is to be added to the DC voltage V_0 [8].

1.4. Control Systems for Buck Converter

Although all controllers perform the sole role of delivering necessary control signals for the power stage to produce a stable output voltage irrespective of changes in input voltage, they exist in many configurations with different functions [37, 42, 46]. Here, we will limit our literature review to the major types of controllers (analog, digital, mixed signal) for Buck converter only as it is the configuration implemented in our design.

1.4.1. Analog Controllers

Analog control systems are the conventional types of controllers that served well for a long time because they show superiority in dynamic response as they are faster to achieve closed-loop bandwidth, provide small area and low power. Moreover, they include a variety of approaches that are suitable for different applications. One of basic control systems that employs the voltage-mode approach while mixing it with time-based techniques for controlling the buck converter is illustrated in Figure 21 [40]. Its main components are a voltage divider (to sample output voltage VO and generate a feedback voltage V_{FB}) that is connected to a preamplifier (to amplify the difference between V_{FB}) and V_{REF}). Then, there are two VCDLs (to convert voltage difference to time difference) followed by a phase detector (to generate an UP and DN signals). Then, the charge pump followed by a loop filter is used to drive a PWM by converting UP and DN signals to a charge or discharge current that increases or decreases a control voltage V_{CTRL} to tune the duty ratio generated through the PWM. Additionally, the two power MOSFETs, used as active switches, are preceded by a dead time control module to eliminate losses from switches being on simultaneously. Finally, the off-chip components are the inductor L and capacitor C_0.

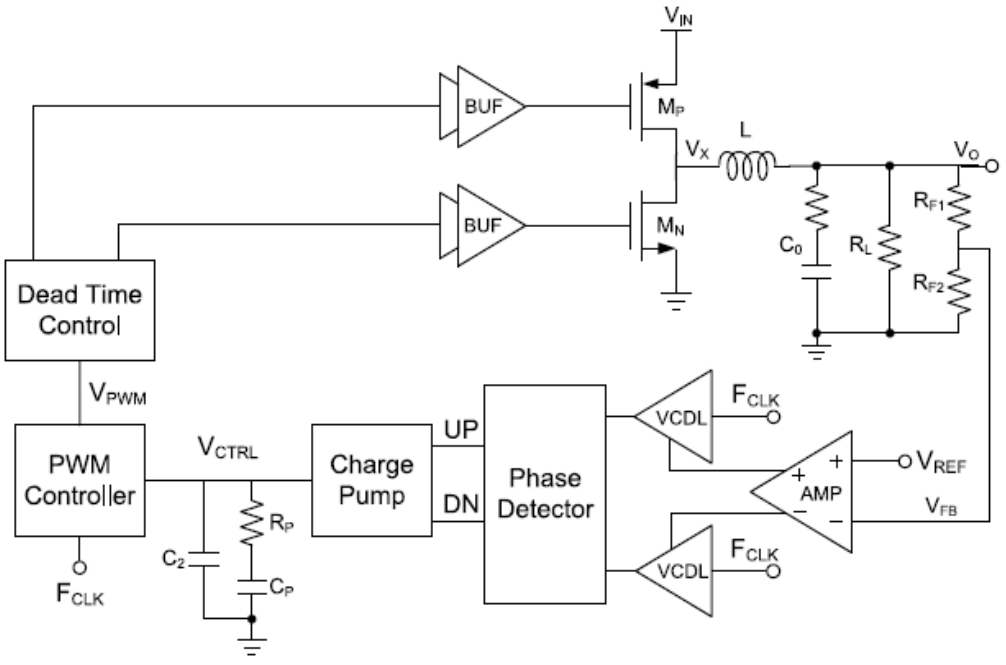

Figure 21: Buck converter control system of [40]

Multiple references introduced innovative time-based controllers that are integrated with the conventional topologies such as in Figure 22. First, Figure 22 depicts a multi-phase buck converter with time-based compensation. This configuration does not need the complex circuitry used to employ active current sharing in an analog controller. Similarly, it does not require any ADC s nor DPWMs of high resolution used to employ passive current sharing in a digital controller. The main components are a time-based (T-PID) compensator, power switches for each phase, and time-based multi-phase generator (MPG) used for producing duty-cycles that are perfectly matched. the T-PID and MPG are designed using digital circuits, there is no quantization error introduced at all. This is because building blocks such as the VCO, VCDL, and PD are of infinite resolution. Consequently, this converter eliminates the unwanted limit cycle behavior usually found in digital controllers [41].

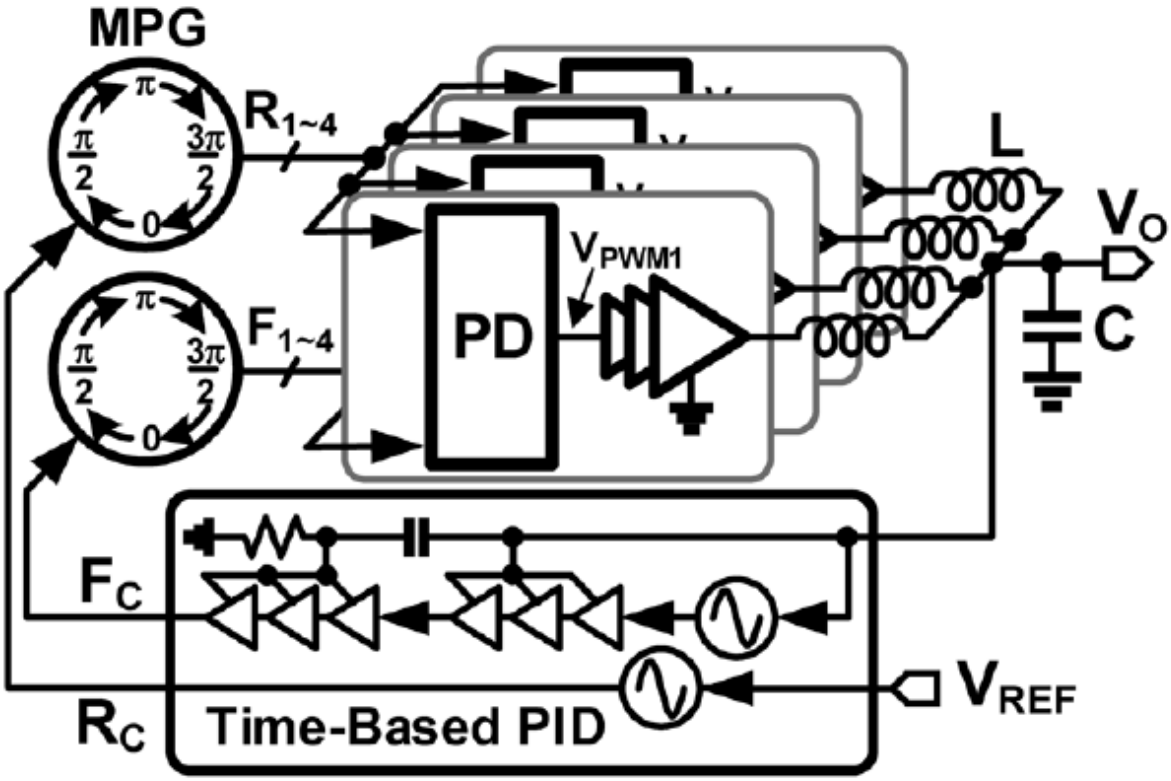

Figure 22: Buck converter control system of [41]

Another time-based compensator was introduced in [41]. It combines the advantages of analog compensators, such as low ripples and high controllability with those of digital compensators, such as noise immunity and small layout area. Figure 23 illustrates its basic operation as follows: the FVCO performs integration of the difference (error) voltage, then conversion into phase ϕ_E . Then, the PD detects the phase difference between ϕ_E and reference phase ϕ_{REF} produced by RVCO and produces the needed PWM signal [41].

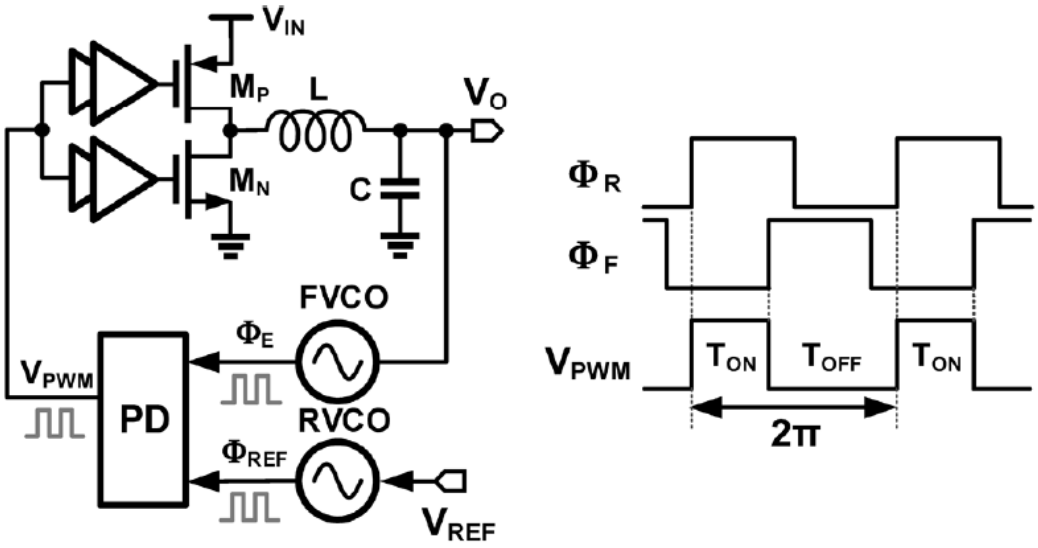

Figure 23: Buck converter control system of [41]

The current control mode is another conventional mode that includes a variety of configurations. For instance, peak current control is the simplest control method for DC-DC converters, but it suffers from the subharmonic oscillations specially, when the duty ratio is greater than 0.5 [44]. On the other hand, average current control is used for reducing the subharmonic oscillations by sensing the average of the inductor current [45]. There is also Nonlinear Average Current Mode control, where switch current is sensed and used for the feedback signal as depicted in Figure 24 [46]. This current control method does not require current compensator, controls the output voltage and is attractive for low power applications owing to the possibility to integrate the control circuitry with the power switch and its improved efficiency.

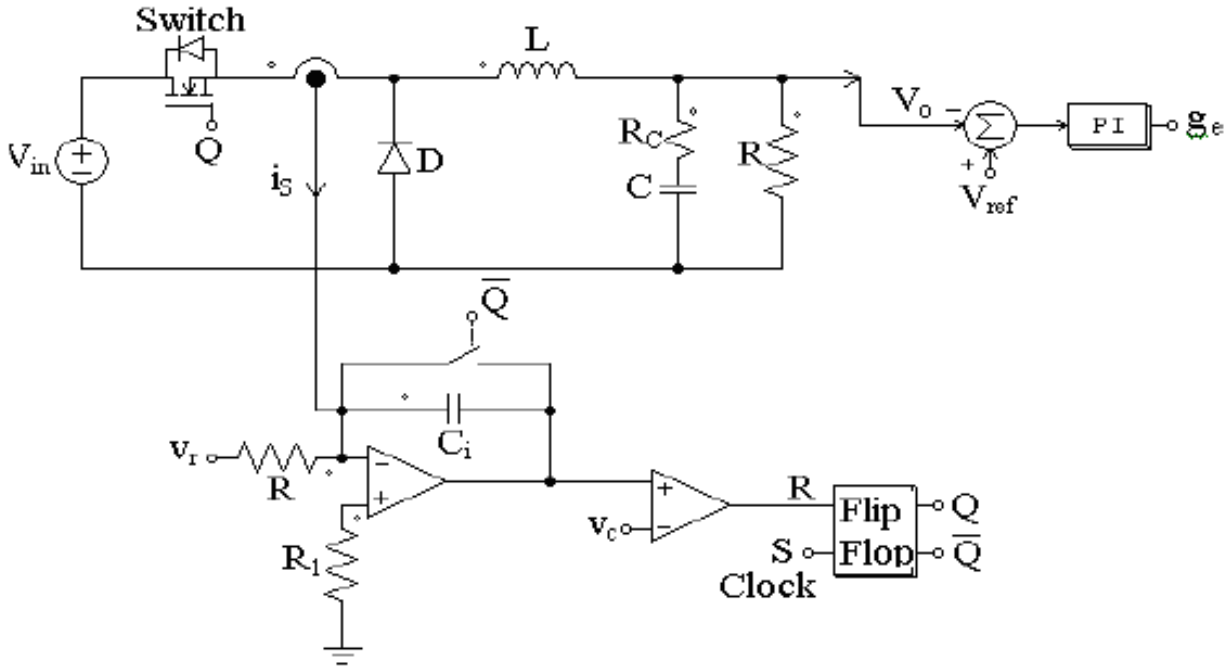

Figure 24: Buck converter control system of [46]

1.4.2. Digital Controllers

The disadvantages of analog controllers have strongly pushed towards the introduction of digital controllers for buck converters. For instance, the analog circuitry is largely complicated with a high count of components. Additionally, it is not easy to modify the design once completed. On the contrary, digital controllers are the perfect candidate for coping with the ever-going down-scaling of the switching power supply with smaller CMOS processes. This is because they have flexibility and are easy to program and correct. Also, the design cycle is not long, and the number of components is minimized. One of digital control systems for the buck converter is illustrated in Figure 25 [42]. The power stage is implemented using the conventional components of the buck converter: The power switch, LC filter, and the load. Regarding the digital control stage, it is composed of three principal blocks: an ADC (analog digital converter) to digitize the error between the reference voltage and the output voltage, and then send it to the second block, The DPID (digital compensator). As the name suggests, this block compensates the whole loop and inserts the signal of the computed duty cycle to the final block, DPWM (digital pulse width modulator). The DPWM then produces control pulses to drive the switch to obtain the desired adjusted output voltage, according to the feedback cycle.

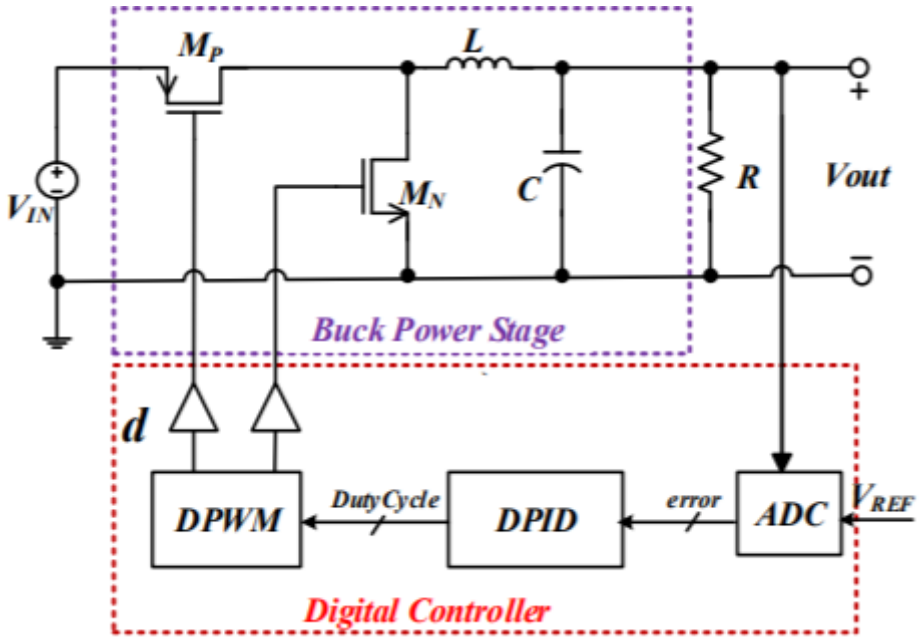

Figure 25: Buck converter control system of [42]

1.4.3. Mixed-signal Controllers

There are many attempts to mix both the analog and digital control systems to get both of their advantages, while overcoming their limitations. For example, one of these mixed control systems for the buck converter is depicted in Figure 26 [37], its operation principle is as follows: the error amplifier performs comparison between the reference

voltage and output voltage. As a result, an error voltage signal is generated at its output. Moreover, V_{OS} is offset voltage and it functions as a method of biasing the generated error signal to the voltage-controlled oscillator's (VCO) region of operation. On a side note, conventional references such as [38, 39] would convert the error voltage to a digital signal using an ADC. After that, the VCO' output acts as a counter 's clock signal. The counter then produces a binary number that is processed to produce a digital error signal called e(n). d(n) signal is generated in the PID compensator and sent to the PWM generator. Finally, the binary digit is transformed into a change in duty cycle and then utilized for controlling the active switch of the converter [37]. The advantages of this controller are easy tuning of the controlling parameters for driving different loads and wide output voltage range. On the other hand, disadvantages are the same as other digital controllers: quantization errors, high output ripples, degraded transient response, requiring high-precision ADC and PWM modules [37-39]. However, the topology in [37] overcomes the problem of ADC and PWM generators by implementing the scheme explained earlier.

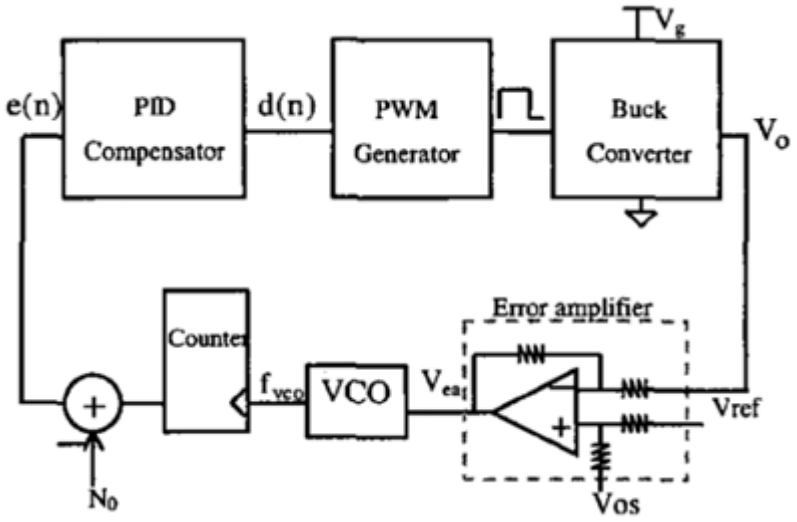

Figure 26: Buck converter control system of [37]

1.5. Motivation

1.5.1. Why mixed signal control:

The literature review on different conventional and novel control systems for DC-DC Buck converters gives us insight on advantages and disadvantages of each approach of designing the controller. For instance, digital control systems have the upper hand regarding accurate output voltages as they are immune to component variations and they can implement advanced control schemes with system diagnostics and autotuning features. Nevertheless, high area, offset error, high power consumption, and low efficiency remain serious issues compared to analog control systems [47-49]. Additionally, even though analog control systems show superiority in dynamic response as they are faster to achieve closed-loop bandwidth, and provide small area,

low power, they still introduce the problem of high settling time, output noise and ripples [48, 49].

For the trade-offs stated earlier, our project is based on a novel mixed signal design of the control systems used for the buck converters. Mixed-signal designs are characterized by the stability and algorithmic abilities of digital logic to control high-performance analog circuitry [49]. Additionally, digital logic is easy to modify and more immune to process variations. That is why it is preferable to design most of the control loop with digital blocks and keep the analog components as simple as possible [50]. Furthermore, our mixed-signal design attempts to overcome each approach's limitations, while taking advantage of their strengths combined. For instance, it exhibits relatively small area, low power consumption, and higher efficiency when compared to digital controllers alone. Also, the output voltage accuracy is enhanced, and offset error is nearly eliminated. Additionally, the addition of PLL enhances controllability of the system even though there are digital modules.

Regarding the analog part in the control system, there are two main approaches for sensing the output signal and feeding it back to the system through the controller to adjust the signal as required: First, single loop control or voltage mode where only one feedback loop is used and it feeds the PWM module. It has advantages of stable modulation, less noise sensitivity, simplicity (single feedback path), and applicability over a broad range of duty cycles. However, this mode has slow response to input voltage variations and its loop gain is proportional to input voltage [7, 40].
Second, two-loop control or current mode which has an additional inner current loop that is used along with the outer voltage loop. Unlike voltage mode, it has advantages of cycle by cycle current limitation, better response to input voltage change, and covering a broader range of frequencies due to its inner current loop. On the other hand, it adds the issue of sense resistor and subharmonic oscillations at duty cycle larger than 0.5. Additionally, it is more complex (two loops) and it is difficult to produce substantial current sense signals [44-46]. That is why we chose the voltage mode in our design and added adjustments to overcome its shortcomings. For instance, the output voltage is fed back to the system and compared with the reference voltage using an error amplifier. Then, the error (voltage difference) is digitized using ADC and turned into time difference by using two DCO's that generate two signals that have frequency and phase difference. This time difference is then detected by a PFD and continues through the system to generate a voltage signal that controls the PWM duty cycle. This time-based approach overcomes the problems of conventional voltage control mode and eliminates the need for high resolution ADCs and wide bandwidth amplifiers [49, 50].

1.5.2. Why high frequency:

In addition to mixed-signal controlling, our project targets working at high frequency for the following reasons: First, it is responsible for reduction of chip layout area because high frequency operation allows for decreasing the capacitance and inductance

in the circuit, which allows for on-chip implementation [51]. This is of great significance since there has been a growing demand for high-speed on-chip power supplies for portable electronics, which requires on-chip components and minimum chip area [52]. Additionally, because values of inductance and capacitance are inversely proportional to switching frequency, and the tracking bandwidth of the control loop increases proportionally with it, the most plausible approach to achieve both fast-tracking response (improved transient response) and small form factor is working at high switching frequency.

Second, it results in ripples enhancement as ripples are one of the main concerns in the design of buck converters. Although the RC circuit at the output tends to reduce ripples and stabilize the output, large capacitance and resistance values are still necessary. Thus, high frequency operation aids in ripples reduction without having to increase RC values since the output voltage will not take much time to move higher or lower than the desired value [53].

Third, it allows for duty cycle extension. This happens because buck converters can perform in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) (where inductor current reaches zero). For DCM, the inductor current is allowed to fully discharge and reach zero. Also, the output voltage is not only a function of the input voltage and duty cycle, but also is dependent on the inductance, frequency of operation and load resistance. On the other hand, the inductor current in CCM never reaches zero and the output voltage is dependent on input voltage and duty cycle only. Consequently, the duty cycle is limited to a small range that is defined by the inductor current. Therefore, a high frequency operation is required to extend the duty cycle [8, 53].

However, increasing the frequency involves many challenges regarding the efficiency and design of the system because high frequency operation implies high dynamic power and switching losses (heat dissipation) which degrades the overall efficiency. That is why we ensured that the system components are capable of handling being subjected to rapid and periodic voltage and current excitations. Moreover, area, transient response, and ripples are optimized to achieve the highest possible efficiency at high frequency operation [8, 52, 53, 54].

2. System Components

2.1. Error Amplifier

2.1.1. Overview

An error amplifier is what its name says, that is, it amplifies an error signal. The error is the difference between the reference voltage and the output voltage. The error amplifier is a two-stage conventional operational amplifier. The first stage is a differential stage and the second one is a high gain stage. The op amp is in the subtractor

configuration as shown in Figure 27. If resistances are equal (R2 = R4 and R1 = R3) then the output voltage is as given in Figure 27.

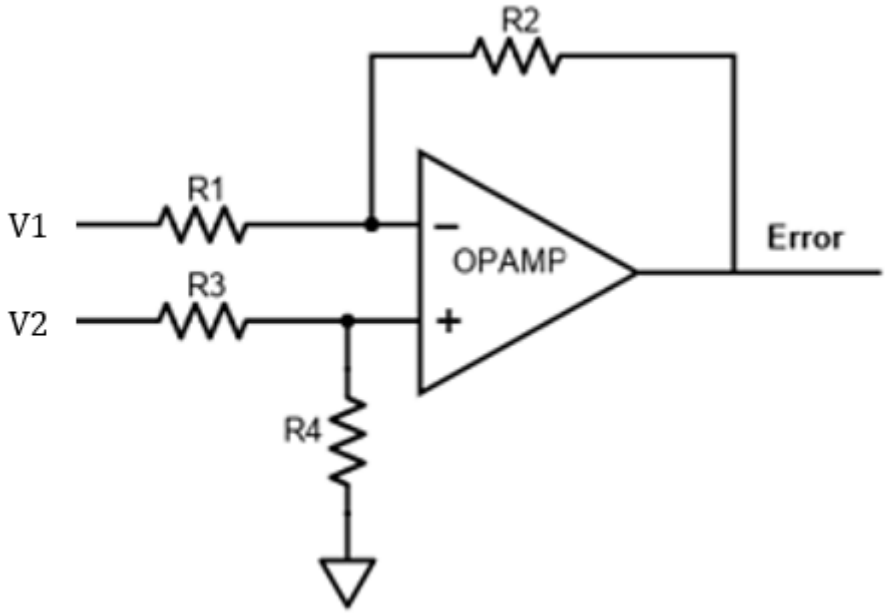

Figure 27: Op-Amp subtractor configuration

$$Error = \frac{R_2}{R_1}(V2 - V1)$$

2.1.2. Schematic

The schematic used in the design is shown in Figure 28. The gain is set to be 18 since we need the system to lock only once, we have very small offset value. Two buffer unity gain op amps are used to isolate the input signals to the resistors. V_{out} and V_{ref} are being subtracted and the difference is multiplied by 18.

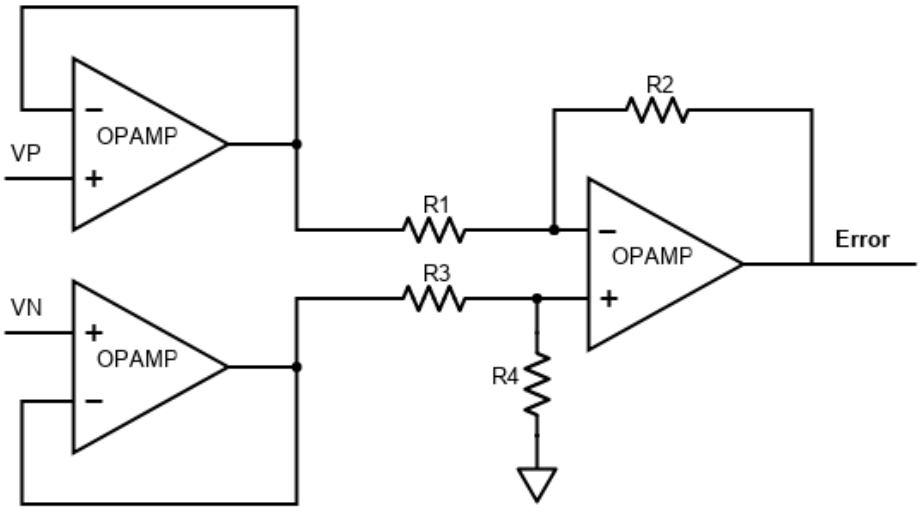

Figure 28: Schematic of implemented EA

2.1.3. Layout

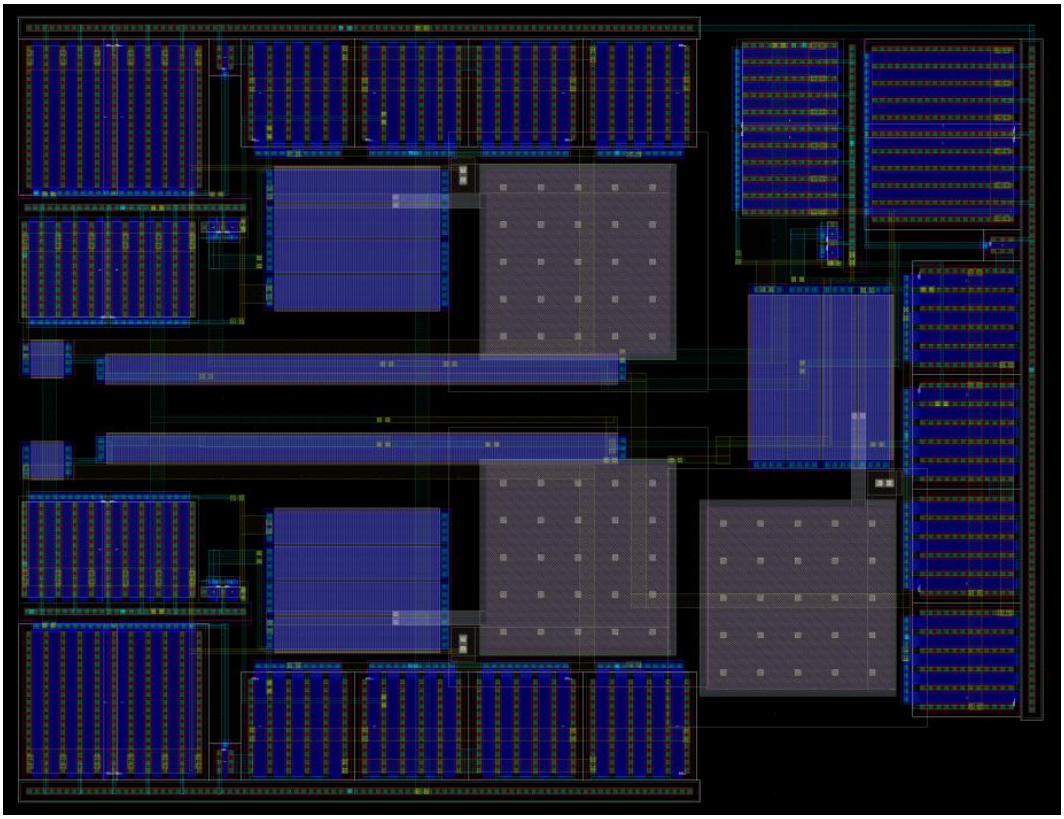

Figure 29: EA Layout

2.1.4. *Output Results*

A simulation for V_{ref} is 0.6 is demonstrated here. In Figure 30 The output voltage is swept from 0.6 to 0.69. it is noticed that the error is linear with the sweep and is constant with time. When the two input signals are equal, the error is nearly zero or less than 30m. This happens mainly when settling is reached and v_{out} is equal to v_{ref}. Figure 31 shows the power of the error op amp for different output voltage. For large values of v_{out}, the power decreases significantly.

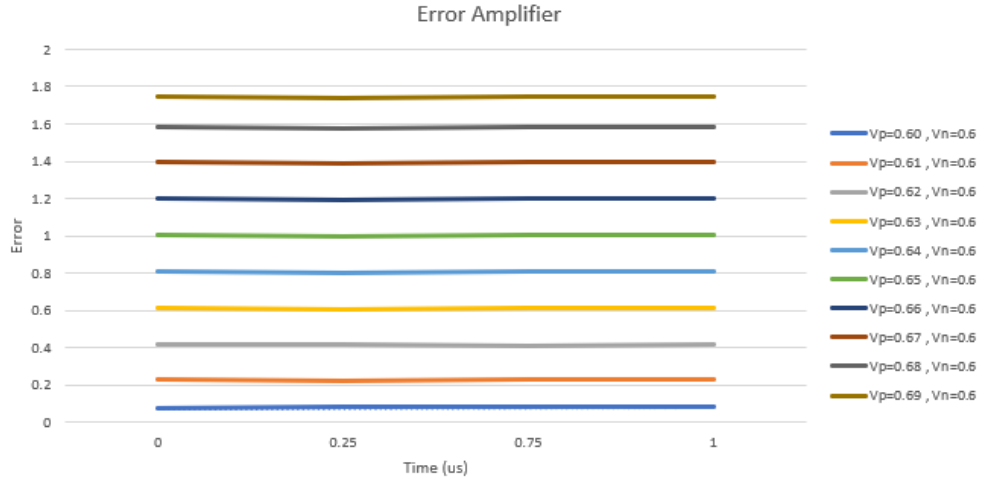

Figure 30: Output error for different v_{out} at v_{ref}=0.6

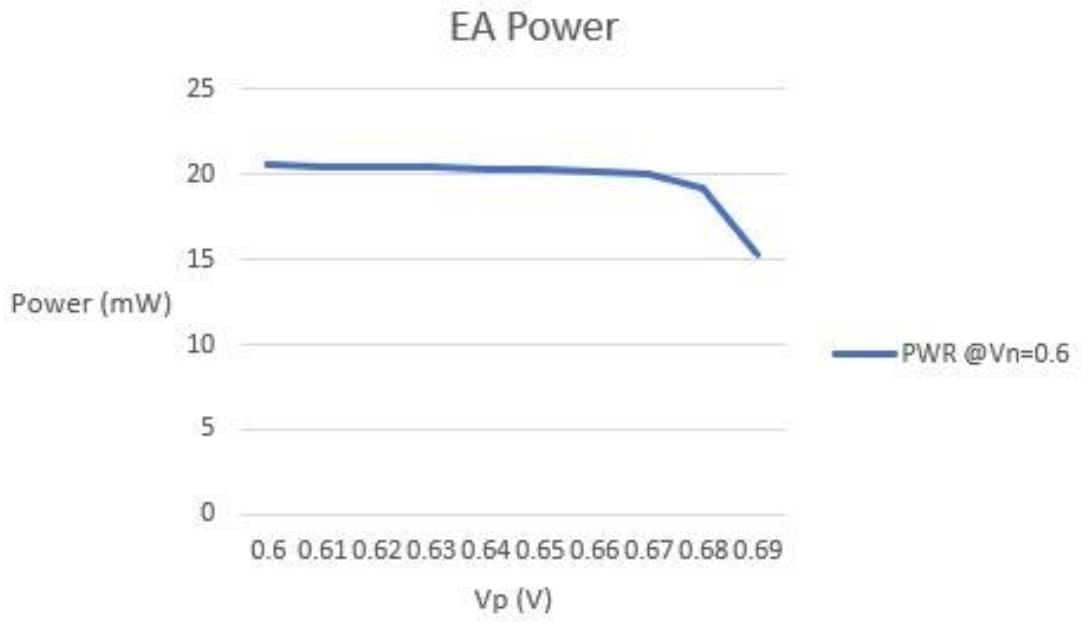

Figure 31: Power of the EA for different v_{out} values

2.2. Analog to Digital Converter

2.2.1. Overview

Due to the high operating frequency of the control system, a high-speed ADC design is required, this design should also compromise the trade-offs between speed, area, and power consumption. For these reasons, a 2-bit flash ADC architecture is implemented. The parallel architecture's $(2^N - 1)$ comparators provide the highest speed an ADC can provide [56], and the low 2-bit resolution minimizes the area and power consumption while maintaining the system's functionality.

2.2.2. Schematic

The design schematic is shown in Figure 32. The architecture is obtained from [56]. The reference voltage "V_{DD}" is divided into 4 values with equivalent voltage drop through each of the four matched resistors, Each resistor level's voltage is compared with the input voltage "V_{IN}" resulting in a thermometer code at the comparator's output, the code is all zeros if the value of V_{IN} is less than the resistor levels and result in ones at a resistor level when V_{IN} is more than or equal the voltage at the level's node. The thermometer code is then fed to a 3:2 digital encoder that determines the ADC's 2-bit word output. Table I shows the corresponding thermometer codes, output bits, and decimal values for the output bits multiplied by V_{DD} for different ranges of V_{IN}.

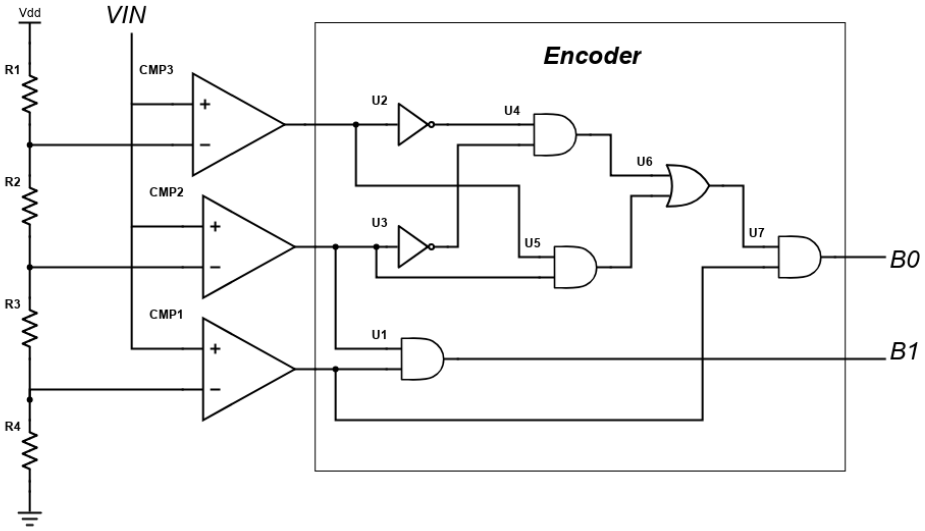

Figure 32: Schematic of implemented ADC

Table I : ADC outputs for different ranges of V_{IN}

V_{IN} range	Thermometer Code	2-Bit Word (ADC Output)	Corresponding Decimal Value × V_{DD}
0 – 0.45	000	00	0
0.45 – 0.9	001	01	1.8
0.9 – 1.35	011	10	3.6
1.35 – 1.8	111	11	5.4

2.2.3. Layout

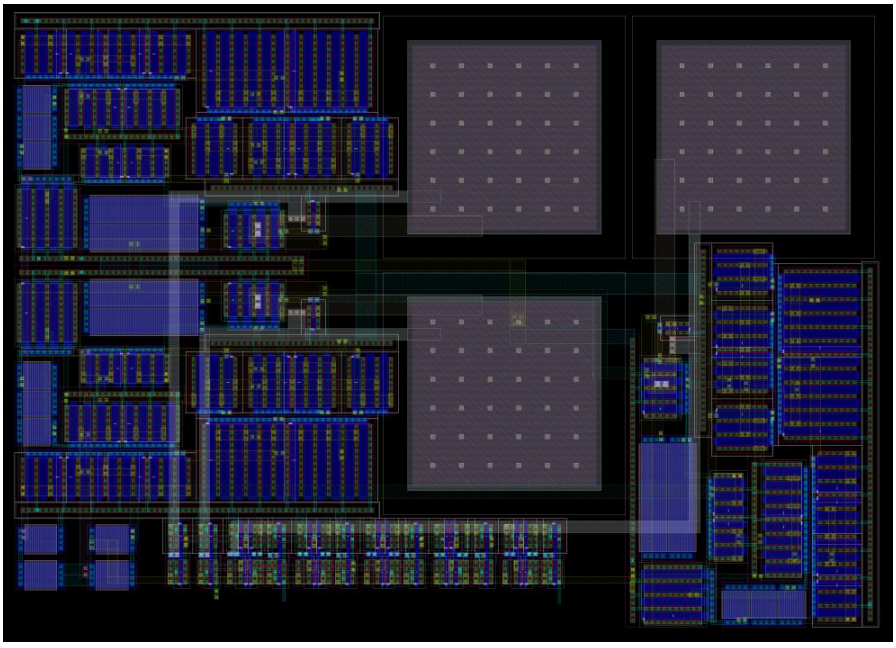

Figure 33: ADC Layout

2.2.4. Output Results

Figure 34 shows the relation between the ADC output and V_{IN} pre and post layout. The functionality is well maintained pre and post layout. Pre-layout power consumption is 3.8912 mW while Post-layout power consumption is 4.07609 mW. The slight increase in the layout's power consumption is due to the power consumed by parasitic resistances and capacitances caused by wiring.

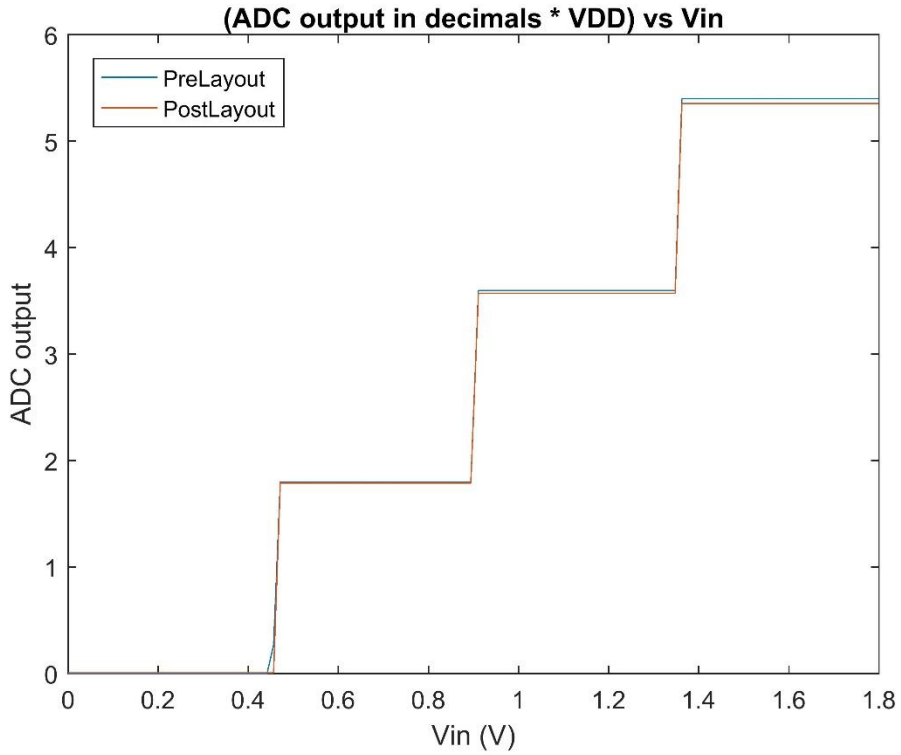

Figure 34: ADC output bs V_{IN} pre-layout and post-layout

2.3. Phase Frequency Detector

2.3.1. Overview

Phase frequency detector detects the difference in the phase and frequency between the two input signals, the reference frequency, and the feedback frequency. If the reference frequency leads, UP signal will be the output and the DOWN signal is zero. If the feedback frequency is leading, the DOWN signal will be the output wave and UP signal is zero.

2.3.2. Schematic

It consists of two master slaves flip flops with reset NAND signal as shown in Figure 35. The operation of this PFD is negative edge trigger. The output signal is the difference between the two input signals fall edges.

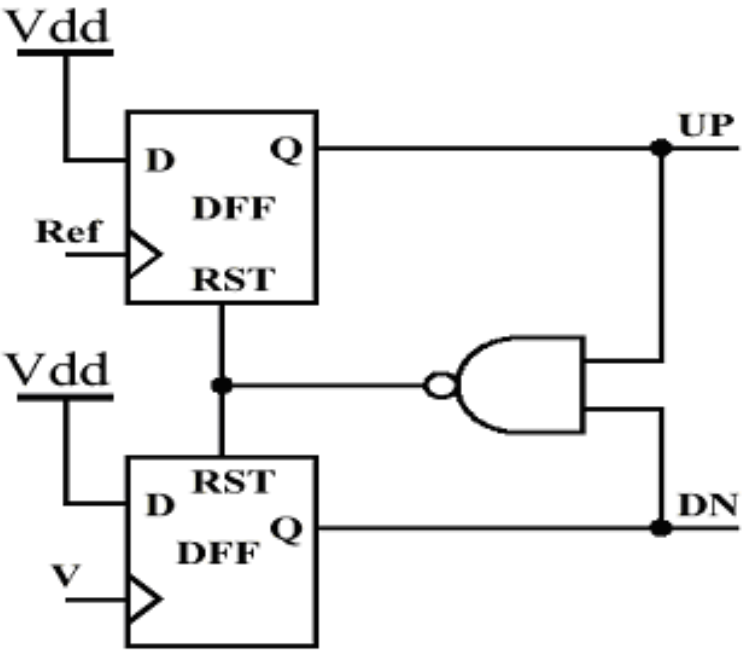

Figure 35: Schematic of implemented PFD

2.3.3. Layout

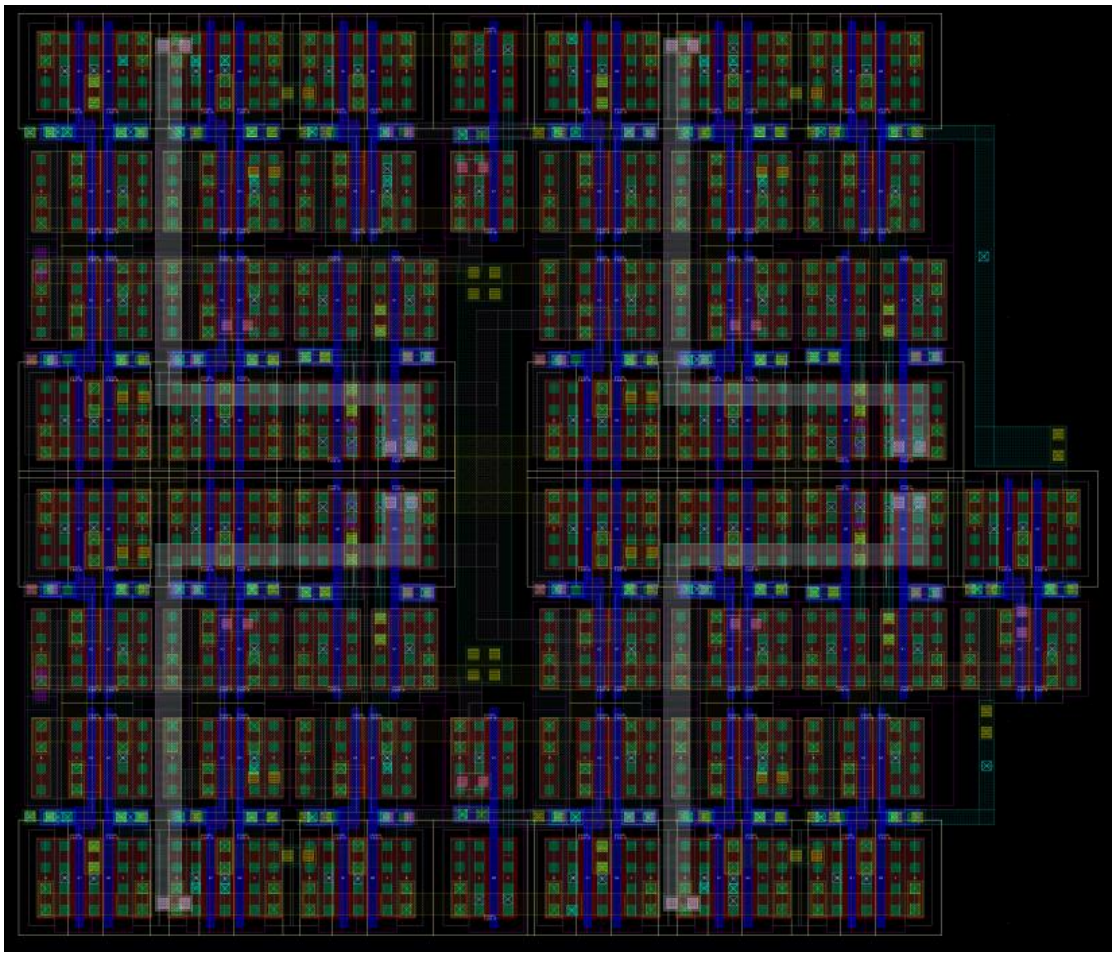

Figure 36: PFD Layout

2.3.4. Output Results

Figure 37 shows the case of the reference frequency leading the output frequency. The UP signal is triggered once V_{ref} signal falls and it continues until the negative edge of the output frequency also drops. The signal is the difference between them.

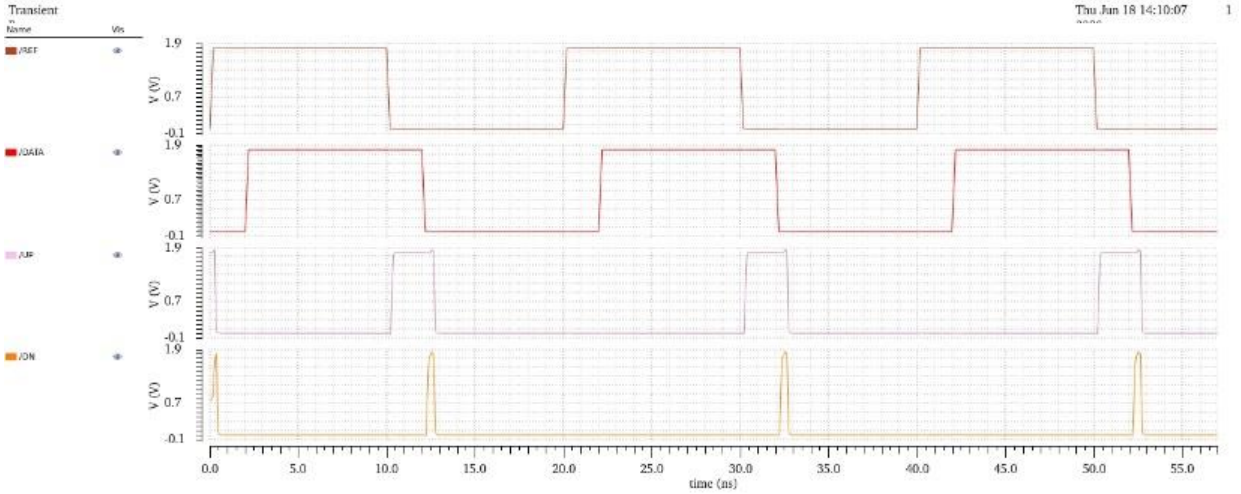

Figure 37: Reference frequency signal leading the output frequency response

Figure 38 shows the case of the output frequency leading the reference frequency. The DOWN signal is triggered once V_{out} signal falls and it continues until the negative edge of the reference frequency also drops. The signal is the difference between them.

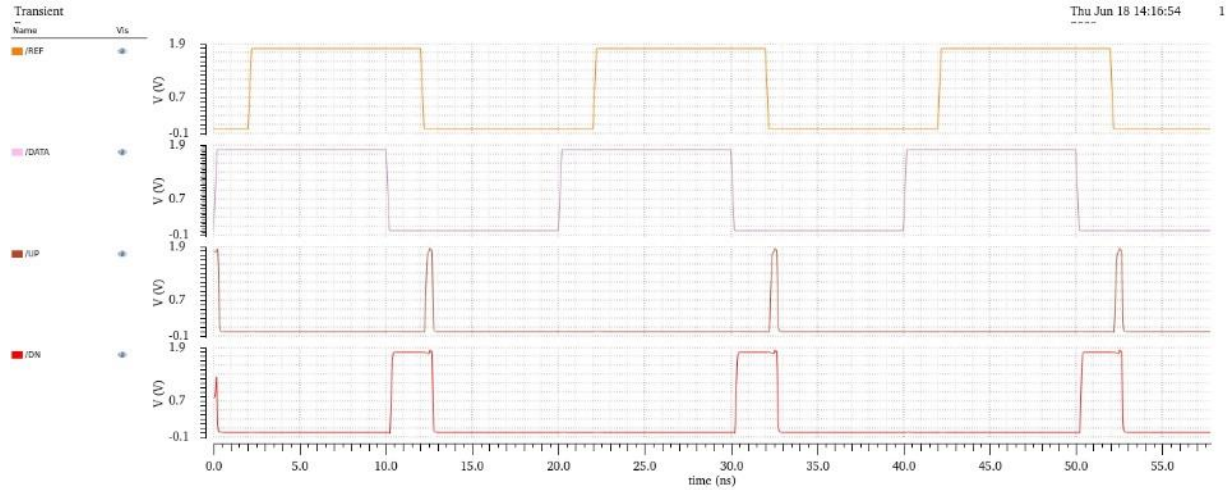

Figure 38: Output frequency signal leading the reference frequency response

2.4. Charge Pump

2.4.1. Overview

Charge pumps is two controlled switching transistors that add charge or discharge current from current sources into a capacitors circuit as shown in Figure 39. When the upper transistor is connected (UP signal is on), the current source starts charging the capacitor. At this time the control voltage starts increasing. When the lower transistor is connected (DOWN signal is on) and the capacitor discharges. This leads to decrease in the control voltage.

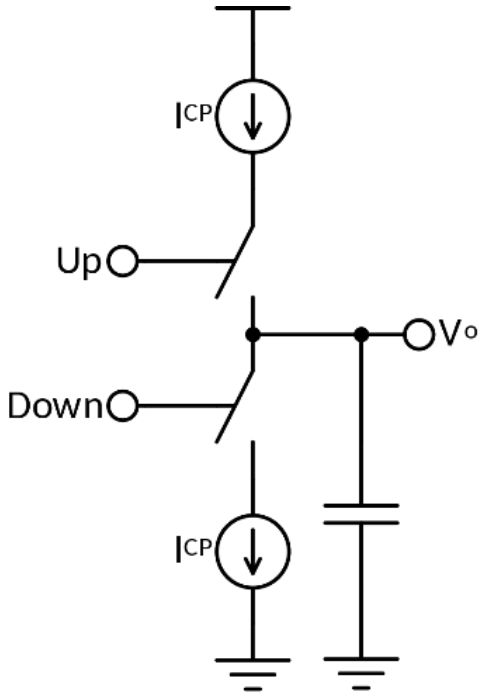

Figure 39: Principle of operation of charge pump

2.4.2. Schematic

The schematic of the used charge pump is shown in Figure 40. The left and the right circuits are current circuits working as current sources. When the reference signal is leading, up is one and the control voltage increases to raise the output voltage of the buck. When the output voltage exceeds the reference value, the down signal is on and the control voltage decreases to decrease the output voltage. The CP is connected to LPF to work as a capacitor circuit.

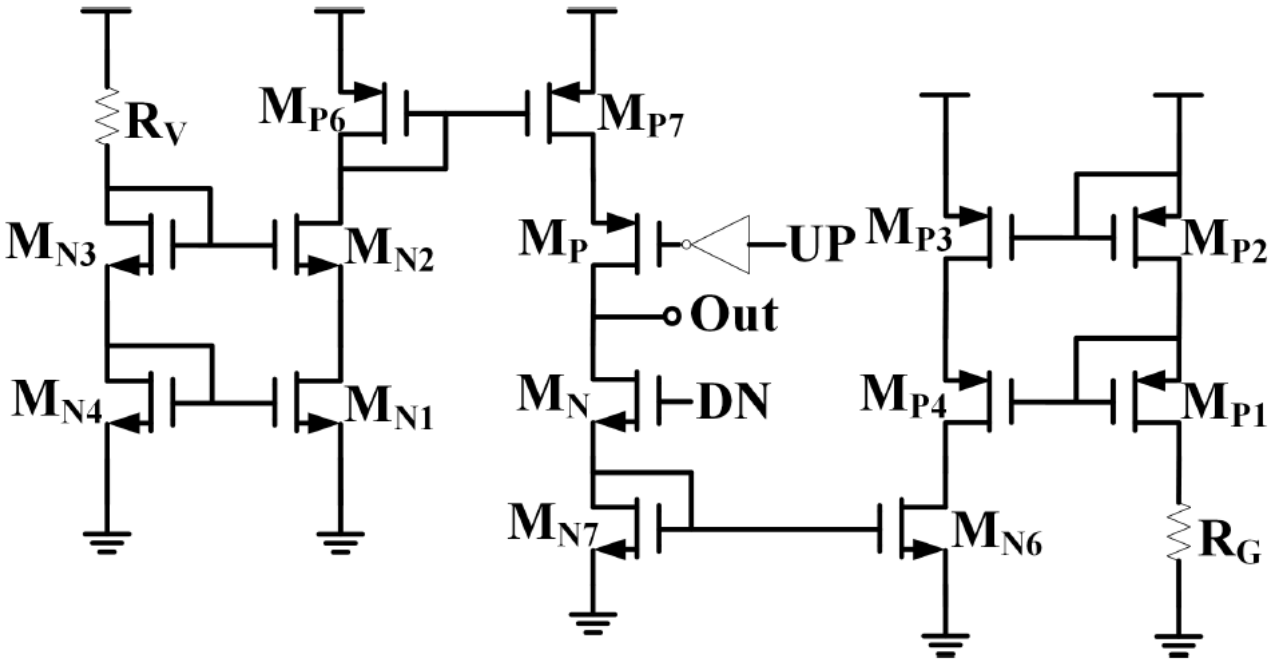

Figure 40: Schematic of the implemented charge pump

2.4.3. Layout

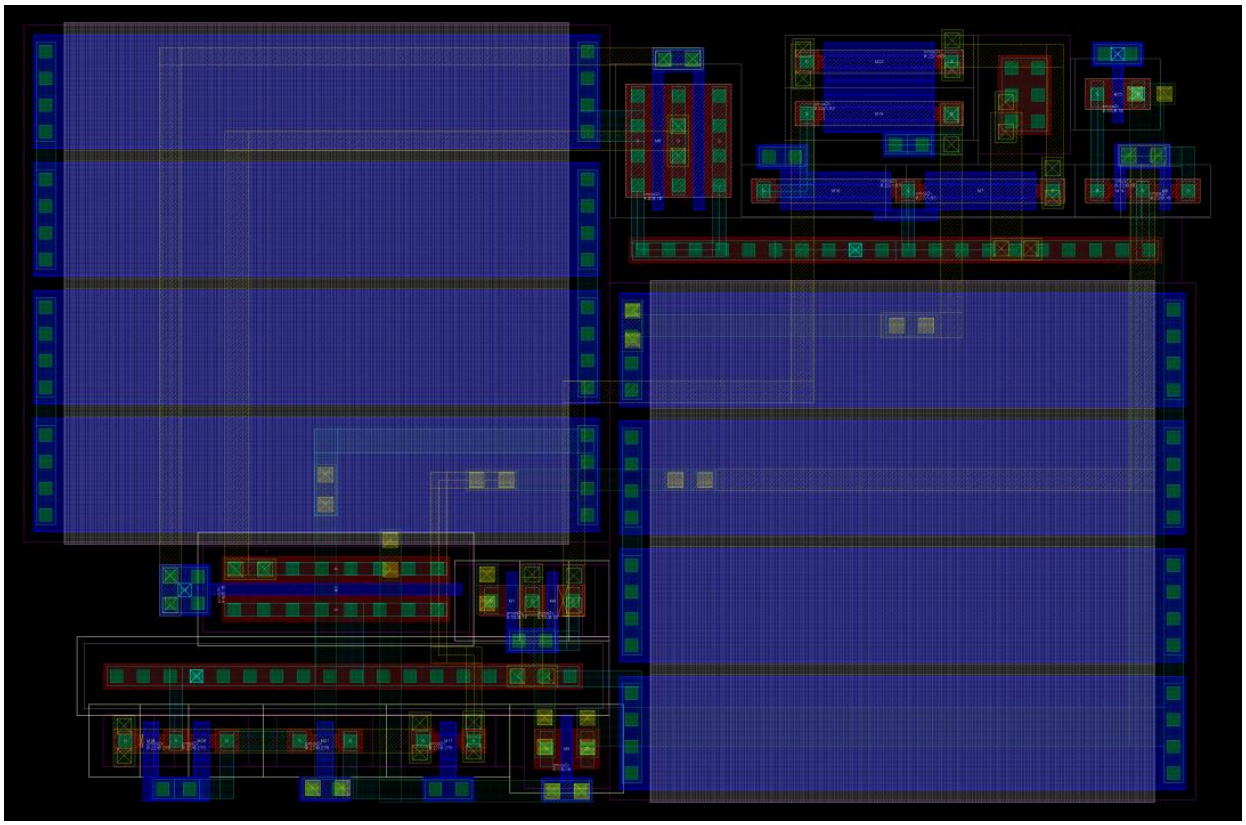

Figure 41: CP Layout

2.4.4. Output Results

Figure 42 shows the output results of the implemented charge pump. As shown, it is important to keep the current symmetric as much as possible. When the UP signal is on, the current goes out of the charge pump and the voltage increases. The current is around 2.4 µA. When DOWN signal is on, the current is around 2.8 µA.

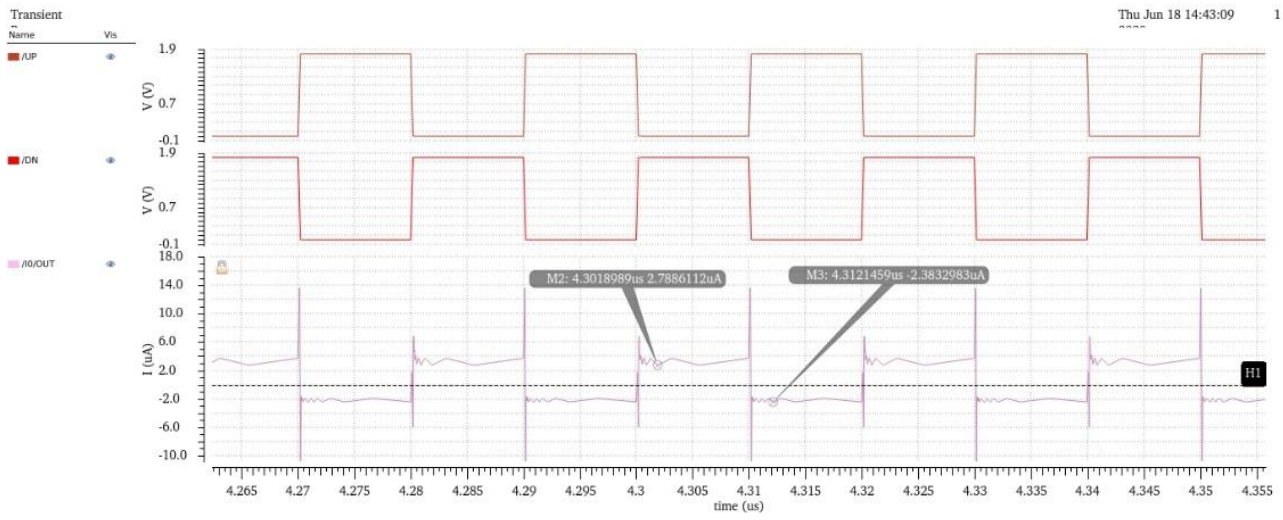

Figure 42: Chare pump behavior

2.5. Pulse Width Modulator

2.5.1. Overview

The design generates an output signal V_{PWM} based on the value of a V_{CTRL} signal by fixing one edge of the CLK and controlling the other edge to change the duty cycle. The design is a replacement to the traditional ramp-comparator-based PWM generator to relieve the design from limitations caused by comparator delays at Very High Frequency (30-300 MHz) operation where nanosecond delays can cause serious restrictions on the control system [49, 55].

2.5.2. Schematic

The PWM circuit design is obtained from [40]. The schematic of the delay-line-based voltage to duty cycle V2D controller is shown in Figure 43.

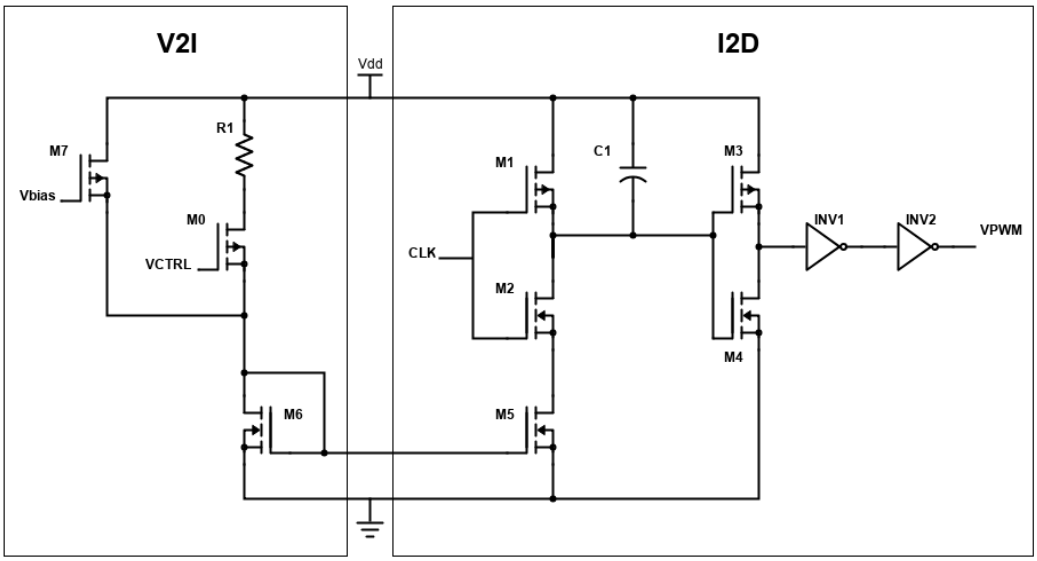

Figure 43: Schematic of implemented PWM

The circuit is divided into two stages

- A Voltage to current V2I stage where V_{CTRL} is converted to current I through a typical current circuit.
- A current to duty cycle stage I2D where the current "I" is converted to V_{PWM} through a current starved delay cell.

When CLK signal is zero, the PMOS M1 is ON which shorts the capacitor's terminals with each other, leading to discharging the cap and V_C rises (ideally to V_{DD}) taking V_{PWM} to zero. When CLK signal is one (V_{DD}) the NMOS M2 is ON which shorts the capacitor's second terminal to the ground leading to the charging of the capacitor and V_C starts decreasing gradually until it falls below the threshold voltage of the MOSFETSs of the next inverter stage taking V_{PWM} up to V_{DD}, therefore controlling the rising edge and the duty cycle of V_{PWM} [40].

Based on the current drawn from the V2I stage, the timing between the rising edge of the CLK and before V_C falls below the transistors' threshold voltage "t_d" can be controlled, which means the rising edge and the duty cycle of the modulated V_{PWM} signal can be controlled. t_d is determined through the equation

$$t_d = \frac{C \cdot (V_{DD} - V_{TH})}{I}$$

As V_{CTRL} changes the drawn current by the V2I circuit changes and therefore the duty cycle changes [40].
Due to the high operating frequency (200 MHz) V_C does not reach V_{DD} but reaches a certain voltage depending on the drawn current and as the duty cycle increases the oscillations take place around a higher voltage.

2.5.3. Layout

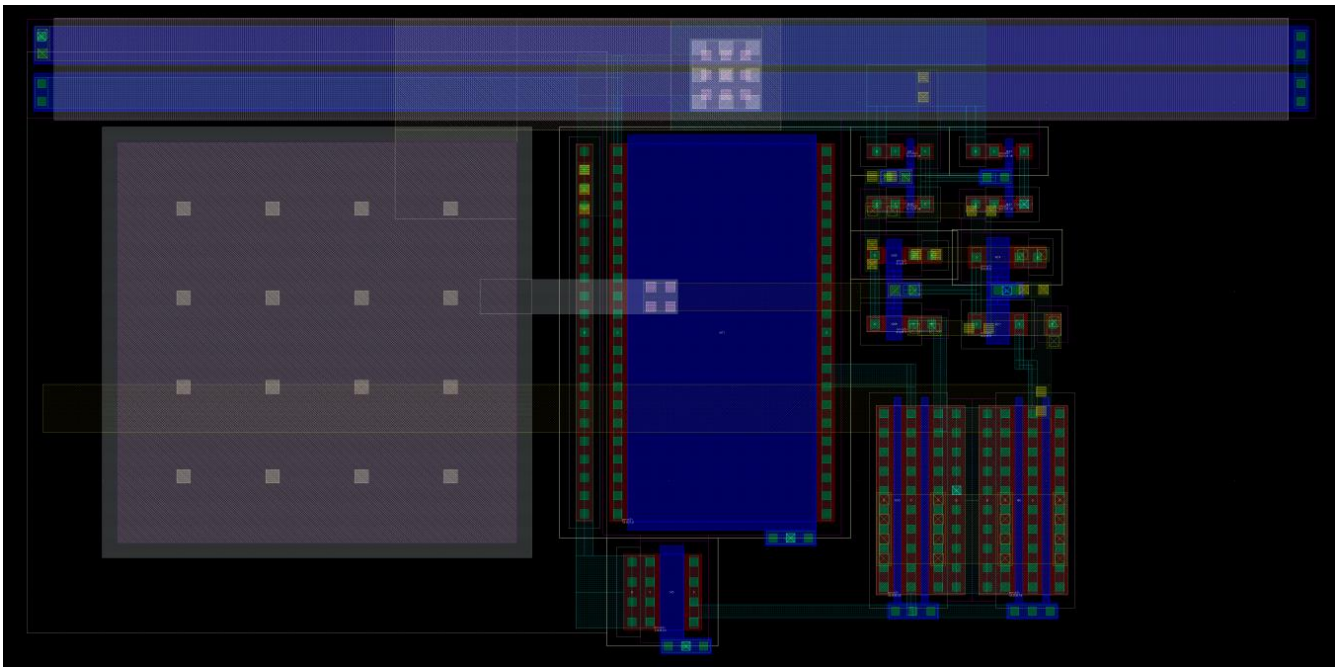

Figure 44: PWM Layout

2.5.4. Output Results

Figure 45 and Figure 46 show the simulated duty cycle and the power consumption respectively, each of them plotted corresponding to different values of the control voltage V_{CTRL} and each is simulated pre and post layout. The pre-layout duty cycle range is 5.684% - 96.1% while the post-layout range is reduced to 4.188% - 87.43%. V_{CTRL} pre-layout range is 0.29V - 1.33V while post-layout range has increased to 0V - 1.38V. The Post-layout power consumption is lower than that of the pre-layout's because the drawn current by the circuit is less in the post-layout case since the duty cycle range is reduced.

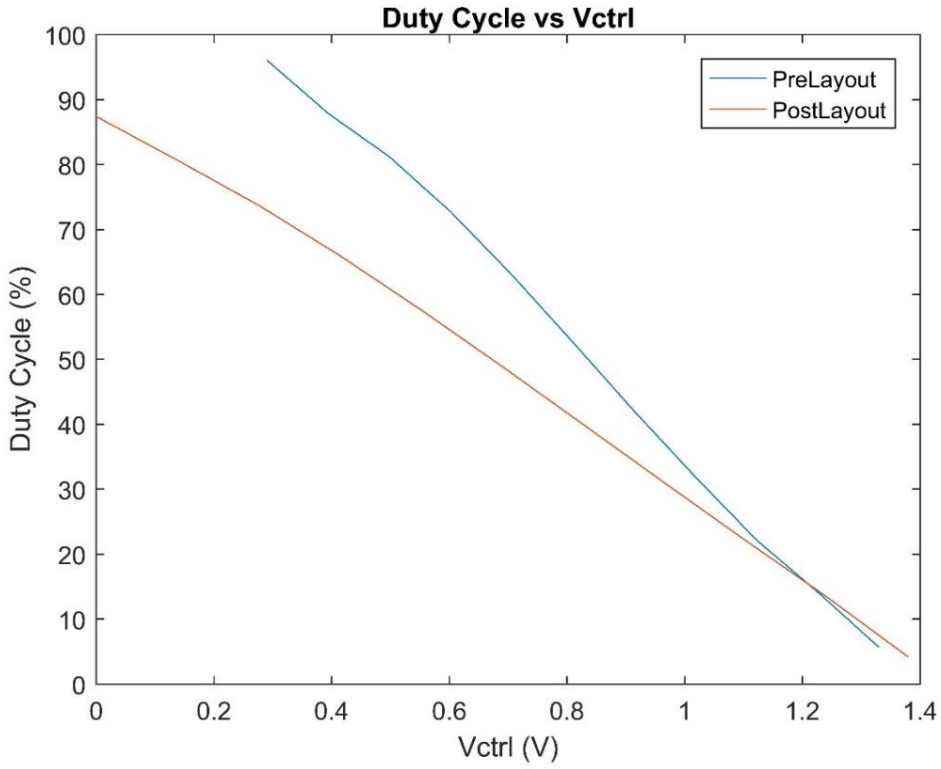

Figure 45: Duty Cycle range pre and post layout

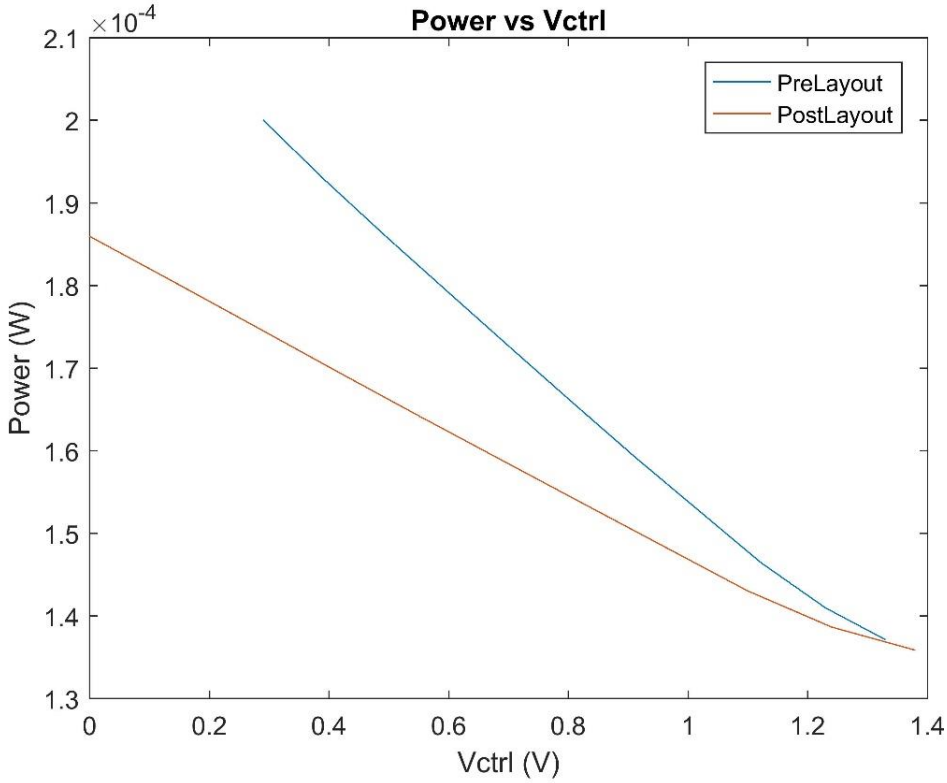

Figure 46: Power consumption pre and post layout

3. System Performance

3.1. Phase Locked Loop

3.1.1. PLL Working Principle

The PLL is a critical subsystem of the design. It is responsible for comparing the feedback signals from the buck output to the reference signal. Upon this comparison the control signal is set to achieve the proper duty cycle of the PWM until it reaches the lock condition or the steady state. The schematic of the PLL is shown in Figure 47.

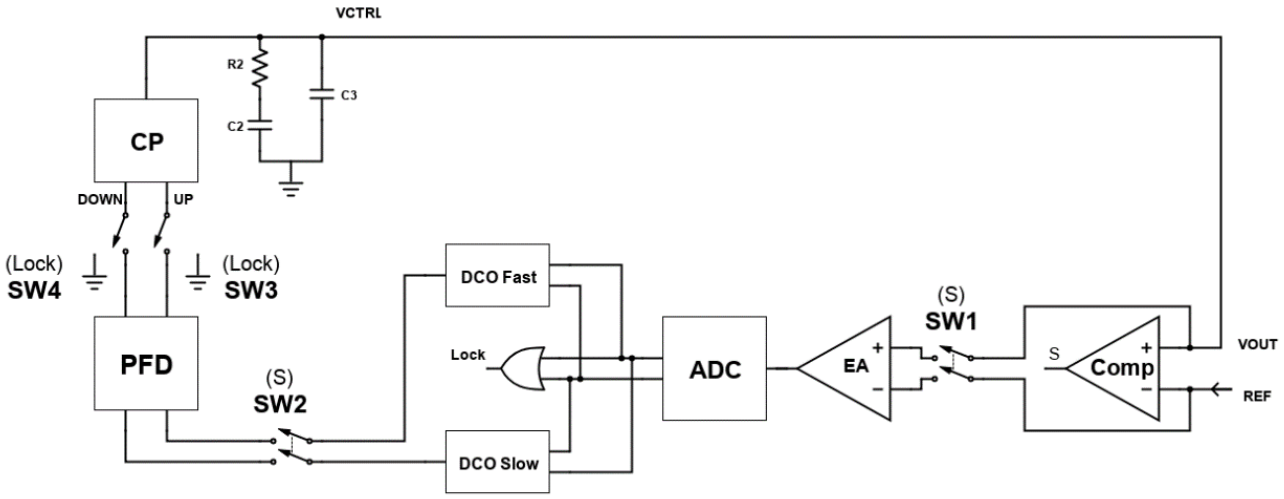

Figure 47: PLL block diagram

To simply understand the operation of the proposed PLL one of 3 cases will be addressed at a time.

First case, the reference voltage is greater than the feedback voltage (V_{ctrl}). In this case the reference voltage is connected to positive terminal of the error amplifier (EA) and the feedback voltage is connected to the negative terminal. The EA amplifies the difference by the gain. In this design the error amplifier gain is 20. The error signal goes as an input for the 2bit flash ADC. Flash ADC is used for its high speed. Moreover, only 2bits are needed so the area will not be large. Based on the digital representation of the errors both DCOs will generate two different frequencies. DCO1 will generate the higher frequency. The two DCOs signals are fed to the PFD which generates up and down signals based on the phase and frequency difference between the DCOs signals. Up and down signals will control the charge pump switches to push or pull current in the loop filter. In this case the current will be pushed in the loop filter causing V_{ctrl} to increase.

Second case, the feedback voltage is greater than the reference. For design purposed the larger signal should be connected to the positive terminals of the EA. To handle this a switch (SW1) is added before the EA which ensures that the greater signal is connected to the positive terminal. This switch is controlled by a comparator signal which indicates which is the larger signal. At this point the signals flow will be the same as in the previous case. The only difference in this case is a switch (SW2) is added before the PFD. SW1 switched the pass in order for the EA to work properly and then

SW2 switched the pass again, so the signals flow as needed. Then the charge pump will pull current from the loop filter and V_{ctrl} will decrease.

The last case, V_{ctrl} is nearly equal to the reference voltage. At this case the error is very small so the ADC outputs will be zeros. The outputs are connected to a NOR gate. If the ADC outputs are zeros -the error is very small- then this NOR gate output is 1. For a better settling time, at this condition (NOR gate output is 1) the charge pump inputs are forced to ground by switches controlled by the NOR gate. So as soon as the system reaches its desired value it will lock. This sudden lock can be noticed from simulation as shown later.

Generally, the PLL works in one of two regions: lock region and non-lock region. In non-lock region the signals flow through the comparator, switch1, EA, ADC, DCOs, switch2, PFD, CP and finally through the loop filter. However, in lock region the signals take the highway from ADC to NOR the CP directly and stops it from pulling or pushing current in the loop filter.

One of the main factors to evaluate the PLL performance is the LOCK condition -the condition at which the V_{ctrl} will settle -. In this design the lock condition will occur whenever the ADC outputs are zeros. With 2bit flash ADC with reference 1.8V, any voltage that is less than 450 mV (1.8VAA 4-/4 levels) will be zero at the output. This condition occurs whenever the difference between reference voltage and V_{ctrl} is less than 22.5mV which is the 450mV divided by 20 -the gain of the EA-. This offset can be reduced by either increasing the number of ADC bits which will need more area and power consumption or increasing the gain of the error amplifier.

3.1.2. PLL Layout

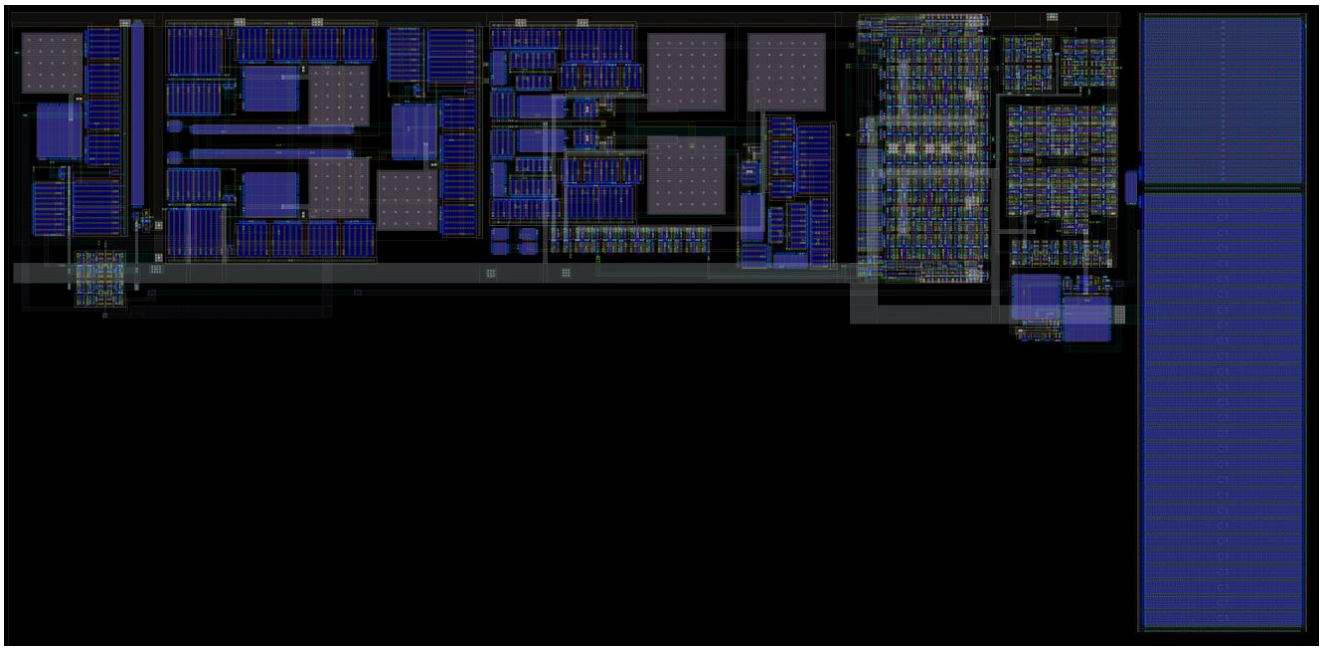

Figure 48: PLL Layout

3.1.3. PLL Performance Analysis

The PLL can be tested with a feedback loop to evaluate its performance separately and ensures its function with the whole system. The pre-layout simulation of the PLL is shown in Figure 49 below. The PLL is designed to achieve the best performance with the entire system. As shown in Figure 49, the offset is in the range of 20mV. This offset can be highly reduced by increasing the gain of the error amplifier to optimize the performance of the PLL independently of the system, but it will be shown that this offset is needed for a better result of the entire system. Settling time can be reduced by lowering the loop filter capacitor value. Again, the performance is optimized to match the requirements of the entire system. The simulations show a pure output with very small ripples (less than 1uV). The post layout simulations of the PLL is shown in Figure 50. The settling time is increased duo to the existence of some parasitics due to the metal wiring.

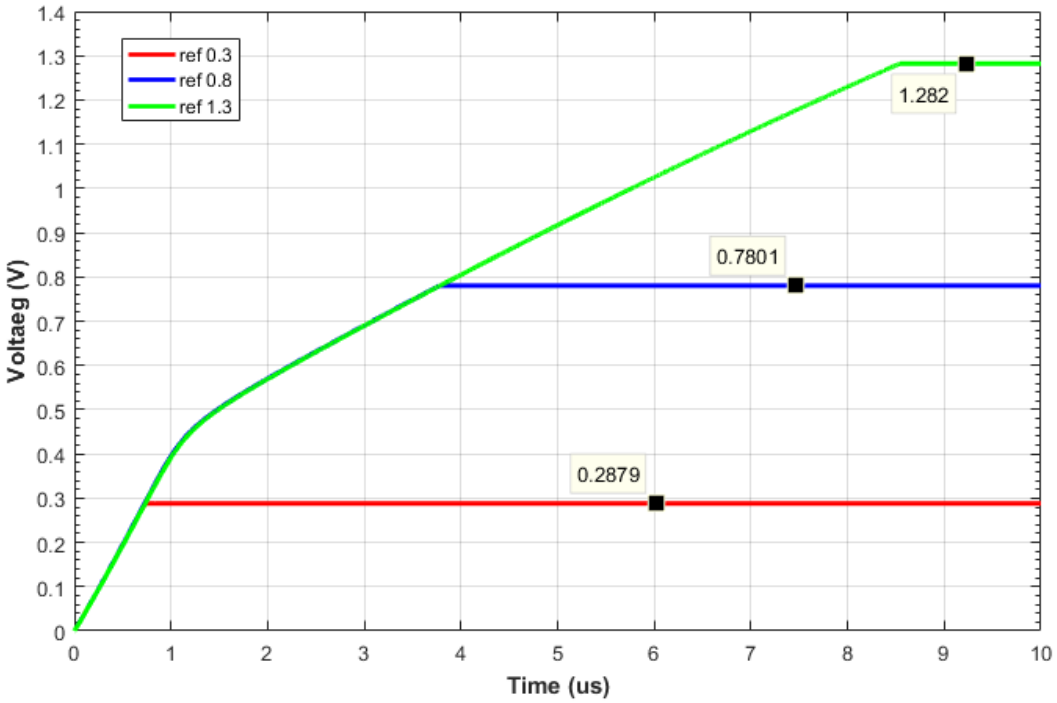

Figure 49: PLL schematic V_{REF} sweep

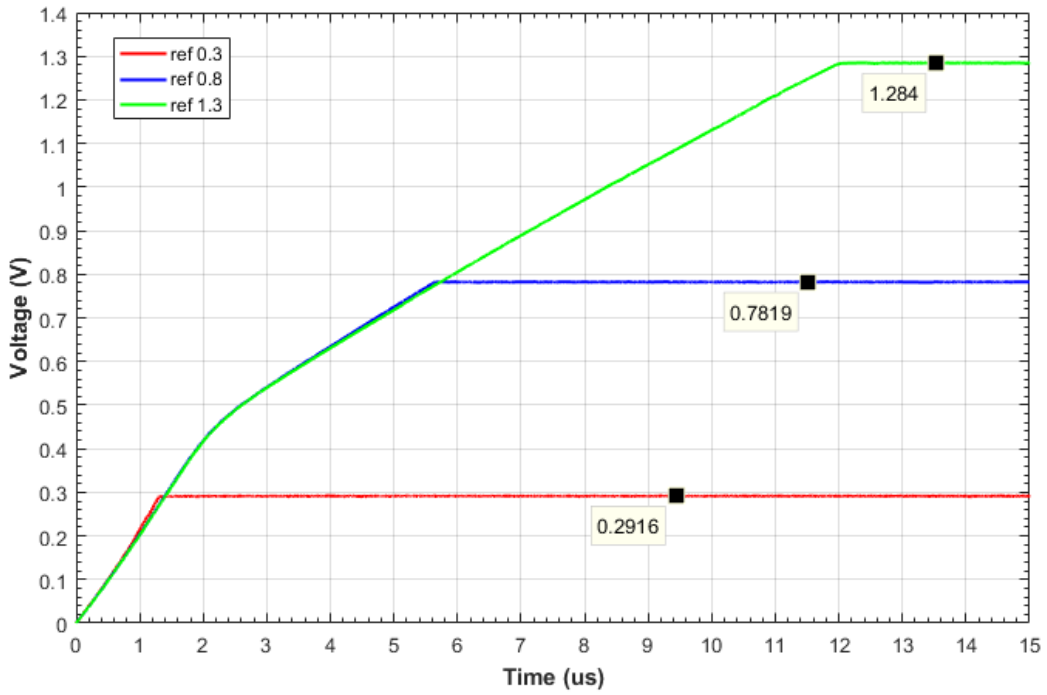

Figure 50: PLL post-layout V_{REF} sweep

3.2. System

3.2.1. System Working Principle

After testing the PLL and makes sure from its performance, the system is integrated as one part. The PLL output is connected to the PWM to set a proper duty cycle. In order to avoid short circuit path a dead time control is implemented to make sure that the PMOS and NMOS are never open at the same time. Gate drivers are important to drive the large buck transistors. The inductor capacitor and the load resistance are connected as shown in the schematic in Figure 51.

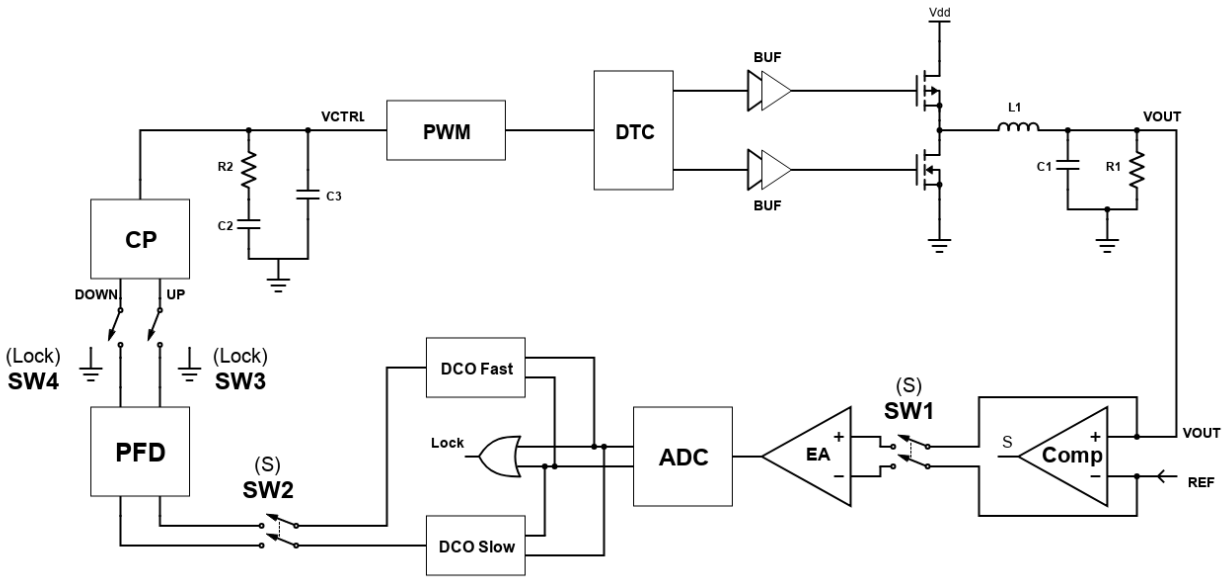

Figure 51: System block diagram

3.2.2. *System Layout*

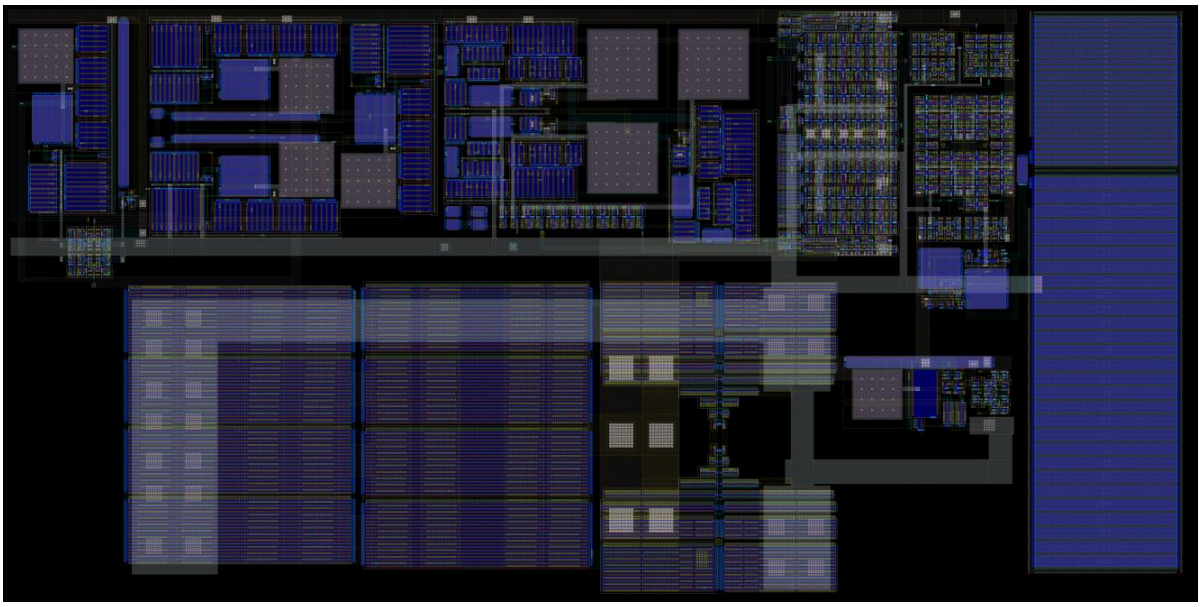

Figure 52: System Layout

3.2.3. *System Performance Analysis*

This section is dedicated to analyzing the entire system performance including settling time, ripples, efficiency and sudden changes. Figure 53 shows the schematic level of the systems under different reference voltages. The offsets are 1mV, 4.3mV and 17mV for references 1.3V, 0.8V and 0.3V, respectively. The maximum settling time is less than 4us. As shown in Figure 53 the settling time is around 500ns, 1.8us and 3.9us for references 0.3V, 0.8V and 1.3V respectively.

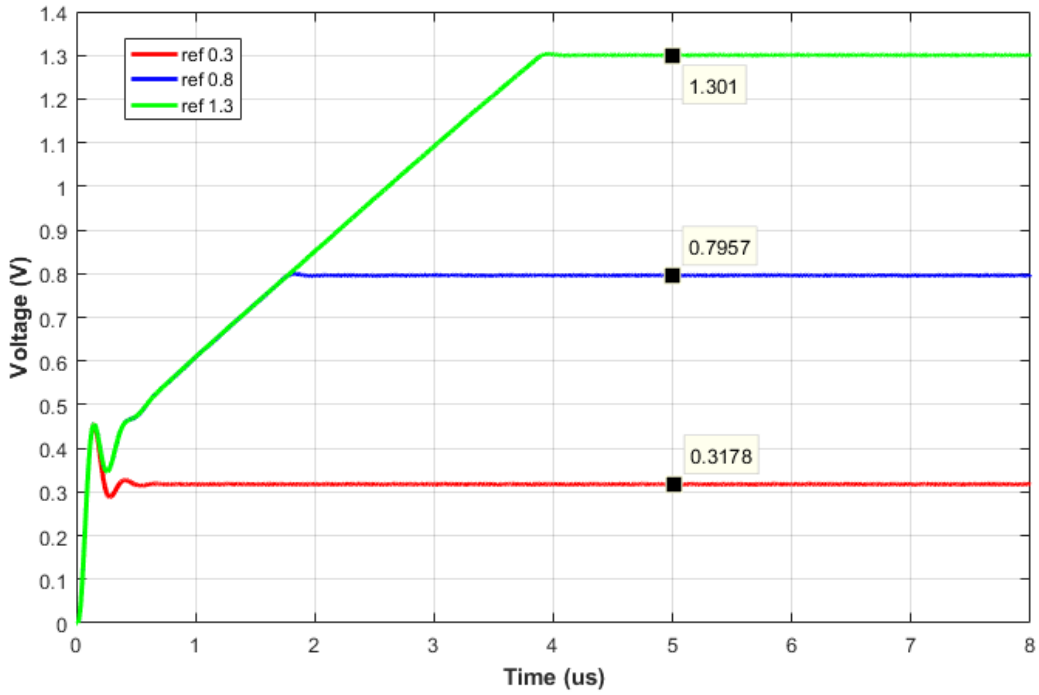

Figure 53: System schematic simulation V_{REF} sweep

The ripples are shown in Figure 54. For reference 0.3V the ripples are around 0.55mV and in Figure 55, the are 0.4mV for reference 1.3V.

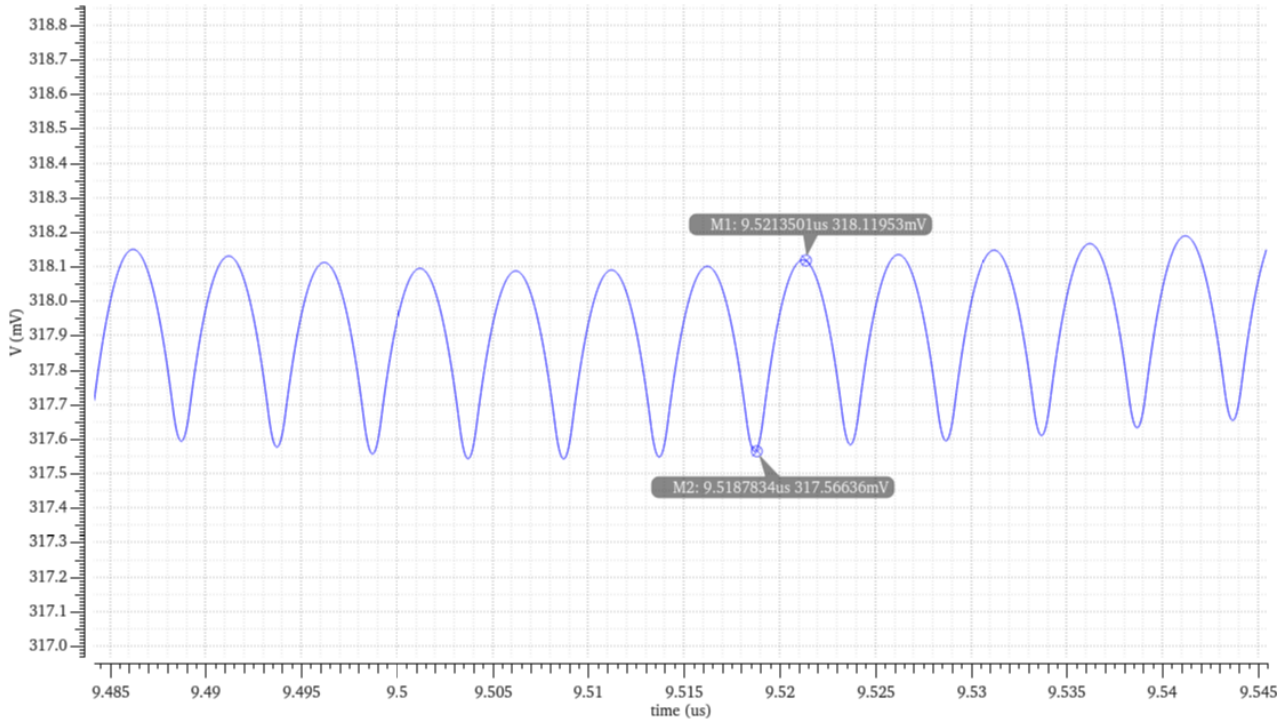

Figure 54: Ripples for system schematic simulation V_{REF} 0.3 V

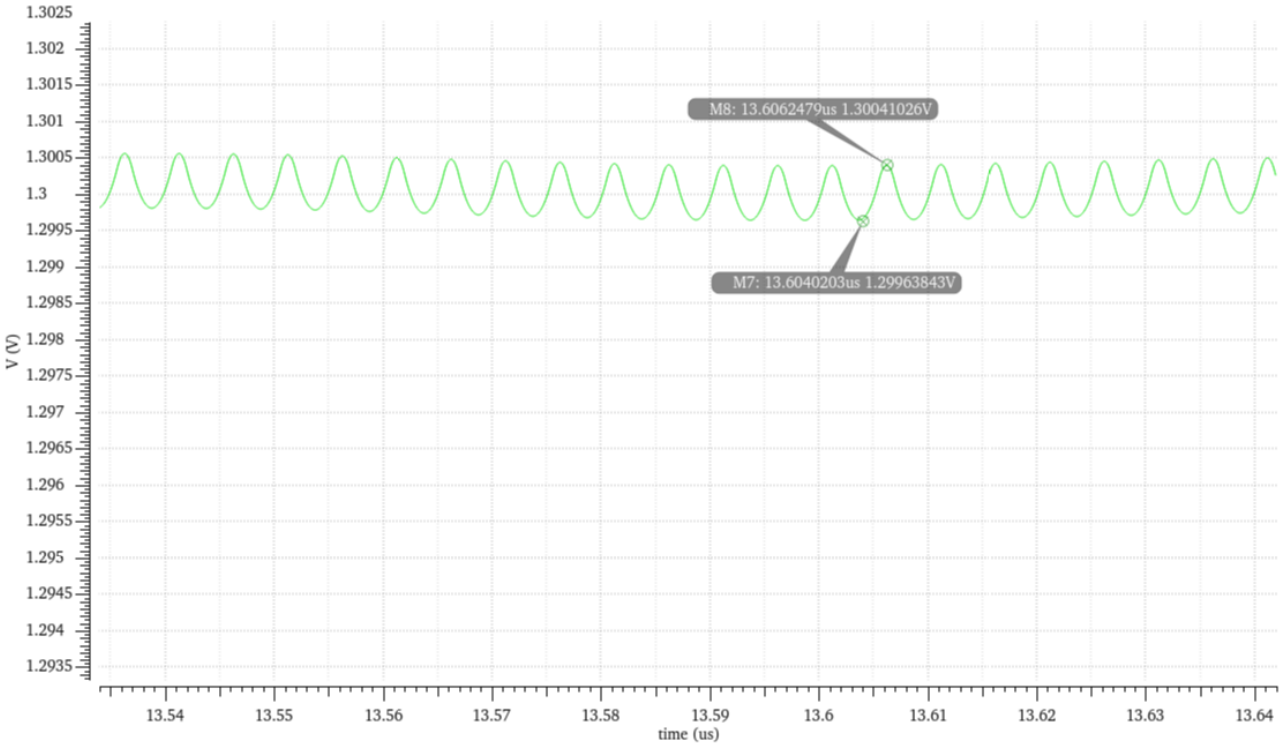

Figure 55: Ripples for system schematic simulation V_{REF} 1.3 V

The system is also tested under reference change. Figure 56 shows the change of the reference from 0.3V to 0.8V and the system follows the change in the reference as expected.

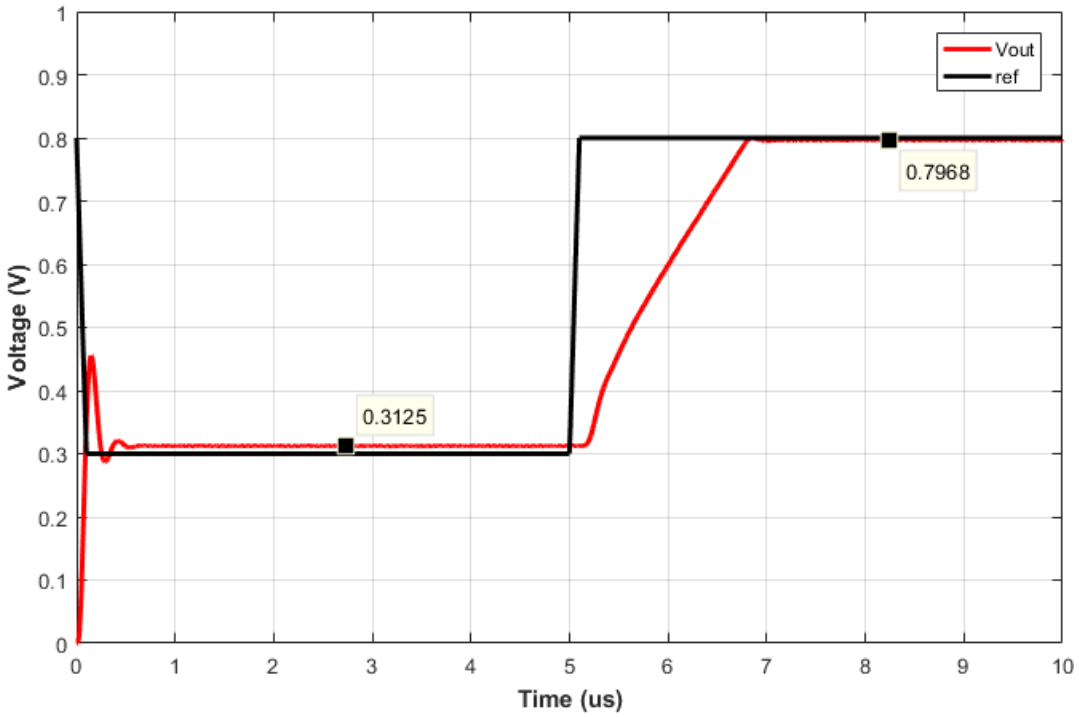

Figure 56: Reference change from 0.3 V to 0.8 V

The efficiency Curve of the system in shown in Figure 57. The peak efficiency is around 82.75%.

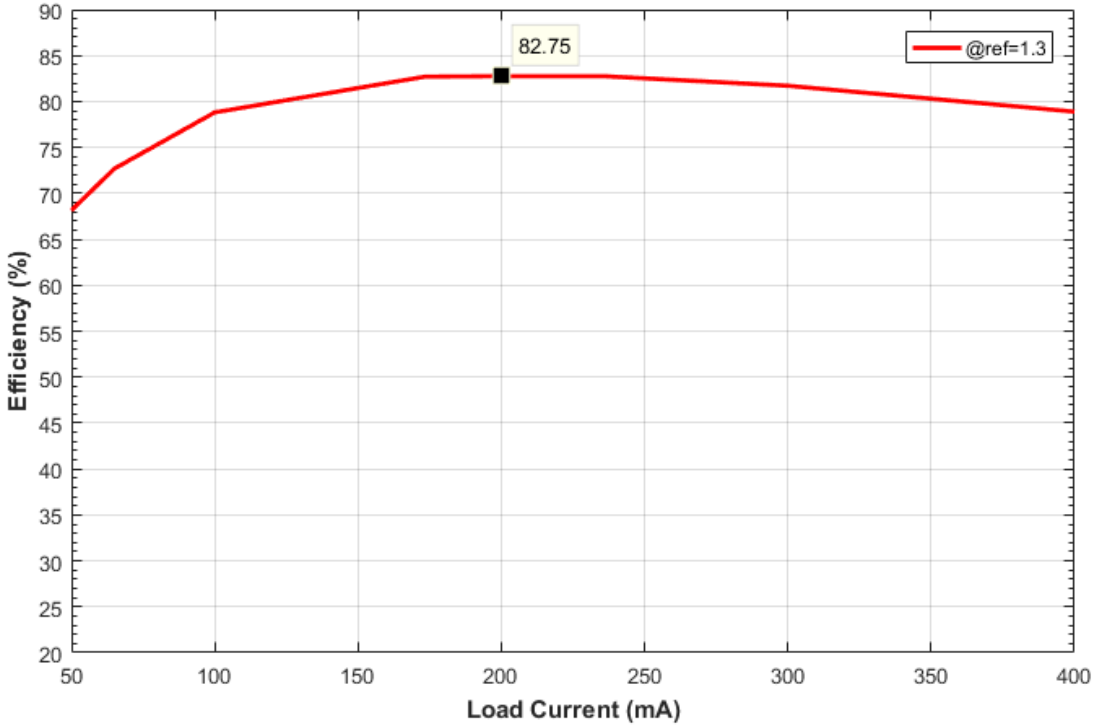

Figure 57: Efficiency curve for system schematic simulation at V_{REF} 1.3 V

The post-layout simulation for the system at V_{REF} 0.6, and 0.8 is shown in Figure 58, and is shown in Figure 59 for V_{REF} 1.3

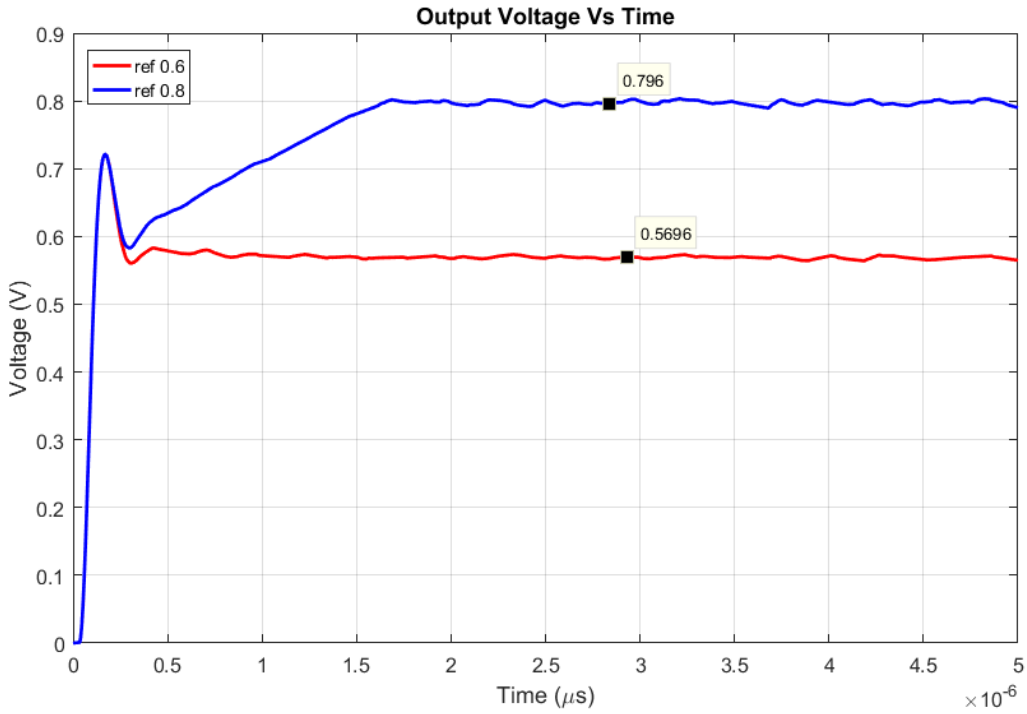

Figure 58: system post-layout simulation at V_{REF} 0.6, 0.8 V

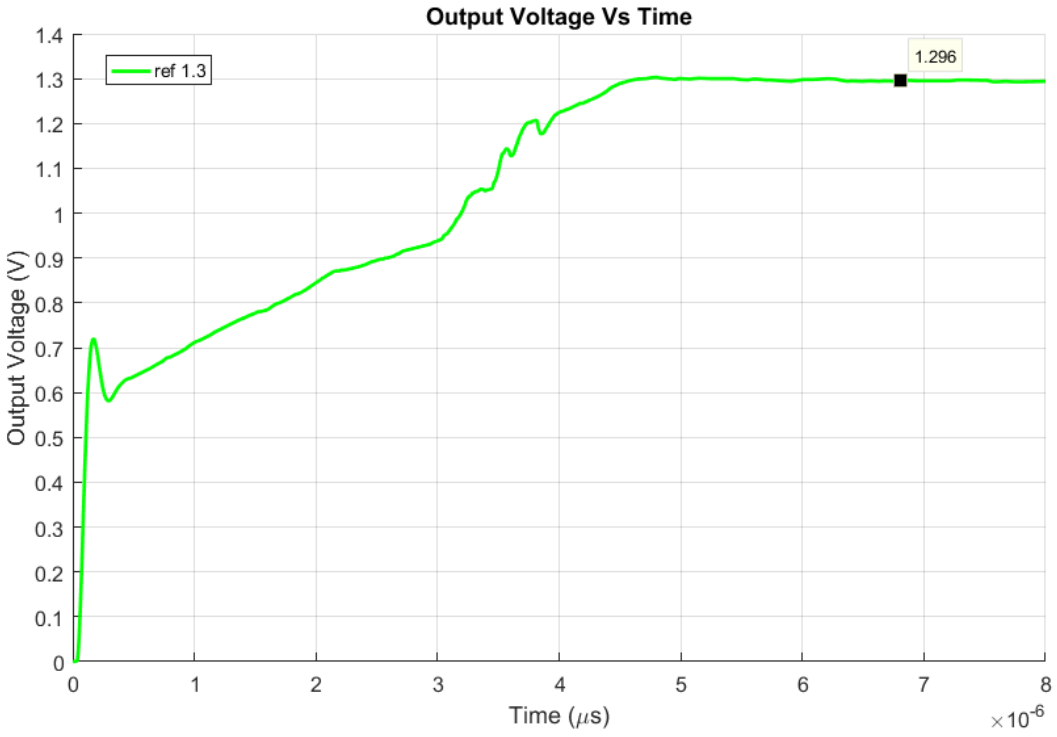

Figure 59: system post-layout simulation at V_{REF} 1.3 V

3.2.4. System Specifications and Comparison

The specifications of the system are summarized and compared with other designs in literature, in Tables II, III, and IV.

Table II : System specs and comparison with [41, 49, 54]

Specs	[41]	[49]	[54]	This work
Year	2015	2018	2015	2020
Technology	65nm	180nm	180nm	180nm
Switching Freq	30MHz	30MHz	11-25MHz	200MHz
Inductor	90nH × 4	90nH	220nH	30nH
Capacitor	0.47uF	2.2uF	4.7uF	50nF
Input	1.8V	3.3V	1.8V	1.8V
Output	0.6-1.5V	0.4-2.2V	0.6-1.5V	0.3-1.3V
Ripples		N/A	3.5mV	1mV
Max Load Current	0.8A	0.8A	0.6A	0.4A
Peak Efficiency	87%	90.2%	94%	82.75%
Efficiency @ Max Pwr	N/A	N/A	N/A	79%
Area	$0.32mm^2$ active area	$0.864mm^2$ (including testing pads)	$0.24mm^2$ (active area)	$0.034mm^2$
Inductor on Chip	No	No	No	No
Power Density	$2.5\ W/mm^2$	N/A		
Settling Time	0.6u	3u	3.5us	500ns

Table III : System specs and comparison with [57-59]

Specs	[57]	[58]	[59]		This work
Year	2008	2011	2014		2020
Technology	130nm	130nm	130nm		180nm
Switching Freq	170MHz	200-300MHz	30MHz	10MHz	200MHz
Inductor	2nH × 2 (spiral)	2nH (stacked)	330nH		30nH
Capacitor	N/A	5nF	1uF	3.3uF	50nF
Input	1.2V	1.2V	3.3V		1.8V
Output	0.204-0.96 V	0.3-0.88 V	0.45-2.4V		0.3-1.3V
Ripples	48mV	16mV	N/A		1mV
Max Load Current	350mA	350mA	1.5A	N/A	0.4A
Peak Efficiency	77.9%	77%	86.6%	91.8%	82.75%
Efficiency @ Max Pwr	76%	68%	N/A		79%
Area	$1.5mm^2$	$1.59mm^2$	N/A		$0.034mm^2$
Inductor on Chip	Yes	Yes	No		No
Power Density	$210mW/mm^2$	$167mW/mm^2$	N/A		
Settling Time	N/A	N/A	5u	4.44us	500ns

Table IV : System specs and comparison with [60, 61]

Specs	[60]	[61]	This work
Year	2010	2019	2020
Technology	180nm	65nm	180nm
Switching Freq	0.5MHz	10MHz	200MHz
Inductor	1880nH	0.22uH	30nH
Capacitor	22uF	4.7uF	50nF
Input	3.3V	1.8V	1.8V
Output	1.8V	0.15-1.69V	0.3-1.3V
Ripples	18mV	10mV	1mV
Max Load Current	1A	0.6A	0.4A
Peak Efficiency	94%	94.9%	82.75%
Efficiency @ Max Pwr	N/A	N/A	79%
Area	2.25mm^2 (active)	0.19mm^2 (active)	0.034mm^2
Inductor on Chip	No	No	No
Power Density	N/A	N/A	
Settling Time	100us	3u	500ns

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