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Analog/RF front-end design of Bluetooth low-energy transceiver in 65nm CMOS technology

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Abstract

ANALOG/RF FRONT-END DESIGN OF BLUETOOTH LOW-ENERGY TRANSCEIVER IN 65NM CMOS TECHNOLOGY

With the increasing need for the Internet of things (IoT) in daily lives, Bluetooth (BT) technology has become a popular solution for portable devices. It is used in mobile phones, medical sensors, and many other consumer electronics. The main reason that BT was the best candidate for IoT compared to other wireless devices was the introduction of the energy saving feature, Bluetooth Low-Energy (BLE). The key elements that allow BLE to have the lowest cost possible are the industrial, scientific, and medical (ISM) band, IP license, and low power. Low power is necessary for mobile devices because consumers are expected to use the devices for extended periods without charging or changing the power source.

In cooperation with Si-Vision LLC, a state-of-art design of the integrated CMOS RF transceiver is carried out. It is following the specifications defined by the Bluetooth core V5.1 standard.

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Chapter 1: Introduction to Bluetooth Low Energy (BLE)

1.1 Introduction

Bluetooth is a wireless technology standard. Bluetooth was developed as a way to exchange data over a short range without the need for wires. That's why Bluetooth is used for wireless headsets, hands-free calling through your car, and wireless file transfers. When considering the difference between Bluetooth and Bluetooth Low Energy (it's newer sibling), it's important to talk about power consumption. Bluetooth was originally designed for continuous, streaming data applications. That means that you can exchange a lot of data at a close range. That's why Bluetooth is such a good fit for consumer products. People like to receive data and talk at the same time, and exchange videos from one device from another. Here are some machine-to-machine (M2M) and Internet of Things (IoT) uses for Bluetooth wireless handsets, file transfer between devices, wireless keyboards and printers, and wireless speakers.

1.2 Bluetooth Vs. BLE

Bluetooth Low Energy hit the market in 2011 as Bluetooth 4.0. When talking about Bluetooth Low Energy vs. Bluetooth, the key difference is in Bluetooth 4.0's low power consumption. Although that may sound like something negative, it's actually extremely positive when talking about M2M communication. With Bluetooth LE's power consumption, applications can run on a small battery for four to five years. Although this isn't ideal for

talking on the phone, it is vital for applications that only need to exchange small amounts of data periodically. Just like Bluetooth, BLE operates in the 2.4 GHz ISM band. Unlike classic Bluetooth, however, BLE remains in sleep mode constantly except for when a connection is initiated. The actual connection times are only a few mS, unlike Bluetooth which would take 100mS. The reason the connections are so short, is that the data rates are so high at 1 Mb/s.

In summary, Bluetooth and Bluetooth Low Energy are used for very different purposes. Bluetooth can handle a lot of data, but consumes battery life quickly and costs a lot more. BLE is used for applications that do not need to exchange large amounts of data, and can therefore run on battery power for years at a cheaper cost. It all depends on what you're trying to accomplish.

1.3 Key Factor of BLE

The key elements that allow BLE to have the lowest cost possible are the industrial, science, and medical (ISM) band, IP license, and low power. One major advantage of using the ISM band is that a permit or fee is not required, although it must follow a specific power requirement for data transmission. The maximum power fed into the antenna must be lower than 30 dBm (equivalent to 1W). The BT special interest group (SIG) provides a reasonable price for an IP license, which is relatively lower than other competitors. The cost of the license can be reduced, because an increasing number of customers and users are supporting BLE devices.

Low power is necessary for mobile devices because consumers are expected to use the devices for extended periods without charging or changing the power source. Making a sustainable device requires more energy storage, low power consumption, or both. However, the energy storage in the device demands additional space. The large device size also meant that manufacturing costs were higher, so increasing the energy storage was an inefficient solution for long-period usage. Therefore, lowering the power of the device not only reduces manufacturing cost but also improves battery usage. Since more power is needed for the device, more space is preserved for the power source or battery.

Even though low power is suitable for the device, sometimes the device needs to operate at high speeds for some specific applications. Therefore, BT version 4.0 was introduced to combine the needs of different usage modes, which led to a solution that allowed for BT to have three operation modes.

1.4 Operation Modes

After BT had evolved to version 4.0, it had three different modes, which are classic BT, BLE, and dual-mode. The Bluetooth Smart Ready mark represents the dual mode, the Bluetooth mark represents the classic BT mode, and the Bluetooth Smart mark represents BLE mode.

Classic BT was initially designed to connect two devices at a short distance for transferring data, such as linking mobile phones to computers. Furthermore, the application was improved to not only transfer data but also to stream audio and video. This improvement provided a robust wireless

connection between devices ranging from smartphone and car audio devices to industrial controllers and medical sensors. However, BLE became a more power efficient and cost-effective solution for many of these applications.

When comparing BLE to classic BT, the main difference is power dissipation. The BLE devices manage to operate for extended periods of time. This advantage is beneficial in machine to machine (M2M) communication because it can last for years without changing the power source once the BLE device is placed in the machine. However, to achieve this goal, the data transmission rate must be sacrificed in exchange for low power dissipation.

BLE devices slow down the data transfer rate, though it effectively decreases the power consumption. Unlike classic BT devices, BLE devices do not need to be at the highest speed possible. For example, while one uses the smartphone to switch on the air conditioner and adjust the room temperature, these applications do not have significant data to transfer. It simply needs to send the package containing "power on" and "increase/decrease temperature" from the transmitter to the receiver. On the other hand, while one uses a smartphone to stream television through a BT connection, it is not a simple package containing a single command; instead, it can be a high definition (HD) video or high quality (HQ) music file that must be smoothly played on television. Otherwise, the user will never replace the wired connection with wireless.

1.5 Summary

Chapter 1 discussed the specifications of BLE compared to BT. The structure is slightly different from the structure of BT because of the low

energy requirements. The ISM band, IP license, and low power are key elements that allow BLE to have the lowest cost possible. The design of BLE was introduced to have an overview of the technology that is utilized in this paper.

Chapter 2: Receiver architectures for BLE

2.1 Direct Conversion Receiver

A study for different receiver architecture to achieve the highest level of integration, lowest power consumption, and best performance. Of course, all these requirements are not met in a single architecture, and therefore, trade-offs were closely studied to find the best architecture that meets the standard specifications with enough margins at lower cost. Two very common architectures are used for Bluetooth receivers, direct-conversion and low-IF.

Although the direct-conversion architecture lends itself to higher integration levels and lower power consumption, it is plagued by quadrature demodulation phase errors, quadrature gain phase mismatch, DC offsets, 1/f noise, and LO feedthrough [1]. Low-IF architecture [2] can be used to avoid the DC offset and 1/f complications associated with direct-conversion. However, Low-IF architecture suffers from the image problem due to the non-zero IF frequency.

The choice of the most suitable receiver architecture depends on many parameters in the wireless standard (e.g. channel bandwidth, preamble time, blocking specifications, sensitivity, modulation format, etc..). In the following two sections, both possible architectures of the Bluetooth receiver will be discussed in some detail.

2.2 Direct-Conversion Receiver Architecture

In direct-conversion receiver (DCR) architecture, the signal is down-converted directly from RF to baseband. A low-pass filter is then employed to suppress nearby interferers as shown in the simplified diagram in Fig.2.1. The use of quadrature I and Q channels is necessary in the Bluetooth case because the signal is frequency-modulated, and therefore the two sidebands of the RF spectrum will carry different information. The spectrum of the complex output signal I+jQ will be a replica of the signal spectrum at RF, but down-converted around dc. Despite the simplicity of the DCR architecture, it suffers from some serious design issues that do not exist or are not as serious in low-IF receivers.

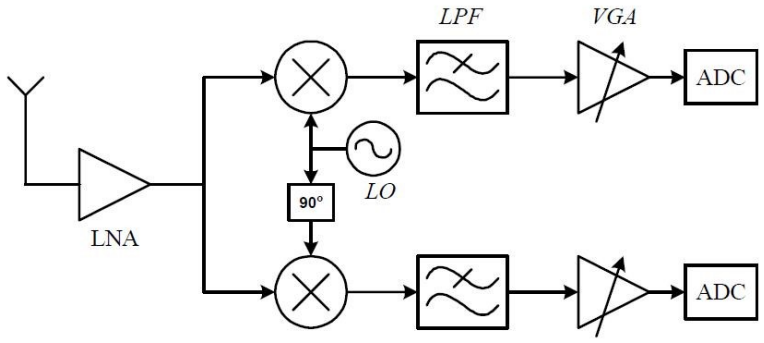

Figure 2.1: Direct conversion receiver architecture

2.3 DC Offsets

There are different sources of DC offsets in an integrated receiver;

1. Components mismatch.
2. LO self mixing.
3. interferers self-mixing.

These sources are explained as follows:

1. Typical MOS transistor VT mismatches are in the order of few millivolts. This might be quite higher than the desired signal level at the mixer output.

2. Due to capacitive and substrate coupling, isolation between the LO port and the inputs of the mixer and the LNA is finite. This effect is called LO leakage. The leakage signal appearing at the input of the LNA and the mixer is now mixed with the LO signal thus producing a dc component at the mixer output. If the LO signal level is 0dBm, and isolation between LO and LNA input is 60dB, then the LO signal at the LNA input is about -60dBm, quite substantial compared to the minimum signal (sensitivity) level at the receiver input.

3. This effect is similar to LO self mixing. When a large interferer leaks from the LNA or mixer input to the mixer LO port, it mixes with itself and generates a low frequency beat at the mixer output corresponding to amplitude variations in the interferer. This resulting offset is even harder to reject since it is varying with time.

This means that if the desired signal level at the end of the receiver chain is at the full swing of the final stage, the dc offset generated by mismatches will saturate the receiver stages. Therefore, this dc offset has to be rejected before it gets amplified by the receiver stages. A possible approach to removing the offset is to employ ac coupling, i.e. high-pass filtering, in the down-converted signal path. However, since the spectrum of the Bluetooth GFSK signal exhibits a peak at dc, such signal may be corrupted if filtered with high cutoff frequency.

2.4 Flicker Noise

In modern technologies and for the minimum gate-length transistors required by RF circuits, the 1/f noise (also called flicker noise) component might exceed the white noise up to several megahertz. On the one hand, flicker noise is not a limiting effect for linear RF circuits, as in the low noise amplifier (LNA) since the operating frequency is much higher than the corner frequency. On the other hand, since minimum length transistors are used in the switching transistors and due to the nonlinear operation of the mixer and the finite slope of the LO signal, flicker noise of the switches appears at the baseband output of the mixer. Flicker noise of the transistors used in the baseband circuits also falls in the signal band and degrades the system noise figure (NF). NF degradation depends on the flicker noise corner frequency and the channel bandwidth. In the case of Bluetooth, the -3dB bandwidth of the signal is about 500kHz, while the 1/f corner frequency is about 1MHz or even larger for smaller transistor lengths. This NF degradation might be so significant that it disqualifies DCR architecture as the optimum choice for Bluetooth. The effect of flicker noise can be reduced by a combination of techniques. As the stages following the mixer operate at relatively low frequencies, they can incorporate longer devices to minimize the magnitude of the flicker noise. Moreover, periodic offset cancellation also suppresses low-frequency noise components through correlated double sampling.

2.5 Even Order Distortion

Unlike other architectures, even-order distortion in the LNA and mixer input transistor becomes problematic in DCR architecture. Suppose two strong interferer ($A_1\cos(\omega_1 t)+A_2\cos(\omega_2 t)$) close to the desired channel ex-

perience a second order nonlinearity in the LNA represented as $y(t) = \alpha_1 x(t) + \alpha_2 x(t)^2$,then y(t) contains a low frequency term $\alpha_1 A_1 A_2 \cos(\omega_1 - \omega_2)$t.

Upon multiplication by cos(t) in an ideal mixer, such a term is translated to high frequencies and hence becomes unimportant. In reality, however, mixers exhibit a finite direct feedthrough from the RF input to the IF output due to mismatches between transistors and deviation of LO dutycycle from 50%. The natural solution to suppress even-order distortion is to use differential LNA and mixer. However, two issues arise here. First the antenna and the duplexer filter are usually single-ended. This necessitates the use of a balun (transformer) to do the single-ended to differential conversion. Baluns typically exhibit several decibels of loss at high frequencies. This loss directly raises the overall system noise figure. Second, differential LNA requires more power consumption than the single ended counterpart to achieve the same noise figure.

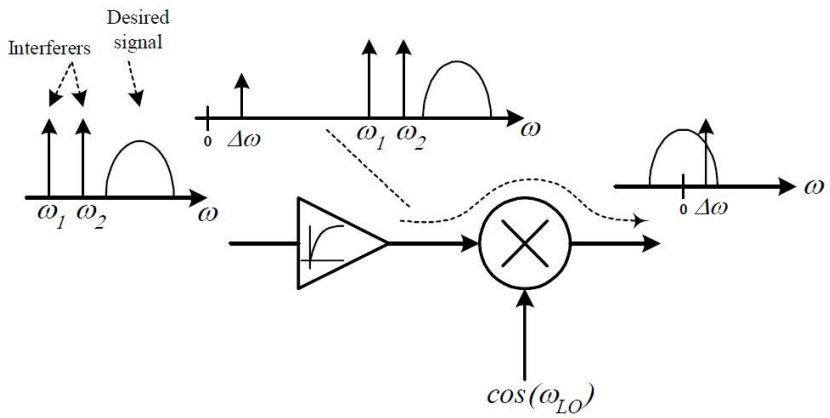

Figure 2.2: Effect of even order distortion

2.6 I/Q Mismatch

Phase and magnitude mismatches between I and Q branches corrupt the Down-converted signal. However, in the case of Bluetooth, since the modulation format in binary GFSK, I/Q mismatch is not a serious problem. Therefore, I/Q mismatch is much.

2.7 Low-IF Receiver Architecture

IF receivers have been in use for a long time, and their principle of operation is very well known. In an IF receiver, the wanted signal is down-converted to from its carrier to the IF by multiplying it with a single sinusoidal signal as shown in Fig.2.3. The main disadvantage here is that apart from the wanted signal, an unwanted signal at a frequency called the image frequency (which is 2 f IF away from the wanted frequency) is down converted to the same IF frequency. To avoid corrupting the wanted signal, the image signal must be suppressed before down-conversion by means of a band-pass RF filter. The Q of such filter is proportional to $\frac{F_{RF}}{F_{IF}}$. High Q external SAW or ceramic filters (typically 50 or more) are used for this purpose. Such filters are bulky and require impedance matching at input and output, which usually raises the power consumption that is needed in order to drive this low impedance. Furthermore, the IF frequency cannot be made arbitrarily small due to the limited Q of the external filter, and hence, raising the power consumption of the circuits operating at the IF frequency. The image frequency problem can be mathematically explained as follows. When RF signal is multiplied by a single sinusoidal signal $\cos(\omega_{LO})$, it is equivalently multiplied by two exponentials $e^{-i\omega_{LO}}$ and $e^{i\omega_{LO}}$ Considering the signal diagram in Fig. 2.4, the spectrum of the down-converted signal is

constructed by shifting the RF spectrum to the left and to the right by ω_{LO} add the two shifted replicas. The result is two overlapping spectra, of the signal and the image, at the IF frequency.

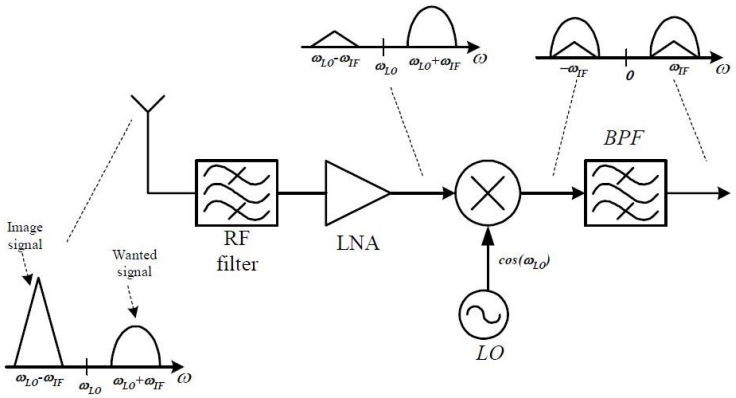

Figure 2.3: IF receiver architecture

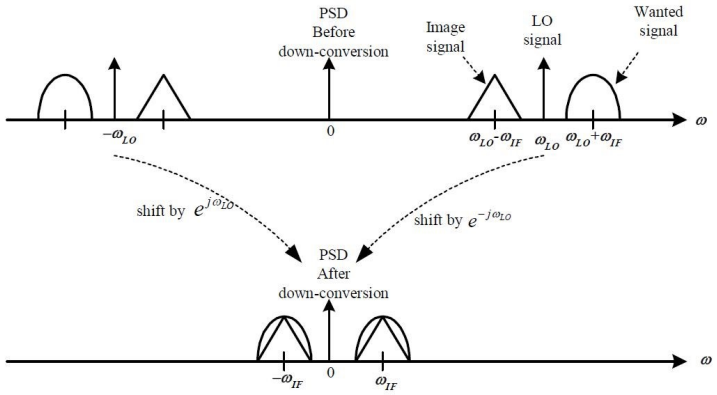

Figure 2.4: Down conversion with a single sinusoidal signal

An obvious solution to avoid this problem is to multiply the RF signal by only exponentials, say $e^{-i\omega_{LO}}$ which means that the down-converted signal is simply a single shifted replica of the RF signal and therefore, no overlapping of signals spectra. The only problem now is that the signal $e^{-i\omega_{LO}}$ is complex signal with real part $\cos(\omega_{LO})$ imaginary part $\sin(\omega_{LO})$.To

implement this complex multiplication using real components, two signal branches I and Q must be constructed. In the I (in-phase or real) branch, the RF signal is multiplied by $\cos(\omega_{LO})$ while in the Q branch (quadrature-phase or imaginary), the RF signal is multiplied by $\sin(\omega_{LO})$ fig. 2.5 shows the signal diagram of the complex down-conversion operation. It is important to note that in each branch, the down-converted signal contains both the wanted and the image signals at the same IF frequency. However, the complex signal $I_0 + jQ_0$ has the wanted signal at ω_{IF} and the image signal at $-\omega_{IF}$. the image signal can then be rejected by means of a complex filter, which will be described in detail in the following section. The same filter is also used for channel selectivity. Therefore, the Q of such filter is proportional to $\frac{-\omega_{IF}}{BW}$ (BW is the channel bandwidth) which is small for low IF frequencies. This is the basic idea behind low-IF receiver architecture.

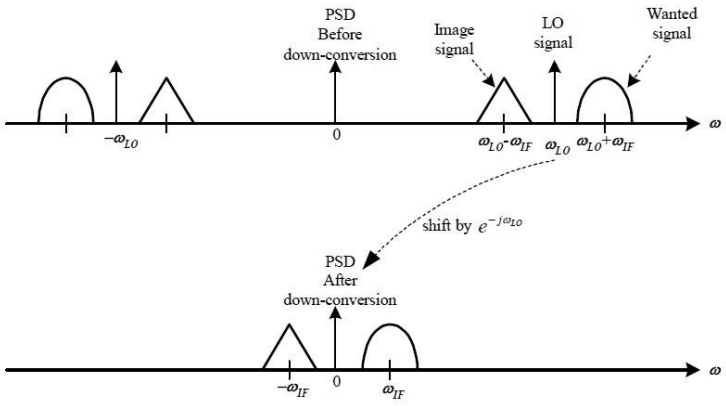

Figure 2.5: Down conversion with a single exponential

Fig. 2.6 shows the basic low-IF receiver architecture. Although low-IF receiver avoids the problems that exist in DCR and high-IF architectures, it has some design issues. Namely, its image rejection capability is limited by matching between I and Q branches and between the quadrature LO outputs. The effect of these mismatches is studied in the following section.

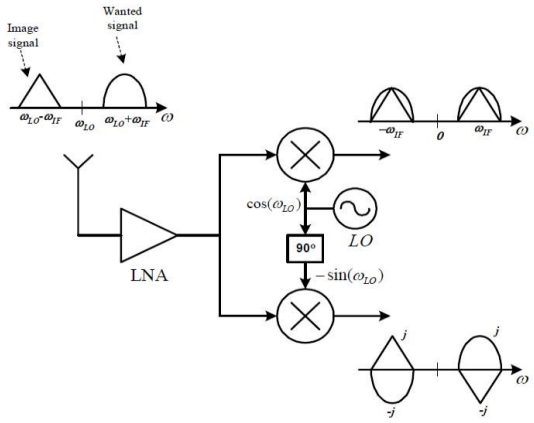

Figure 2.6: Basic low IF receiver architecture

2.8 BLE Receiver Architecture

In a baseband Bluetooth signal, 99% of the signal power is contained within the DC to 430kHz bandwidth. Therefore, if direct-conversion architecture is used, the flicker noise and DC offset might significantly degrade the signal-to-noise ratio (SNR). Hence, a low-IF architecture seems to be a suitable architecture in Bluetooth, especially when considering the relaxed image rejection requirement in the Bluetooth standard [3]. To relax the image rejection requirement and reduce the folded-back interference level, a very low-IF is preferable, i.e. half of the channel bandwidth. However, such a very low- IF requires a sharp cut off from the channel selection filter to reject the DC offset and flicker noise. On the other hand, a higher IF improves the demodulator performance, but the required selectivity of the channel selection filter will increase, and power consumption will be higher. As a good compromise, an IF of equal the channel bandwidth is chosen, i.e. 2 MHz for the two-mega mode and 1MHz for the one-mega mode. For a low-IF Bluetooth receiver, the image signal is an in-band Bluetooth modulated adjacent channel interference, which becomes co-channel interference after

frequency down-conversion.

Nowadays, current-mode receiver are preferred for the following reasons:

1. Low power consumption at higher frequencies.
2. Less affected by voltage fluctuations as the voltage swing is low.
3. High speed.
4. Voltage suffers from attenuation for long distance but, Current do not.
5. Current-mode RF receivers have simpler architecture due to lower supply voltage, and better linearity..

For voltage mode circuits, impedance of internal nodes is usually large so, the signal information could be carried with the time varying voltage signal. Therefore, large voltage swing is required to keep signal information that's why voltage mode circuit is not preferred for low voltage supply. In contrast with current-mode circuit, low-impedance node and signal information is carried by the time varying current signal so, voltage at each node could be small.

Chapter 3: Power Amplifier

3.1 Overview

Power Amplifiers (PAs) are most power-hungry building block of RF transceivers and pose difficult design challenges. In terms of the transmitter performance, PA design is a big challenge facing the RF transceivers designers as it has to deliver power for a certain load with maximum efficiency. The fundamental issue in PA design is the trade off between output power and the voltage swing experienced by the the output transistor. The design of PA is concerned by many parameters that determine the choice of suitable topology.

3.2 Design Parameters

There are many factors and parameters that have to be considered with the design of PA, such as effect of high currents, efficiency, linearity, and single ended and differential PAs. These factors are introduced here to understand what compromises are needed to achieve the design specs.

3.2.1 Effect of High Currents

The enormous currents flowing through the output device and matching network are difficulties in the design of PAs and the package. If output device is chosen wide to carry a large current then, it's input capacitance is large and this makes design of preceding stages difficult.We may deal with this issue by interposing number of stages between mixer and output stage. This may limit the TX ouput compression point and consume power thus,

lowering efficiency. We may deal with this issue by interposing number of tapered stages.

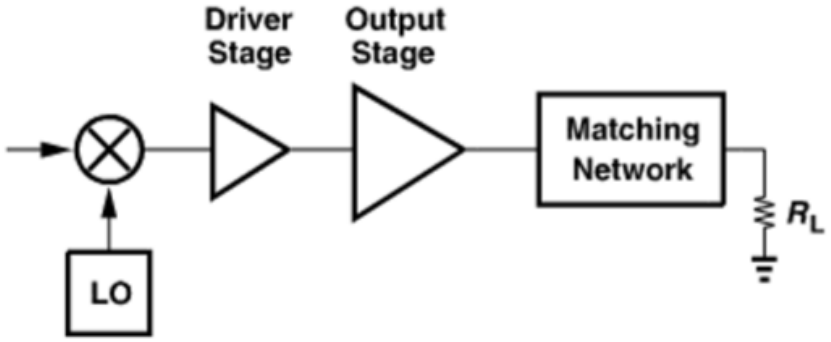

Figure 3.1: Tapering in TX chain

3.2.2 Efficiency

Since PAs are the most power-hungry block in RF transceivers their efficiency is critical. The efficiency of PAs is defined by two metrics. The drain efficiency is defined as :

$$\eta = \frac{P_l}{P_{supp}} \tag{3.1}$$

Where Pl is the average power delivered to the load and Psupp is average power drawn from supply. In some cases the output stage may have a relatively low power gain e.g., 3dB requiring high input power. The quantity embodying this effect is the "power-added efficiency" (PAE), defined as :

$$\eta = \frac{(P_l - P_{in})}{P_{supp}} \tag{3.2}$$

3.2.3 Linearity

The linearity of PAs becomes critical for some modulation schemes. Nonlinearity leads to two effects: (1) High adjacent channel power as result of spectral regrowth and (2) Amplitude compression. The PA characterization begins with two generic tests of nonlinearity based on unmodulated tones, intermodulation and compression, by applying two sufficiently large tones, the amplitude of the tones is chosen such that each main component at the output is 6dB below the full power level thus, producing the max desired output voltage swing when added in phase. For compression, a single tone is applied and its amplitude gradually increases to determine the output 1-dB compression point.

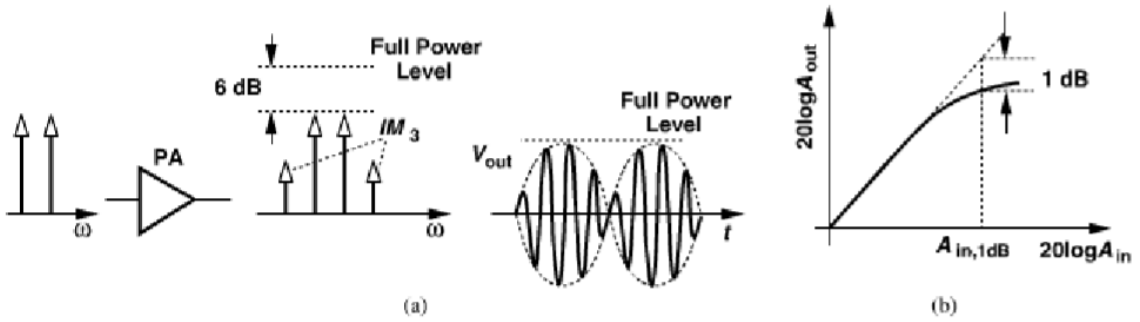

Figure 3.2: Linearity tests

3.2.4 Single Ended and Differential PAs

Most stand-alone PAs have been designed as a cascade of single-ended stages as single ended RF circuits are simpler to test. Single-ended PAs, however, suffer from two drawbacks. First, they waste half of transmitter gain as they sense only one output of the upconverter. This problem can be solved by inserting a balun between the upconverter and PA but, it may introduce some losses.

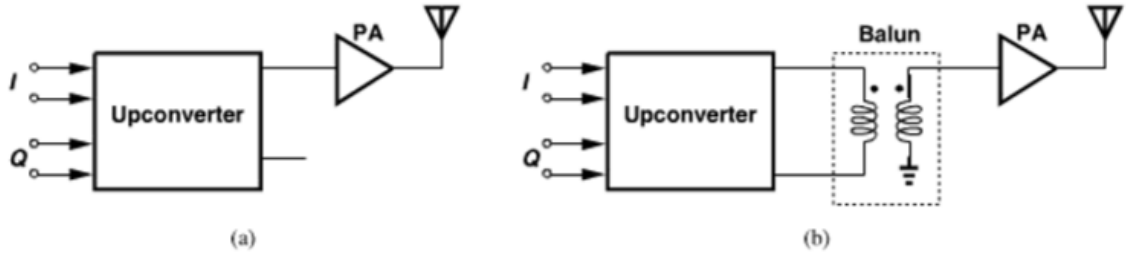

Figure 3.3: (a) single-ended or (b) balun connection

The second drawback stems from large transient current they pull from supply to ground. The supply wire inductance LB1 alters the output impedence of the network if it is comparable with Ld. LB1 allows some of output signal to travel back to preceding stages through the vdd line causing ripples in frequency Similarly, ground wire inductance LB2 degenerates the output and introduces feedback.

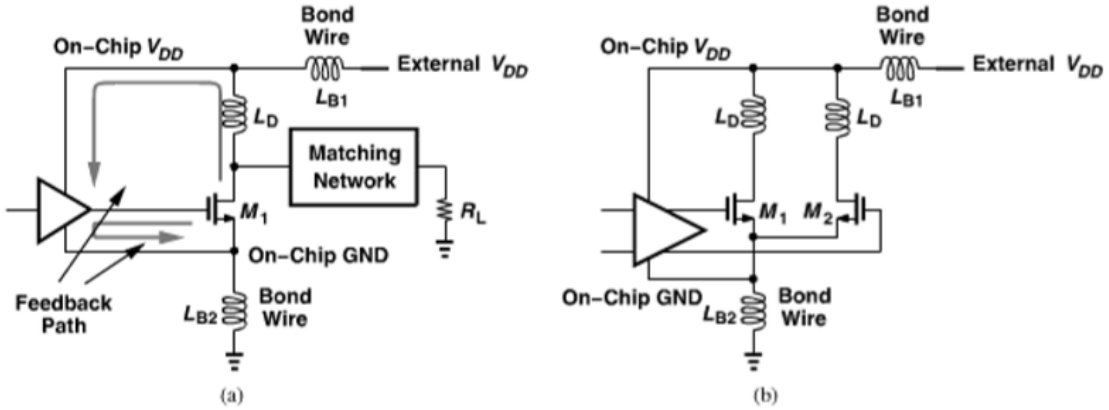

Figure 3.4: (a) feedback in single ended PA, (b) less problematic situation in differential PA

By contrast, the differential realization eases the two issues. This topology draws much smaller transient current from vdd and ground lines exhibiting less sensitivity to LB1 and LB2. A balun must now be inserted between the PA and antenna.

3.3 Classification of Power Amplifiers

Power amplifiers have been traditionally categorized under many classes: A, B, C, D, E, F, etc. An attribute of classical PAs is that both the input and the output waveforms are considered sinusoidal.

3.3.1 Class A Power Amplifiers

Class A is defined as circuit in which transistors remain on and operate linearly across the full input and output range. Transistor bias current is chosen higher than peak signal current to ensure that the device doesn't turn off at any point. If linearity is required, then class A operation is necessary.

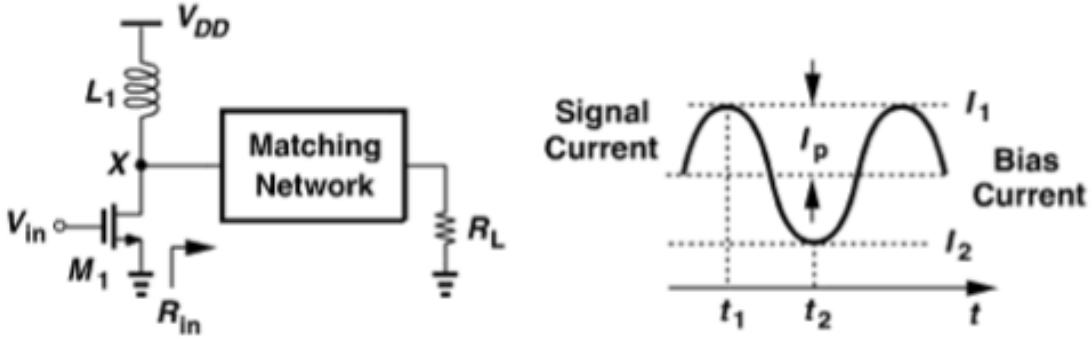

Figure 3.5: class A stage

To reach max efficiency we allow Vx to reach 2Vdd and nearly zero. Power delivered is approximately equals to

$$P_{load} = \frac{v_{dd}^2}{2R_{in}} \tag{3.3}$$

The inductive load carries a const current of Vdd/Rin. The maximum efficiency class A can reach is 50 %. The other 50 % is dissipated by M1.

3.3.2 Class B Power Amplifiers

The traditional class B PA employs two parallel stages conducts for 180 degree, Thereby achieving higher efficiency than class A. We can view the circuit as a quasi Differential stage and a balun driving the single ended load.

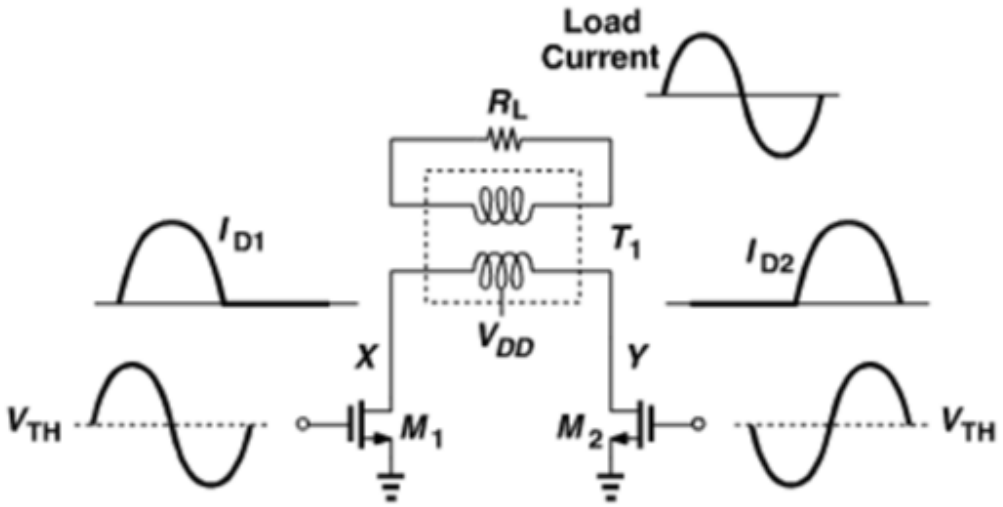

Figure 3.6: class B stage

$$\eta = \frac{\pi m^2}{4V_{dd}n^2} * I_p * R_l \tag{3.4}$$

$$\eta_{max} = 79\%$$

3.3.3 Class C Power Amplifiers

A smaller conduction angle yields higher efficiency, in class C this angle is reduced further and the circuit becomes more nonlinear. M1 turn on if peak value of vin raises Vx above Vth. The matching network provides some filtering to make the drain voltage a sinusoid .

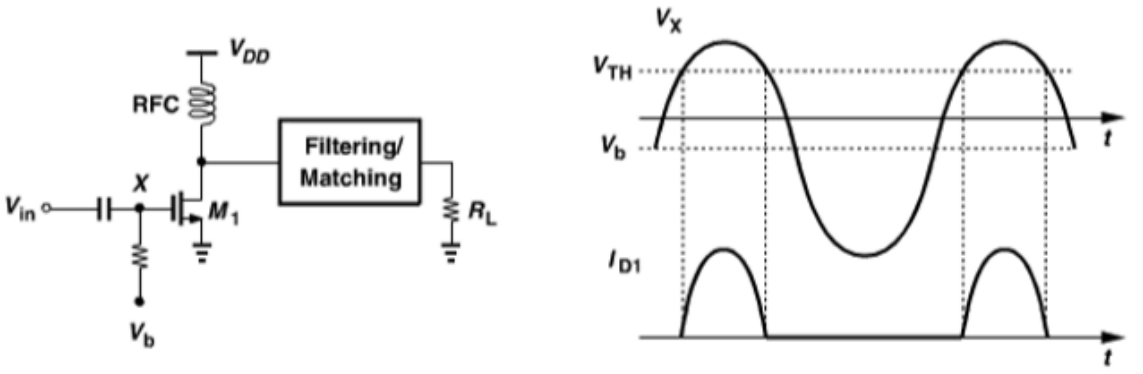

Figure 3.7: class C stage and it's waveforms

$$\eta = \frac{1}{4} * \frac{\Theta - \sin(\Theta)}{\sin(\frac{\Theta}{2}) - \frac{\Theta}{2} * \cos(\frac{\Theta}{2})} \tag{3.5}$$

Class C provides high efficiency only if it delivers fraction of peak output power .The small conduction angle dictates that output transistor be very wide to deliver high Current for short time.

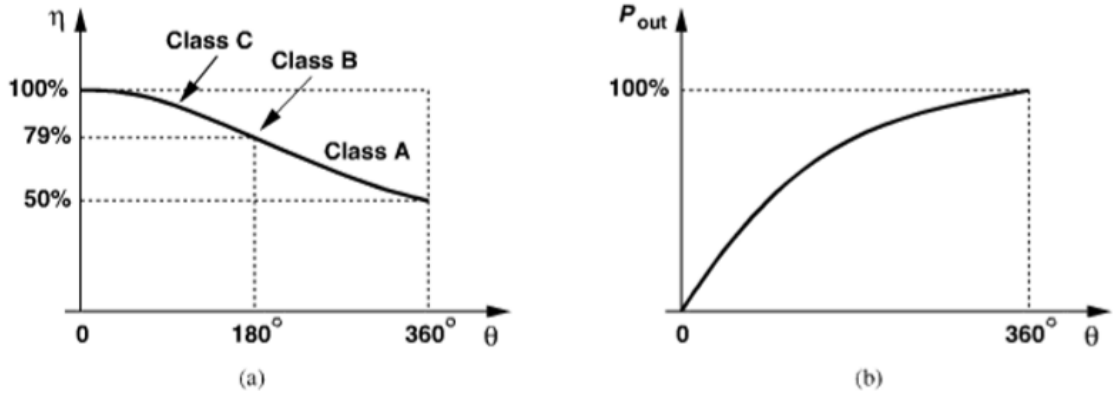

Figure 3.8: (a) efficiency and (b) output power as function of conduction angle

3.4 High Efficiency Power Amplifiers

The main premise in class A,B and C is that, output current and voltage waveforms are sinusoidal. this premise is discarded, higher harmonics can be exploited to improve the performance. The following topologies rely on specific output passive network to shape the wave forms and minimizing the time during which the transistor carries a large current and sustains large voltage.This approach reduces the power consumed by the transistorand raises efficiency.

3.4.1 Class A with Harmonic Termination

In class A, for max efficiency, the current swings by large amount experiencing nonlinearity. thus, the current contains significant second and third order harmonic Suppose the matching network is designed such that its input impedance is low at fundamental and high at second harmonic. The resulting voltage waveform exhibits narrow pulses, reducing overlap time between and voltage in transistor hence, efficiency increases.

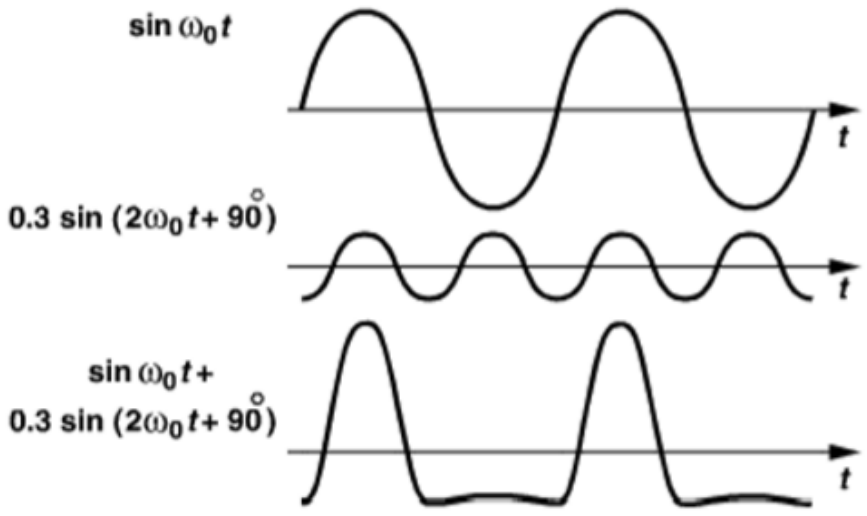

Figure 3.9: example of second harmonic enhancement

This technique simply realizes different impedence terminations for different harmonics to make drain voltage approaches a square wave.

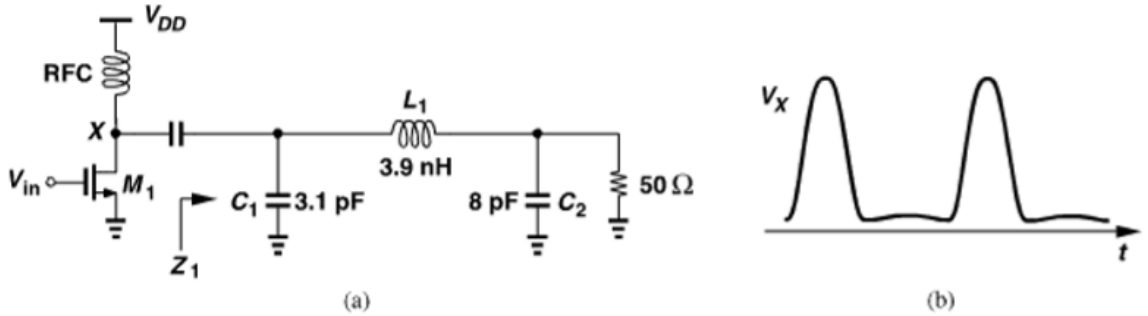

Figure 3.10: (a) class A with harmonic enhancement, (b) drain waveform

3.4.2 Class E Power Amplifiers

Class E PAs achieve efficiencies approaching 100%. Output transistor operates as switch "switching PA". Such topology achieve high efficiency if :

1. M1 sustains small voltage when carrying current.
2. M1 carries small current when it sustains finite voltage.
3. Transition times between on and off states are minimized.

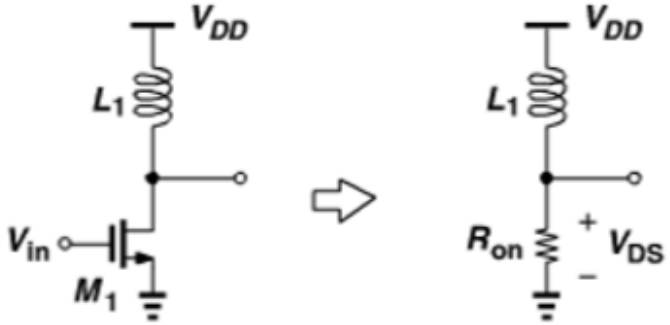

Figure 3.11: output stage with switching transistor

In previously studied PAs, the transistor operates as a current source, whereas in this class this is not necessary. To act as current source, Vds

must be controlled to operate in SAT region , this Vds translates to lower efficiency. A serious problem is that, the gate of output device must be switched abruptly but, large output transistor necessitate resonance at it's gate, receiving nearly sinusoid waveform. Class E PAs deals with switching problem by proper load design.

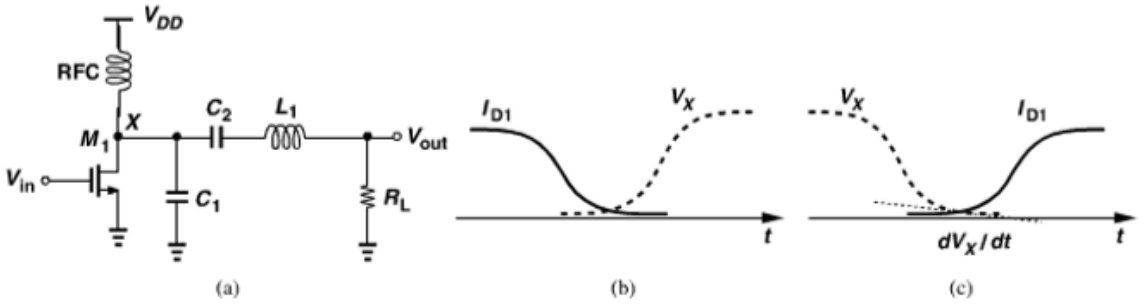

Figure 3.12: (a) class E stage (b) condition to ensure minimum overlap between drain current and voltage (c) condition to ensure low sensitivity to timing errors

In this example C1,C2,L1,Rl are chosen to satisfy conditions.

1. As switch turns off Vx remains low until Id drops to zero.

2. Vx reaches zero just before switch turns on.

3. dVx/dVt is near zero when switch turns on.

For Second and third condition implementation, After switch turns off the load network operate as damped second order system. depending on Q the network exhibits underdamped, overdamped and critically damped response. There is a trade off between efficiency and output harmonics as for low harmonics, Q must be higher than that required by second and third conditions.

3.4.3 Class F Power Amplifiers

Class F relays on the idea of harmonic termination. If in generic switching stage the load provides high termination at second or third harmonics, the waveform across the switch exhibits sharper edges than sinusoid thus, reduce power loss in this figure L1,C1 resonates at twice or three times the input frequency thus, Vx approaches rectangular waveform. If drain current is assumed half wave rectified sinusoid thenthe peak efficiency of class F is equal to 88%.

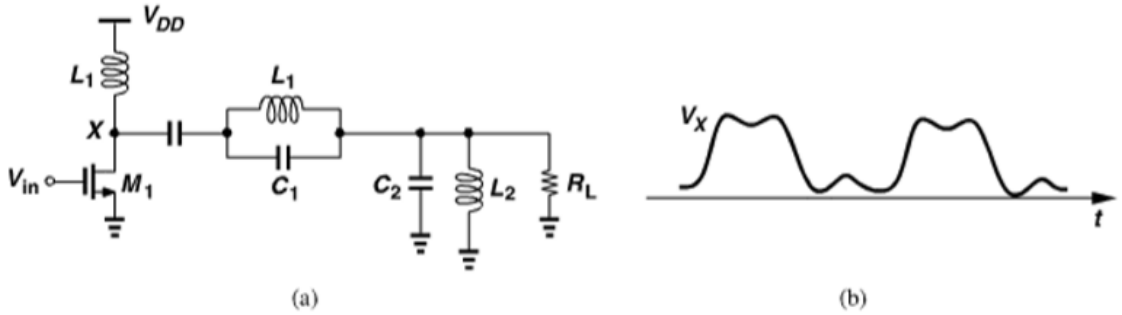

Figure 3.13: class F example

3.5 Cascode Output Stages

In previous sections to achieve high efficiency the output stage produce a waveform with swing of nearly 2Vdd. If Vdd is chosen equal to nominal value then, the transistor experiences breakdown or substantial stress. If we choose Vdd half of max tolerable voltage of transistor, the lower headroom limits linear range and higher current (for the same power) leads to greater loss in matching network. A cascode device relaxes the above costrains, as it shields the input transistor as Vx rises.

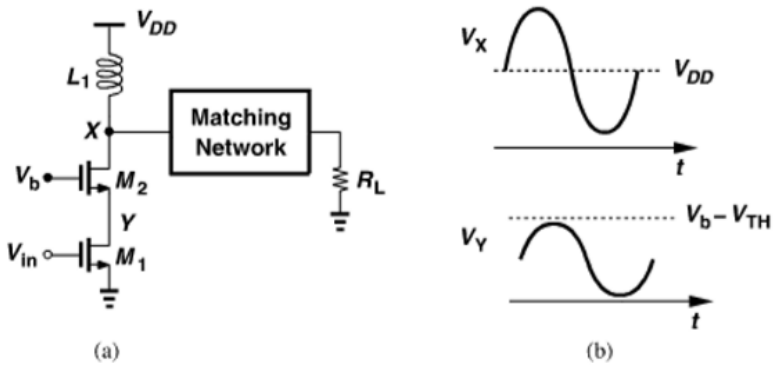

Figure 3.14: (a) cascode PA and (b) it's waveforms

3.6 Specifications and Design Methodology

Parameter	**Specification**
Output Power	programmable from -20 dBm to 6 dBm with step of less than 2dB.
Efficiency	> 50 % at 6dBm
Second Harmonic	< -45 dBm at all Power Levels
Third Harmonic	< -45 dBm at all Power Levels
Input Capacitance	$< 20fF$
Number of L & C Components	$<= 6$ Components

Table 3.1: Specifications of the Proposed PA

The physical schematic design will be presented and simulated in the Cadence ADE with TSMC 65 nm process Technology. The circuit can be broken into three parts:

1. An output stage implemented using switching topology to achieve the required efficiency, cascode device to act as protection for the

input device and a third order low pass filter to achieve the required attenuation and filtering for 2nd and 3rd harmonics.

2. Driving stages implemented by CMOS inverters to drive the output stage, modify the input duty cycle to achieve required specs and achieve the required input capacitance.

3. Biasing circuit for the cascode device with digital input to control the biasing voltage of the cascode device by applying different voltage drops at the gate thus, control Vds of the input device and control the drawn current from the supply to achieve the required power levels.

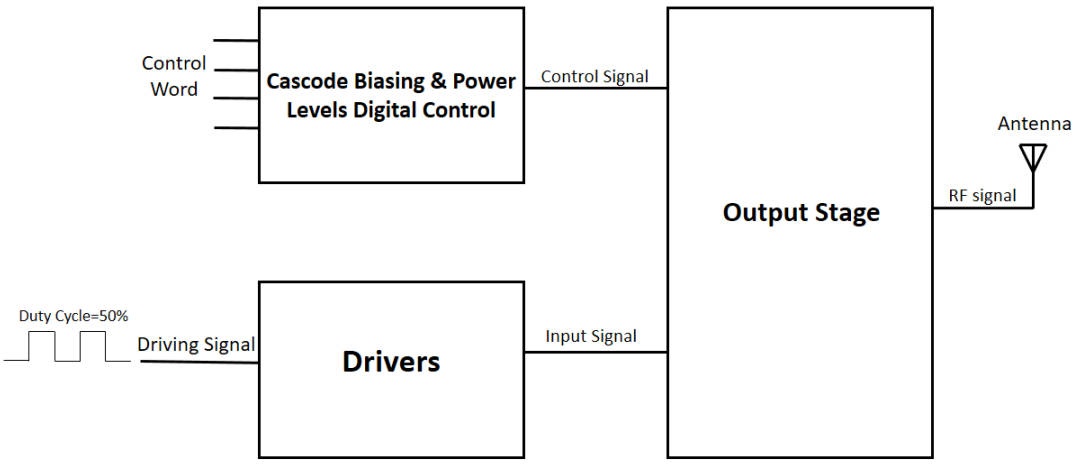

Figure 3.15: top level view of PA

3.6.1 Output Stage

The output stage is implemented using class E to achieve the required efficiency and as there is no spec on linearity so, a switching topology seems to be convenient to meet the required specs. A RF device is used as the

switching input device and another device is used as a cascode device to protect the input device from breakdown as the drain voltage jumps to twice the supply value. A third order low pass filter is placed at the rear to help attenuation of 2nd and 3rd harmonics and to transform the load resistance (antenna input resistance) to the optimum loading value so as to achieve the best results for power, efficiency and harmonics. In order to decrease the number of used L C off-chip components, we make use of pad capacitance of value 250 fF as the drain capacitance in class E topology. The values for circuit components and devices sizing are obtained using class E design equations and using optimization to get to the best point to achieve required specs.

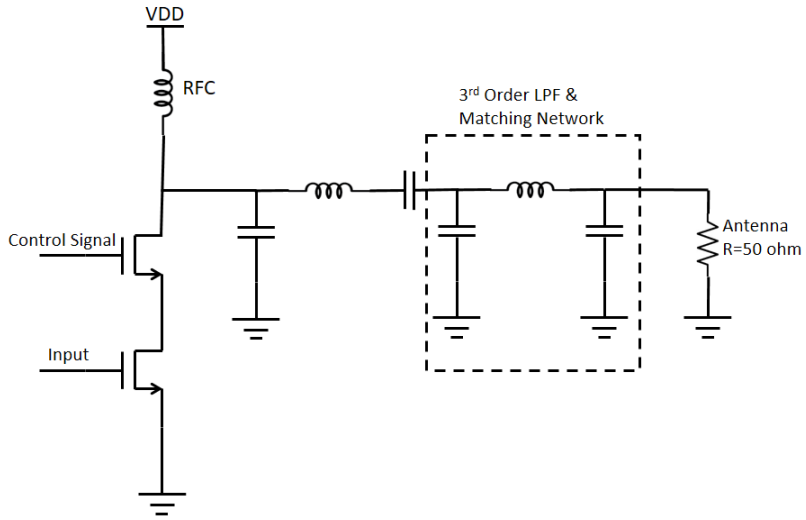

Figure 3.16: Output Stage

3.6.2 Driving Stages

The driving stages are CMOS inverters as the driving signal is a square wave of duty cycle 50%. The inverters are sized such that the input capaci-

tance of the power amplifier is less than 20fF and to achieve the optimum value of duty cycle to the output stage.

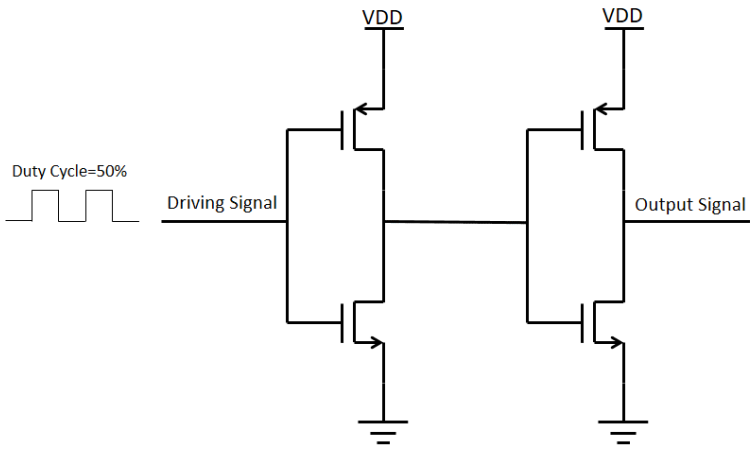

Figure 3.17: Driving Stages

3.6.3 Biasing Circuit and Digital Control

Power Levels are implemented by controlling the voltage drop at the gate of the cascode device in order to control Vds of input device thus, changing the drawn current from the supply. This can simply achieved by using number of resistors and switches equals to the number of power levels and a current source. Each resistor can be chosen by a applying a high voltage to the gate of the switch while other switches are open by applying zero voltage at their gates. Another device of the same length of the cascode device is added and diode connected to the gate of the cascode device. The main function of this device is to achieve good tracking for the cascode device across process, voltage and temperature variations. So, each time

a resistor is selected, the gate voltage equals to Vgs+i*R. The gate of each switch is connected to AND gate, the output of the gate will be high only when It's level is activated by the input digital bits.

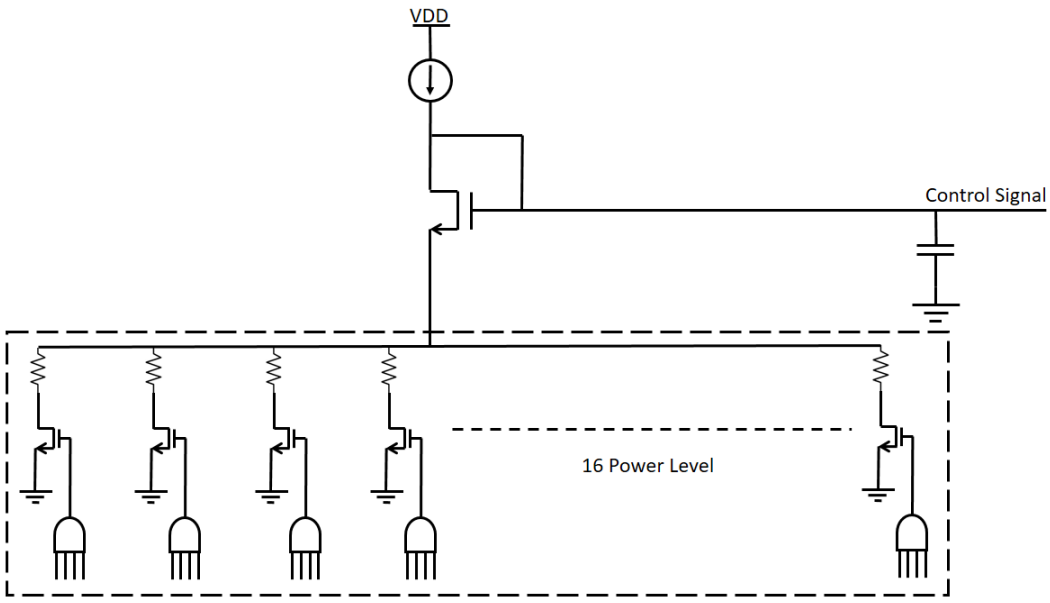

Figure 3.18: biasing circuit and digital control

3.7 Simulation Results

The whole circuit has been simulated and tested using cadence virtuoso design suit to make sure that it meets the specs across typical, corners and montecarlo simulation.

3.7.1 Typical Simulation Results

The harmonic balance analysis was performed to observe the power levels, harmonics and efficiency and make sure that the required specs are met across the band of Bluetooth from 2.4GHz to 2.48GHz with center frequency 2.44GHz.

3.7.1.1 Input Capacitance

The proposed design achieves an input capacitance of 17 fF .

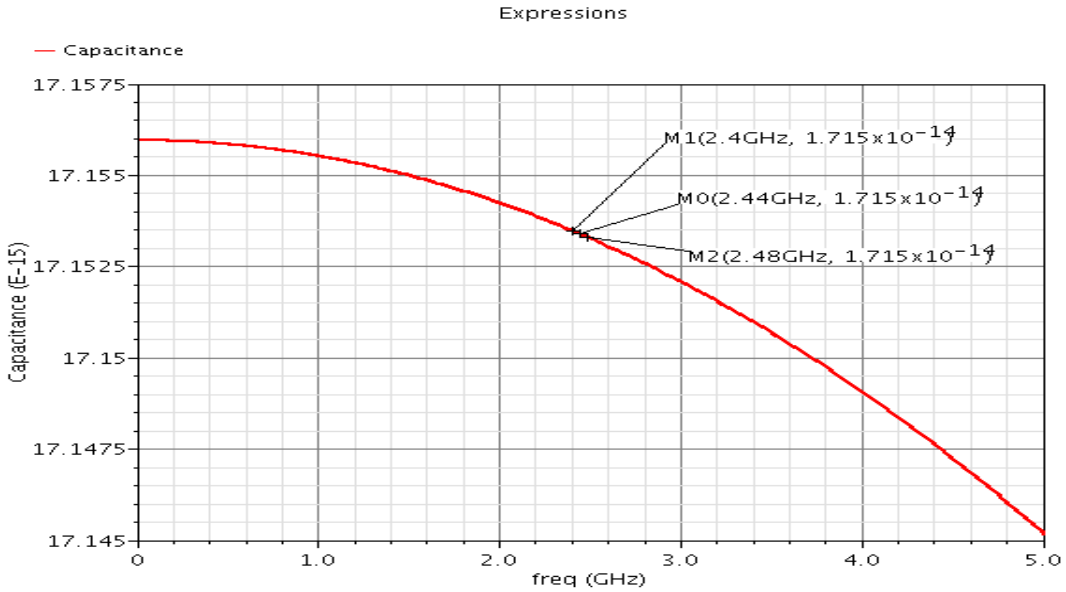

Figure 3.19: input capacitance

3.7.1.2 Power Levels

The proposed design achieves 16 power level from -20 dBm to 6 dBm with step size of 1.75 dB. These power levels are digitally controlled using four input digital bits from state 0000 (6 dBm) to state 1111 (-20 dBm).

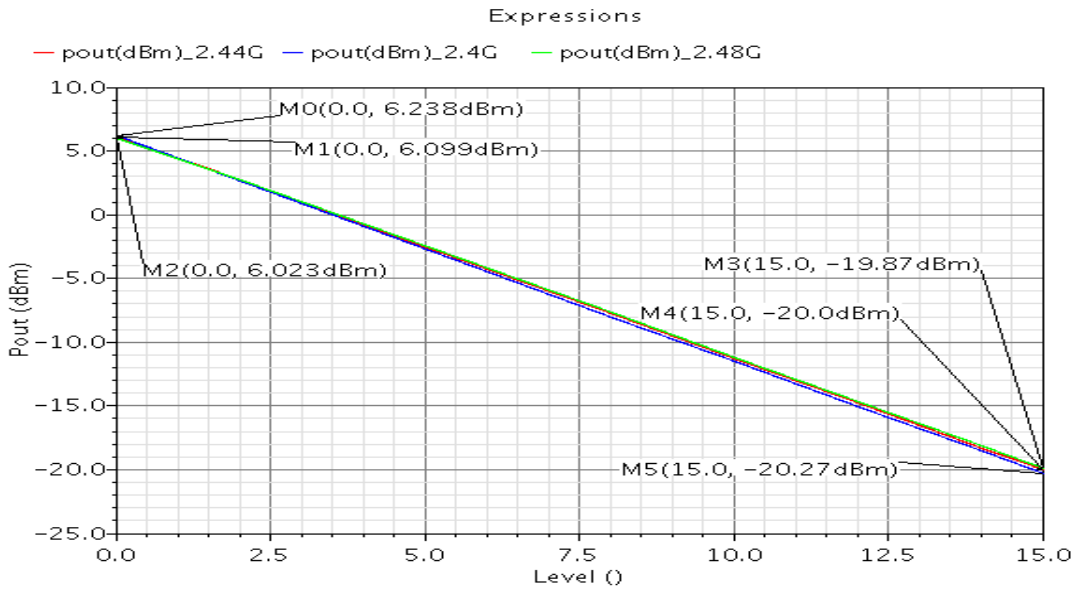

Figure 3.20: power levels

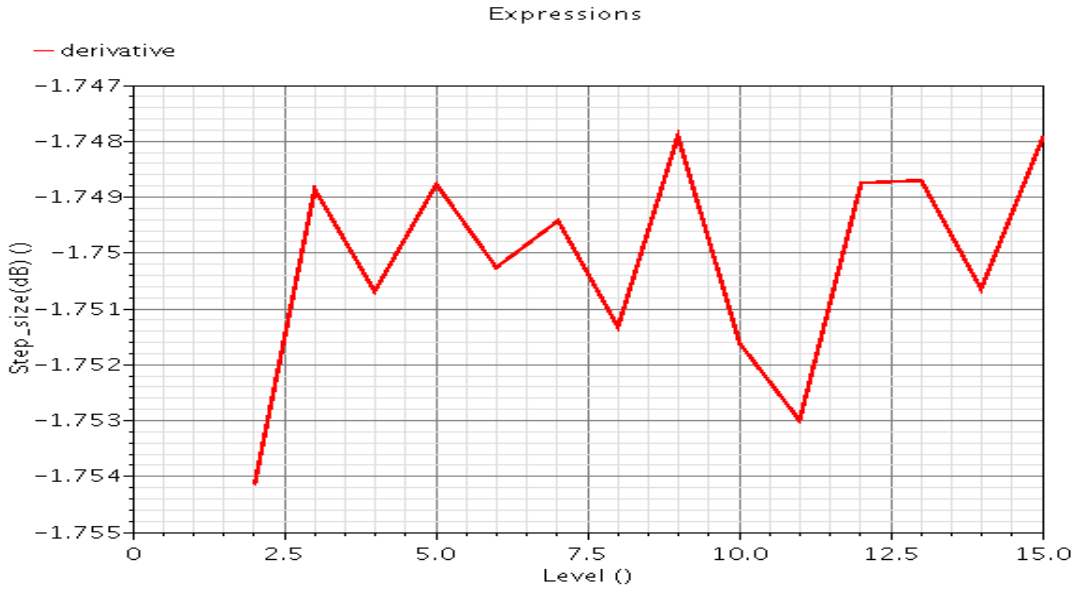

Figure 3.21: Step size

3.7.1.3 Efficiency

The proposed design achieves an efficiency around 58% at 6 dBm.

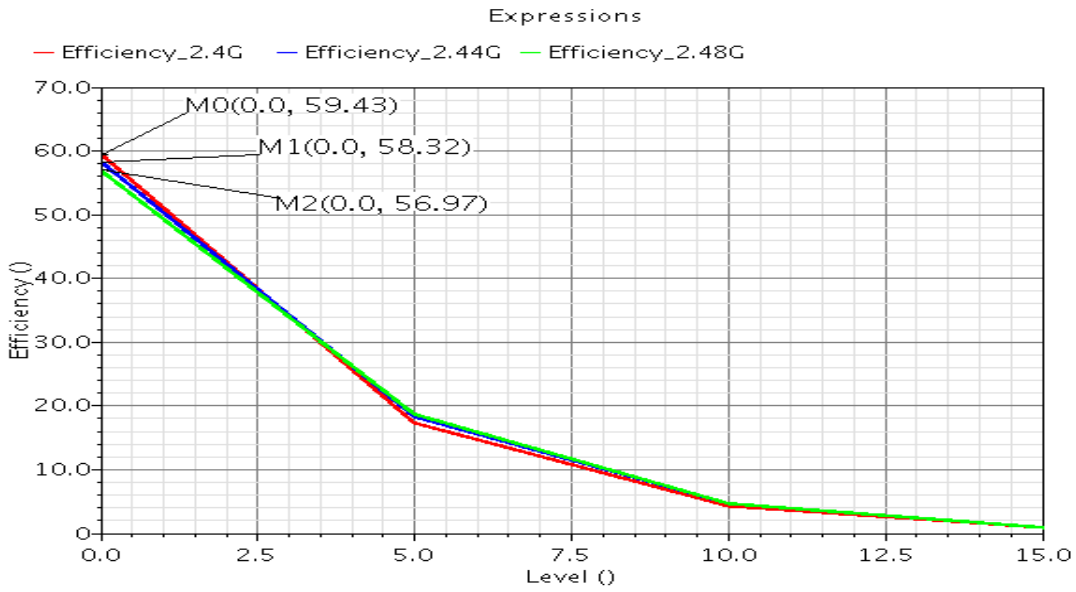

Figure 3.22: efficiency

3.7.1.4 Second Harmonic

The proposed design achieves a second harmonic level below -45 dBm at all power levels across the frequency band. It equals to -49 dBm at maximum power level.

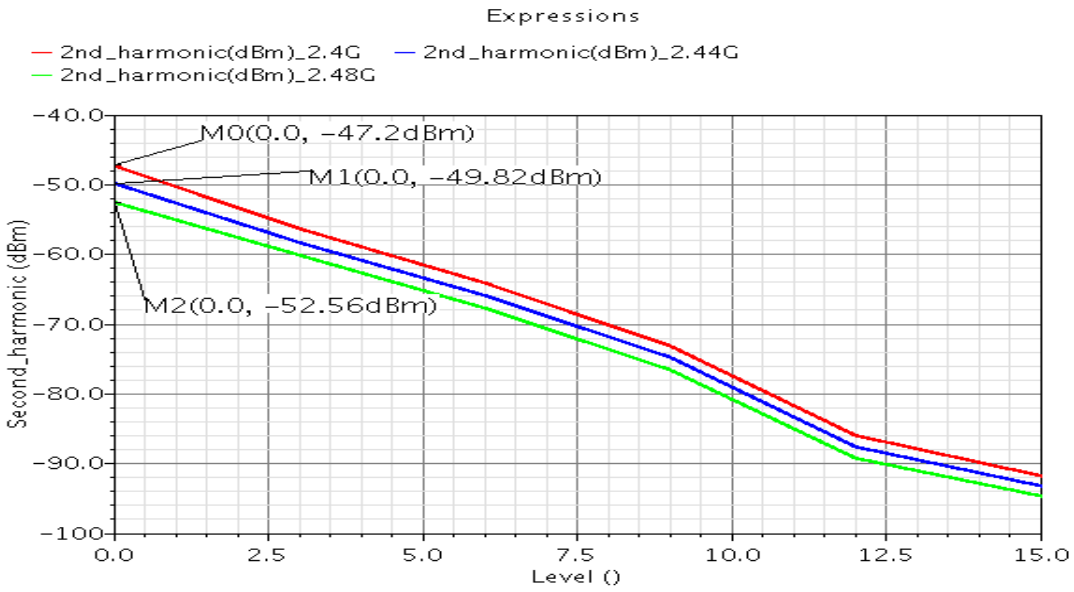

Figure 3.23: second harmonic

3.7.1.5 Third Harmonic

The proposed design achieves a Third harmonic level below -45 dBm at all power levels across the frequency band. It equals to -100 dBm at maximum power level.

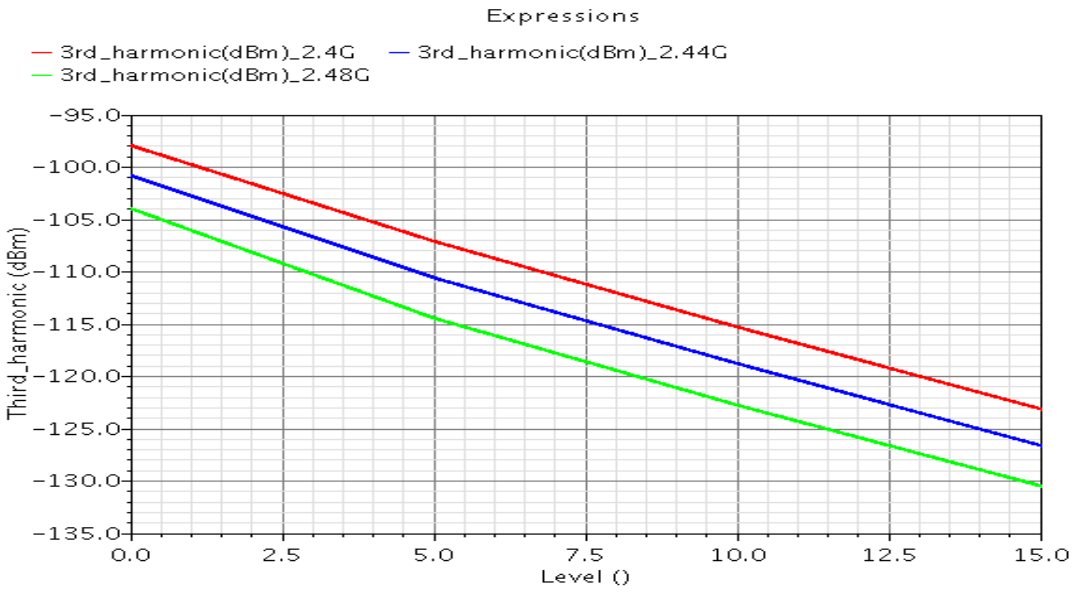

Figure 3.24: third harmonic

3.7.2 Corners Simulation Results

Corners are simulated to consider PVT variations as shown in table 1.2. The corners are simulated versus power levels at the center frequency 2.44GHz and at edges of Bluetooth band 2.4GHz and 2.48GHz. The accepted deviation of power levels from the nominal value is 2 dB at high Power levels and 3 dB at low power levels.

Parameter	**Variation**
Temperature	$\{-40^oC, 125^oC\}$
Supply	$\{0.95V, 1.05V\}$
Transistors	$\{FF, SS, FS, SF\}$
Resistors	$\{FF, SS\}$
Capacitors	$\{FF, SS\}$
Input Duty Cycle	$\{47.5\%, 52.5\%\}$

Table 3.2: Simulated PVT Corners

3.7.2.1 Power Levels

-Results at 2.4GHz

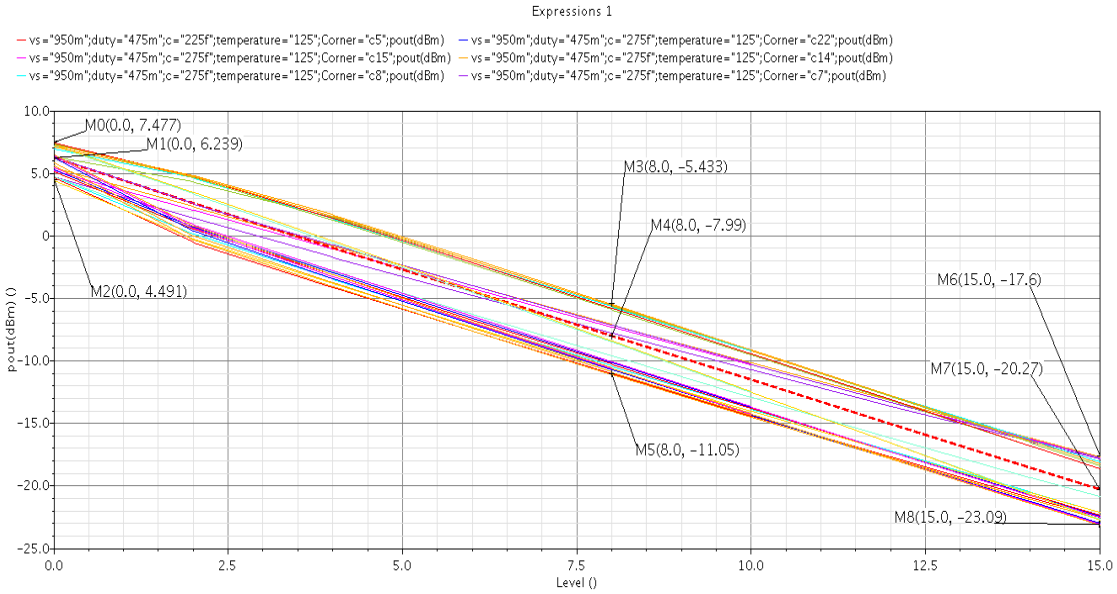

Figure 3.25: power levels across corners at 2.4GHz

-Results at 2.44GHz

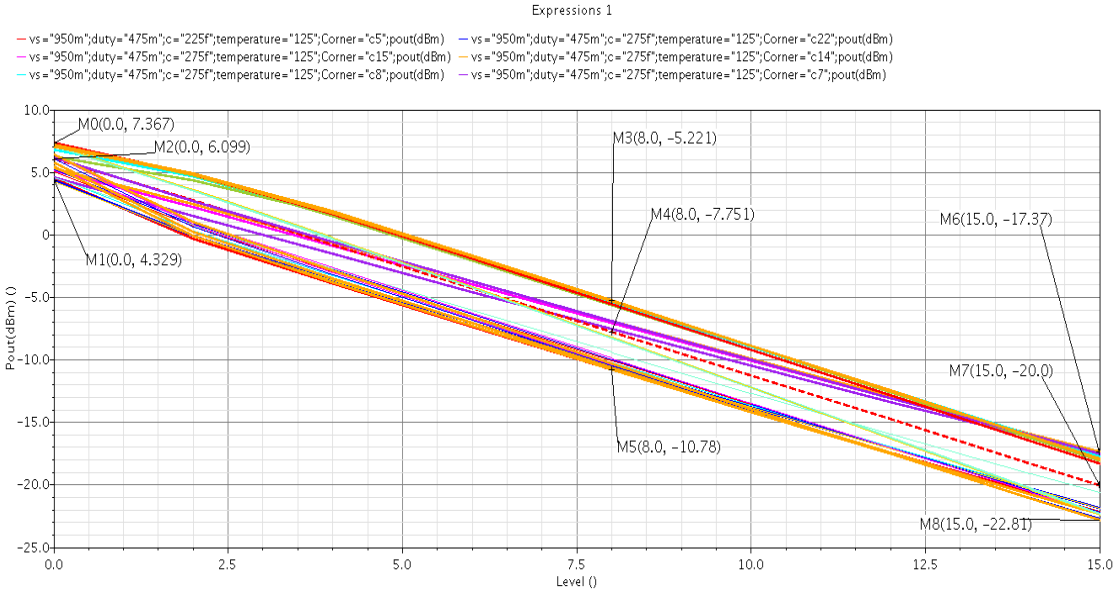

Figure 3.26: power levels across corners at 2.44GHz

-Results at 2.48GHz

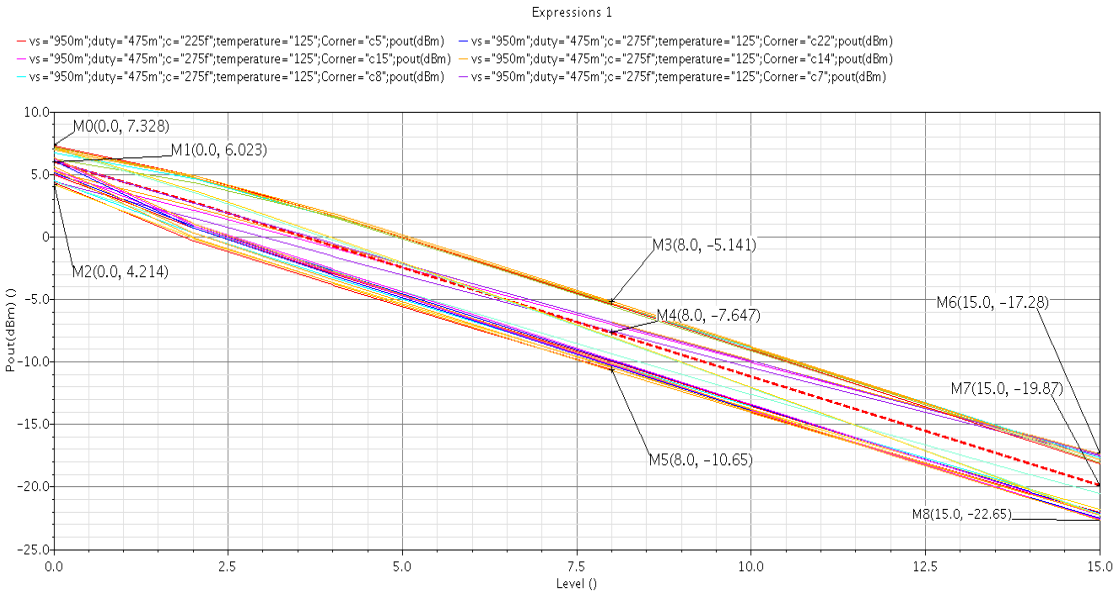

Figure 3.27: power levels across corners at 2.48GHz

3.7.2.2 Efficiency

-Results at 2.4GHz

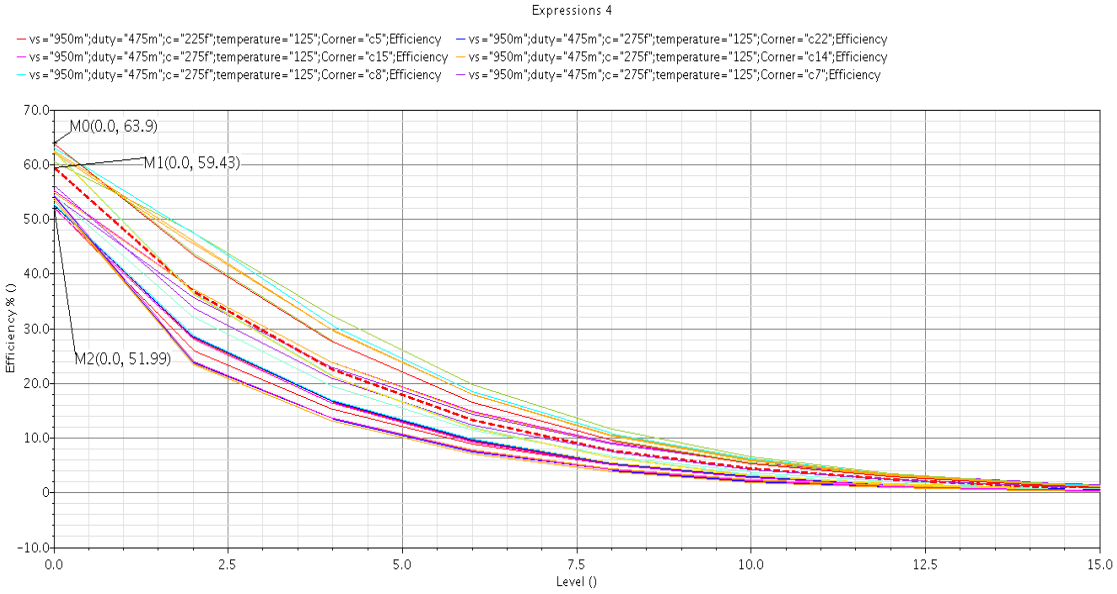

Figure 3.28: efficiency across corners at 2.4GHz

-Results at 2.44GHz

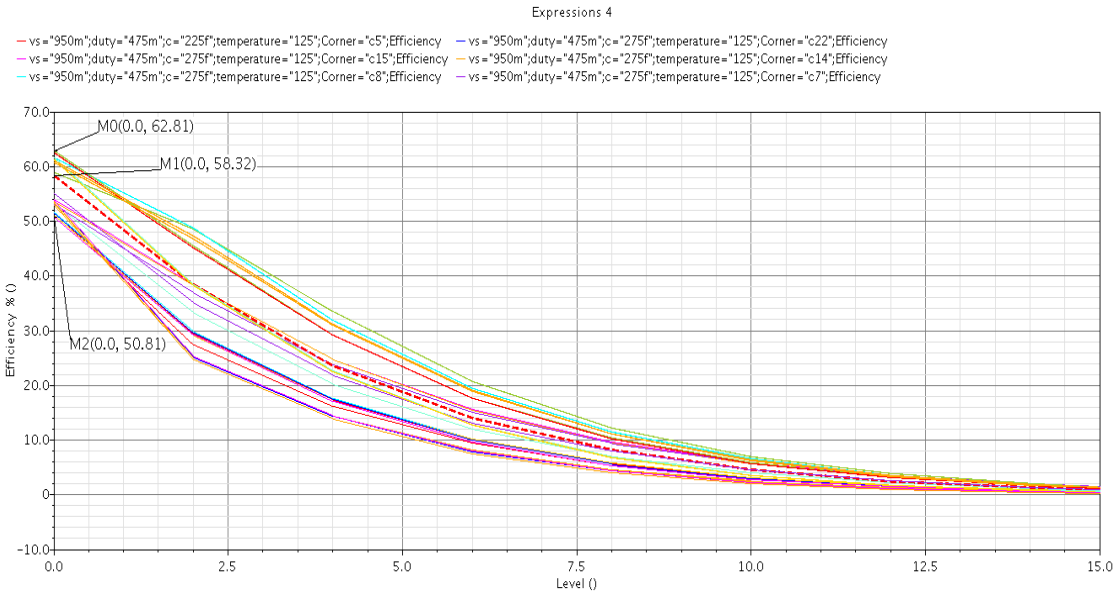

Figure 3.29: efficiency across corners at 2.44GHz

-Results at 2.48GHz

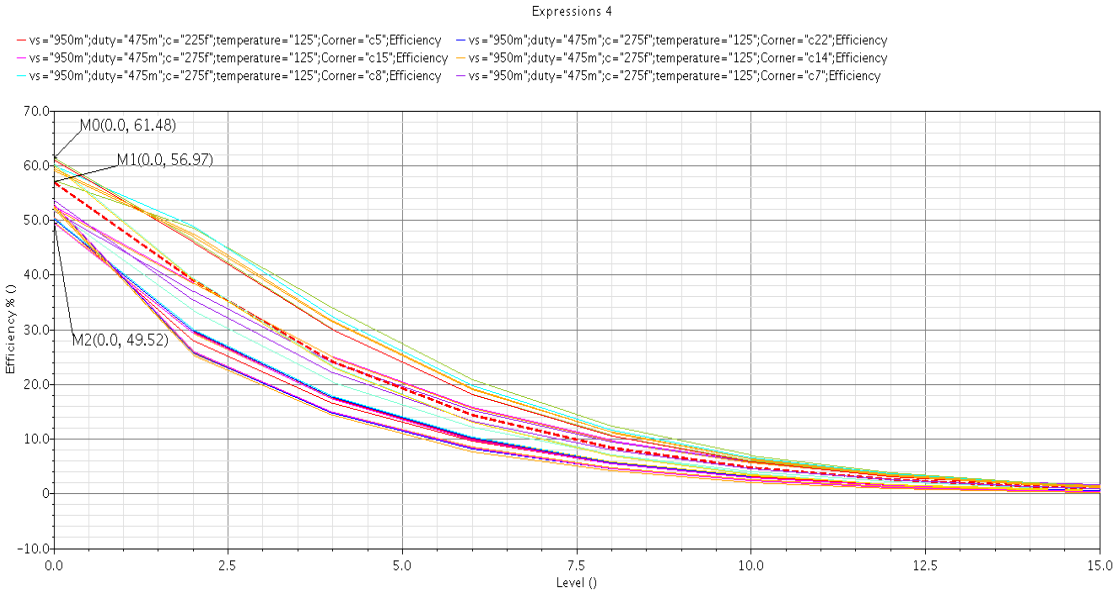

Figure 3.30: efficiency across corners at 2.48GHz

3.7.2.3 Second Harmonic

-Results at 2.4GHz

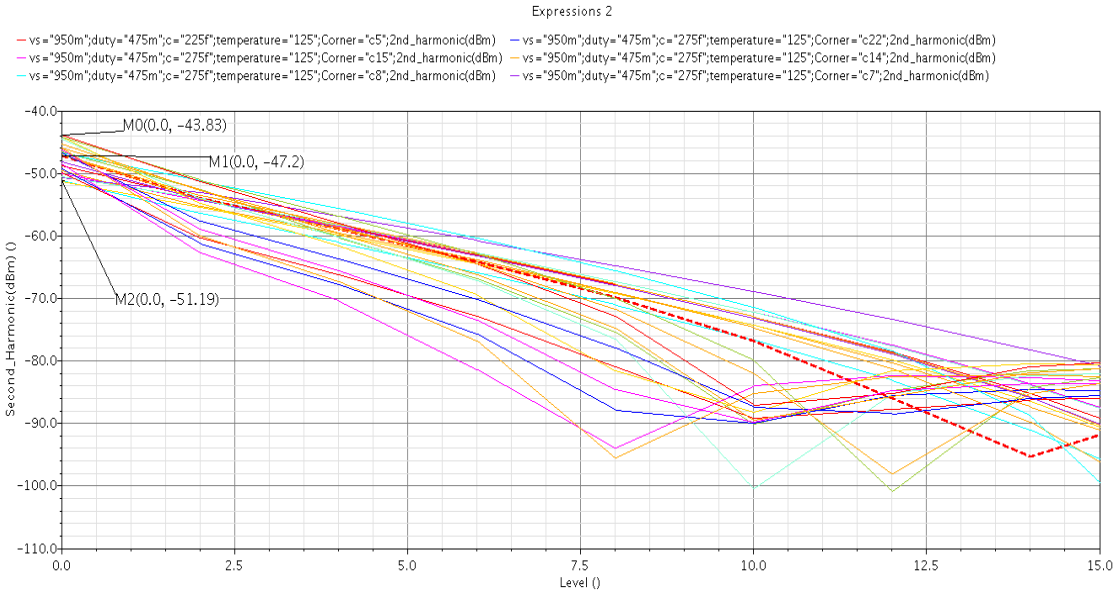

Figure 3.31: second harmonic across corners at 2.4GHz

-Results at 2.44GHz

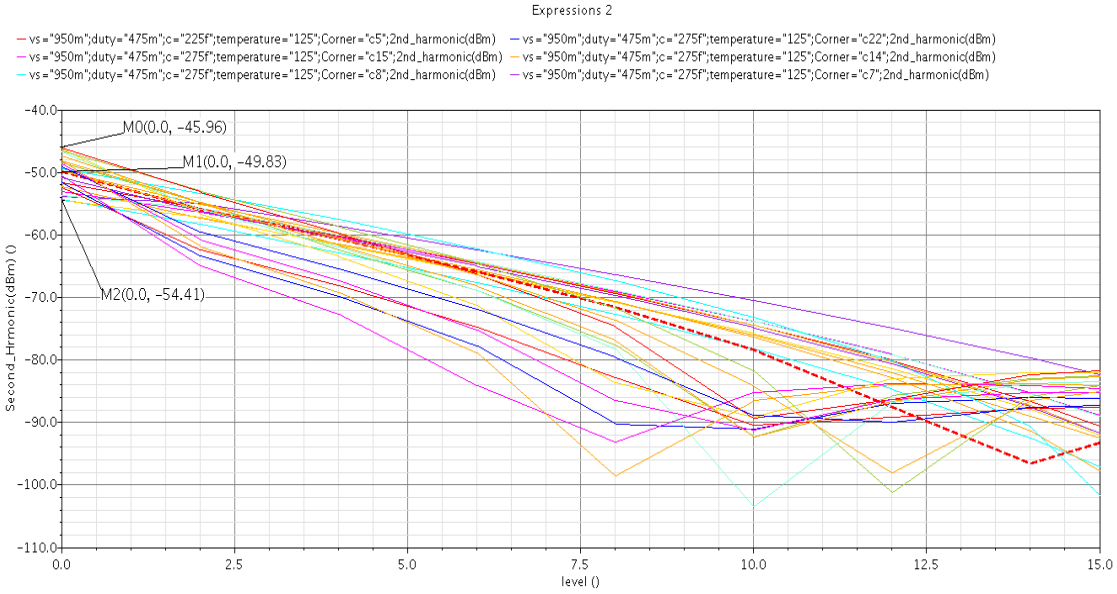

Figure 3.32: second harmonic across corners at 2.44GHz

-Results at 2.48GHz

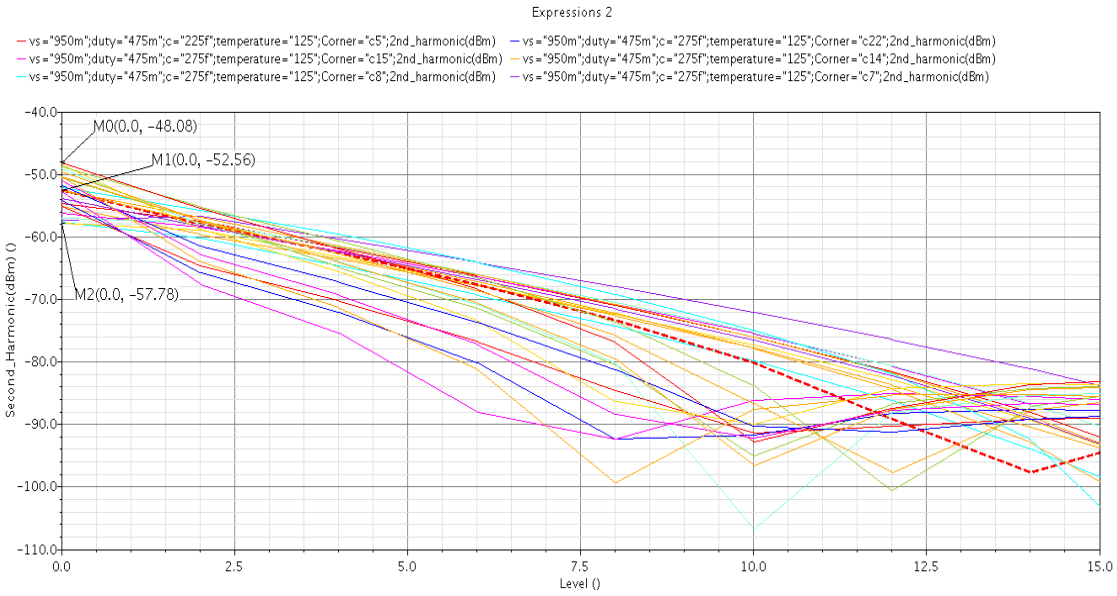

Figure 3.33: second harmonic across corners at 2.48GHz

3.7.2.4 Third Harmonic

-Results at 2.4GHz

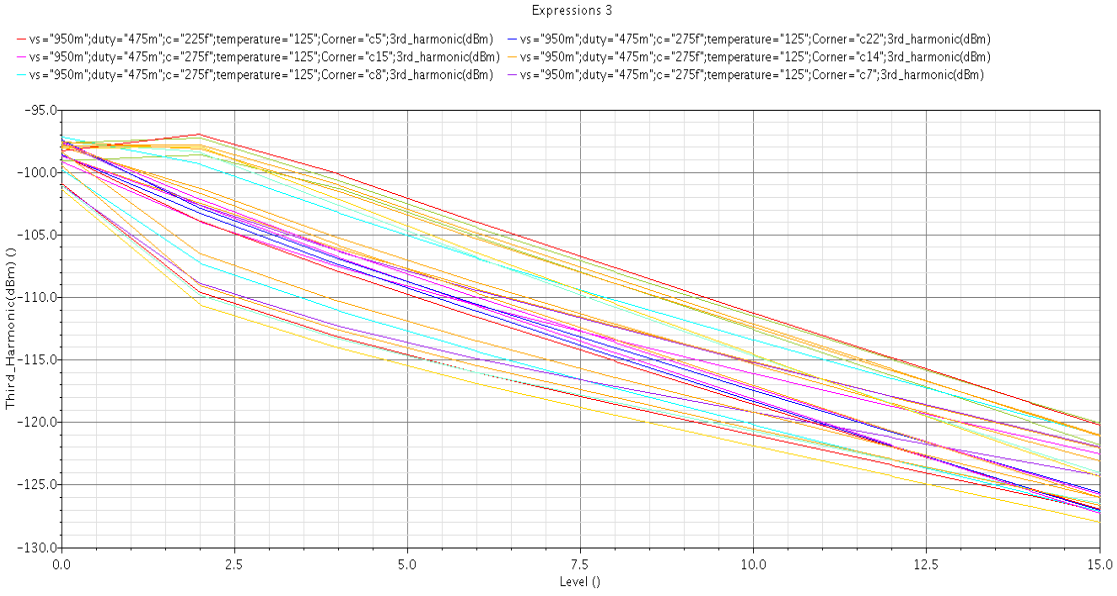

Figure 3.34: Third harmonic across corners at 2.4GHz

-Results at 2.44GHz

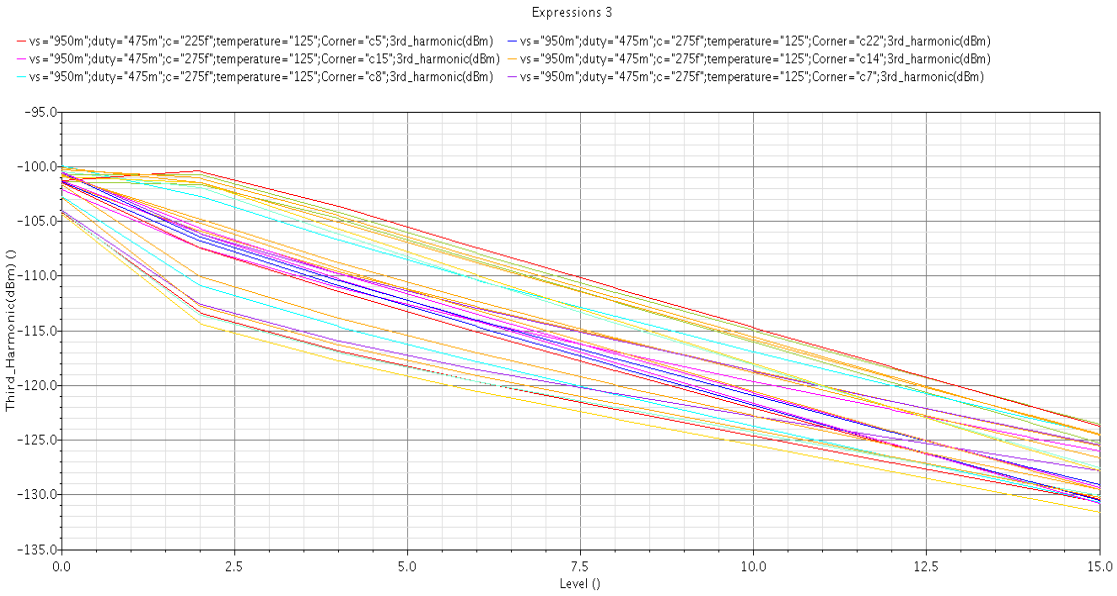

Figure 3.35: Third harmonic across corners at 2.44GHz

-Results at 2.48GHz

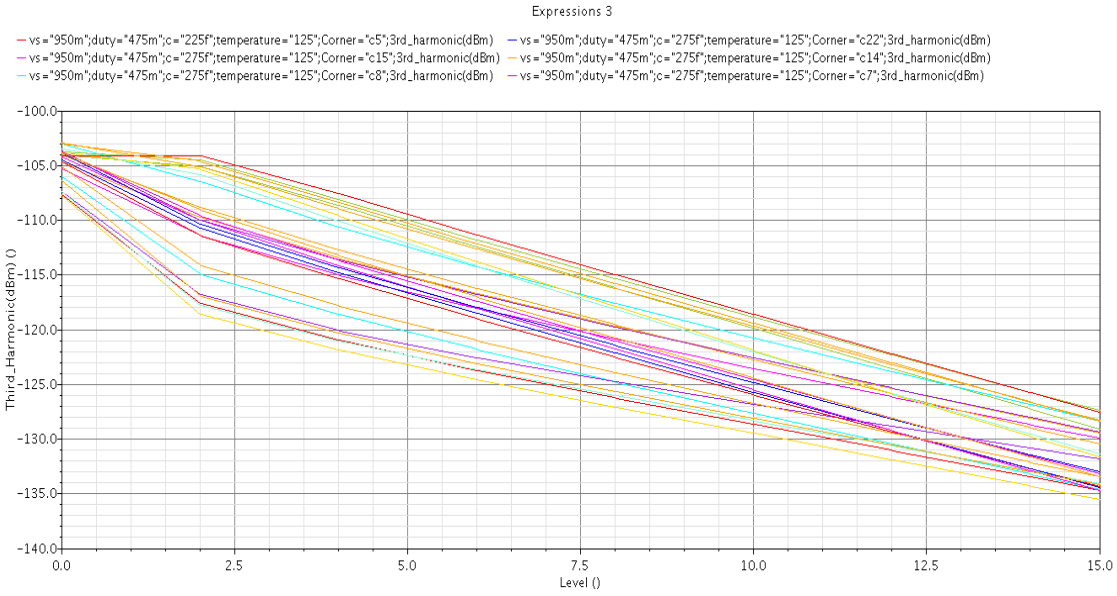

Figure 3.36: Third harmonic across corners at 2.48GHz

3.7.3 Monte-Carlo Results

Monte-Carlo sampling (Mismatch) of 500 points was run at the worst case corners of power levels, efficiency and second harmonic. As we have 16 level of power, monte-carlo was run only At worst Corners (high low) and typical of $\text{level}_0(6.1Bm), level_8(-7.75dBm) and level_{15}(20dBm)$.

3.7.3.1 Power Levels

-Level0 Results

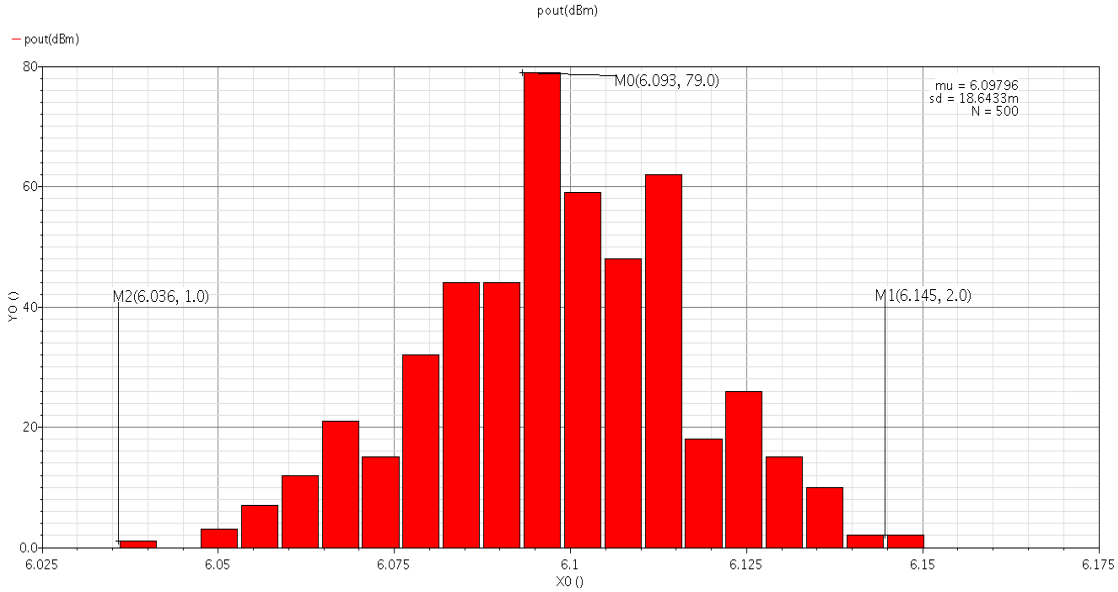

Figure 3.37: nominal results (mean= 6.1dBm)

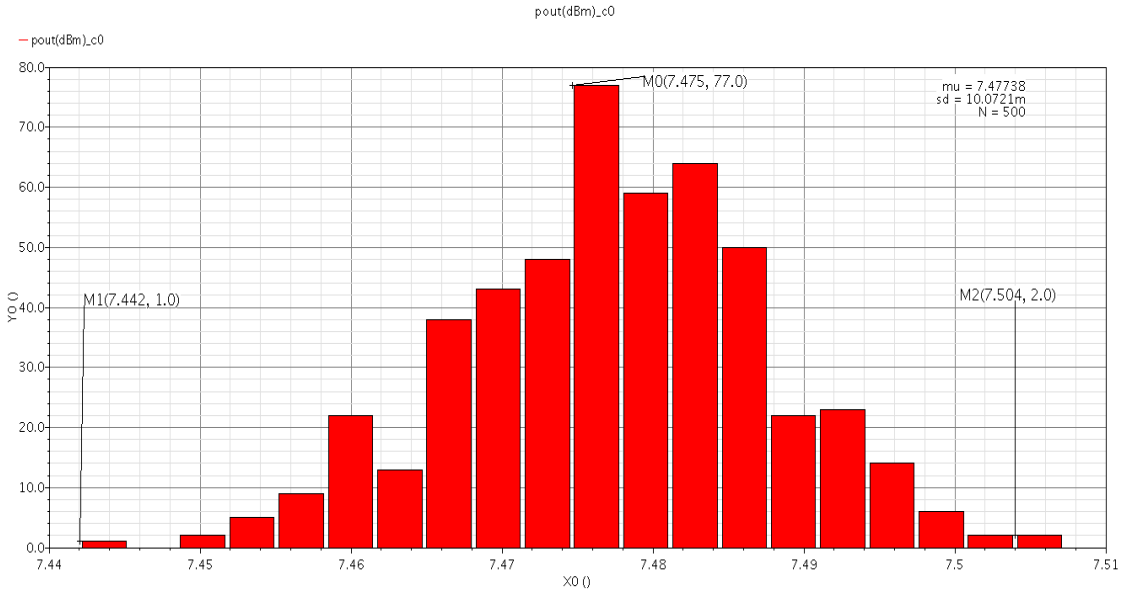

Figure 3.38: high corner results (mean= 7.47dBm)

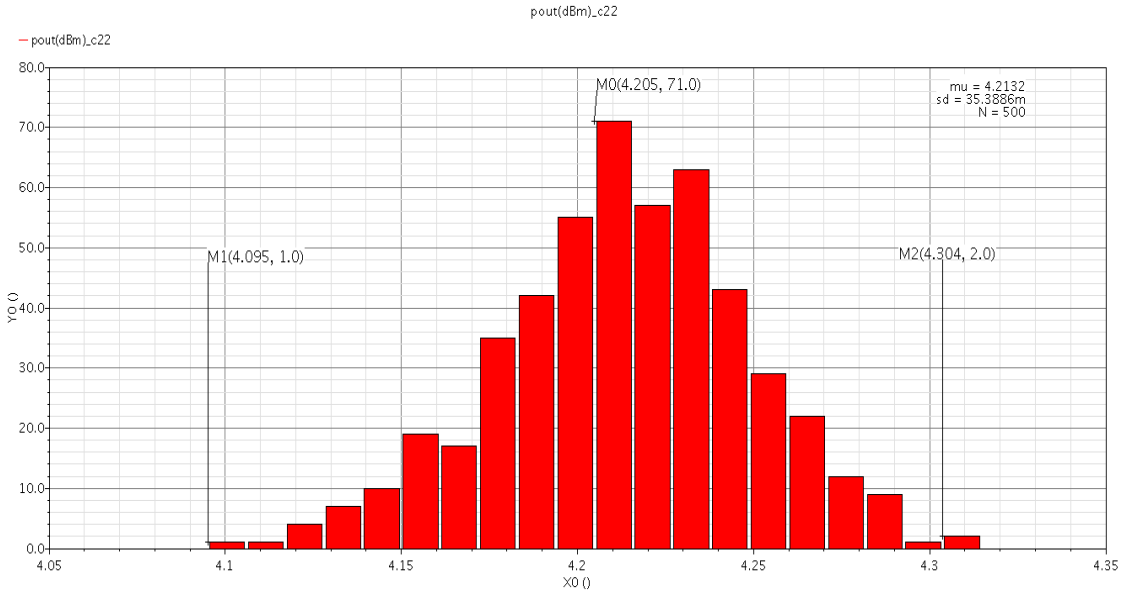

Figure 3.39: low corner results (mean= 4.2dBm)

-Level8 Results

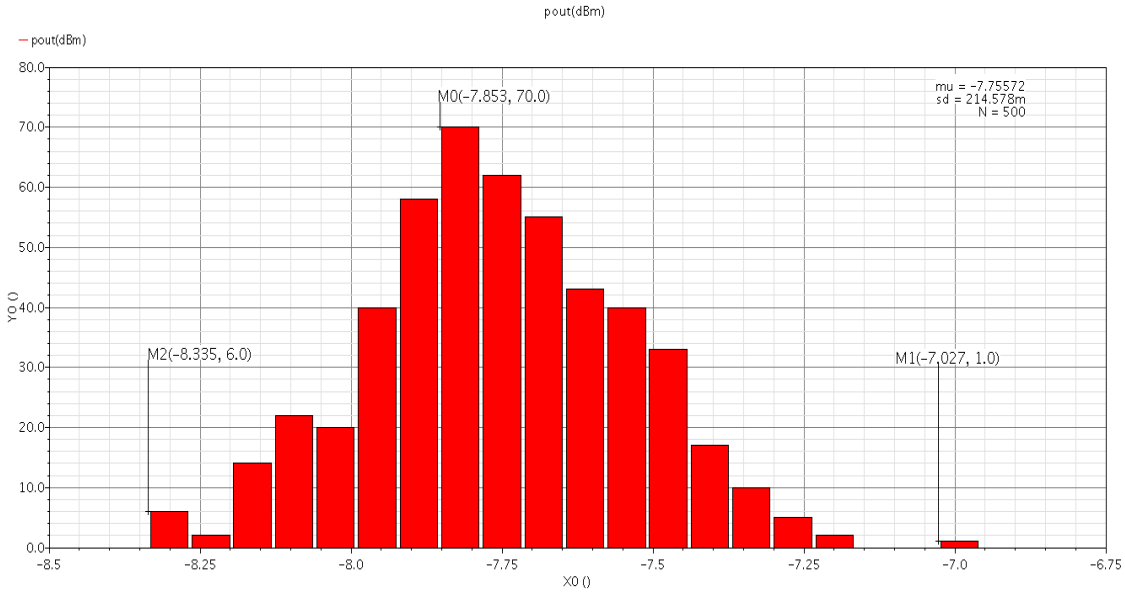

Figure 3.40: nominal results (mean=-7.75dBm)

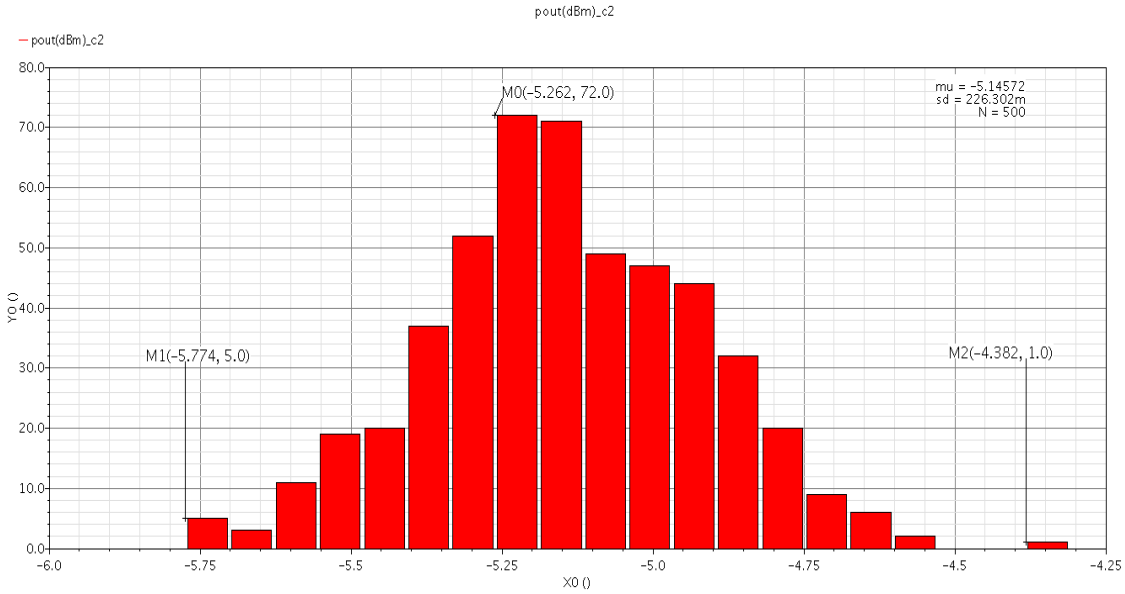

Figure 3.41: high corner results (mean=-5.14dBm)

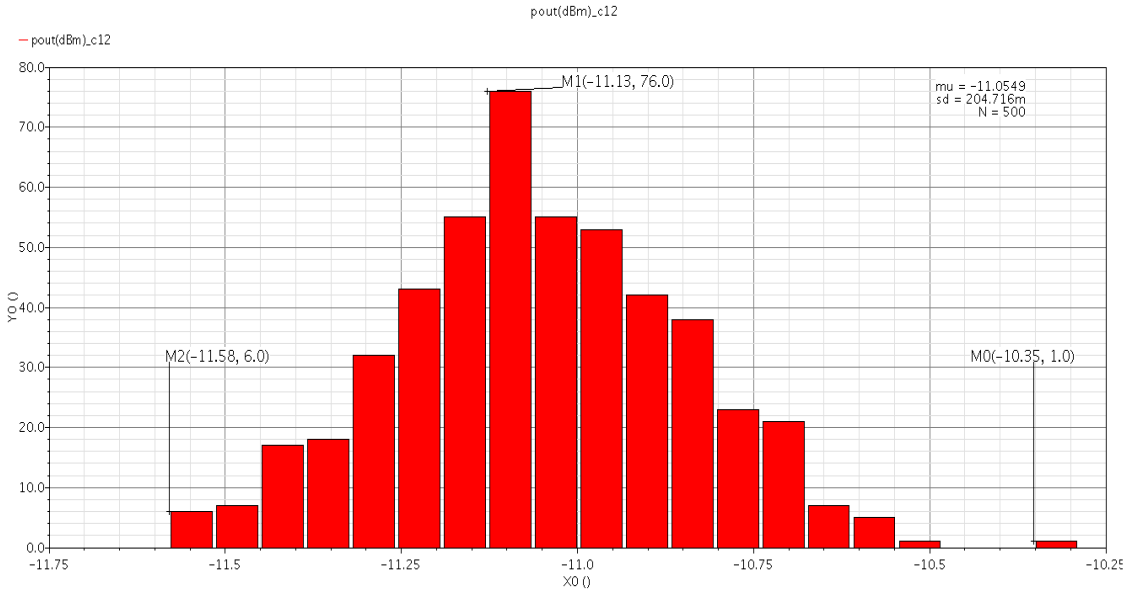

Figure 3.42: low corner results (mean=-11.05dBm)

-Level15 Results

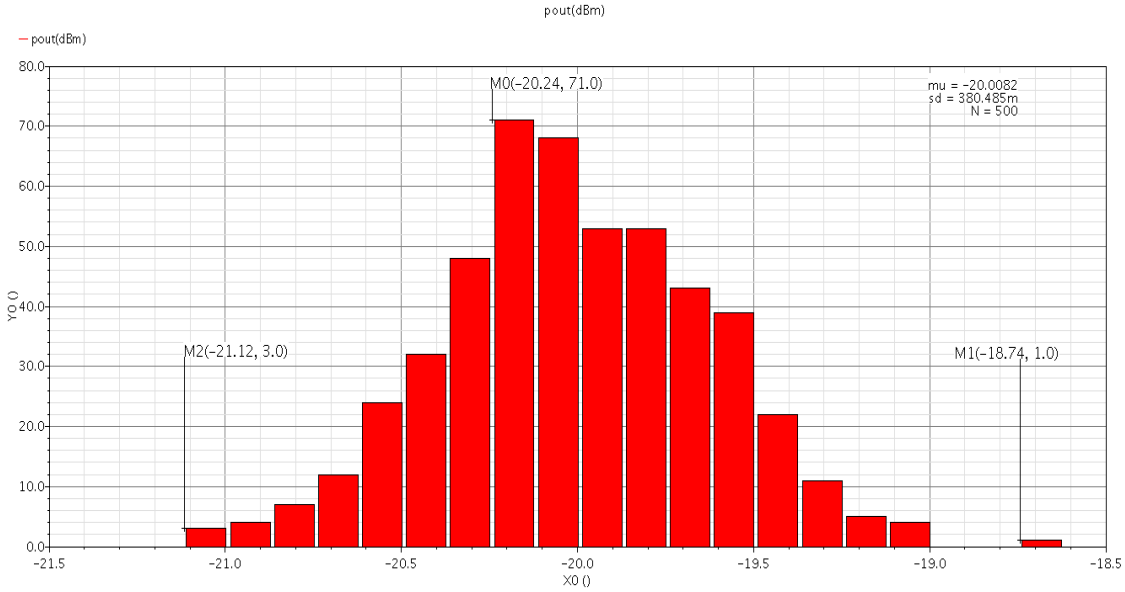

Figure 3.43: nominal results (mean=-20dBm)

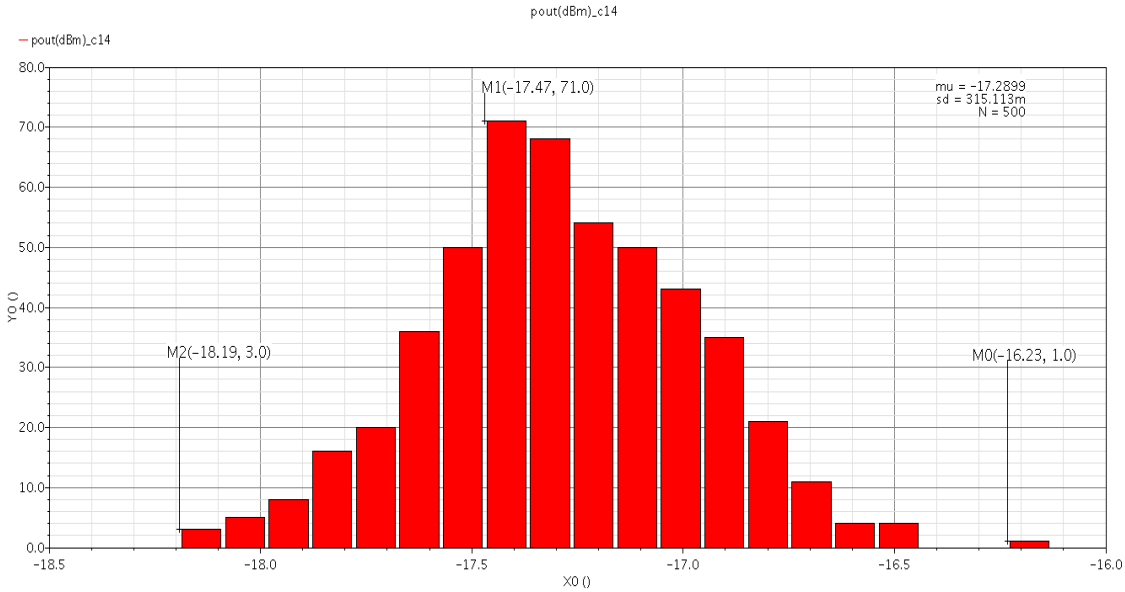

Figure 3.44: high corner results (mean=-17.28dBm)

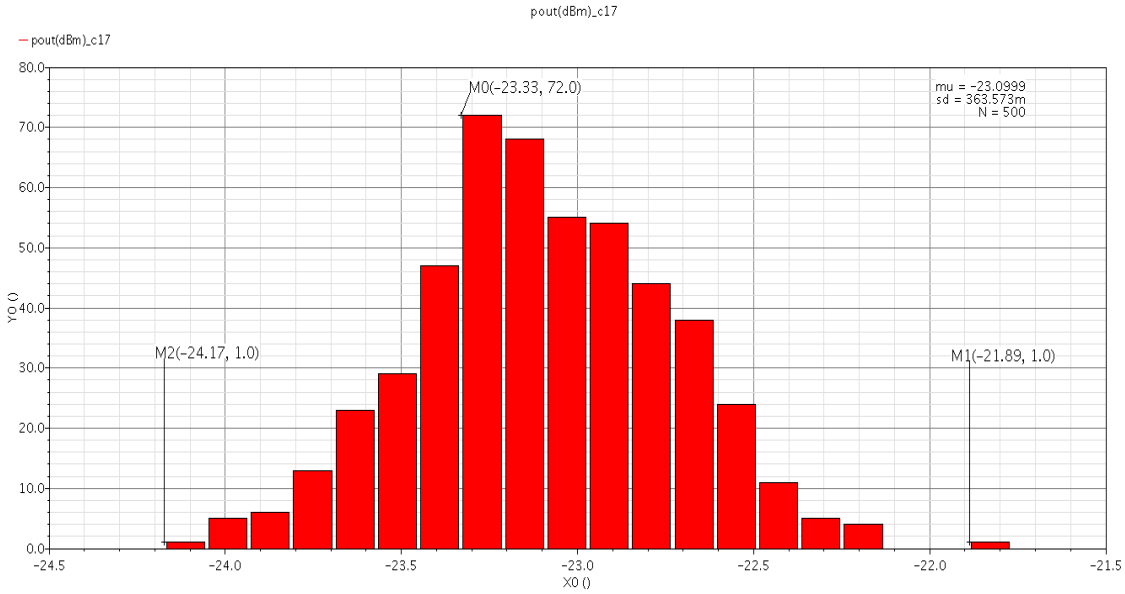

Figure 3.45: low corner results (mean=-23.09dBm)

3.7.3.2 Efficiency

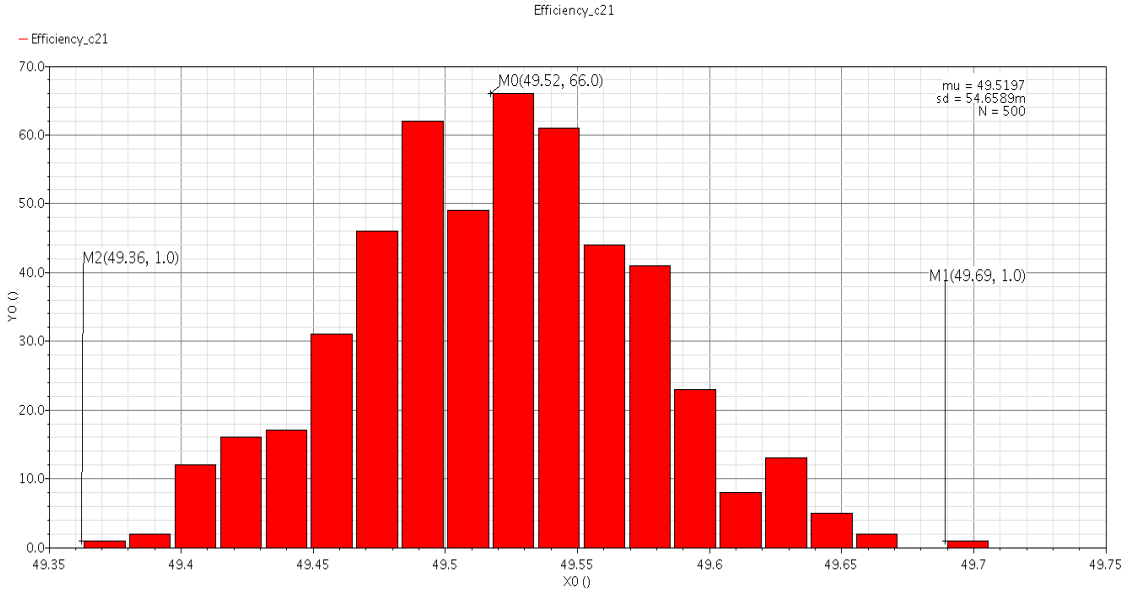

Figure 3.46: efficiency montecarlo results (mean=49.52%)

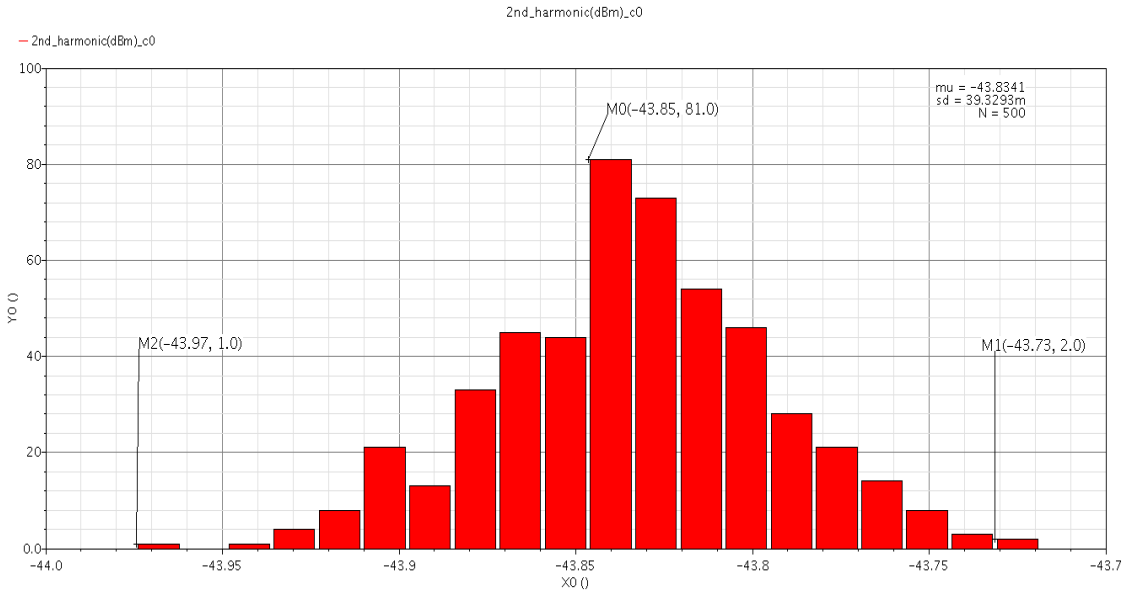

Figure 3.47: second harmonic montecarlo results (mean=-43.83dBm)

3.8 Layout of PA

The Layout of PA was done using TSMC-65nm process kit with a stack consists of 9 metal layers, VDD and GND are chosen to be at top metal layers to improve the parasitic resistances. This layout passed DRC, LVS simulations and a parasitic extraction (PEX) was done for post layout simulation.

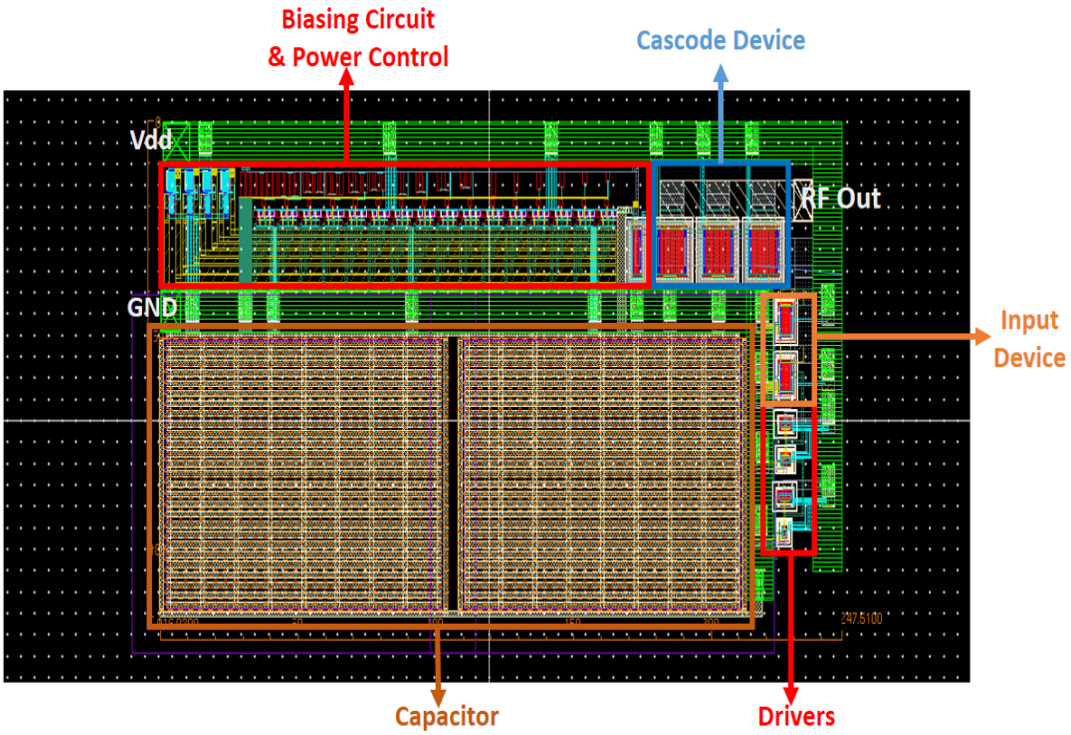

Figure 3.48: layout of PA

Total Area = $247\mu m * 116\mu m = 0.02865mm^2$

3.8.1 Typical Post Layout Simulation Results VS Schematic Results

3.8.1.1 Input Capacitance

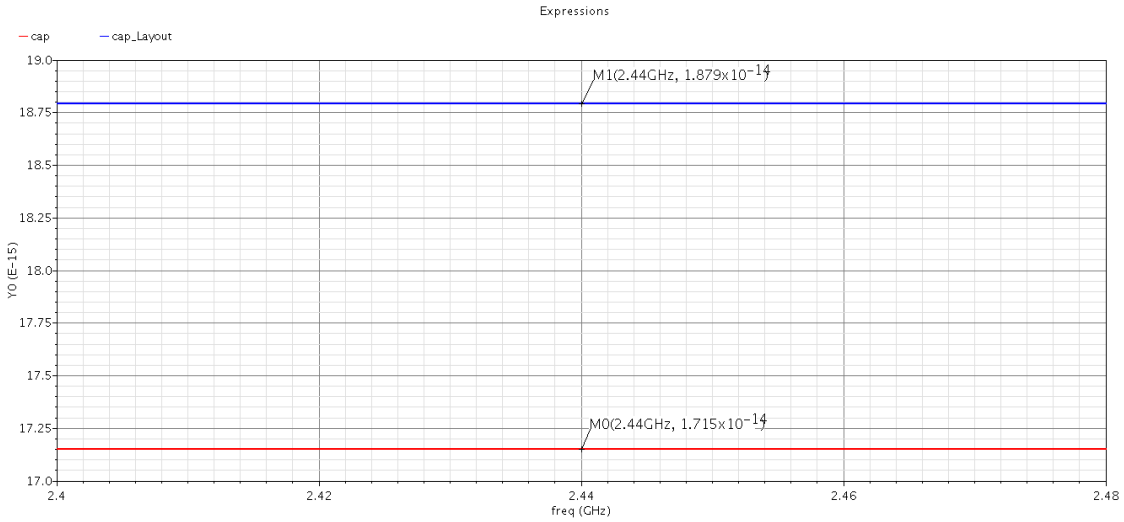

Figure 3.49: input capacitance

3.8.1.2 Power Levels

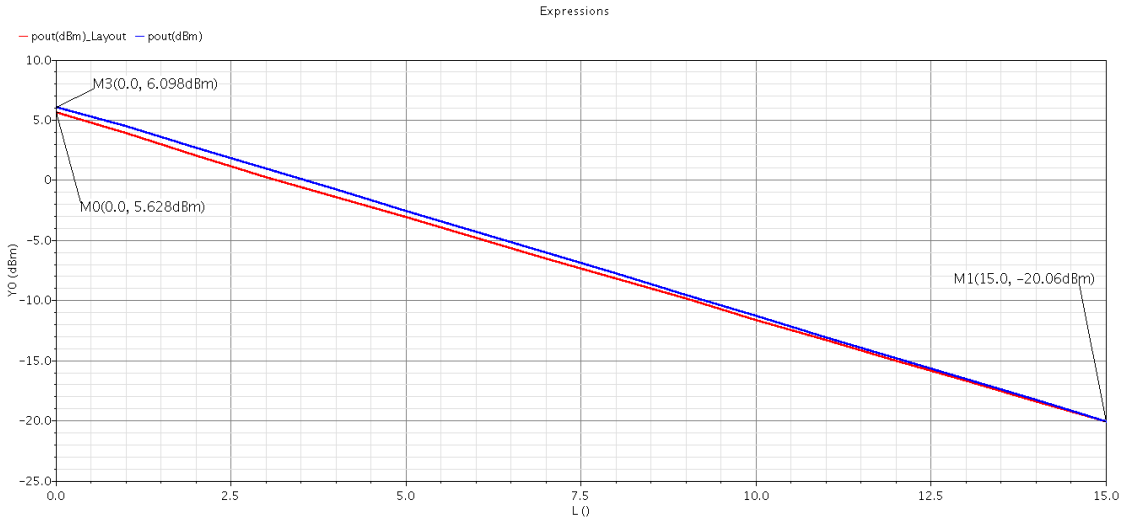

Figure 3.50: output power levels

3.8.1.3 Efficiency

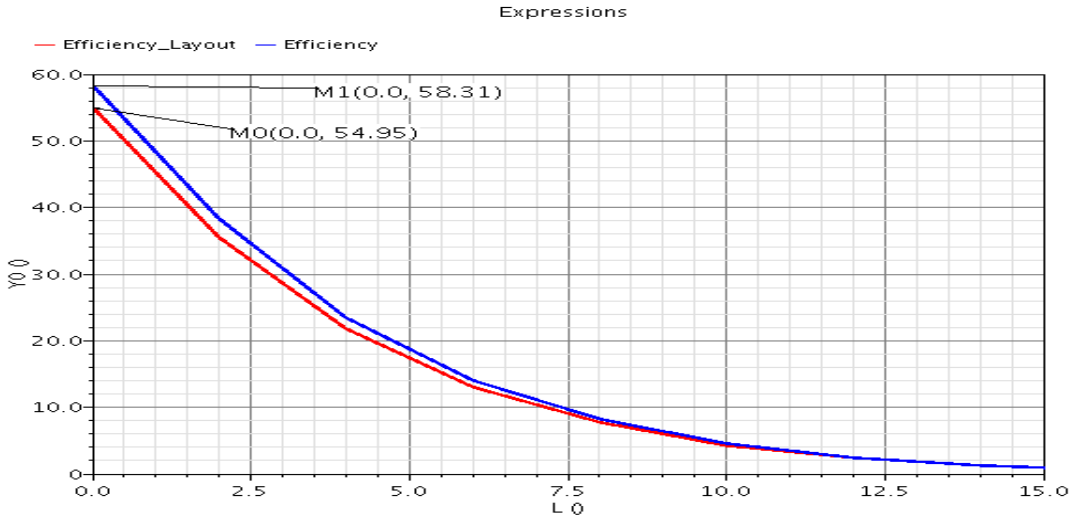

Figure 3.51: efficiency

3.8.1.4 Second Harmonic

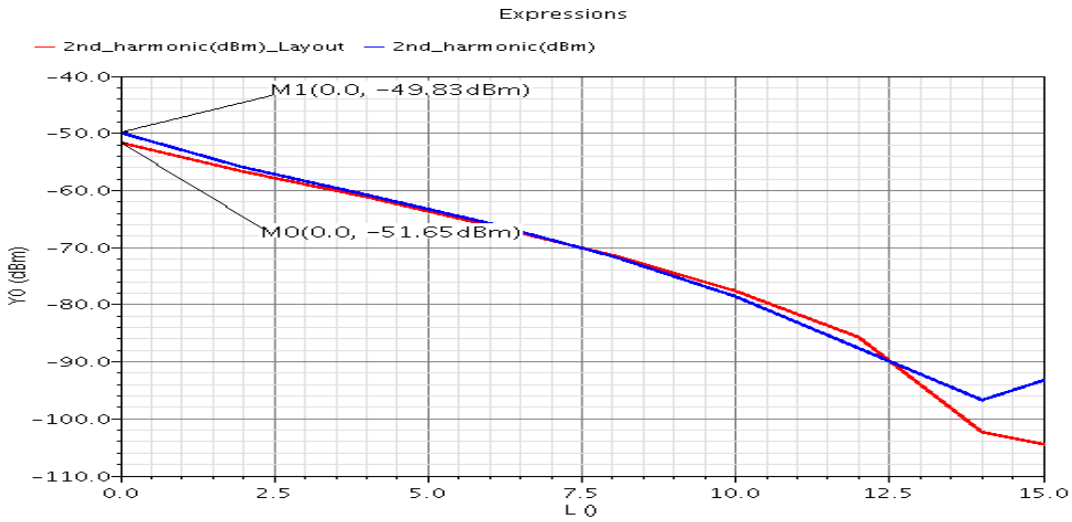

Figure 3.52: second harmonic

3.8.1.5 Third Harmonic

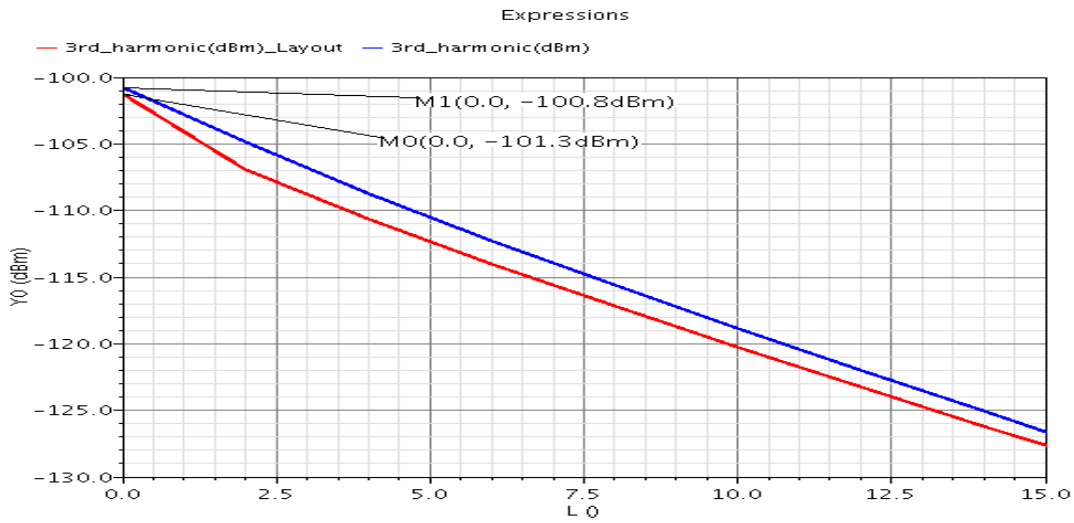

Figure 3.53: Third harmonic

As shown from the post layout simulation results results above, the Layout needs more debugging and optimization to get better results, as the output power has a loss of about .5dB and efficiency degraded by 3% , also the the output of PA has a pad and should be modeled by a shunt capacitor to model the pad(already modeled in the schematic) and series inductor to model the bond wire to the external pin.

3.9 Performance Summary

3.9.1 Typical & Layout Summary

Parameter	Specification	Typical	Layout
Number of L&C Components	$<= 6$ Components	6 Components	6 Components
Input Capacitance	$< 20fF$	$17fF$	$18.8fF$
Output Power	Programmable from -20dBm to 6dBm, step < 2 dB	16 Power Level From -20dBm to 6.1dBm With Step of 1.75 dB	Power Degraded by 0.5dB at High Power Levels
Efficiency	$> 50\%$ at 6dBm	58.3%	55%
Second Harmonic	$< -45dBm$ at all Power Levels	$< -49dBm$	$< -51dBm$
Third Harmonic	$< -45dBm$ at all Power Levels	$< -100dBm$	$< -101dBm$

Table 3.3: Summary of Typical & Layout Simulation Results

3.9.2 Corners Summary

Parameter	**Specification**	**Worst Case Corner**
Deviation of Power at $\text{Level}_0(6.1dBm)$	Within $\pm 2dB$	+1.37dB, -1.88dB
Deviation of Power at $\text{Level}_8(-7.75dBm)$	Within $\pm 3dB$	+2.61dB, -3.3dB
Deviation of Power at $\text{Level}_{15}(-20dBm)$	Within $\pm 3dB$	+2.72dB, -3dB
Efficiency	$> 50\%$ at 6dBm	49.52%
Second Harmonic	$< -45dBm$ at all Power Levels	$< -43.8dBm$
hird Harmonic	$< -45dBm$ at all Power Levels	$< -96dBm$

Table 3.4: Summary of Corners Simulation Results

3.9.3 Monte-Carlo Summary

Parameter	Specification	Max Deviation
Deviation of Power at $\text{Level}_0(6.1dBm)$	Within $\pm 2dB$	+1.4dB, -2dB
Deviation of Power at $\text{Level}_8(-7.75dBm)$	Within $\pm 3dB$	+3.36dB, -3.83dB
Deviation of Power at $\text{Level}_{15}(-20dBm)$	Within $\pm 3dB$	+3.77dB, -4.17dB
Efficiency	$> 50\%$ at 6dBm	49.36%
Second Harmonic	$< -45dBm$ at all Power Levels	$< -43.7dBm$

Table 3.5: Summary of Monte-Carlo Results

3.10 Conclusion

In this chapter, the fundamentals and classes of power amplifiers were discussed and analyzed. A class E power amplifier with digital control was designed and optimized to achieve high efficiency and programmable output power for Bluetooth Low Energy applications (BLE) according to standard version 5.1. The proposed design of PA was implemented and simulated using cadence virtuoso design suit. the proposed design was optimized to meet the given specifications in typical conditions, PVT corners and Monte-carlo(mismatch).The total layout of the on chip components was implemented and optimized to achieve best area and small parasitics, also post layout simulations for typical conditions were presented and compared with schematic results.

3.11 Future Work

Exert more effort in debugging and optimization of layout to get better performance for output power and efficiency.

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Chapter 4: Low-Noise Amplifier

4.1 Introduction

As the first active stage of receivers, LNAs play a critical role in the overall performance. The main function is to amplify the input signal with as minimum as possible added noise to guarantee no degradation in the signal to noise ratio. Also they should achieve high matching with the antenna so, LNAs have different topologies that meet different systems requirements.

4.2 General Considerations

LNAs have many design parameters to achieve certain performance such that low noise figure, high input matching, high current gain and with low power consumption. The following subsections illustrate the main specs of LNAs.

4.2.1 Noise Figure

The noise figure of the LNA directly adds to that of the receiver so, it should be minimized to improve the overall system SNR. NF is defined as the ratio between the input SNR and the output SNR and can be determined from equ. 4.1

$$NF = 1 + \frac{\overline{V_{n,out}^2}}{4KTR_S \cdot A_v^2} \tag{4.1}$$

In RF systems we include only Thermal noise because it is the dominant noise at RF frequencies rather than other types of noise like Flicker noise and this is illustrated in Fig. 4.1

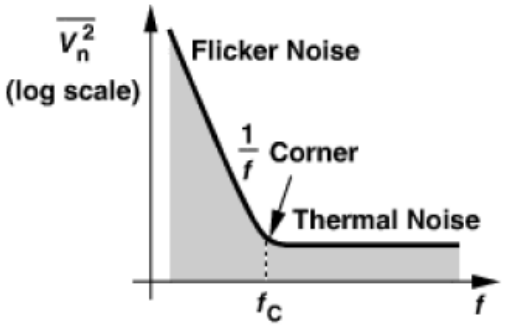

Figure 4.1: Flicker Noise corner frequency

4.2.1.1 Thermal noise of Resistor

the ambient thermal energy leads to random agitation of charge carriers in resistors and hence noise. The noise can be modeled by a series voltage source with a PSD of $\overline{V_n^2} = 4KTR_1$ Thevenin equivalent Fig. 4.2(a) or a parallel current source with a PSD of $\overline{I_n^2} = \frac{4KT}{R_1}$ Norton equivalent Fig. 4.2(b)

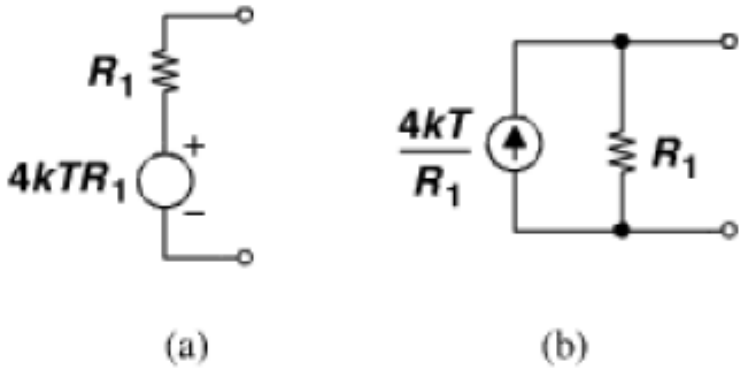

Figure 4.2: (a) Thevenin and (b) Norton models of resistor thermal noise

4.2.1.2 Thermal Noise of MOSFETs

the thermal noise of MOS transistors operating in saturation region is approximated by a current source tied between the source and drain terminals Fig. 4.3(a) and can alternatively be modeled by a voltage source in series with the gate Fig. 4.3(b).

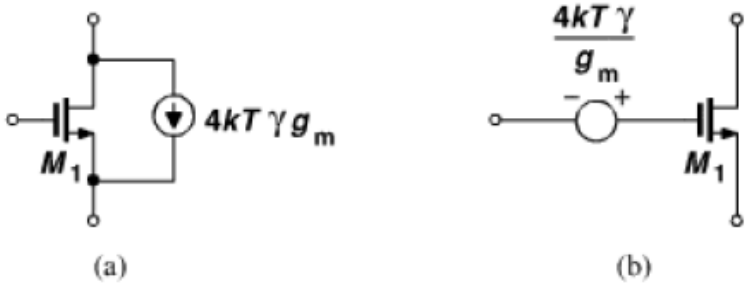

Figure 4.3: Thermal channel noise of a MOSFET modeled as a (a) current source, (b) voltage source

4.2.2 Gain

The gain of the LNA must be large enough to minimize the noise contribution of subsequent stages, specifically, the down-conversion mixer(s) So, the gain can be compromised between low NF and high IIP_3.

4.2.3 Input Return Loss

The interface between the antenna and the LNA entails an interesting issues. Considering the LNA as a voltage amplifier we may expect that its input impedance must ideally be infinite. From the signal power point of view, we may realize conjugate matching between the antenna and the LNA. From noise point of view, we may precede the LNA with a transformation network to obtain minimum NF by obtaining voltage gain from this matching network in the form of equ. 4.2

$$\frac{V_0}{V_{in}} = \sqrt{\frac{R_{in}}{R_S}} \tag{4.2}$$

Where R_{in} is the input resistance seen at the input of the LNA, R_s is the resistance of the antenna. Also this matching network relaxes the matching requirements of the LNA itself. The quality of the input match is expressed by the input "return loss", defined as the reflected power divided by the incident power. For a source impedance of R_s, the return loss is given by equ. 4.3

$$\Gamma = \left| \frac{Z_{in} - R_s}{Z_{in} + R_s} \right| \tag{4.3}$$

4.2.4 Stability

The LNA must interface with the "outside world", specifically, a poorly-controlled source impedance "antenna impedance". For this reason, the LNA must remain stable for all source impedance at all frequencies because if the LNA begins to oscillate at any frequency, it becomes highly nonlinear and its gain is very heavily compressed. A parameter often used to characterize the stability of the circuits is the "Stern stability factor", defined as equ. 4.4

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}|\,|S_{21}|} \tag{4.4}$$

Where $\Delta = S_{11}S_{22} - S_{12}S_{21}$ if K>1 and $\Delta < 1$, then the circuit is unconditionally stable.

4.2.5 Linearity

The linearity in RF systems is usually quantified by two main parameters, IIP_3 and P_{1dB}. Where the first one is a measure of inter- modulation and characterized by a "two-tone" test, and the last one is a measure of the max input power that the LNA can accept before gain compression happens. The LNA doesn't limit the linearity of the receiver. Owing to the cumulative gain through the RX chain, the latter stages tend to limit the overall input IP_3 or P_{1dB}.

4.2.6 Power Consumption

The LNA typically exhibits a direct trade-off among noise, linearity, and power consumption. Nonetheless, in most receiver designs, the LNA consumes only a small fraction of the overall power. In other words, the circuit's noise figure generally proves much more critical than its power dissipation.

4.3 LNA Topologies

To meet the principal targets in the LNA design like noise figure, input matching and gain, LNA has different topologies that is suitable for different systems. Some of these topologies are presented in this section.

Common–Source Stage with	Common–Gate Stage with	Broadband Topologies
▪ Inductive Load	▪ Inductive Load	▪ Noise–Cancelling LNAs
▪ Resistive Feedback	▪ Feedback	▪ Reactance–Cancelling LNAs
▪ Cascode, Inductive Load, Inductive Degeneration	▪ Feedforward	
	▪ Cascode and Inductive Load	

Figure 4.4: Overview of LNA topologies

4.3.1 Common-Gate Stage

The low input impedance of the common-gate stage makes it attractive for LNA design. Considering only a CG circuit with inductive loading Fig. 4.5, Here L_1 resonates with the total capacitance at the output node, R_1 represents the loss of L_1. Neglecting the channel-length modulation and body effect, $R_{in} = \frac{1}{g_m}$. Thus the dimensions and bias current of M_1 are chosen to yield $g_m = \frac{1}{R_S}$.

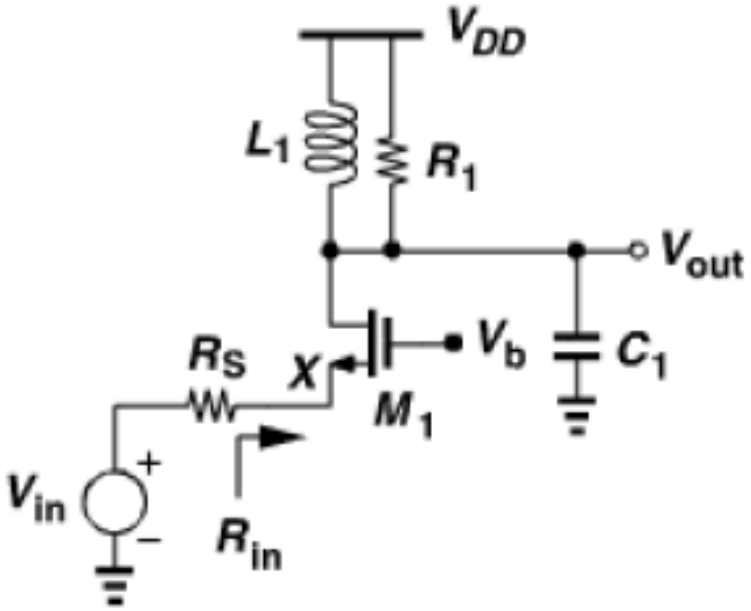

Figure 4.5: Common Gate Stage

The voltage gain is given by equ. 4.5

$$\frac{v_o}{v_{in}} = \frac{R_1}{2R_S} \tag{4.5}$$

The noise figure of the circuit under the condition of input matching "$g_m = \frac{1}{R_S}$"

and at resonance frequency is given by equ. 4.6

$$NF = 1 + \gamma + 4\frac{R_S}{R_1} \tag{4.6}$$

This equation illustrates that the minimum NF that can be achieved "assuming large R_1 compared to 50Ω", is 3dB, this is due to the matching condition.

4.3.2 Common-Source Stage with Resistive Feedback

The feedback common source stage usually used in systems that operates at frequencies an order of magnitude lower than the f_t of the transistor. As shown below in Fig. 4.6, M_2 operates as a current source and R_f senses the voltage and returns a current to the input. This configuration also has input resistance equals to $\frac{1}{g_m}$ because R_f is simply in series with an ideal current source and M_1 appears as a diode-connected device. So, g_{m1} is chosen to achieve the input matching according to equ. 4.7

$$g_{m1} = \frac{1}{R_S} \tag{4.7}$$

The voltage gain is given by equ. 4.8

$$A_v = \frac{1}{2}\left(1 - \frac{R_f}{R_S}\right) \approx -\frac{R_f}{R_S} \tag{4.8}$$

The Noise Figure is given by equ. 4.9

$$NF = 1 + \gamma + 4\frac{R_S}{R_f} + \gamma g_{m2} R_S \tag{4.9}$$

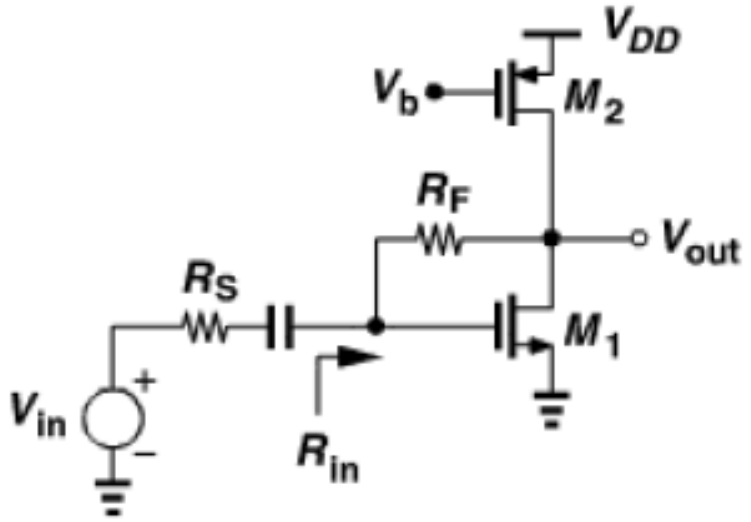

Figure 4.6: Common Source Stage with Resistive Feedback

This topology also has a problem of high NF as it exceeds 3dB.

4.3.3 Common-Source Stage with Inductive Degeneration

In this topology, the 50Ω input resistance is achieved by a CS stage with inductive degeneration, as shown in Fig. 4.7

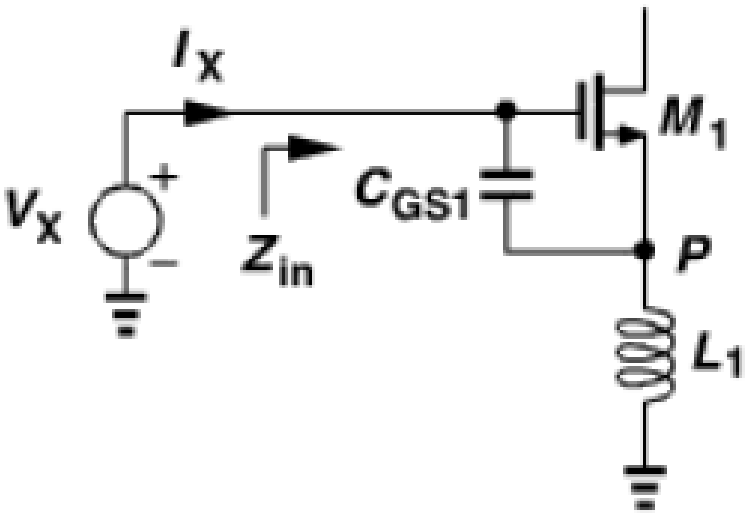

Figure 4.7: Common Source Stage with Inductive Degeneration

The input impedance is given by equ. 4.10

$$Z_{in} = \frac{1}{C_{GS_1} S} + L_1 S + \frac{g_m L_1}{C_{GS_1}} \tag{4.10}$$

This input impedance contains a frequency-independent real part and can be chosen equal to 50Ω. This topology has a trans-conductance gain given by equ. 4.11

$$\left| \frac{I_{out}}{V_{in}} \right| = \frac{1}{\omega_o \left(L_1 + \frac{R_S C_{GS_1}}{g_m} \right)} \tag{4.11}$$

The Noise Figure is given by equ. 4.12

$$NF = 1 + g_m R_S \gamma \left(\frac{\omega_o}{\omega_T} \right)^2 \tag{4.12}$$

This equation is valid under the matching conditions and at resonance frequency. Some of the advantages of this topology is that it has low NF and high gain compared to the above mentioned topologies.

4.3.4 Comparison between different Topologies

Table 4.1 is a comparison between the most useable topologies in the designs.

Parameter	Common Gate	Common Source (ID)
Gain	Moderate gain	Higher Gain
Noise Figure	High NF	Low NF
Matching Bandwidth	Wider in bandwidth	Narrow bandwidth
Stability	Both needs a Cascode device to improve stability	

Table 4.1: Comparison between different Topologies of LNA

4.4 Design of LNA

4.4.1 Required Specifications

The following specs come from BLE standard version 5.1

Parameter	Specification
Trans-Conductance Gain	$> 65.3mA/V$
Noise Figure	$< 3dB$
S_{11}	$< -12dB$
IIP_3	$> -20dBm$
Output Resistance	$> 5K\Omega$
Output Capacitance	$< 20fF$
Current Consumption	$< 1.2mA$

Table 4.2: Specifications of the Proposed LNA

These Specifications should be achieved within the bandwidth of operation "From 2.4GHz up to 2.48GHz", also the design should guarantee proper operation across all corners and under mismatch conditions.

4.4.2 Number of Stages and Topology Selection

The proposed LNA was designed and simulated using Cadence Virtuoso with TSMC 65nm process technology. The LNA Consists of two stages, the first one was chosen to be "Common Source with Inductive degeneration" based on the comparison mentioned above, and the second stage should be voltage to current converter to achieve the current mode function of the receiver and was chosen to be "Stacked Inverter-Based Amplifier" due to its high gain and high output resistance.

4.4.2.1 First Stage Design Procedure

This Stage Fig. 4.8 is directly Connected to the antenna so, the input matching is mainly determined from the input of this stage. In normal designs of this topology, the matching is achieved from the Amplifier only which limits its performance because it needs certain g_m,C_{GS} and degenerated inductor which makes the design parameters limited to a certain values so, a matching network was preceded this stage to relax the constrains on the amplifier and also with its voltage gain equ. 4.2 it is greatly improves the noise figure and slightly affecting the IIP_3 so, a LC matching network used and its inductor was off chip for the high quality factor required for matching and to compensate the effect of the DC blocking capacitor at the input, the off chip inductor was selected from MURATA MANUFACTURING CO. and simulated using ADS. The g_m of the input transistor was optimized to compromise between the voltage gain of this stage, the noise figure and its IIP_3. A cascode device used to improve the stability of the LNA by separating its output from its input to prevent positive feedback, the sizing of this transistor was optimized for low parasitic capacitance. The output of this

stage is connected to a parallel LC tank which resonates at the required band of operation, this LC tank improves the headroom of the first stage and also relax the IIP_3 requirements on the next stages. the spiral inductor was optimized between its area and quality factor which determines the output impedance of this stage.

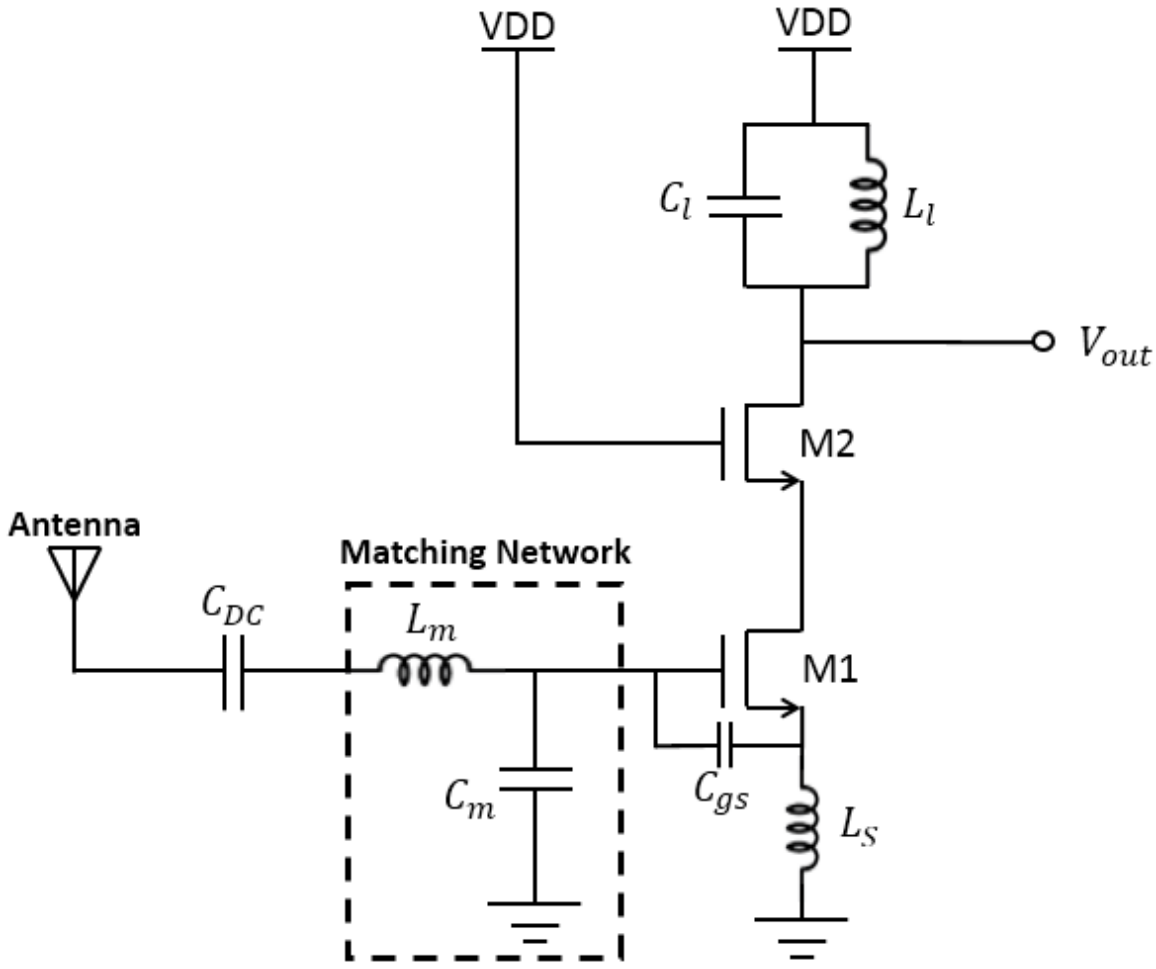

Figure 4.8: First Stage of the Proposed LNA

4.4.2.2 Second Stage Design Procedure

The second stage is mainly a voltage to current converter to deliver the output current to the mixer, and it was chosen to be "Stacked Inverter-Based Amplifier" Fig. 4.9, Inverter-Based amplifier because it gives almost double

g_m with the same current using current reuse technique (PMOS and NMOS), and was stacked to achieve high output resistance. the sizing of the main transistors was optimized for high gain and high IIP_3, the cascode devices were sized such that the headroom of the main devices is large enough the improve the IIP_3, and were optimized for high output resistance and low output capacitance. The problem of this topology is that it has high impedance output node which needs to be set to a certain voltage level so, a common mode feedback circuit was used to set the voltage of the output node to an optimum value which was chosen to be $\frac{V_{DD}}{2}$.

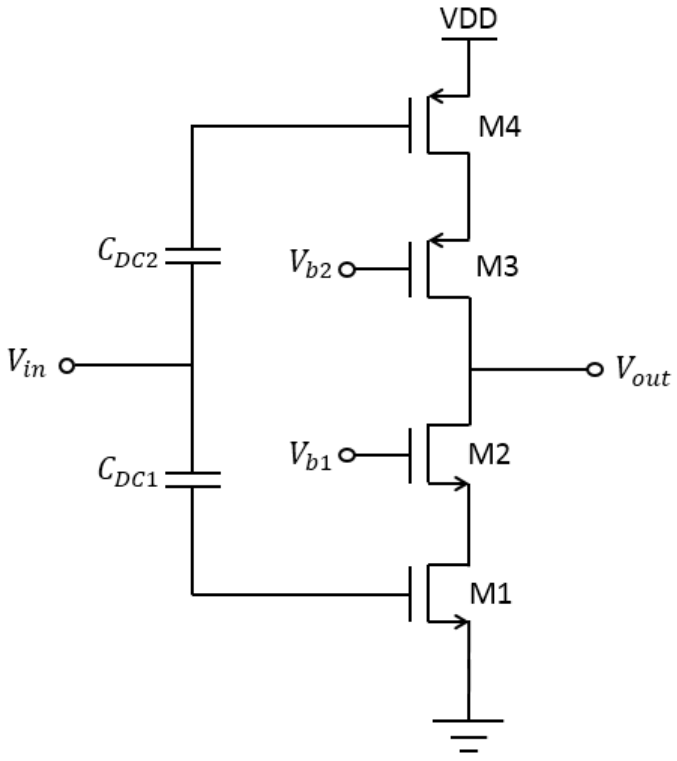

Figure 4.9: Stacked Inverter Based Amplifier as a Second Stage

4.4.2.3 Common Mode Feedback Design Procedure

The CMFB was simply 5T OTA to set the output voltage of the output node of the second stage, the output of this circuit used to bias the PMOS

transistor M_4 in Fig. 4.10, and the sizing of the transistors was optimized to improve the phase margin of the loop and it was designed to consume very low Current.

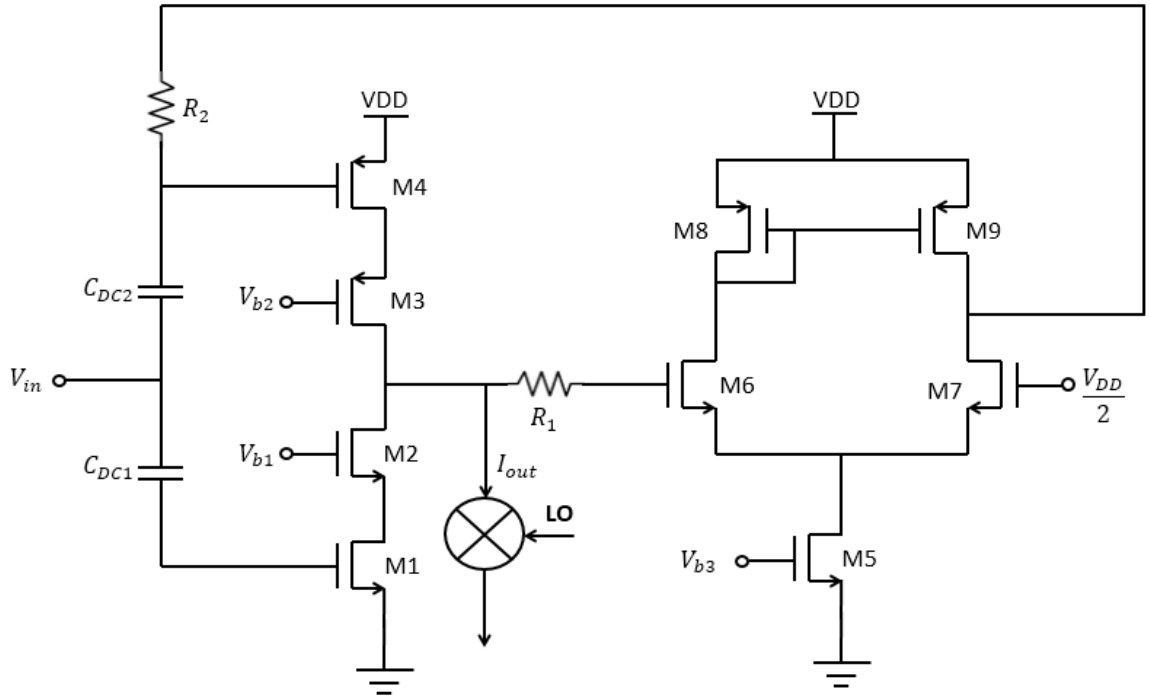

Figure 4.10: Second Stage with CMFB Circuit

Fig. 4.11 shows the top-level schematic of the Proposed LNA.

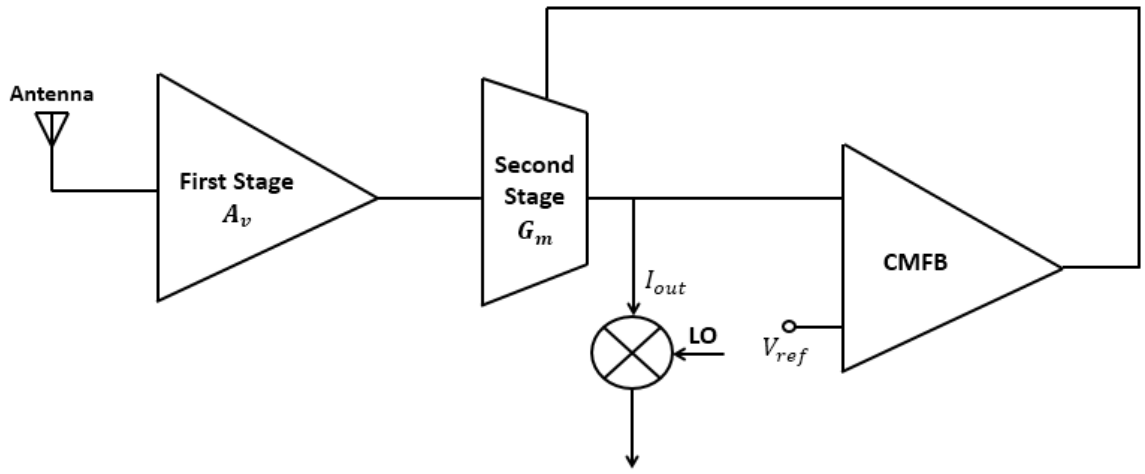

Figure 4.11: Top-Level Schematic of the Proposed LNA

4.4.3 Typical Simulation Results of the proposed LNA

The proposed LNA was designed and optimized to meet the different specifications with enough margin to guarantee proper performance across corners and mismatch, also the input of the LNA was a Port with 50Ω resistance to model the antenna impedance, the AC magnitude was set to be one.

4.4.3.1 Trans-Conductance Gain

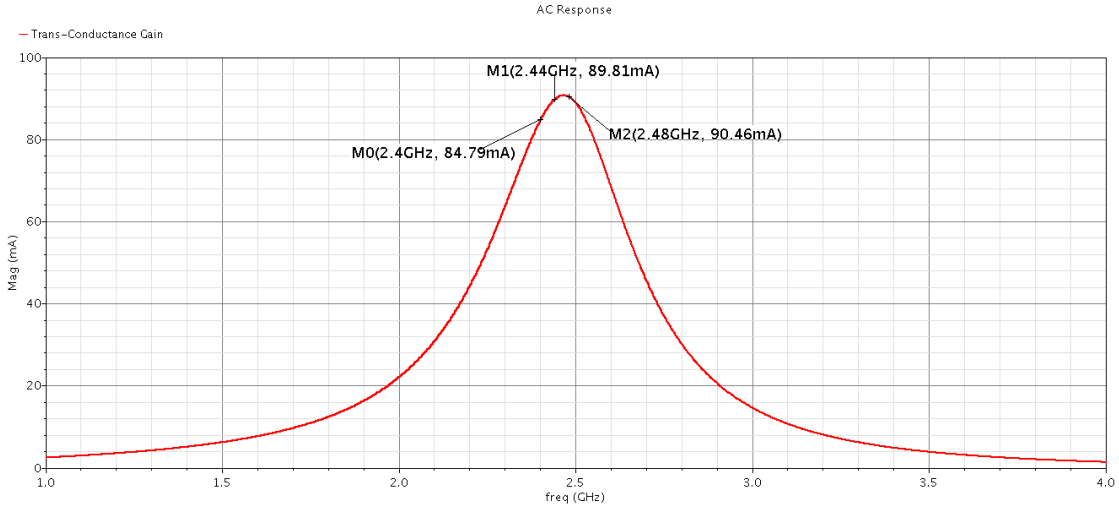

Figure 4.12: Trans-Conductance Gain of the Proposed LNA

4.4.3.2 Noise Figure

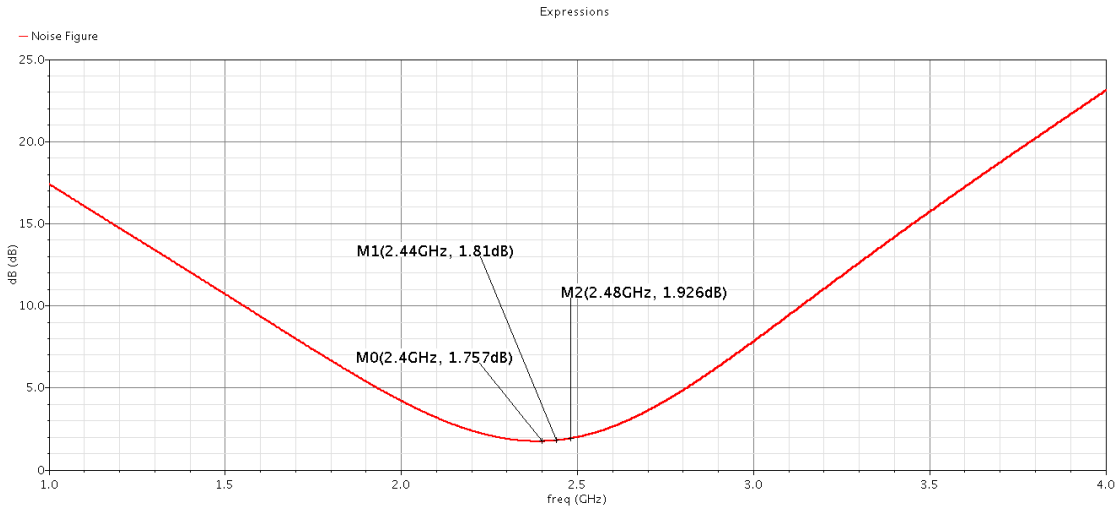

Figure 4.13: Noise Figure of the Proposed LNA

4.4.3.3 Input Matching

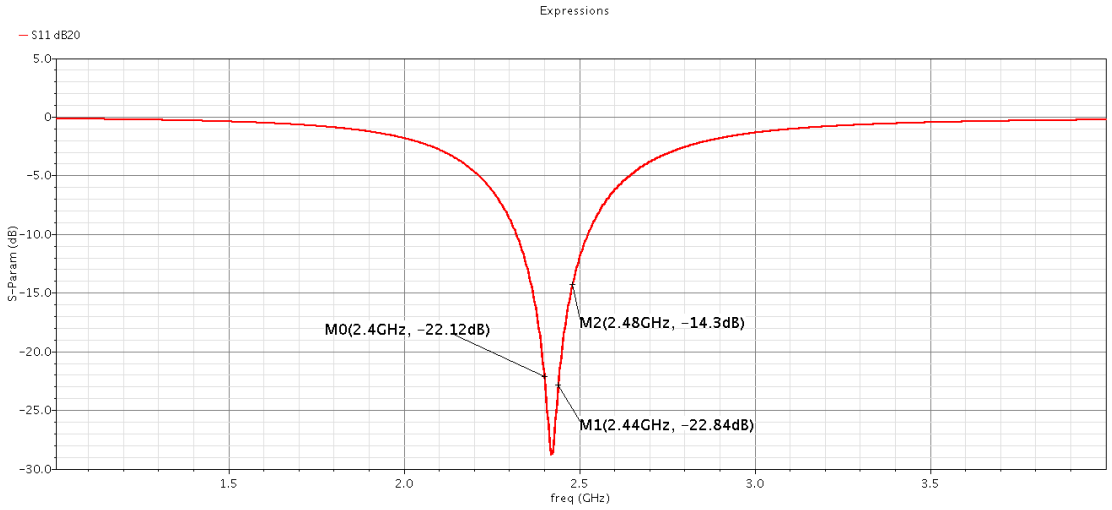

Figure 4.14: Input Matching of the Proposed LNA

4.4.3.4 IIP_3 and P_{1dB}

IIP_3 was simulated using two tones test, The frequency of the two blockers was 2.434GHz and 2.437GHz and their amplitudes were -32dBm, the two blockers produce two IM_3 components at 2.431GHz and 2.44GHz, which were calculated from $2f_1 - f_2$ and $2f_2 - f_1$ respectively.

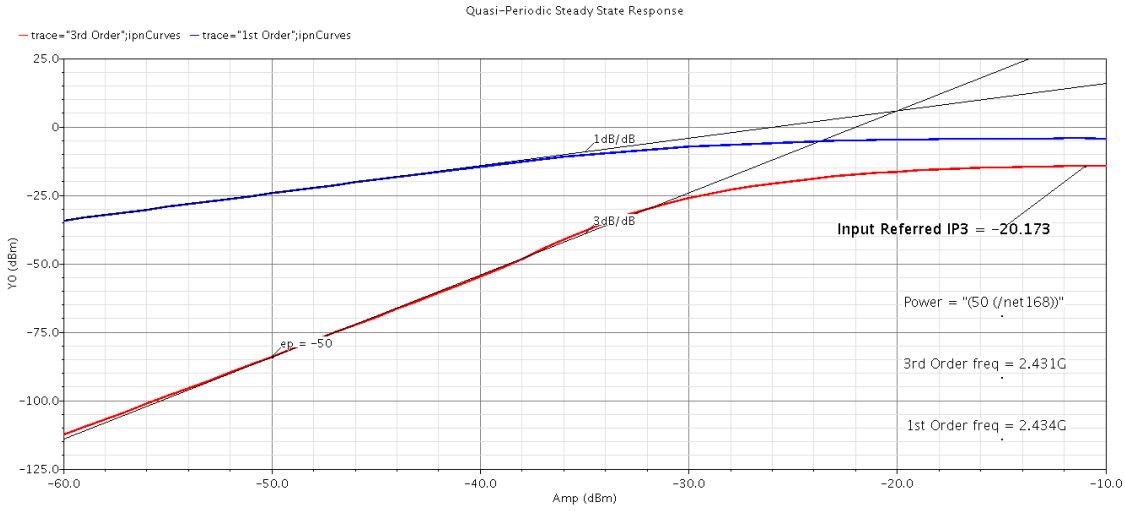

Figure 4.15: IIP_3 of the Proposed LNA

IIP_3 can also be calculated from the power spectral of the output from equ. 4.13. Fig. 4.16 shows the amplitudes of the two tones and their IM_3 components.

$$IIP_3 = \frac{P_{out} - P_{IM_3} + 2P_{in}}{2} \tag{4.13}$$

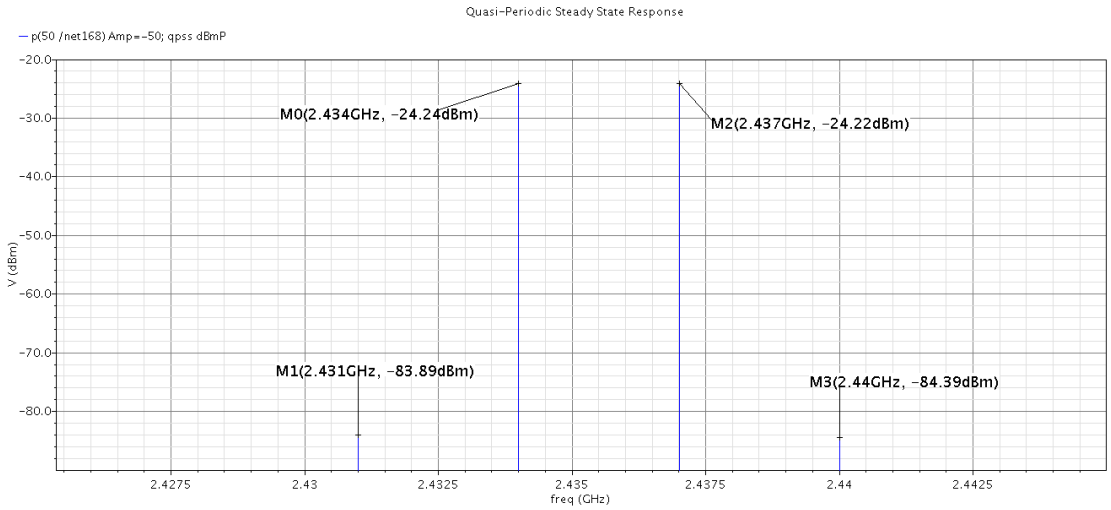

Figure 4.16: Output Power Spectral

P_{1dB} was simulated using single tone test at the center frequency (i.e. 2.44GHz), the amplitude of this tone was swept till the gain is compressed by 1dB. As a rule of thumb, P_1dB is 10dB below IIP_3.

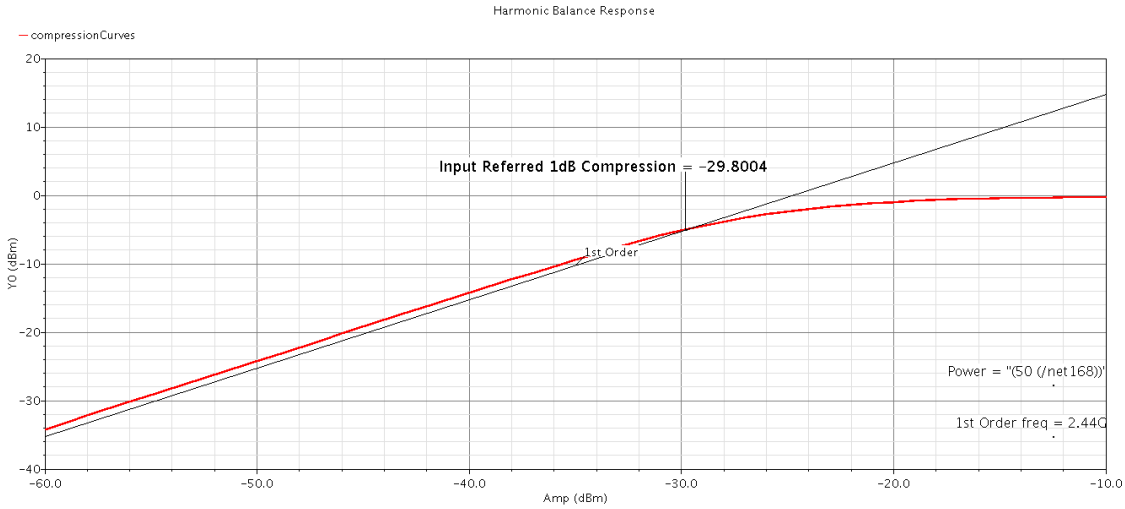

Figure 4.17: 1dB Compression Point of the Proposed LNA

4.4.3.5 Output Resistance

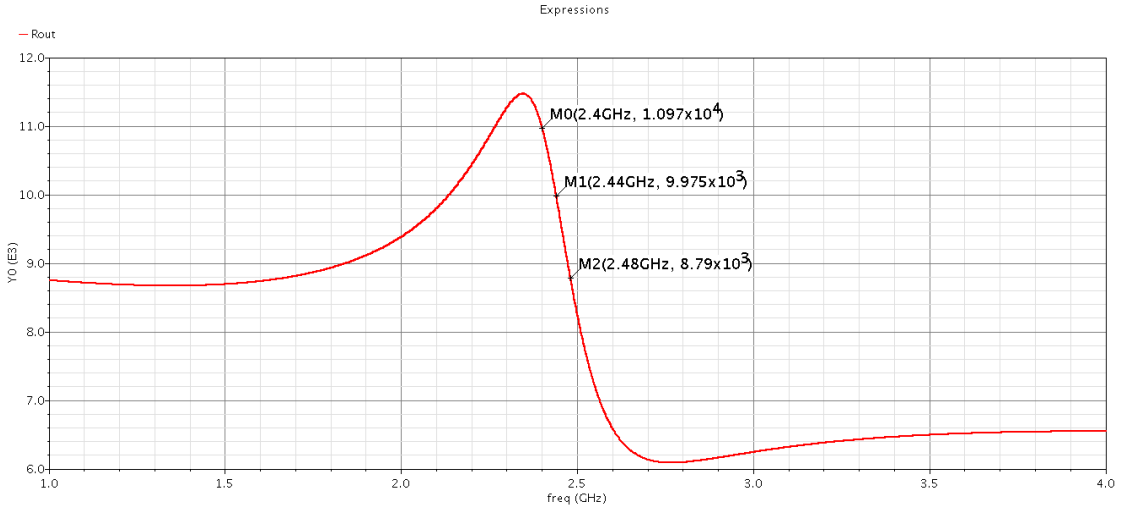

Figure 4.18: Output Resistance of the Proposed LNA

4.4.3.6 Output Capacitance

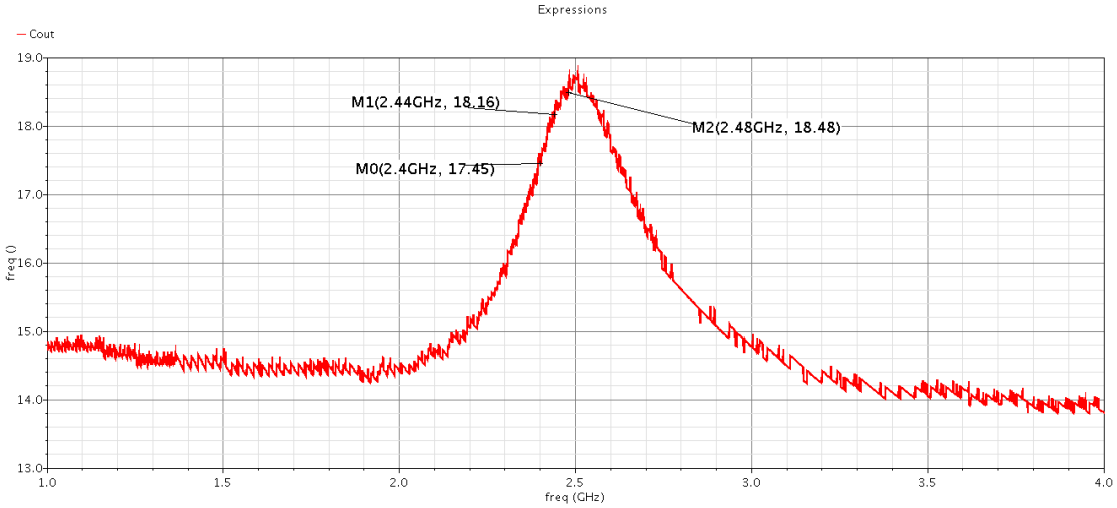

Figure 4.19: Output Capacitance of the Proposed LNA

4.4.3.7 Current Consumption

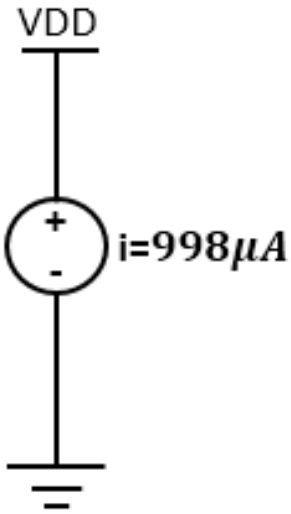

Figure 4.20: Current Consumption the Proposed LNA

4.4.3.8 CMFB Stability

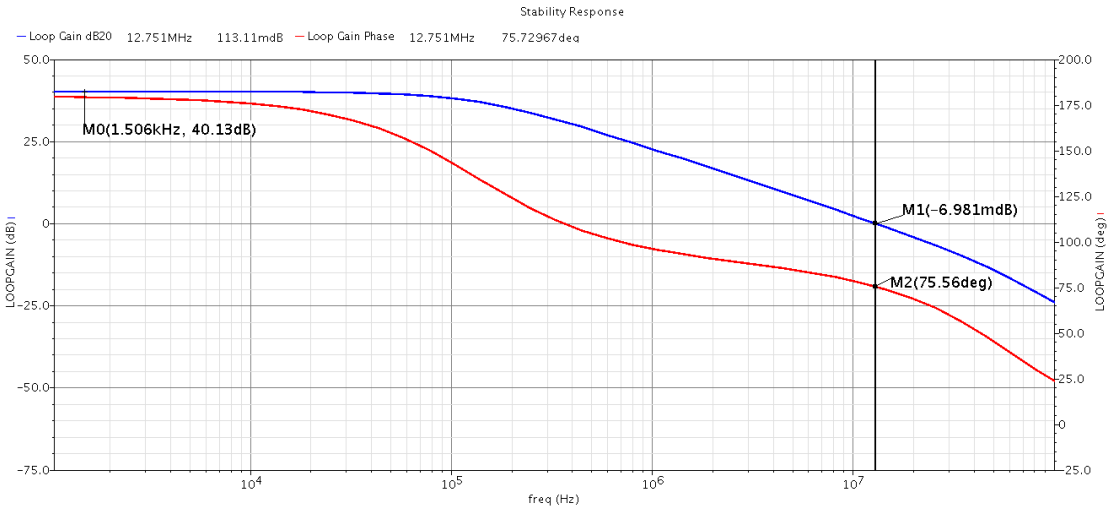

Figure 4.21: Phase Margin of the CMFB

4.4.3.9 Summary of Typical Simulation Results

Parameter	**Specification**	**Achieved**
Trans-Conductance Gain	$> 65.3mA/V$	$90mA/V$
Noise Figure	$< 3dB$	$1.81dB$
S_{11}	$< -12dB$	$-23dB$
IIP_3	$> -20dBm$	$-20.17dBm$
P_{1dB}	$> -30dBm$	$-30dBm$
Output Resistance	$> 5K\Omega$	$9.975K\Omega$
Output Capacitance	$< 20fF$	$18.2fF$
Current Consumption	$< 1.2mA$	$998\mu A$
Phase Margin	$> 60^\circ$	75.5°

Table 4.3: Summary of Typical Simulation Results @ 2.44GHz

4.4.4 Techniques to Improve the Performance across Corners

4.4.4.1 Different Combination of Corners under which the LNA was tested

128 different corners were simulated according to table 4.4. the off chip inductor was excluded from the corners simulation because its variation is negligible compared to on chip components.

Variation	**Corners**
Temperature	$\{-40^oC, 125^oC\}$
Supply	$\{950mV, 1.05V\}$
Transistors	$\{FF, SS, FS, SF\}$
Resistors	$\{FF, SS\}$
Capacitors	$\{FF, SS\}$
Spiral Inductors	$\{FF, SS\}$

Table 4.4: Simulated PVT Corners

4.4.4.2 Capacitor Bank Solution

The variations of the capacitors across corners are found to be very large, and these variations cause shifting in response of both gain and S11, which make the band of operation if far from the required band as shown in Fig. 4.22, and Fig. 4.23

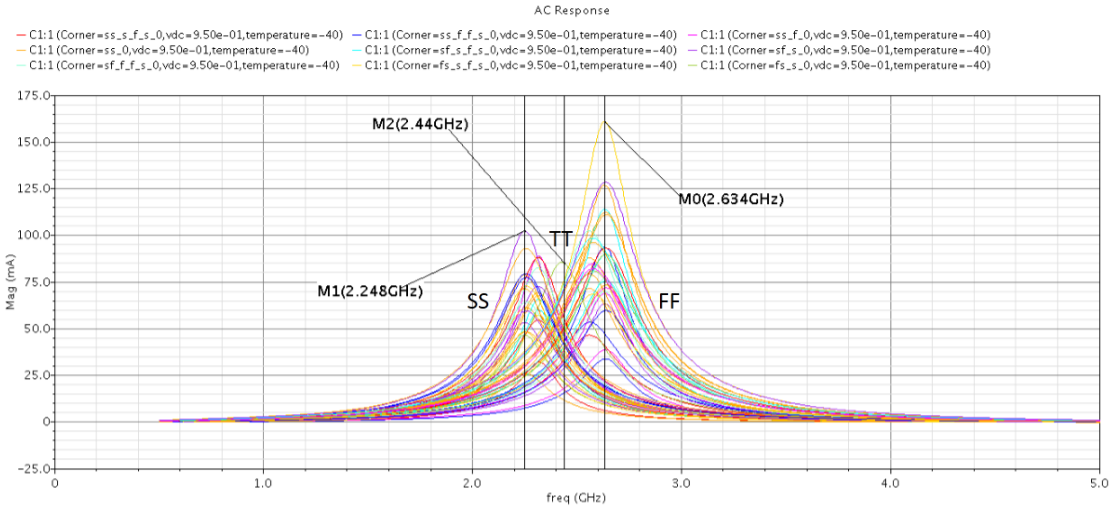

Figure 4.22: Gain Shifting due to Capacitors Variation

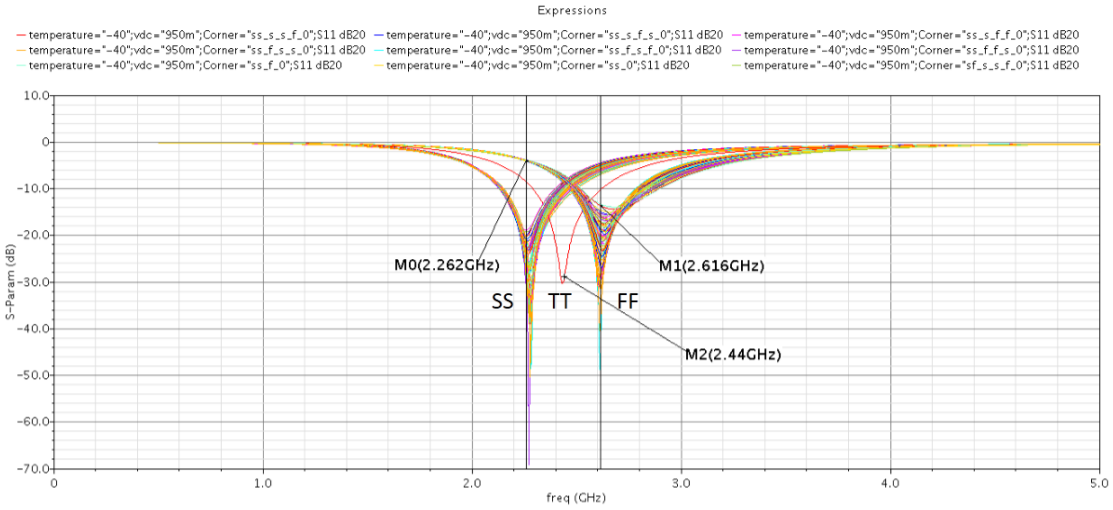

Figure 4.23: S11 Shifting due to Capacitors Variation

So, a digitally controlled capacitor bank was presented Fig. 4.24, the Cap.Bank should be controlled by a process-monitor circuit, the sizes of

the switches have a big trade-off between R_{on} and R_{off}, C_{off}.

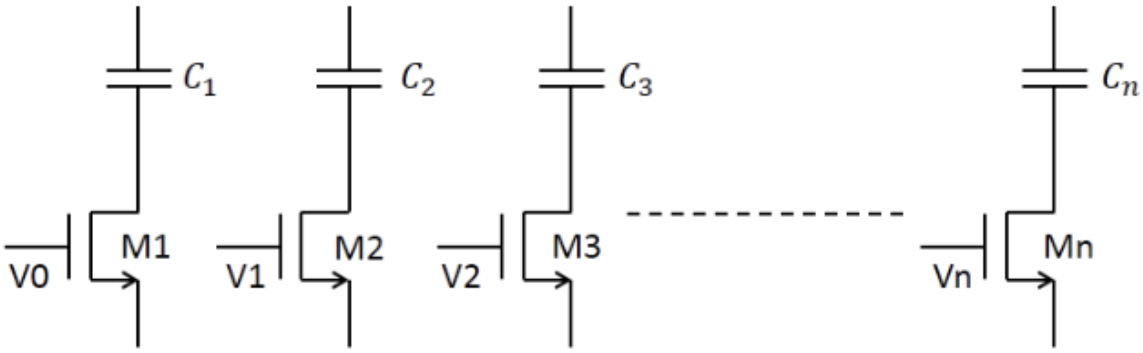

Figure 4.24: Capacitor Bank used for Matching and Gain

4.4.4.3 Mixing between PTAT and POLY Biasing Currents

The main idea is to get the advantages from each type to get the best current behavior across corners, Fig. 4.25 shows the behavior of each current type and the mixing one with Temperature for different resistance corners.

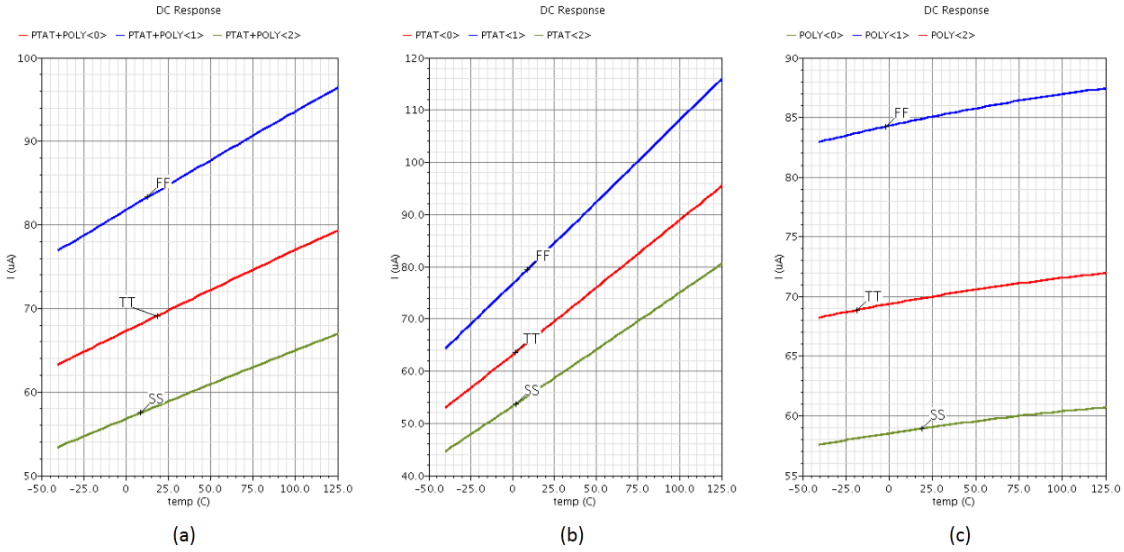

Figure 4.25: (a) PTAT+POLY current, (b) PTAT Current, (c) POLY Current

so, after optimization to get the best current behavior across corners, the biasing current was consisted of 68% POLY current and 32% PTAT current.

4.4.5 Corner Simulation Results of the Proposed LNA

In this subsection, the results of the proposed LNA were presented across Corners, due to large number of corners (128), only some curves were plotted include the worst and the best cases, followed by a Summary of the results.

4.4.5.1 Trans-Conductance Gain across Corners

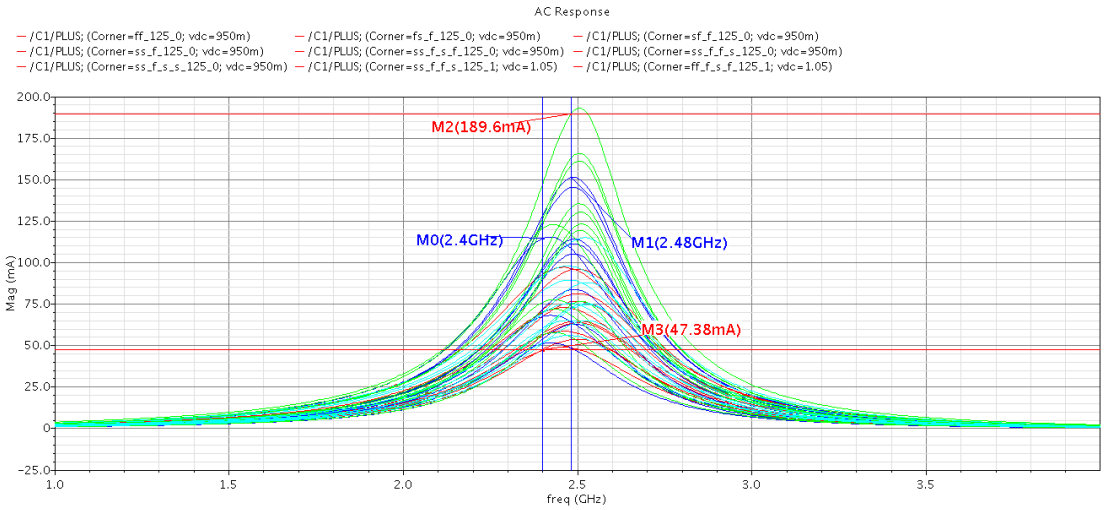

Figure 4.26: Trans-Conductance Gain across Corners

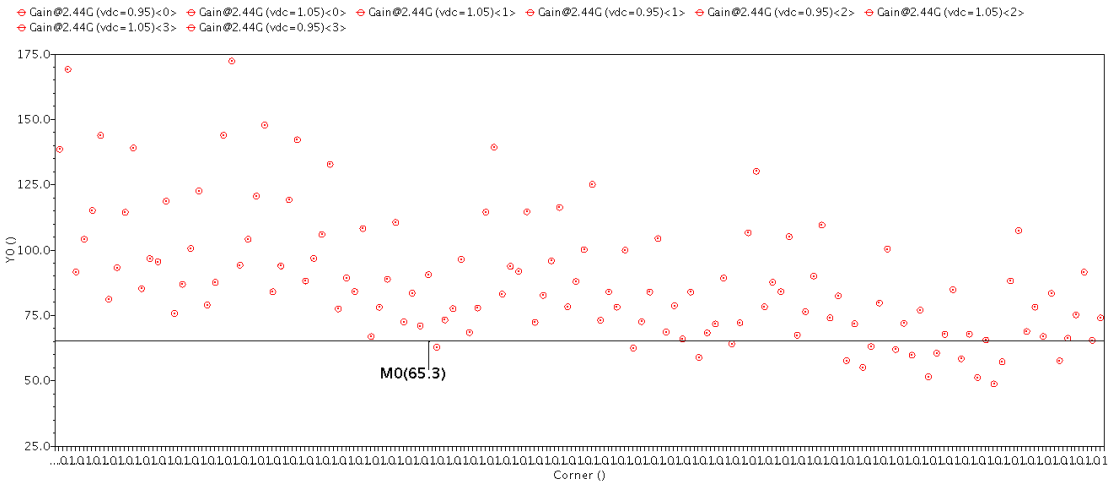

Figure 4.27: Trans-Conductance Gain across Corners @2.44GHz

The common factors between failed corners were: SS-MOSFETs, SS-Resistance, Low-Supply, Cap.Bank with open Switches.

Summary:

Parameter	**Min**	**Max**	**Mean**
G_m@2.4GHz	$47mA/V$	$152mA/V$	$83mA/V$
G_m@2.44GHz	$49mA/V$	$173mA/V$	$89mA/V$
G_m@2.48GHz	$49mA/V$	$190mA/V$	$92mA/V$

Table 4.5: Summary of G_m across Corners

4.4.5.2 Noise Figure across Corners

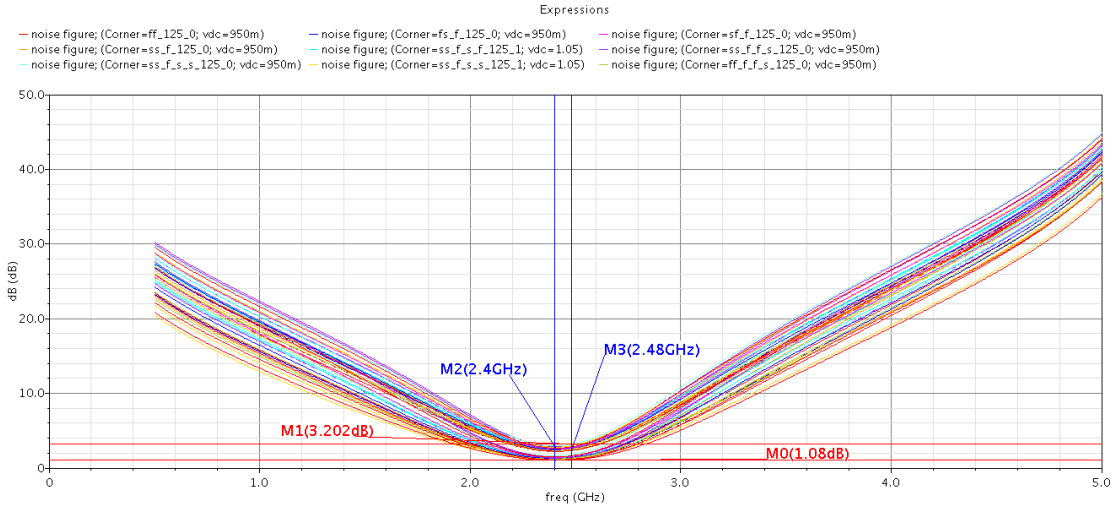

Figure 4.28: Noise Figure across Corners

Summary:

Parameter	Min	Max	Mean
NF@2.4GHz	1.08dB	3dB	1.91dB
NF@2.44GHz	1.094dB	3.05dB	1.94dB
NF@2.48GHz	1.147dB	3.2dB	2.03dB

Table 4.6: Summary of Noise Figure across Corners

4.4.5.3 Input Matching across Corners

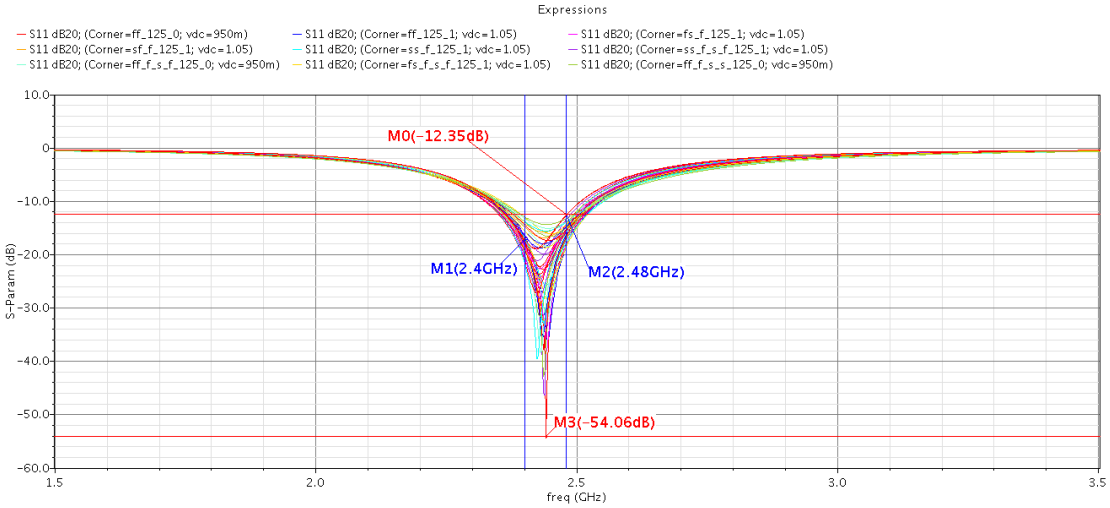

Figure 4.29: Input Matching across Corners

Summary:

Parameter	Min	Max	Mean
S_{11}@2.4GHz	$-21dB$	$-12.4dB$	-17dB
S_{11}@2.44GHz	$-49dB$	$-13.8dB$	$-24dB$
S_{11}@2.48GHz	$-18.5dB$	$-12.4dB$	$-15dB$

Table 4.7: Summary of Input Matching across Corners

4.4.5.4 IIP_3 and P_{1dB} across Corners

As shown above from typical simulation results, the IIP_3 is equal to the required value without any margins so, it was expected to decrease across corners, thus this Spec. is hardly achieved in corners simulation and the LNA was optimized to get the best value across corners.

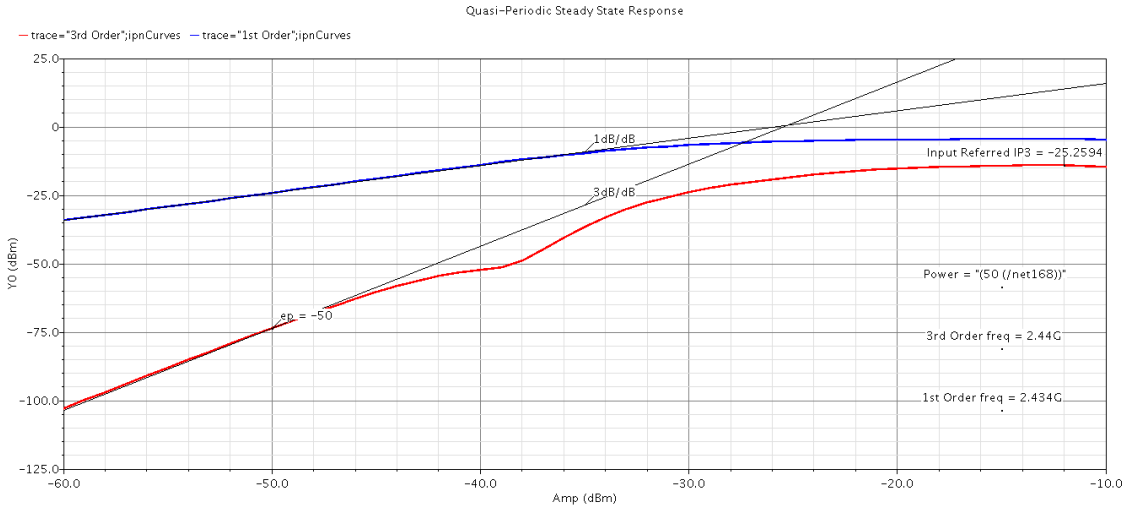

Figure 4.30: Worst Case IIP_3

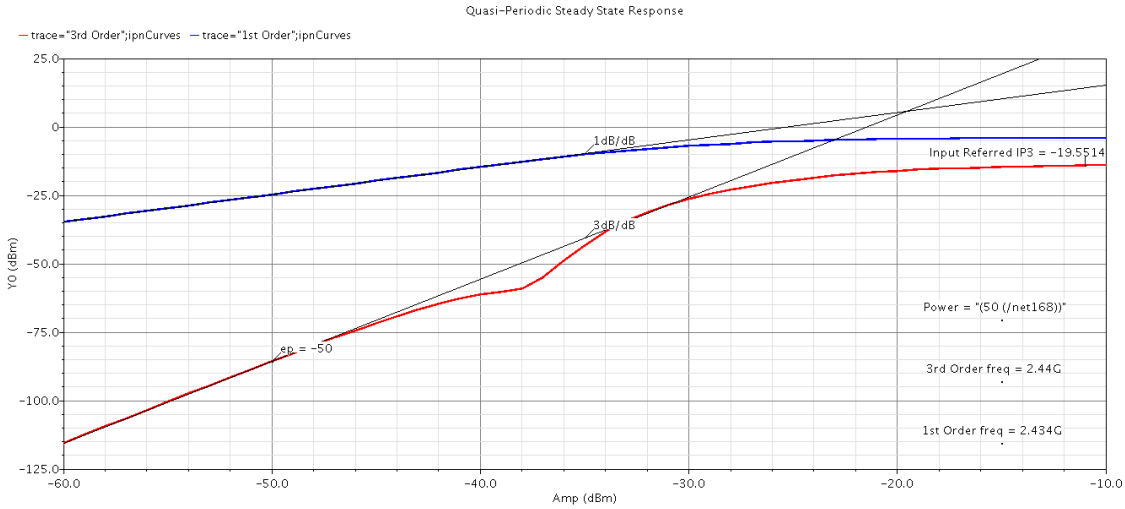

Figure 4.31: Best Case IIP_3

Summary:

Parameter	**Min**	**Max**	**Mean**
IIP_3	$-25.22dBm$	$-19.56dBm$	$-22dBm$
P_{1dB}	$-33dBm$	$-23dBm$	$-30dBm$

Table 4.8: Summary of IIP_3 and P_{1dB} across Corners

4.4.5.5 Output Resistance across Corners

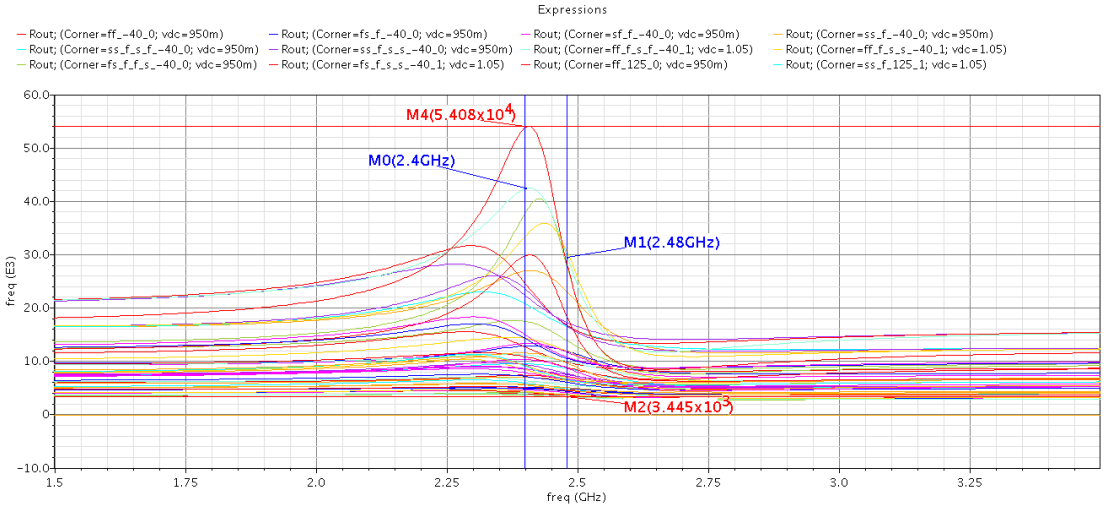

Figure 4.32: Output Resistance across Corners

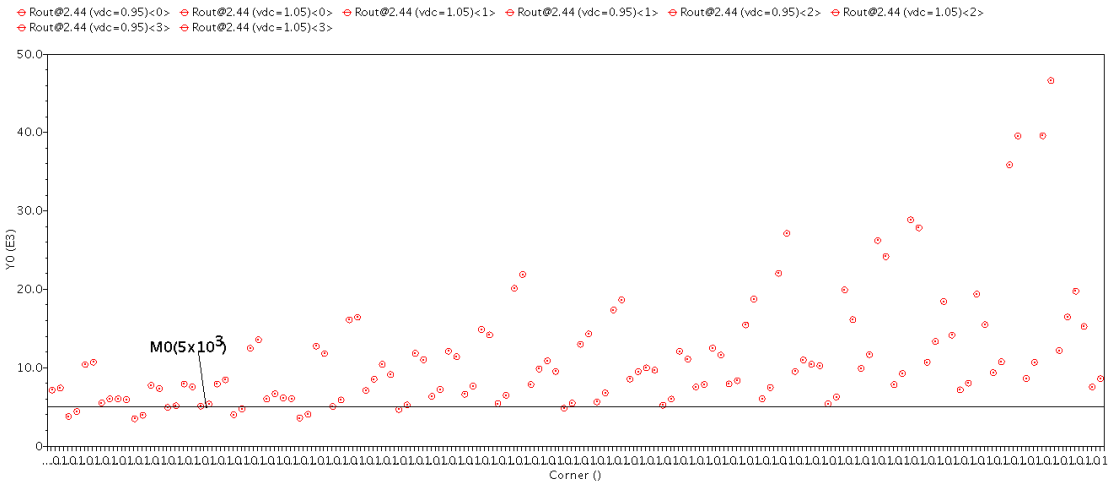

Figure 4.33: Output Resistance across Corners @2.44GHz

The common factors between failed corners were: FF-MOSFETs, FF-Resistance, Low-Supply, high-Temp.

Summary:

Parameter	Min	Max	Mean
R_{out}@2.4GHz	$3.88K\Omega$	$54K\Omega$	$12.4K\Omega$
R_{out}@2.44GHz	$3.6K\Omega$	$46.7K\Omega$	$11.4K\Omega$
R_{out}@2.48GHz	$3.44K\Omega$	$30.5K\Omega$	$9.76K\Omega$

Table 4.9: Summary of Output Resistance across Corners

4.4.5.6 Output Capacitance across Corners

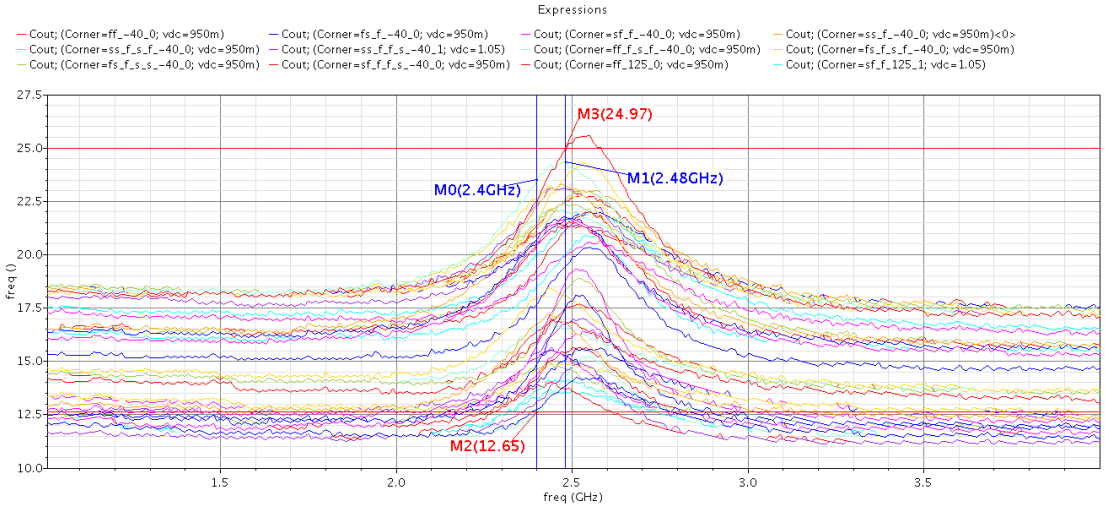

Figure 4.34: Output Capacitance across Corners

Summary:

Parameter	Min	Max	Mean
C_{out}@2.4GHz	$12.65fF$	$23.5fF$	$18fF$
C_{out}@2.44GHz	$13.44fF$	$24.3fF$	$18.6fF$
C_{out}@2.48GHz	$13.34fF$	$25fF$	$19fF$

Table 4.10: Summary of Output Capacitance across Corners

4.4.5.7 Current Consumption and Phase Margin across Corners

Parameter	Min	Max	Mean
I	$560\mu A$	$1.72mA$	$1.05mA$
PM	44.5°	88.5°	$74.5\circ$

Table 4.11: Summary of Current Consumption and PM across Corners

4.4.5.8 Summary of Specs In Typical, Worst and Best Corner @ 2.44GHz

Parameter	Spec	Typical	W.Corner	B.Corner
Gain	$> 65.3mA/V$	$90mA/V$	$49mA/V$	$173mA/V$
NF	$< 3dB$	$1.81dB$	$3.05dB$	$1.094dB$
S_{11}	$< -12dB$	$-23dB$	$-13.8dB$	$-49dB$
IIP_3	$> -20dBm$	$-20dBm$	$-25.22dBm$	$-19.56dBm$
P_{1dB}	$> -30dBm$	$-30dBm$	$-33dBm$	$-23mdB$
R_{out}	$> 5K\Omega$	$9.975K\Omega$	$3.6K\Omega$	$46.7K\Omega$
C_{out}	$< 20fF$	$18.2fF$	$24.3fF$	$13.44fF$
Current	$< 1.2mA$	$998\mu A$	$1.72mA$	$560\mu A$
PM	$> 60^\circ$	75.5°	44.5°	88.5°

Table 4.12: Summary of Specs In Typical, Worst and Best Corner @ 2.44GHz

4.4.6 Monte Carlo Mismatch Simulation Results

A Monte Carlo Mismatch simulation was performed at typical conditions with total number of runs equal 1500 run.

4.4.6.1 Trans-Conductance Gain

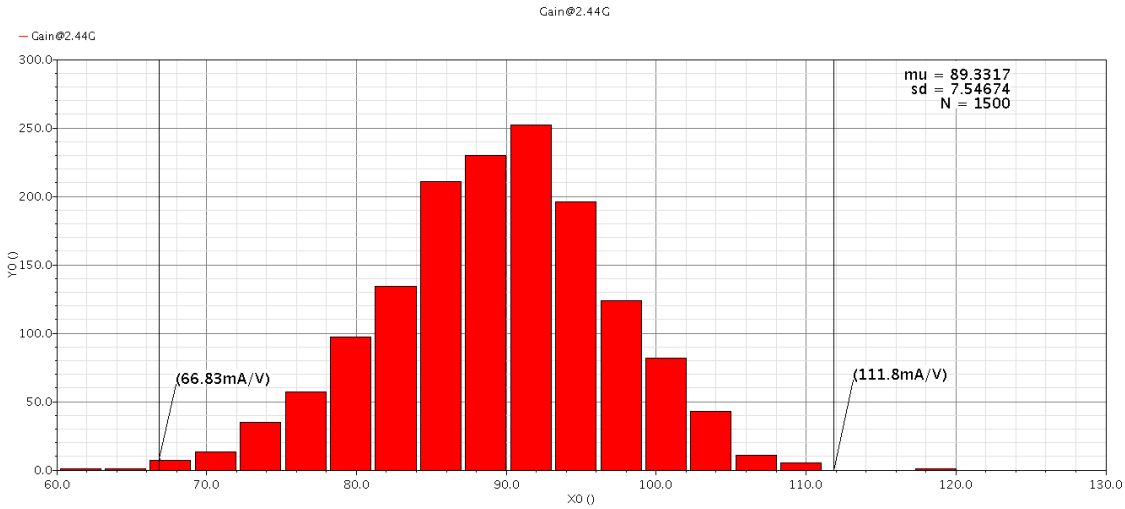

Figure 4.35: Gain with Mismatch Effect

4.4.6.2 Noise Figure

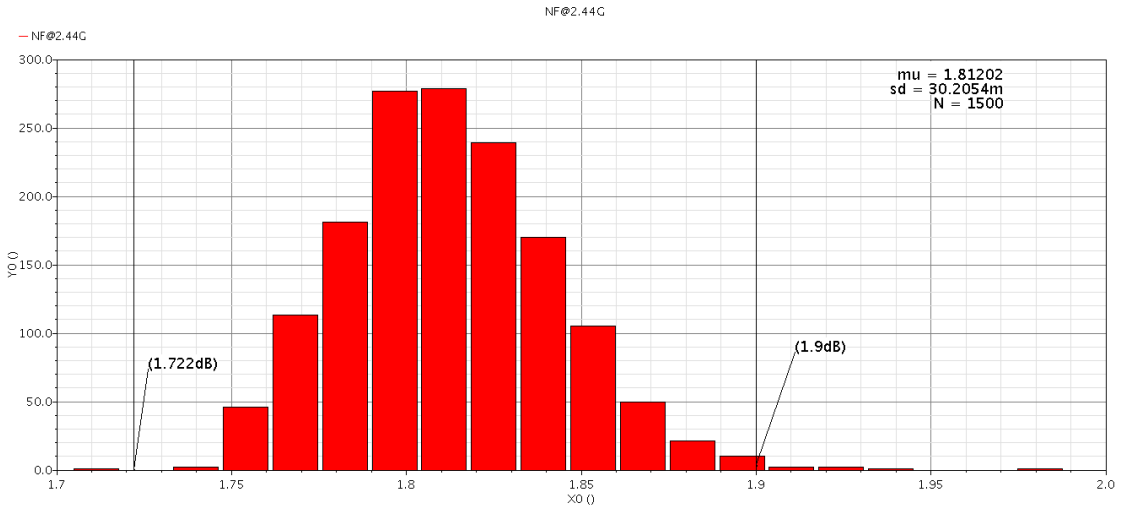

Figure 4.36: NF with Mismatch Effect

4.4.6.3 Input Matching

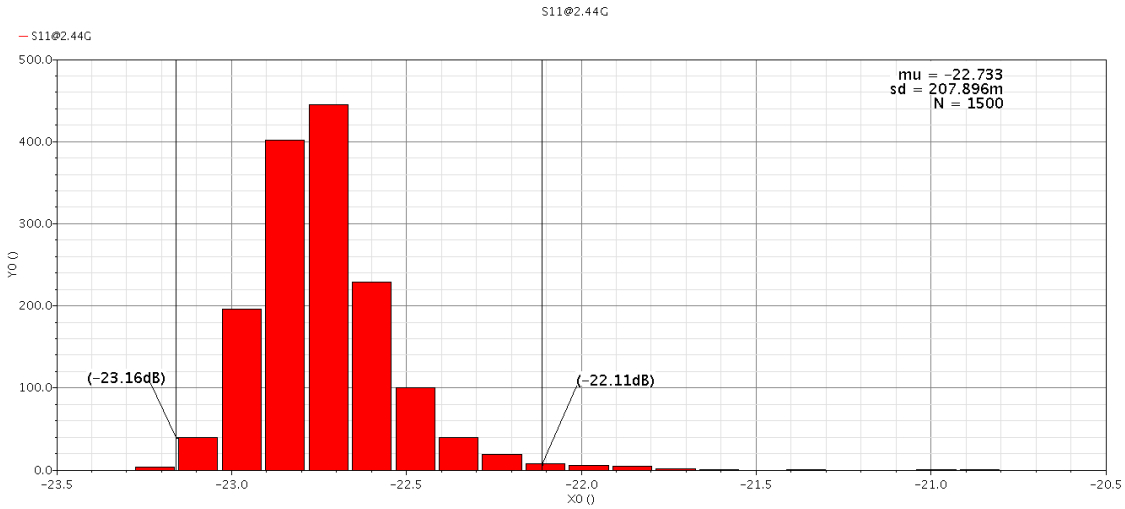

Figure 4.37: S_{11} with Mismatch Effect

4.4.6.4 IIP_3

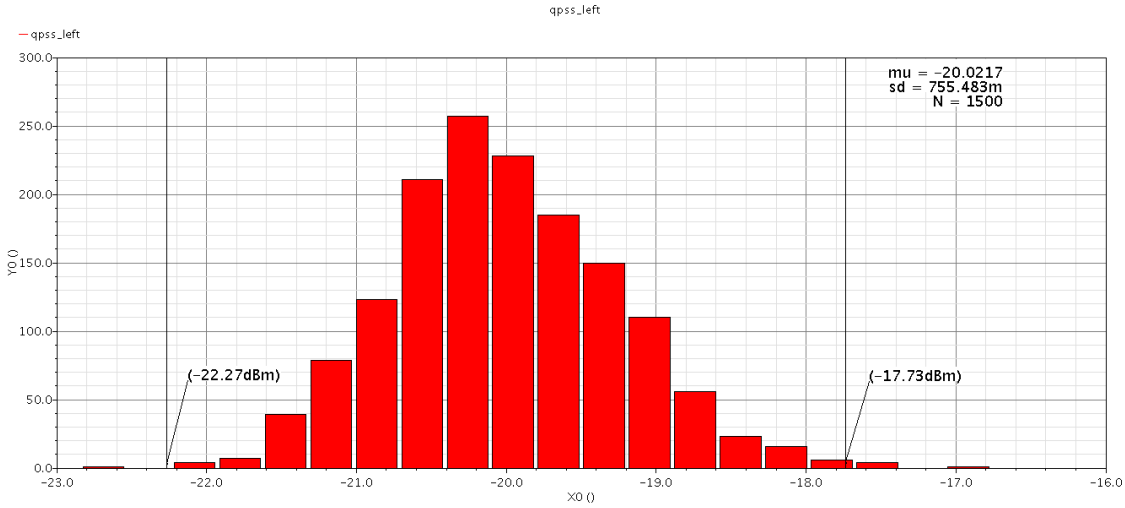

Figure 4.38: IIP_3 with Mismatch Effect

4.4.6.5 P_{1dB}

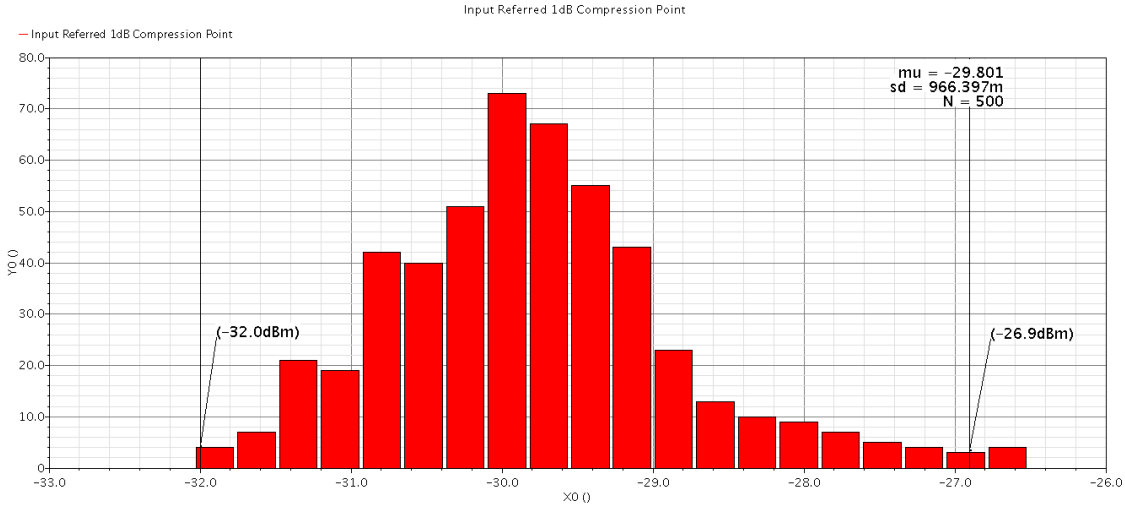

Figure 4.39: P_{1dB} with Mismatch Effect

4.4.6.6 Output Resistance

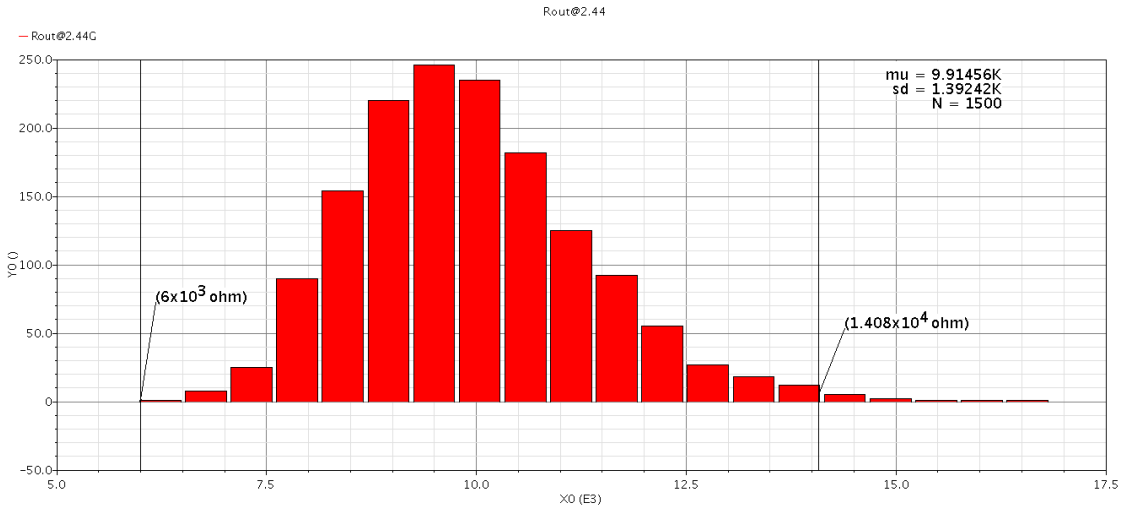

Figure 4.40: Output Resistance with Mismatch Effect

4.4.6.7 Output Capacitance

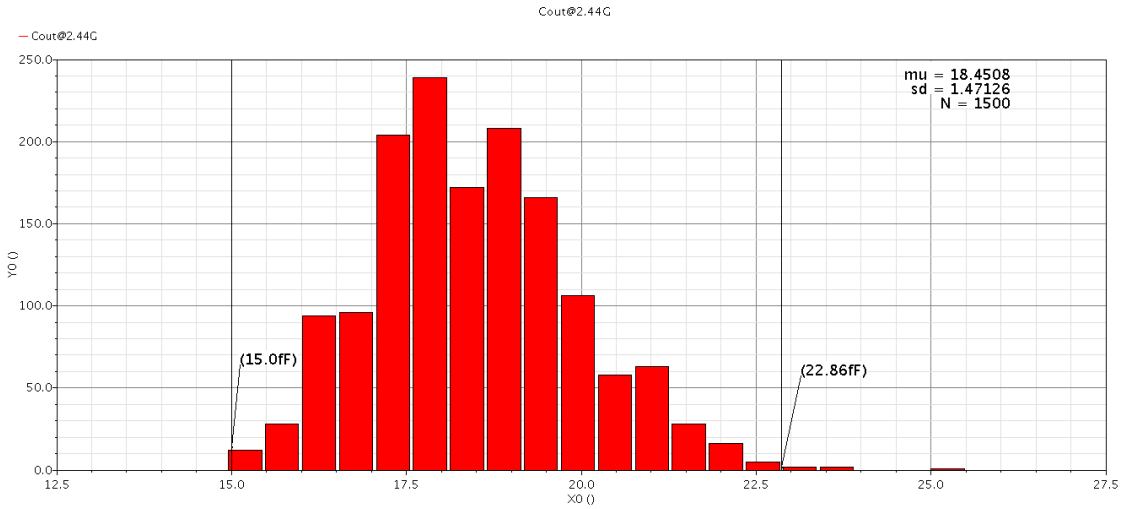

Figure 4.41: Output Capacitance with Mismatch Effect

4.4.6.8 Current Consumption

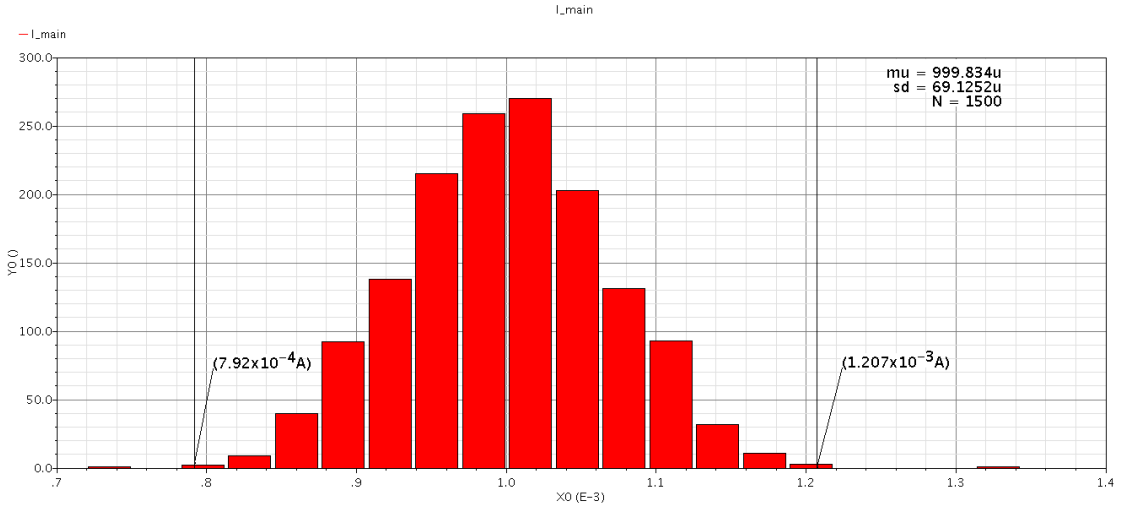

Figure 4.42: Current Consumption with Mismatch Effect

4.4.6.9 Phase Margin

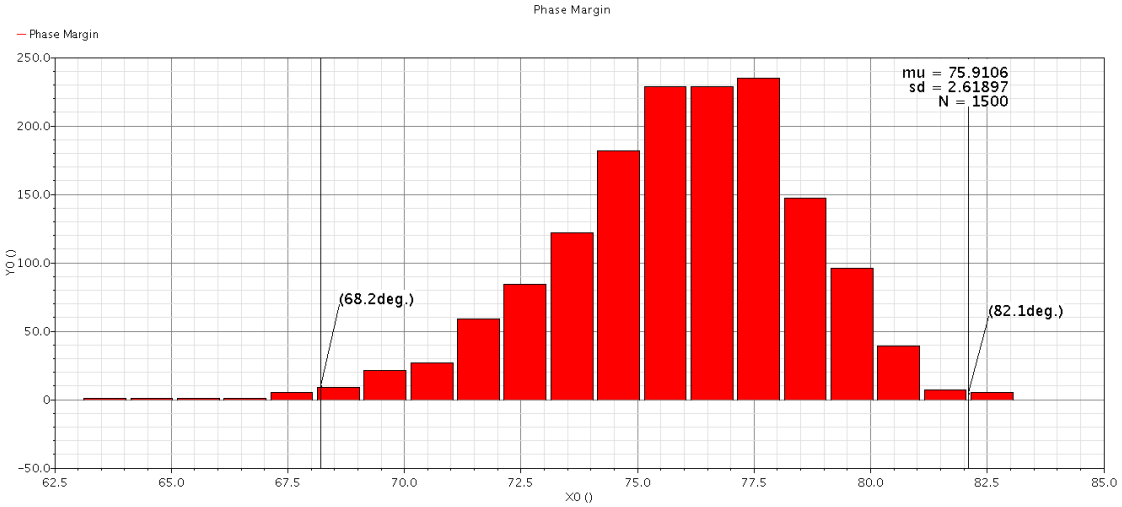

Figure 4.43: PM with Mismatch Effect

4.4.6.10 Summary of the results in mismatch simulation

Parameter	**Mean**	**Mean-3σ**	**Mean+3σ**
Gain	$89mA/V$	$66.83mA/V$	$112mA/V$
NF	$1.81dB$	$1.722dB$	$1.9dB$
S_{11}	$-22.7dB$	$-23.16dB$	$-22.11dB$
IIP_3	$-20dBm$	$-22.27dBm$	$-17.73dBm$
P_{1dB}	$-29.8dBm$	$-32dBm$	$-27dBm$
R_{out}	$9.9K\Omega$	$6K\Omega$	$14K\Omega$
C_{out}	$18.45fF$	$15fF$	$22.8fF$
Current	$1mA$	$792\mu A$	$1.207mA$
PM	76°	68°	82°

Table 4.13: Summary of the results in mismatch simulation

4.5 Layout of the Proposed LNA

The Layout of the proposed LNA was done using TSMC-65nm process kit using 9-Metal layers, VDD and GND are chosen to be at top metal layers to improve the parasitic capacitances and resistances, the area of the spiral inductors was optimized so, the spiral inductors are in metal 9 because it is the top thick metal in the stack and also to improve the quality factor of the inductors. The LNA passed DRC, LVS simulations and a parasitic extraction (PEX) was done for post layout simulation.

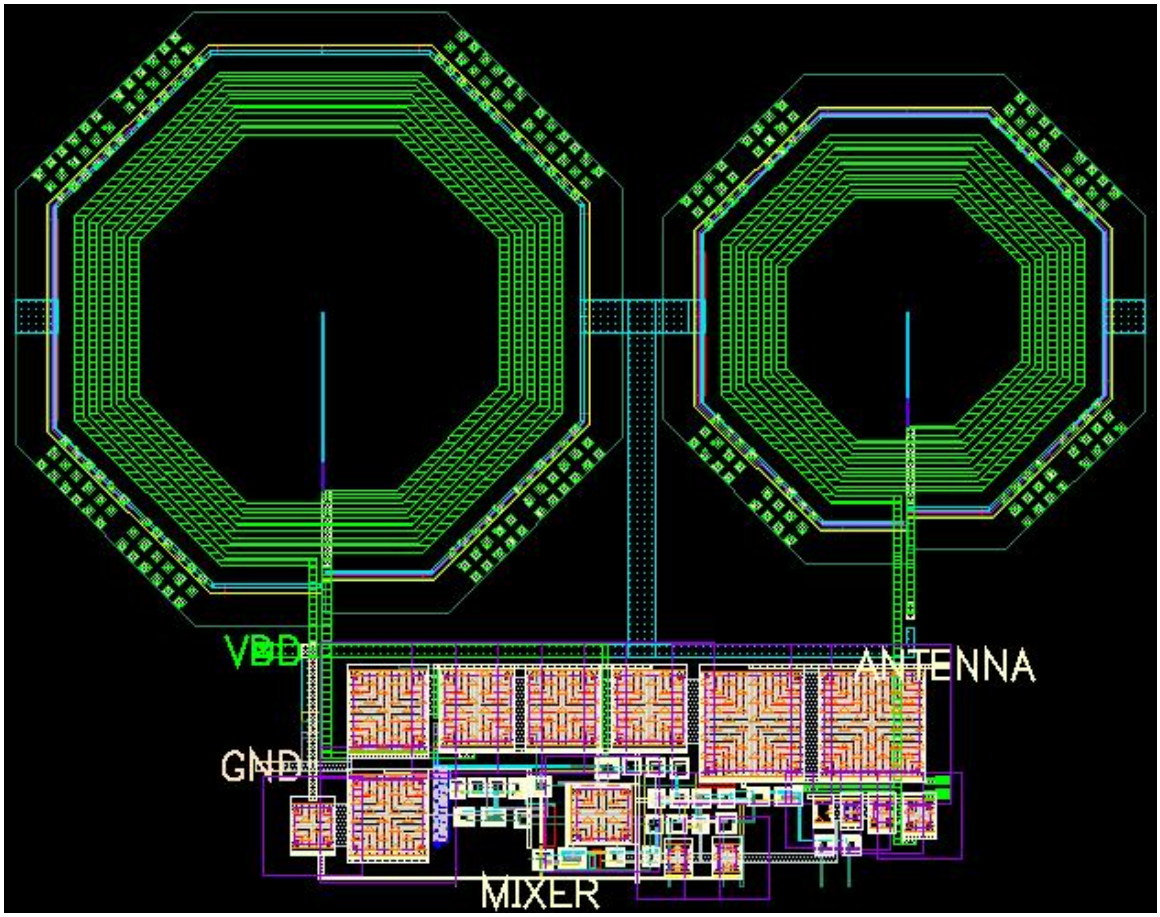

Figure 4.44: Layout of the Proposed LNA

Total Area is $420 * 324 \mu m^2 \equiv 0.136 mm^2$

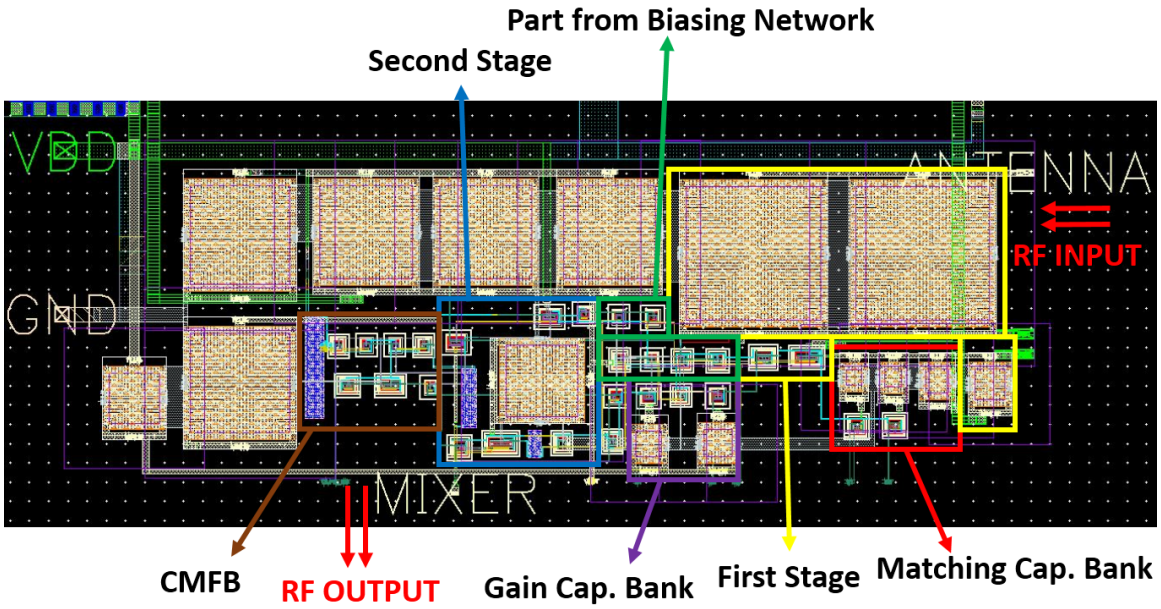

Figure 4.45: Layout without Spiral Inductors

4.5.1 Typical Post Layout Simulation of the Proposed LNA

4.5.1.1 Trans-Conductance Gain

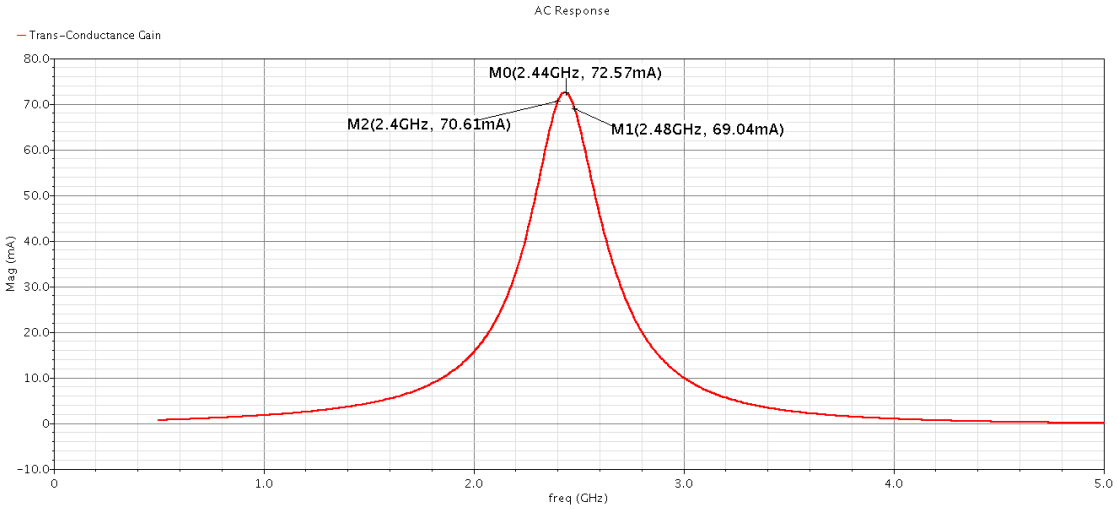

Figure 4.46: Post Layout G_m

4.5.1.2 Noise Figure

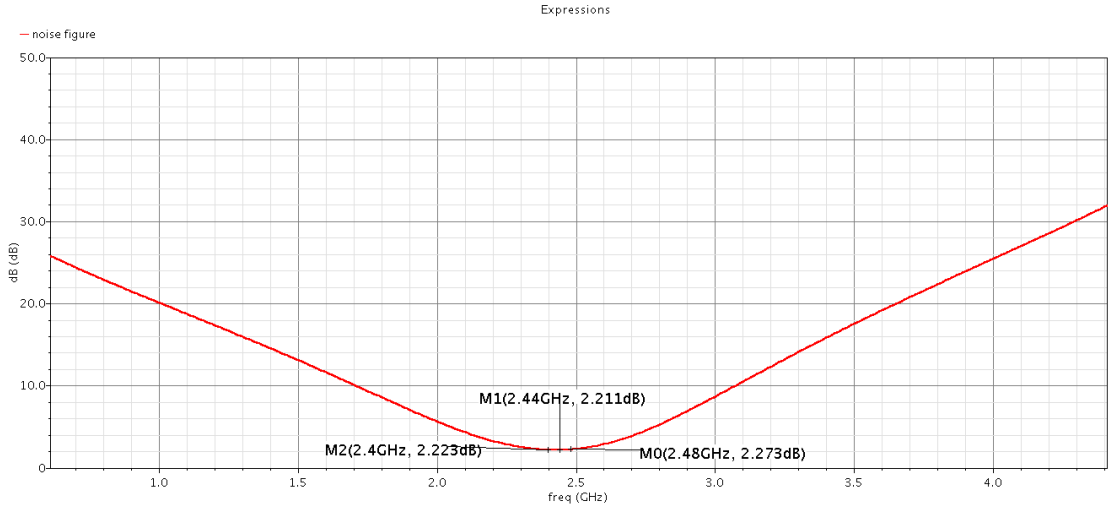

Figure 4.47: Post Layout Noise Figure

4.5.1.3 Input Matching

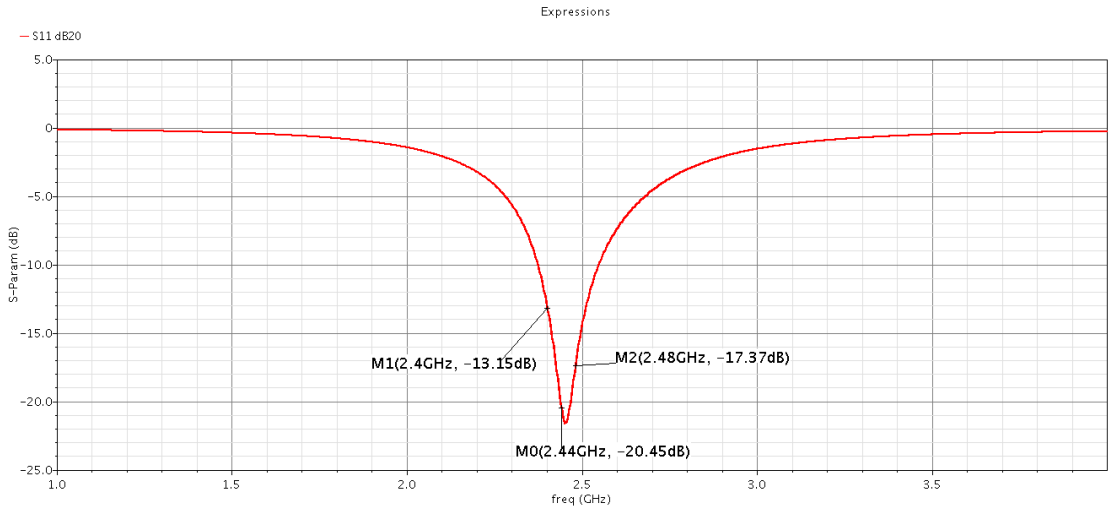

Figure 4.48: Post Layout Input Matching

4.5.1.4 IIP_3

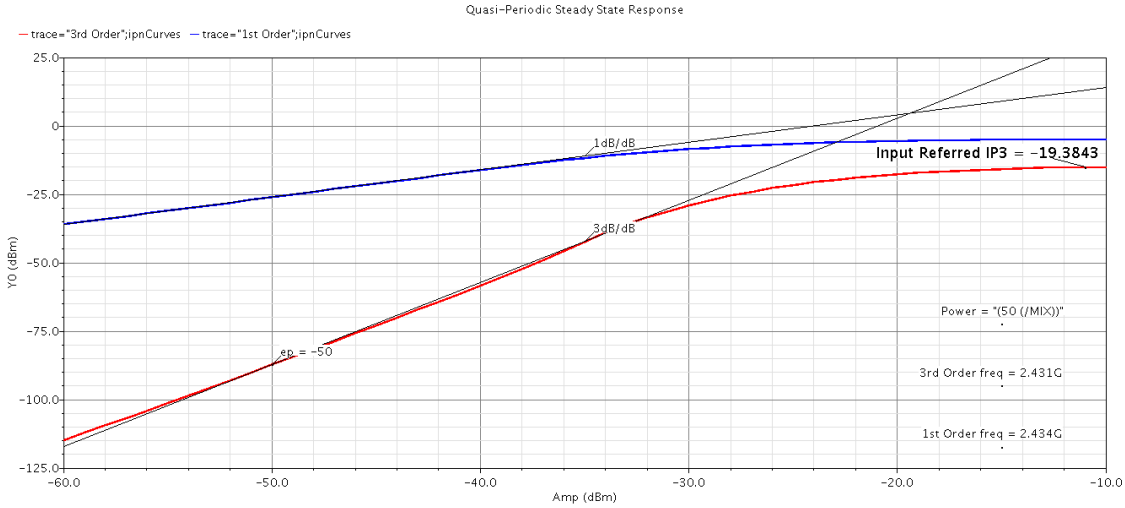

Figure 4.49: Post Layout IIP_3

4.5.1.5 P_{1dB}

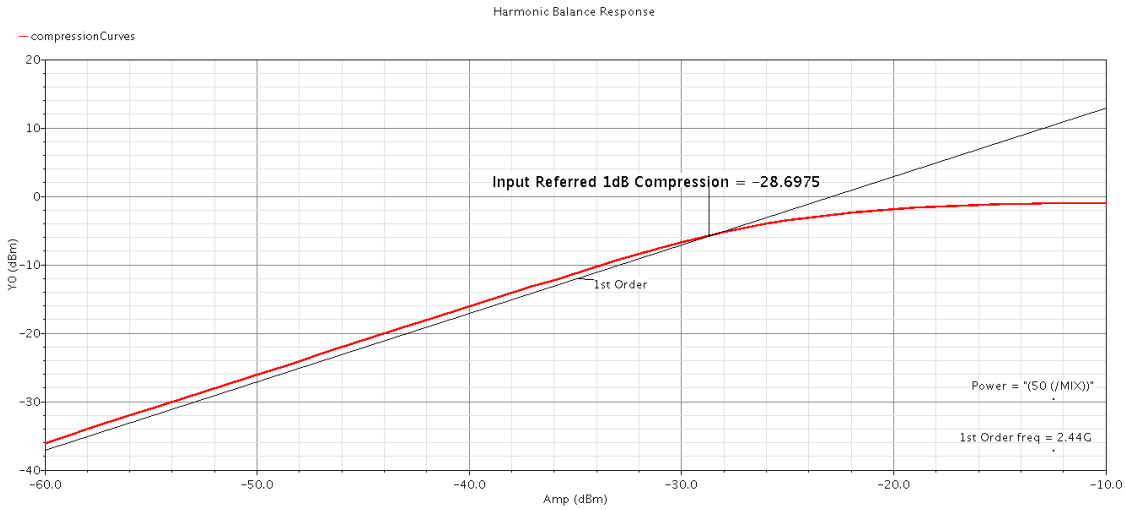

Figure 4.50: Post Layout P_{1dB}

4.5.1.6 Output Resistance

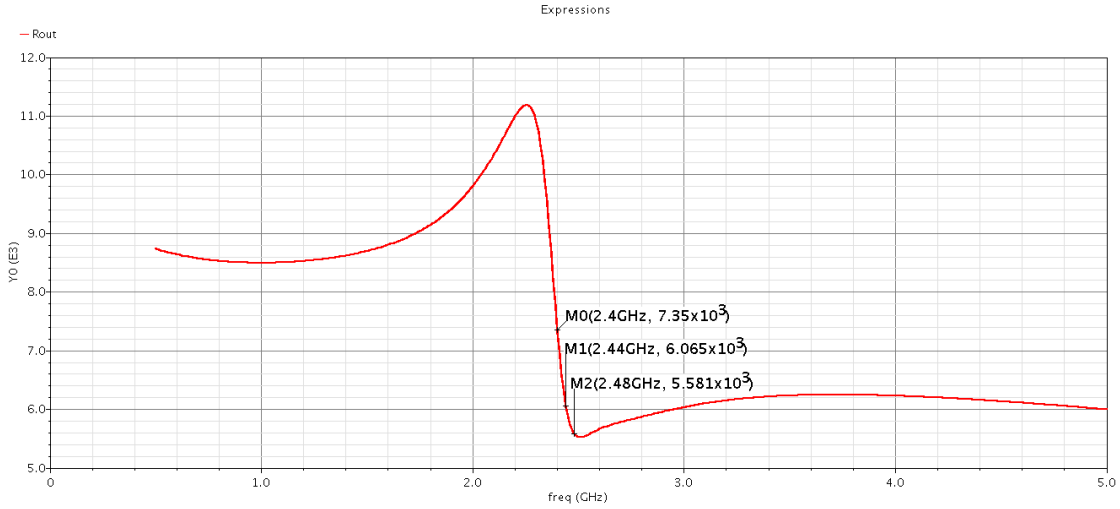

Figure 4.51: Post Layout Output Resistance

4.5.1.7 Output Capacitance

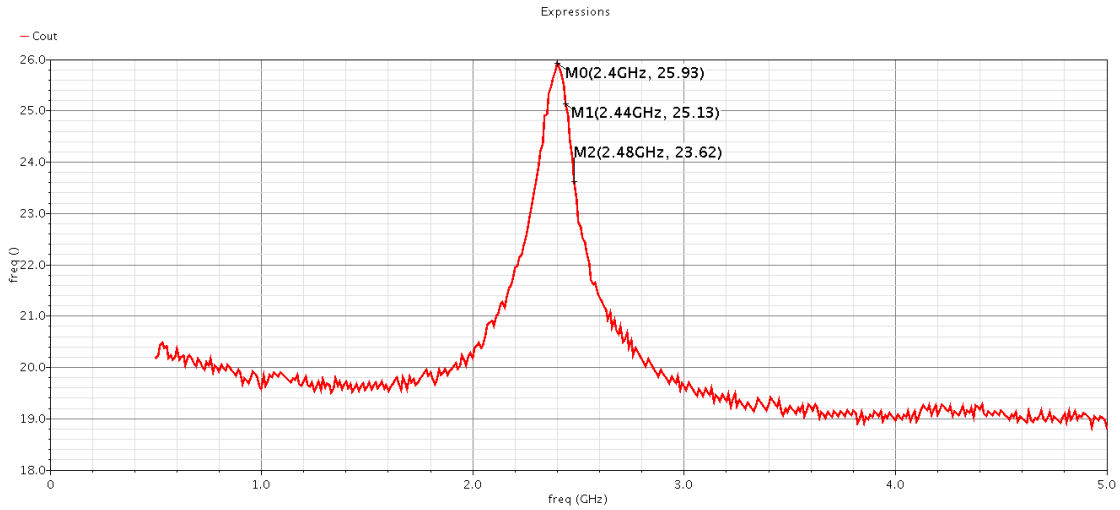

Figure 4.52: Post Layout Output Capacitance

The output capacitance was the most degraded spec. after layout as the extracted parasitics directly affect the spec.

4.5.1.8 Current Consumption

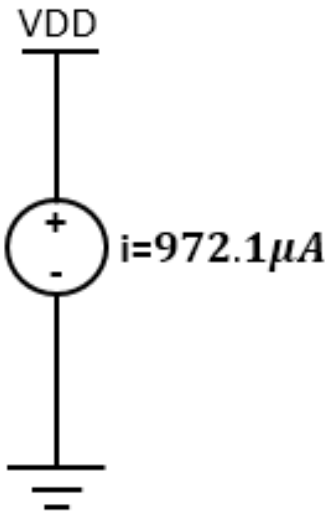

Figure 4.53: Post Layout Current Consumption

4.5.1.9 CMFB Stability

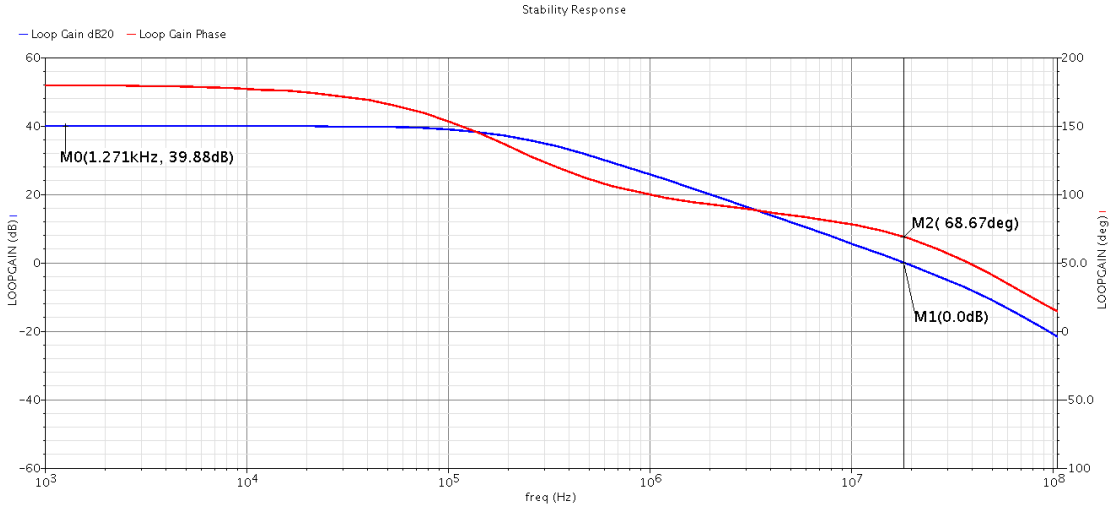

Figure 4.54: Post Layout Phase Margin

4.5.1.10 Comparison between Schematic and Layout @ 2.44GHz

Parameter	Schematic	Layout
Gain	$90mA/V$	$72.5mA/V$
NF	$1.81dB$	$2.2dB$
S_{11}	$-23dB$	$-20.4dB$
IIP_3	$-20dBm$	$-19.3dBm$
P_{1dB}	$-30dBm$	$-28.7dBm$
R_{out}	$9.975K\Omega$	$6K\Omega$
C_{out}	$18.2fF$	$25fF$
Current	$998\mu A$	$972\mu A$
PM	75.5°	68.6°

Table 4.14: Comparison between Schematic and Layout @ 2.44GHz

4.5.2 Post Layout Corner Simulation of the Proposed LNA

Here, Only 8 extreme Corners were simulated table 4.15

Variation	Corners
Temperature	$\{-40^oC, 125^oC\}$
Supply	$\{950mV, 1.05V\}$
Overall Chip Process	$\{FF, SS\}$

Table 4.15: Simulated PVT Corners in Post Layout Simulation

4.5.2.1 Trans-Conductance Gain

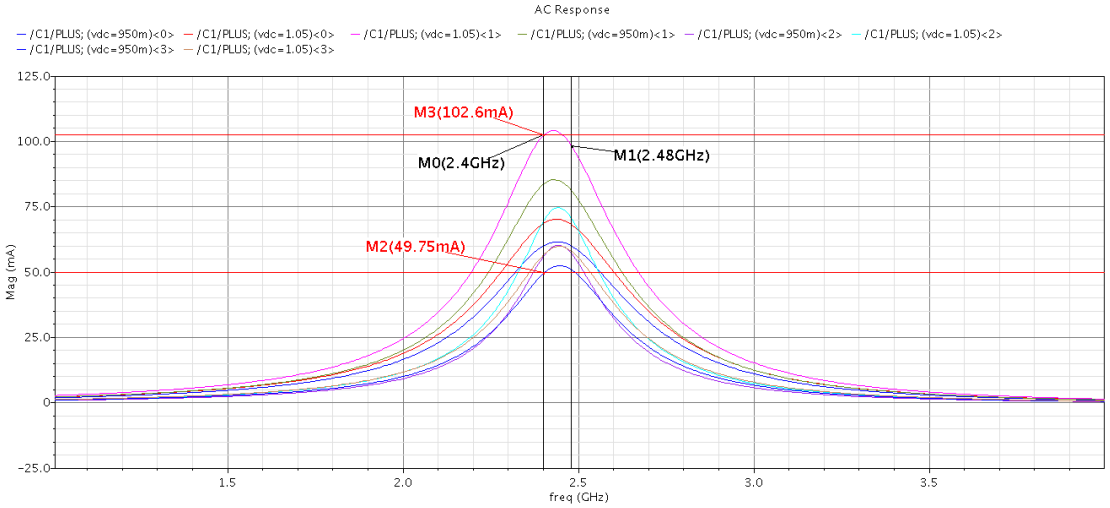

Figure 4.55: Post Layout G_m across Corners

4.5.2.2 Noise Figure

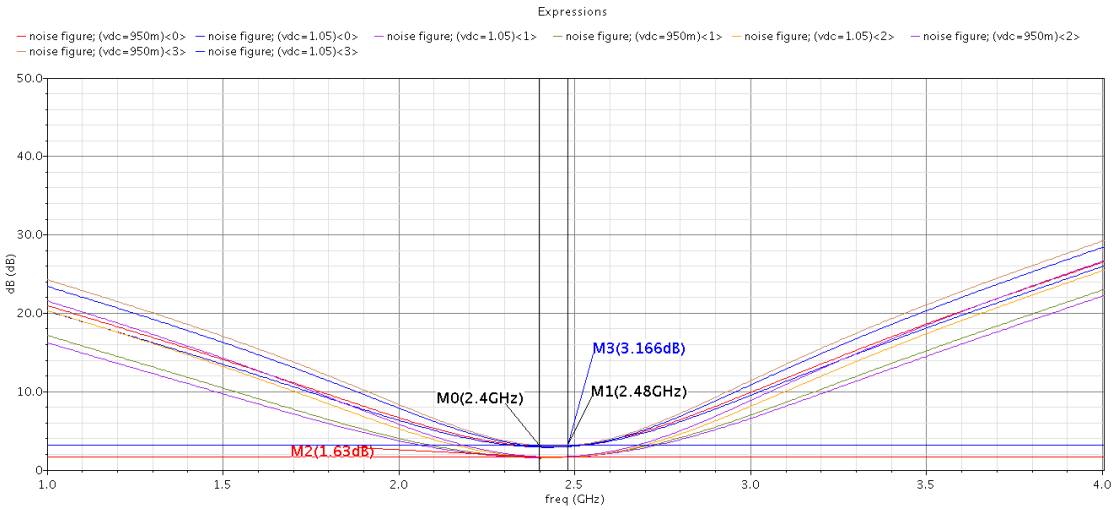

Figure 4.56: Post Layout Noise Figure across Corners

4.5.2.3 Input Matching

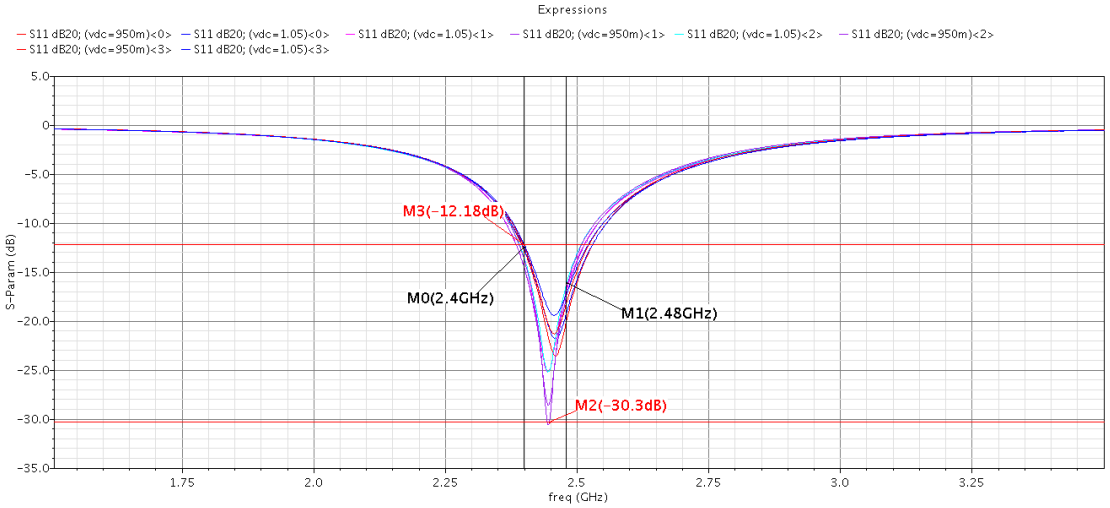

Figure 4.57: Post Layout S_{11} across Corners

4.5.2.4 Output Resistance

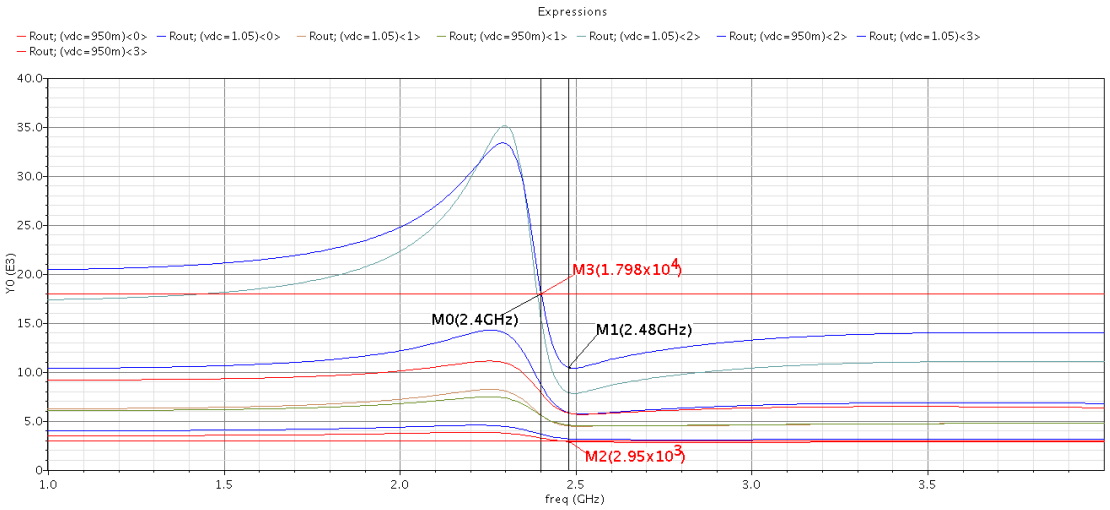

Figure 4.58: Post Layout R_{out} across Corners

4.5.2.5 Output Capacitance

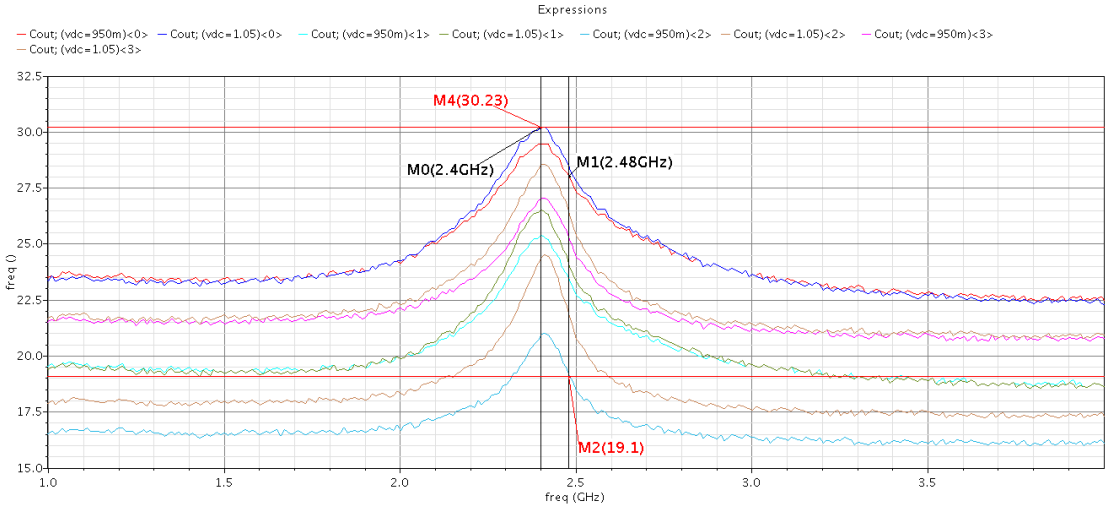

Figure 4.59: Post Layout C_{out} across Corners

4.5.2.6 IIP_3 and P_{1dB}

Parameter	Min	Max	Mean
IIP_3	$-23.6dBm$	$-18dBm$	$-21dBm$
P_{1dB}	$-30.2dBm$	$-25dBm$	$-28.4dBm$

Table 4.16: Summary of Post Layout IIP_3 and P_{1dB} across Corners

4.5.2.7 Current Consumption and Phase Margin

Parameter	Min	Max	Mean
I	$550\mu A$	$1.662mA$	$1.05mA$
PM	43°	86°	67.5°

Table 4.17: Summary of Post Layout Current Consumption and PM across Corners

As shown from the results presented above, the Layout needs further debugging and optimization to get more best results across corners simulation, also the off chip connections and the input of the LNA have pads and should be modeled by a shunt capacitor to model the pads, series inductor to model the bond wire to the external pin Fig. 4.60.

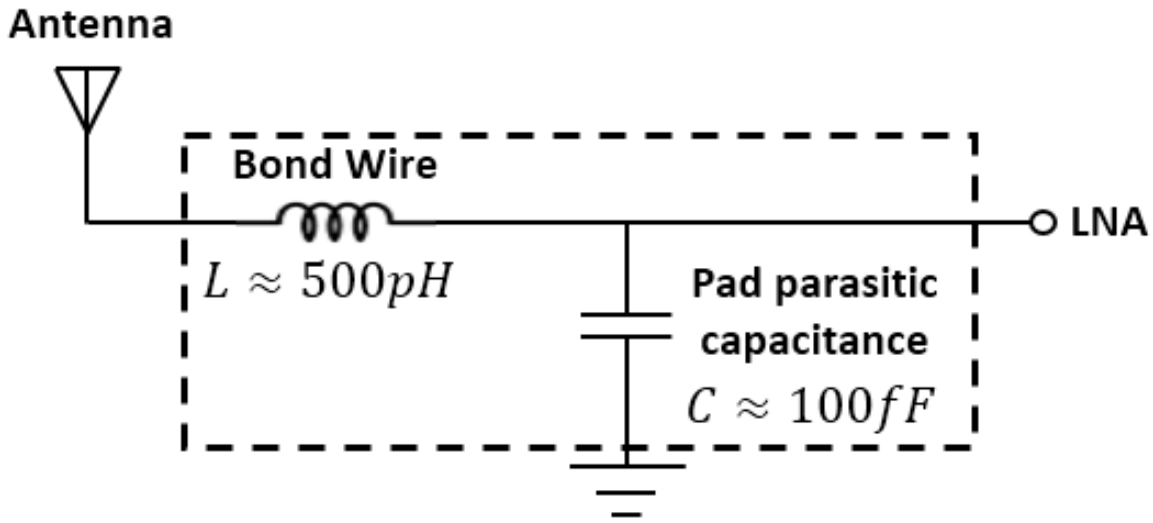

Figure 4.60: Pad Modeling

4.6 Performance Summary

Parameter	**Spec**	**Typical**	**W.Corner**	**Mean**$\pm 3\sigma$	**Layout**
Gain	$> 65.3mA/V$	$90mA/V$	$49mA/V$	$66.83mA/V$	$72.5mA/V$
NF	$< 3dB$	$1.81dB$	$3.05dB$	$1.9dB$	$2.2dB$
S_{11}	$< -12dB$	$-23dB$	$-13.8dB$	$-22.11dB$	$-20.4dB$
IIP_3	$> -20dBm$	$-20dBm$	$-25.22dBm$	$-22.27dBm$	$-19.3dBm$
P_{1dB}	$> -30dBm$	$-30dBm$	$-33dBm$	$-32dBm$	$-28.7dBm$
R_{out}	$> 5K\Omega$	$9.975K\Omega$	$3.6K\Omega$	$6K\Omega$	$6K\Omega$
C_{out}	$< 20fF$	$18.2fF$	$24.3fF$	$22.8fF$	$25fF$
Current	$< 1.2mA$	$998\mu A$	$1.72mA$	$1.207mA$	$972\mu A$
PM	$> 60^\circ$	75.5°	44.5°	68°	68.6°

Table 4.18: Performance Summary @$2.44GHz$

4.7 Conclusion

Low Noise Amplifiers have many types, which are chosen according to some design considerations to meet different systems requirements. LNAs determine the noise figure of the overall receiver so, LNAs are optimized to achieve relatively high gain to relax the noise figure requirement on subsequent stages. Although the linearity of the receivers is determined from last blocks, the Linearity of LNAs Inconsistent with gain and noise figure and this makes the design of LNAs is more challenging to compromise between different specification. Also in most of the designs, LNAs determine the input matching of the receiver so, LNAs should guarantee proper matching in the band of interest and should guarantee stability with variations of the

antenna impedance. A current mode LNA was designed for Bluetooth Low Energy applications (BLE), according to standard version 5.1. The proposed LNA was design and simulated using Cadence Virtuoso. It was two stages because of high gain spec. the first one was "Common-Source with inductive degeneration" and the second was "Stacked Inverter-Based amplifier" which was voltage to current amplifier to achieve current mode operation. The proposed LNA was optimized to meet the specifications in typical conditions, PVT Corners and Mismatch. The layout of the proposed LNA was presented also and was optimized for area and small parasitics.

4.8 Future Work

Complete debugging in the layout for better performance across different corners, and also doing some EM-Simulations to have more accurate modeling. design the process monitor circuit that generates the control signals for the Cap.Bank.

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[2] B. Razavi. *Design of analog CMOS integrated circuits*. Tata McGraw-Hill Education, 2002.

[3] Bluetooth core specification v5.1. `https://vtsociety.org/wp-content/uploads/2019/07/Core_v5.1.pdf`, 2019.

[4] M. M. Tarar, M. Wei, and R. Negra. Stacked inverter-based amplifier with bandwidth enhancement by inductive peaking. In *2014 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC)*, pages 1–3, 2014.

[5] D. Mirzoyan and A. Khachatryan. A new process variation monitoring circuit. In *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pages 1–5, 2016.

Chapter 5: Down-Conversion Mixer

5.1 Introduction

A mixer is a three-port device that performs frequency translation by multiplying two waveforms. In a transmitter, it up-converts the data signal from a low frequency to the carrier frequency while in a receiver, it down-converts the data signal from the carrier frequency to a low frequency. Ideally, the signal at the output is a replica of the signal at the input, translated to a lower or higher frequency, with no loss of information and no added distortion. The down-conversion mixer consists of the input port "RF port", the local oscillator port "LO port" and the output port which is called the "IF port" in a heterodyne receiver or the "baseband port" in a direct-conversion receiver.

The motivation behind employing down-conversion mixers in wireless receivers is that ideally a data converter should be in front of an antenna as this gives the maximum programmability as shown in Fig. 5.1. The problem with this configuration is that the filter only rejects out-of-band blockers while in-band blockers require a power hungry, high-resolution data converter. For that reason, most receivers use the configuration shown in Fig. 5.2, where the down-conversion relaxes the IF signal processing and makes it more efficient and at lower power.

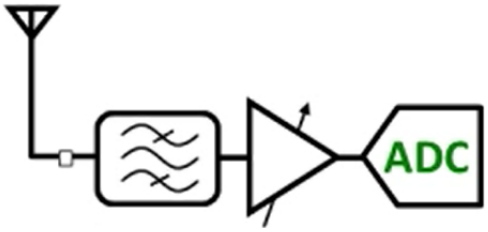

Figure 5.1: Receiver without a mixer

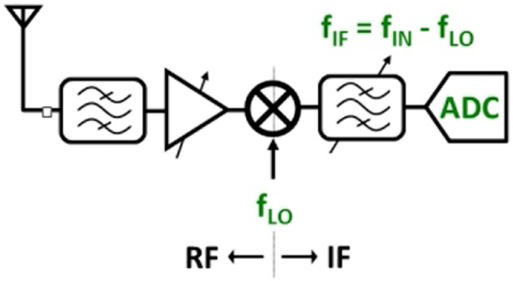

Figure 5.2: Receiver with a down-conversion mixer

A nonlinear system $y(t) = a_1x(t) + a_2x^2(t) + a_3x^3(t)$ can be used as a linear mixer where the input applied is $x(t) = A_1cos(\omega_1 t) + A_2cos(\omega_2 t)$. Due to the second order nonlinearity, the output will be $y(t) = a_2A_1A_2sin(\omega_1 - \omega_2)t + a_2A_1A_2sin(\omega_1 + \omega_2)t + ...$, which are the down-conversion and up-conversion terms as shown in Fig. 5.3. If a_2 does not change with the input applied, then the mixing operation will be linear.

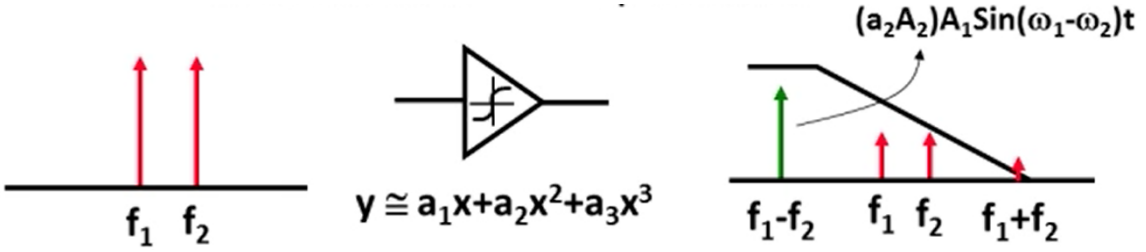

Figure 5.3: Nonlinear System used as a linear mixer

The mixer can be realized by an ideal switch that turns on and off by V_{LO}, yielding $V_{IF} = V_{RF}$ or $V_{IF} = 0$ as shown in Fig. 5.4. With abrupt switching, the operation can be viewed as multiplication of the RF input by a square wave toggling between 0 and 1 even if the LO waveform itself is a sinusoid, which is equivalent to the convolution operation in the frequency domain as shown in Fig. 5.5. Thus the circuit mixes the RF input with all of the LO

harmonics producing mixing spurs.

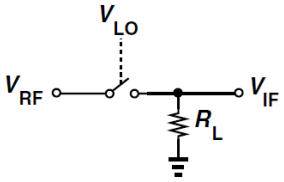

Figure 5.4: Mixer as an ideal switch

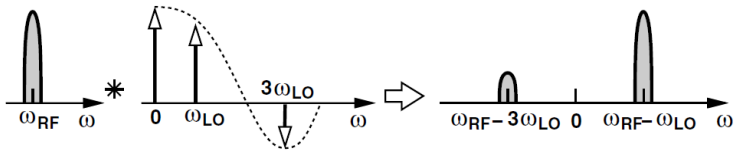

Figure 5.5: Input and output spectra

Therefore, the mixer is a time-variant circuit, it should be sufficiently linear with respect to the input port but it is non-linear with respect to the LO port and this nonlinearity or time variance is what causes frequency translation.

5.2 Performance Parameters

5.2.1 Conversion Gain

The "voltage conversion gain" of a down-conversion mixer is defined as the ratio of the rms of the IF output signal to the rms of the RF input signal. In modern RF design, voltage or current quantities are preferred rather than power quantities because the input impedances are mostly imaginary, making the use of power quantities difficult and unnecessary.

5.2.2 Noise Figure

It is defined as the signal to noise ratio at the input divided by the signal to noise ratio at the output in decibels but due to frequency translation, the

noise figure of down-conversion mixers is often a source of great confusion and there are multiple definitions for it.

If an ideal noiseless mixer with unity gain is considered as shown in Fig. 5.6, the "single-sideband" (SSB) noise figure is equal to 3 dB as the noise from the image band will fold into the desired IF band as shown in Fig. 5.7. This definition assumes that there is no signal at the image frequency which is the case in heterodyne receivers. The "double-sideband" (DSB) noise figure is equal to 0 dB as the signal resides on both sides of the LO frequency which is the case in direct-conversion receivers as shown in Fig. 5.8.

It should be noted that for a real mixer due to the LO harmonics, noise from multiple sidebands can fold into the IF frequency and cause more degradation to the NF. Also, the single-sideband noise figure can be improved by approximately 3 dB in an image-reject receiver because the noise from the antenna, LNA and mixer in the image band is filtered by the complex filter.

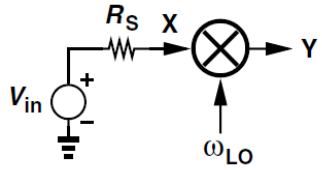

Figure 5.6: Ideal Noiseless Mixer

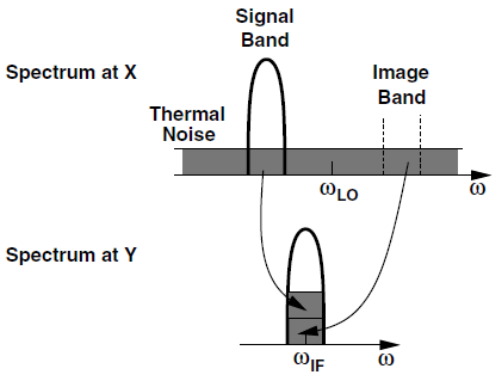

Figure 5.7: Input and output spectra in a heterodyne receiver

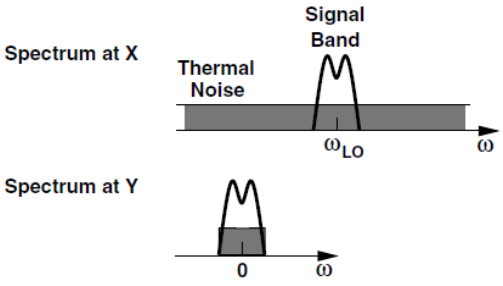

Figure 5.8: Input and output spectra in a direct-conversion receiver

5.2.3 Linearity

The linearity of the down-conversion mixer is defined in much the same way as that of a low-noise amplifier or a receiver, using the 1-dB compression point (P_{1dB}) and the third-order intercept point at the input (IIP_3). In the receiver chain, the input noise of the mixer following the LNA is divided by the LNA gain when referred to the receiver input. Similarly, the IIP_3 of the mixer is scaled down by the LNA gain. Therefore, the design of down-conversion mixers entails a compromise between the NF and the IIP_3.

5.2.4 Port-to-Port Feedthrough (Isolation)

Isolation between two ports can be defined as the ratio between the power at a certain frequency in the first port to the power leaked at the same frequency in the second port assuming the two ports are operating at different frequencies. Owing to device capacitances, mixers suffer from unwanted coupling (feedthrough) from one port to another as shown in Fig. 5.9. For example, if the mixer is realized by a MOSFET then the gate-source

and gate-drain capacitances create feedthrough from the LO port to the RF and IF ports as shown in Fig. 5.10. Therefore, isolation is mostly affected by the topology of the mixer, the sizing of the devices and the layout of the mixer.

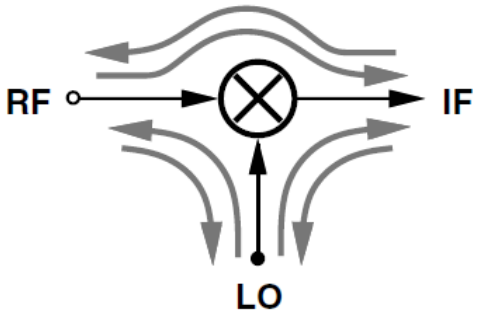

Figure 5.9: Feedthrough paths in a mixer

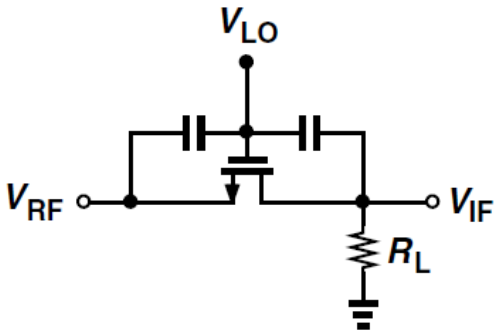

Figure 5.10: Mixer realized by a MOSFET

The effect of mixer port-to-port feedthrough on the performance depends on the receiver architecture. In direct-conversion and low-IF receivers:

• The LO-RF feedthrough is very critical and undesirable as it produces LO radiation from the antenna and also causes self-mixing (in case of direct-conversion receivers) which produces DC offsets that can saturate the blocks following the mixer.

• The LO-IF feedthrough is heavily suppressed by the baseband low-pass filters.

• The RF-LO feedthrough is problematic as a large in-band interferer can couple to the LO and injection-pull it corrupting the LO spectrum.

• The RF-IF feedthrough corrupts the baseband signal by the beat component resulting from even-order distortion in the RF path.

5.2.5 Power Consumption

The power consumption is a critical performance parameter especially in low-power wireless standards. The power consumption of the down-conversion mixer will depend on the topology being used, the sizing of the mixer switches and the LO driver gates.

5.3 Topologies and Architectures

Mixers can be categorized according to multiple aspects. As already stated, they can be classified into up-conversion or down-conversion based on the relation between the input and the output frequencies. Based on the balance of the input and output ports, mixers can be classified into unbalanced, single-balanced or double-balanced mixers. They can be classified into active or passive mixers based on whether their switching transistors operate as amplifying devices or not. Also, passive mixers can be classified into voltage-mode (voltage-driven) or current-mode (current-driven) based on the quantity being switched.

5.3.1 Single-Balanced and Double-Balanced Mixers

The unbalanced mixer shown in Fig. 5.4 is rarely used in modern RF design as it discards the RF signal for half of the LO period. The more efficient approach is shown in Fig. 5.11, where two switches are driven by differential LO phases commutating the RF input to one of the two outputs during each half period. This configuration is called a “single-balanced” mixer and it provides twice the conversion gain of the unbalanced mixer but

of course using twice the number of components. The LO-RF feedthrough vanishes if the circuit is symmetric but it suffers from significant LO-IF feedthrough which is a serious problem in heterodyne receivers as it can desensitize the IF mixers and also, the noise at the LO port appears at the output. To eliminate those effects, two single-balanced mixers are connected such that their LO feedthroughs cancel but their output signals do not as shown in Fig. 5.12. This configuration is called a "double-balanced" mixer and it comes at the cost of twice the number of components but most importantly at twice as much power for the same conversion gain. It has double the output noise and it also requires the input to be differential which may not be desirable in many applications.

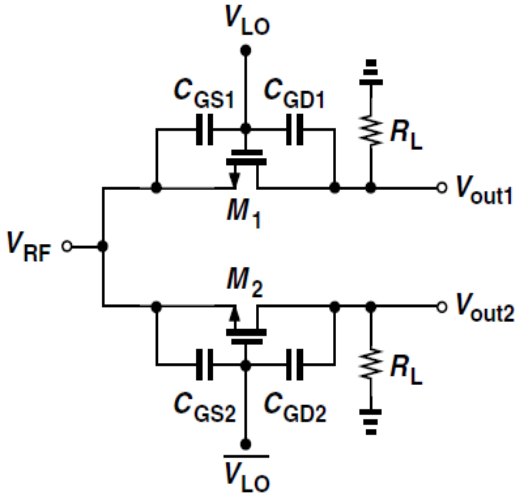

Figure 5.11: Single-balanced mixer

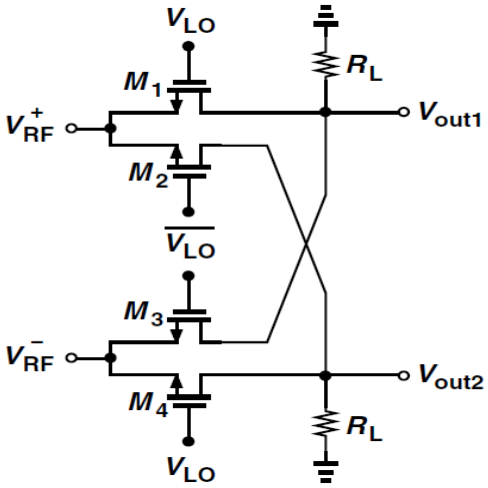

Figure 5.12: Double-balanced mixer

To summarize, a comparison is made between single-balanced and double-balanced mixers in Table 5.1.

Table 5.1: Comparison between single-balanced and double-balanced mixers

Parameter	**Single-Balanced Mixers**	**Double-Balanced Mixers**
Conversion Gain	Equal	
LO-RF Feedthrough	Rejected	
Power Consumption	Lower	Doubled
Output Noise	Lower	Doubled
LO-IF Feedthrough	Not Rejected	Rejected

5.3.2 Active and Passive Mixers

A double-balanced active mixer is shown in Fig. 5.13, it is commonly known as the Gilbert cell. An active mixer basically consists of three stages, a V/I converter that converts the RF voltage to current, a current switch that commutates (steers) the RF current by the LO producing the IF current and then an I/V converter that converts the IF current to voltage. Ideally, it has a conversion gain of $\frac{2}{\pi} g_{m1} R_D$ which improves its NF and the NF of subsequent stages. Also, its LO drive is modest and does not require rail-to-rail LO drive because the four switching devices are kept in saturation. Its disadvantages are mainly due to the DC bias current drawn from the supply which will consume more power and also since this current is steered with the RF current, it will cause the mixer to suffer from high flicker noise. Another critical disadvantage is its poor linearity as the three stages are stacked on top of each other causing the mixer to suffer from headroom issues leading to a poor linearity performance.

On the other hand, a double-balanced passive mixer is shown in Fig. 5.14, it is commonly known as the ring mixer. Passive mixers can commutate either voltage or current depending on the output impedance of the preceding stage and the input impedance of the following stage. An ideal double-balanced voltage-mode passive mixer will have a conversion gain of $\frac{2}{\pi}$ which is lower than unity and thus its NF and the NF of subsequent stages will be worse. Also, the switching devices need to be fully turned on (in deep triode) and off as this will affect the conversion gain and NF of the mixer by affecting the on-resistance of the devices. This means that the switching must be abrupt requiring rail-to-rail LO drive that is power hungry and hard to synthesize at very high frequencies. The advantage of the passive mixer is that it draws no DC current from the supply so it will have very low flicker noise. Also, it is proven to be very linear with respect to the active mixer mainly because it does not suffer from headroom issues.

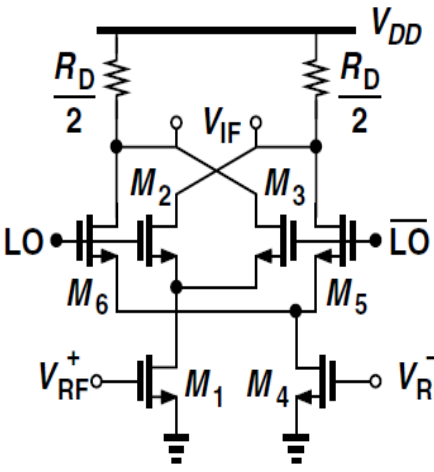

Figure 5.13: Double-balanced active mixer

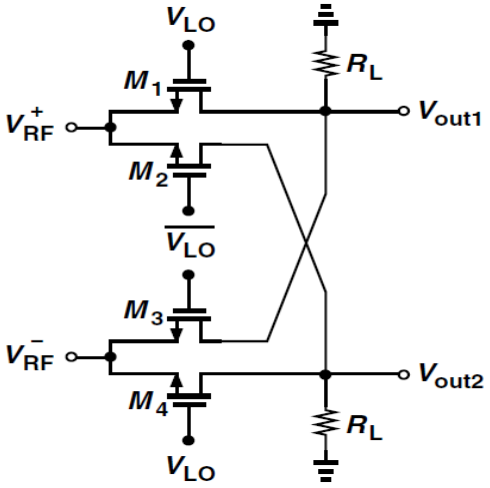

Figure 5.14: Double-balanced passive mixer

To summarize, a comparison is made between active and passive mixers

in Table 5.2, but it should be noted that this will depend on the technology being used and the design of the mixer.

Table 5.2: Comparison between active and passive mixers

Parameter	**Active Mixers**	**Passive Mixers**
Commutates	Current	Current or Voltage
Conversion Gain	Higher (usually>1)	Lower (usually<1)
Requires DC current	Yes	No
White Noise	Comparable	
Flicker Noise	High	Very Low
Loading	Capacitive	Resistive and Capacitive
Linearity	Poor	Good
LO Drive	Modest	Rail-to-Rail
Power Consumption	Mainly due to the DC current	Mainly due to the LO drivers
Reverse Isolation between RF and IF ports	Exists	Does not exist

5.4 Current-Driven Passive Mixers

In this section, the current-driven passive mixer will be further analyzed as it will be the topology of choice according to the required specifications stated later. As shown in Fig. 5.15, the mixer with the preceding G_m cell (or LNA) and the following I/V converter (or TIA) can be viewed as a folded version of its active counterpart. Therefore as stated above, it can be ac coupled with the RF input leading to a zero DC current which improves the

flicker noise dramatically. It has superior linearity compared with its active counterpart as it has no headroom issues but at the cost of Rail-to-Rail LO drive, lower conversion gain and higher noise figure.

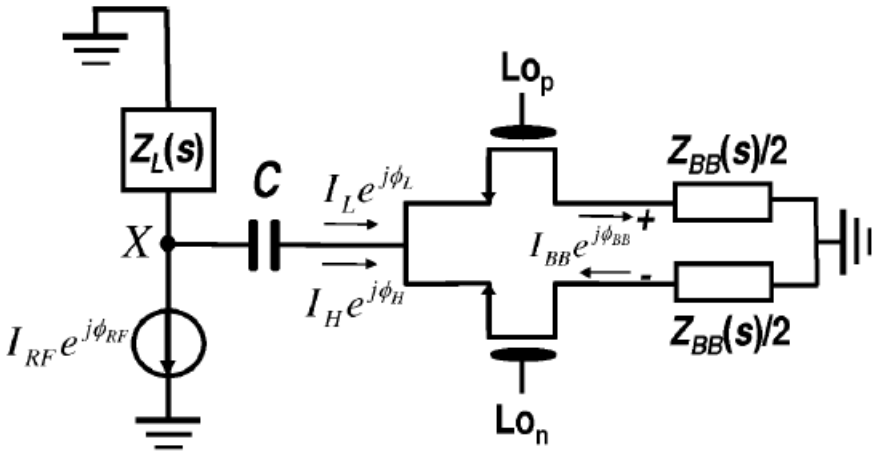

Figure 5.15: Single-balanced current-driven passive mixer with a simplified model for LNA and TIA

First, the mixer is analyzed with 50% duty-cycle LO waveforms, then the effect of changing the duty-cycle to 25% is analyzed.

5.4.1 Conversion Gain

The detailed analysis can be found in [1], the transfer function from the RF current to the baseband current is shown in eq. 5.1.

$$\frac{I_{BB}}{I_{RF}} = -\frac{\frac{1}{\pi} Z_L(\omega_{LO}) \left[Z_s^*(\omega_{LO}) + R_{SW} \right] e^{j\phi_{RF}}}{|Z_s(\omega_{LO}) + R_{SW}|^2 + \frac{1}{\pi^2} \left[Z_s(\omega_{LO}) + Z_s^*(\omega_{LO}) + 2R_{SW} \right] Z_{BB}(\omega_m)} \tag{5.1}$$

Where $Z_L(s)$ is the output impedance of the LNA, $Z_s(s)$ is equal to $Z_L(s)$ + $Z_C(s)$ where $Z_C(s)$ is the impedance of the series capacitor, $Z_{BB}(s)$ is the base-

band impedance of the TIA, R_{SW} is the on-resistance of the MOS switch, ω_{LO} is the local oscillator frequency and ω_m is the IF frequency. It should be noted that eq. 5.1 is a simplification assuming that $Z_L(s)$ and $Z_C(s)$ are almost constant from (ω_{LO}–ω_m) to (ω_{LO}+ω_m). For a zero baseband impedance (Z_{BB}=0), the conversion gain becomes the expected value of $|\frac{Z_L(\omega_{LO})}{\pi[Z_L(\omega_{LO})+Z_C(\omega_{LO})+R_{SW}]}|$. Also, high and low-side conversion gains are the same which is not the case for an IQ down-conversion mixer (in case of 50% duty-cycle LO waveforms), where the I and Q mixers are going through mutual interaction leading to unequal high and low-side conversion gains unless $Z_{BB}(s)$ is significantly lower than $Z_L(s)$ and $Z_C(s)$ across the IF channel of interest.

5.4.2 IQ Cross-Talk

In a current-driven passive IQ mixer with 50% duty-cycle LO waveforms as shown in Fig. 5.16, it is noted that if the RF input is located at the high sideband of the LO frequency, the voltages at nodes A and B not only have sidebands at the high side but they also have sidebands at the low side. In the I-branch, the low-sideband is equal and in-phase with the high-sideband but in the Q-branch, the low-sideband is equal and 180 degrees out-of-phase with the high-sideband as shown in Fig. 5.17. This results in the generation of an image current flowing between the I and Q branches which leads to unwanted effects like different high-side and low-side conversion gains, leakage of intermodulation products from one channel to the other and noise of the buffer in one channel appearing at the other channel too. The image current can be reduced by increasing the impedance of the coupling capacitor (decreasing the value of the capacitor) which maybe counter-intuitive to the traditional approach of increasing the value of the

capacitance to present an AC short circuit at the desired RF input frequency.

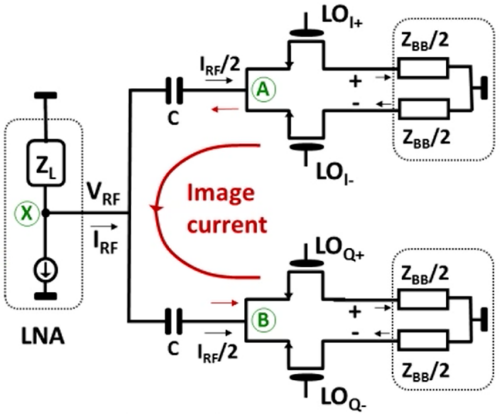

Figure 5.16: A current-driven passive IQ mixer with 50% duty-cycle LO waveforms

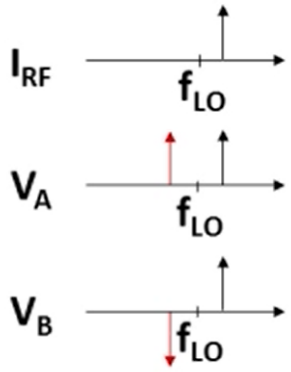

Figure 5.17: Spectra of the RF current, voltage at node A and voltage at node B

5.4.3 25% and 50% Duty-Cycle Clocks

Current-driven passive IQ mixers utilizing 25% duty-cycle LO clocks are proved to be superior to their 50% duty-cycle counterparts. One of the advantages is that their conversion gain is higher by 3 dB. This can be shown intuitively as the LO component of the 25% duty-cycle square wave is lower by 3 dB than its 50% counterpart but at the same time, in the 25% duty-cycle mixer, the switches in two quadrature channels are not simultaneously on as shown in Fig. 5.18 unlike those in the 50% duty-cycle mixer, the switches in two quadrature channels are simultaneously on for quarter of the LO period which results in the division of the RF current between the 2 channels (6 dB loss in conversion gain) as shown in Fig. 5.19. This leads to an overall improvement of 3 dB in the conversion gain of the 25% duty-cycle mixer and also, the two channels do not load each other.

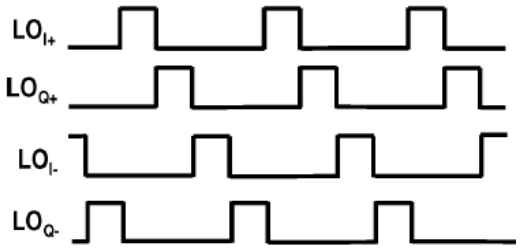

Figure 5.18: 25% duty-cycle quadrature clocks

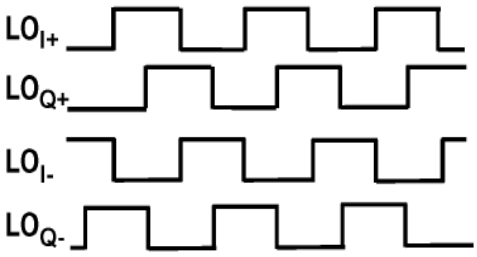

Figure 5.19: 50% duty-cycle quadrature clocks

Other advantages of the 25% duty-cycle mixer relative to the 50% counterpart are that it lowers the noise contribution of the buffer, lowers the image current, improves the balance between the high-side and low-side conversion gains and lowers the IQ cross-talk. The only disadvantage is that it requires the generation of 25% duty-cycle quadrature LO waveforms which will consume more power.

A mixer utilizing 25% duty-cycle LO waveforms is shown in Fig. 5.20, it should be noted that unlike the 50% duty-cycle counterpart, only one ac coupling capacitor is used and that is because, as stated above, the switches in two quadrature channels are not simultaneously on.

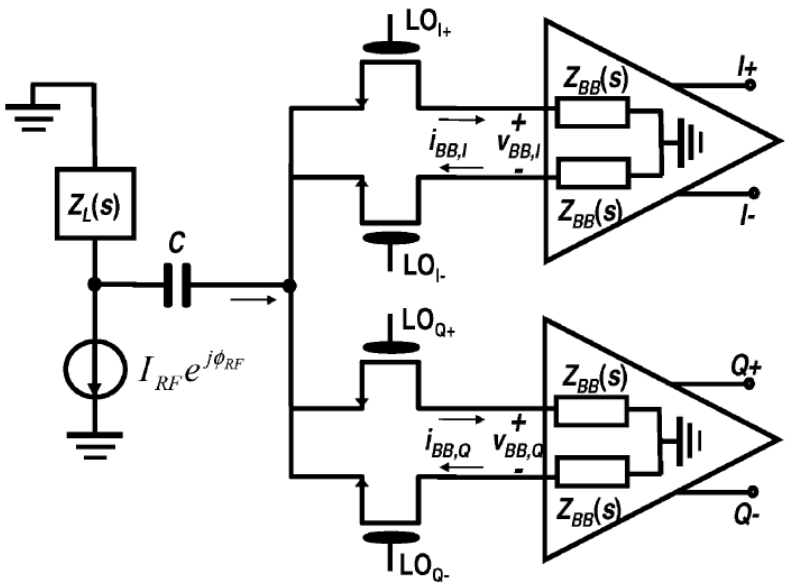

Figure 5.20: A current-driven passive IQ mixer with 25% duty-cycle LO

The transfer function from the RF current to the baseband current is shown in eq. 5.2 and the detailed analysis can be found in [2].

$$\frac{I_{BB,I}}{I_{RF}} = \frac{e^{-j\frac{\pi}{2}} I_{BB,Q}}{I_{RF}} = \frac{\frac{\sqrt{2}}{\pi} Z_L(\omega_{LO}) e^{j(\phi_{RF}-\frac{\pi}{4})}}{Z_L(\omega_{LO}) + Z_C(\omega_{LO}) + R_{SW} + \frac{2}{\pi^2} Z_{BB}(\omega_m)} \tag{5.2}$$

Thus, the conversion gain ideally approaches a constant value of $\frac{\sqrt{2}}{\pi}$ (-6.93 dB) if the series capacitor impedance at the LO frequency, the resistance of the switch and the baseband impedance at the image frequency are much smaller than the LNA output impedance at the LO frequency. Therefore, as stated above intuitively, the 25% duty-cycle IQ mixer has a 3 dB improvement in the conversion gain relative to that of a 50% duty-cycle IQ mixer that has a conversion gain ideally approaching a constant value of $\frac{1}{\pi}$ (-9.94 dB).

It should also be noted that the definition used for the baseband currents in the proposed design is different from that in eq. 5.2. The equation defines $i_{BB}(t) = i_{BB,+}(t) - i_{BB,-}(t)$, while in our proposed design, $i_{BB}(t) =$

$i_{BB,+}(t) = -i_{BB,-}(t)$, therefore the current conversion gain is lower than that in eq. 5.2 by 6 dB and ideally approaches a constant value of $\frac{1}{\sqrt{2}\pi}$ (-12.95 dB). Both definitions lead to the same baseband differential voltage as in the first definition, $V_{BB}(s) = I_{BB}(s) \times Z_{BB}(s)$, while in the second definition, $V_{BB}(s) = I_{BB}(s) \times 2Z_{BB}(s)$.

5.4.4 Impedance Transformation

Due to the lack of reverse isolation in a current-driven passive mixer, the baseband voltages are up-converted to the RF node leading to the impedance transformation property. For an IQ current-driven passive mixer with 25% duty-cycle clocks as shown in Fig. 5.20, it can be shown that the input impedance seen from the RF node is actually the switch resistance in series with the baseband impedance shifted to the integer harmonics of the LO frequency along with a scaling factor. In the vicinity of the LO frequency, the input impedance can be simplified as shown in eq. 5.3.

$$Z_{in}(\omega) \approx R_{SW} + \frac{2}{\pi^2}[Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})] \tag{5.3}$$

Therefore, the system transfers a low-Q (quality factor) baseband impedance to a high-Q RF impedance simply by frequency shifting as shown in Fig. 5.21. This can be utilized as an on-chip high-Q RF band-pass filter in a variety of applications.

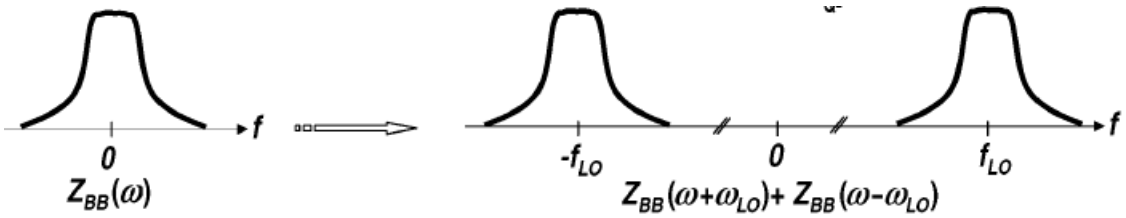

Figure 5.21: The baseband impedance up-converted to the LO frequency

5.4.5 Noise

There are three regions of operation for the current-driven passive mixer which are OFF overlap, zero overlap and ON overlap. Overlap refers to a window in time around the LO zero crossings where two FETs are either both ON or both OFF. If $V_G > V_B + V_{th}$, the mixer operates in ON overlap as shown in Fig. 5.22 but if $V_G < V_B + V_{th}$, the mixer operates in OFF overlap as shown in Fig. 5.23 where V_G is the bias voltage at the gate of the mixer switches, V_B is the voltage at the source terminal and V_{th} is the threshold voltage. Current-driven passive mixers are best operated in ON overlap because in OFF overlap, large voltage swings appear at the input of the mixer due to the charging of the capacitor at this node which will degrade the linearity performance of the mixer.

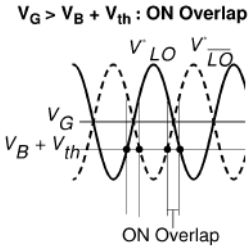

Figure 5.22: ON Overlap mode of operation

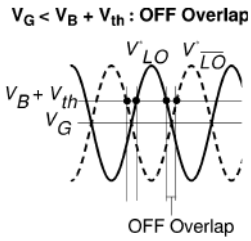

Figure 5.23: OFF Overlap mode of operation

5.4.5.1 Flicker Noise

Only the blockers located at special frequencies determine the flicker noise, therefore the switch flicker noise in a current-driven passive mixer appears at the output only in special cases. So, if the passive mixer is used in a narrowband receiver, where the faraway blockers are removed before reaching the mixer, the core of the current-driven passive mixer will not create any baseband flicker noise.

5.4.5.2 White Noise

During the non-overlap time, one switch is OFF so it contributes no noise and the other switch is ON so its current is fixed by the RF input trans-conductance stage and it also contributes no noise. Therefore, the switches contribute noise to the mixer output only during the overlap time when they are both ON. The single-sided baseband current noise spectrum for the single-balanced mixer is shown in eq. 5.4 and the detailed analysis can be found in [3].

$$S_{ino} = \frac{16(4kT\gamma)}{3S \times T_{LO}} \beta V_{eff}^2 \tag{5.4}$$

Where V_{eff} = V_G - V_B - V_{th},$\beta = \mu C_{ox} \frac{W}{L}$, S is the slope of the LO signal during the transition and T_{LO} is its period.

5.4.6 Linearity

Linearity of passive mixers in general is superior to that of active mixers as the passive mixer does not suffer from headroom issues. Current-driven

passive mixers have another important feature which is that they have negligible signal swings across the switches which further results in a significantly better linearity. The main cause of nonlinearity in current-driven passive mixers is the nonlinear switch resistance.

5.4.7 Effect of Parasitic Capacitances on TIA Noise

In many receivers, the TIA is implemented using a feedback-based op-amp as shown in Fig. 5.24. The resistance seen at the op-amp input terminals (R_p) is actually a switched capacitor resistor where the total parasitic capacitance at the RF side (C_p) is charged and discharged at the LO frequency resulting in a resistor with a value given by 5.5.

$$R_p = \frac{1}{4 f_{LO} C_p} \tag{5.5}$$

Thus, the op-amp input referred noise is transferred to the output with a transfer function given by 5.6.

$$\overline{v_o^2} = (1 + \frac{2R_f}{R_p})^2 \, \overline{v_{amp}^2} \tag{5.6}$$

Therefore, to minimize this noise, the op-amp noise and the total parasitic capacitance C_p have to be minimized employing limits in the design of the LNA and the mixer.

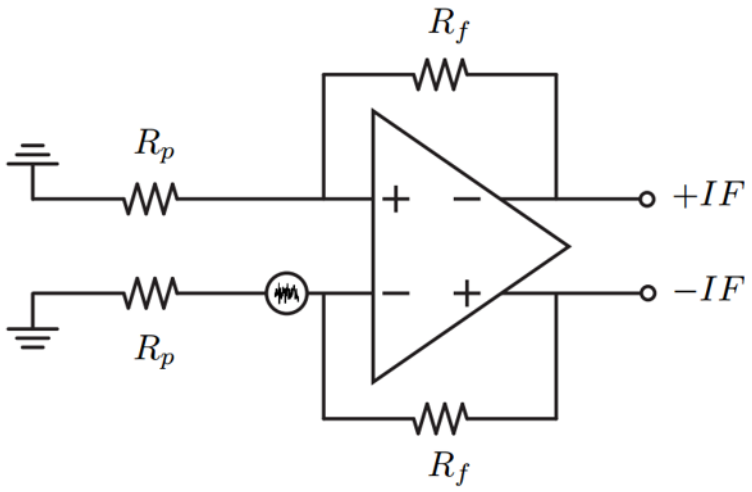

Figure 5.24: TIA implemented using a feedback-based op-amp

5.5 Design of the Proposed Down-Conversion Mixer

5.5.1 Required Specifications

According to the system design, it was required to design the down-conversion mixer achieving the following specifications shown in Table 5.3.

Table 5.3: Required specs from the down-conversion mixer

Parameter	**Specification**
Conversion Gain	> -16 dB
Noise Figure	< 61 dB
IIP_3	> 50 dBm
Current Consumption	< 360 μA

The RF bandwidth of operation is from 2.4 GHz up to 2.48 GHz with 1 or 2-MHz IF channels, also the design should guarantee proper operation in typical conditions and across PVT corners.

It should be noted that the spec on the NF is actually 58 dB but because the receiver is an image-reject receiver employing an IQ mixer followed by a complex filter, the NF of the mixer is expected to be enhanced by 3 dB due to the complex filter image filtering nature.

5.5.2 Topology Selection

From the above specs, it is noted that the specs on the gain and NF are relaxed while the spec on the IIP_3 is much tightened. Therefore, the passive topology is chosen for the design. Also from the system architecture, the system employs a low noise trans-conductance amplifier with a single-ended output before the mixer and a differential trans-impedance amplifier after the mixer so that the internal nodes are low impedance nodes as this lowers the voltage swings and improves the overall linearity of the receiver chain. The LNA is chosen to be single-ended to avoid using RF baluns in the matching network whether passive to decrease the number of components or active due to issues with their Monte Carlo performance. Also, the LO-IF feedthrough present in the single-balanced topology will not be a problem as the receiver is a low-IF receiver so the LO frequency is much higher than the IF frequency. Therefore, the down-conversion mixer is chosen to be a current-driven passive single-balanced IQ mixer with 25% duty cycle LO waveforms.

5.5.3 Design Procedure

The proposed down-conversion mixer was designed using TSMC 65nm CMOS process technology and simulated using Cadence Virtuoso Spectre-

RF simulator. The design parameters are the sizing of the mixer switching transistors, the value of the series ac coupling capacitor, the topology of the LO drivers generating the 25% duty-cycle quadrature waveforms and the sizing of their transistors. The design is started by analyzing the effect of the mixer switch size on conversion gain, NF and linearity assuming ideal LO waveform generators and then choosing the optimum size that achieves the required specs with enough margins to guarantee proper performance across PVT corners. Also, the effect of increasing the capacitance of the ac coupling capacitor is analyzed and a proper value is selected. After that, the LO driver gates are implemented and sized based on the optimum switch size selected for the mixer core transistors.

5.5.4 Selecting the Optimum Switch Size

The test-bench is shown in Fig. 5.25, the LNA is modeled by a VCCS with an output resistance of 5KΩ parallel with an output capacitance of 20fF. C_c is the ac coupling capacitor between the LNA and the mixer and it is implemented using a mimcap from the kit. The single-ended input impedance of the TIA consists of a 500Ω resistor parallel with a 1pF capacitor. The current flowing into the resistor is sensed and multiplied by the trans-resistance gain of the TIA which is equal to 120KΩ to generate the IF voltages in both the I and Q channels. The trans-conductance of the VCCS that models the LNA is set to be 8.33μS ($\frac{1}{120K\Omega}$) so that the total gain from the RF voltage to the IF voltage is equal to the current conversion gain of the mixer only. DC voltage sources with large inductors are used to set the common-mode input voltage of the TIA to 0.5V. The LO generators are implemented using pulse voltage sources with rise and fall times equal to 1% of LO period.

The length (L) of all the RF transistors used for the mixer switches and the LO drivers is chosen to be 60nm which is the minimum length in the process.

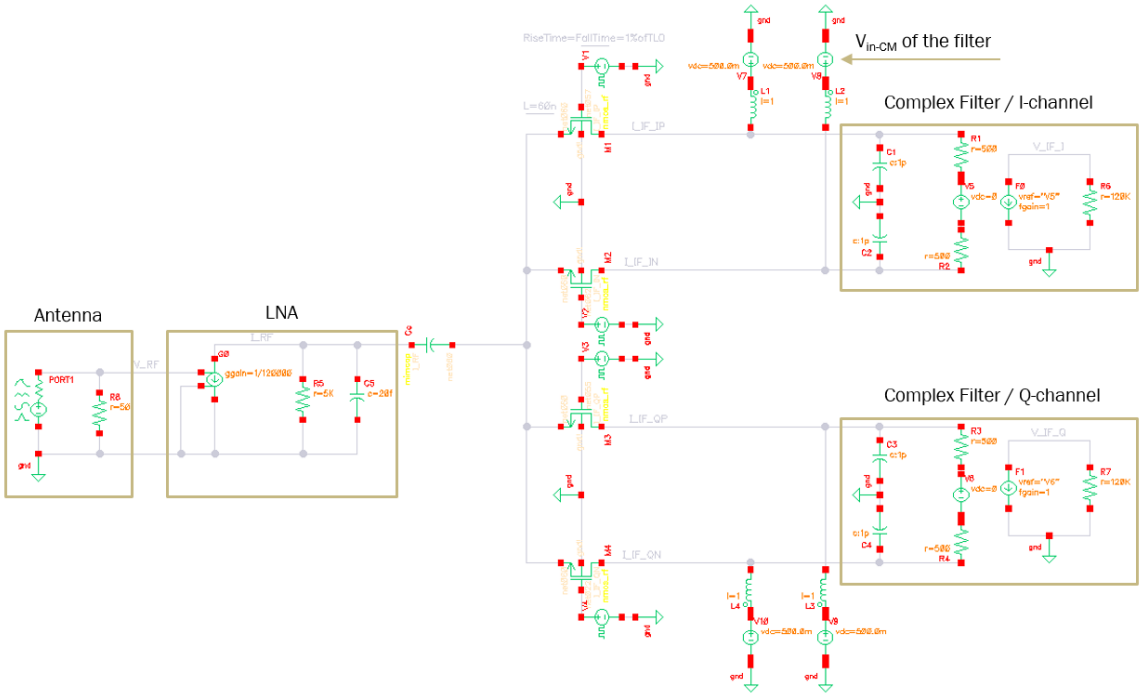

Figure 5.25: Test-Bench of the mixer switches with ideal LO waveform generators

The LO frequency used is 2.439 GHz, the conversion gain is simulated using periodic steady state analysis (PSS) with periodic ac analysis (PAC) sweeping the RF frequency from 2.44 GHz to 2.442 GHz for the high-side conversion gain and from 2.436 GHz to 2.438 GHz for the low-side conversion gain. The NF is simulated using PSS with periodic noise analysis (pnoise). The IIP_3 is simulated using quasi-periodic steady state analysis (QPSS) with the two tones at 2.437 GHz and 2.434 GHz.

5.5.4.1 Effect of Switch Width on Conversion Gain

The conversion gain is selected at 3MHz IF frequency as it is the worst case conversion gain. Before W=2.5μm, the conversion gain is enhanced due to decreasing the on-resistance of the mixer switches (R_{on}) but after W=2.5μm, the conversion gain is degraded due to increasing the capacitive load at the RF input of the mixer as shown in Fig. 5.26.

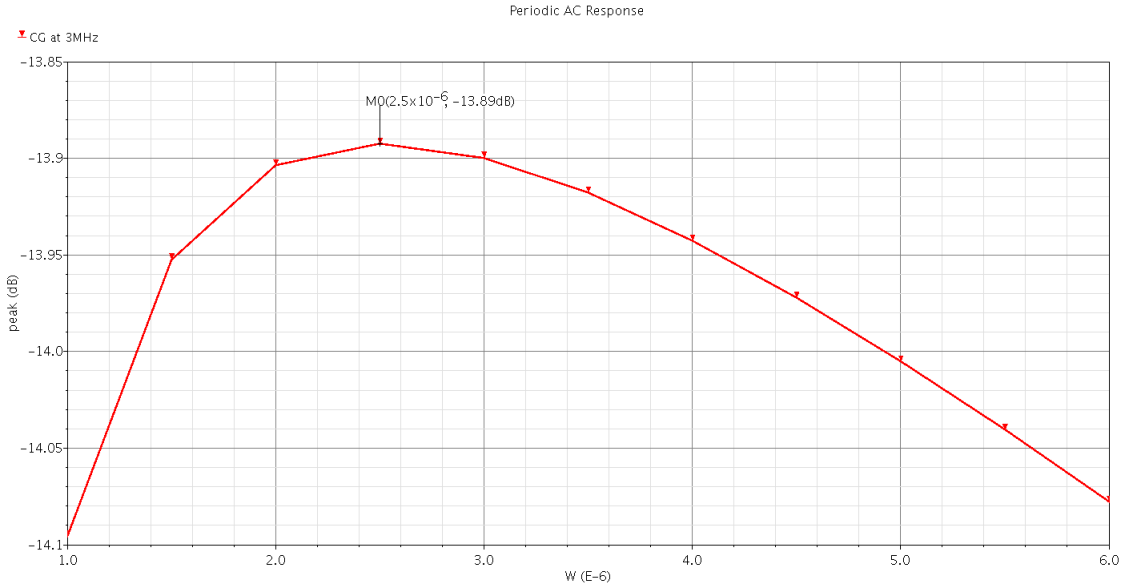

Figure 5.26: Effect of switch width on conversion gain

5.5.4.2 Effect of Switch Width on Noise Figure

The noise figure is selected at 1MHz IF frequency as it is the worst case noise figure.

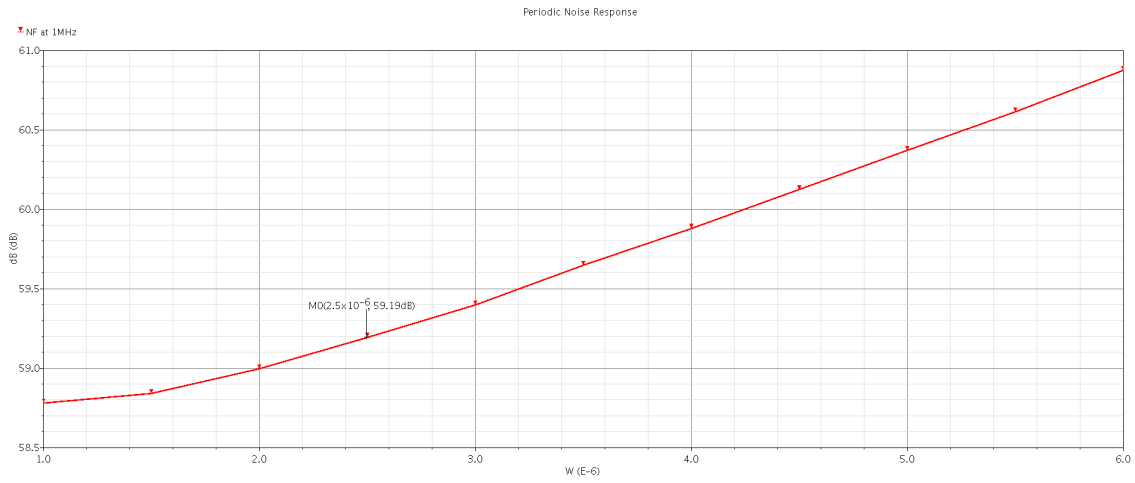

Figure 5.27: Effect of switch width on noise figure

From Fig. 5.26 and Fig. 5.27, the optimum width size of the mixer core switches is chosen to be 2.5μm as it has the highest conversion gain and it achieves the noise figure spec with about 2 dB margin.

5.5.4.3 IIP_3 and P_{1dB} at 2.5μm Switch Size

As shown in Fig. 5.28, IIP_3 is approximately equal to 64 dBm, so it achieves the spec with a 14 dB margin.

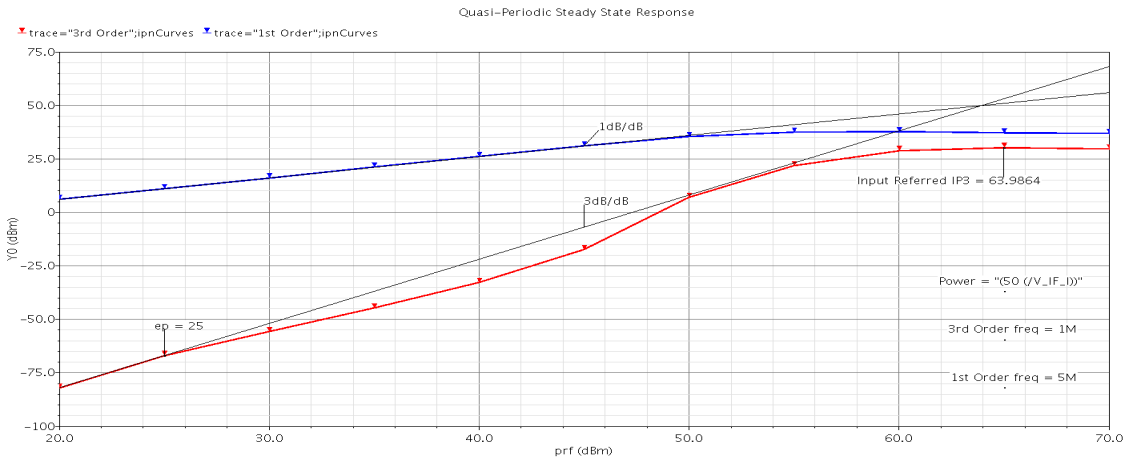

Figure 5.28: IIP_3 at 2.5μm Switch Size

As a rule of thumb, the P_{1dB} should approximately be 10 dB below the IIP_3 which is verified in Fig. 5.29.

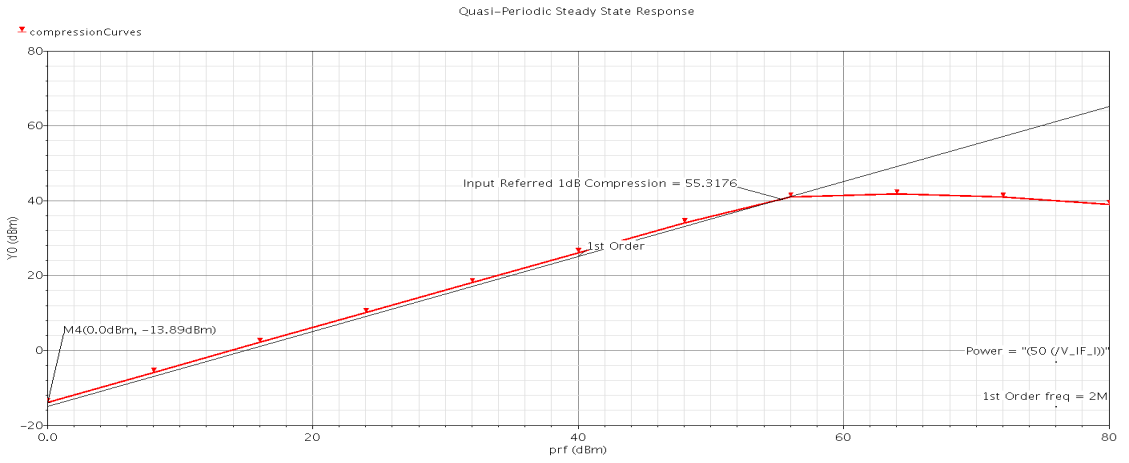

Figure 5.29: P_{1dB} at 2.5μm Switch Size

5.5.4.4 Effect of Switch Width on Parasitic Capacitances

As mention in subsection 5.4.7, as the parasitic capacitances (Cp) at the output of the LNA increase, the output noise of the TIA increases. Therefore, it is required from the mixer to not add a large parasitic capacitance at the output of the LNA and this affects the selection of the switch size. As shown in Fig. 5.30, at 2.5μm switch size, C_p is approximately equal to 37fF which means that the mixer transistors add about 17fF parasitic capacitances to the 20fF required from the LNA output capacitance and this is acceptable.

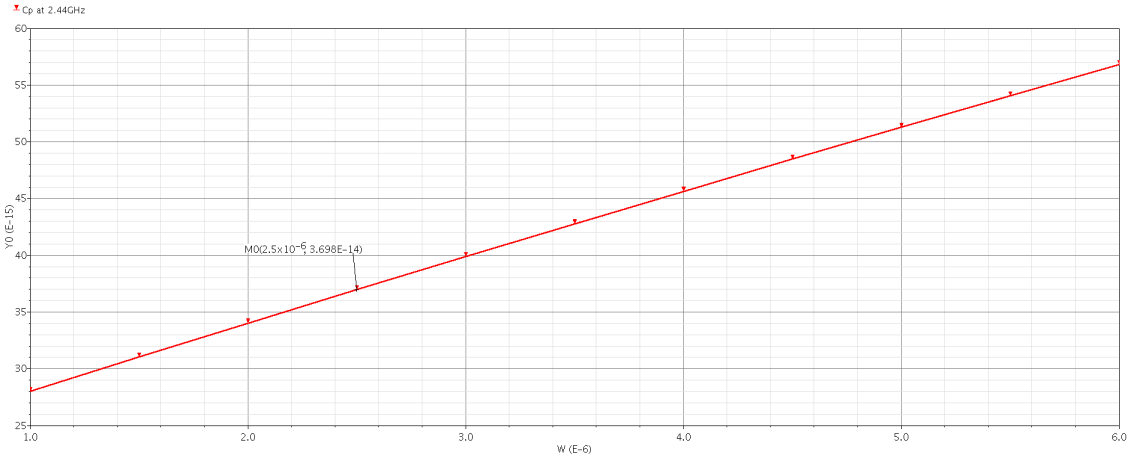

Figure 5.30: Effect of switch width on C_p

5.5.5 Selecting the Value of the AC Coupling Capacitor (C_c)

5.5.5.1 Effect of C_c on conversion gain

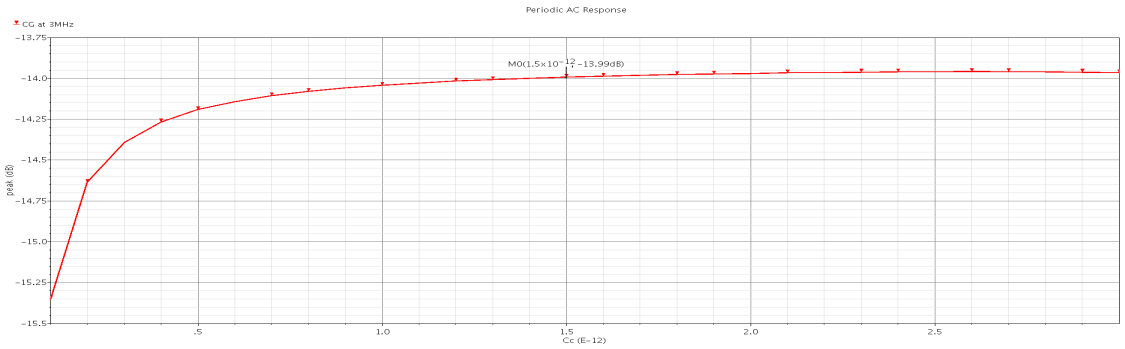

Figure 5.31: Effect of C_c on conversion gain

5.5.5.2 Effect of C_c on noise figure

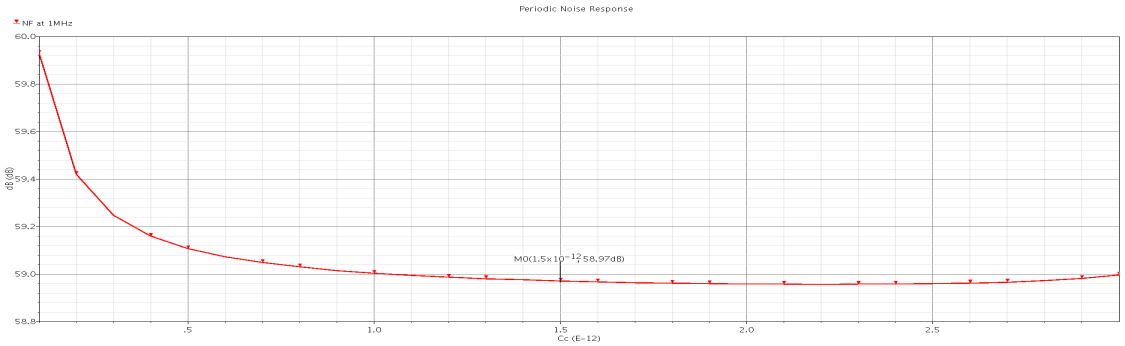

Figure 5.32: Effect of C_c on noise figure

From Fig. 5.31 and Fig. 5.32, the value of the ac coupling capacitor between the LNA and the mixer is selected to be 1.5pF as beyond this value, the conversion gain and noise figure are degraded rapidly and above this value, they don't see much improvement.

5.5.6 Implementing the 25% Duty-Cycle LO Driver Gates

The frequency divider in the receiver produces 50% duty-cycle quadrature LO waveforms with rise time and fall time equal to 10% of the LO period. The 25% duty-cycle waveforms are generated using CMOS AND gates where each two 50% duty-cycle waveforms with 90^o phase shift between them generate a 25% duty-cycle waveform with the output being high at the quarter of the LO period in which the two waveforms are overlapping and both high. The symbol of the AND gate is shown in Fig. 5.33 and its schematic is shown in Fig. 5.34. A first order high-pass filter is implemented after each AND gate using a mim capacitor and a poly resistor to set the DC bias voltage for the gates of the mixer core switches. The sizing of the AND gates entails a trade-off between the delay and the power consumption noting that the delay, or in other words the slope of the transition regions, will affect the conversion gain and noise figure of the mixer due to the increase in the overlap times.

Figure 5.33: Symbol of the AND gate

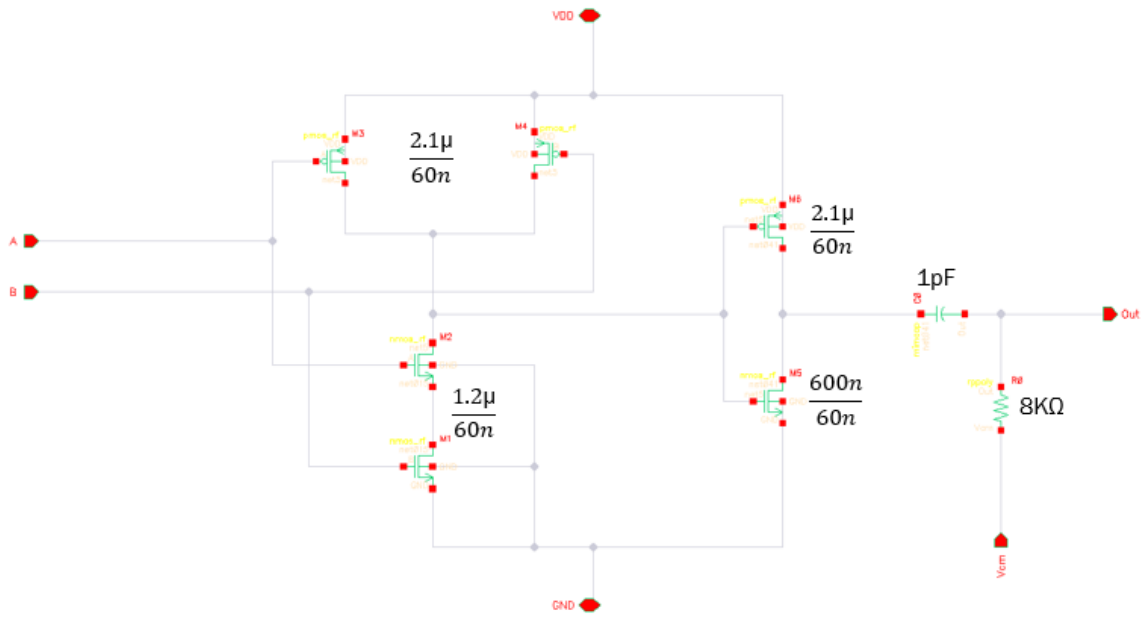

Figure 5.34: Schematic of the AND gate and sizing of the components

The sizing of the driver gates is optimized taking into consideration the stated trade-off and also, it should be noted that the driver gates should not load any single-ended output of the frequency divider with more than 20fF and this is achieved as shown in Fig. 5.35.

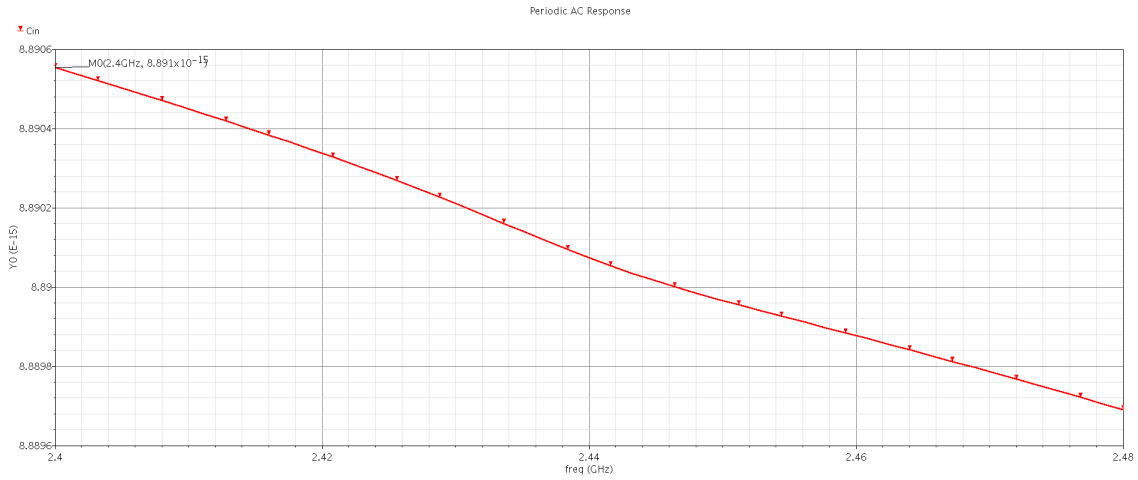

Figure 5.35: Input capacitance seen at any single-ended output of the frequency divider

5.6 Typical Simulation Results of the proposed Down-Conversion Mixer

5.6.1 Test-Bench

The supply voltage used is 1V and V_{cm} is 0.5V.

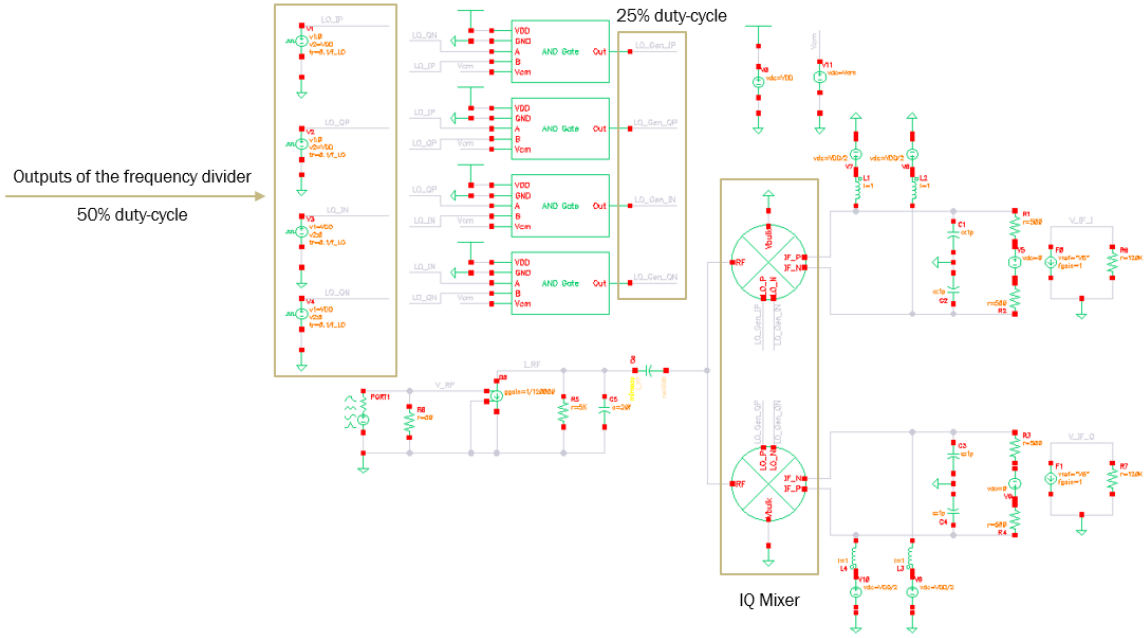

Figure 5.36: Test-bench of the proposed down-conversion mixer

5.6.2 LO Waveforms

The overlap time between each two phases should be minimized as it causes degradation of the conversion gain and noise figure. As shown in Fig. 5.38, the rise time is equal to 32.5psec (8.125% of the LO period at 2.5 GHz) and the fall time is equal to 29.5psec (7.375% of the LO period at 2.5 GHz).

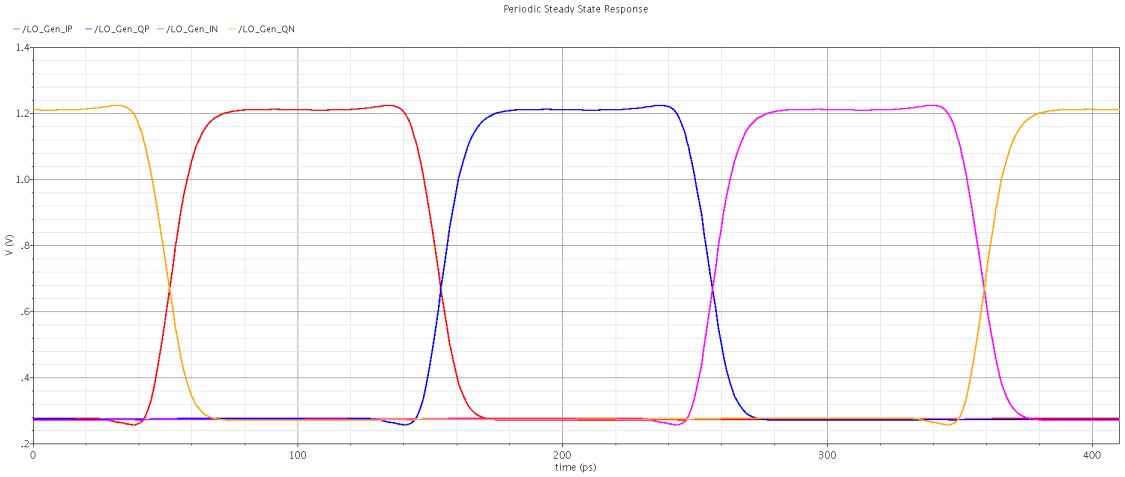

Figure 5.37: The 25% duty-cycle quadrature LO waveforms

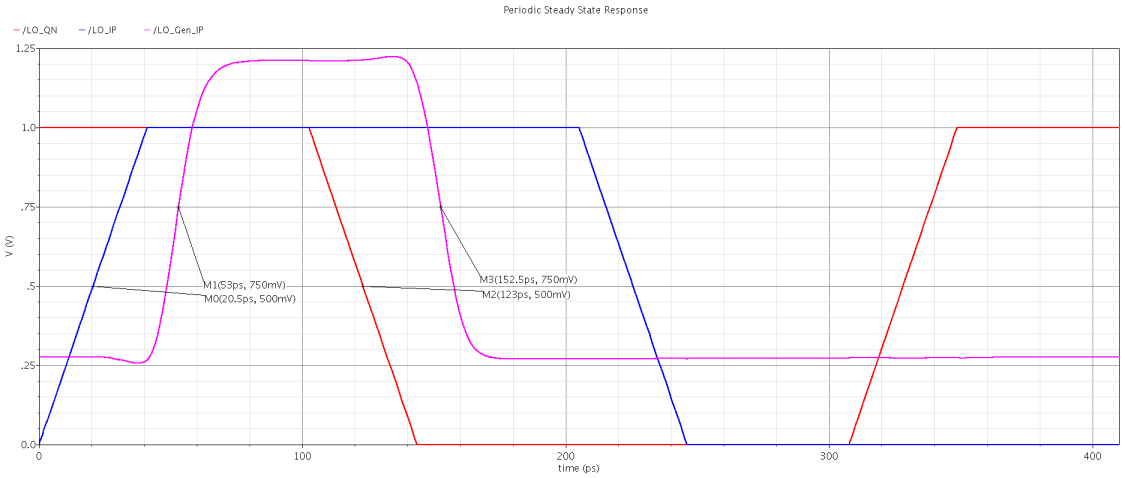

Figure 5.38: The generation of one 25% duty-cycle LO waveform

5.6.3 Current Conumption

The current consumption is the average of the waveform shown in Fig. 5.39 and it is equal to 264.7 μA.

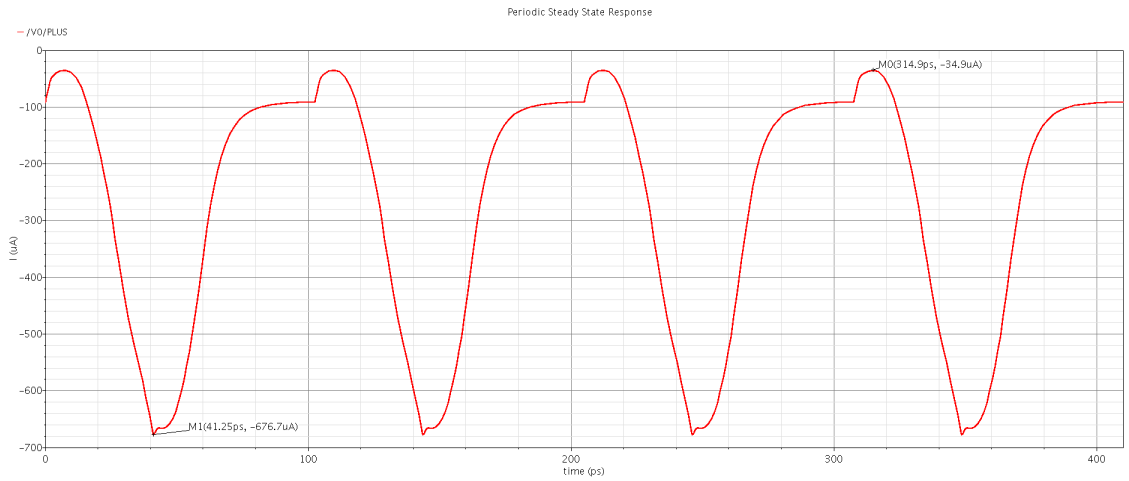

Figure 5.39: Transient current drawn from the supply in one LO period

5.6.4 Conversion Gain

As shown in Fig. 5.40, the spec is achieved with about 2 dB margin and the balance between the high-side and low-side conversion gains across the IF channel is very good due to the use of the 25% duty-cycle clocks.

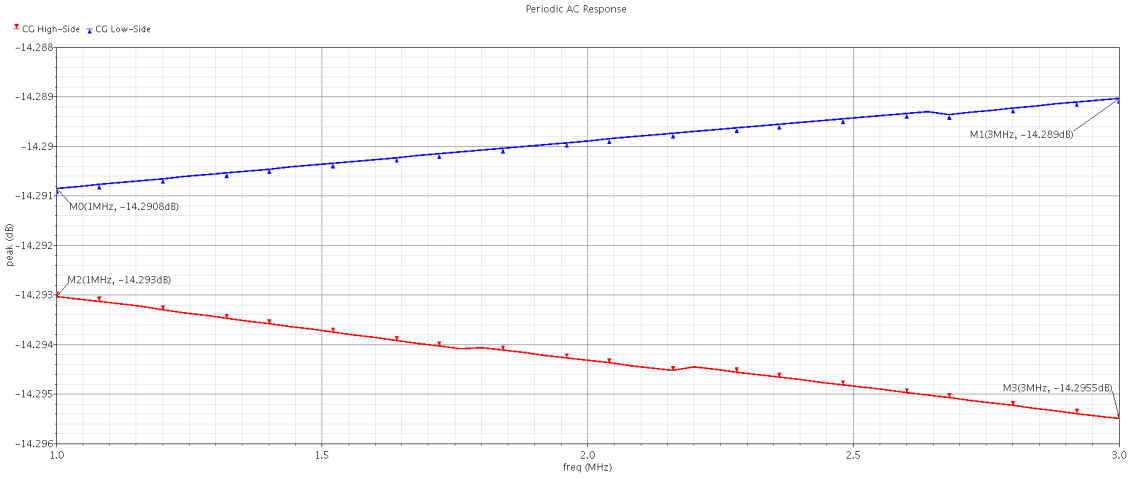

Figure 5.40: High-Side and Low-Side conversion gains in typical conditions

5.6.5 Noise Figure

As shown in Fig. 5.41, the spec is achieved with about 2 dB margin.

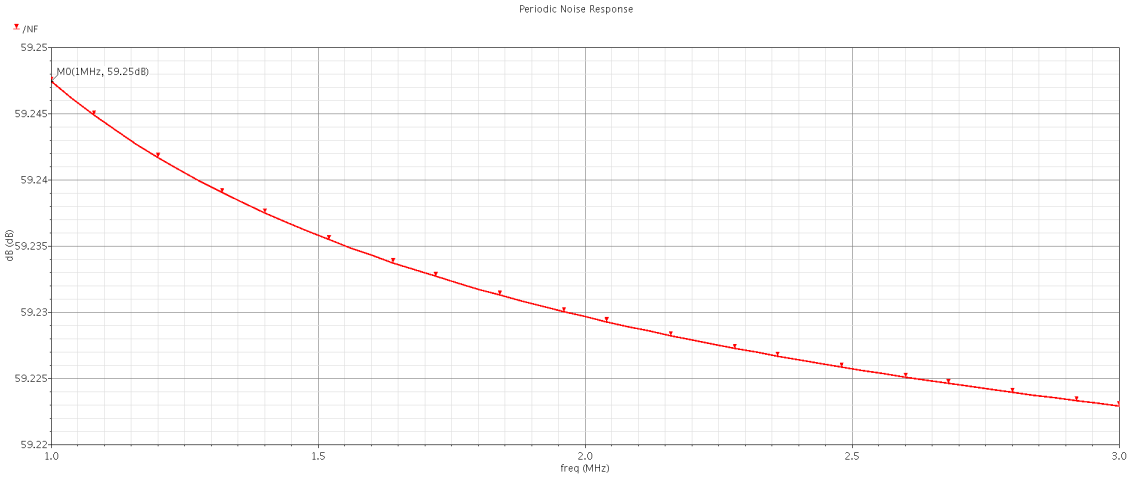

Figure 5.41: Noise Figure in typical conditions

5.6.6 IIP_3 and P_{1dB}

As shown in Fig. 5.42, the spec is achieved with 7 dB margin.

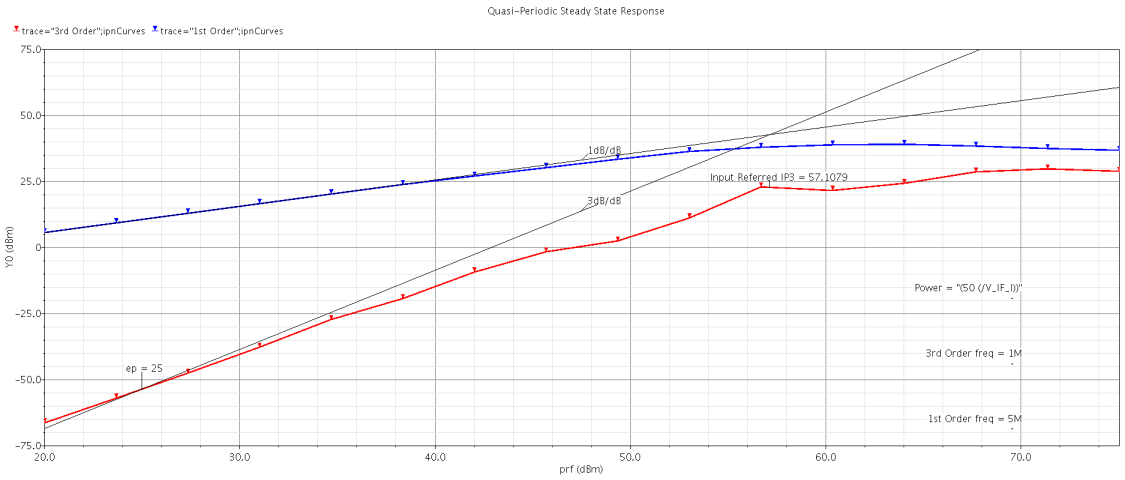

Figure 5.42: IIP_3 in typical conditions

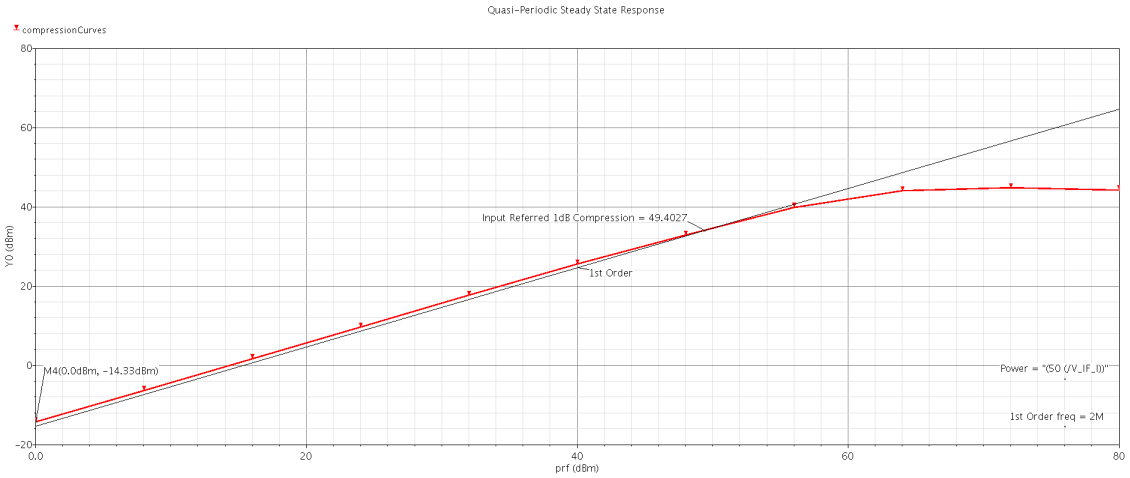

Figure 5.43: P_{1dB} in typical conditions

5.6.7 Summary of Typical Simulation Results

Table 5.4: Summary of typical simulation results of the proposed down-conversion mixer

Parameter	**Spec**	**Achieved**	**Unit**
Conversion Gain	> -16	-14.3	dB
Noise Figure	< 61	59.25	dB
IIP_3	> 50	57.1	dBm
P_{1dB}	> 40	49.4	dBm
Current Consumption	< 360	264.7	μA

5.7 Corners Simulation Results of the proposed Down-Conversion Mixer

64 PVT corners were simulated according to Table 5.5.

Table 5.5: Simulated PVT corners

Variation	**Corners**
Temperature	{ -40^oC , 125^oC }
Supply	{ 0.95V , 1.05V }
RF Transistors	{ FF , FS , SF , SS }
MIM Capacitors	{ FF , SS }
Poly Resistors	{ FF , SS }

5.7.1 LO Waveforms

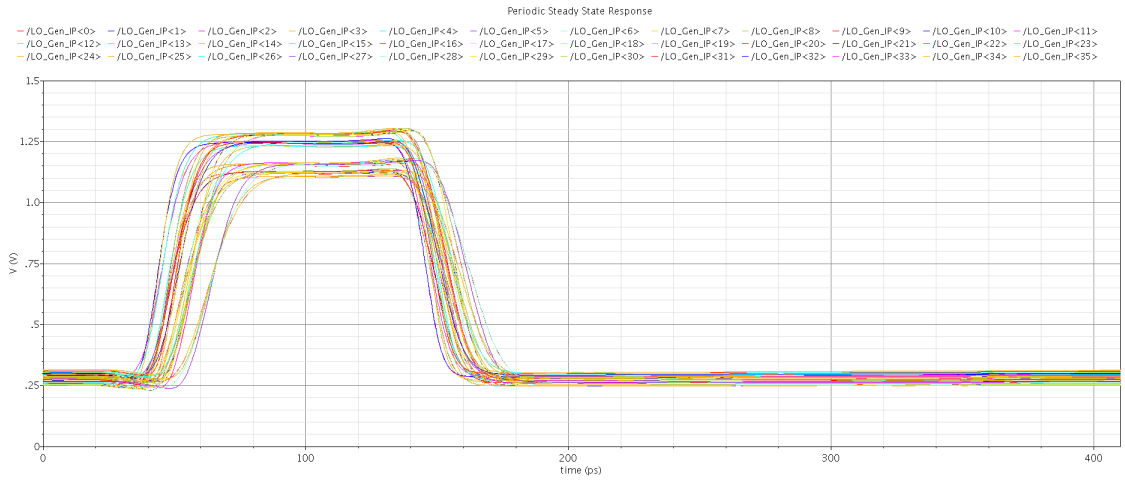

Figure 5.44: Variations of one phase of the 25% duty-cycle LO waveforms across corners

5.7.2 Current Consumption

The spec is achieved across all corners as shown in Fig. 5.45. Most of the corners that result in high current consumption are the high supply / fast resistor corners as higher supply leads to higher current drawn and smaller resistance value leads to larger equivalent capacitance seen at the output of the driver gates leading to the same result.

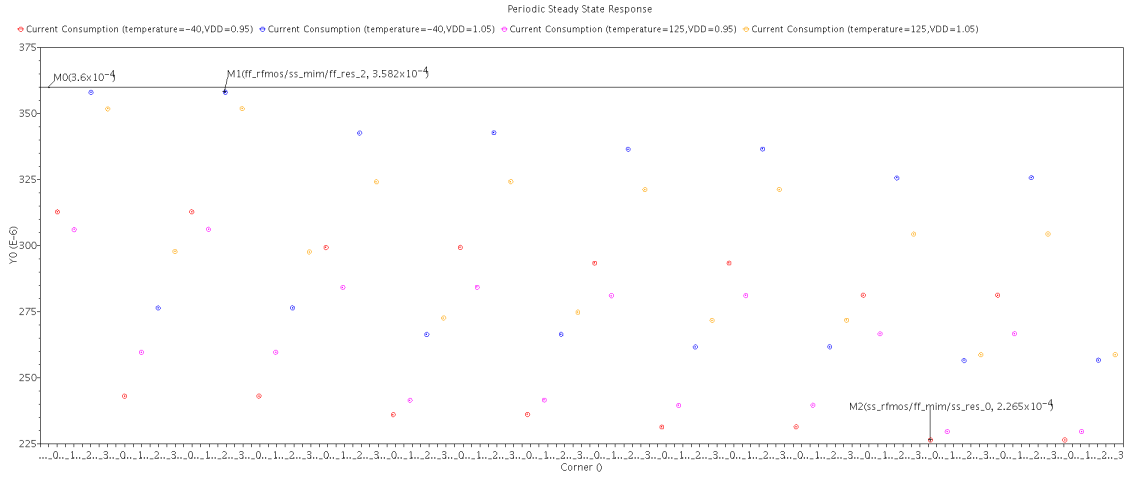

Figure 5.45: Current consumption across corners

5.7.3 Conversion Gain

The spec is achieved across all corners as shown in Fig. 5.46. Most of the corners that result in low conversion gain are the low supply corners as this increases the on-resistance of the mixer switches, the effect is the worst in transistors-SS corner due to the increase in the threshold voltage.

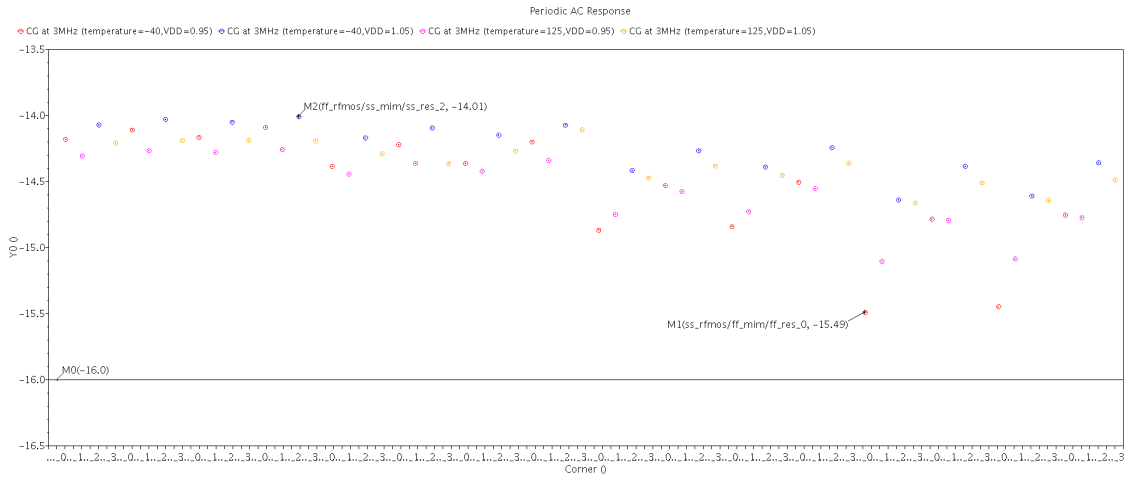

Figure 5.46: Conversion gain at 3 MHz across corners

5.7.4 Noise Figure

The spec is achieved across most corners as shown in Fig. 5.47. Most of the corners that result in high noise figure are the high temperature corners as this increases the thermal noise of the resistors and the white noise of the mixer switches.

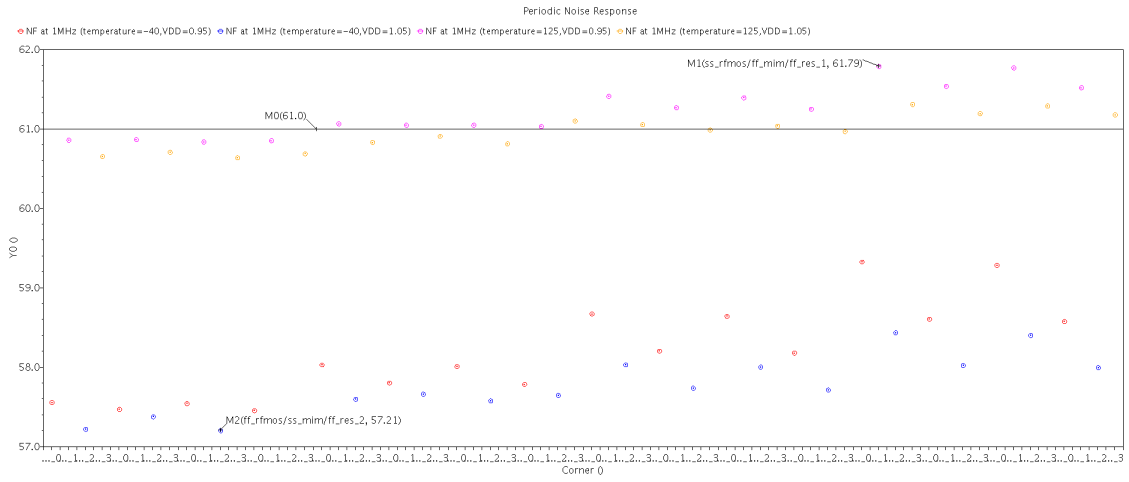

Figure 5.47: Noise Figure at 1 MHz across corners

5.7.5 IIP_3 and P_{1dB}

The spec is achieved across most corners as shown in Fig. 5.48.

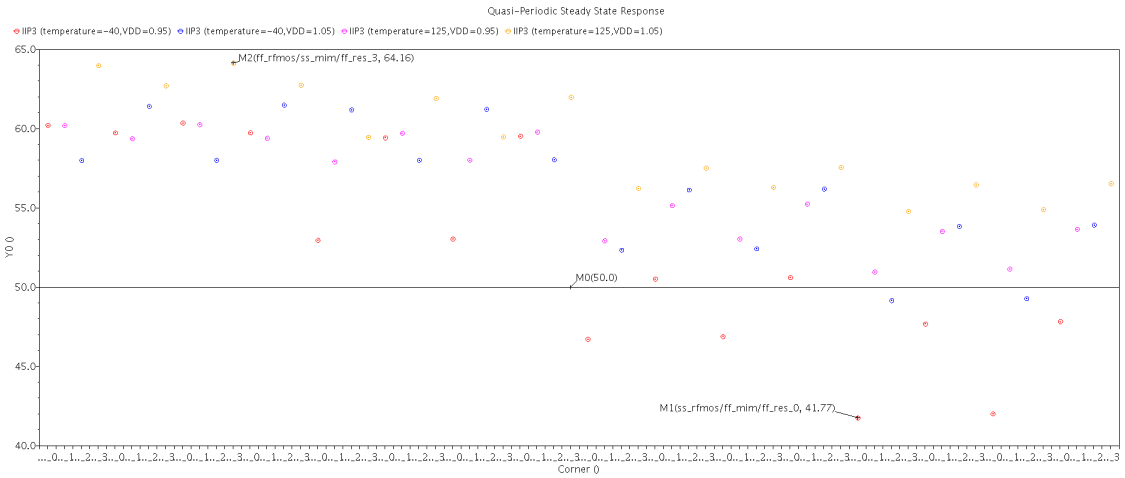

Figure 5.48: IIP_3 across corners

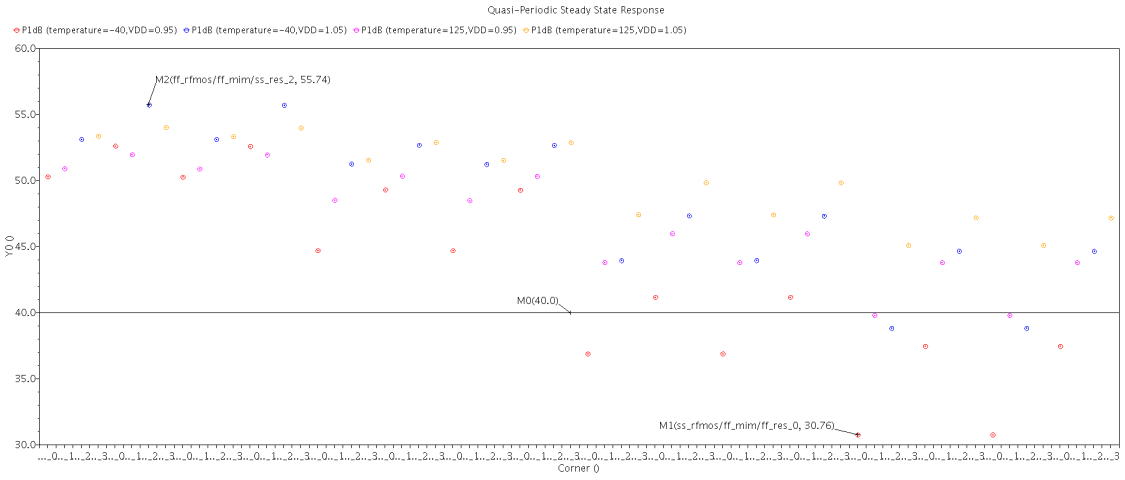

Figure 5.49: P_{1dB} across corners

5.7.6 Summary of Corners Simulation Results

Table 5.6: Summary of corners simulation results of the proposed down-conversion mixer

Parameter	**Spec**	**Min**	**Max**	**Mean**	**Stddev**	**Unit**
Conversion Gain	> -16	-15.49	-14.01	-14.43	314.4m	dB
Noise Figure	< 61	57.21	61.79	59.54	1.618	dB
IIP_3	> 50	41.77	64.16	56.06	5.038	dBm
P_{1dB}	> 40	30.76	55.74	47.11	5.789	dBm
Current Consumption	< 360	226.5	358.2	283.2	36.85	μA

5.8 Summary of Specifications in Typical, Worst and Best Corners

Table 5.7: Summary of specs in typical, worst and best corners

Parameter	**Spec**	**Typical**	**Worst Corner**	**Best corner**	**Unit**
Conversion Gain	> -16	-14.3	-15.49	-14.01	dB
Noise Figure	< 61	59.25	61.79	57.21	dB
IIP_3	> 50	57.1	41.77	64.16	dBm
P_{1dB}	> 40	49.4	30.76	55.74	dBm
Current Consumption	< 360	264.7	358.2	226.5	μA

5.9 Conclusion

Mixers are essential blocks in any wireless transceiver, they are difficult to analyze and have unique features due to their nonlinearity and time variance behavior. Their performance parameters are mainly the conversion

gain, noise figure, linearity, port-to-port feedthrough and power consumption. They can be categorized into up-conversion or down-conversion mixers, single-balanced or double-balanced mixers, active or passive mixer, voltage-driven or current-driven mixers. In this work, current-driven passive mixers have been studied, they have different unique features like IQ crosstalk and impedance transformation property. The effect of changing the duty-cycle of the LO waveforms on their performance has been studied and also their effect on the output noise of the following TIA has been studied. A single-balanced down-conversion current-driven passive IQ mixer with 25% duty-cycle LO waveforms and the driver gates generating these waveforms have been designed (according to a proposed design procedure) for the Bluetooth low energy (BLE) standard version 5.1 in a TSMC 65nm CMOS process and simulated using Spectre-RF. The proposed down-conversion mixer has been optimized to meet the required specifications in typical conditions and across PVT corners.

5.10 Future Work

- Improving the linearity of the mixer across corners.
- Design of a bandgap circuit that generates the bias voltage for the mixer switch gates.
- Performing Monte Carlo Simulation to study the effect of mismatch on the performance.
- Layout of the design and performing post layout simulations.

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Chapter 6: Complex Filter

6.1 Overview

Low-IF receivers have many advantages that makes them favorable for BLE technology. It avoids the main issues of the direct-conversion receivers namely, the DC offset resulting from the self-mixing at the down-conversion mixer, also the high flicker noise near the DC and up to the corner frequency which is mostly avoided. In the Low-IF receivers, the signal is down-converted by a single sinusoid signal as shown in Fig. 6.1. The main disadvantage here is that an unwanted signal located at the image frequency (which is located at $2f_{IF}$ away from the wanted signal) gets down-converted to the same IF frequency as the wanted signal. Thus, to avoid corrupting the wanted signal, an RF bandpass filter should be placed (before the down-conversion mixer) to suppress the image signal. However, the Q of such a filter is proportional to f_{RF}/f_{IF}. Such high Q filters (SAW or ceramic filters) are bulky and requires input and output impedance matching which usually raises the power consumption. In addition to that, the IF frequency can't be made arbitrarily small due to the limited Q of the external filter, and hence, raising the power consumption of the circuits operating at the IF frequency.

One of the solutions to this problem is to multiply the RF signal by only an exponential (ie:$e^{j\omega_{LO}}$). As shown in Fig. 6.2, this will solve the problem of the image signal corrupting the wanted signal. However, the main problem here is that the exponential signal $e^{j\omega_{LO}}$ is a complex signal which consists of the real part $cos(\omega_{LO})$ and the imaginary part $-sin(\omega_{LO})$. In order to implement the complex multiplication using real components, two signal branches I and Q must be constructed. In the I branch (in-phase), the RF signal is

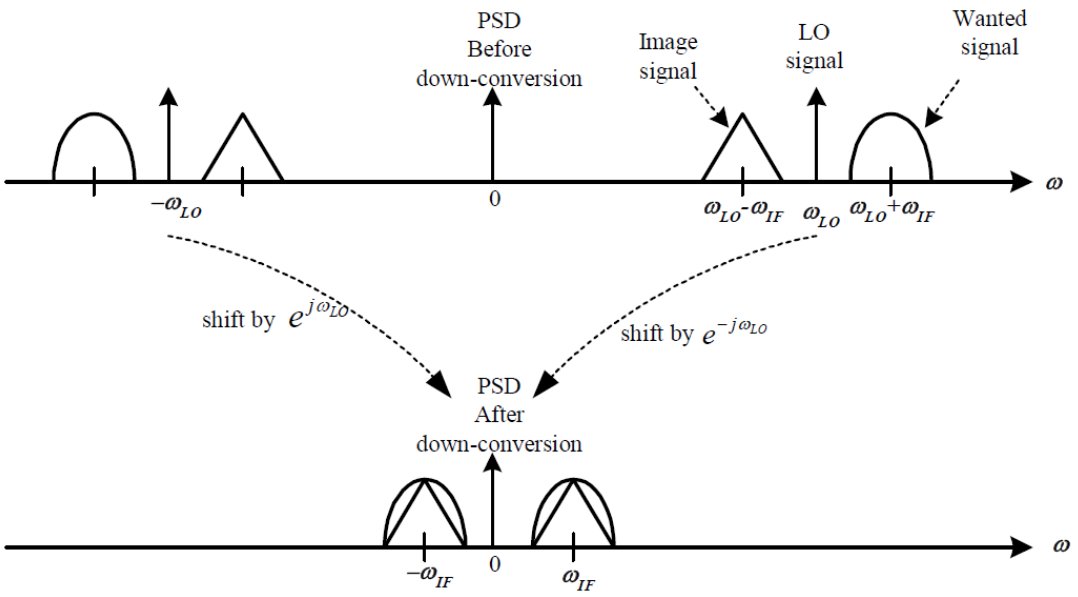


Figure 6.1: Single sinusoid down-conversion operation

multiplied by $cos(\omega_{LO})$. While in the Q branch (quadrature-phase), the RF signal is multiplied by $cos(\omega_{LO})$. This complex down-conversion operation is demonstrated In Fig. 6.3, it is worth-mentioning that both the I and Q branches has the down-converted signal containing the wanted and image signal both at ω_{IF}. However, the complex signal $I_o + jQ_o$ has the wanted signal at ω_{IF} and the image signal at $-\omega_{IF}$, the image signal can be rejected by means of a complex filter as will be discussed in the following section. Thus, the same filter is used for image rejection as well as channel selectivity. Therefore, the Q of the filter is proportional to $\omega_{IF}/BW_{channel}$, which is small for small IF frequencies.

Although the low-IF architecture solve the problems of the DCR and high-IF architectures. However, it has some inherent issues as well. Namely, its capability to reject the image signal is limited by the mismatch between the I and Q branches and the quadrature LO outputs, this effect is quantified in the following section.

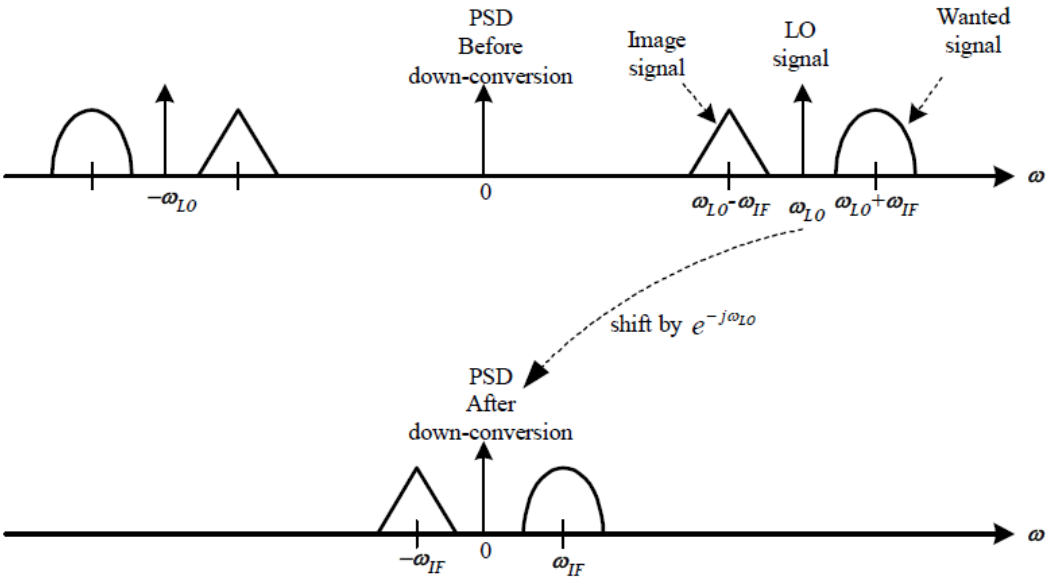


Figure 6.2: Exponential down-conversion operation

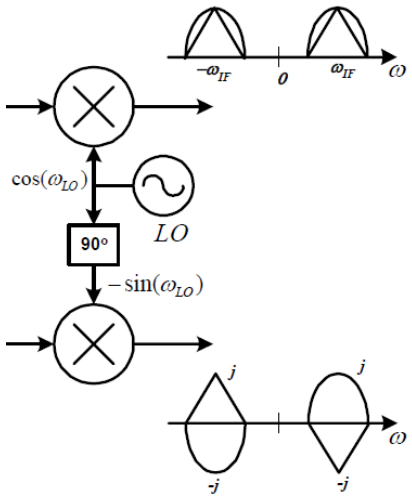


Figure 6.3: Basic low-IF mixer diagram

6.2 Complex filter theory

As aforementioned, quadrature low-IF receiver architecture down-converts the RF signal using only an exponential, as shown in Fig. 6.2. A complex filter can be then implemented to select the desired channel at ω_{IF} and reject the image at $-\omega_{IF}$. To explain the implementation of such a filter, a brief theoretical discussion follows.

For the sake of illustration, we will assume that only the desired signal and the image signal are present at the mixer input. Without loss of generality, we will assume that the desired signal and the image signal frequencies are $\omega_{LO}+\omega_{IF}$ and $\omega_{LO}-\omega_{IF}$, respectively. Thus, the result of mixing the LO and RF signals in the complex domain is as follows:

$$B = G_{mixer}(x_{sig}e^{j\omega_{IF}t} + x_{image}e^{-j\omega_{IF}t}) = B_I + jB_Q \tag{6.1}$$

This is equivalent to the following equations in the real domain:

$$\begin{aligned} B_I &= G_{mixer}(x_{sig}cos(\omega_{IF}) + x_{image}cos(\omega_{IF})) \\ B_Q &= G_{mixer}(x_{sig}sin(\omega_{IF}) - x_{image}sin(\omega_{IF})) \end{aligned} \tag{6.2}$$

The complex channel-select filter is then a frequency-shifted version of a low-pass filter response, as illustrated in Fig.6.4. This means that the filter can pass the signal at ω_{IF} and attenuates the signal at $-\omega_{IF}$. Since the filter response is asymmetrical around the $j\omega$-axis, its time domain response is complex, hence comes the name complex filter. However, the complex filter frequency response is symmetrical around ω_{IF}. Since the

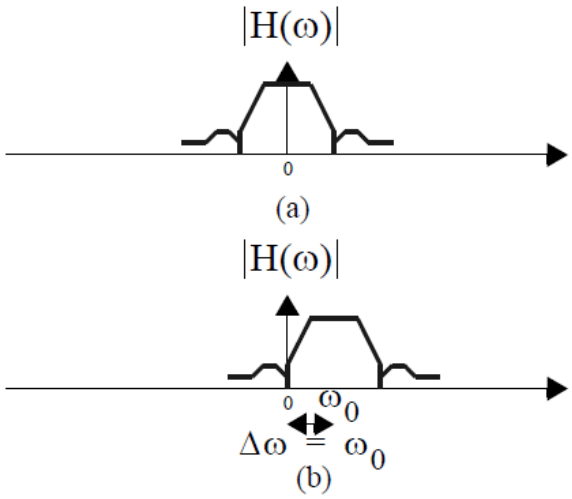


Figure 6.4: (a) A base-band prototype magnitude filter response and (b) the magnitude response of a complex filter obtained by the substitution $S > S - j\omega_o$.

blocking specifications of a receiver around the desired frequency ω_{IF} are symmetrical, this is considered an advantage of the complex filter over the real BPF that has asymmetrical frequency response around its center frequency.

The complex multiplication of the RF signal by $e^{j\omega_{LO}}$ is practically performed using a quadrature mixer, which basically consists of two mixers whose LO inputs are in quadrature phase, as shown in Fig. 6.5. In the real implementation shown in Fig. 6.5, the desired (image) signal in the I branch leads (lags) the Q branch by $90°$. Phase and magnitude imbalances at the mixer output due to LO and mixer mismatches, will cause the image signal at $-\omega_{IF}$ to spill over the desired signal band at ω_{IF}. As a result, the filter ability to reject the image will be limited by these mismatches, this is quantified by the image-rejection ratio (IRR) which is described as follows

$$IRR_{max}(dB) \approx 10log[sin(\theta/2)^2 + (\Delta/2)^2] \tag{6.3}$$

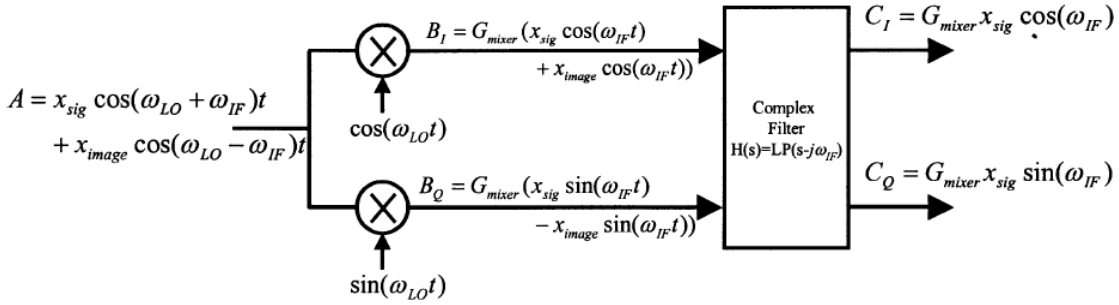


Figure 6.5: Practical implementation of the image-reject receiver architecture.

Where, θ and Δ are the phase and magnitude imbalances, respectively.

As aforementioned, the complex BPF is a frequency-shifted version of a real LPF. To convert an arbitrary LPF to a complex BPF centered at ω_{IF}, every frequency-dependent element in the LPF should be altered to be a function of $S - j\omega_{IF}$ instead of S. The basic frequency-dependent element of a filter is an integrator. Consider the simple case of converting a first-order LPF with cut-off frequency ω_{LP}, to a complex BPF with center frequency ω_{IF}. Thus, the shifted LPF transfer function is as follows

$$X_o = \frac{\omega_o}{S + \omega_{LP} - j\omega_{IF}} X_i \tag{6.4}$$

Where $X_o = X_{oI} + jX_{oQ}$ and $X_i = X_{iI} + jX_{iQ}$. Then, from the previous equation

$$\begin{aligned} X_{oI} &= \frac{\omega_o}{S + \omega_{LP}}\left(X_{iI} - \frac{\omega_{IF}}{\omega_o} X_{oQ}\right) \\ X_{oQ} &= \frac{\omega_o}{S + \omega_{LP}}\left(X_{iQ} + \frac{\omega_{IF}}{\omega_o} X_{oI}\right) \end{aligned} \tag{6.5}$$

The previous equations are simply implemented as seen in Fig. 6.6.

For the sake of illustration, an active-RC implementation of the first-order complex filter in Fig. 6.6 is illustrated in Fig. 6.7. Note that an inverting

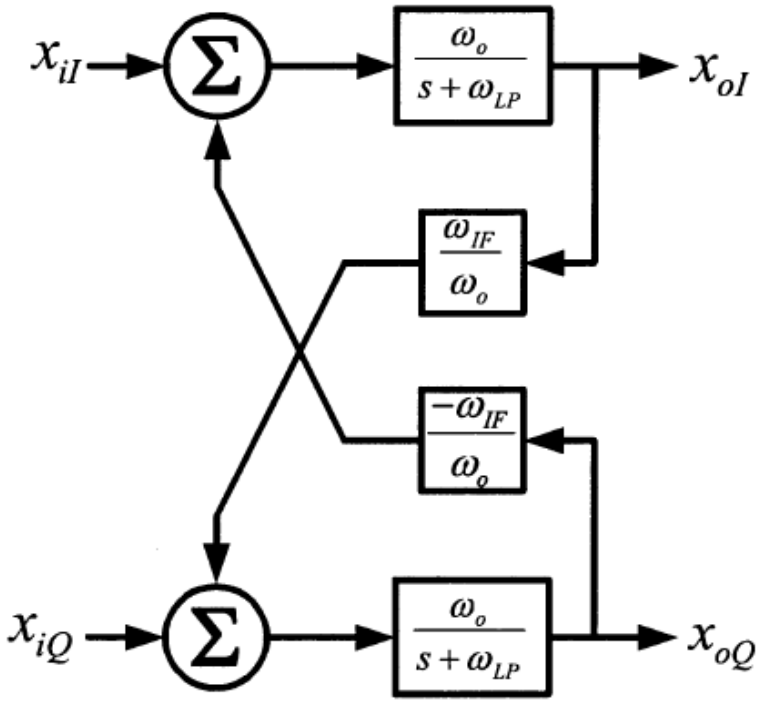


Figure 6.6: Real building-block implementation of a 1^{st}-order complex band-pass filter centered at ω_{IF}.

amplifier is needed in the cross feedback from the Q-branch to the I-branch. In a differential implementation, the inverting amplifier can be avoided by exchanging the differential signals.

6.3 Complex filter implementation

6.3.1 Filter specifications and approximation

A 3^{rd}-order Butterworth specification was pre-determined on the system level design of the BLE receiver. The order of the filter is determined so as to achieve the $C/I_{interference}$ specification defined in the BLE standard. Furthermore, the Butterworth approximation achieves acceptable in-band phase linearity, along with acceptable out-of-band rejection for relatively low

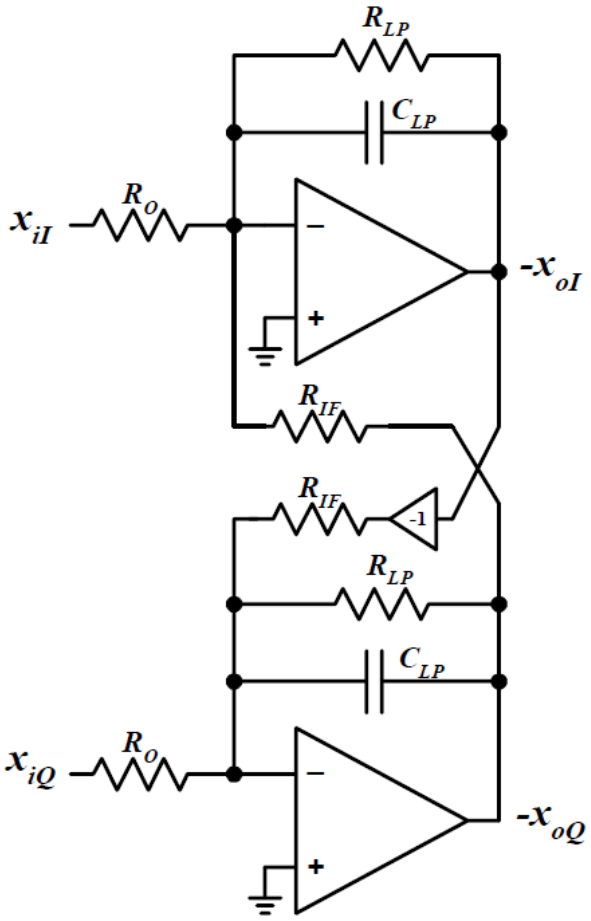


Figure 6.7: Active-RC implementation of the 1st-order complex filter in Fig. 6.6.

Parameter	Specification
Center frequency	1MHz, 2MHz (programmable)
Bandwidth (1dB)	1MHz, 2MHz (programmable)
Passband trans-impedance	$120K\Omega$
Current consumption (typical)	1mA
Load capacitance	1pF
Input impedance	$< 3K\Omega$
IIP3	>30dBm
Noise figure	<50dB
Image-rejection ratio	>9dB

Table 6.1: Complex filter specifications

filter order. The system level specifications of the complex filter are shown in Table 6.1.

6.3.2 Filter implementation

Active conversion of LC ladder implementation is chosen to implement the filter mainly because of its better immunity to component variations and mismatch, compared to the cascade-of-biquads implementation. This is an important issue for the complex filter because the IRR degradation is mainly a function of the mismatch between the I- and Q-paths. Moreover, the Butterworth response is more preserved across the complex filter modes. Therefore, an LC ladder filter implementation is extracted from the normalized tables [1]. The implementation is as shown in Fig. 6.8.

This implementation is then frequency-scaled to obtain the required LPF cut-off frequency. Moreover, it is also impedance-scaled to obtain the required trans-impedance in the active implementation that is discussed later. Table 6.2 shows the values of the capacitors and inductor.

Where, k is a scaling factor to switch the mode of the filter, it is 1 for the 1 MHz-mode and 2 for the 2 MHz-mode. The active implementation of the

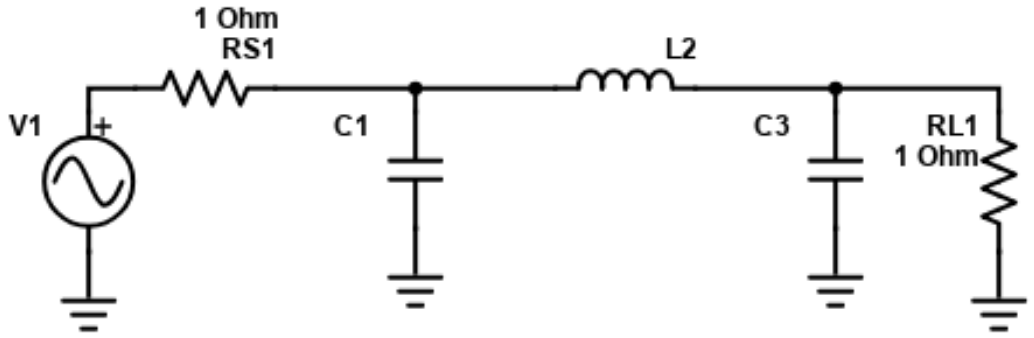


Figure 6.8: LC ladder implementation.

C1	**L2**	**C3**
(3.23/k) pF	(2.95/k) pH	(1.11/k) pF

Table 6.2: LC ladder element values

filter shown in Fig. 6.8 was chosen to be a fully-differential integrator-based opamp-RC implementation for numerous reasons; its feedback configuration allowing for achieving good linearity (low voltage swing on the inputs of the OTAs), as the linearity is a hard specification on the complex filter as shown in table 6.1. Furthermore, the integrator-based opamp-RC implementation is very suitable for discrete-step tuning of the filter to switch between the 1 MHz- and 2 MHz-modes. Switching between the two IF modes is done by replacing each integrator capacitor with a capacitive bank as will be discussed later.

By applying the conventional state equations, the integrator-based opamp-RC implementation of the LC ladder LPF can be obtained, as shown in Fig. 6.9. This filter is a trans-impedance amplifier, it converts the input current to an output voltage.

As previously illustrated in Fig. 6.7, the opamp-RC implementation of a

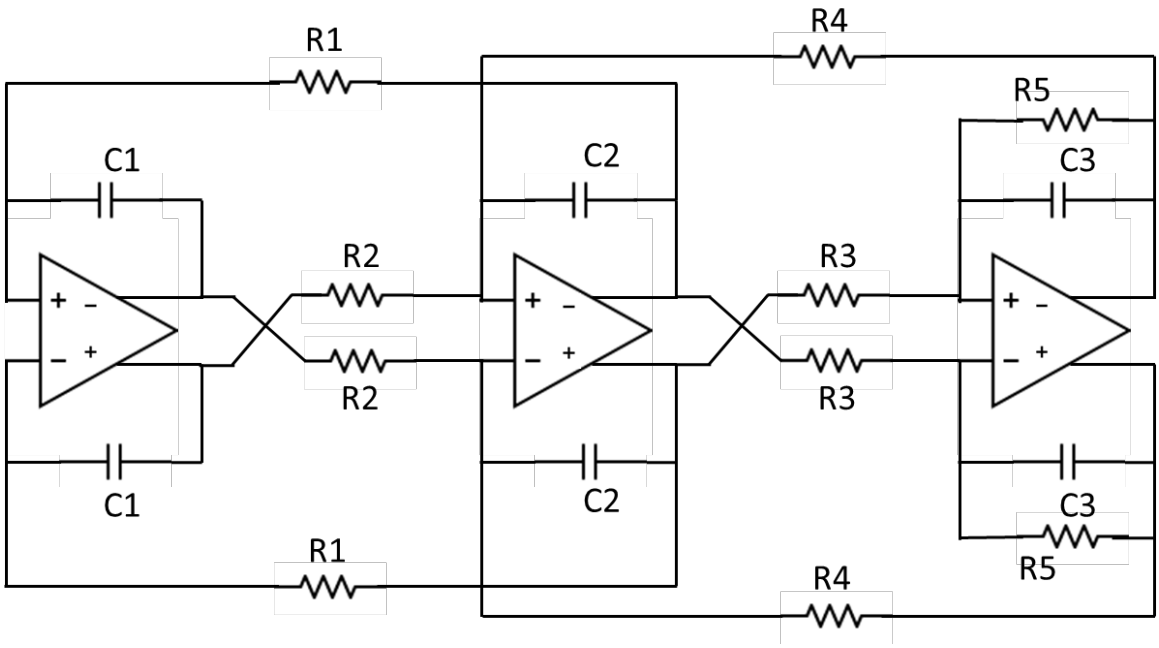


Figure 6.9: Integrator-based Opamp-RC implementation of the 3^{rd}-order Butterworth filter shown in Fig. 6.8.

1^{st}-order complex filter, the same idea can be systematically applied on the 3^{rd}-order opamp-RC LPF, shown in Fig. 6.9, to transform it to a 3^{rd}-order complex filter, as shown in Fig. 6.10. The resistances $R1_{IF}$, $R2_{IF}$, and $R3_{IF}$ transform the LPF, shown in Fig. 6.9, to the complex BPF centered at ω_{IF}. The value of each resistance is determined by the following equation

$$R_{IF} = \frac{1}{\omega_{IF} C_i} \tag{6.6}$$

Where, ω_{IF} is the center frequency of the complex filter, and the C_i is the capacitance of the respective integrator. Table 6.3 shows the values of each component of the filter.

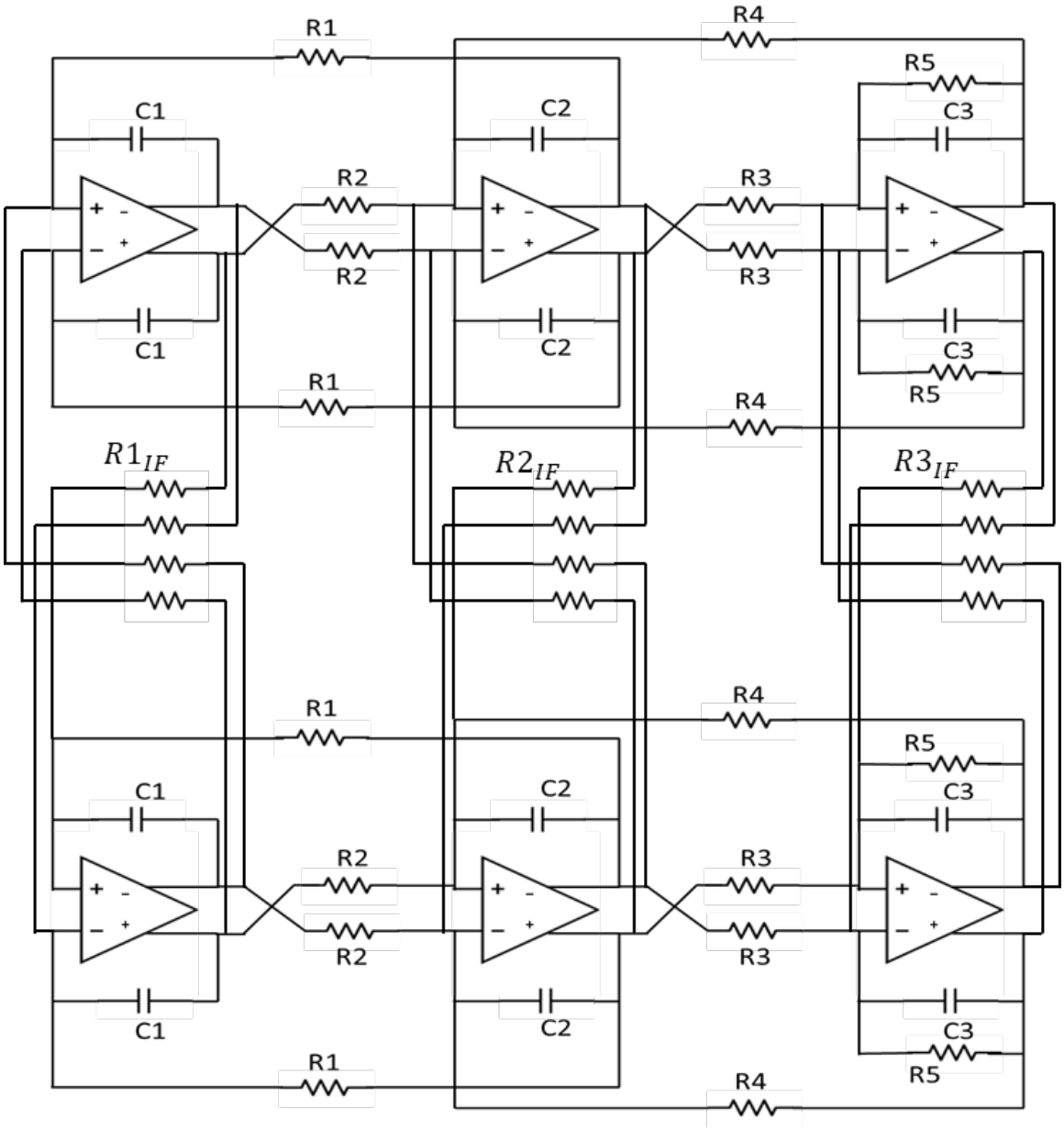


Figure 6.10: A 3^{rd}-order bandpass complex filter centered at ω_{IF}.

Component	Value	Component	Value
R1	$60K\Omega$	$R1_{IF}$	$24.5K\Omega$
R2	$60K\Omega$	$R2_{IF}$	$27K\Omega$
R3	$120K\Omega$	$R3_{IF}$	$144K\Omega$
R4	$60K\Omega$	C1	(6.466/k) pF
R5	$120K\Omega$	C2	(5.893/k) pF
		C3	(1.105/k) pF

Table 6.3: Component values of the 3^{rd}-order bandpass complex filter shown in Fig. 6.10.

6.3.3 OTA topology and CMFB

6.3.3.1 OTA implementation

The design of the OTAs was based on the conventional two-stage OTA [2], shown in Fig. 6.11. The two-stage OTA implementation suits this design for numerous reasons; its high gain capability, partial insensitivity of gain to resistive loading, and its high output swing. Enhanced Miller compensation scheme is also incorporated in the design to enhance the stability of the OTAs.

The design procedure was as follows, the first stage was designed to provide high gain with the input pair sized to maintain the required GBW that provides the required filter response. Hence, relatively low current biases the first stage to achieve high gain, and the desired GBW which is given by $g_{m1,2}/C_c$. Moreover, the second stage was designed to provide low gain to avoid resistive loading, provide high output swing, and to drive the capacitive load and maintain good phase margin, where first non-dominant pole is approximately described by $g_{m5,6}/C_L$. Hence, high current is consumed in the second stage, mainly for stability purposes. The input devices of the second stage $M_{5,6}$ were sized small to avoid loading the first stage and

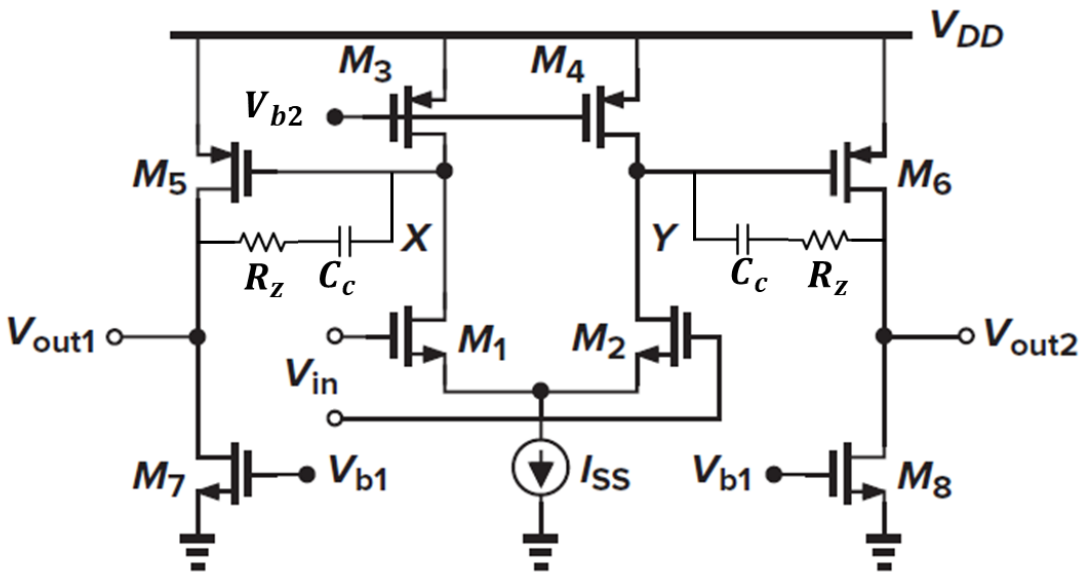


Figure 6.11: Two-stage OTA with enhanced Miller compensation scheme.

limiting the GBW. And finally, the nulling resistor R_z avoids the existence of the RHP zero which proves detrimental for stability, it is chosen such that the RHP zero is moved to the LHP to help enhance the PM of the OTA.

The input devices of the OTA were implemented as low-VT devices. Although that is extra mask during fabrication which means extra cost. However, the use of low-VT devices greatly enhances the overall linearity of the complex filter across PVT corners. That is because, in the cold-slow corner of the 65nm CMOS technology, the threshold voltage can go up to 420mV, and for about 500mV CM level, it results in the biasing current source being pushed into triode region. Thus, necessitating the use of the low-VT devices to achieve the required linearity across corners.

6.3.3.2 OTAs nominal response

The nominal Bode plots of each OTA are shown in Fig. 6.12. These bode plots are obtained for the OTAs existing in the complex filter configuration, which is apparent by the filter poles present around 2 MHz in Fig. 6.12. It can be seen that good loop-gain and PM are obtained.

6.3.3.3 OTAs results summary

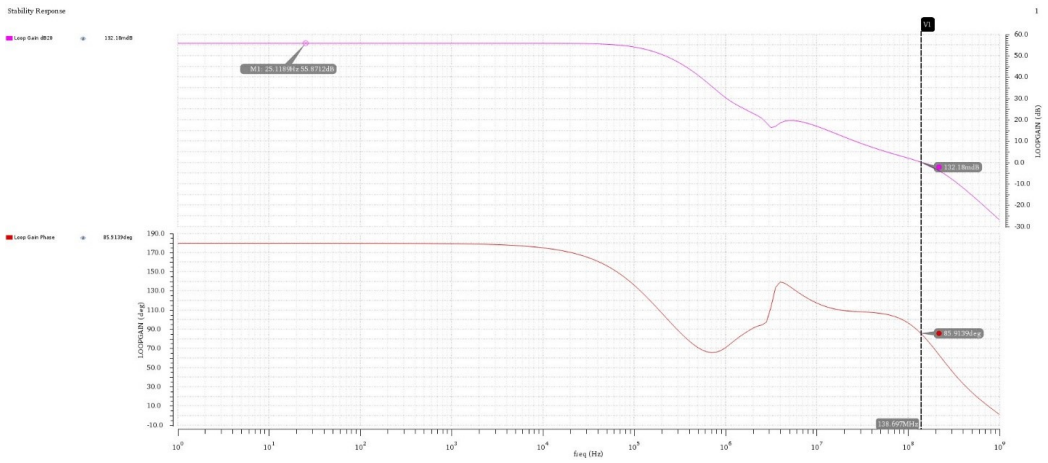
Table 6.4 summarizes the OTAs performance across PVT corners.

	OTA1			**OTA2**			**OTA3**			
	Min	**Typ.**	**Max**	**Min**	**Typ.**	**Max**	**Min**	**Typ.**	**Max**	**Unit**
DC gain	47.62	55.87	59.3	35.9	42.74	50	42.18	47.64	52.62	**dB**
GBW	84.43	138.7	229.2	70.39	96.83	224.8	69.63	87.9	136.2	**MHz**
PM	48.54	85.9	96.6	60.92	93.5	97.5	43.44	72.6	84.12	$^\circ$

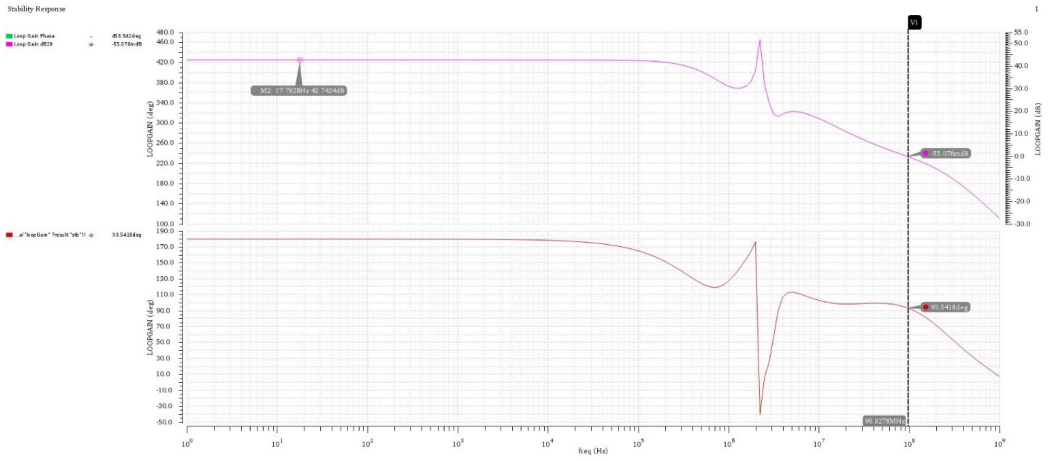
Table 6.4: OTAs summary across PVT corners.

6.3.3.4 CMFB

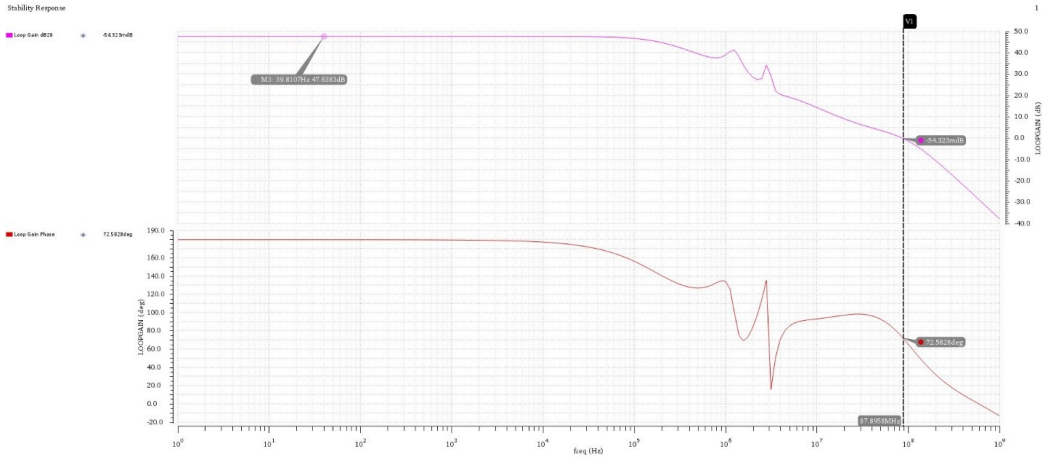
The fully-differential OTA, shown in Fig. 6.11, requires an auxiliary CMFB circuit to maintain the CM voltage level on the differential high-impedance output nodes. The CMFB circuit basically senses the CM level of the output and corrects it by biasing the OTA accordingly to set the output CM level at mid-rail. The CMFB architecture implemented is shown in Fig. 6.13, where each stage of the OTA has its own CMFB circuitry. Although this may look like extra power consumption at first glance. However, this implementation was necessary for various reasons; firstly, each CMFB



(a)



(b)



(c)

Figure 6.12: (a), (b), and (c) are the Bode plots of the first, second, and third integrators opamps, respectively.

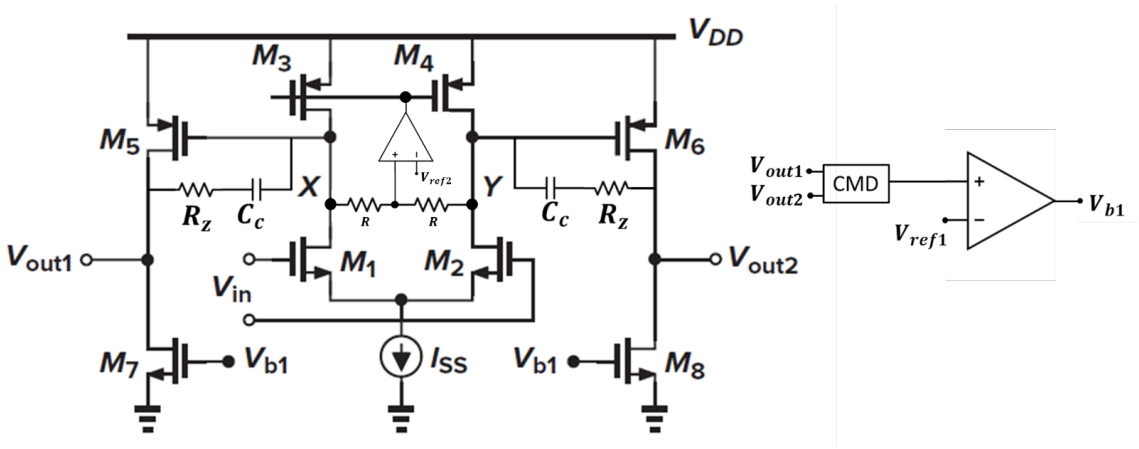


Figure 6.13: CMFB implementation.

loop is simply a two-stage amplifier that can be easily compensated using conventional Miller compensation technique, while maintaining good loop-gain. For a single CMFB loop over the whole two-stage OTA, the loop becomes very complex to compensate and stabilize, while maintaining reasonably high loop-gain. Also, in the context of the complex filter, where each OTA in the I-path is interconnected in feedback configuration with another OTA in the Q-path, there exists positive common-mode feedback loops that may dominate the loop across some PVT corners. Thus, maintaining high loop-gain for the CMFB while stabilizing this complex loop becomes very challenging across PVT corners. Therefore, justifying the use of two CMFB circuits which provide much stable CM levels across PVT corners, as discussed later, while consuming the same power compared to a single CMFB configuration.

The Common-mode detector (CMD) is simply a resistor voltage-divider that senses the average of the differential output of the OTA (the common-mode level). The CMFB OTAs are implemented using a single-ended 5T OTA [2], which provides the needed loop-gain while having good output swing compared to a telescopic implementation. The CMFB OTA biasing V_{b1} is

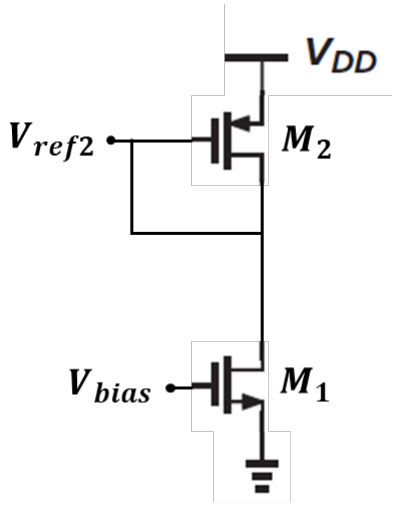


Figure 6.14: Circuit implementation for generating the voltage V_{ref2}.

implemented with PMOS input devices, while the CMFB OTA biasing V_{b2} is implemented with NMOS input devices. Both are implemented as low-VT devices for the same reason mentioned above, which is to ensure proper operation and linearity in the extreme PVT corners.

The voltage V_{ref1} simply comes from a reference band-gap circuit, this voltage is 500mV to maintain a differential CM level at mid-rail, this is done by the CMFB OTA which corrects the V_{gs} voltage of M7 and M8 in Fig. 6.13 such that they maintain the same currents supplied by M5 and M6. Moreover, the voltage V_{ref2} is such that to provide a certain V_{gs} voltage for M5 and M6 of Fig. 6.13 to provide the desired current in the output stage of the OTA, this current level is important to maintain mainly for the stability of the OTA. The voltage V_{ref2} is simply provided by the simple circuit shown in Fig. 6.14, where M2 is a unit multiple of M5 and M6 in Fig. 6.13.

6.3.3.5 CMFB results summary

Table 6.5 shows the performance summary of the CMFB for the first stage of each OTA.

	OTA1			OTA2			OTA3			
	Min	**Typ.**	**Max**	**Min**	**Typ.**	**Max**	**Min**	**Typ.**	**Max**	**Unit**
DC gain	48.46	58	62.8	44.36	54.6	60.1	48.5	57.8	62.6	**dB**
GBW	5.35	6.44	8.9	5.47	6.58	9.18	3.18	3.83	5.4	**MHz**
PM	77.43	82.8	92	86.86	91.88	102.4	82.96	88.67	100.1	°

Table 6.5: First-stage CMFB error OTA summary across PVT corners.

	OTA1			OTA2			OTA3			
	Min	**Typ.**	**Max**	**Min**	**Typ.**	**Max**	**Min**	**Typ.**	**Max**	**Unit**
DC gain	38.63	43.28	48.97	37.28	42.1	47.87	39.15	44.25	50.1	**dB**
GBW	4.2	4.8	5.87	3.98	4.58	5.71	3.46	3.96	5.2	**MHz**
PM	55.3	58.23	62.15	59.73	63	66.37	68.6	72.85	76.43	°

Table 6.6: Second-stage CMFB error OTA summary across PVT corners.

Table 6.6 shows the performance summary of the CMFB for the second stage of each OTA.

Furthermore, Table 6.7 shows the steady-state CM error across PVT corners, which is shown to not deviate beyond 12mV which is very acceptable.

6.3.4 Switching between 1 MHz- and 2 MHz-modes

A capacitive bank is used to switch between the two IF modes of the complex filter, it is also used to correct the error in the integrators time-constant due to RC process corners. The basic structure of the capacitive bank is shown in Fig. 6.15. It's simply a binary-weighted array of unit

	Ref.	Min.	Typ.	Max.	Unit
SS CM error	500	502	507	512	**mV**

Table 6.7: Steady-state CM error summary across PVT corners.

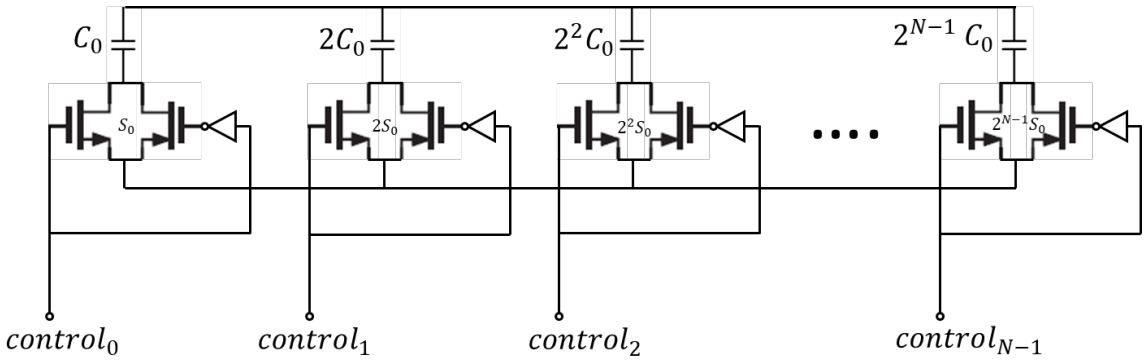


Figure 6.15: Capacitive bank implementation.

capacitors that are switched by binary-weighted transmission gates, where C_0 is the capacitance of the unit capacitor, and S_0 is the size of the unit transmission gate. The use of transmission gates is mainly to achieve lower on-resistance which peaks at mid-rail and provides relatively constant on-resistance across corners compared to just a single transistor. The devices of the transmission gates are sized to achieve lowest possible on-resistance and off-capacitance. Moreover, the devices should be wide enough to stay in triode region even with peak current swing, this enhances the overall linearity of the complex filter.

The obtained on-resistance for the unit-switch is $1.922K\Omega$, and the off-capacitance of the biggest switch is $8.56fF$.

Moreover, the choice of the number of bits of the capacitive bank cannot be arbitrary. The low number of bits results in poor resolution of correcting the error due to RC process corners, and the high number of bits results in degraded linearity due to the non-linearity of the switches, and degrades the complex filter response due to parasitics, as well as consuming more are. Thus, the optimum number of bits can be chosen such that the unit capacitor can correct the smallest variation due to RC process corners, and the maximum word can cover beyond the maximum range required for the

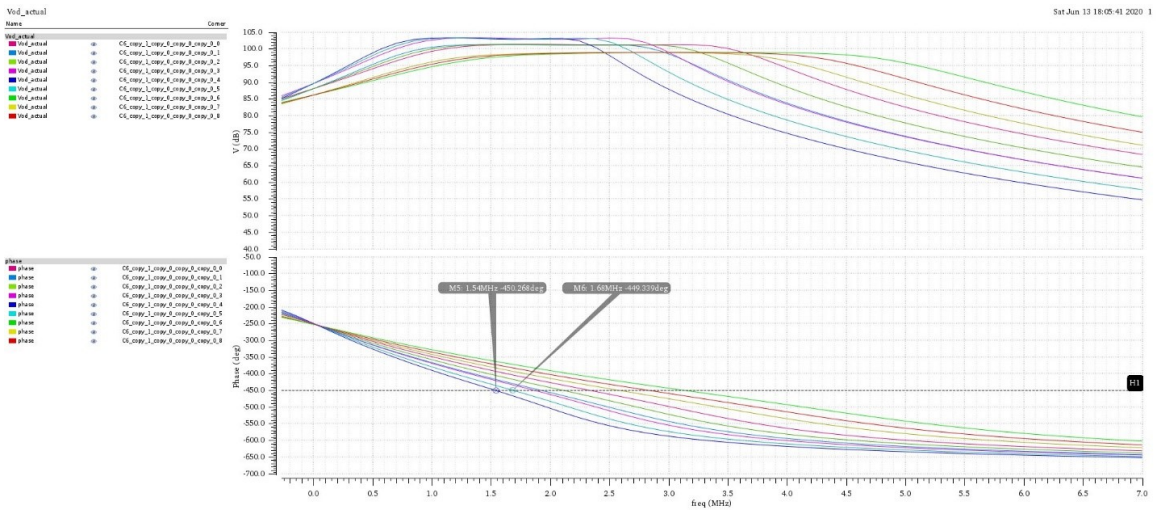


Figure 6.16: Variations in the magnitude and phase response of the complex filter due to RC process corners.

fastest corner of the smallest IF mode. Fig. 6.16 illustrates the variations of the filter response (magnitude and phase) due to RC process corners. Given that the phase should equal $-90°$ in mid-band, it's seen that the minimum frequency step is about 140 KHz. This value can simply be used to determine the unit capacitor for each integrator capacitive bank, while the maximum word is chosen such that, the word for the 1 MHz-mode is all ones with a zero in the MSB. This results in a six-bit word.

Fig. 6.17 shows the effect of changing one LSB for the marked corners in Fig. 6.16. The frequency offset changes from 140 KHz to 54 KHz which results almost identical responses.

The devices of the transmission gate are also implemented using low-VT devices to obtain better linearity across PVT corners. Table 6.8 shows the correcting words applied for the capacitive bank to fix the error resulting from the RC process corners in both IF modes.

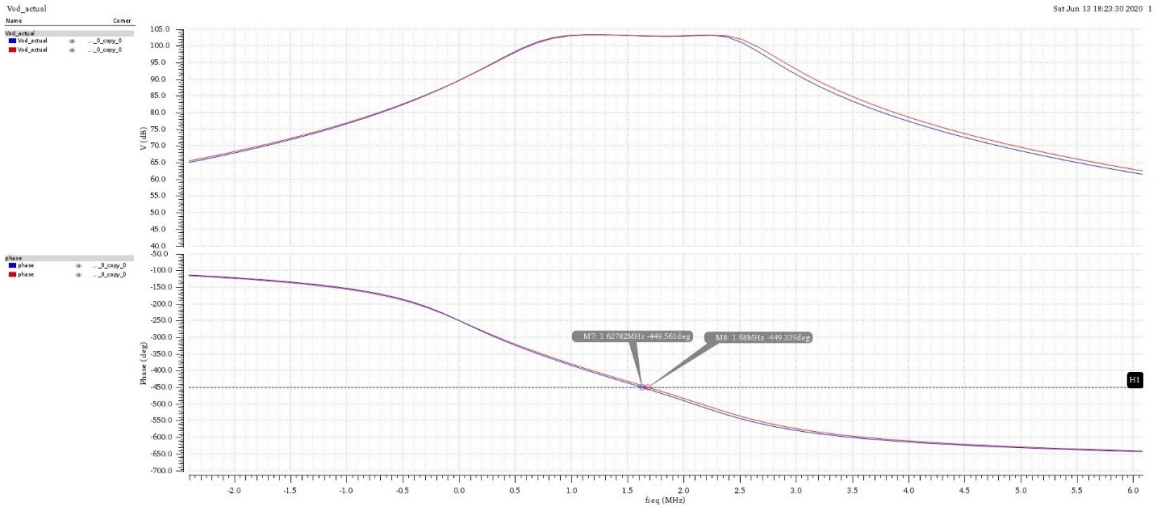


Figure 6.17: The two marked responses of Fig. 6.16 after changing 1 LSB of the capacitive bank word.

	1 MHz-mode			**2 MHz-mode**		
C / R	**Typ.**	**slow**	**fast**	**Typ.**	**slow**	**fast**
Typ.	011111	011001	101001	001111	001100	010101
slow	011100	010110	100110	001110	001011	010010
fast	100001	011011	101110	010001	001110	010111

Table 6.8: Capacitive bank words for all RC process corners.

6.3.5 Design procedure of the complex filter

There are some important issues that has been addressed in the design process to further optimize the complex filter and obtain best overall performance given power consumption limitations, these points are discussed in this section.

As shown in Fig. 6.9, the real LPF is simply a three-stage cascade of interconnected integrators, each with a certain time-constant which results in the Butterworth response of the filter. The time-constant of an integrator is simply given by RC. Thus, opposite scaling of R and C while keeping the time-constant won't change the filter response, but it affects other parameters such as noise, linearity, and op-amp gain and stability. Furthermore, the differential trans-impedance of the complex filter is simply determined by $2R_1R_5/R_3$. Thus, this has to be maintained and equal to $120K\Omega$.

The scaling of the R's and C's was to mainly ensure that the linearity of the filter is only limited by the last integrator stage. This is illustrated in Fig. 6.18, it shows the 1dB compression point test for each integrator stage, it can be seen that the P1dB is limited by the last integrator stage.

It can be noted that, decreasing R_1 while increasing R_5 to maintain constant trans-impedance results in lower gain from the first stages. Thus, improving overall linearity of the complex filter. However, this results in degradation of the noise performance of the filter. Therefore, the values were optimized as shown in table 6.3, to obtain best noise and linearity performance across PVT corners as discussed in the following sections. It is worth-mentioning that the main noise contributors in the complex filter shown in Fig. 6.10 are $R1_{IF}$, $R3$, $R5$, and the input devices of the first integrator op-amp, respectively. It should be noted that the noise performance is not limited by the op-amps due to the high transconductance of the first stage of the op-amps to obtain

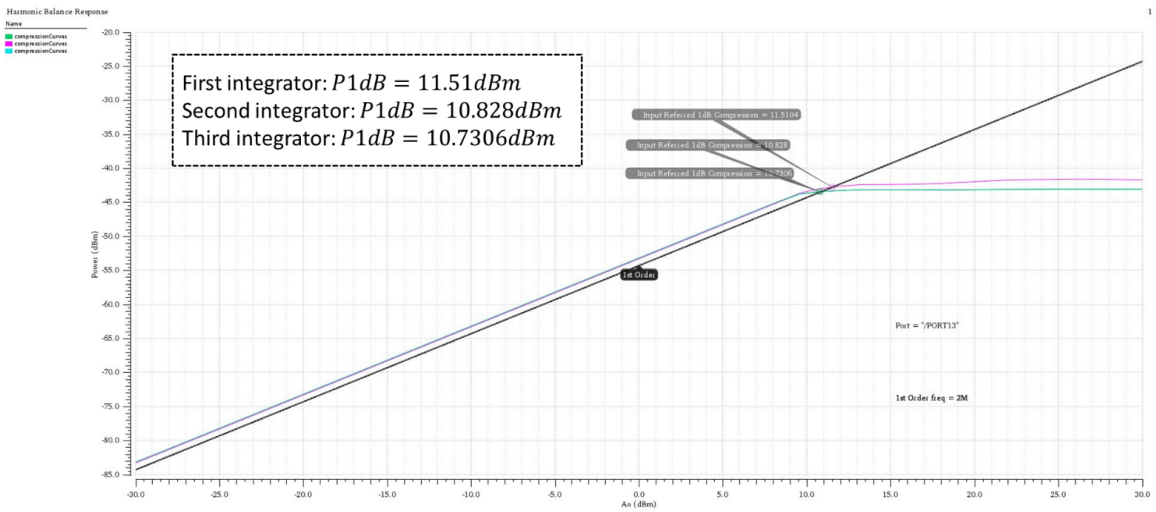


Figure 6.18: 1dB compression point test for each integrator stage of the filter.

desired GBW in order to lower the filter input impedance.

Furthermore, the finite non-dominant poles of the OTAs results in phase-lag for each integrator, which results in peaking in the magnitude response in passband, which results in more deviation from the ideal response, specially across PVT corners. This is simply fixed by adding a zero which adds extra phase-lead at ω_o of the integrator, this results in less peaking in the passband. This zero is simply added using the resistor R_s shown in Fig. 6.19, the zero is a LHP zero approximately located at $1/R_SC$ which is higher in frequency than ω_o of the integrator. The effect of the zero is shown in Fig. 6.20.

Finally, the biasing current of the filter is a poly current, generated as shown in Fig. 6.21. Since the deviation of this poly current affects the performance of the filter significantly across corners. a calibrating technique is also incorporated for the poly resistance in order to avoid these effects. As shown in Fig. 6.22, where the control lines can be generated from the cap. bank words shown in table 6.8 by simple digital logic gates.

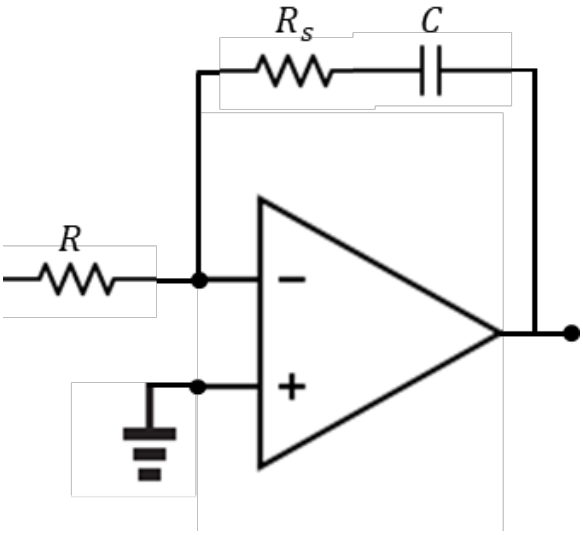


Figure 6.19: Addition of a zero using the series resistance R_s.

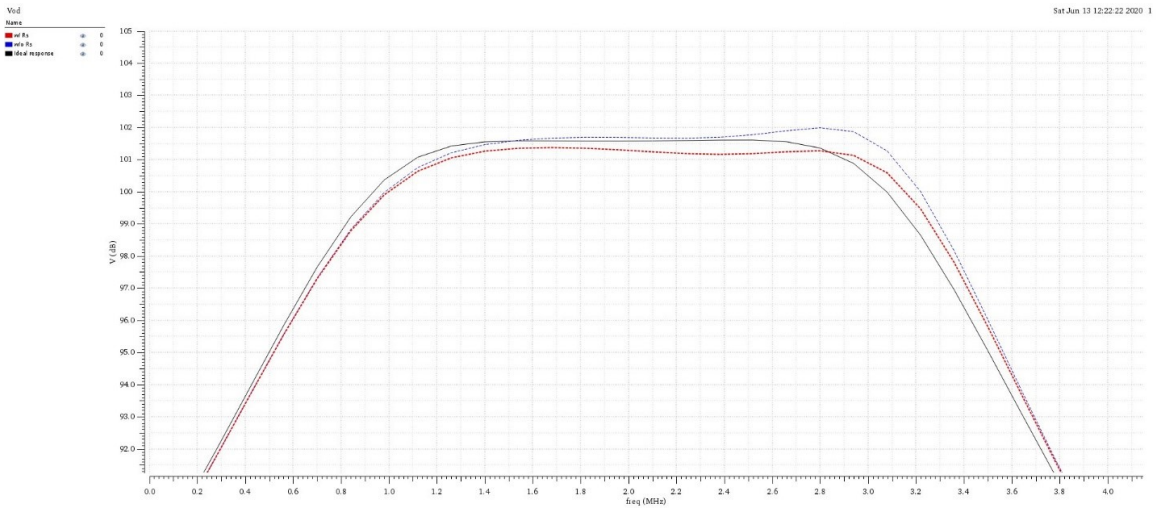


Figure 6.20: Change in magnitude response after the addition of R_s.

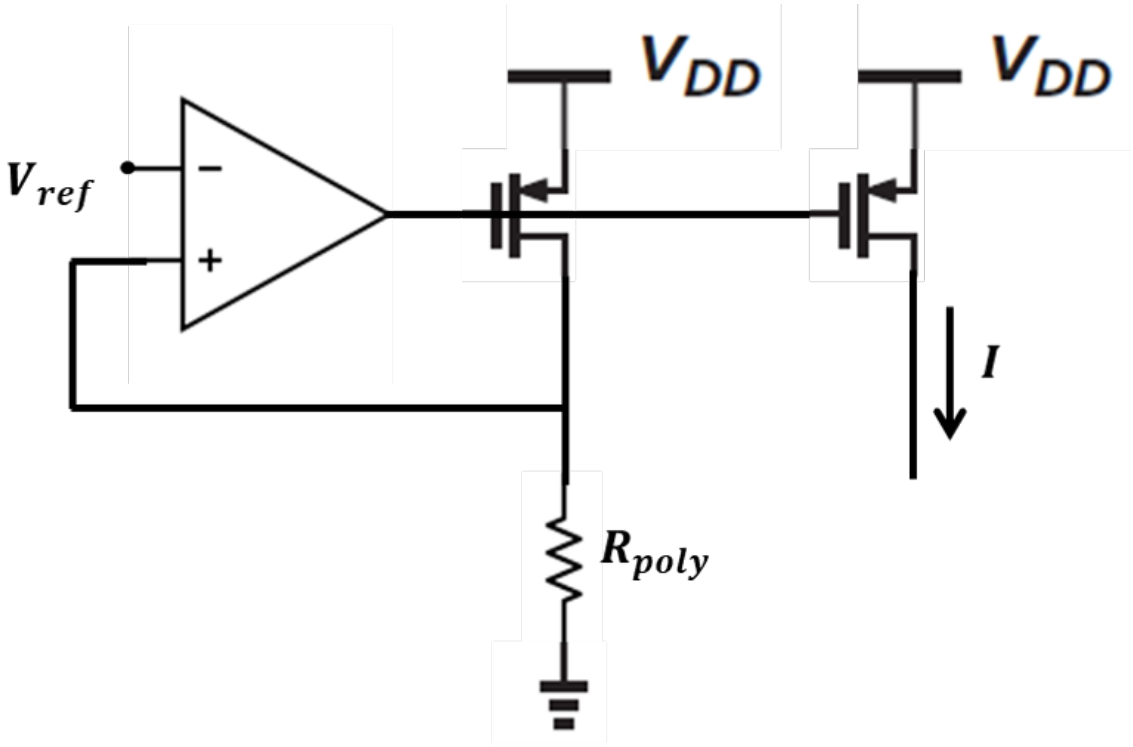


Figure 6.21: Typical poly current generation circuit.

6.4 Nominal Complex filter response

6.4.1 1 MHz-mode

6.4.1.1 Magnitude response and group delay

Fig. 6.23 shows the complex filter magnitude response, and group delay for the 1 MHz-mode. Maximum group delay variation can be defined by the bit-rate of the corresponding IF mode. Thus, the maximum passband group delay variation in 1 MHz-mode is maintained below 300nS. This is maintained as shown in Fig. 6.23, with a near-ideal magnitude response. The error in the magnitude response relative to the ideal Butterworth response is shown in Fig. 6.24, the error in the magnitude response should

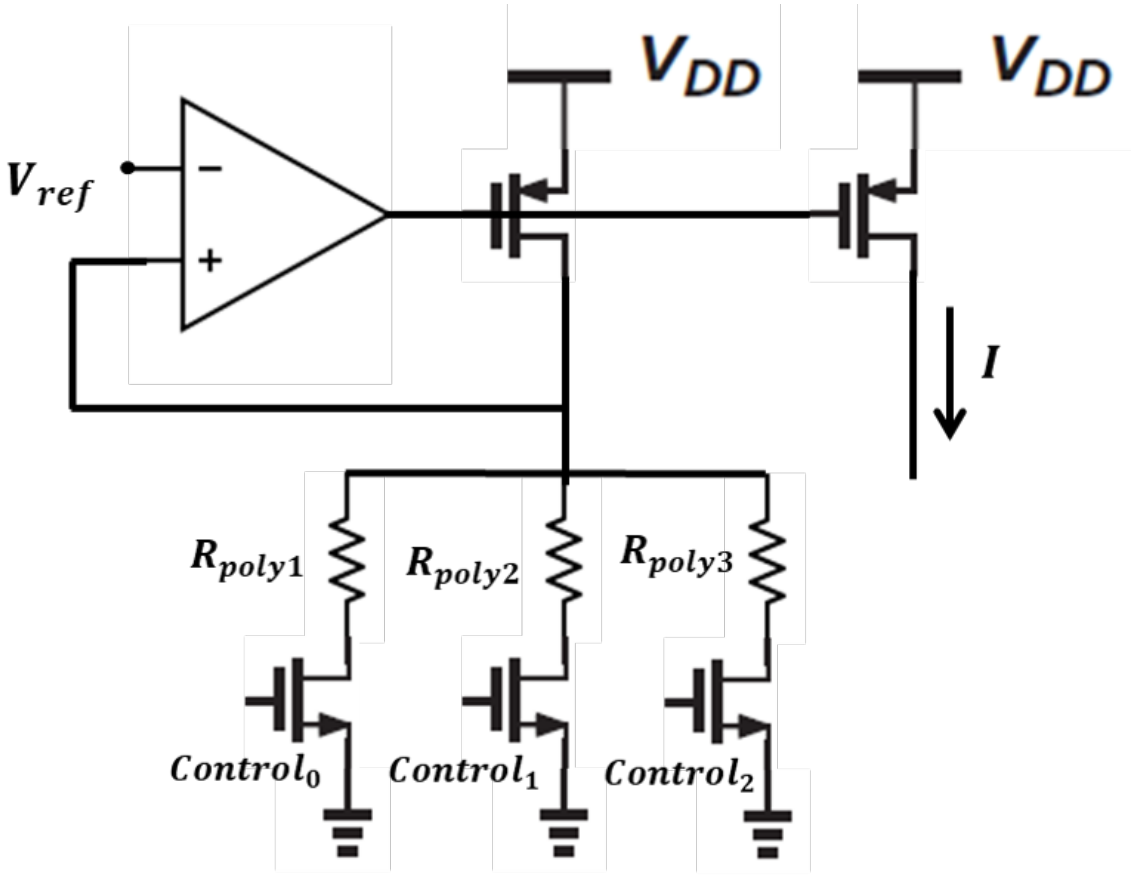


Figure 6.22: Modified poly current generation circuit with calibration.

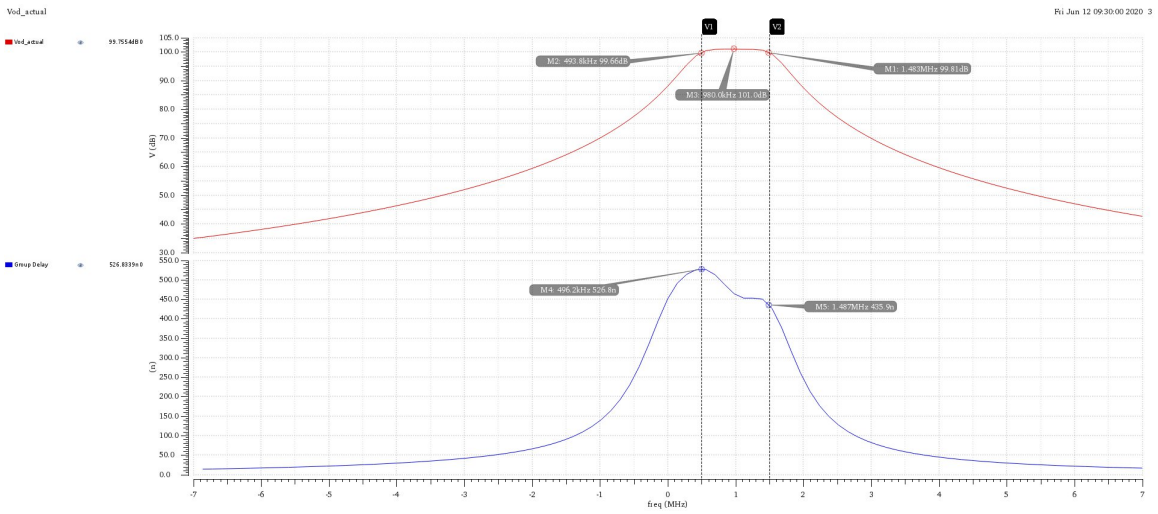


Figure 6.23: Magnitude response and group delay in the 1 MHz-mode.

be less than 1.5dB, which is maintained.

6.4.1.2 Input impedance

As aforementioned, the input impedance should be less than $3K\Omega$. The input impedance in the 1 MHz-mode is shown in Fig. 6.25.

6.4.1.3 Noise figure

The noise figure is shown in Fig. 6.26. The average passband noise figure is maintained below 50dB.

6.4.1.4 IIP3 test

The IIP3 test is carried out per standard by applying two tones at 4 MHz and 7 MHz, and observing the third-order inter-modulated tone at 1MHz resulting from the nonlinearity of the complex filter. As shown in Fig. 6.27,

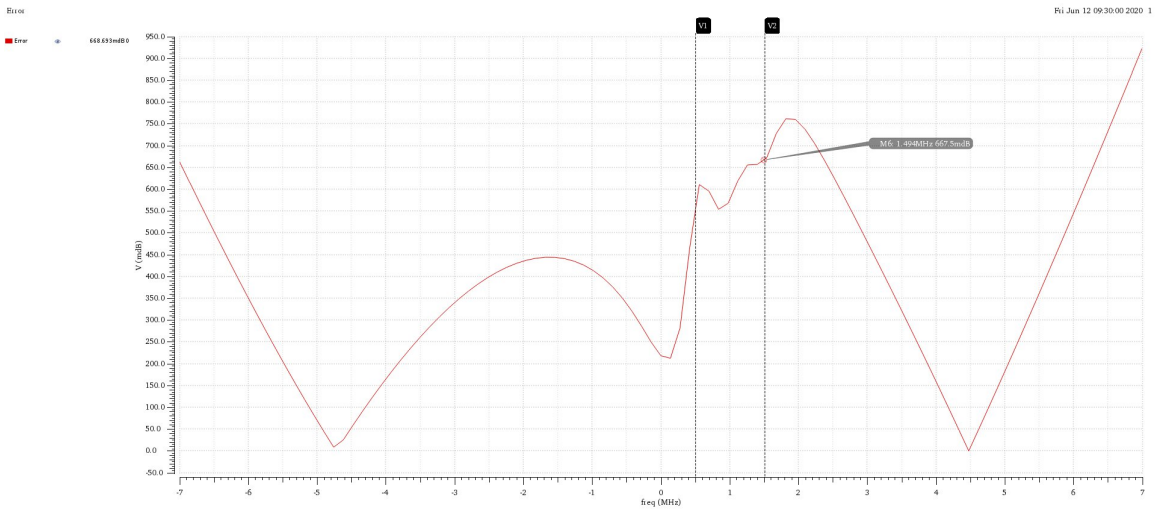


Figure 6.24: Error in magnitude response relative to the ideal Butterworth response in the 1 MHz-mode.

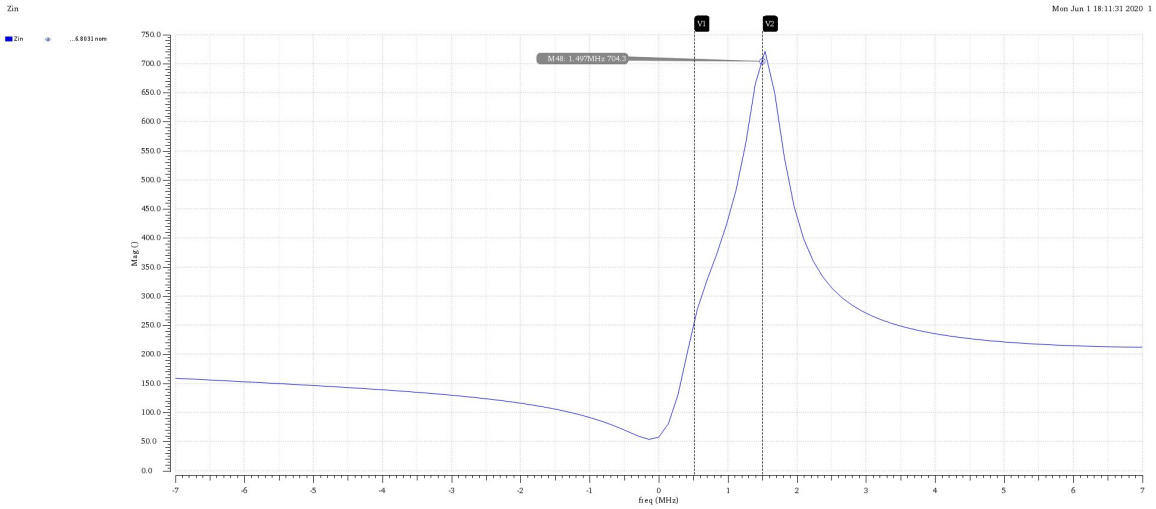


Figure 6.25: Input impedance in the 1 MHz-mode.

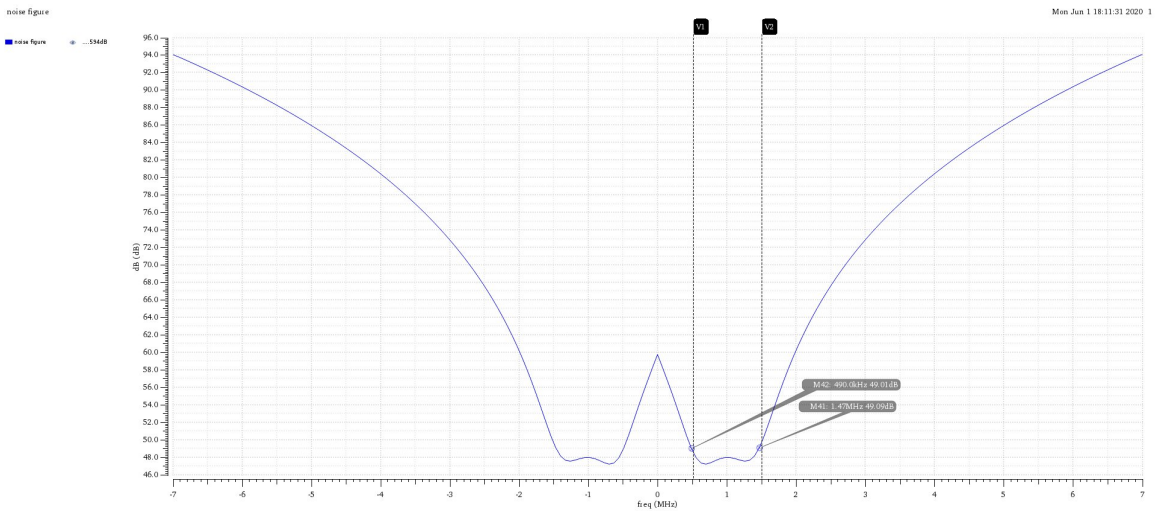


Figure 6.26: Noise figure in the 1 MHz-mode.

the IIP3 value is 34.846dBm in the 1MHz-mode.

6.4.1.5 Transient response

As shown in Fig. 6.28, the transient response of the complex filter in the 1 MHz-mode. It can be seen that the filter maintains a stable response for a CT sinusoidal signal.

6.4.2 2 MHz-mode

6.4.2.1 Magnitude response and group delay

Fig. 6.29 shows the complex filter magnitude response, and group delay for the 2 MHz-mode. Maximum passband group delay variation in 2 MHz-mode is about 200nS. This is maintained as shown in Fig. 6.29. The error in the magnitude response relative to the ideal Butterworth response is shown in Fig. 6.30, the error in the magnitude response should be less

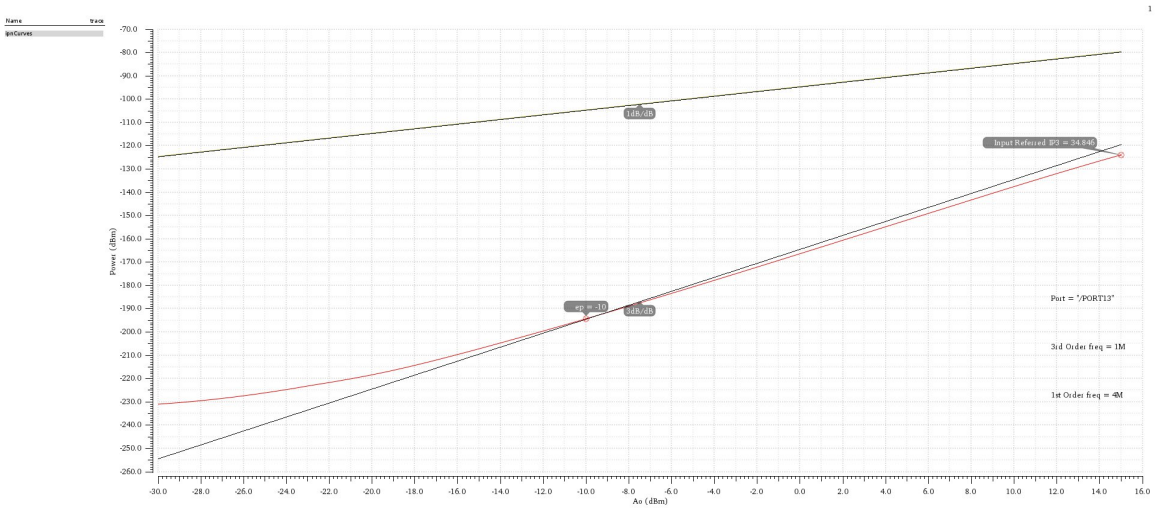


Figure 6.27: IIP3 test in the 1 MHz-mode.

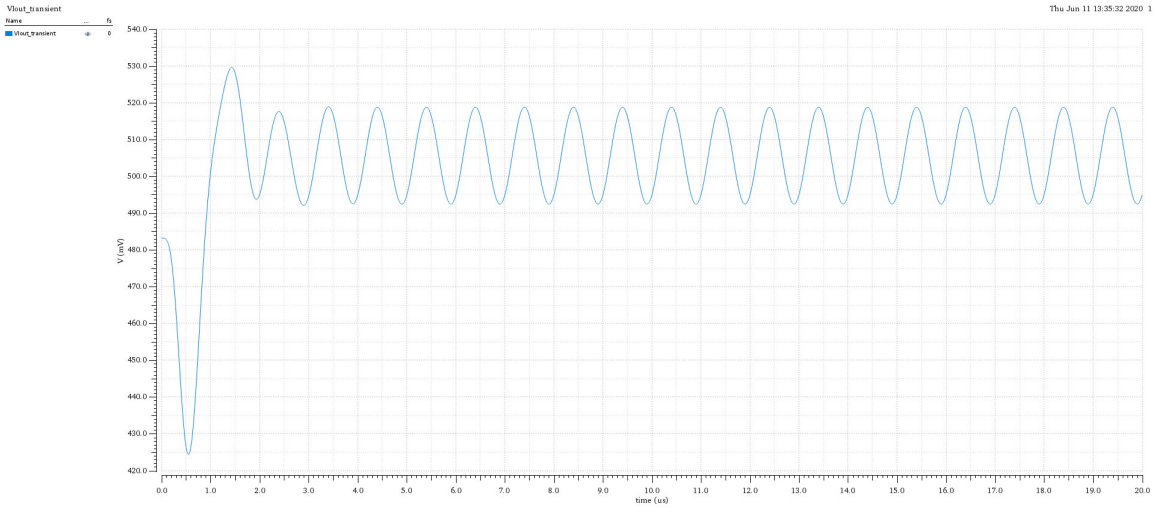


Figure 6.28: Transient response in the 1 MHz-mode.

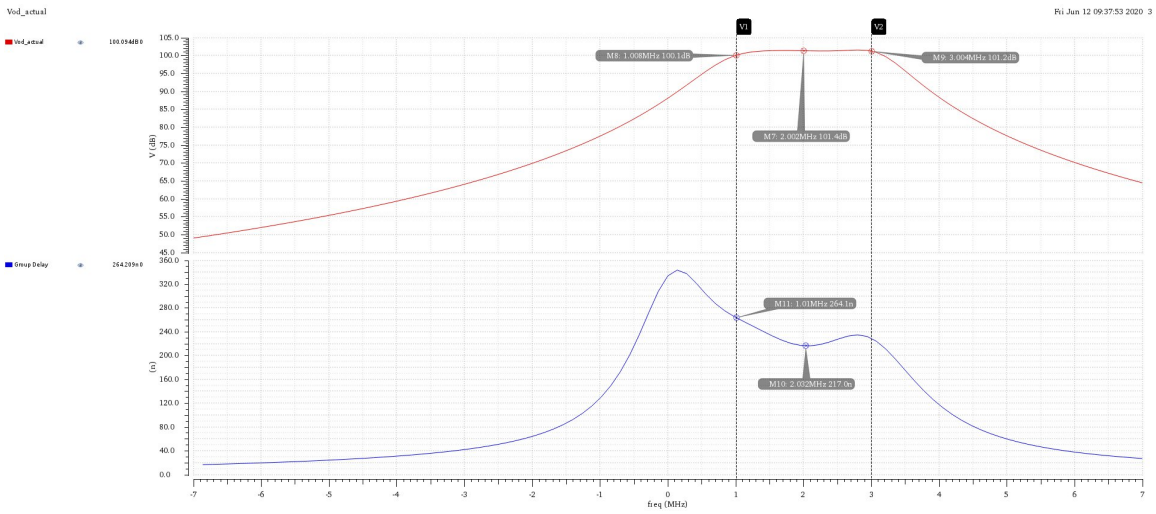


Figure 6.29: Magnitude response and group delay in the 2 MHz-mode.

than 1.5dB, which is maintained.

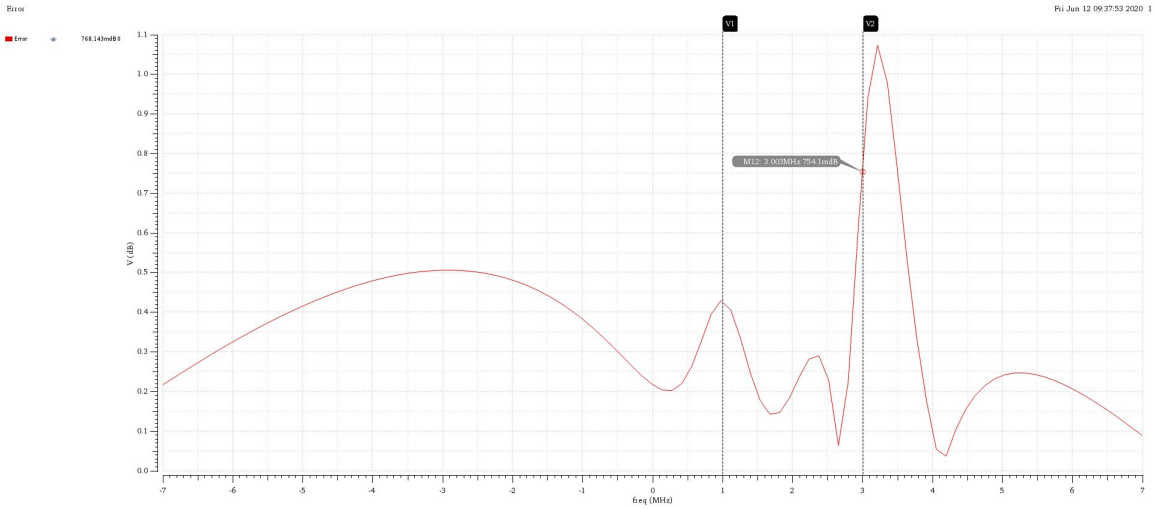


Figure 6.30: Error in magnitude response relative to the ideal Butterworth response in the 2 MHz-mode.

6.4.2.2 Input impedance

As aforementioned, the input impedance should be less than $3K\Omega$. The input impedance is shown in Fig. 6.31 for the 2 MHz-mode.

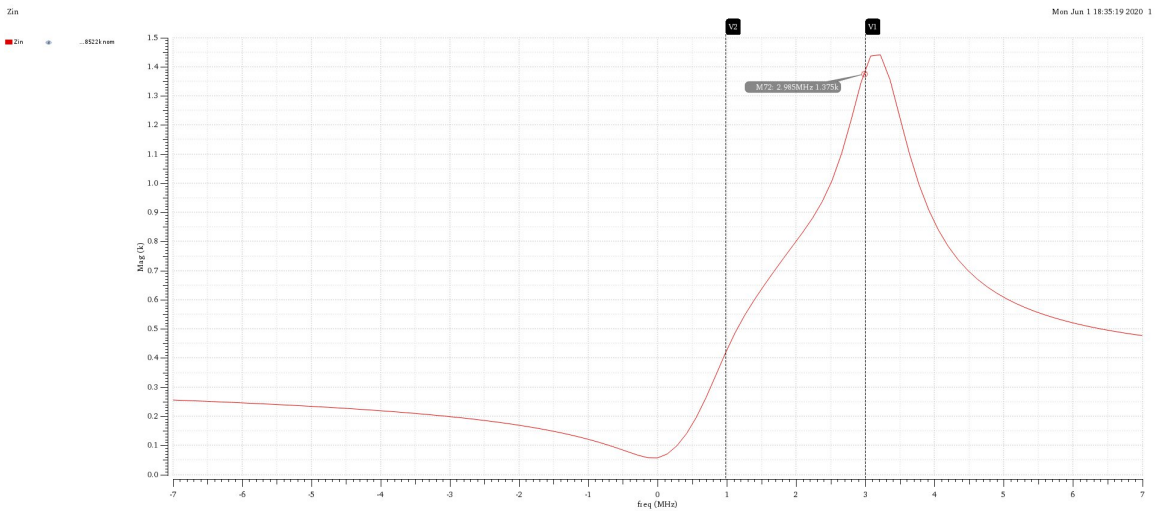


Figure 6.31: Input impedance in the 2 MHz-mode.

6.4.2.3 Noise figure

The noise figure for the 2 MHz-mode is shown in Fig. 6.32. The average passband noise figure is maintained below 50dB.

6.4.2.4 IIP3 test

The IIP3 test is carried out per standard by applying two tones at 8 MHz and 14 MHz, and observing the third-order inter-modulated tone at 2 MHz resulting from the nonlinearity of the complex filter. As shown in Fig. 6.33, the IIP3 value is 36.17dBm in the 2MHz-mode.

6.4.2.5 Transient response

As shown in Fig. 6.34, the transient response of the complex filter in the 2 MHz-mode. It can be seen that the filter maintains a stable response for

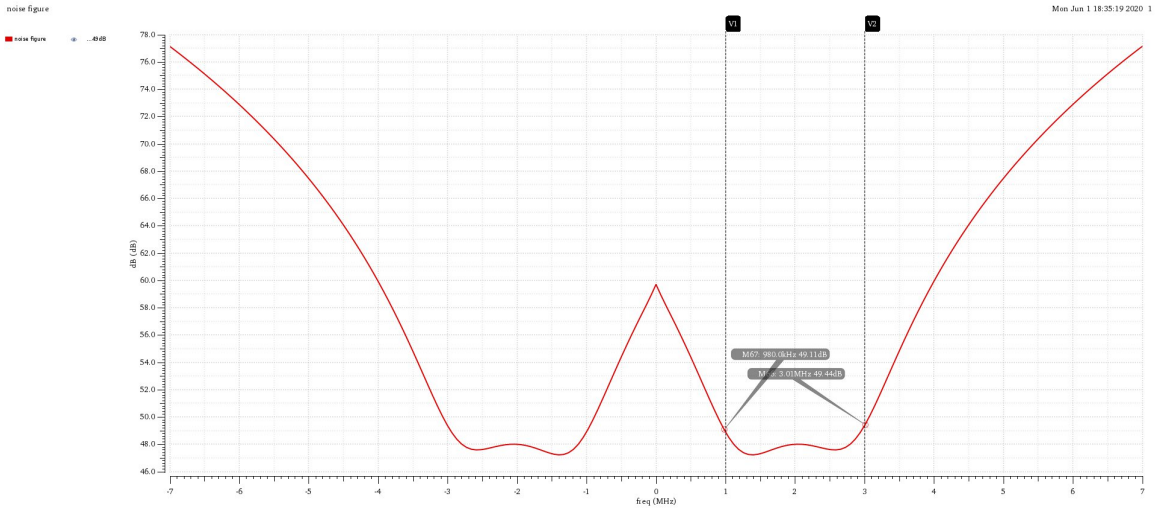


Figure 6.32: Noise figure in the 2 MHz-mode.

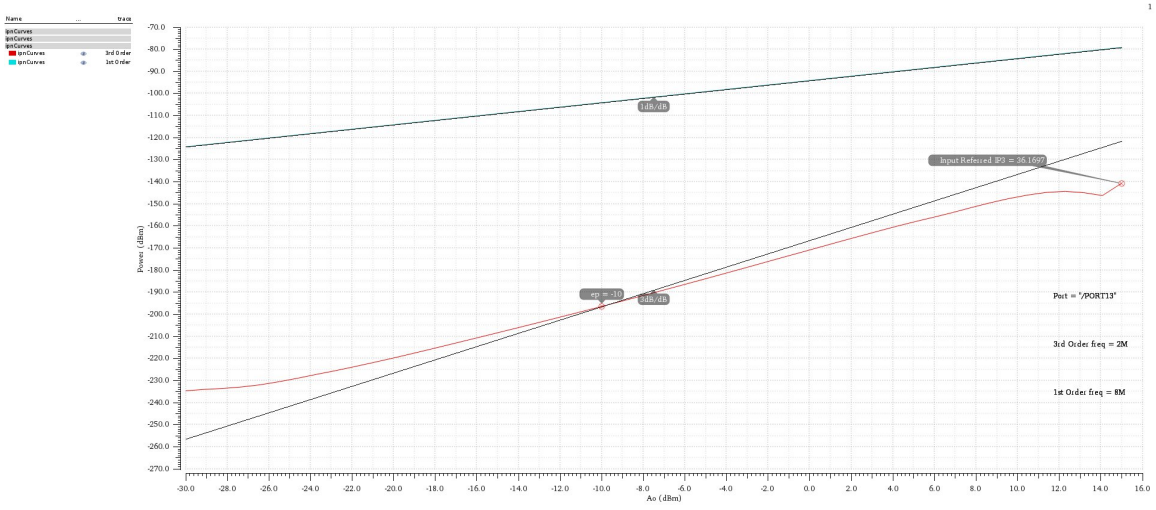


Figure 6.33: IIP3 test in the 2 MHz-mode.

a CT sinusoidal signal.

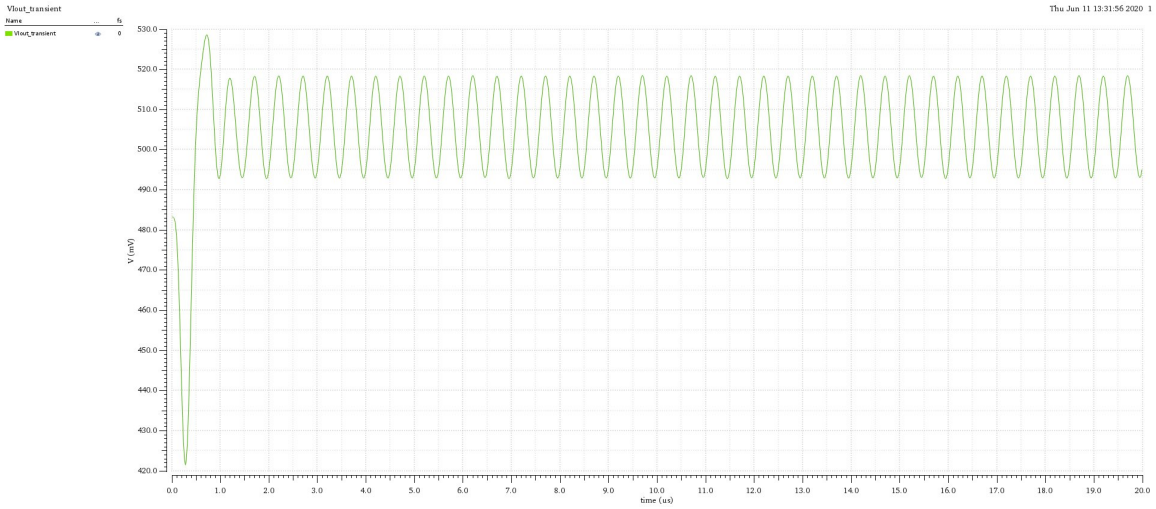


Figure 6.34: Transient response in the 2 MHz-mode.

6.5 Complex filter response across PVT corners

In this section, the performance of the complex filter across PVT corners is illustrated in detail. Table 6.9 shows the PVT corners that were simulated, it's a total of 2025 corners.
It is worth-mentioning that for each RC corner, the appropriate word from table 6.8 is inserted to the cap. banks to maintain the filter response at the desired IF frequency.

6.5.1 1 MHz-mode

6.5.1.1 Magnitude response

As shown in Fig. 6.35, the magnitude response of the complex filter in the 1 MHz-mode. The error in the integrators time-constant due to RC process corners is fixed by applying the corresponding word from table 6.8.

Parameter	Variation
Temperature	-40, 27, 125 °
Supply	0.95, 1, 1.05 Volts
Resistance	SS, TT, FF
Capacitance	SS, TT, FF
MOSFET	SS, SF, TT, FS, FF
LVT MOSFET	SS, SF, TT, FS, FF

Table 6.9: PVT corners run on the complex filter.

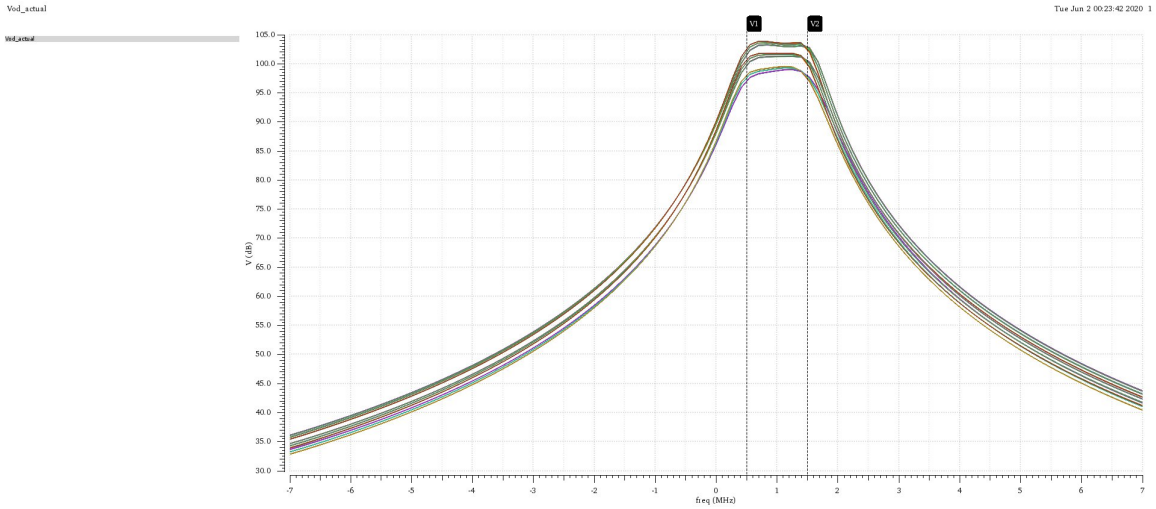


Figure 6.35: Magnitude response across PVT corners in the 1 MHz-mode.

It can be noted that the steps of the gain of the passband is due to the process corners of R1 in Fig. 6.10, this resistance determines the trans-conductance of the complex filter. These variations are acceptable in this receiver chain. However, it can be generally fixed by replacing R1 with a resistive bank that is calibrated to correct the trans-conductance, the same as done for the integrators time-constant, but it will slightly degrade the complex filter linearity.

Fig. 6.36 also shows the error in the magnitude response normalized to the ideal Butterworth response. The error in the magnitude response should not exceed 1.5dB, which is maintained across PVT corners, with maximum

error equals 1.33dB.

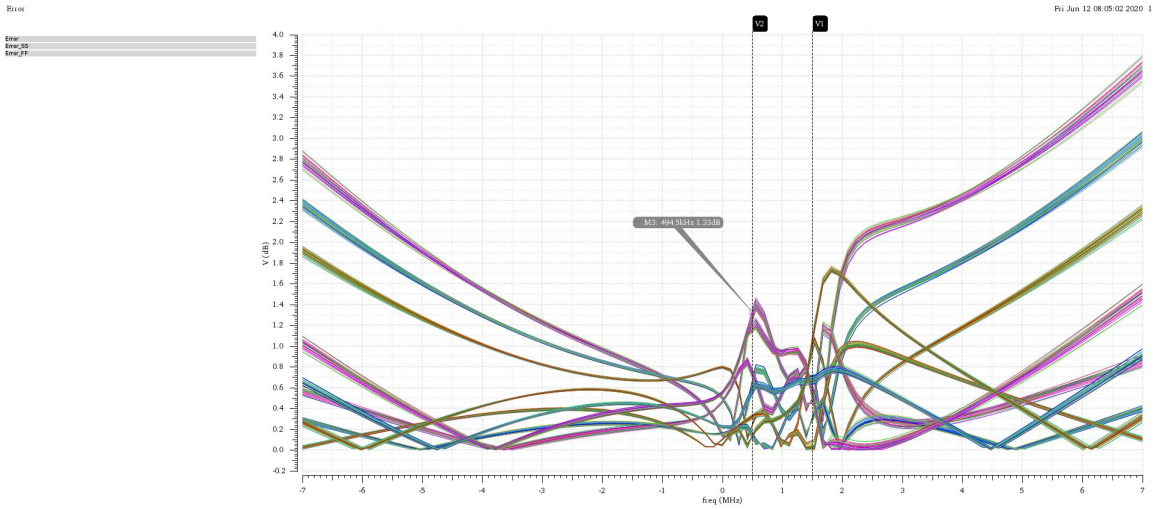


Figure 6.36: Error in the magnitude response across PVT corners in the 1 MHz-mode.

6.5.1.2 Group delay

As aforementioned, the maximum in-band group delay variations in the 1 MHz-mode should be less than 300nS. As shown in Fig. 6.37, this is maintained across PVT corners, with maximum in-band variations of about 180nS.

6.5.1.3 Input impedance

As illustrated in Fig. 6.38, the input impedance is kept below $3K\Omega$ across PVT corners, with maximum value of $1.13K\Omega$.

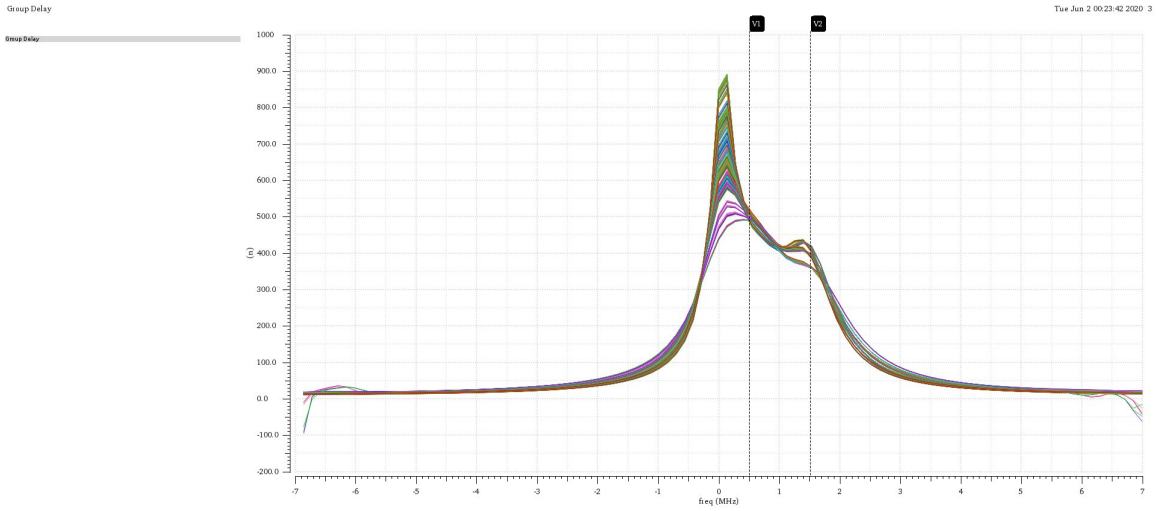


Figure 6.37: Group delay across PVT corners in the 1 MHz-mode.

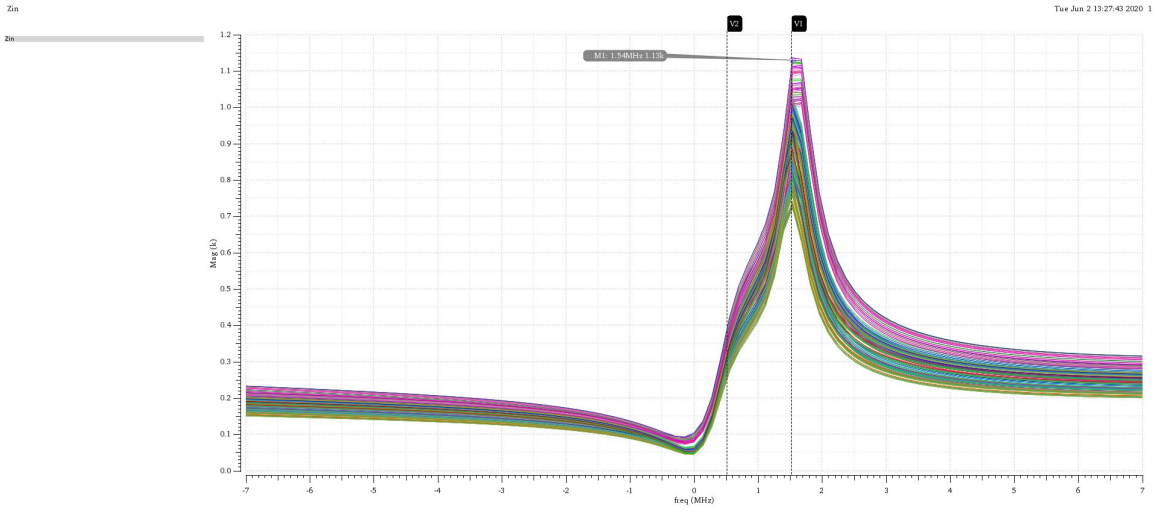


Figure 6.38: Input impedance across PVT corners in the 1 MHz-mode.

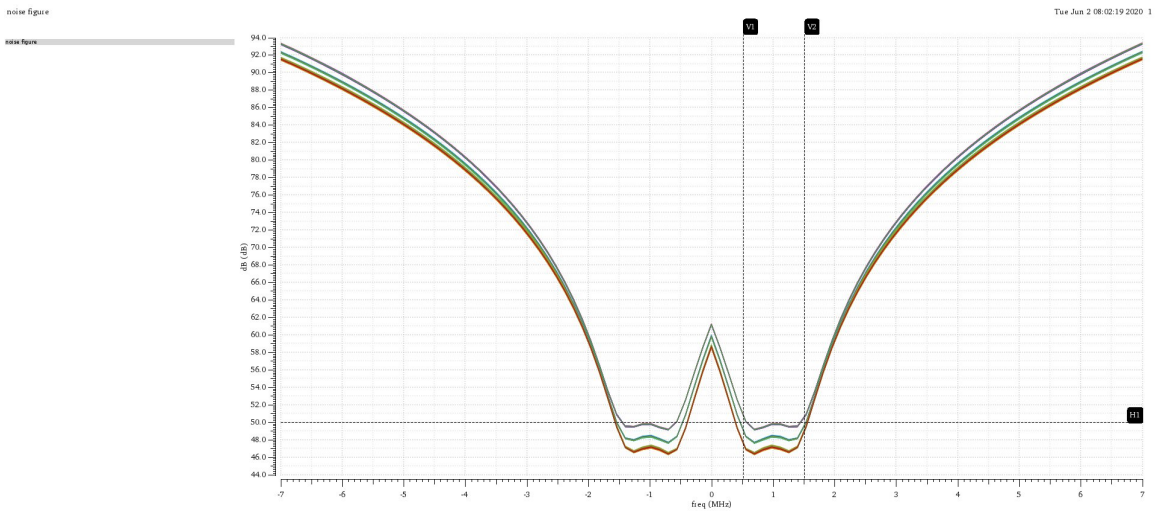


Figure 6.39: Noise figure across PVT corners in the 1 MHz-mode.

6.5.1.4 Noise figure

The average noise figure of the complex filter in the 1 MHz-mode is maintained below 50 dB in passband across PVT corners, as shown in Fig. 6.39.

6.5.1.5 IIP3 test

As shown in Fig. 6.40, the IIP3 should be maintained above 30 dBm, which is maintained across PVT corners for the 1 MHz-mode.

6.5.2 2 MHz-mode

6.5.2.1 Magnitude response

Fig. 6.41 illustrates the magnitude response for the 2 MHz-mode across PVT corners.

The maximum passband error in the magnitude response relative to the

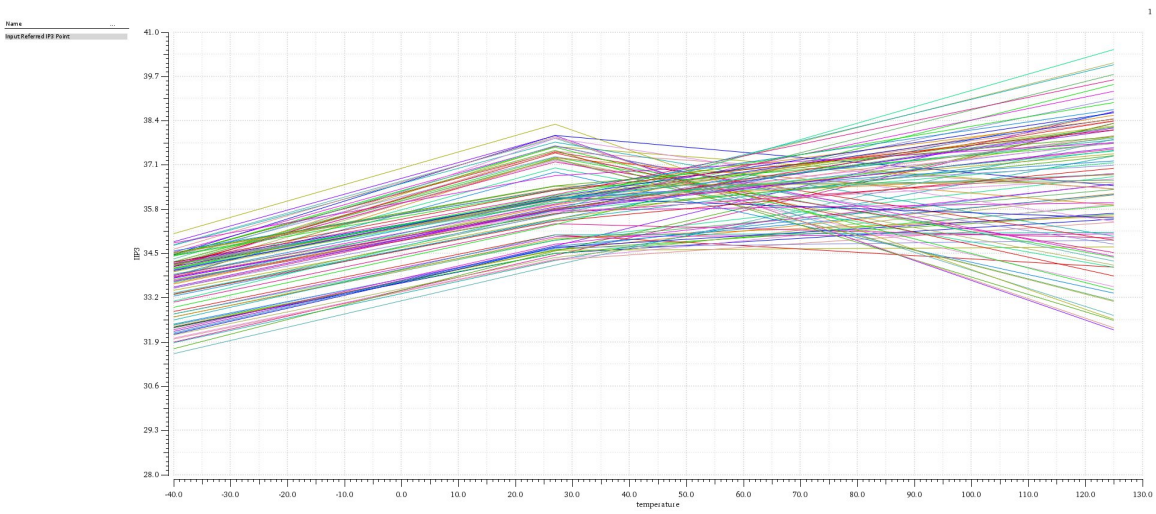


Figure 6.40: IIP3 test across PVT corners in the 1 MHz-mode.

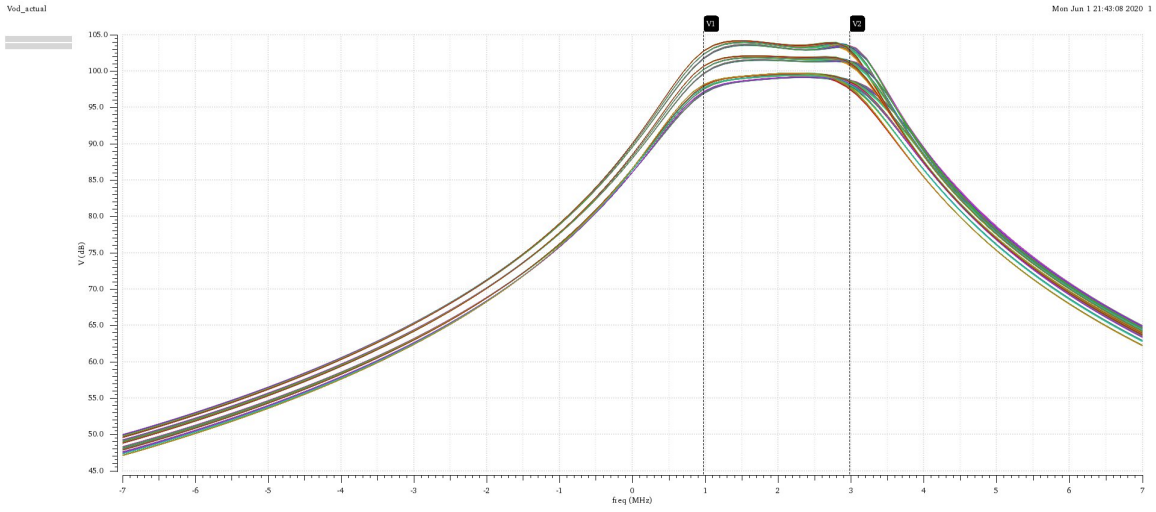


Figure 6.41: Magnitude response across PVT corners in the 2 MHz-mode.

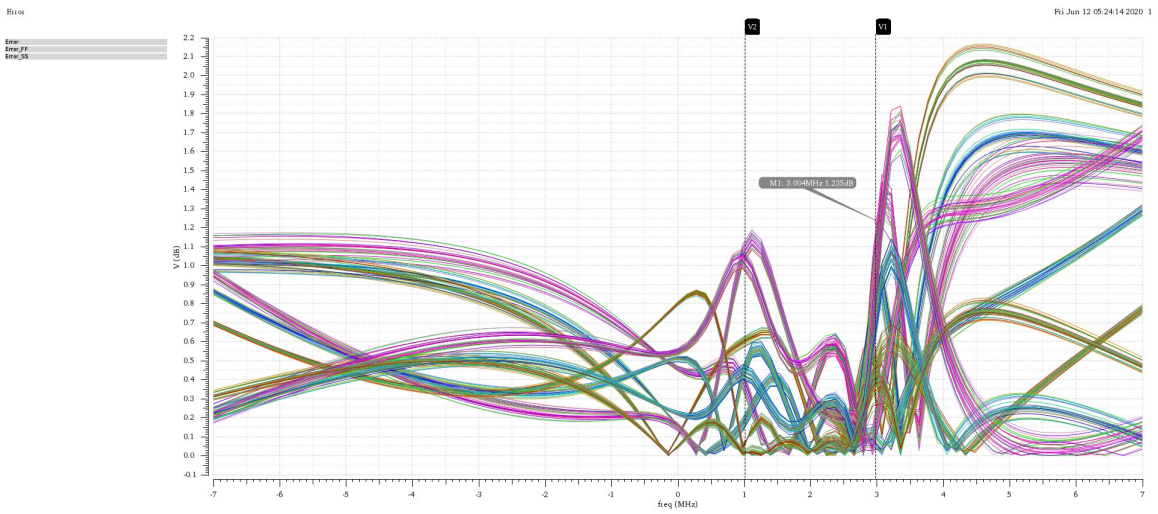


Figure 6.42: Error in the magnitude response across PVT corners in the 2 MHz-mode.

ideal Butterworth response should be maintained less than 1.5dB, which is maintained across PVT corners, as shown in Fig. 6.42, with maximum passband error of 1.235dB.

6.5.2.2 Group delay

As aforementioned, the maximum in-band group delay variations in the 2 MHz-mode should be less than 200nS. As shown in Fig. 6.43, this is maintained across PVT corners, with maximum in-band variations of about 70nS.

6.5.2.3 Input impedance

As previously mentioned, the input impedance should be maintained less than $3K\Omega$, which is maintained as well across PVT corners in the 2 MHz-mode as shown in Fig. 6.44, with maximum value of $2.233K\Omega$.

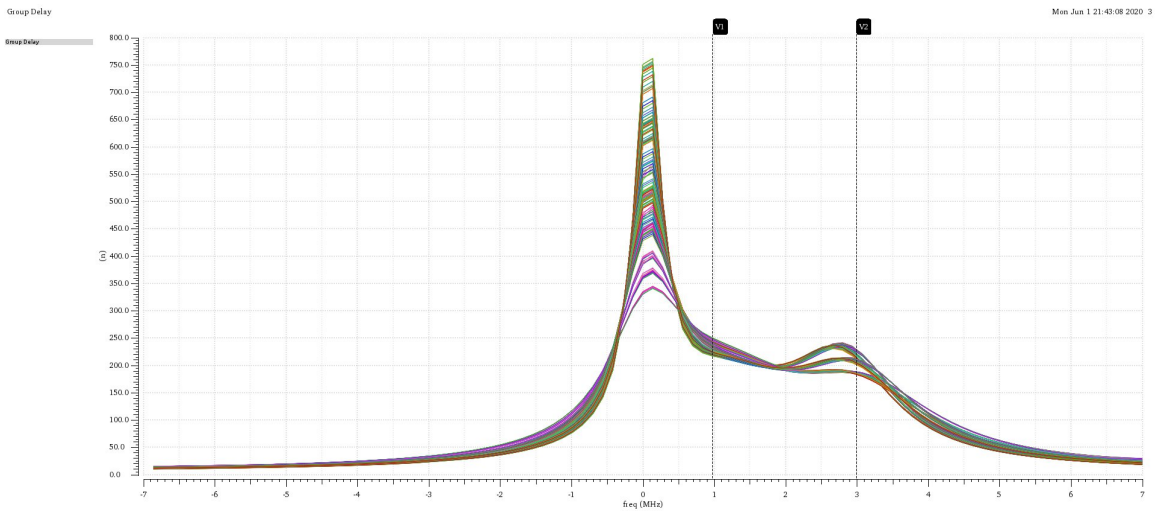


Figure 6.43: Group delay across PVT corners in the 2 MHz-mode.

6.5.2.4 Noise figure

As aforementioned, the noise figure of the complex filter should be maintained below 50dB. This maintained across PVT corners for the 2 MHz-mode as shown in Fig. 6.45.

6.5.2.5 IIP3 test

As stated before, the IIP3 should be maintained above 30dBm. As illustrated in Fig. 6.46, some corners fall below the specification by about 3dBm at extreme temperatures, and low-supply corners, that is due to the finite bandwidth of op-amps, which is limited by the current consumption specification. However, this is considered acceptable for the complex filter in the 2MHz-mode, because the IIP3 specification is a competitive specification, the BLE standard IIP3 specification in the 2MHz-mode is less than 30dBm [3].

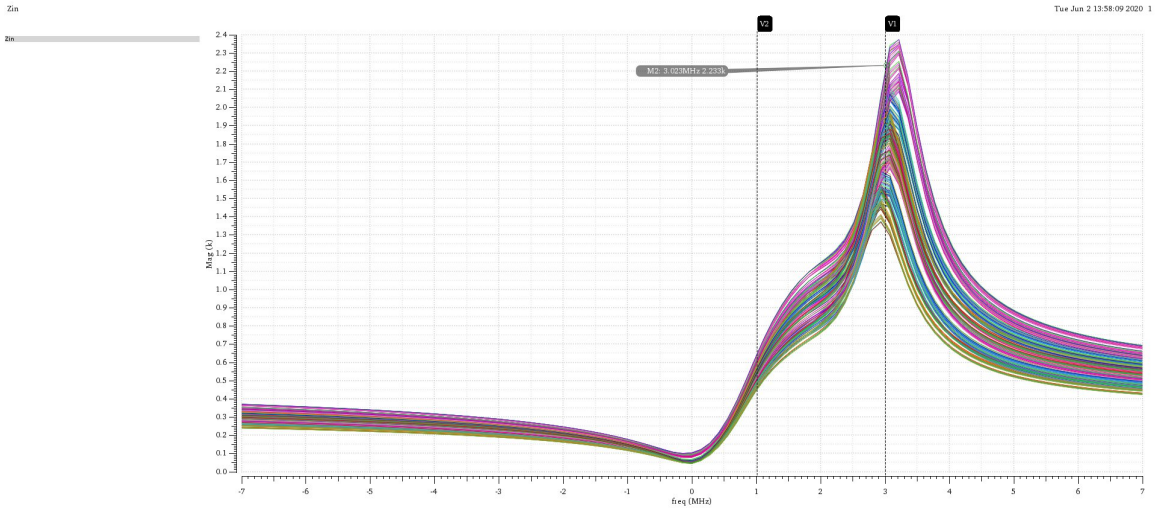


Figure 6.44: Input impedance across PVT corners in the 2 MHz-mode.

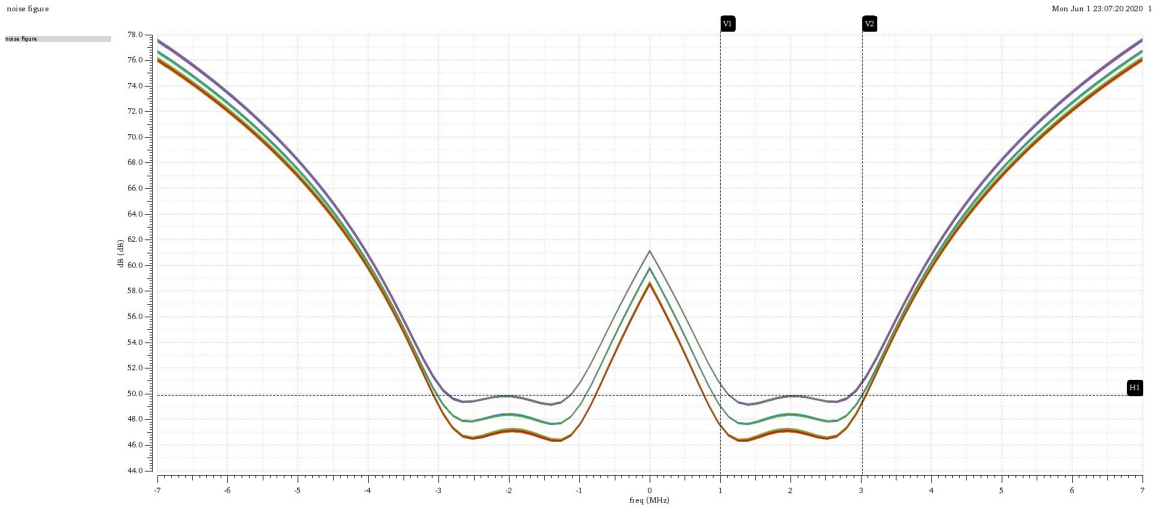


Figure 6.45: Noise figure across PVT corners in the 2 MHz-mode.

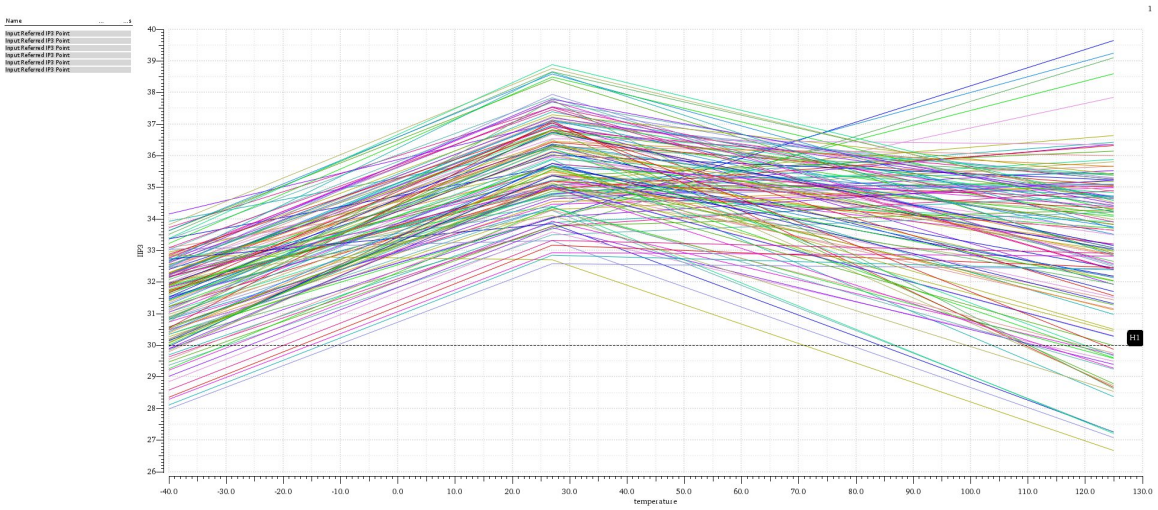


Figure 6.46: IIP3 test across PVT corners in the 2 MHz-mode.

6.5.2.6 Transient response

Fig. 6.47 illustrated the transient response across PVT corners in the 2 MHz-mode. It can be noted that the complex filter maintains a stable response across PVT corners, with about 3.5uS settling time.

6.5.3 PVT corners results summary

Table 6.10 illustrates the complex filter performance parameters that are achieved across PVT corners.

6.6 Monte Carlo simulation results

Statistical mismatch (Monte Carlo) simulation was performed to further assess the complex filter performance under the effects of mismatch. The

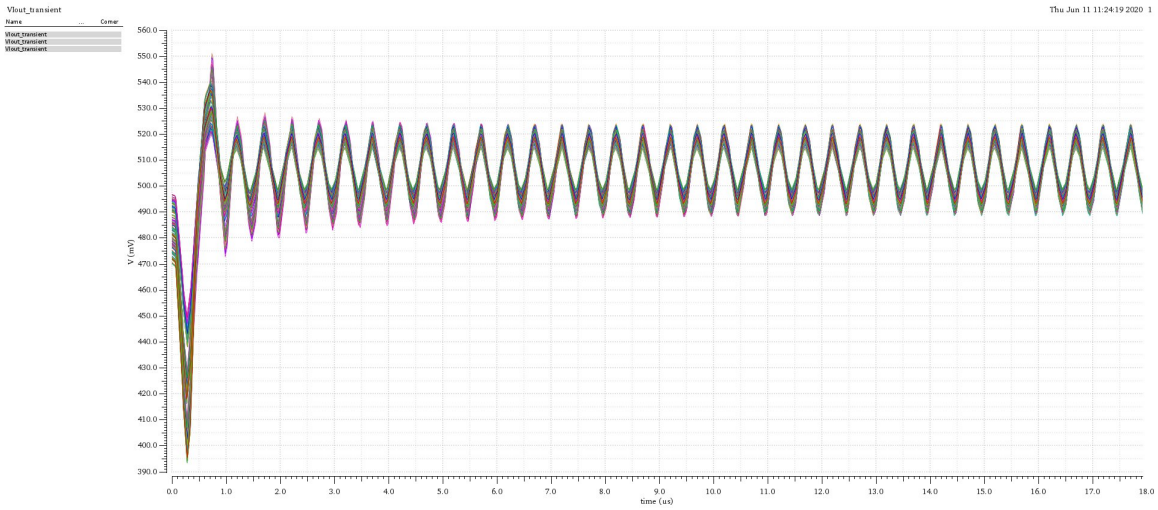


Figure 6.47: Transient response across PVT corners in the 2 MHz-mode.

		Achieved						
		1 MHz-mode			2 MHz-mode			
Parameter	**Specification**	**Min**	**Typ.**	**Max**	**Min**	**Typ.**	**Max**	**Unit**
Current Consumption	=1 (typical)	0.85	1.03	1.32	0.85	1.03	1.32	**mA**
Error in magnitude response	<1.5	0.2	0.67	1.33	0.2	0.75	1.235	**dB**
Group delay variation	<200	80	91	160	25	47.1	70	**nS**
Noise Figure	<50	45.58	47.84	50.43	45.7	47.84	50.4	**dB**
IIP3	>30	31.8	34.85	41	26.6	36.17	40	**dBm**
Input impedance	<3	0.4	0.7	1.13	0.8	1.375	2.233	$K\Omega$

Table 6.10: Complex filter performance summary across PVT corners.

simulation was run over the typical process corners only, and 200 simulation runs were performed.

6.6.1 Image-rejection ratio (IRR)

As previously mentioned, IRR is mainly degraded due to the component mismatch between the I and Q paths. Ideally, as shown in Fig. 6.35 and Fig. 6.41, IRR equals 31dB. However, due to component mismatch, the IRR degrades as shown in Fig. 6.48 and Fig. 6.49 for the 1 MHz- and 2 MHz-modes, respectively. The worst IRR in the 1 MHz-mode is 30.2dB. Whilst for the 2 MHz-mode, the worst IRR is 30.33dB. It is worth-mentioning that the BLE standard specifies the image-frequency interference C/I_{Image} to be 9dB which is ensured and maintained with very good margin [3].

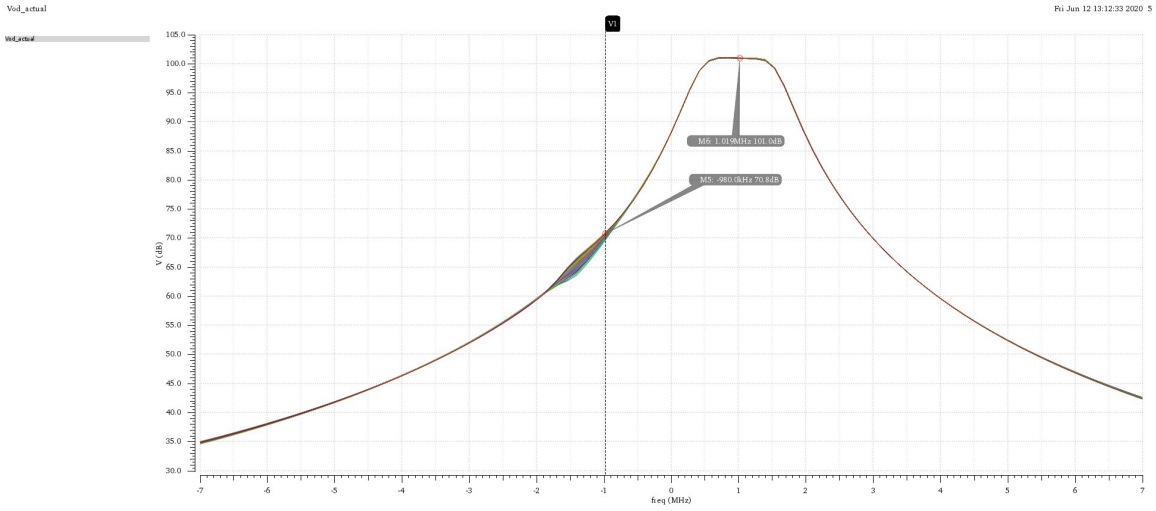


Figure 6.48: Image spill-over in the magnitude response in the 1 MHz-mode.

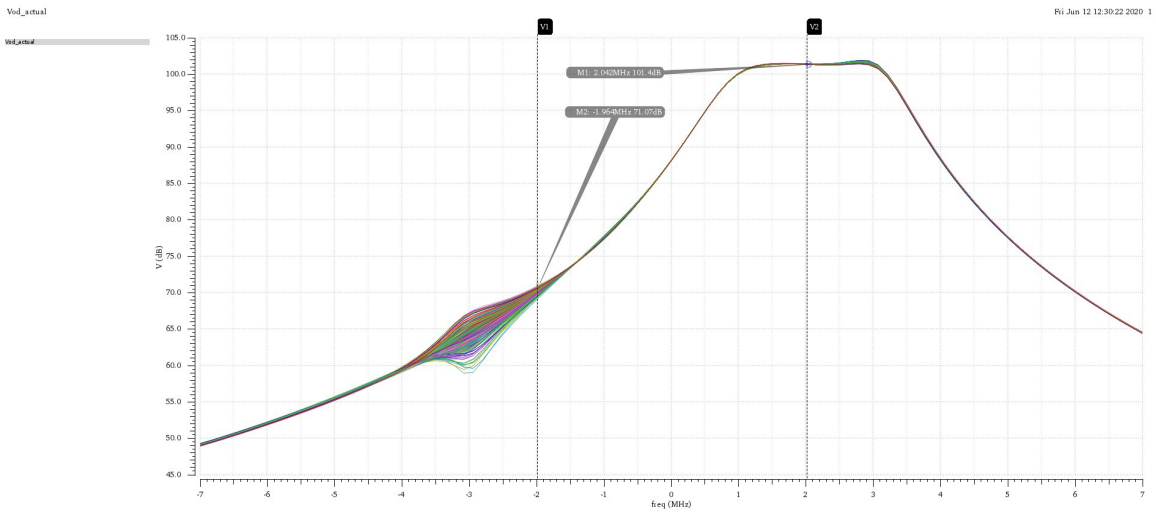


Figure 6.49: Image spill-over in the magnitude response in the 2 MHz-mode.

6.6.2 Current consumption

The total current consumption varies slightly with mismatch as shown in Fig. 6.50. With a mean value of about 1.04mA.

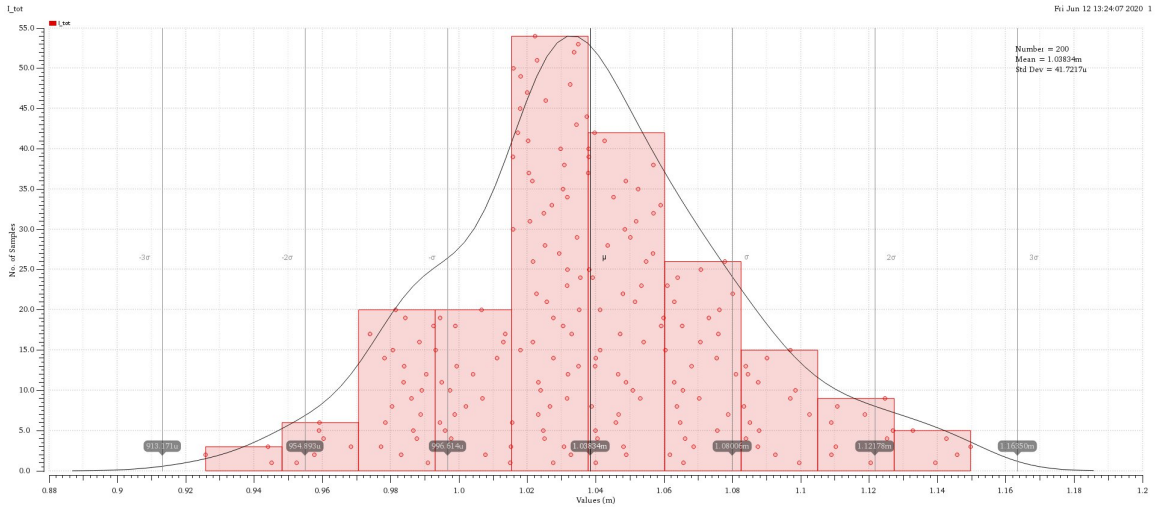


Figure 6.50: Current Consumtion histogram of Monte Carlo simulation.

6.6.3 Complex filter DC offset

As a result of mismatch, the differential outputs have an offset in their CM levels, this offset is displayed in Fig. 6.51. It can be seen that the maximum offset is 10mV which is acceptable and doesn't introduce non-linearity problems.

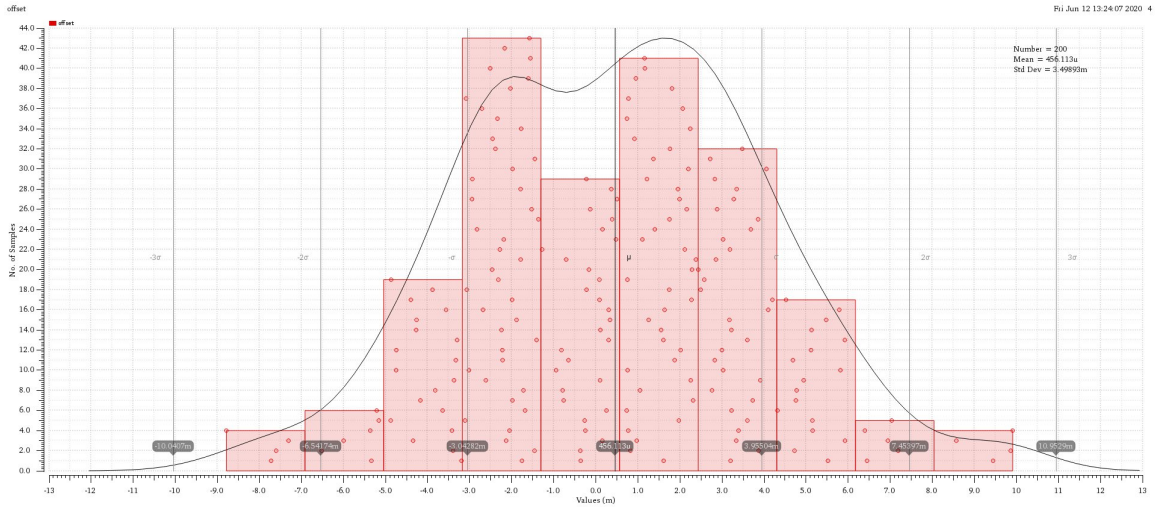


Figure 6.51: Offset mismatch histogram of Monte Carlo simulation.

6.6.4 Complex filter quadrature phase offset

Similarly, as a result of mismatch, the quadrature phase difference between the I and Q paths slightly differs, as shown in Fig. 6.52 and Fig. 6.53 for the 1 MHz- and 2 MHz-modes, respectively. For the 1 MHz-mode, the maximum phase offset is $0.35°$. And for the 2 MHz-mode, the maximum phase offset is $0.2°$.

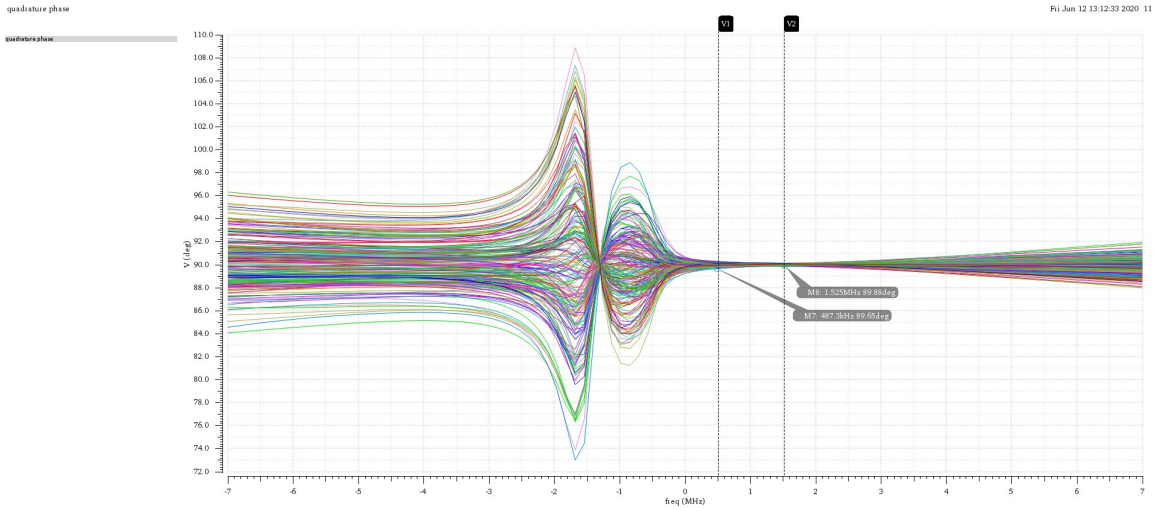


Figure 6.52: Quadrature phase mismatch of Monte Carlo simulation.

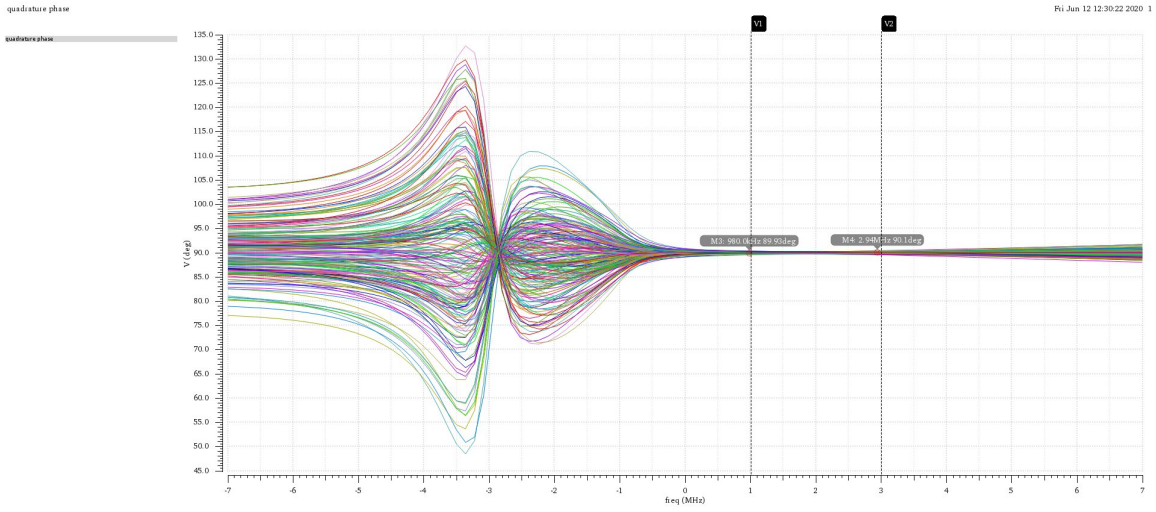


Figure 6.53: Quadrature phase mismatch of Monte Carlo simulation.

6.6.5 Noise Figure

The noise figure specification slightly differs due to mismatch, as shown in Fig. 6.54 and Fig. 6.55 for the 1 MHz- and 2 MHZ-modes, respectively.

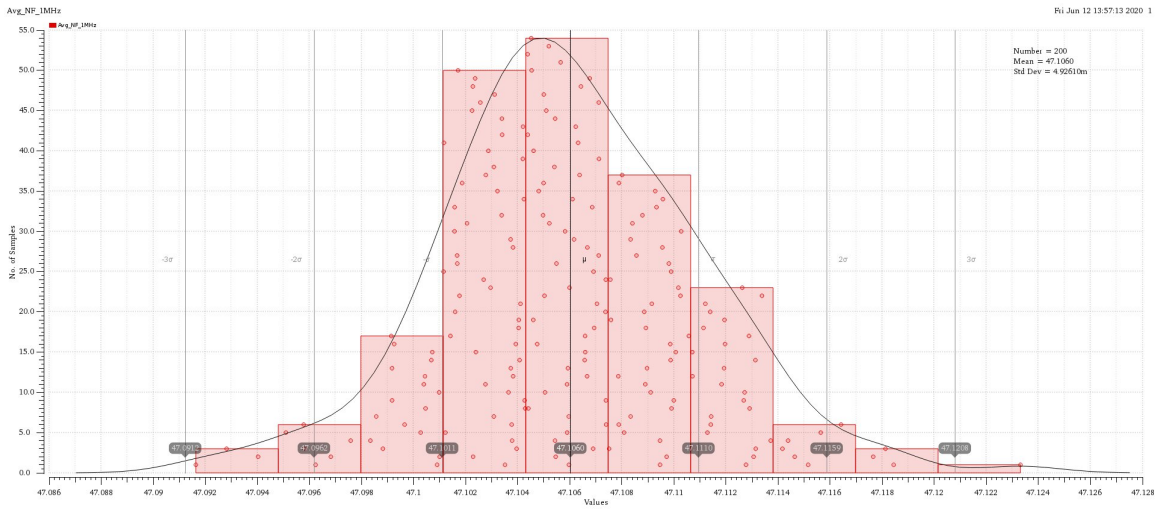


Figure 6.54: Average in-band noise figure histogram of Monte Carlo simulation in the 1 MHz-mode.

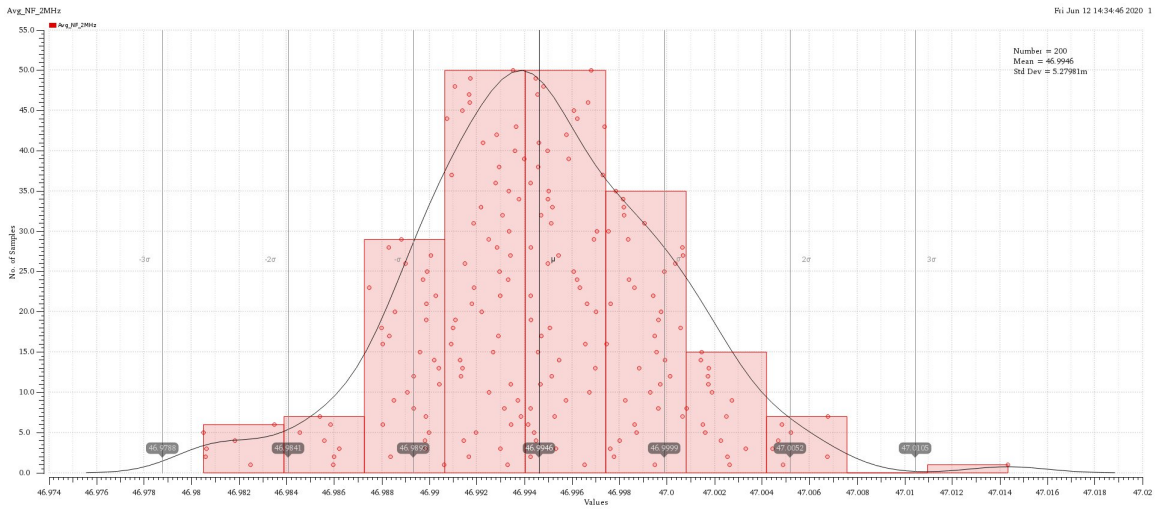


Figure 6.55: Average in-band noise figure histogram of Monte Carlo simulation in the 2 MHz-mode.

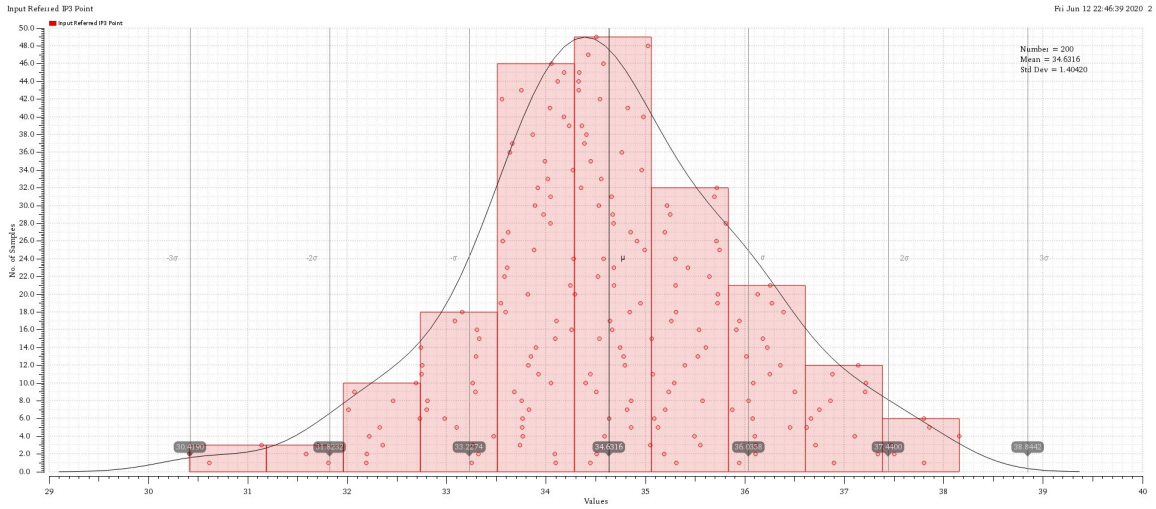


Figure 6.56: IIP3 histogram of Monte Carlo simulation in the 1 MHz-mode.

6.6.6 IIP3 test

Similarly, as shown in Fig. 6.56 and Fig. 6.57 for the 1 MHz- and 2 MHz-modes, respectively. The IIP3 value differs slightly.

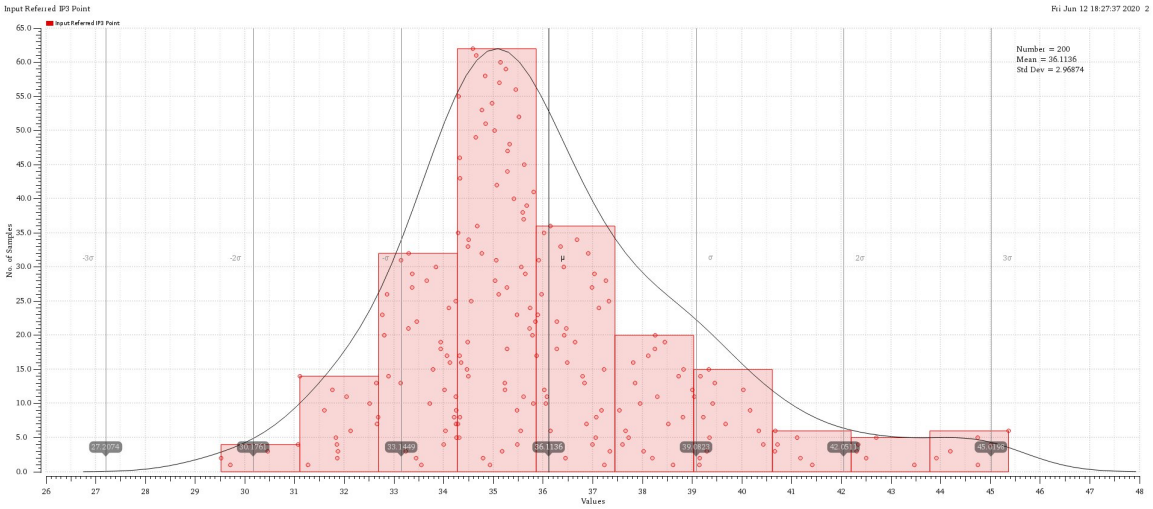


Figure 6.57: IIP3 histogram of Monte Carlo simulation in the 2 MHz-mode.

6.7 Conclusion

In this chapter, the fundamentals of the complex filter are discussed and analyzed. The filter approximation was chosen to be a 3^{rd}-order Butterworth, and was implemented as a fully-differential integrator-based Opamp-RC Complex filter for various reasons discussed. The design procedure of the OTAs and their CMFBs is discussed with the achieved results. Lastly, the filter was further optimized to obtain the required specifications across PVT corners and components mismatch and variations. It can be concluded that the 3^{rd}-order Butterworth, integrator-based Opamp-RC complex filter greatly fits the desired specifications for a standard 5.1 BLE receiver. The complex filter achieves channel-selectivity and image-rejection with high linearity and relatively low power consumption for the two IF modes.

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Chapter 7: Analog-Digital Converter

7.1 Analog to Digital Conversion Principles and Metrics

ADCs convert analog signals to digital signals. They are widely used as the interface between the analog world and DSP blocks. This section discusses some of the basics in sampling theory.

7.1.1 Sampling

Analog signals are continuous in time. They have infinite time samples that need a memory of infinite size to store and process which is not practical. Fortunately, it is proven that any band limited continuous signal can be represented by finite samples with, theoretically, no loss in information. This was introduced by Harry Nyquist in his Sampling Theory.

7.1.1.1 Sampling theory

If a signal contains no frequencies higher than BW hertz, it is completely determined by giving its ordinates at a series of points spaced $T_s = \frac{1}{2BW}$ seconds apart.

Using Sampling Theory, continuous signals could be discretized in time. Analog to digital converters use sampling as the first step to discretize the analog input signal in time so that it can be processed. The rate at which the ADC samples the analog input signal is called the Sampling Rate which is known to be one of the most important performance metrics for any ADC. Figure 7.1 shows the quantization effect of a continuous signal in the

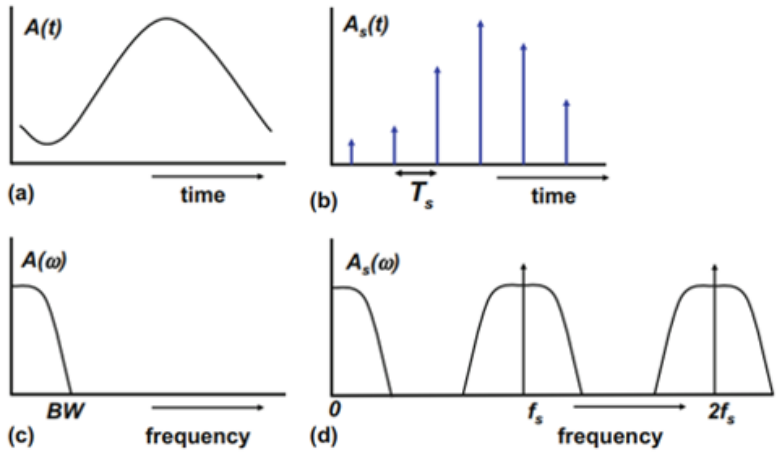

Figure 7.1: Time-domain and frequency-domian representation of CT signals [1].

frequency domain.

7.1.2 Quantization

Analog signals are continuous in amplitude. They have infinite precision that need an infinite resolution to be measured exactly which is not practical. For realizability, a loss of accuracy is inevitable as the range of values the analog signal can take at any time sample is discretized to finite values (steps) where the signal value cannot lie in between. This process is called Quantization. Figure 7.2 shows the quantization prcess.

7.2 Required specifications

The ADC discussed in this work is part of a Bluetooth low energy (BLE) transceiver chain. Bluetooth low energy requires its circuits to consume low power during operation and low leakage during shutdown mode to

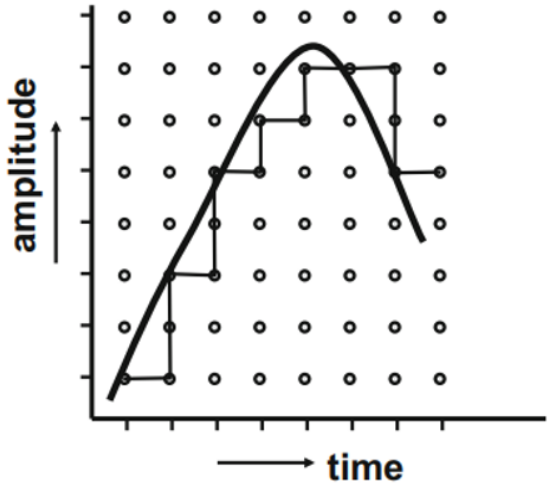

Figure 7.2: Quantization of a signal [1].

avoid draining the battery rapidly, so the target in this design is power consumption.

The specifications of the ADC were provided by Si-Vision LLC. following the Bluetooth 5.1 standard. Table 7.1 shows the required specifications.

7.3 System and Timing Design

SAR ADC has 4 main blocks: track and hold, digital-to-analog converter, comparator, and SAR logic.

- Digital to analog converter challenges:

  To avoid static power and low dynamic power, a capacitive DAC topology is chosen as section 7.4 discusses. The capacitive bank representation can be unary, binary, or segmented. The capacitive DAC topology can be conventional or split capacitor. The chosen topology and unit capacitor size directly affect noise, linearity, gain error, power consumption and speed. So it should be designed carefully.

- Comparator challenges:

Table 7.1: ADC specifications.

Paramter	Conditions	Min	Typ.	Max	Unit
Technology			TSMC65nm		
Resolution			10		bits
Junction temperature		-40	25	+125	°C
Full-scale differential input range		-400		400	mV
Input signal common mode			VDD/2		Volts
Input sampling capacitance at each input	No parasitic capacitances included		1		pF
Leakage Current			5	50	nA
Minimum T_{sample}		3	8		ns
Input reference current (i_{bias})	Poly current		5		uA
Input clock frequency (SoC)			32/16		MHz
Clock duty cycle		40	50	60	%
Data latency			1		CLK cycles
Power up time (t_{up})			1	2	uS
Analog Supply Current Consumption	32 MHz		200	240	uA
	16 MHz		100	120	uA
Digital Supply Current Consumption	32 MHz		50	160	uA
	16 MHz		25	120	uA
Reference Current Consumption	32 MHz		10	20	uA
	16 MHz		5	10	uA
Output Logic Coding	2's complement				
DNL	Note 1 – Value measured with a –0.5dB FS input signal and then extrapolated to full scale. Note 2 – The "Gain Error" parameter, as defined above, refers to the SAR ADC core with respect to the reference voltage it receives.			**1**	LSB
INL				**1**	LSB
ENOB			**9**		Bits
Offset Error (3σ)				**15**	LSB
Gain Error				**1**	%FS

The comparator offset and power consumption dominate the offset error and power consumption of the ADC. It also has a direct effect on the ADC noise as the comparator input referred noise directly adds to the noise floor of the ADC. Choosing the monotonic switching scheme adds another challenge affecting the ADC linearity as the monotonic switching scheme has different common mode levels for each comparison biasing the comparator. This introduces an input dependant offset that degrades the linearity of the ADC. In addition to that, the parasitic capacitance added to the DAC output node is also non-linear and depends highly on the value of the common mode. This is another challenge added to the stack of problems introduced due to using the monotonic switching scheme. The basic solution for this is to design the input stage of the comparator to have high a CMRR. This requires a high output impedance bias current source to bias the comparator eliminating the non-desirable effects of the common mode modulation. Given that the common mode is nominally 0.5V this will not be sufficient for the comparator to operate properly. So, a common mode lowering technique is proposed in the system as shown in section 7.4. However, the constant offset is not a challenge as a novel offset cancellation technique is introduced in this work that can cancel the overall offset of the ADC in the digital domain.

- SAR logic challenges:

  SAR logic is a digital circuitry implemented in a right manner in order to control the operation of the ADC properly. The main challenge in this system is that is chosen to work asynchronously which needs more timing circuits and more challenges.

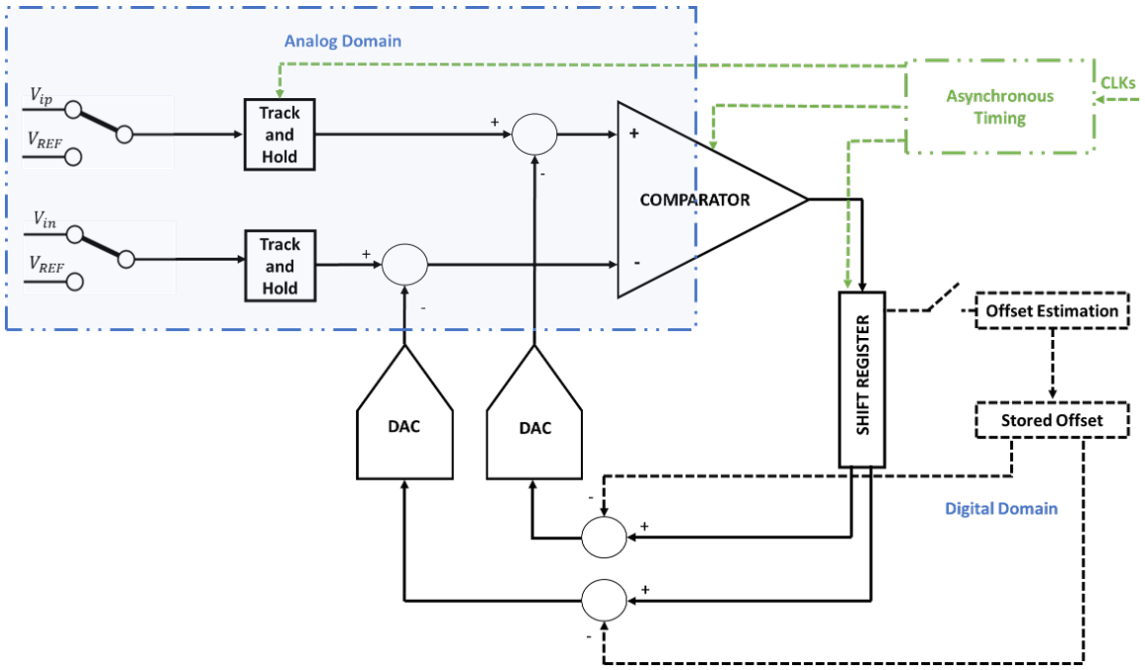

Figure 7.3: System block diagram.

- Track and hold challenges:

  The design of track and hold should be sufficiently fast and linear in order to reach the required resolution.

7.3.1 System operation

The core of the ADC is like any basic ADC: the track and hold, digital-analog converter, shift register and the comparator. The track and hold samples the input, the DAC generates the comparison reference. The shift register is used to store the output bit by bit and control the DAC to perform the binary search algorithm. The comparator is used to compare the sampled input with the comparison reference generated by the DAC.

In addition, switches and other digital circuitry are added to the ADC for it to be able to work in two modes: Normal operation mode, and Offset

evaluation mode.

7.3.2 Offset cancellation technique

This work proudly presents a novel offset cancellation technique. This technique can be described as follows.

Offset evaluation mode:

Initially, before any calibration is done, the stored offset is zero. In the offset evaluation mode, V_{REF} is connected to both terminals of the ADC instead of the differential input signal. This is done using another switch identical to the input switches and connected in parallel to it acting as a single pole double throw (SPDT) input switch. This means that the ADC is fed with $V_{in} = 0$.

Subsequently, a normal ADC conversion is carried out. The resulting digital output is in fact the input offset of the ADC. Assuming that this offset is constant and common mode independent, which can be ensured by a good comparator design, means that we now know the error value added to the signal. By subtracting this offset value from every other conversion, the ADC can operate with zero offset error regardless the value of the initial offset.

This offset stored in a register in order to be cancelled when the ADC is back to the normal operation mode.

Normal operation mode:

In this mode, the ADC has the digital signed value of the offset stored in its register. The input is reconnected to the track and hold switches and

the offset estimation circuitry is disconnected holding the last stored offset. The value of the stored offset is subtracted each conversion by manipulating the state of the DAC switches during the tracking phase. The default state of these switches during the tracking phases is connecting the capacitors to V_{ref}. The conversion phase switches flip these switches to GND depending on their current state.

The idea lies in manipulating the state of one side of the differential DAC during the tracking phases, then reconnecting them to V_{ref} when it is over. Effectively adding a certain value to the sampled input. This value is taken from the offset register and is added so as to cancel out with the systematic offset.

This means that any arbitrary offset can be cancelled out with this technique without having to add any extra circuitry or consume a significant amount of power. The offset estimation does not require a long time to be carried out. It only requires to be carried out once at the start-up of the ADC and then this value is stored for as long is it is on.

An improvement can be made to this technique by sampling the offset multiple times and taking the average of these samples in the digital domain. Then using the average value of these samples instead of just once. This eliminates the potential offset cancellation errors due to the noise added to each conversion. This noise is canceled out more and more by taking more samples and averaging them. This effect can be described as follows:

$$\sigma_{offset\ after\ averaging} = \frac{\sigma_{noise}}{\sqrt{N}} \tag{7.1}$$

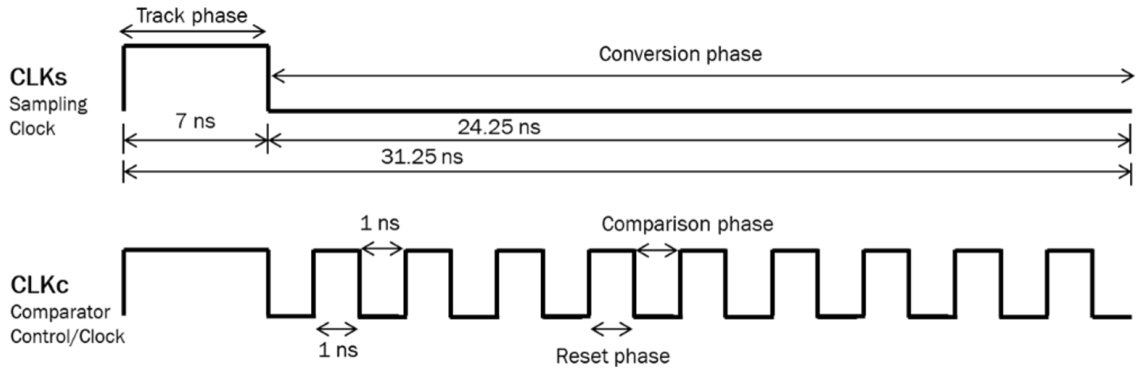

Figure 7.4: Timing design.

Where N is the number of samples taken for averaging. The limiting value when taking a large enough value for N ensures that the offset will be zero.

This method does not alter the dynamic range of the ADC unlike most other offset cancellation methods. Also, the range of offsets that could be cancelled out is greater than any other previously known technique.

7.3.3 Timing Design

The tracking phase duration should be sufficient for accurate input tracking, capacitive DAC settling and reference buffer settling. 7 ns is left for the tracking phase to relax the reference buffer specifications to be easily realizable and the remaining time is left for the quantization phase.
In the quantization phase, the comparator is required to perform 10 comparisons and 9 resets. The comparator reset phase duration should be sufficient for capacitive DAC and reference buffer to settle after switching. The comparison phase should be sufficient for the comparator digital output to be produced and stored. Accordingly, 1 ns is left for the comparison phase and 1ns for the reset phase as shown in figure 7.4.

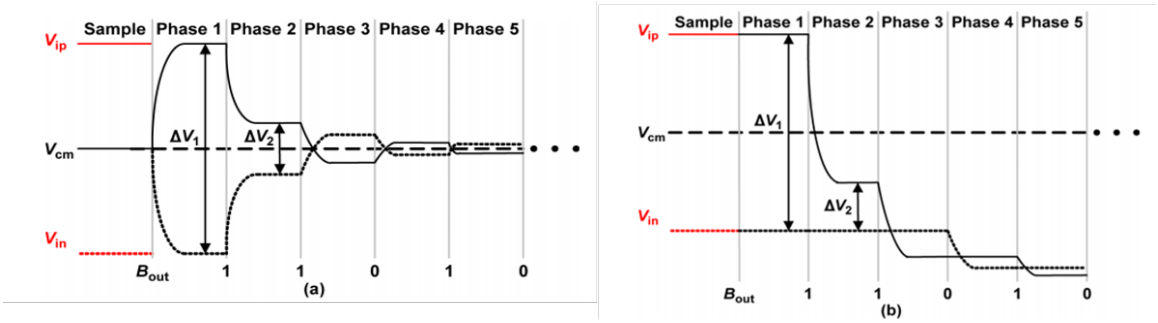

Figure 7.5: Switching Schemes: (A) Non-monotonic switching. (B) Monotonic Switching.[2]

Table 7.2: Non-monotonic vs. Monotonic Switching. [2]

	Non-monotonic	**Monotonic**
Average switching energy	$1365.3CV_{ref}^2$	$255.5CV_{ref}^2$
Area	X	0.5X
Common mode	Constant	Varying
Complexity	Needs N-bit DAC	Needs N-1-bit DAC

7.3.4 DAC switching schemes

There are two common switching schemes for any differential SAR ADC: constant common mode switching, and monotonic switching. Figure 7.5 shows the operation of these two modes. Table 7.4 shows the main differences between these two schemes.

As the design target is power, monotonic switching is the scheme of choice because it consumes 83% less power and takes 50% lower area[2]. The issue of the varying common mode is solved by designing the comparator to have a high CMRR as section 7.6 discusses.

7.3.5 Noise and nonlinearity budget

Non-linearities and noise in the ADC system add up and contribute in decreasing the SINAD of the output signal. Hence, decreasing the effective number of bits. The ENOB must not fall below 9 bits across the worst corner

and with the worst possible mismatches and noise conditions. This implies that there exists a certain budget of "Bits" that must be distributed initially on the entire design. This means that each design component will be only allowed to contribute by a certain amount of non-linearity, noise, etc...

Provided that each of these components has met its system-design implied specifications ensures that the entire system as a whole will also meet the required specifications.

Table 7.3: Noise and Nonlinearity budget

	Specification on resolution degradation sources
Comparator	SNR >64 dB
	Eliminate nonlinear offset. High CMRR.
Track and Hold	$SNR_{sampling}$ >68 dB
	THD >80 dB
Cap-DAC	THD >64 dB
Total SINAD	>58 dB

7.4 Capacitive DAC design

One of the most critical blocks of and low power ADC is the capacitive DAC. The Power consumption reduction is achieved by eliminating the static currents and depending of charge redistribution in a capacitor array. The capacitive DAC topology is also very useful because it can also be used as a passive S&H. They only consume power at the beginning of the conversion when the matrix is loaded during the tracking phase. Therefore, they are most suitable for low power applications such as BLE. One of the main problems of these capacitive DACs is that their performance is in many cases strongly affected by the parasitic capacitances. We will present an exhaustive study about the different types of capacitive DACs and multiple methods of implementation. A novel capacitor array configuration with

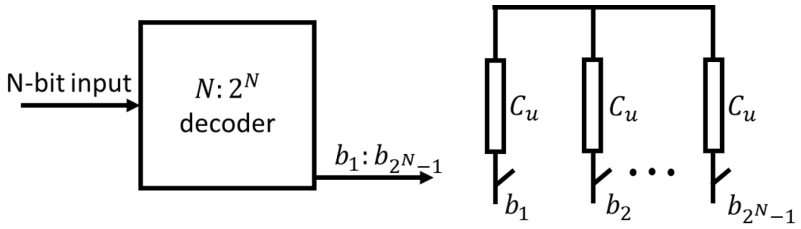

Figure 7.6: N-Bit Unary DAC.

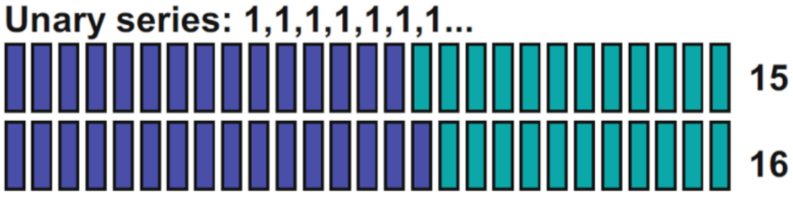

Figure 7.7: Mid-scale transition. [1]

favourable performance and characteristics will be presented. The effect of the parasitic capacitances on the performance of the capacitive-based DACs is also discussed.

Depending on their structure, the capacitive-based DACs can be divided into different subtypes.

7.4.1 Basic DAC representations

- **Unary:**

The unary representation uses a series of 2^N identical elements (elements are resistors, capacitors, currents, devices, etc.). A unary numerical value is created as:

$$B_u = \sum_{i=0}^{i=2^N-1} b_i \tag{7.2}$$

where b_i represents the i^{th} bit of the 2^N-bit output encoded from the N-bit input to the DAC.

Complexity:

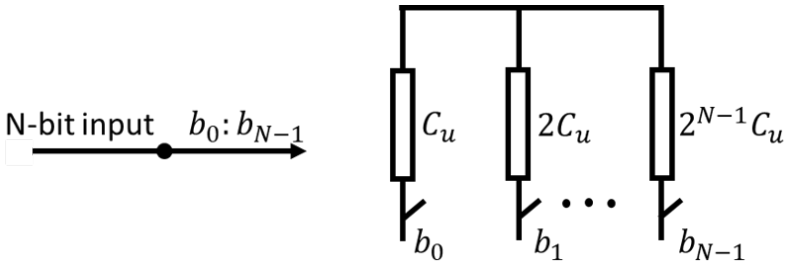

Figure 7.8: N-Bit binary DAC.

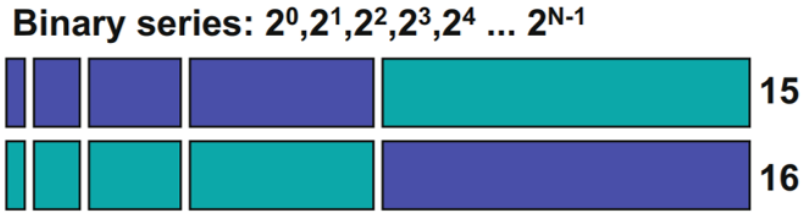

Figure 7.9: Mid-scale transition.[1]

For an N-bit unary capacitive DAC, 2^N capacitor unit is required with $2^N - 1$ switches. The number of switches increase exponentially with number of bits which makes routing is harder in higher resolutions.This is shown in figure 7.6.

INL and DNL:

The monotonicity is guaranteed in unary representation as that the unit elements are always added to represent higher values. this is shown in figure 7.7. The maximum INL and DNL are given by:

$$\sigma_{DNL} = \frac{\sigma_{C_u}}{C_u}, \quad \sigma_{INL} = 2^{\frac{N-1}{2}} \frac{\sigma_{C_u}}{C_u} \tag{7.3}$$

- **Binary:**

In order to avoid the exponential growth of components in a unary architecture, the exponential behavior must be included in the representation itself. In a binary structure the elements are chosen such that the resulting

voltages or currents form an exponential series.

$$B_b = \sum_{i=0}^{i=N-1} b_i * 2^i \tag{7.4}$$

where b_i represents the i^{th} bit of the N-bit input.

Complexity:

For an N-bit binary capacitive DAC around N capacitors are required with N switches which makes the binary representation more compact than the unary representation in routing, area, and layout as shown in figure 7.8.

INL and DNL:

The monotonicity is not guaranteed in binary representation due to that some elements are replaced by others in most of the DAc output steps. This is shown in figure 7.9. The maximum INL and DNL are given by:

$$\sigma_{DNL} = 2^{\frac{N}{2}} \frac{\sigma_{C_u}}{C_u}, \quad \sigma_{INL} = 2^{\frac{N-1}{2}} \frac{\sigma_{C_u}}{C_u} \tag{7.5}$$

From the equations binary representation shows worse linearity than unary representation but it's more compact in area and easier to route and to implement in layout.

- **Segmented**:

In high resolution $(N > 8)$ converters the better DNL performance of the unary architecture must be traded off against the smaller size of the binary architecture. Many solutions exist that combine the best of both. These "segmented" digital-to-analog converters realize N_{MSB} bit resolution with a unary architecture and combine that with an N_{LSB} bit binary structure. Figure 7.10 shows an example where the coarse unary steps are supplemented

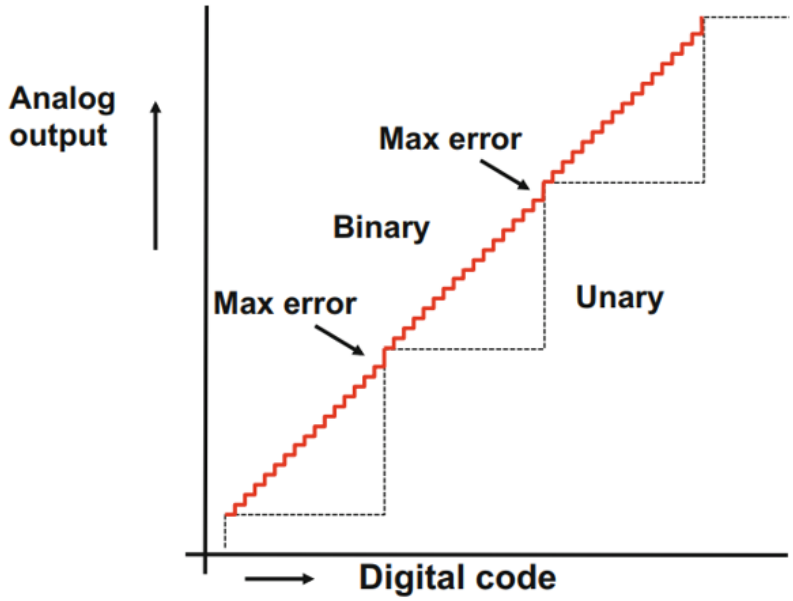

Figure 7.10: Segmented DAC maximum error transitions. [1]

by a binary addition. The unary steps must have the accuracy of an LSB, which is the smallest step of the binary structure. As the same binary structure is used for every coarse unary step, a deviation in the binary pattern will repeat over all unary sections.

For an N-bit can be divided into $N_{MSB}+N_{LSB}$ where the MSB is unary and LSB is binary to compromise between layout simplicity and nonlinearity the MSBs are decoded to $2^{N_{MSB}}-1$ signals to control the unary part and the LSB bits are use to control the binary part.

The monotonicity is not guaranteed in segmented representation and the maximum INL and DNL are given by:

$$\sigma_{DNL} = 2^{\frac{N_{binary}+1}{2}} \frac{\sigma_{C_u}}{C_u}, \quad \sigma_{INL} = 2^{\frac{N-1}{2}} \frac{\sigma_{C_u}}{C_u} \tag{7.6}$$

Table 7.4 shows a brief comparison between the three representations.

Table 7.4: Different DAC representations

Representation	**INL**	**DNL**	**No. of switches**
Unary	$\sigma_{INL} = 2^{\frac{N-1}{2}} \frac{\sigma_{C_u}}{C_u}$	$\frac{\sigma_{C_u}}{C_u}$	$2^N - 1$
Segmented		$2^{\frac{N_{binary}+1}{2}} \frac{\sigma_{C_u}}{C_u}$	$2^{N_{unary}} - 1 + N_{binary}$
Binary		$2^{\frac{N}{2}} \frac{\sigma_{C_u}}{C_u}$,	N_{binary}

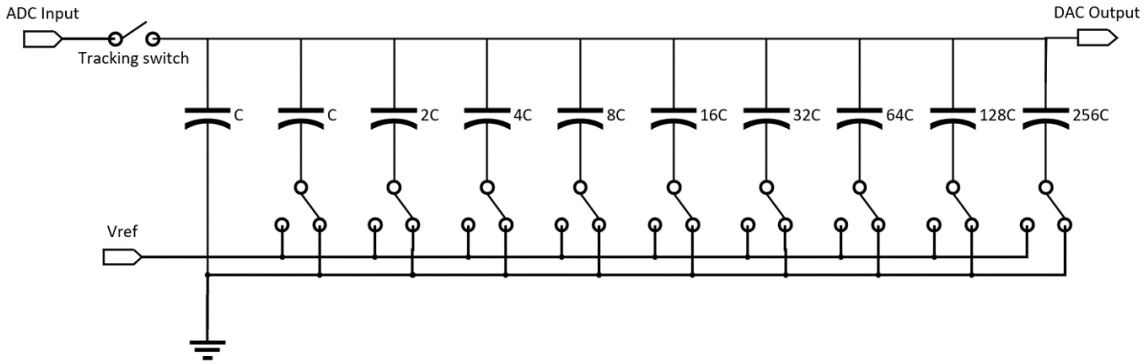

Figure 7.11: 9-Bit conventional binary DAC.

7.4.2 Implementation

Charge redistribution-based architectures have the advantage of low power operation. This was the main reason for choosing this approach. However, as the number of bit increases, input load capacitance and area of binary-weighted capacitor DAC too increase exponentially. There is, however, more than one architectural solution to this problem. Figure 7.11 shows the conventional binary weighted single ended capacitive 9-Bit DAC. In this approach, the capacitors are all connected to the input sampling switch. This is why this method gives the greatest value of input sampling capacitance. For an N-bit ADC, typically, the input sampling capacitance will be given by:

$$C_{in} = C * 2^N \tag{7.7}$$

However, since that the SAR algorithm used in this work is based on monotonic switching, the exponent is reduced to (N-1) due to the removal of the MSB capacitor. When monotonic switching is used, an (N-1)-Bit DAC is used for an N-Bit ADC.

This parasitic capacitance on the output node will cause a positive gain error on the output signal. The Gain error is given by:

$$G.E. = \frac{C_p}{C_{hold} + C_p} \tag{7.8}$$

The capacitance value in digital-to-analog converters based on binary capacitor arrays requires some trade-off. For instance, the choice for the unit capacitor and the lowest capacitor value is determined by both the $\frac{kT}{C}$ noise of the total array, and also the technological limit of the minimum size a capacitor could be made. It is technologically difficult to fabricate accurately a capacitor far below a $1fF$ value. And it is very hard to keep the parasitics under control. Increasing the size of the unit capacitor will increase the input capacitance which may conflict with the speed requirements and this also increases the power requirements of the circuit.

For large number of bits, or when the input sampling capacitance is required to be low for low power and speed requirements, the split capacitor array is the solution. Using this method, LSB value is extended. An auxiliary capacitor array is used instead of the LSB unit capacitor. Its equivalent value is still one unit capacitance, hence, not contributing to the total input sampling capacitance of the DAC while still increasing the resolution.

The bridging capacitor, see figure 7.12, is an elegant solution to implement the voltage division. In this example the four MSB bits are formed in a conventional binary fashion. The LSB bits use a bank with the same size

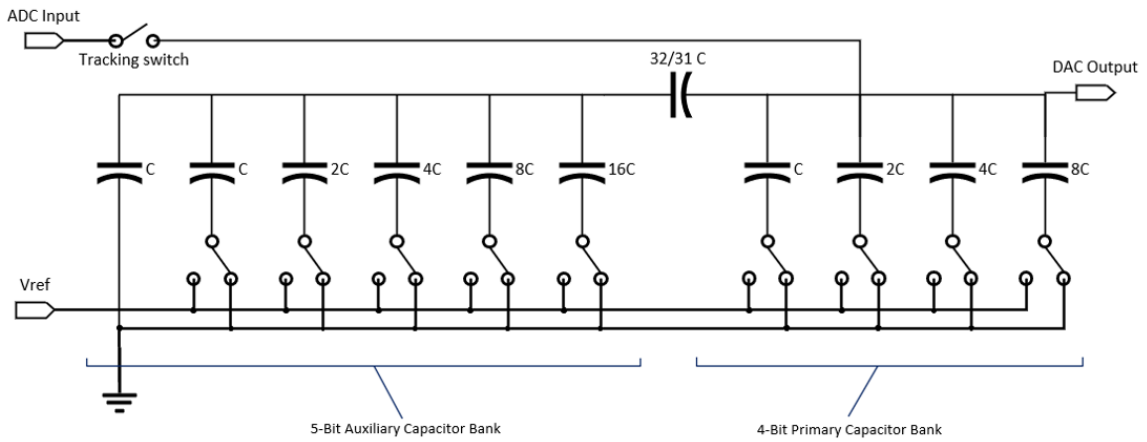

Figure 7.12: 9-Bit split capacitor DAC.

capacitors but are coupled via a bridging capacitor C_{bridge} to the MSB side.

C_{bridge} has a fractional value of typically $\left(\frac{2^n}{2^n-1} \times C_0\right)$, where n is the number of bits of the auxiliary capacitor bank. That way, the two capacitor banks have the same scaling. In the charge redistribution, the total weight of the left array is equal to the total weight of the lowest bit in the right array.

The analysis for this topology is presented here to prove that further improvements can be devised.

Figure 7.13 shows a simple example for a 6-Bit split capacitor DAC that is comprised of an m=3 bits primary DAC and an n=3 bits auxiliary DAC.

First, we can derive the value of the bridge capacitor CB. For this case with n=3, the equivalent capacitance of the auxiliary capacitor array connected in series with the bridge capacitor must be equal to the unit capacitance C. That way, from the primary array's perspective, the entire auxiliary array is equivalent to the dummy single unit capacitor in the normal non-split capacitor DAC case. Therefore, its value can be calculated to be:

$$\frac{1}{\frac{1}{C_B}+\frac{1}{8C}} = C \tag{7.9}$$

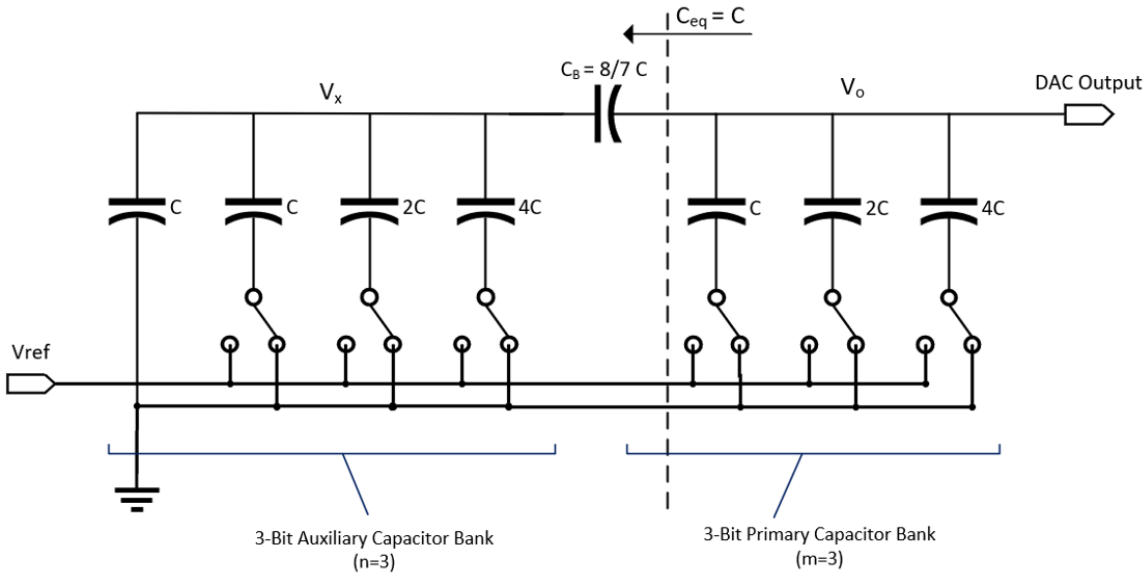

Figure 7.13: 6-Bit split capacitor DAC.

Therefore:

$$C_B = \frac{8}{7}C \tag{7.10}$$

Or generally, for arbitrary n and m:

$$\frac{1}{\frac{1}{C_B} + \frac{1}{2^n C}} = C \tag{7.11}$$

Therefore:

$$C_B = \frac{2^n}{2^n - 1}C \tag{7.12}$$

In this case, changing the MSB (Most Significant Bit) switch position from GND to V_{ref} yields a $\Delta V_o = \frac{V_{ref}}{2}$ as expected, which can be verified as follows: Assuming zero initial conditions for simplicity, the value of V_o after flipping the switch is equivalent to ΔV_o with non-zero initial conditions. Charge conservation applies:

$$0 = V_o * (C + C + 2C) + \left(V_o - V_{ref}\right) * 4C \tag{7.13}$$

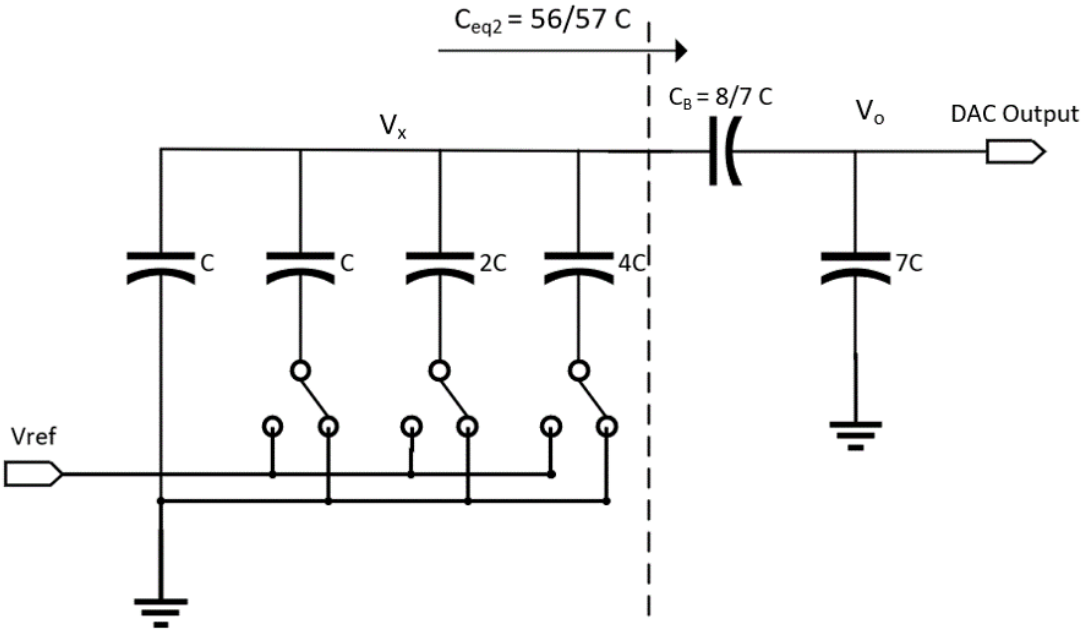

Figure 7.14: Auxiliary DAC analysis.

Therfore:

$$\Delta V_o = \frac{V_{ref}}{2} \tag{7.14}$$

This was the intuitive case of switching on of the primary array's bits. The auxiliary bits work differently and require more analysis.

In this case, as shown in figure 7.14, the entire primary array can be reduced to its equivalent capacitor of 7C. changing the LSB (Least Significant Bit) switch from GND to V_{ref} is expected to cause a ΔV_o of $\frac{V_{ref}}{64}$ since that this is a 6-Bit DAC. This could be verified as follows:

The equivalent capacitance at the bridge capacitor seen from the auxiliary array side can be calculated to be:

$$C_{eq2} = \frac{\frac{8}{7}C * 7C}{\frac{8}{7}C + 7C} = \frac{56}{57}C \tag{7.15}$$

This way, ΔV_x can be calculated and hence, ΔV_o is derived from it using

the capacitor divider formula.

$$\Delta V_x = V_{ref} * \frac{C}{8C + C_{eq2}} = V_{ref} * \frac{1}{8 + \frac{56}{57}} = \frac{57}{512} V_{ref} \tag{7.16}$$

Since that:

$$\Delta V_o = \Delta V_x * \frac{\frac{8}{7}C}{\frac{8}{7}C + 7C} = \frac{8}{57}\Delta V_x \qquad (capacitive\ divider) \tag{7.17}$$

Therefore:

$$\Delta V_o = \frac{8}{57} * \frac{57}{512} V_{ref} = \frac{V_{ref}}{64} \tag{7.18}$$

Generally, for arbitrary n and m, and for an arbitrary switched capacitor in the auxiliary cap array, the same derivation applies. In case that $x * C$ out of the $2^n C$ capacitors is switched from GND to V_{ref}, and assuming zero initial conditions:

$$C_{eq2} = \frac{C_B * C_{primary}}{C_B + C_{primary}} = \frac{\frac{2^n}{2^n - 1} * (2^m - 1)}{\frac{2^n}{2^n - 1} + (2^m - 1)} * C \tag{7.19}$$

$$V_x * \left((2^n - x)C + C_{eq2}\right) + \left(V_x - V_{ref}\right) * xC = 0 \tag{7.20}$$

Therefore:

$$\Delta V_x = \frac{x}{2^n + \frac{C_{eq2}}{C}} \tag{7.21}$$

Also, using the capacitive divider formula:

$$\Delta V_o = \frac{\frac{2^n}{2^n - 1} * C}{\frac{2^n}{2^n - 1} * C + (2^m - 1) * C} * \Delta V_x \tag{7.22}$$

$$= \frac{\frac{2^n}{2^n - 1} * C}{\frac{2^n}{2^n - 1} * C + (2^m - 1) * C} * \frac{x}{2^n + \frac{C_{eq2}}{C}} \tag{7.23}$$

$$= \frac{\frac{2^n}{2^n-1}}{\frac{2^n}{2^n-1}+(2^m-1)} * \frac{x}{2^n+\frac{C_{eq2}}{C}} \tag{7.24}$$

$$= \frac{\frac{2^n}{2^n-1}}{\frac{2^n}{2^n-1}+(2^m-1)} * \frac{x}{2^n+\frac{\frac{2^n}{2^n-1}*(2^m-1)}{\frac{2^n}{2^n-1}+(2^m-1)}} \tag{7.25}$$

$$= \frac{\frac{2^n}{2^n-1}*x}{\left(\frac{2^n}{2^n-1}+(2^m-1)\right)2^n+\frac{2^n}{2^n-1}*(2^m-1)} \tag{7.26}$$

$$= \frac{x}{2^n+(2^m-1)(2^n-1)+(2^m-1)} \tag{7.27}$$

Therefore:

$$\Delta V_o = \frac{x}{2^{n+m}} \tag{7.28}$$

Which proves that this topology works linearly for any value of n or m.

As stated before, this topology is used to solve the problems that appear with the conventional binary weighted DAC. The trade-offs for using this topology however is that the fractional value of the bridge capacitor causes poor matching with other capacitors. The capacitors in any capacitor array are typically built from multiple copies of similar unit capacitors. That way, matching is greatly improved due to the independence on the absolute value of the capacitor rather the relative values of the array sub-units.

The linearity here is heavily dependent on the matching of the bridge capacitor fractional value to the unit capacitance value. Also, the parasitic capacitance that may be present due to routing or other connected components (like the comparator in the ADC case) is also responsible for degrading the performance of the DAC. Like in the conventional binary weighted DAC, parasitics at the output node cause a positive gain error

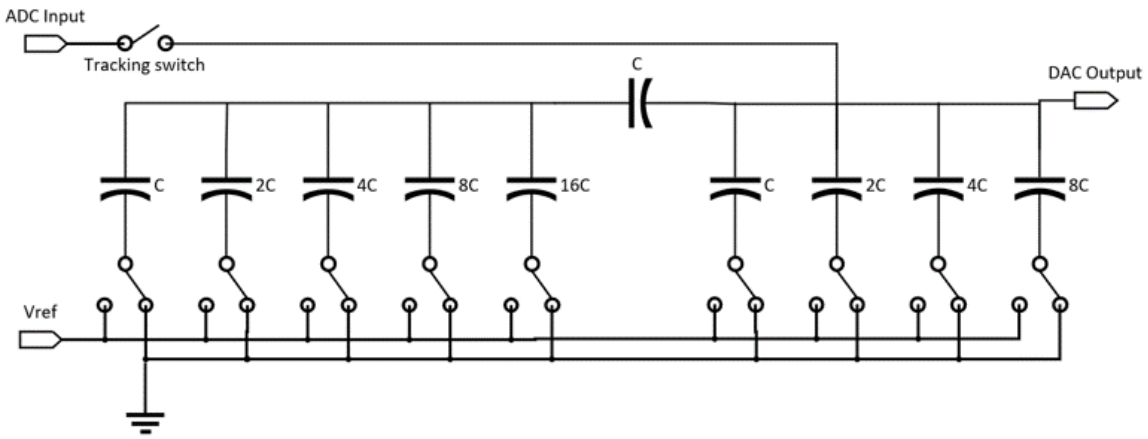

Figure 7.15: Proposed Split-Capacitor DAC.

which can be calculated as:

$$G.E. = \frac{C_p}{C_p + 2^m \cdot C} \tag{7.29}$$

This gain error is greater than the conventional case because here it depends on the ratio of the parasitic capacitance to the capacitance of the primary DAC only.

On the other hand, parasitic capacitance on the floating node causes an inherent non-linearity. This is the main drawback from using this topology. Routing parasitics must be kept to a minimum to reduce the effect of this non-linearity. Increasing the value of the unit capacitor can also reduce the effect of this non-linearity.

7.4.3 Proposed Split-Capacitor DAC

In this topology, as shown in figure 7.15, a unit bridge capacitor is implemented, and the dummy capacitor (C) is removed. This already solves one of the greatest challenges of implementing the split capacitor DAC, which is the matching of the fractional value capacitor. This topology however has

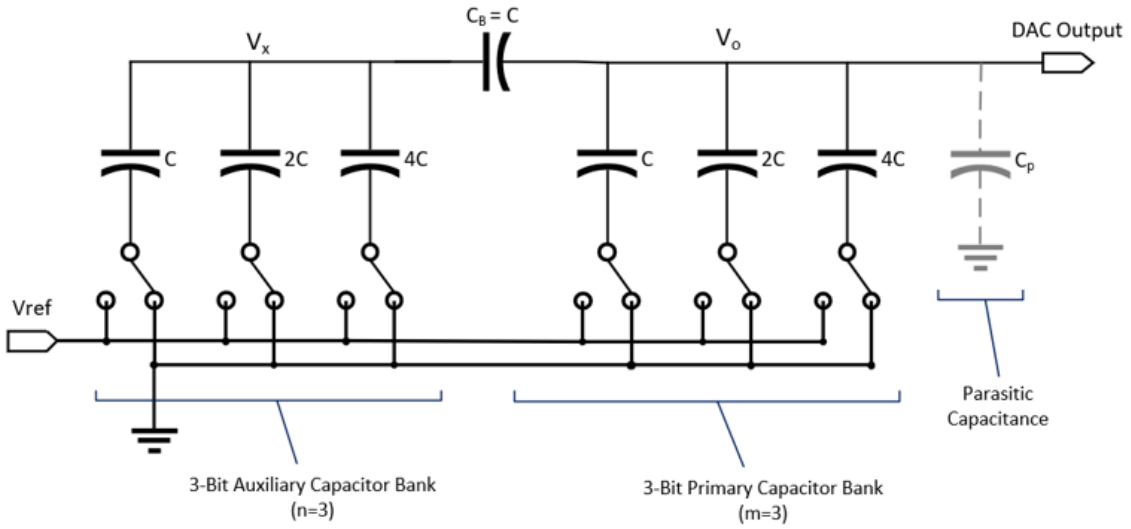

Figure 7.16: 6-Bit version of the proposed DAC.

an inherent -1 LSB gain error. This my seem like a drawback at first, but in reality, it is one of its merits. The parasitic capacitance at the output node introduces a positive gain error. This means that the inherent negative gain error cancels out some of the gain error introduced due to parasitics. This goes to show that this topology is a better alternative to the previous one in every way. The analysis for this topology is as follows:

As before, a simpler 6-bit example is shown in figure 7.16. However, to make the analysis easier, the parasitic capacitance (C_p) should be taken into consideration. It is divided into two parts: C_{p1} and C_{p2} as shown in figure 7.17.

C_{p1} part is responsible for cancelling out the negative gain error by completing the equivalent capacitance of the auxiliary DAC to a whole unit capacitance value. Without it, the equivalent capacitance is given by:

$$C_{eq} = \frac{C * 7C}{C + 7C} = \frac{7}{8}C \tag{7.30}$$

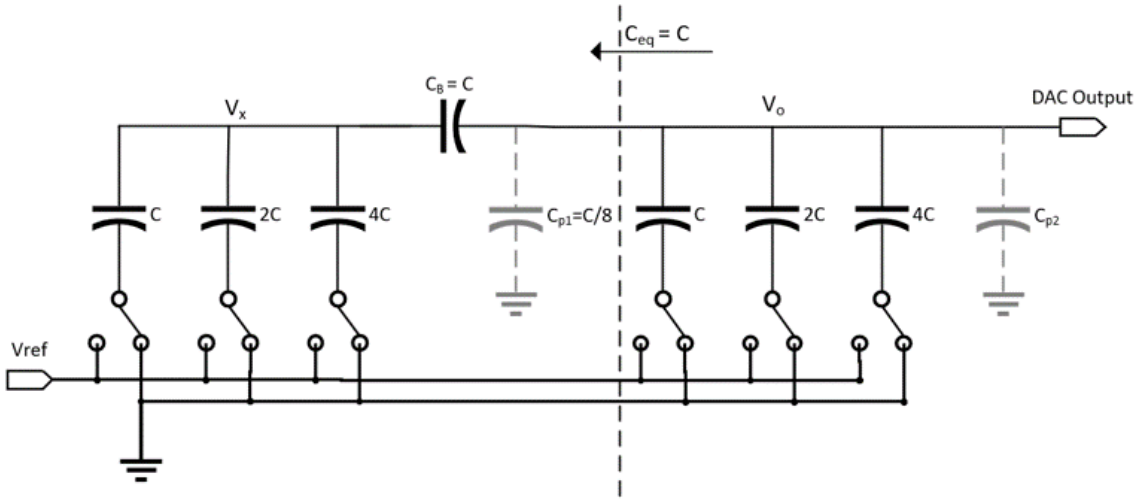

Figure 7.17: Parasitic capacitance distribution.

This is why C_{p1} is considered $\frac{1}{8}C$. Generally for arbitrary n and m, C_{eq} would be given by:

$$C_{eq} = \frac{2^n - 1}{2^n} C \tag{7.31}$$

Therefore, generally:

$$C_{p1} = \frac{1}{2^n} C \tag{7.32}$$

As for C_{p2}, it will only be responsible for a positive gain error like previously discussed topologies. Hence, its effect will be ignored in further analysis.

When a capacitor is switched in the primary array side, this case is exactly like the previous topology and works the same way. On the other hand, switching the capacitors of the auxiliary DAC requires further analysis for validation.

Once more, the entire primary array can be reduced to its equivalent capacitor of 7C. changing the LSB switch from GND to V_{ref} is expected to cause a ΔV_o of $\frac{V_{ref}}{64}$ for proper operation.

The equivalent capacitance at the bridge capacitor seen from the auxiliary

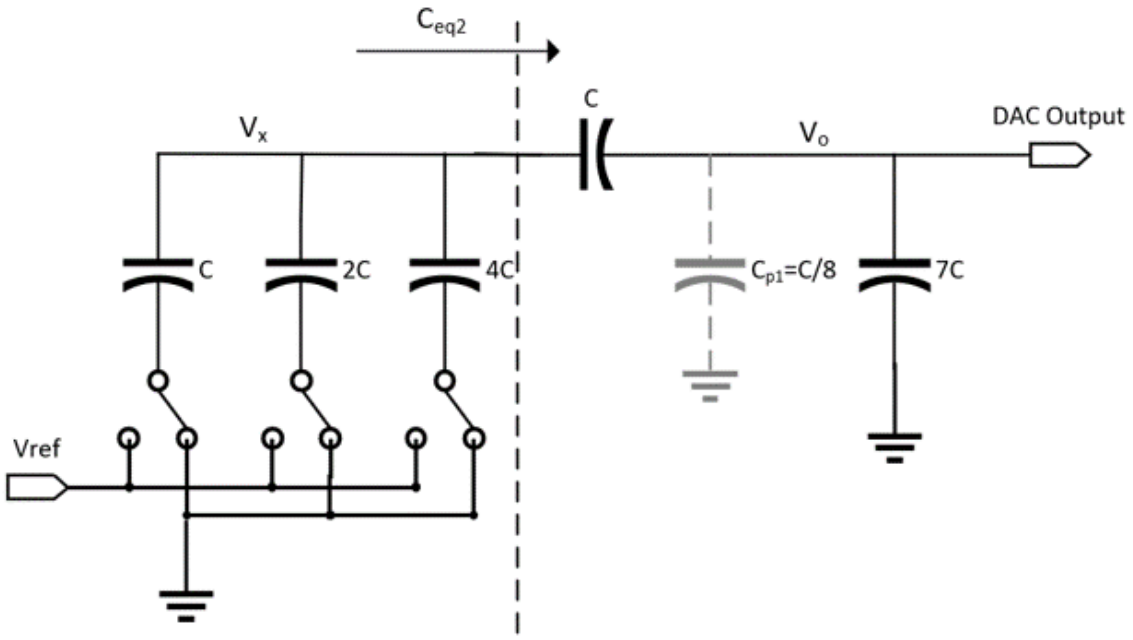

Figure 7.18: Equivalent Capacitance from the auxiliary DAC side.

array side can be calculated to be:

$$C_{eq2} = \frac{C * \left(7C + \frac{C}{8}\right)}{C + 7C + \frac{C}{8}} = \frac{57}{65}C \tag{7.33}$$

This way, ΔV_x can be calculated and hence, ΔV_o is derived from it using the capacitor divider formula.

$$\Delta V_x = V_{ref} * \frac{C}{7C + C_{eq2}} = V_{ref} * \frac{1}{7 + \frac{57}{65}} = \frac{65}{512}V_{ref} \tag{7.34}$$

Since that:

$$\Delta V_o = \Delta V_x * \frac{C}{C + 7C + \frac{C}{8}} = \frac{8}{65}\Delta V_x \tag{7.35}$$

Therefore:

$$\Delta V_o = \frac{8}{65} * \frac{65}{512}V_{ref} = \frac{V_{ref}}{64} \tag{7.36}$$

Generally, for arbitrary n and m, and for an arbitrary switched capacitor

in the auxiliary cap array, the same derivation applies. In case that $x*C$ out of the 2^nC capacitors is switched from GND to V_{ref}, and assuming zero initial conditions:

$$C_{eq2} = \frac{C_B * (C_{primary} + C_{p1})}{C_B + (C_{primary} + C_{p1})} = \frac{2^m - 1 + \frac{1}{2^n}}{2^m + \frac{1}{2^n}} * C \tag{7.37}$$

$$V_x * \left((2^n - 1 - x)C + C_{eq2}\right) + \left(V_x - V_{ref}\right) * xC = 0 \tag{7.38}$$

Therefore:

$$\Delta V_x = \frac{x}{2^n - 1 + \frac{C_{eq2}}{C}} \tag{7.39}$$

Also, using the capacitive divider formula:

$$\Delta V_o = \frac{C}{C + \left(2^m - 1 + \frac{1}{2^n}\right) * C} * \Delta V_x \tag{7.40}$$

$$= \frac{1}{2^m + \frac{1}{2^n}} * \frac{x}{2^n - 1 + \frac{C_{eq2}}{C}} \tag{7.41}$$

$$= \frac{1}{2^m + \frac{1}{2^n}} * \frac{x}{2^n - 1 + \frac{2^m - 1 + \frac{1}{2^n}}{2^m + \frac{1}{2^n}}} \tag{7.42}$$

$$= \frac{x}{\left(2^m + \frac{1}{2^n}\right)(2^n - 1) + 2^m - 1 + \frac{1}{2^n}} \tag{7.43}$$

$$= \frac{x}{2^{n+m} - 2^m + 1 - \frac{1}{2^n} + 2^m - 1 + \frac{1}{2^n}} \tag{7.44}$$

Therefore:

$$\Delta V_o = \frac{x}{2^{n+m}} \tag{7.45}$$

Which once again proves that this proposed topology performs linearly for arbitrary n and m.

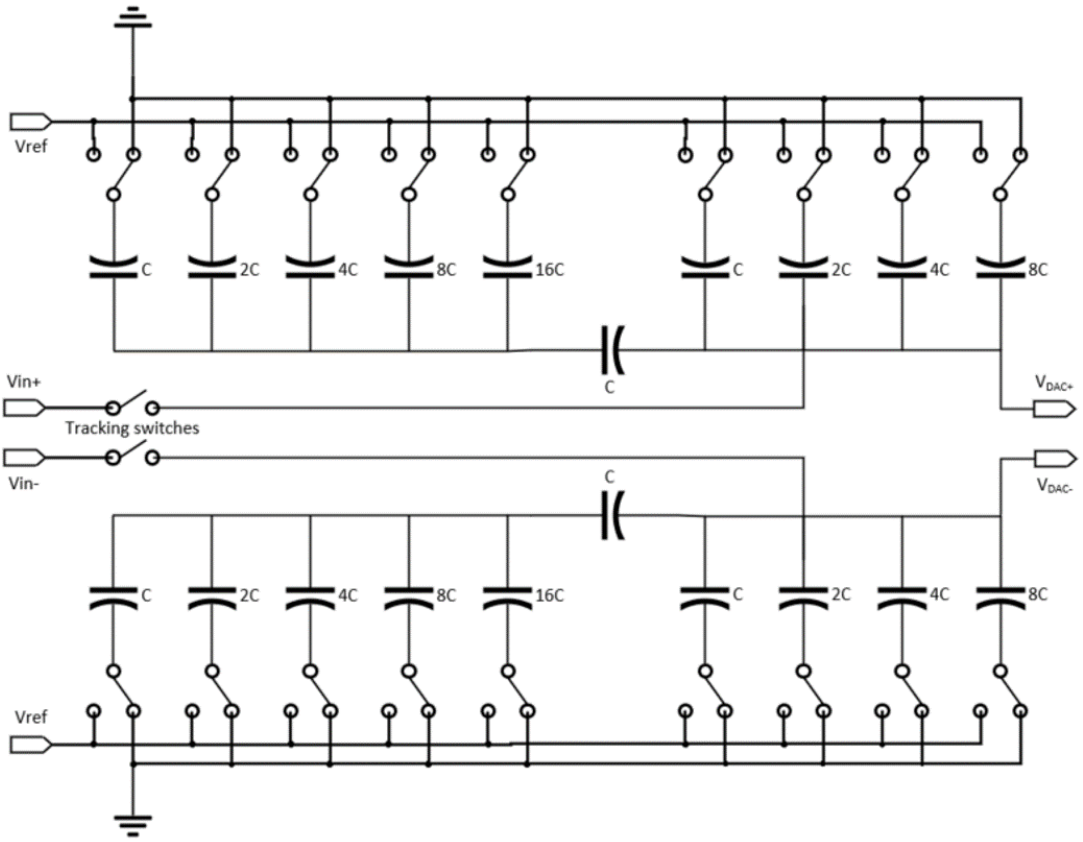

Figure 7.19: Differential DAC.

7.4.4 Differential DAC

Since that the ADC is differential, the DAC is also required to be differential. The same concepts apply. Figure 7.19 shows the final proposed differential DAC design.

7.4.5 Capacitor Types

There are many ways to implement capacitors on-chip. Each type of capacitor has its merits and demerits.

- Metal-insulator-metal (MIM): Vertical field capacitor

A special capacitor metal layer is added to the stack. These capacitors

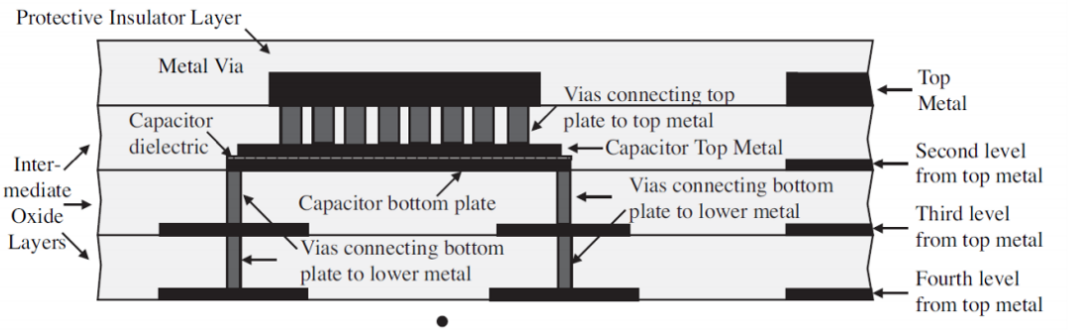

Figure 7.20: MIM cap structure.

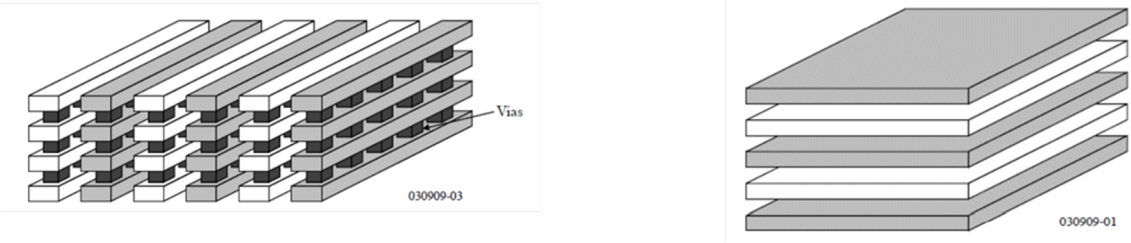

Figure 7.21: Two examples for MOM capacitor implementations.

have a highly linear capacitance with very low voltage coefficient (less than -100ppm/V, can be neglected in most cases). The parasitic capacitance on the bottom plate can account to up to 2-% of the total capacitance. There exists a technology dependent minimum value capacitance that could be achieved using MIM caps. Figure 7.20 shows a cross-section of the silicon stack with a MIM cap.

- Metal-oxide-metal (MOM): Lateral and vertical field

Capacitors made using the parasitic capacitance between the metal lines or metal plates placed in normal metal layers. Therefore, they do not need an extra special mask to manufacture unlike the MIM capacitors. Arbitrarily low value capacitances can be achieved using MOM caps. MOM caps typically have worse area efficiency compared to MIM caps. However, MOM caps designed to depend on lateral fields have balanced parasitics.

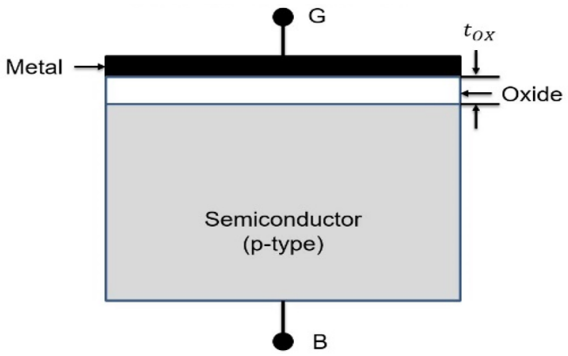

Figure 7.22: MOS capacitor.

MOM capacitors also have a highly linear capacitance with very low voltage coefficient that can also be neglected. Figure 7.21 shows two examples for MOM capacitor implementations.

- MOSCAP: highest density, but highly non-linear

NMOS or PMOS devices can be used as capacitors. This is very useful when linearity is not an issue. Accurate DACs cannot be made from this type of capacitors.Figure 7.22 shows the MOSCAP.

7.4.6 Analysis and simulations

In this work, MIM caps were used to implement the capacitive DAC. Random mismatch between the capacitors in any capacitive DAC topology lead to the existence of differential and integral non-linearities (DNL and INL). These nonlinearities decrease with increasing the capacitor area. MATLAB is used to find the smallest value of the unit capacitor that could be used without sacrificing monotonicity or linearity.

To do this, we first need to experimentally measure the standard deviation of the variation of the capacitors in the used technology. This is done by running a Monte Carlo process and mismatch variation analysis on

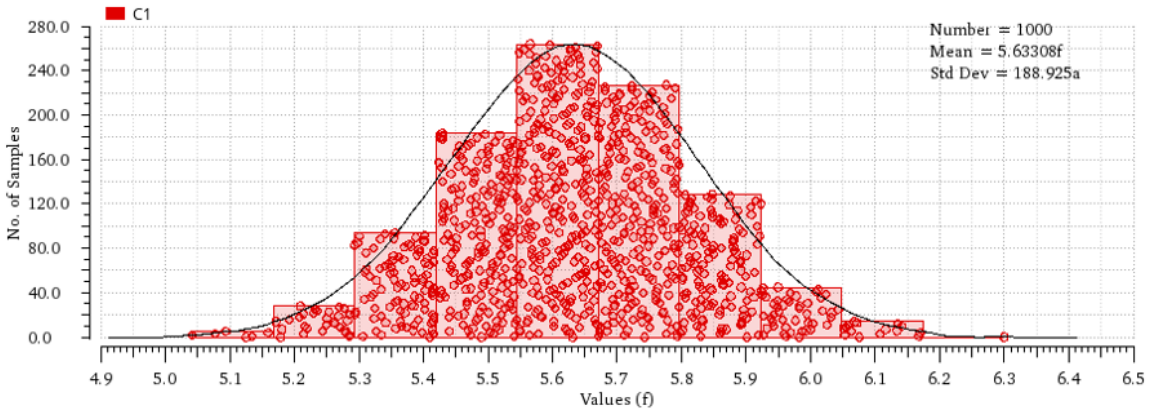

Figure 7.23: Capacitance variation across process corners and mismatch.

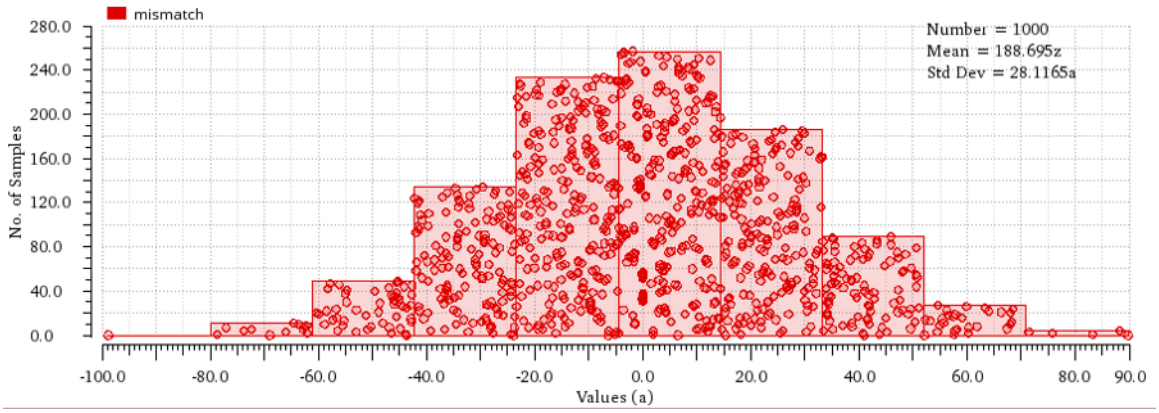

Figure 7.24: Mismatch between two capacitors.

two capacitors and plotting the value of their capacitances along with the difference between them (mismatch).

The simulation results are shown in figures 7.23 and 7.24. The capacitors used have an area of $2\mu m \times 2\mu m$ corresponding to a nominal capacitance of $5.633fF$ which is the smallest capacitor size available in the TSMC65nm kit.

For each capacitor, the capacitance varies across the process corners and due to mismatch. Figure 7.23 shows this variation. The mean value is $5.633\mu F$. The mismatch effect alone, however, can be derived from the difference between them. The difference is shown in figure 7.24.

The resulting standard deviation of this random variable is $28.11aF$. The

mismatch standard deviation is this value divided by the square root of 2. Hence, for an area of 4×10^{-12} μm^2 The standard deviation (σ) turns out to be $19.87aF$. The normalized standard deviation ($\frac{\sigma}{\mu}$) is hence calculated to be 3.5286×10^{-3}.

Pelgrom's law states that the mismatch between two identical capacitors reduces inversely with its area. [1]

$$\sigma^2 = \frac{A_p^2}{WL} \tag{7.46}$$

Where A_p is Pelgrom's constant, W and L are the dimensions of the capacitor. From the previous results, Pelgrom's constant can be calculated to be used in the MATLAB simulations.

$$A_p = \sigma\sqrt{WL} = 3.5286 \times 10^{-3} \times \sqrt{4 \times 10^{-}12} = 7.057 \times 10^{-9}\ F.meter \tag{7.47}$$

Having calculated the Pelgrom constant, a MATLAB simulation model for our proposed differential capacitor bank architecture is coded and used to find the worst INL and DNL for this architecture for different capacitor sizes. The minimum usable capacitor size is the one that gives a $3-\sigma$ INL or DNL of 1. Using this capacitor size exactly ensures a yield of 99.73%.

This value turns out to be $1.92\mu m \times 1.92\mu m$ which is smaller than the smallest manufacturable capacitor size. Which means that any capacitor size we pick will be usable in this topology and number of bits. The smallest MIM capacitor size manufacturable using the TSMC65nm Kit is $2\mu m \times 2\mu m$ which corresponds to a capacitance of $5.633fF$.

Figures 7.25 and 7.26 show the results of the MATLAB simulations calculated from the statistical data of 10,000 random iterations at this

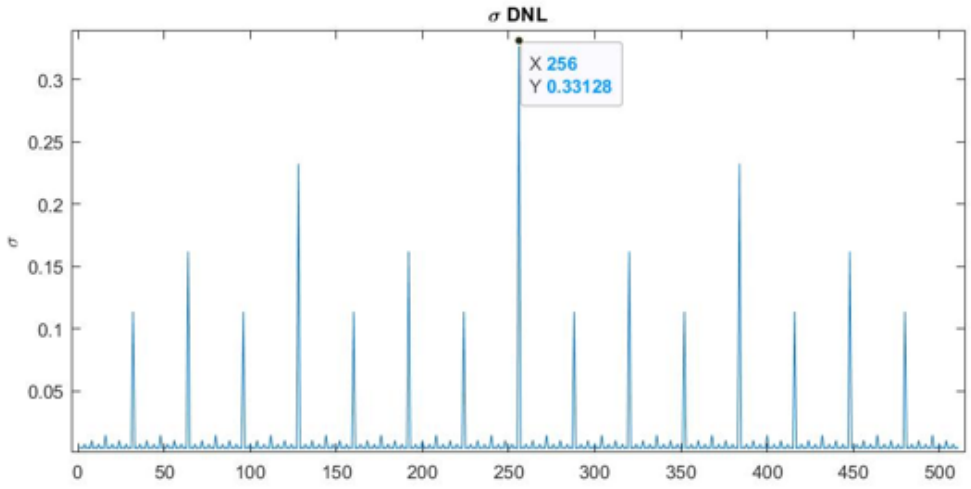

Figure 7.25: DNL.

limiting value.

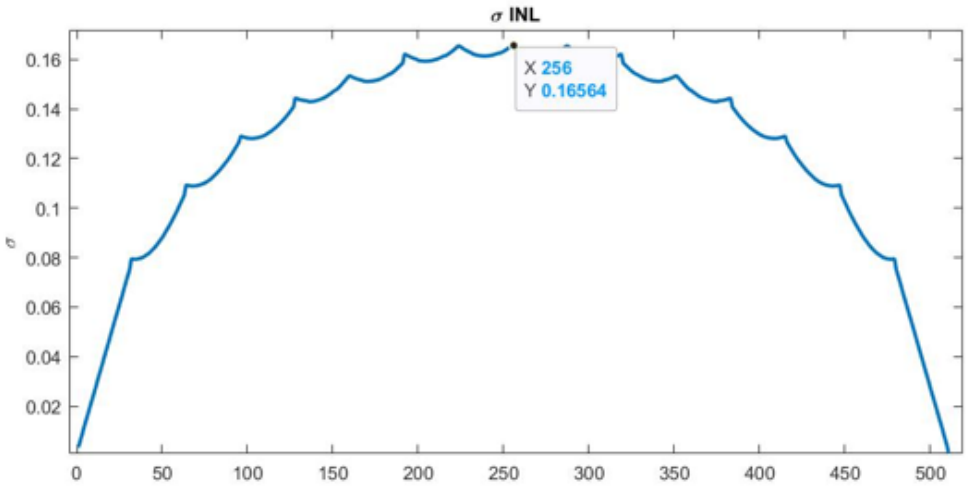

Figure 7.26: INL.

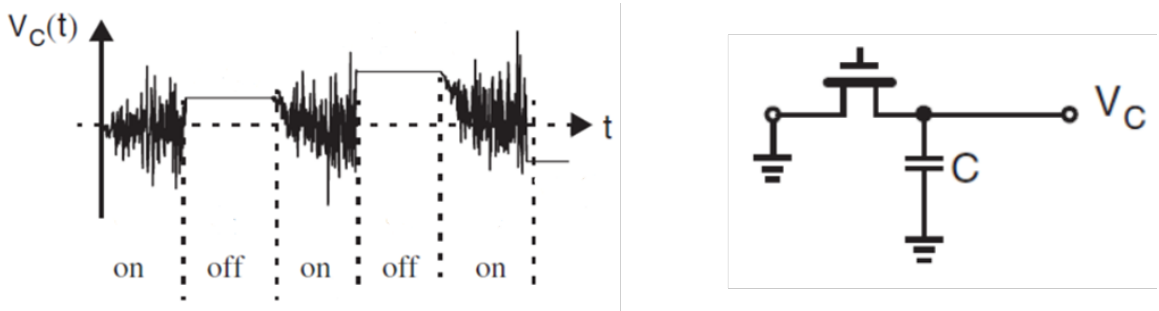

Figure 7.27: Thermal sampled noise.

7.4.7 Sampled Thermal Noise

The value of the input capacitance directly determines the sampling noise of the ADC, and it is given by the following formula:

$$P_n = \frac{2kT}{C} \tag{7.48}$$

The thermal noise must be much lower than the quantization noise in order not to cause any significant degradation in the signal to noise ratio.

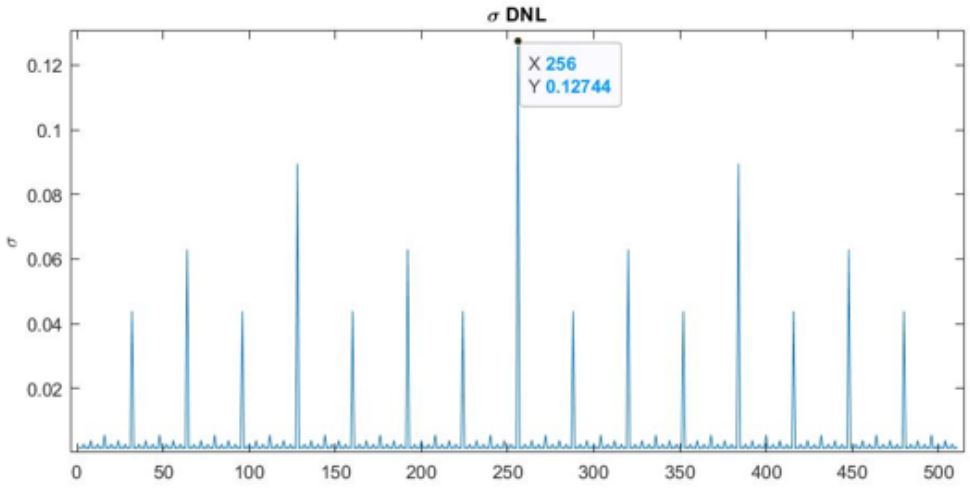

Figure 7.28: DNL of the implemented capacitor size.

The SNR due to the thermal noise only can be calculated as follows:

$$SNR = 20Log\left(400m\right) - \left(10Log\left(2kT\right) - 10Log\left(C\right)\right) \tag{7.49}$$

The worst-case noise is when the temperature is at its upper limit $125°C$. Setting the SNR to a minimum worst-case value of 68dB will cause a maximum degradation in the effective number of bits (ENOB) by 0.2 Bits. This happens when the input capacitance is $433fF$. Since that the input sampling capacitance comprises of 16 C_u this gives another lower limit to the minimum value of usable unit capacitance of $27fF$.

The value of the unit capacitance is chosen to be $29.5fF$ as a safety margin for when the value of the capacitors decreases across the process corners. The dimensions of the unit capacitor in this case is $5\mu m \times 5\mu m$. Using this value produces the following results. Figure 7.28 shows the standard deviation of the DNL with a maximum value of 0.12744 and figure 7.28 shows the standard deviation of the INL with a maximum value of 0.0637 ensuring high linearity and guaranteed monotonicity.

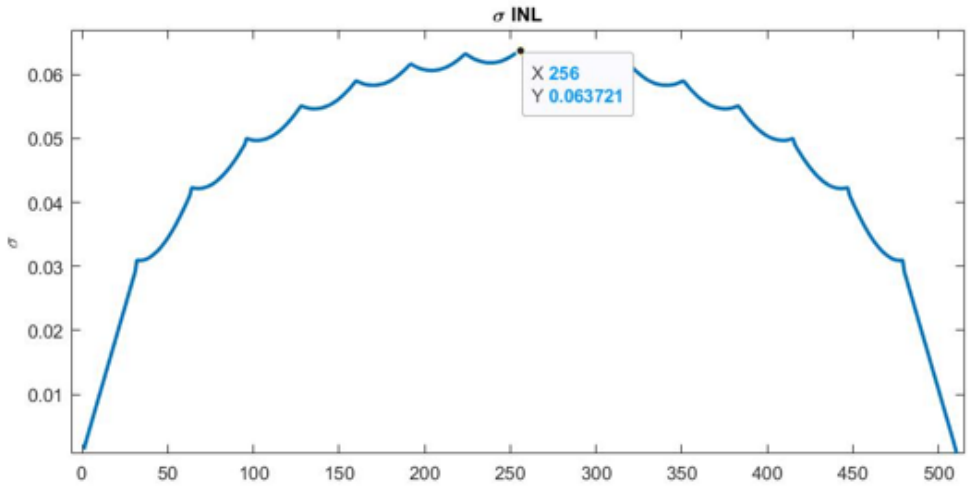

Figure 7.29: INL of the implemented capacitor size.

7.4.8 Common-Mode Lowering

The input signal initially has a common mode of $\frac{VDD}{2}$. This, and the fact that monotonic switching scheme is used, makes the comparator's work much harder. This means that it has to operate successfully, meeting its required speed, power and noise specifications across a wider range of input common modes. This is possible to implement but will certainly not be an optimal solution. This was the motivation behind this common mode lowering technique.

The second most significant bit capacitor switch is modified. Every other switch has to connect its capacitor to Vref or GND. This switch is modified as shown in figure 7.30 to be a single pole triple throw switch (SPTT), having a third terminal connected to VDD.

Relying on the same concept behind our proposed offset cancellation technique, these switches are connected to VDD during the tracking phase instead of being connected to Vref. When the tracking is complete, they are switched back to Vref. Effectively lowering the common mode of the input

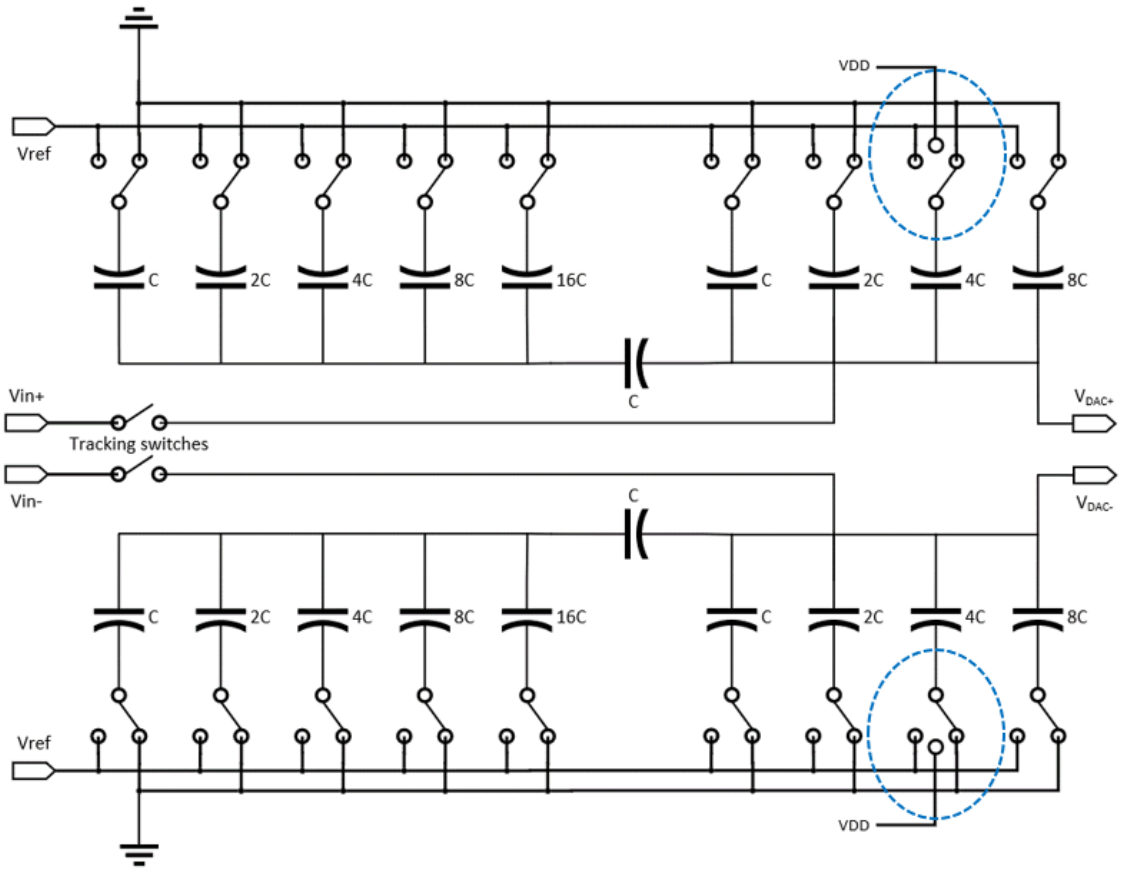

Figure 7.30: Common mode lowering switch.

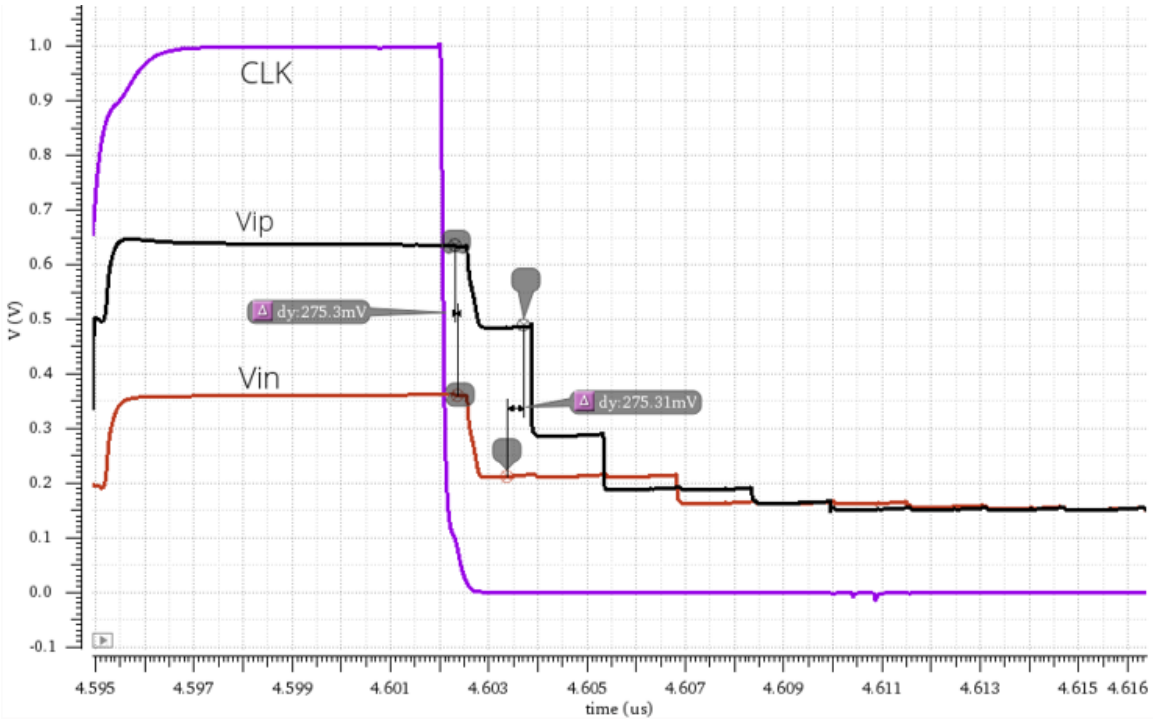

Figure 7.31: Common mode lowering waveforms.

sampled signals by:

$$\Delta V_{cm} = -\frac{VDD - V_{ref}}{4} \tag{7.50}$$

Since that this switch is now used for common mode lowering, this means that it cannot be simultaneously used for offset cancellation. This limits the range of the offset cancellation to the first seven bits of the DAC which corresponds to a ± 128 LSB offset cancellation range. This range is still more than enough as that the actual offset due mismatch never reaches anywhere near these values. Figure 7.31 shows the common mode lowering in action.

7.5 Track and Hold Design

7.5.1 Definition

A Track and hold circuit that samples (tracks) the voltage of a continuously varying analog signal and holds its value at a constant level for a specified minimum period of time. They are used in analog-to-digital converters to eliminate variations in input signal that can corrupt the conversion process. A typical track and hold circuit stores electric charge in a capacitor and contains at least one switching device such as a FET (field effect transistor) switch. To sample the input signal the switch connects the capacitor to the input. In hold mode the switch disconnects the capacitor from the input. The capacitor is invariably discharged by its own leakage currents and useful load currents, which makes the circuit inherently volatile, but the loss of voltage (voltage drop) within a specified hold time remains within an acceptable error margin. In SAR ADCs, the input is compared to a voltage generated internally from a digital-to-analog converter (DAC). The circuit tries a series of values and stops converting once the voltages are equal, within some defined error margin. If the input value were permitted to change during this comparison process, the resulting conversion would be inaccurate and possibly unrelated to the true input value. In addition, track and hold circuits are often used when multiple samples are needed to be measured at the same time. Each value is tracked and held, using a common time-interleaved clock. This approach is called time interleaved ADCs.

7.5.2 Metrics and Nonidealities

The track and hold circuit is a source of noise and nonlinearity that directly affects the ADC resolution, and it can also introduce gain and offset errors. These effects should be considered in the design process. The track and hold generate two main types of noise:

A- Thermal noise:

The track and hold switch is the main source of the sampling thermal noise but the integrated thermal noise is independent on the switch itself. As it is considered $\frac{KT}{C}$ noise, it only depends on the hold capacitor (The input sampling capacitance of the capacitive DAC) which was designed before to be nominally around 70dB (11.33 ENOB), so its value is predetermined from the DAC design.

B- Flicker noise:

Part of the sampling noise is the switch flicker noise that should be taken into consideration. It adds to the thermal noise degrading the sampling noise, hence the resolution. The designer should size the MOS switch in the circuit sufficiently large to keep the sampling noise dominated by the predetermined thermal noise.

The nonlinearity in the track and hold switch can be due to:

A- Insufficient acquisition time:

For an N-bit ADC the track and hold block should settle with a voltage error lower than V_{LSB} and this could be satisfied by the following equation:

$$t_{acq} = 0.69 N R_{on} C_{Hold} \tag{7.51}$$

$$R_{on} < \frac{t_{acq}}{0.69 N C_{Hold}} \tag{7.52}$$

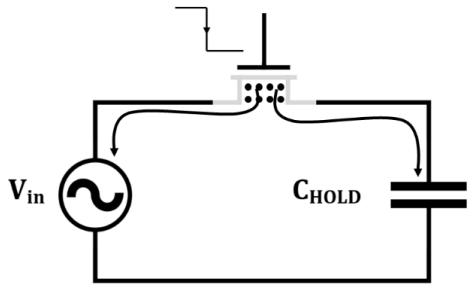

Figure 7.32: Charge injection in MOS switch.

B- Variable tracking time due to the nonlinear on resistance of the switch: If R_{on} of the switch is input dependant that distorts the passing signal one way to solve this is sizing the switch large enough to lower the R_{on} until its variation has negligible effect on the linearity of the ADC. Another way is to fix R_{on} is using bootstrapping techniques, that will be introduced later, to improve the switch linearity.

C- Charge Injection:

When the sampling clock abruptly turns the switch off (fast turn off), the hold capacitor is seen as low impedance path and the trapped charges in the switch adds to the hold capacitor stored charges introducing a voltage step on it. Figure 7.32 shows this phenomenon. These trapped charges depend on V_{th} by the equation:

$$Q = WLC_{ox}(V_{DD} - V_{in} - V_{Tn}) \tag{7.53}$$

The threshold voltage is a nonlinear function of the input so the switch area should be designed small enough to achieve good linearity. The differential topologies enhance this much.

D- Hold mode droop:

When the switch is off that does not mean there is a perfect open circuit between the input and the output. MOSFET has high off resistance that can be considered open circuit but sometimes at large MOSFET widths and small lengths the leakage of the input to the output becomes crucial. This should be taken into consideration that the stored value will not remain the same during the hold phase it will change according to the equation:

$$V_{Hold}(t) = V_{Hold_{initial}} e^{-\frac{t}{R_{off} C_{Hold}}} + V_i \left(1 - e^{-\frac{t}{R_{off} C_{Hold}}}\right) \tag{7.54}$$

This equation shows that each comparator comparison will sense different attenuation, and this causes nonlinearity. In addition to the attenuation, time dependant offset is present due to the leakage. The designer should be careful to keep the leakage acceptable for better linearity especially in the leaky submicron MOSFETs.

E- Hold mode feedthrough:

Due to the MOSFET parasitic capacitance C_{DS}, the input signal can feedthrough to the hold capacitor by the capacitive divider if the transistor area is large enough. The feedthrough can be calculated using the equation:

$$\Delta V_{Hold} = V_{in} \frac{C_{DS}}{C_{DS} + C_{Hold}} \tag{7.55}$$

The hold capacitance is changing in the hold mode due to DAC switching, so the feedthrough increases at the LSB comparison because the C_{Hold} is at its minimum. This is crucial for low unit capacitor DACs causing nonlinearity. The designer should take the C_{DS} into consideration to preserve good linearity.

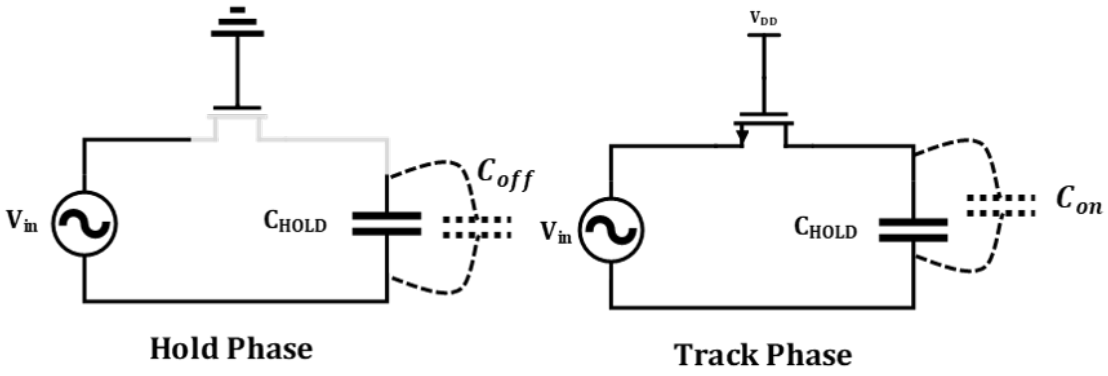

Figure 7.33: On/Off capacitance switching in MOS switch.

The gain and offset errors in the track and hold switch can be due to:

A- Switch parasitic on to off capacitance switching:

As shown in figure 7.33, the switch practically loads the output node by an on capacitance C_{on} in the track phase. When the switch is turned off, the switch abruptly loads the output node by an off capacitance C_{off}. This abrupt change in the capacitance introduces gain error that can be seen by applying the conservation of charges:

$$V_{Hold} = \frac{V_{in}\left(C_{Hold} + C_{on}\right)}{C_{Hold} + C_{off}} - \frac{V_{REF}\left(C_{on} - C_{off}\right)}{C_{Hold} + C_{off}} \tag{7.56}$$

The usage of differential topology cancels the offset but the gain error still present and its value:

$$Gain\ Error = \frac{C_{on} - C_{off}}{C_{Hold} + C_{off}} \tag{7.57}$$

It's seen that this gain error can be eliminated by making the output node capacitance in the track phase is the same as it is in the hold phase $\frac{C_{on}}{C_{off}} = 1$, or it can be reduced by sizing the switch MOSFET as small as possible to minimize its capacitances.

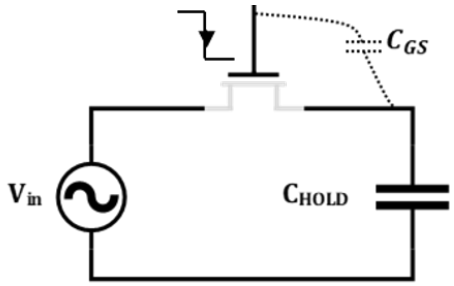

Figure 7.34: Clock feedthrough in MOS switch.

B- Switch output capacitance loading the capacitive DAC:

In the capacitive DAC design, it was discussed that any loading parasitic capacitance on the capacitor bank while switching introduces gain error. The track and hold loads the capacitive DAC while switching by its off capacitance hence the gain error can be calculated as discussed before by the equation:

$$Gain\ Error = \frac{C_P}{C_{Hold}+C_P} \tag{7.58}$$

where C_{off} is included in C_P with other parasitic capacitances loading the capacitive DAC.

C- Clock feedthrough:

The fast turnoff of the switch is done by a step on the gate of the MOSFET switch $\Delta V_G = -V_{DD}$ if the parasitic capacitor between the output and the transistor gate is sufficiently large the step will feedthrough to make a voltage step on the hold capacitor which value is given by:

$$\Delta V_{Hold} = \Delta V_G \frac{C_{GS}}{C_{GS}+C_{Hold}} \tag{7.59}$$

It is shown from the equation that this effect causes offset error that will be eliminated if differential topology is used.

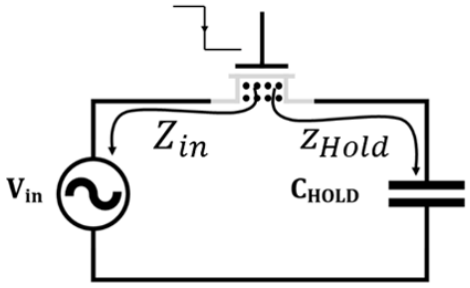

Figure 7.35: Charge Injection in MOS switch.

D- Charge injection:

Due to fast turnoff, charge injection happens. The equation of the trapped charges is given by the equation:

$$Q = WLC_{ox}(V_{DD} - V_{in} - V_{Tn}) \tag{7.60}$$

In addition to nonlinearity discussed before, it is shown from the equation that the charge injection causes gain and offset errors that are given by the equations:

$$Gain\ Error = \frac{-\gamma WL\ C_{ox}}{C_{Hold}} \tag{7.61}$$

$$Offset\ Error = \frac{\gamma WL\ C_{ox}V_{DD}}{C_{Hold}} \tag{7.62}$$

where:

$$\gamma = \frac{Z_{in}}{Z_{Hold} + Z_{in}}$$

The switch should be sized to be small to reduce the gain and offset errors. The differential topologies eliminate the offset error.

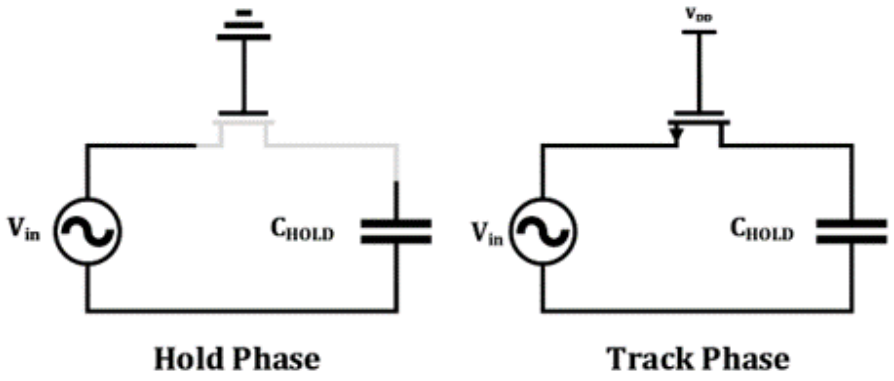

Figure 7.36: NMOS switch.

7.5.3 Switch topologies

MOSFETs are good switches as they have high off-on resistance ratio. Thanks to this, they are widely used in digital circuits. MOSFETs as analog switches are not as good as they're as digital switches because of their variable resistance in the linear region which distorts the passing analog signal through their resistance, and this is crucial in the design of track and hold circuit for an ADC as it causes degradation of the ADC resolution.

A- NMOS as an analog switch:

NMOS is an excellent switch when the input signal voltage is low and close to GND. The closer the input signal is to GND, the lower the resistance of the NMOS it passes through. When the input signal voltage increases, the NMOS on resistance increases until the MOSFET turns off and the NMOS cannot pass the input signal. NMOS cannot pass signals higher than $|V_{DD} - V_{Tn}|$. This can be seen through the square law model in the following equations:

$$r_{ds|_{linear}} \approx \frac{1}{\mu_n C_{ox} \frac{W_N}{L_N} (V_{GS} - V_{thn})} \approx \frac{1}{\mu_n C_{ox} \frac{W_N}{L_N} (V_{DD} - V_{in} - V_{thn})} \tag{7.63}$$

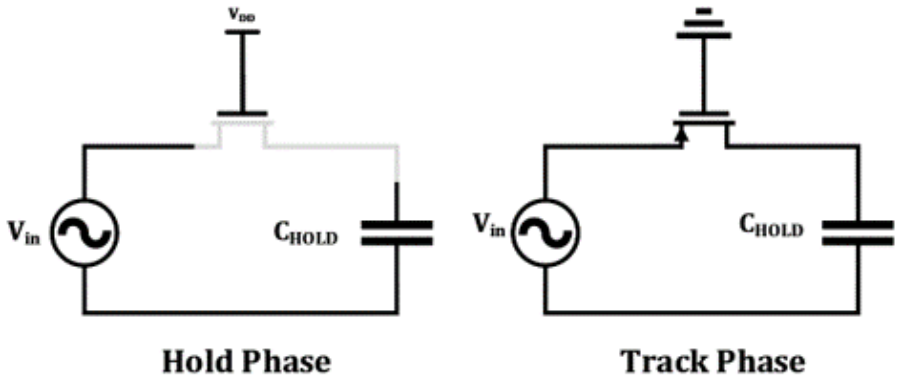

Figure 7.37: PMOS switch.

Conclusions:

- NMOS switch has an input dependant on resistance which causes nonlinearity.
- NMOS can be used only for analog signals that its voltage varies near ground.

B- PMOS as an analog switch:

Unlike NMOS, PMOS is the opposite. The more near the input signal is to the supply, the lower the resistance of the PMOS it passes through. When the input signal voltage approaches GND, the PMOS on resistance increases until the MOSFET turns off at $V_{in} = |V_{Tp}|$ and the PMOS cannot pass the input signal. PMOS cannot pass signals lower than $|V_{Tp}|$. This can be seen through the square law model in the following equations:

$$r_{ds|_{linear}} \approx \frac{1}{\mu_p C_{ox} \frac{W_P}{L_P} \left(V_{SG} - |V_{thp}|\right)} \approx \frac{1}{\mu_p C_{ox} \frac{W_P}{L_P} \left(V_{in} - |V_{thp}|\right)} \tag{7.64}$$

Conclusions:

- PMOS switch has an input dependant on resistance which causes

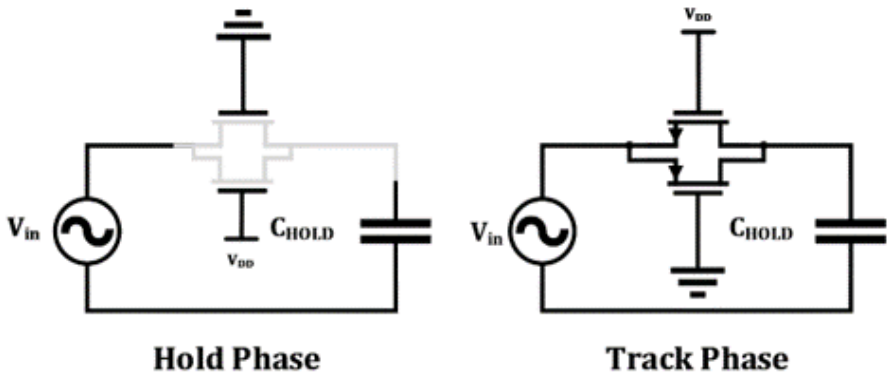

Figure 7.38: Transmission Gate switch.

non-linearity.

- PMOS can be used only for analog signals that its voltage varies near the supply voltage.

C- Transmission Gate as an analog switch:

A transmission gate is implemented by connecting NMOS analog switch and PMOS analog switch in parallel. This maximizes the input range the switch can pass to be rail to rail as NMOS works for the low voltage range and PMOS works for the high voltage range. Generally, The input signal passes through a resistance that is a parallel combination of NMOS and PMOS switches resistance. This effect is shown in figure 7.39. Conclusions:

- Transmission gate still has an input dependant on resistance which causes non-linearity.
- Transmission gate can be used as a switch for analog signals varies in the mid voltage range, or generally, anywhere from rail to rail.

D- Bootstrapped analog switch:

NMOS has lower resistance than PMOS, so it can make a better switch

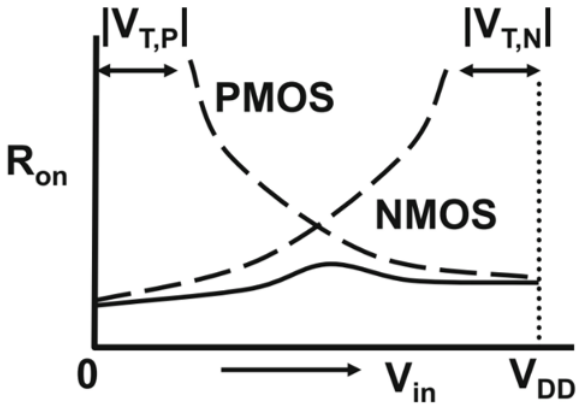

Figure 7.39: TG vs. PMOS vs. NMOS Ron [1].

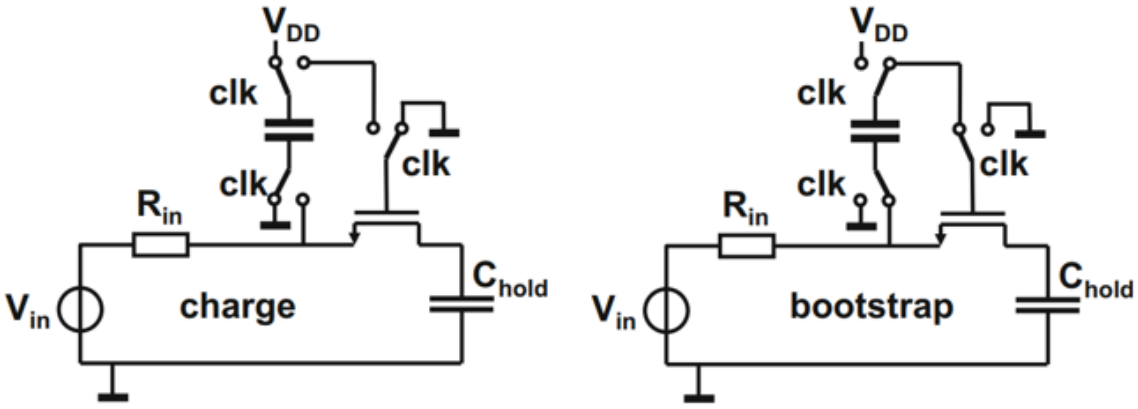

Figure 7.40: Bootstrapped switch [1].

than PMOS in lower sizes. The main problem of using an NMOS as an analog switch was discussed before that it has an input dependant on resistance and it cannot pass high voltage range. One solution to these two problems is maintaining a constant V_{GS} for the NMOS transistor. This can be done by charging a capacitor to the supply voltage in a precharge phase. Then connecting it between the gate and source terminals of the NMOS. Figure 7.40 shows the basic concept of bootstrapping. Fixing the NMOS V_{GS} to VDD maintaining a low constant on-resistance while passing the input signal and maintaining a rail-to-rail operation. This can be seen through the square law model

in the following equation:

$$r_{ds|_{linear}} \approx \frac{1}{\mu_n C_{ox} \frac{W_N}{L_N} (V_{GS} - V_{thn})} \approx \frac{1}{\mu_n C_{ox} \frac{W_N}{L_N} (V_{DD} - V_{thn})} \approx const \qquad (7.65)$$

Conclusions:

- Bootstrapped switch has a rail-to-rail operation region.
- Bootstrapped switch has excellent linearity thanks to its constant input independent on-resistance.
- Bootstrapped switch can have low resistances in very low NMOS sizes which means low parasitic capacitance on the output node.

7.5.4 Realization of specifications

As discussed before, the signal to thermal noise ratio is predetermined by the hold capacitance it is designed to be nominally at $68\ dB$. To let the track and hold thermal noise dominate, it is required to design a switch with THD less than $-80\ dB$ which is equivalent to $(13\ ENOB)$. It is also required to design the switch with the lowest gain error, offset error, and integrated flicker noise as possible.

To design the switch, the testbench in figure 7.41 is used to measure ENOB, gain error and offset for different design points.
The two chosen candidates to realize the specification was the transmission gate switch and the bootstrapped switch and ideally the bootstrapping capacitor was modeled to be ideal fixed voltage source as shown in figure 7.42.
The simulation parameters are given in table 7.6:
The gain error is calculated from the 1st harmonic in the spectrum by the

Table 7.5: Track and Hold block specifications

Specifications	**Required**		
ENOB (no transient noise)	$> 13bits$		
Gain Error	As low as possible		
Offset Error			
Flicker noise			
Sampling Clock Frequency	32MHz		
$\mathbf{T_{on}}$	7ns		
VDD	0.95V	1V	1.05V
Temperature	$-40°$	$27°$	$125°$
Common Mode	$\frac{V_{DD}}{2}$		
Differential Signal Amplitude	$400mV$		
$\mathbf{C_{Hold}}$	$480fF$		

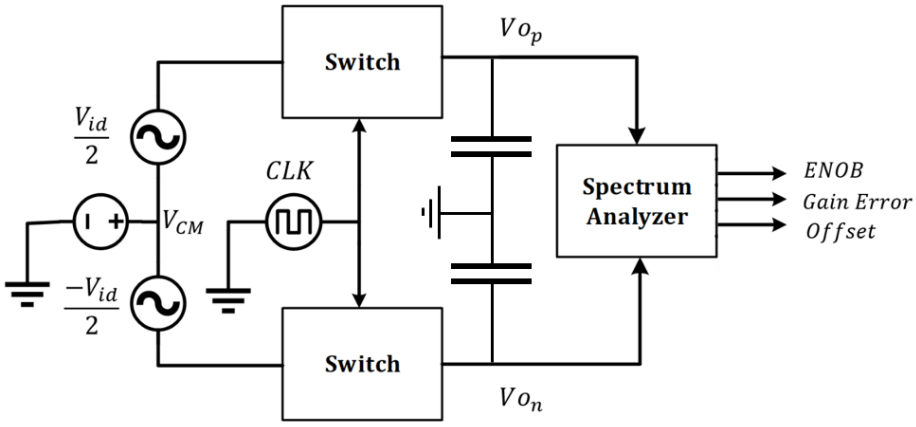

Figure 7.41: Testbench Used.

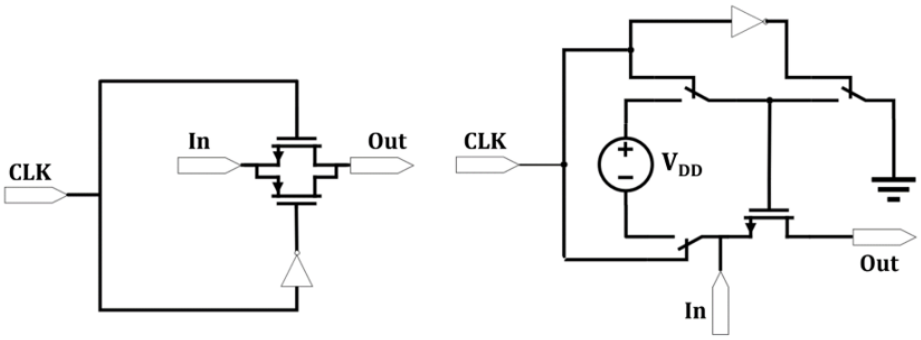

Figure 7.42: Transmission gate vs. bootstrapped switch.

Table 7.6: Track and Hold simulation parameters

Simulation Parameters	
Simulation	Transient (noiseless)
Simulation time	$\frac{5.5}{F_{in}}$
$\mathbf{N_{FFT}}$	2^8
$\mathbf{N_{CYC}}$	5
$\mathbf{F_{CLK_s}}$	32MHz
$\mathbf{F_{in}}$	$\frac{N_{CYC}}{N_{FFT}} F_S$
$\mathbf{C_{Hold}}$	$480fF$
FFT samples	$\frac{0.5}{Fin} : \frac{5.5}{F_{in}}$
$\mathbf{V_{CM}}$	$\frac{VDD}{2}$
$\mathbf{V_{id}}$	$400mV$
$\mathbf{T_{on}}$	$5ns$
Multiplier	2:2:100

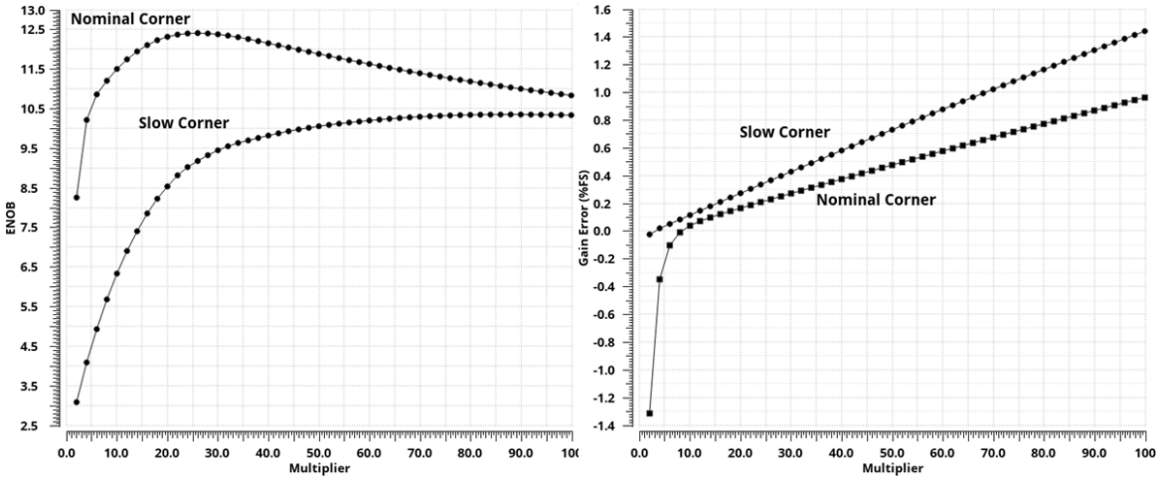

Figure 7.43: Transmission Gate linearity and gain error vs. multiplier.

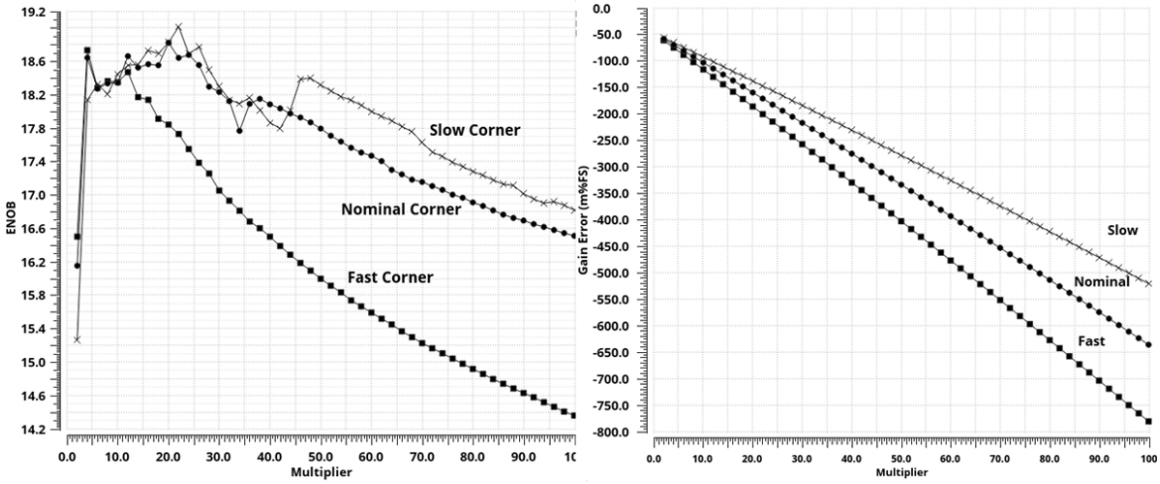

Figure 7.44: Bootstrapped switch linearity and gain error vs. multiplier.

following equation:

$$Gain\ Error = \frac{V_{1^{st}\ harmonic} - 400m}{400m} \tag{7.66}$$

The simulation results shown in figures 7.43, and 7.44 shows as expected that the bootstrapped switch can get much higher linearity than the transmission gate in lower areas. The transmission gate does not reach the 13 ENOB limit required even in large areas. Unlike the transmission gate

switch, the bootstrapped switch suffers from a negative gain error, but this is more acceptable than the positive gain error. Positive gain errors reduce the dynamic range of the ADC when the negative gain error could be solved by input preamplification before sampling (i.e. using the AGC if the ADC is used in a transceiver chain). Another good point about the negative gain that it can compensate the positive gain error caused by the capacitive DAC loading parasitic capacitances (i.e. comparator gate capacitances, switch off capacitances and layout wiring). The bootstrapped switch shows a very good linearity in low multipliers, and then it decreases due to mainly charge injection problems and the hold mode feedthrough due to the increase of C_{DS} for large multipliers. It is shown that the bootstrapping is better to get the required linearity with small area and gain error. In the next subsection, the chosen bootstrapped switch will be discussed in detail.

7.5.5 The implemented bootstrapped switch topology

The shown schematic in figure 7.45 is inspired by the work in [2]. The topology works as a bootstrapped switch that was discussed before. The MOSFET M_N1 is the core NMOS switch. The capacitor C_{BS} is the bootstrapping capacitor. M_P1 and M_N3 provides paths to V_{DD} and GND respectively for the bootstrapping capacitor in the hold mode. M_P3 works as a switch to connect the bootstrapping capacitor to the core switch gate in the track mode. M_N2 isolates the input terminal from the ground terminal in the hold mode to avoid short circuiting. M_N5 is bootstrapped in the track mode helping M_N4 to provide low impedance path between M_P3 gate and C_{BS} negative terminal to protect M_P3 at the transition from V_{GS} higher than the supply. M_N4 and M_P2 defines the gate of M_P3 to work properly in the track and hold modes. M_N6 is used as a cascode for reliability protecting M_N7 from V_{DS} higher than

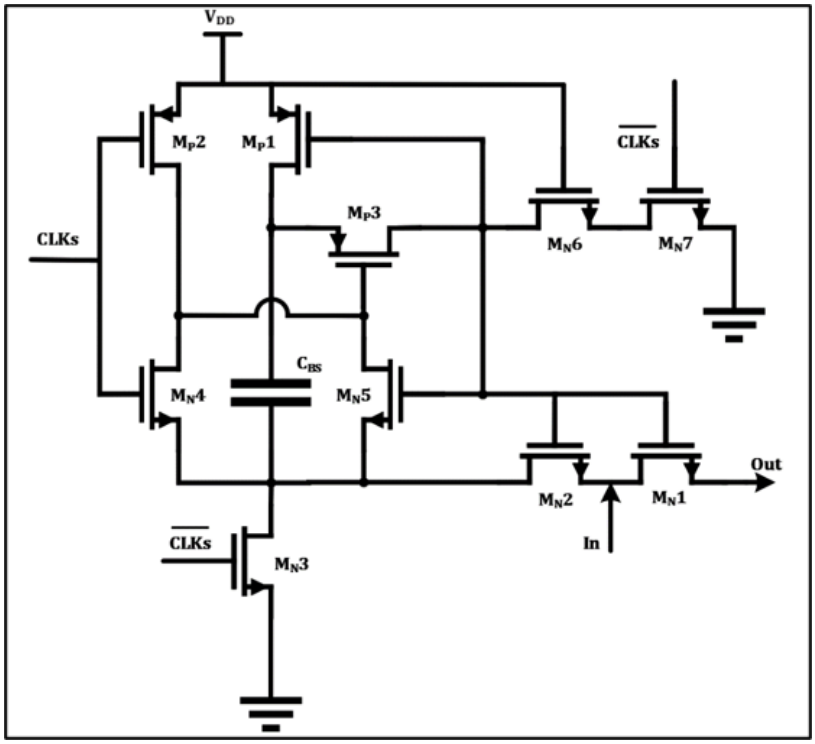

Figure 7.45: The chosen architecture.

the supply voltage. M_P1 and M_P3 bodies should be connected to C_{BS} positive terminal to avoid body terminal leakage.

7.5.5.1 Operation

A- Precharge/Hold Phase:

As shown in figure 7.46 (A), When the sampling clock (CLKs) is low, the bootstrapping capacitor C_{BS} is connected to V_{DD} and GND through M_P1 and M_N3 respectively and it is charged to the supply voltage. The core switch M_N1 is maintained off by M_N7 connecting its gate to GND through M_N6 holding the last sampled value stored on the output node capacitance.

B- Tracking Phase:

As shown in figure 7.46 (B), After the sampling clock is high, the

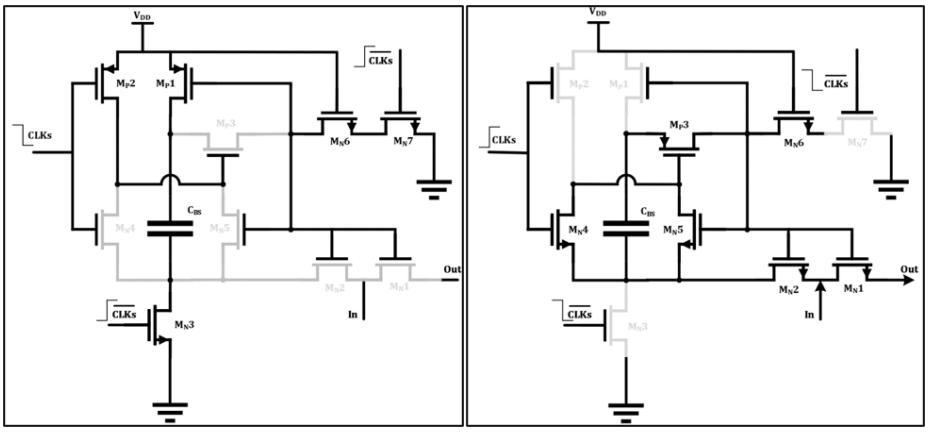

Figure 7.46: (A) Precharge Phase. (B) Tracking phase.

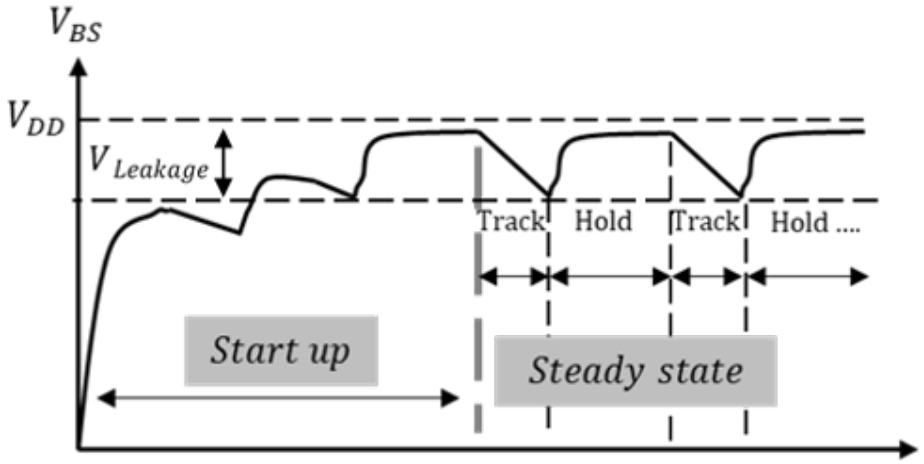

Figure 7.47: Bootstrapped switch transient.

bootstrapping capacitor C_{BS} is connected to set the gate source voltage of M_N1 to V_{DD} by M_P2 and M_N2 maintaining low constant on resistance and thus enhances the core switch linearity.

7.5.5.2 Design equations and guidelines

A- Hold phase power and leakage:

One of the important parameters is the hold phase power charging the capacitor. As shown in figure 7.47, When the circuit starts up and settles to the steady state the hold capacitor should be charged to the

supply voltage. Ideally, the capacitor should hold this value forever, but due to the tracking phase leakage, the capacitor discharges through the equivalent off resistance seen by the capacitor in the tracking phase. In the next hold phase, the capacitor charges again to compensate the lost charges and this consumes average power that could be calculated in steady state by the equation:

$$Hold\ phase\ average\ power = V_{DD}V_{Leakage}C_{BS}\left(1 - e^{-\frac{-T_{hold}}{R_{charge}C_{BS}}}\right) \tag{7.67}$$

T_{hold} is the time window of the hold phase. R_{charge} is the resistance seen by the capacitor while charging.

$$R_{charge} = R_{M_P1,on} + R_{M_N3,on} \tag{7.68}$$

$V_{leakage}$ is the amount of voltage the capacitor loses at the end of the tracking phase. The equation shows a direct relation between the leakage amount and the hold phase power as the more leakage in the tracking phase, the more power consumed to compensate the lost charges in the hold phase. Figure 7.48 The leakage could be calculated using the following equations:

$$V_{Leakage} = V_{DD}\left[\frac{R_{off_{up},eq}}{R_{M_N7,off}} + \frac{R_{off_{down},eq}}{R_{M_P2,off}}\right] - V_{DD}\left[\frac{R_{off_{up},eq}}{R_{M_N7,off}} + \frac{R_{off_{down},eq}}{R_{M_P2,off}}\right]e^{-\frac{T_{track}}{R_{off,eq}C_{BS}}} \tag{7.69}$$

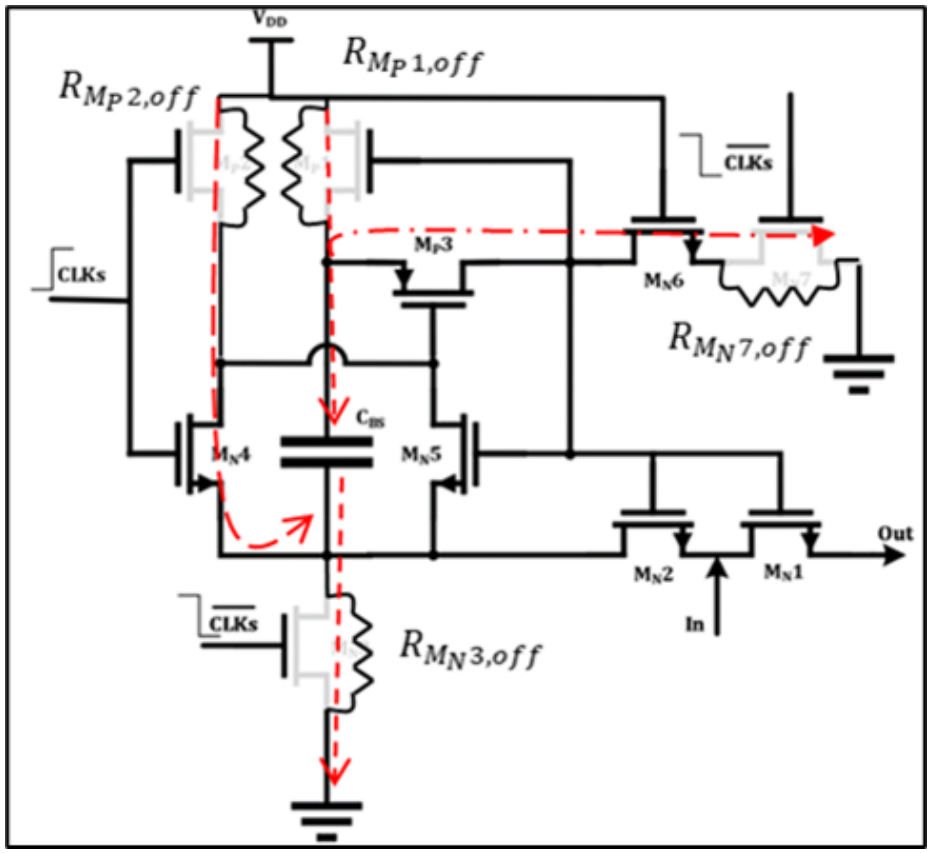

Figure 7.48: Bootstrapping capacitor leakage paths in tracking phase.

$$R_{off_{up},eq} = \frac{R_{M_P1,off} R_{M_N7,off}}{R_{M_P1,off} + R_{M_N7,off}}, \quad R_{off_{down},eq} = \frac{R_{M_P2,off} R_{M_N3,off}}{R_{M_P2,off} + R_{M_N3,off}} \; R_{off,eq} = R_{off_{up},eq} + R_{off_{down},eq} \tag{7.70}$$

The equations show that the leakage is directly proportional to V_{DD} hence the hold phase power is directly proportional to V_{DD}^2 as it is basically a dynamic power. One way to avoid leakage is to make the track phase short but this trades off with accuracy needed while tracking. The practical way to avoid high leakage is to design the circuit for C_{BS} to see highest R_{off},eq possible during tracking. Especially, the transistors M_N7, M_P2, M_P1 and M_N3 should be designed to have the lowest leakage to reduce hold mode power and the degradation of the bootstrapping voltage.

B- Speed and linearity:

The time the capacitor needs to retrieve leakage in steady state is given by:

$$T_{BS,charge} = R_{charge} C_{BS} \ln\left(\frac{V_{leakage}}{V_{DDerror}}\right) \tag{7.71}$$

$V_{DD_{error}}$ is the dynamic error in settling. The hold window should be larger than this retrieval time to ensure highest V_{GS} and constant switch linearity.

The acquisition time needed to the input to track the output with N accuracy is given by:

$$t_{acq} = 0.69 N R_{on} C_{Hold} \tag{7.72}$$

That defines a maximum on resistance for the core switch that is given by:

$$R_{on} < \frac{T_{track}}{(0.69NC_{Hold})} \tag{7.73}$$

C- Switching Errors:

The bootstrapped switch has input dependant clock feedthrough as $\Delta V_G = -(V_{DD} + V_{in})$ at the switching instance. The pedestal step due to the clock feedthrough is given by:

$$V_{pedestal} = \frac{-C_{GS}}{C_{GS} + C_{Hold}} (V_{DD} + V_{in}) \tag{7.74}$$

This introduces a gain error of:

$$\frac{-C_{GS}}{C_{GS} + C_{Hold}} \%FS$$

And Offset error of:

$$\frac{-C_{GS}}{C_{GS} + C_{Hold}} V_{DD}$$

that can be eliminated if differential topology is used.

The bootstrapped has nonlinear charge injection is given by:

$$Q = WLC_{ox} (V_{DD} - V_{th}) \tag{7.75}$$

V_{th} is a nonlinear function of V_{in} this causes linearity degradation in large switch areas. There are many advanced solutions for this problem, but in this design this issue is solved simply by keeping the core switch small as possible.

7.5.6 Results and achieved Specs

Using this topology, we succeeded to realize the required specification across PVT corners all combinations of the following corners is simulated:

- $Process: \ ff, \ ss, \ tt, \ sf, \ and \ fs.$

- $Temperature: \ -40, \ 27, \ and \ 125 degree$

- $Voltage: \ 0.95, \ 1, \ and \ 1.05 \ V$

- $Capacitor: \ ss, \ tt, \ and \ ff.$

The results are shown in the following table:

Table 7.7: Track and hold achieved specifications

Realized Specifications				**Units**
Specification	**Minimum**	**Nominal**	**Maximum**	
ENOB (without noise)	13.29	18.25	20.63	bits
Gain Error	<0.001			%LSB
Offset	<0.5			μV
$\mathbf{T_{on}}$	6			ns

7.6 Comparator Design

Comparator is the core and the actual quantizer in any ADC. It converts analog signals to digital bits. A comparator is considered a 1-bit ADC. It directly can affect the entire ADC concerning the gain error, offset and resolution. It can also produce some sort of hysteresis and metastability when designed incorrectly.

There are many commonly known comparator architectures. These can usually be divided into one of these architectures:

- Multiple cascaded high gain stage amplifier
- Static preamplifier and dynamic latch
- Dynamic preamplifier with dynamic latch

The comparator in this work consists of a dynamic preamplifier with extra gain stages along with a dynamic latch to regenerate the input differential signal and store it. The design procedure is presented as follows.

7.6.1 Dynamic Preamplifier

The topology in figure 7.49 operates as dynamic preamplifier. M_P4 operates as a current source bias that its high output impedance provides high CMRR that solves the problem of the varying common mode of the monotonic switching scheme discussed before. M_P3 operates as a switch to disconnect the current source bias in the reset phase. M_P1 and M_P2 operate as the input pair that injects the differential perturbation on the common mode current charging the shown capacitors. The capacitors determine the value of $\frac{KT}{C}$ thermal noise. M_N1 and M_N2 operate as reset switches to

discharge the capacitors in the reset phase to eliminate the memory effect. M_N3 and M_N4 operate as switches to disconnect the capacitor after the comparison decision is made in order to save power.

A- Reset phase:

To avoid hysteresis, the memory effect should be eliminated so capacitors should be discharged totally so a sufficient duration of reset phase is needed. The minimum duration of the reset phase is determined by knowing the time required to discharge the capacitors. The capacitors need infinite time to be fully discharged. The worst-case time required for the capacitor voltage to reach infinitesimal voltage ε is given by:

$$(R_{M_N3,on} + R_{M_N1,on})\, C_{PRE} \ln\left(\frac{V_{DD} - VDSAT_{M_P4}}{\varepsilon}\right) = t \tag{7.76}$$

ε should be much less than V_{LSB} in order to prevent the effect of hysteresis from affecting ADC resolution using the comparator.

B- Amplification phase:

In the amplification phase, the comparator clock (CLK_c) is low. M_P3 is on to connect the current source M_P4 to the differential pair $M_P1,2$. The differential pair start from saturation as their drains start from GND, so it generates a differential current depending on $V_{id} = V_{IP} - V_{IN}$ super imposed on the common mode current $\frac{I_0}{2}$ that gets integrated by the C_{PRE} capacitors generating a differential output voltage that could be calculated by:

$$V_{od} = \frac{I_0 V_{id} t}{C_{pre} V_{ov}} \sqrt{1 - \left(\frac{V_{id}}{2V_{ov}}\right)^2} \approx \frac{I_0 V_{id} t}{C_{pre} V_{ov}} \tag{7.77}$$

The output common mode voltage is given by:

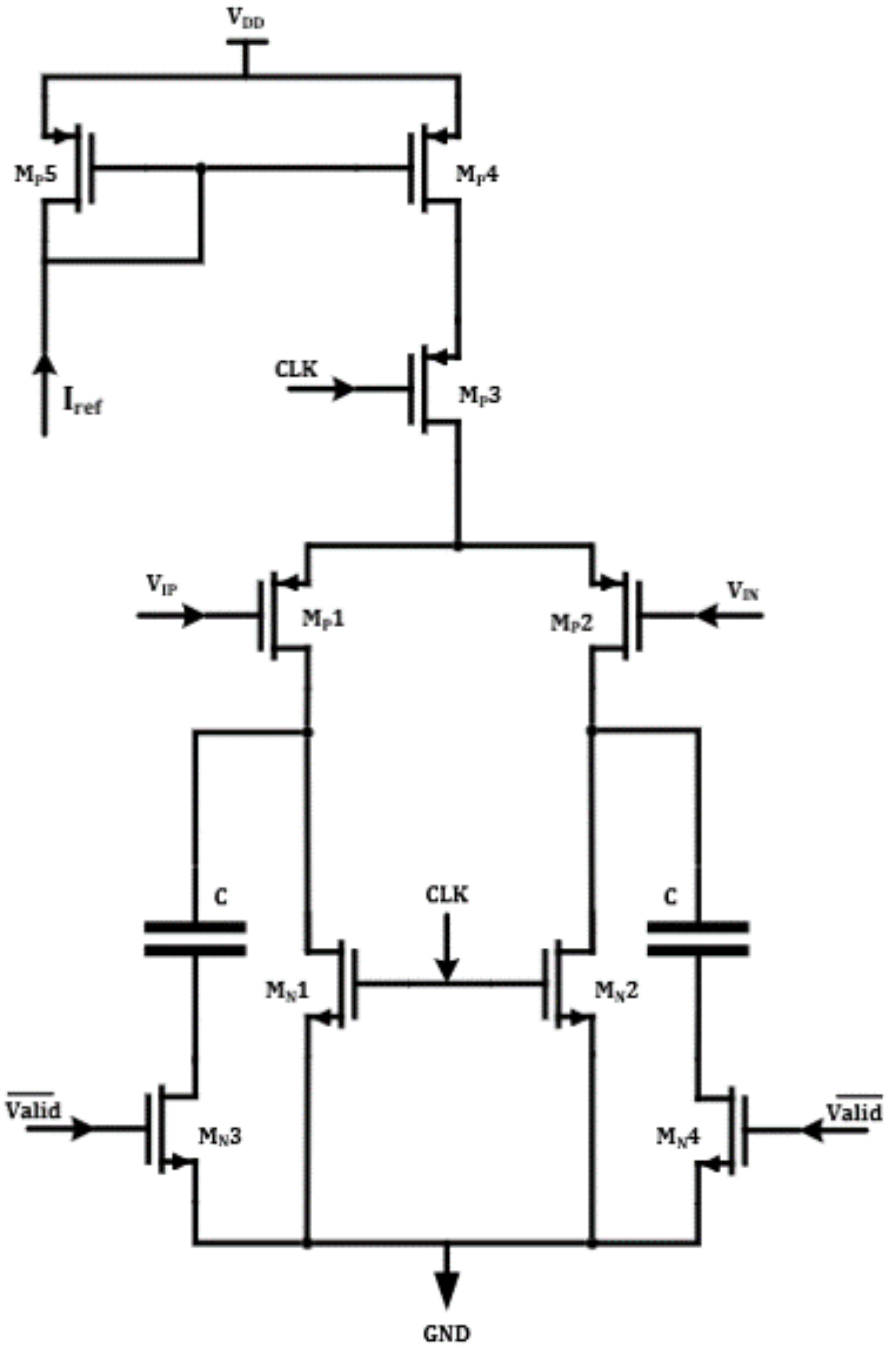

Figure 7.49: Proposed dynamic preamplifier.

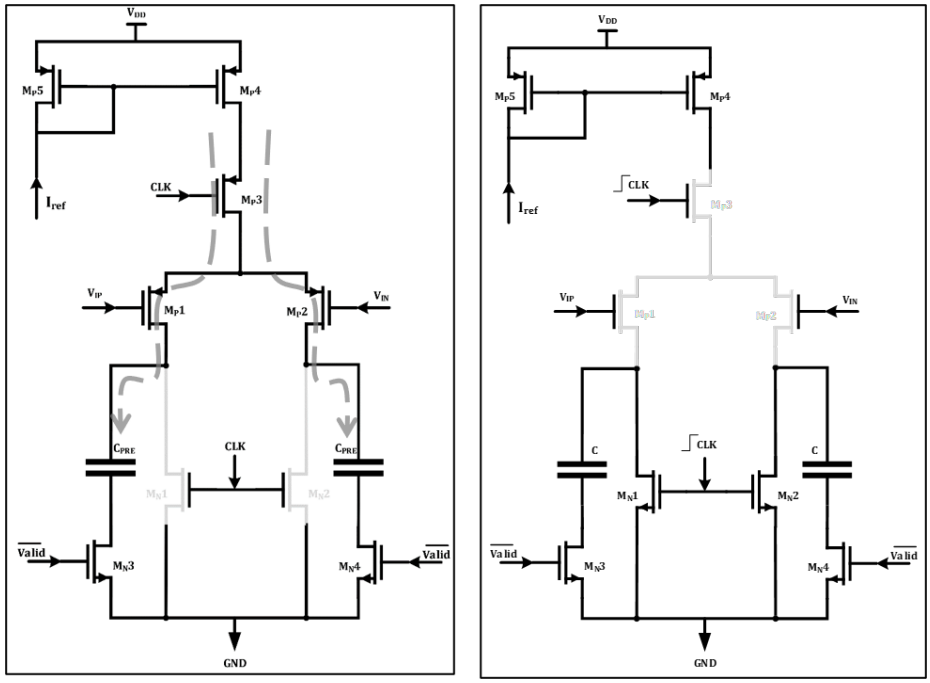

Figure 7.50: (A) Amplification phase. (B) Reset Phase.

$$V_{o,cm} = \frac{I_0}{2C_{pre}}t \tag{7.78}$$

These equations are valid while the differential pair are in saturation. The differential output voltage keeps increasing with time until the differential pair reach the edge of the linear region the differential output voltage starts to decrease until it becomes zero when the two capacitors are fully charged.

The following analysis is inspired by the work of [3]:

- Dynamic Gain:

  The dynamic amplifier provides a dynamic gain that increases with time in the saturation region that can could be calculated

using the following equation:

$$A_v(t) = \frac{I_0 t}{C_{pre} V_{ov}} = \frac{2V_{window}}{V_{OV_{1,2}}} \tag{7.79}$$

It is shown that the gain is too low to isolate the dynamic latch.

- Input Dependant Speed:

  The rate at which the amplifier output voltage increases with time is input dependant and could be calculated in the saturation region using:

$$\frac{dV_{od}}{dt}(V_{id}) = \frac{I_0 V_{id}}{C_{PRE} V_{OV}} \tag{7.80}$$

- Common Mode Rejection:

  For the common mode signals, the equivalent common mode $G_{m,CMeff}$ is degenerated by the current source output resistance of the current source to be given by:

$$G_{m,CMeff} = \frac{g_{m1,2}}{1 + 2g_{m1,2} Ro_{M_p 4}} \tag{7.81}$$

  Figure 7.51 shows the transconductance (gm) of the input pair during the conversion process while varying the input common mode. It shows that the gm is constant regardless the CM level which proves that the preamplifier common mode rejection ratio is high which is crucial for the monotonic switching scheme to work.

- Input Referred Offset:

  The main benefit of using the dynamic comparator with a current source is to eliminate the effect of the common mode signal as possible because it generates input dependant offset degrading the linearity of the ADC. This is crucial especially for this design

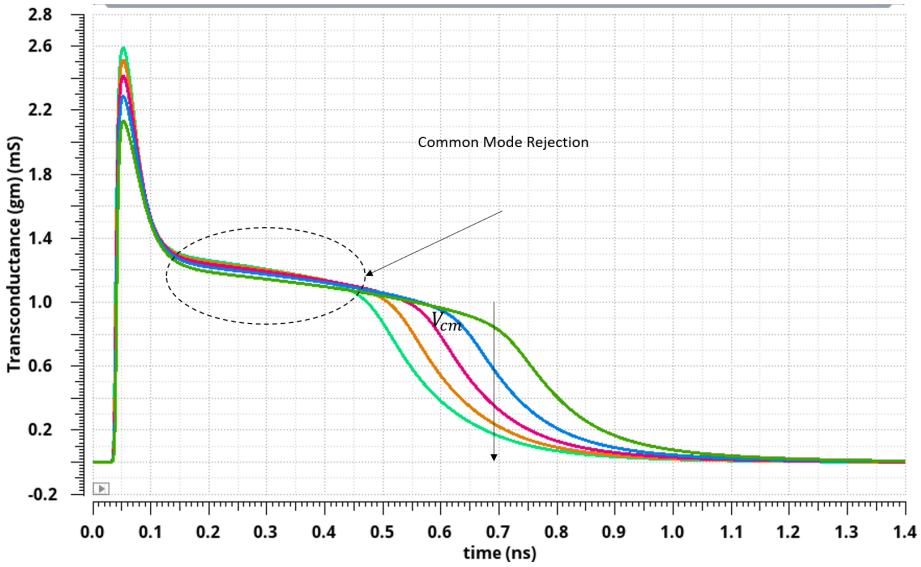

Figure 7.51: Preamplifier common mode rejection.

as the ADC uses monotonic switching (varying common mode).

$$\sigma^2_{V_{offset}} = \sigma^2_{V_{TP}1,2} + \left[\frac{V_{OV_{MP}1,2}}{2\left(1+2g_{mMP}1,2Ro_{MP}4\right)}\right]^2 \left(\frac{\sigma^2_{C_{PRE}}}{C^2_{PRE}} + \frac{\sigma^2_{S_{MP}1,2}}{S^2_{MP}1,2}\right) \tag{7.82}$$

- Input Referred Noise:

  The input referred integrated thermal noise can be calculated using:

$$\sigma^2_{noise} = \frac{2KT}{C_{PRE}} \tag{7.83}$$

7.6.2 CMOS Inverter

The CMOS is commonly used in digital circuits to invert the digital signal. It is considered a very narrow range dynamic amplifier as it amplifies the signal around the output voltage at its transition voltage V_M with a high gain (Inverter Gain $A_{v,inv}$). Inverters are used in this design in cascade to the preamplifier to add extra gain to further isolate the latch offset and noise.

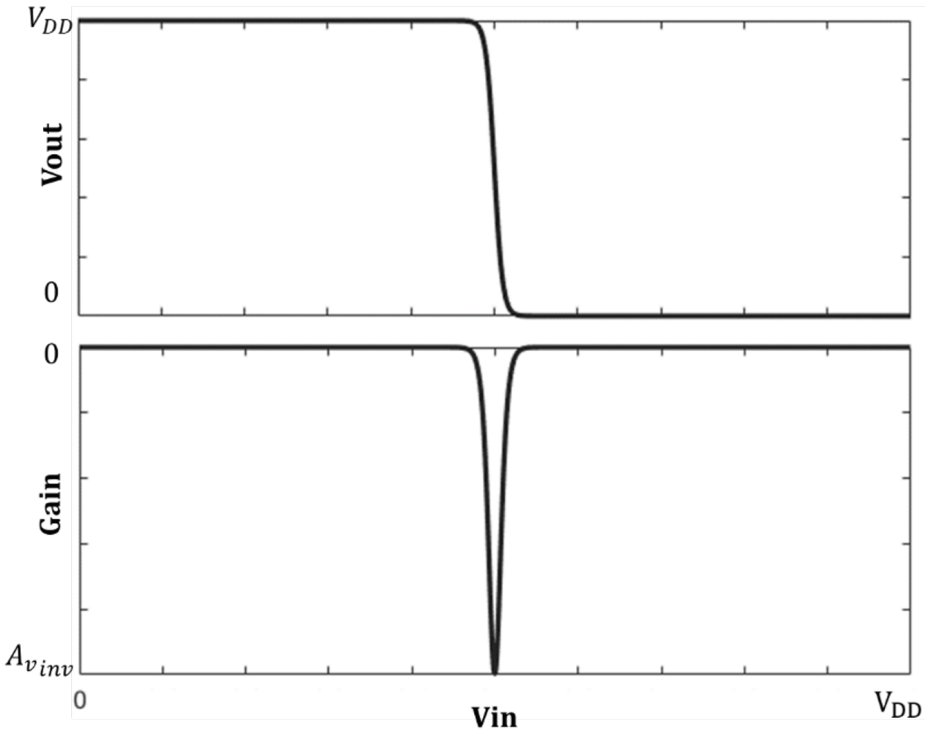

Figure 7.52: Inverter gain with respect to its input voltage.

The inverter gain is the gain the inverter provides when the N and P MOSFETs are both in saturation and this happens in very narrow output voltage region. Figure 7.52 shows this effect. The inverter gain can be calculated using the equation:

$$A_{v,inv} = -g_{m_{inv}}(V_{out} = V_M) * R_{out}(V_{out} = V_M) \tag{7.84}$$

The inverter output noise voltage at V_M mainly depends on the integration of all thermal noise current charging the capacitor since the transition started. It is complex to analyze such process but the most contributor in this integration is the noise at the time the 2 MOSFETs were in SAT that can be easily calculated using:

$$\sigma^2_{noise} \approx \frac{4KT\gamma}{g_{m_{inv}}(V_{out} = V_M)} \tag{7.85}$$

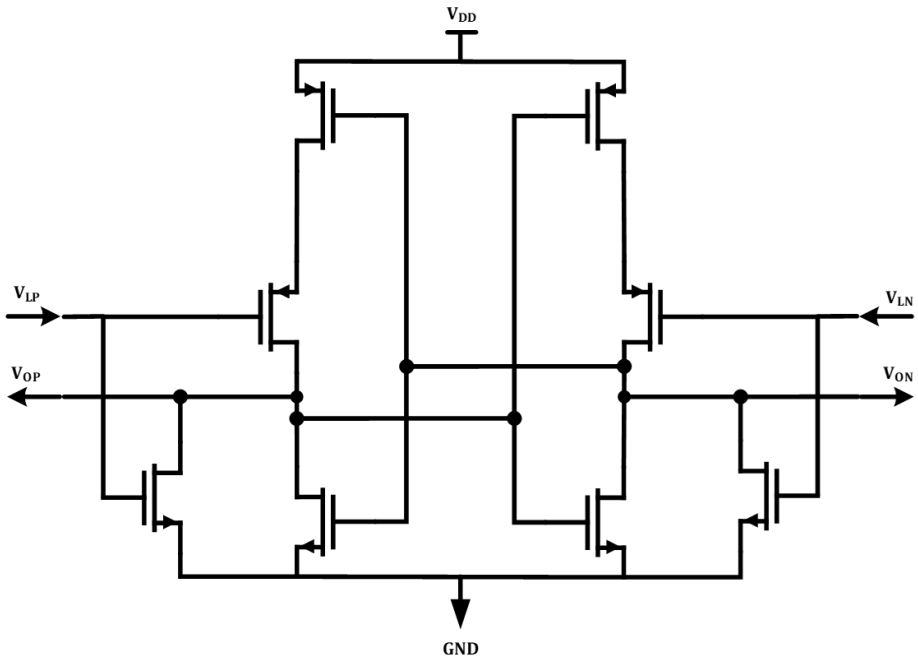

Figure 7.53: Dynamic latch schematic.

This equation neglects triode region noise, so it is not accurate, but it gives a design intuition that increasing the aspect ratio reduces the transition thermal noise.

7.6.3 Dynamic Latch

A dynamic latch is a used to regenerate and store the amplified input. Basically, latches use positive feedback to provide high settling speed, but it also can introduce sources of error such as meta-stability and dynamic offset can be minimized and the other can be isolated by using high gain stages before the latch.

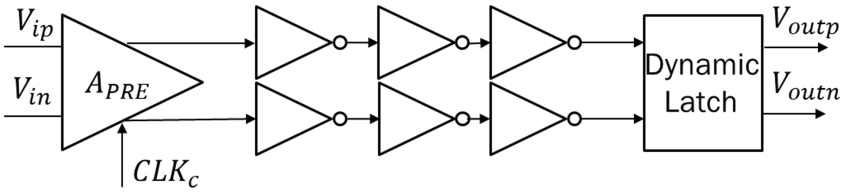

Figure 7.54: proposed comparator structure.

7.6.4 Proposed comparator architecture

The dynamic preamplifier is used to isolate the latch noise and offset. Since that dynamic preamplifiers cannot provide high gain, as shown in figure 7.55, three cascaded inverters were used to further amplify the signal. The preamplifier gain after connecting these cascaded inverters increases by around 70 times as shown in figure 7.56. This is due to that the small differential signal from the dynamic preamp is implicitly converted to two high slew rate signals with a time delay between them. For relatively larger input signals (in the range of tens of LSBs), the time delay between the two outputs is too great eliminating any possibility for the latch to fail. The dynamic latch is then used to regenerate the differential amplified input and store it as a differential digital signal. The latch stores this signal until it is reset again for the next comparison. The operation of the latch is shown on figure 7.57. Another benefit from using the inverter chain is that the dynamic latch delay is minimized to the point that it can be neglected compared to the preamplifier delay.

7.6.5 Simulation results

A testbench was created for the comparator to test its characteristics. The parameters that were tested in the test bench were:

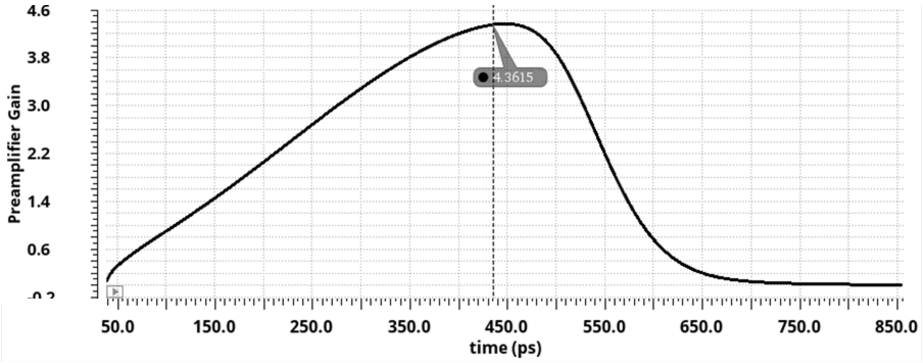

Figure 7.55: Preamplifier gain.

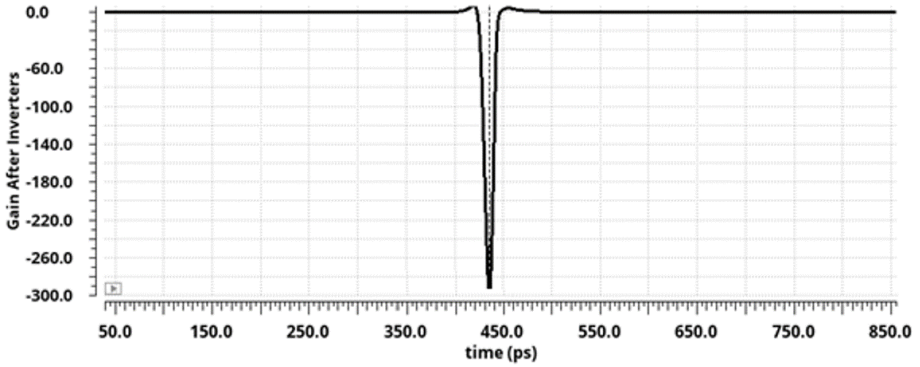

Figure 7.56: Preamplifier gain after connecting the inverters.

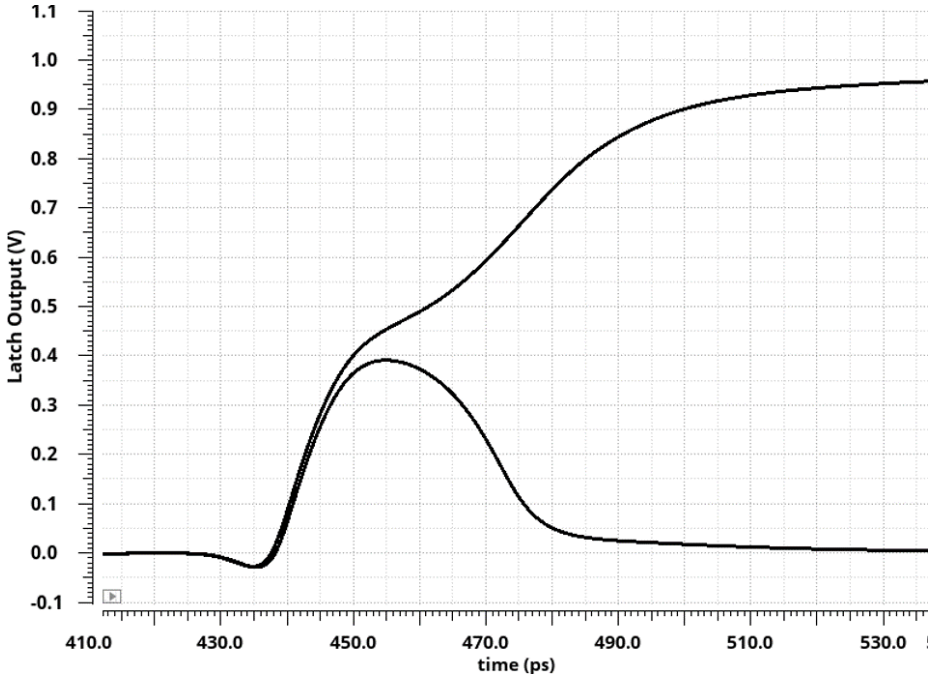

Figure 7.57: Dynamic latch regenerative postive feedback operation.

1. Power draw
2. Delay
3. Input referred noise
4. Power down current
5. Equivalent ENOB
6. SNR
7. Comparison error rate for 1 LSB input
8. AC bandwidth and gain
9. Dynamic offset error

This testbench heavily depended on the works of [3]. The most important parameters when testing a comparator are the speed and input referred noise. These two together specify whether or not this comparator is usable in a certain design. Since that this circuit is time variant, there is no straight forward method to analyze the noise using the conventional simulation methods. The conventional method to estimate this input referred noise is to set a small differential input to the comparator and run a transient noise simulation for a suitably long period. A period long enough to estimate the conversion error rate of the comparator. The standard deviation of the input noise can be derived easily from this value. However, this is a very computationally expensive process and could take a long time to run especially for corner simulations. This makes the design optimization process harder and sometimes not feasible.

The works of [3] eliminate this problem by setting up a method of a highly accurate estimation of output noise from the jitter in the delay of the comparator for a constant input. The periodic AC gain can be also measured from another simulation enabling us to measure the input referred noise to a high degree of confidence.

This method was first verified for our architecture comparing its results with the brute force method. The jitter noise method appeared to perform to more than 90% accuracy which is more than fine given the immense amount of time saved.

The testbench was set to consecutively carry out multiple comparisons at a speed higher than the actual speed that it will operate at when connected to the ADC system. Hence, the power consumption values in this testbench only give hints on whether the comparator is too power hungry or if the power varies too much with corners indicating a potential issue.

The equivalent effective number of bits can be derived from the input referred noise of the comparator. The targeted minimum ENOB across corners was 9.6 Bits.

The delay was measured as the average time between the start of conversion and settling of the latch output with its READY signal. The common mode of the input signal was set as a variable and varied across corners to simulate the effects of monotonic switching common mode decrease with each conversion step.

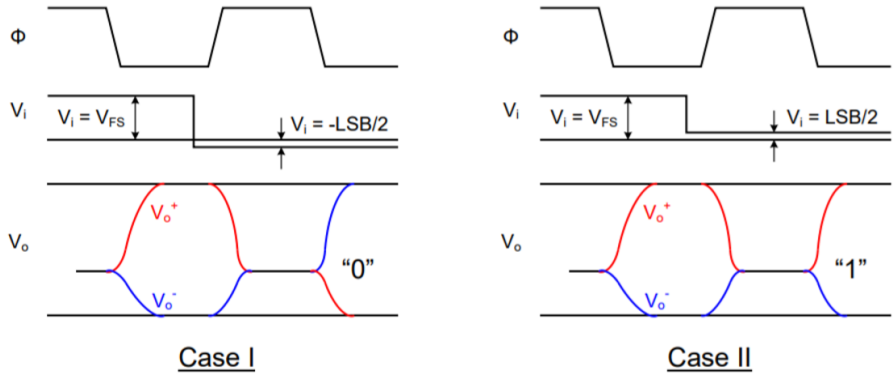

Figure 7.58: Overdrive recovery test

The power down current was also measured to ensure that the comparator works even under the effects of the power down transistors. While also ensuring that the power down current is within the specifications.

Another testbench was created to test the overdrive recovery of the comparator. A small input (0.5 LSB) is applied to the comparator input in a cycle right after a full-scale input is applied. The comparator should be able to resolve to the right output in either case which implies that its memoryless.

Table 7.8 shows the final achieved specifications across all design corners.

Table 7.8: Achieved specification across PVT corners.

Specifications	Required	Achieved			Units
		min	typ.	max	
Delay	<1.2	0.33	0.52	1.14	ns
ENOB (SQNR included)	>9.6	9.696	9.822	9.9	Bits
SNR (SQNR included)	-	60.13	60.89	61.35	dB
Input referred noise	-	127	171	233	uV
Current consumption	-	52	72	113	uA
Power down current	<8	0.05	0.07	5.7	nA
AC gain	-	1.04	1.55	3.7	KV/V
Bandwidth	-	427	1000	1637	MHz

7.7 Synchronization and Digital Delays

The proposed ADC is event-driven (asynchronous), it does not require an external clock to trigger the comparator. This means that numerous precise delays are needed for proper operation. These delays can be implemented in many ways depending on its duration and how accurate it is required to be. All the signals that require a delay in this context are digital control signals.

As discussed before in section 7.3, the sampling time was chosen to be approximately 7ns. However, the input 32 MHz clock signal has a duty cycle of 50% nominally. This means that a special circuit is needed to modulate this input clock signal and change its duty cycle. Figure 7.59 shows a circuit example that can be used for this purpose. The modulated clock signal must have a high time of around 7 ns. This can be achieved by a simple digital circuit that compares the input clock signal with a 7 ns delayed version of it. When it detects that both the clock and its delayed version are high, the output goes low. Thus, achieving the required function. Figure 7.60 shows this circuit in action. In this way, the problem of setting a certain duty cycle is turned into a problem of creating an accurate and

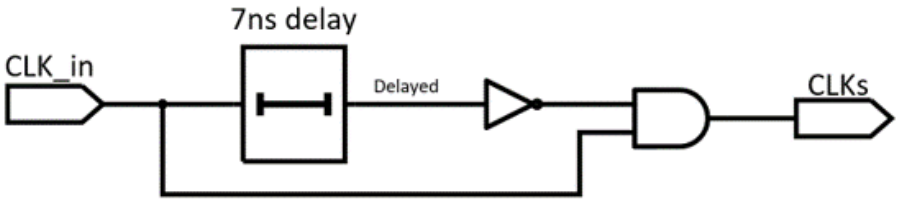

Figure 7.59: Sampling Clock Modulator

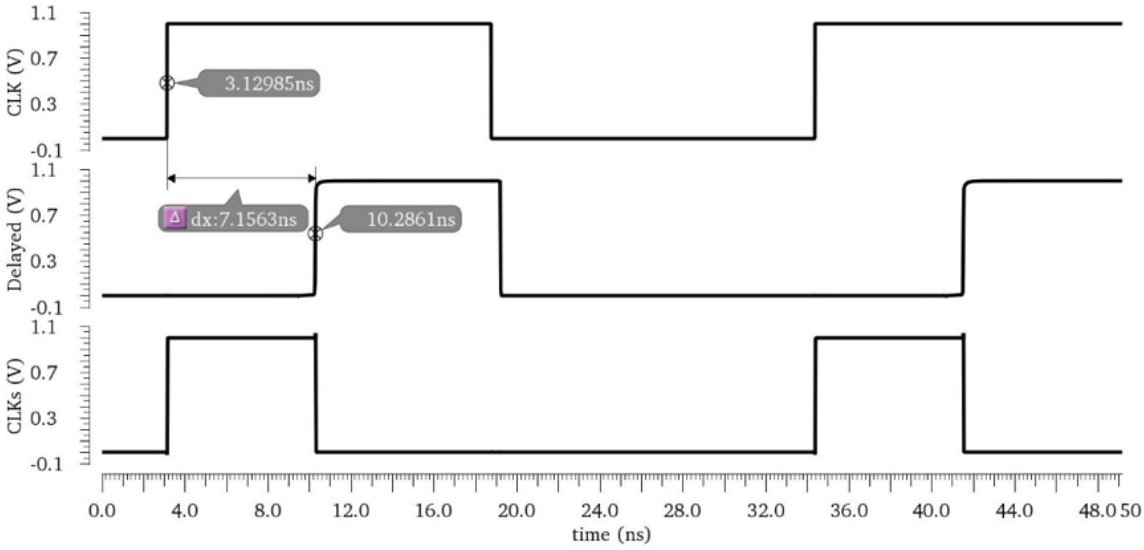

Figure 7.60: Sampling Clock Modulator waveforms

stable delay. This delay circuit should only delay the rising edges of the clock and have negligible delay on the falling edge for proper operation. This delay needs to be highly stable across corners. If not, the ADC may either fail to finish its conversion cycles before the start of the next clock if the delay is too high, or fail to sustain enough time for the tracking phase to accurately track the input signal in case that the delay is too low.

Another important delay element is needed for the proper operation of the ADC conversion steps. When the comparator clock (CLKc) falls, the comparator starts its first conversion. Then, when the conversion is complete, the comparator generates a signal (Valid) indicating that its outputs are

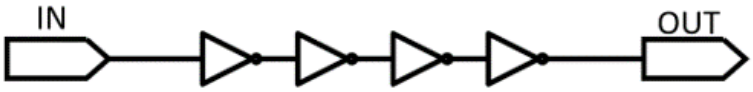

Figure 7.61: Inverter chain

ready to be read. When this happens, the SAR logic changes the capacitor switches' positions accordingly. This causes a disturbance in the Vref signal. The Reference buffer supplying this signal needs some time to recover before the next conversion can take place. This recovery period was chosen to be 1 ns. The Reference buffer must be able to settle with sufficient accuracy in this period. This delay is used to ensure that each successive conversion takes place after at least 1 ns.

7.7.1 Methods of implementing a digital delay

There are several kinds of delay elements. In this thesis work, some of them which consume less power are explored.

7.7.1.1 Inverter Based Delay Line

The Inverter-based delay line is one of the basic well-known delay elements. It is constructed from a chain of inverters in a row. The sizing and the number of inverters used can be tuned to provide the required delay. Figure 7.61 shows the circuit diagram of this simple device.

The benefit of using this method is simplicity. It is well suited to sit-

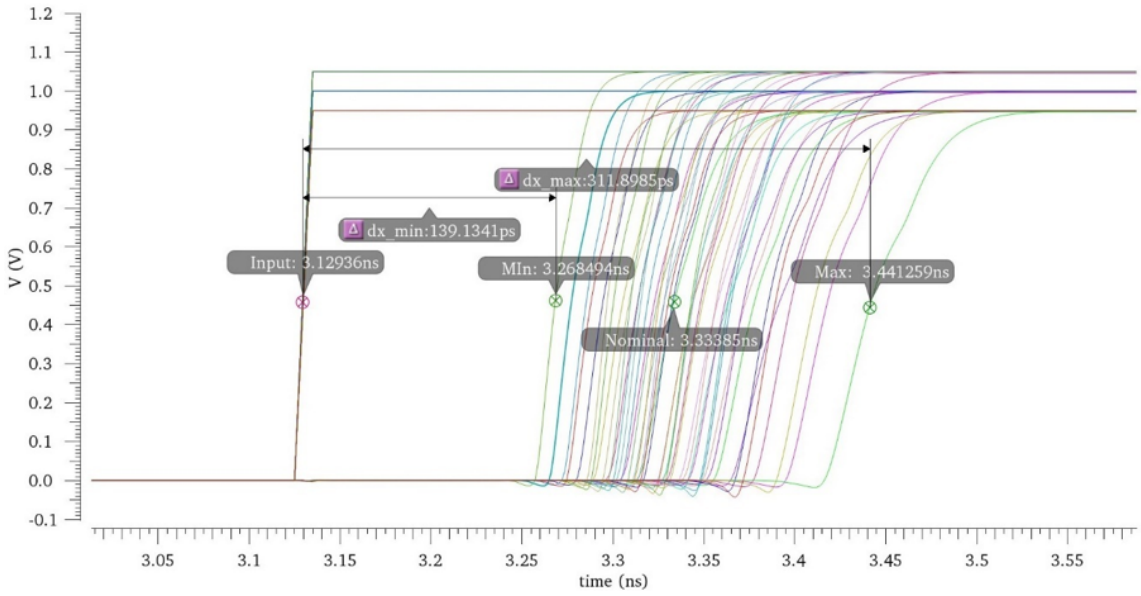

Figure 7.62: Inverter chain across corners

uations when a relatively low delay is needed $(10-200ps)$. However, this method is very power hungry compared to other methods when implementing greater delay values. The relative sizing of the PMOS to NMOS of these inverters can be used to generate a different delay for the rising and falling edges easily. Inverter chains cannot be used when an accurate delay is needed. The inverter chain is unstable across corners as shown in figure 7.62. The delay can be seen to vary form arroud 60% to 150% of its nominal value which is unacceptable for most applications.

In addition to its inherently high variation across corners, the inverter chain delay suffers from high output jitter. Especially for larger values as that the output jitter is proportional to the square root of the number of inverter stages.

The inverter chain can provide an adjustable delay by using a multiplexer. The multiplexer can choose one of the internal nodes of the chain for a

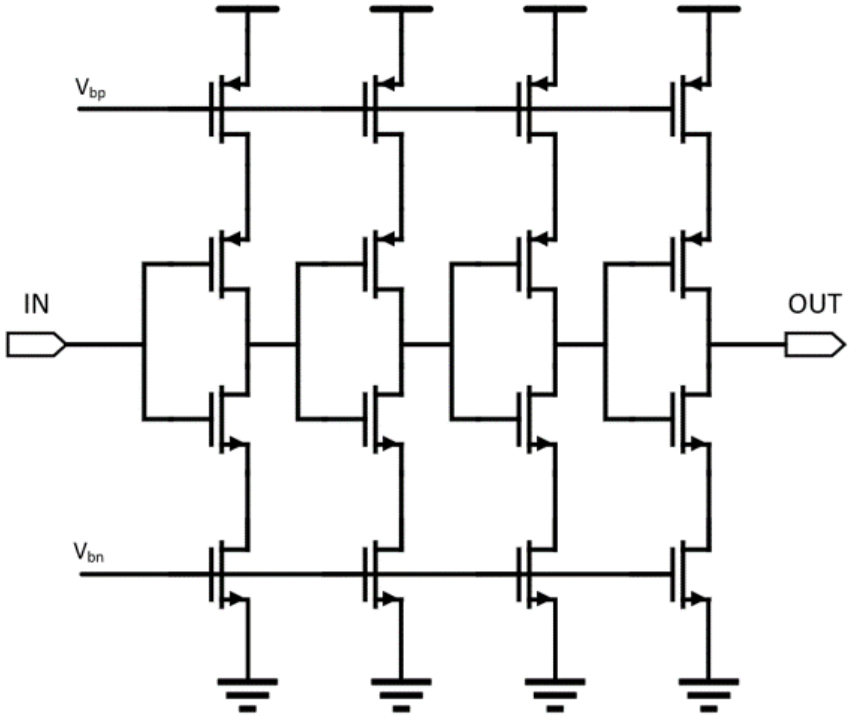

Figure 7.63: Current-starved inverter

shorter delay. As a result, it is a digitally controlled system which is not power efficient and precise compared to the analog control systems. Thus, analog control delay elements are desirable.

7.7.1.2 Current starved inverter delay line

By adding current source-like biasing transistors in series with the inverters, as shown in figure 7.63, this structure is called current-starved inverter. The delay is adjusted using the bias voltage applied to the series transistors changing the current through the inverter. The gate voltage in fact changes the resistance of the transistor. Hence, the current starved inverter is considered a resistive controlled delay element. The delay increases when the current through the inverter is decreased. The bias voltages can be tuned to precisely control the delay. This method consumes lower power

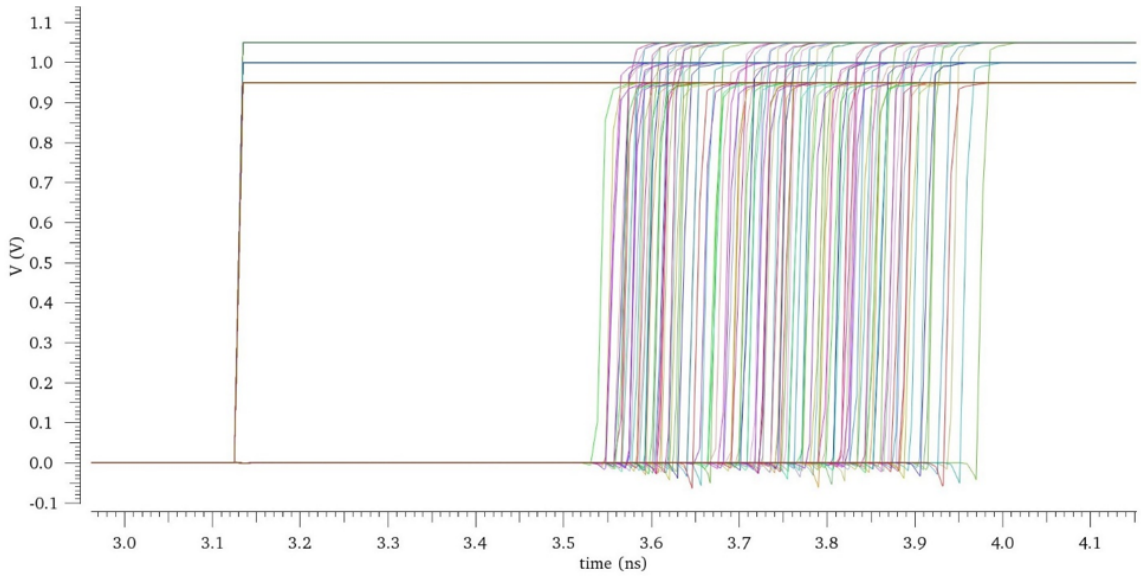

Figure 7.64: Current-starved inverter across corners

than the inverter chain method. It can also produce much larger delay values.

The output jitter can be reduced by using fewer number of inverters with a higher delay each. The bias voltage is generated from a diode connected device. Increasing the bias current helps in decreasing the output jitter as well at the expense of increased static power.

This structure is also sensitive to process and temperature variations. In addition to that, the bias voltage is generated using a reference current source. The variations in the reference current translates to variation in the delay.

The delay variation across temperature, voltage, and process corners is $65\% - 140\%$. To further increase the delay, the inverters can be loaded with capacitors. However, this increases the delay spread across corners due to

the process variations of the added capacitors. In case this architecture is used to generate the required 7ns delay, the generated delay would vary from greatly (4.55-9.8ns) Taking the variations into consideration ahead of time, the delays can be designed to be (3.25-7ns), which always guarantee that the 10 comparison cycles finish before the next track phase. However, this means that the bootstrapped switch must be designed to provide suitable accuracy in 3.25ns only. This is a highly inefficient design methodology. The same applies to the 1ns delay. It can be designed to provide a variation of (0.46-1ns). This would force the reference buffer settling time to be 0.46ns, which is inefficient.

The solution to this problem is to calibrate the delays to a certain value at the start-up of the ADC. This ensures that the design always works in its optimal state and reliefs the tight specifications that are otherwise present to support different operating conditions. In this way, the power usage is reduced due to the fact that various circuit components need not be as fast anymore. The overall area also decreases consequently.

7.7.1.3 Calibratable delay element

For highly critical applications, some manufacturers calibrate their devices after manufacturing their ICs. Each IC is measured and calibrated consequently. This can be done in many ways. One is to have more than one copy of the circuit required to be calibrated and then measure the most fitting one and permanently choose that one by hardwiring a fuse for example. Another more accurate (and much more expensive) method is by tuning certain components like the length of a resistor by laser etching

it and continuously measuring its value until a certain value is achieved. Both methods yield great accuracy in the expense of cost and IC testing time. This is inapplicable in applications where low cost is a must.

In this thesis, the proposed delay element is self-calibrating. At the start up of the ADC, the value of the delay is measured and recalibrated until it matches its set point.

In order to calibrate any physical phenomenon, it must be measured accurately. Any variation or uncertainty in the measuring device is superimposed on the measured value. The idea behind this calibration method arises from the fact that the only component in the entire IC that has a low variation is the 32MHz clock. The clock frequency is generated from a crystal oscillator. The variation in the crystal frequency is typically measured in ppm (parts-per-million). Therefore, if the delay can be compared relative to the input clock period, theoretically, it can be calibrated with ppm accuracy.

7.7.2 Proposed delay calibration system

7.7.2.1 Top level design

The main idea behind this system is that to obtain an accurate absolute value for the delay. Figure 7.65 shows a simplified overview of this delay calibration loop. The calibration is done in a series of steps. The variable delay element is placed in a feedback loop to turn it into an oscillator. The oscillation frequency of this oscillator f_{vco} depends on the variable set delay, hence, it is a Digitally Controlled Oscillator (DCO). The output of this DCO is fed to a frequency divider based on a digital counter. Its purpose is to

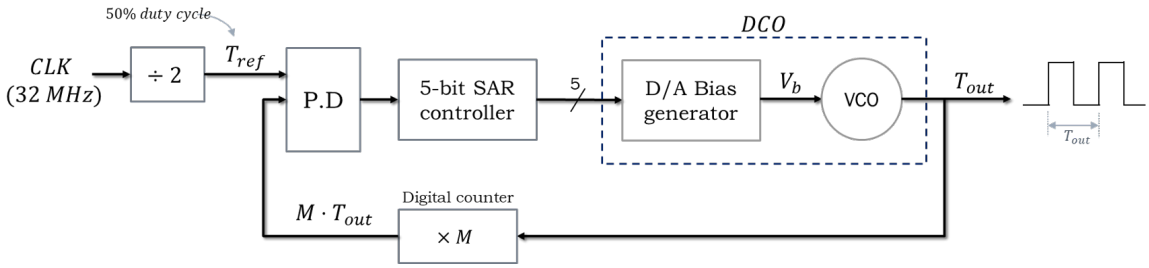

Figure 7.65: Proposed delay calibration system.

adjust the required delay to a value shorter than the input clock period. In this design, since that the delay is used twice in each DCO period:

$$f_{DCO} = \frac{1}{2 \times delay} \tag{7.86}$$

The output of the clock divider is compared to the pulse width of the input clock. However, the 32 MHz clock duty cycle can vary greatly. That is why a divide-by-two block is used. It ensures that the duty cycle is exactly 50% for its 16 MHz output. Its clock-high time is always 31.25 ns exactly. This will now be the reference time period that the delay will be compared against.

In order to calibrate the delay to $\approx 1\ ns$, the divide-by-M block is used, with M=15.5.

At the positive edge of the 16 MHz clock, the DCO is triggered and its output starts. The counter had been reset and starts counting to M. Outputting '0' until it counts M cycles. Its output is sampled at the negative edge of the 16 MHz clock. Depending on the value of the delay at that calibration cycle, the counter may have reached M or not Outputting either a '0' or a '1'. This value indicates whether 31 times the delay (15.5×2) is greater than 31.25 ns.

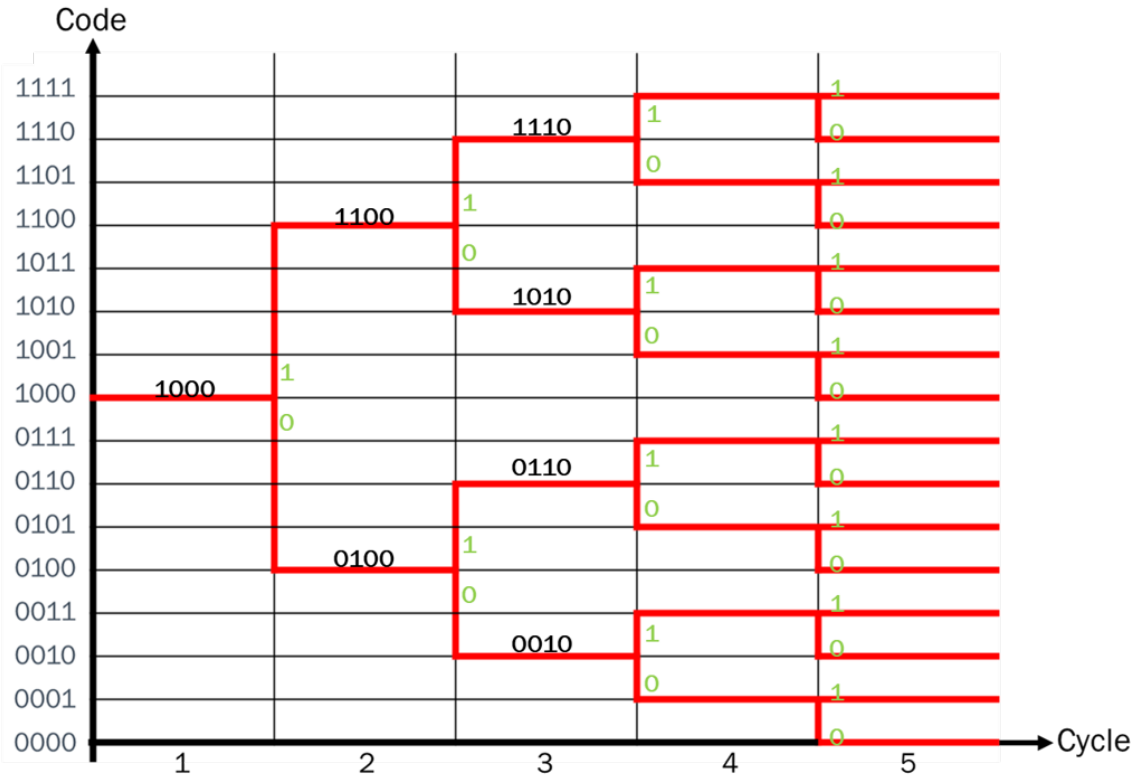

Figure 7.66: 5-Bit binary search algorithm.

Based on this measurement, the delay value can be increased or decreased accordingly. The delay is then remeasured with the next positive edge and its accuracy increases more and more with each cycle.

A binary search algorithm is used to find the best fitting delay value. Binary search only needs N cycles to reach N-bit accuracy. The DCO used in this work is 5-Bits, hence, the calibration time is 5 clock cycles. The calibration clock is 16 MHz, which gives a calibration time of 312.5 ns. The SAR logic starts from the mid scale "10000_2" working its way to the last bit as shown in figure 7.66.

7.7.2.2 Digitally Controlled Oscillator (DCO)

The DCO consists of a Digital to analog Bias generation circuit and a Voltage Controlled Oscillator (VCO). The VCO is based on the calibratable delay element that is intended for calibration.

Calibratable delay element

The calibratable delay element, as shown in figure 7.67, is implemented based on the current starved inverter chain concept. It is designed to provide a 1 ns delay for the rising edges of its input signal. The first inverter stage has an NMOS (NM1) acting as a current source. The bias voltage applied to this transistor controls the delay applied to the rising edge of the input signal. The falling edge experiences a negligible delay. The sizing of this circuit is designed to produce delays ranging from 0.2ns to 3ns for various values of V_{bn} while guaranteeing that the 1ns point always lies in that range for all possible process corners.

Digital to analog Bias generation circuit

The bias voltage Vb_n is generated using a current mirror with variable digitally controlled mirroring ratio. Figure 7.68 shows the bias generation circuit. The control signals Vc_1 through Vc_5 are the 5-Bit digital signals used to either enable or disable their corresponding branch. The current mirror branches are binary weighted to produce 32 different delay values.

A cascode current mirror is used to mirror the 5μ A input reference current (I_0) to the variable current mirror. The cascode current mirror has the benefit of having a higher mirroring accuracy and stability with temperature variations.

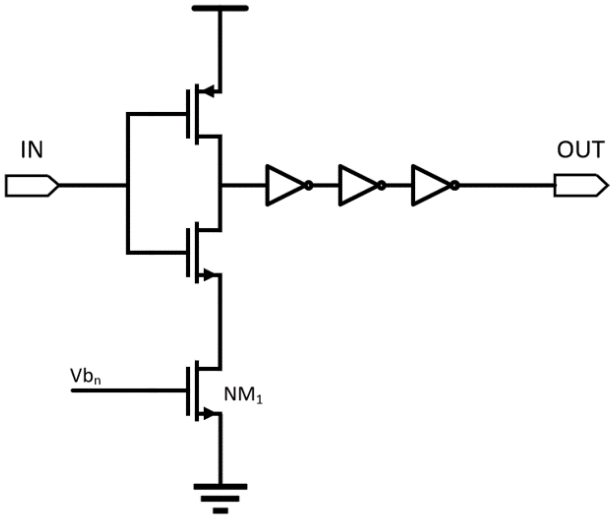

Figure 7.67: Calibratable delay element.

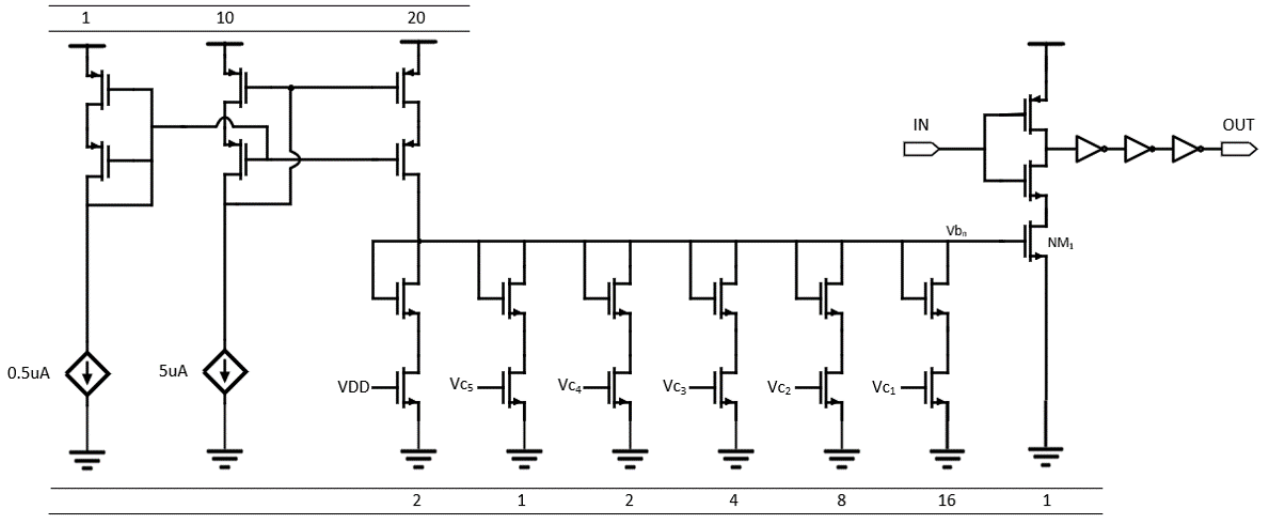

Figure 7.68: Digital to analog bias generation circuit.

With the rising edge of the input to the delay element, the capacitance on the output node of the first inverter stage is discharged through the current source biased by Vb_1. For the sake of simplicity, assuming that this capacitance (C) is constant and that the discharge current (I_d) is also constant, the delay can be calculated as follows:

$$i = C\frac{dv}{dt}, \quad delay = C \times \frac{VDD}{2} \times \frac{1}{I_d} \tag{7.87}$$

The delay is inversely proportional to I_d, which is the only variable in this simple model, and it depends on the mirroring ratio. The first cascode current mirror has a mirroring ratio of 1:2, doubling the input current, increasing the linearity. The digital inputs Vc_1 through Vc_5 can vary the mirroring ratio of the variable current mirror form 2:1 to 33:1 giving a total mirroring ratio of $\frac{2}{N}$, where N ranges from 2 to 33. The delay can now be calculated to be:

$$delay = C \times \frac{VDD}{2} \times \frac{N}{2I_o} \tag{7.88}$$

Which indicates that the delay is directly proportional to N. The lowest mirroring ratio (Highest N) will result in the longest delay and vice versa.

Voltage Controlled Oscillator (VCO)

The VCO is constructed using as shown in figure 7.69 using two of the variable delay element blocks in feedback. Initially, the clock is LOW, hence, the flipflops are reset. With the clock rising edge, delay block A is triggered, and its output rises after a certain delay. This delayed output is stored in a D-flipflop. This flipflop triggers the delay block B in a similar way. Each delay block is self resetting. The inverted output of each flipflop $(\bar{Q})$ is buffered

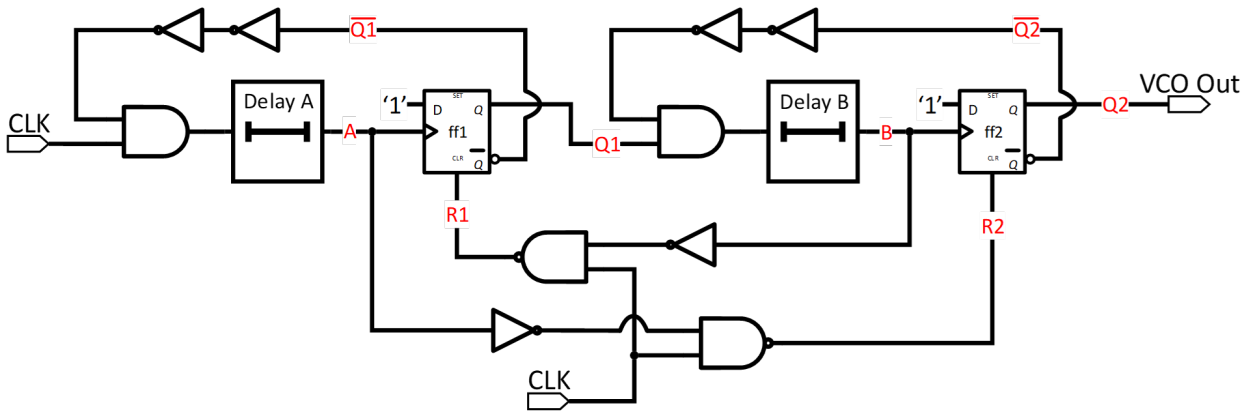

Figure 7.69: Voltage Controlled Oscillator (VCO).

then used in feedback to reset its delay block to make it ready for the next cycle. The buffering inverters are used to add extra delay before resetting the delays to ensure proper flipflops resetting and to prevent setup and hold time violations. Each flipflop is reset when the other delay block is activated.

In this configuration, the delay blocks are used to generate a digital oscillating signal from either one of the flipflops. if the delay provided by each block is t_d, then the frequency of oscillation is given by this simple equation:

$$f_{vco} = \frac{1}{2t_d} \tag{7.89}$$

The period of this output is twice the delay since that the HIGH and LOW times are generated by one delay each. The extra parasitic delays due to the digital circuitry are negligible.

$$T_{DCO} = T_{min} + n \times T_{LSB} \tag{7.90}$$

$$T_{LSB} = \frac{T_{max} - T_{min}}{2^N} \tag{7.91}$$

The D2A bias generator circuit sets the delay; hence the frequency, making

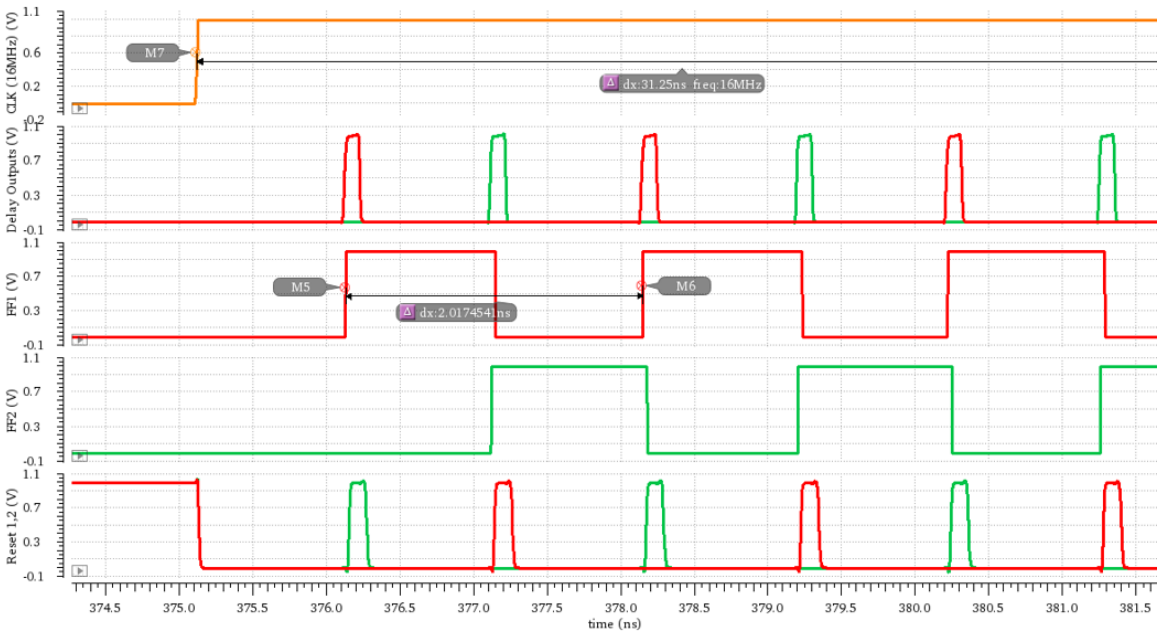

Figure 7.70: VCO waveforms.

this system a digitally controlled oscillator (DCO). The Period of oscillation is set digitally with a linear relation to the digital code. This is the key difference between this DCO and other VCOs commonly used in PLLs. The digital code linearly adjusts the period ($n \propto T \propto \frac{1}{f}$), while for the ones used in PLLs, the digital code linearly adjusts the frequency ($n \propto f \propto \frac{1}{T}$). Figure 7.70 shows the VCO output in action.

7.7.2.3 Frequency divider and phase discriminator

It is based on a 4-bit ripple counter as shown in figure 7.71. This counter is reset before each calibration cycle and starts counting with the output from the DCO. A four-input NOR gate detects the "11112_2" from the counter and triggers a flip flop. This is the output of the frequency divider. The output of the DCO is taken from the second flipflop, counting an extra half cycle. Therefore, M is equal to 15.5.

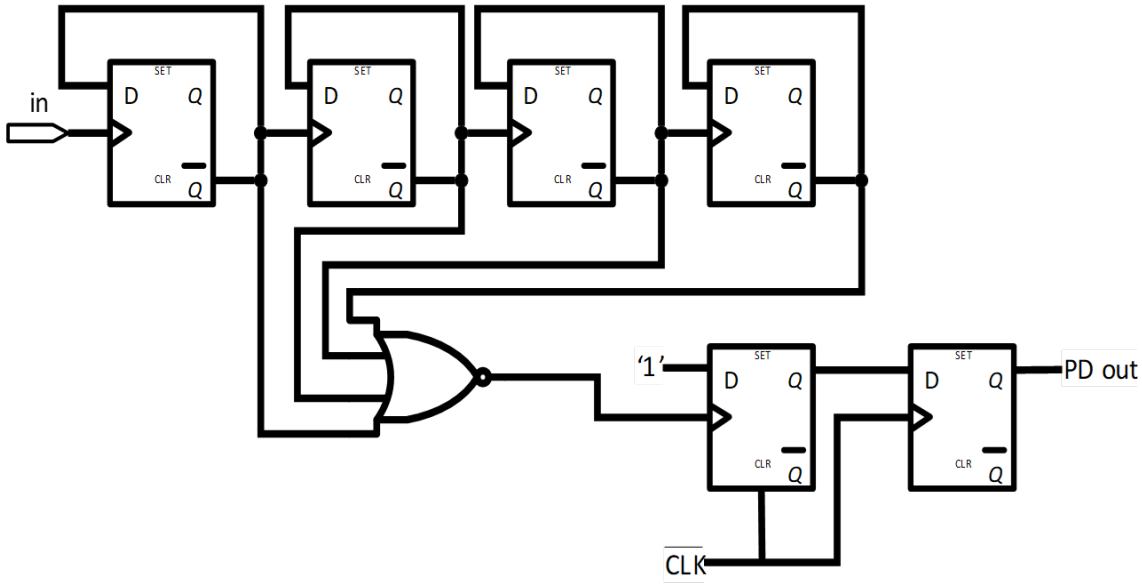

Figure 7.71: Digital counter.

$$\mathrm{T}_{divider} = MT_{in}, \quad T_{in} = 2t_d, \quad T_{divider} = 31t_d \tag{7.92}$$

The output of the frequency divider is sampled at the negative edge of the 16 MHz clock using another flip flop. This flip flop functions as a phase discriminator. It is used to decide if a time event T_{event} leads or lags a reference event T_{ref}.

T_{event} here being whether the counter has finished counting, indicating that the delay is probably lower than needed or otherwise. While T_{ref} being the pulse width of the reference 16 MHz clock (31.25ns).

$$Y_{PD} = \{1\ (lead), \quad T_{out} \leq T_{ref} 0\ (lag), \quad T_{out} > T_{ref} \tag{7.93}$$

- If the targeted delay in the lock region then the loop will lock at:

$$T_{ref} = M\left(T_{out} \pm T_{LSB}\right) \tag{7.94}$$

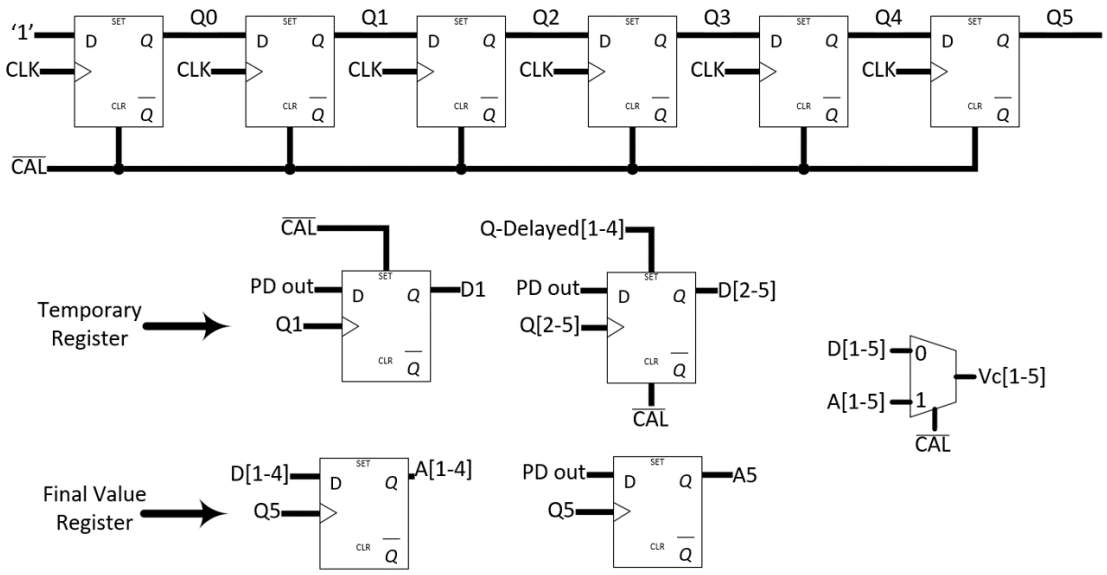

Figure 7.72: 5-Bit SAR controller implementation.

$$T_{out} = \frac{T_{ref}}{M} \pm T_{LSB} \tag{7.95}$$

- The output time jitter is dominated by the DCO time jitter.

$$T_{ref} = M\left(T_{out} \pm T_{LSB} + t_{jitter}\right) \tag{7.96}$$

$$T_{out} = \frac{T_{ref}}{M} \pm T_{LSB} + \ t_{jitter} \tag{7.97}$$

7.7.2.4 SAR controller

The brains of the delay adjustment system lies inside the SAR controller logic. The Binary Search algorithm is implemented in a simple yet effective manner. Figure 7.72 shows the circuit representation of the digital logic used in this system.

The input for the SAR logic is the output of the Phase-Discriminator (PD out), Calibration control line (CAL), and the 16 MHz Clock (CLK). The Calibration control line (CAL) is one of the ADC inputs that must be activated

by the ADC start up control logic. It should be raised to VDD for five 16MHz periods and then lowered again indicating that the delay adjustment system has finished the calibration process and that the ADC is ready to commence its conversions.

Initially, CAL is '0', resetting all the crucial flipflops in the SAR controller. When raised to VDD, the outputs Q[1-5] start getting raised as well consecutively with each of the five clock cycles. These are control signals that are used by the SAR controller itself. A delayed version of these signals (only 1-4) is generated by using an inverter delay line or any other relatively short delay method. These are also required for proper operation.

Another set of D-Flip-flops (register) is used to hold the temporary value of the VCO digital control signal (Vc[1-5]) during the binary search period. The signals Q[1-5] is used as a clock for each flip-flop. And the PD output as the input for them. In that way, the PD output is stored bit by bit in this register. The delayed-Q signal is used to implement the activation of every next bit. This way, the binary search algorithm is applied. With the activation of the last bit (Q5), the temporary value is stored permanently in another register. Five 2-to-1 multiplexers (MUXs) are used to select between connecting the VCO control signal (Vc[1-5]) to either the temporary register during the calibration phase (while CAL='VDD') or otherwise connect it to the final value register for normal operation.

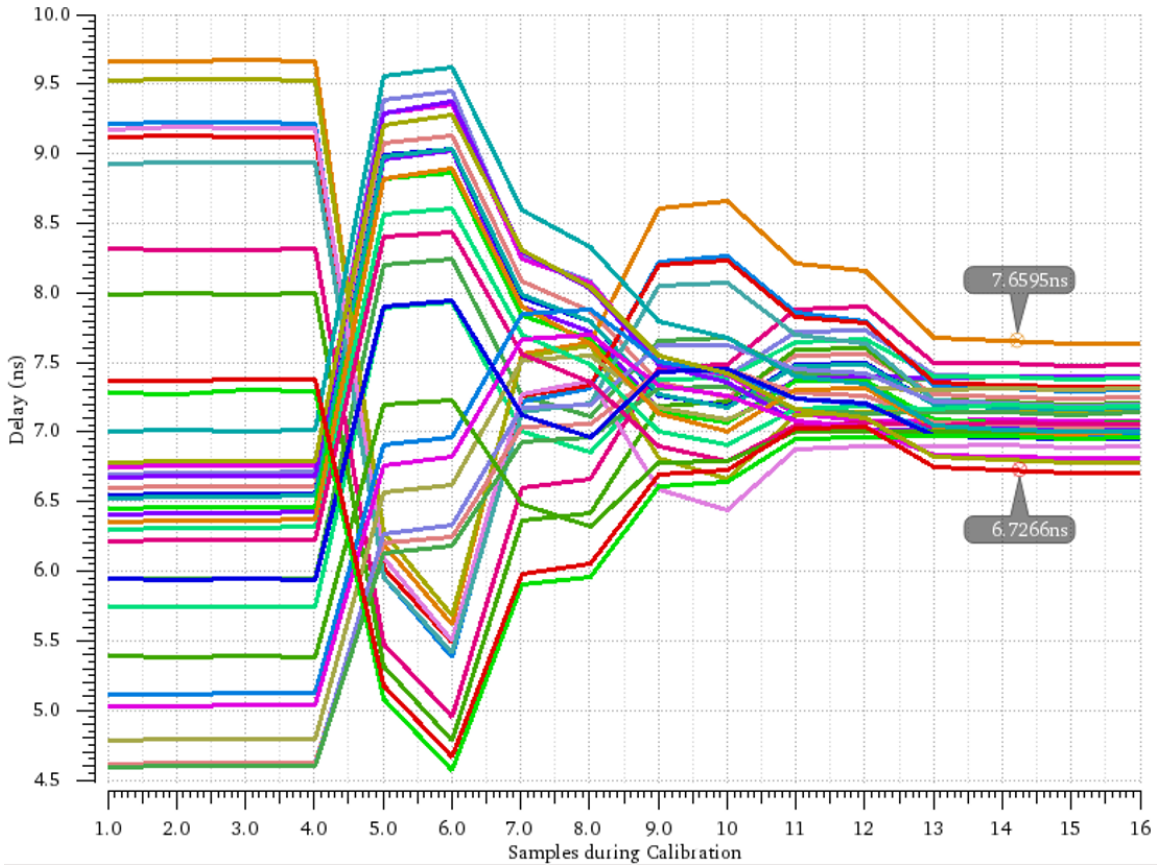

Figure 7.73: Corners simulation for the delay calibration progress.

7.7.3 Integration

The delay units are calibrated inside their loop in this calibration system. However, these delay units will be required to be connected elsewhere in the ADC. For this reason, a digital 2-to-1 MUX is used before each delay unit to select either to connect it to the calibration loop or reconnect it to its desired circuit. Also, a decoder is used after the delay unit for the same purpose and to prevent unnecessary dynamic power consumption in the calibration loop when the delay unit is reconnected back to its circuit.

7.7.4 Simulation results

The delay calibration system must be tested across corners to validate that the delay value after calibration is within the acceptable limits of variation. As seen in Figure 7.73, the variation is very high (4.6-9.7ns) which corresponds to a variation of $\pm 30\%$ before the calibration starts. However, after the calibration ends, the variation is low to an acceptable value $\pm 6.5\%$. The set value for this calibration run was 7ns. For other applications where more absolute value accuracy and lower variation is needed, the number of bits of the SAR controller and the variable delay elements could be increased. However, 5 bits was very reasonable in our case.

7.7.5 System advantages

The proposed delay calibration system has many merits that encourage any designer with a similar problem to implement. Among these merits is that the entire calibration process is only required to be carried out once when the ADC is power on, consuming a minimal amount of power in the process. After that, the entire system can be shut down for zero static and dynamic power (except for the bias generation circuit which consumes a small amount of static current, 15.5μ A in our case). This makes it a very low power solution. Another advantage is that the delay unit which is calibrated to a certain value can be cascaded multiple times in order to generate multiples of that delay. This was the case with the 7ns delay used to adjust the tracking clock of the ADC. The delay unit was calibrated to be a close to 1ns.

Also, if fractional (shorter) values of the delay are required, the delay unit itself can be biased with different values of currents. The same effect can also be done by changing the multipliers of some of its transistors. This shows that multiple accurate delays can be placed in the ADC with arbitrary values using only one calibration loop that only operates once at start-up. The binary search algorithm used unsure fast locking and is a self calibrating process which a great advantage of the design. Off-chip calibration or post-manufacturing calibration is not required.

7.8 Leakage Current

In low power circuit design, low leakage current when the device is turned off is just as important as low power consumption during operation. And in some cases, it is more important. A circuit element may only be required for limited periods of time. It could be turned on when needed and turned back off to save power. The leakage current may be the deciding variable of how long a device is expected to operate on a single battery charge.

Leakage current can come from many sources. When a MOS transistor is switched of, we expect that a transistor in its cut-off region acts as an open switch with infinite resistance. In the real case, a turned off MOS switch has a finite resistance value that is responsible for a small amount of leakage current.

Another source of leakage is the gate leakage. Ideally, the gate has an infinite resistance and passes no DC current. In the real case, a small gate current passes through the gate to the source or drain or vice versa depending on the terminal differential potential conditions. This gate leakage current is due to the quantum tunneling through the gate oxide. These two

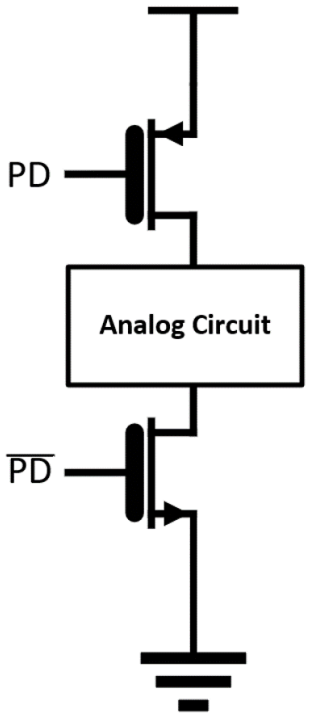

Figure 7.74: Power down transistor.

effects increase with decreasing the transistor feature size. The gate oxide thickness keeps decreasing, increasing the gate leakage, and short channel devices suffer from higher leakage that long channel devices as well.

The leakage current specifications that we were executing implied the impossibility of using conventional thin 1.2V devices. These devices as explained above suffer greatly concerning leakage due to their thin gate oxide. Also, these devices generally have a lower R_{on}/R_{off} values than a similarly sized thick device. This along with the fact that the gate oxide of the "Thick" devices is much thicker than the thin devices' oxide was a deciding variable on choosing to use the thick devices. This ensures that the gate leakage is minimized (in the order of $aA - pA$ compared to nA range of thin devices).

Thick MOS devices are rated for 2.5V operation, which is much greater

	Specification			Achieved			Units
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Power Down Current	-	5	50	0.7	1.3	40	nA

Table 7.9: Power Down Current across corners and Monte Carlo

than our 1V supply voltage. For this reason, underdriven 1.8V devices were used instead.

As shown in figure 7.74, PMOS transistors were used to completely turn of the VDD supply from the circuit that is required to be turned off. And NMOS transistors were used for the GND rail in the same manner. These two transistors were sized with a minimum length of $400nm$. The width was chosen according to the on-mode current draw. Wider transistors were used for more power hungry components ensuring minimal voltage drop during normal operation. All the circuit simulations carried out in this chapter were carried out with the power down transistors in place, to verify that all devices are operational and working even under their effects and hindrance.

Table 7.9 shows the DC simulation results of the entire ADC at power down. The specifications were met across all design corners, including the temperature, voltage, process variations, etc... Added to that, the $3-\sigma$ variations of the Monte Carlo simulation.

7.9 ADC specifications and final simulation results

7.9.1 Corners and Monte Carlo results:

Having completed the ADC design, corners and Monte Carlo simulations are a crucial step to ensure that the design is viable and working and that it could be manufactured and implemented with a respectable yield

Table 7.10: Required vs. achieved specifications

Specification	Required			Achieved			Units
	Min	Typ	Max	Min	Typ	Max	
ENOB	9			9.066	9.755	9.93	Bits
SNR		-		57.85	60	61.53	dB
SFDR		-		69.3	72	76	dB
Input Capacitance		1			0.472		pF
Leakage Current		5	50	0.7	1.3	40	nA
Min T_{sample}	3	8		6.72	7	7.66	ns
Data Latency		1			1		CLK cycle
Power up time		1	2		0.35	0.4	s
Current Consumption		200	240	79	103	198	μA
Reference Current Consumption		10	20	-1.8	1.75	9.45	μA
DNL	-1		1	-0.4	0	0.4	LSB
INL	-1		1	-0.2	0	0.2	LSB
Offset Error	-15		15	-2	0	1	LSB
Gain Error	-1		1	0.53	0.69	0.98	%FS

percentage.

The testbench used for testing these specs uses an input pure tone signal with a frequency of 625 kHz. It has a full scale amplitude (-1% for gain error compensation) and it is raised to VDD/2 common mode value.

The ADC is given its appropriate control signals in order to start it up at first, enabling the delay calibration system and after that setting up the offset cancellation. After the start-up sequence ie complete, five complete periods of the sinusoid are sampled at 32MHz using the ADC. The digital 10-Bit output is fed to an ideal DAC. The output of this DAC is used to extract the specs shown here.

Table 7.10 shows the required VS. achieved specifications. Theses results include the typical simulation results, the maximum and minimum values of the corner simulations added to it the $3-\sigma$ variations from the Monte Carlo simulation of the entire ADC. As clearly seen, all the specifications

are met. And some even a high margin indicating that the design was implemented successfully with good optimization and design practices.
The Walden figure of merit can be also calculated:

$$FOM_{walden} = \frac{power}{2^{ENOB} \times f_s} \tag{7.98}$$

$$= \frac{103\mu}{2^{9.755} \times 32 \times 10^6}$$

$$= 3.725\ fj/conv.\ step$$

This shows that the ADC has a competitive FOM. However, this FOM was calculated without the digital power consumption. Estimating the digital power as another $60\mu W$, the Walden FOM can be recalculated to be $\approx 6\ fj/conv.\ step$.

7.9.2 Offset cancellation results:

The Monte Carlo simulation shows that the offset error before being cancelled ranges from $\pm 17.3mV$ which corresponds to $\pm 22LSB$. This is shown in figure 7.75.
After the calibration, the offset only varies with $\pm 1LSB$ around the midscale values. This is shown in figure 7.76.

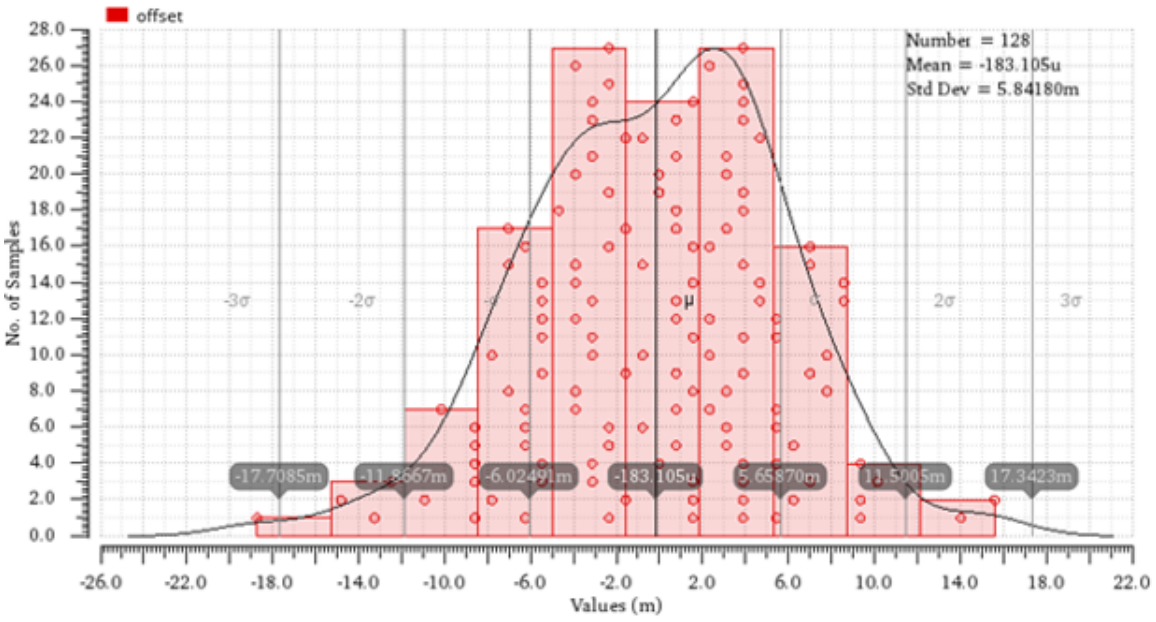

Figure 7.75: Offset error before being cancelled.

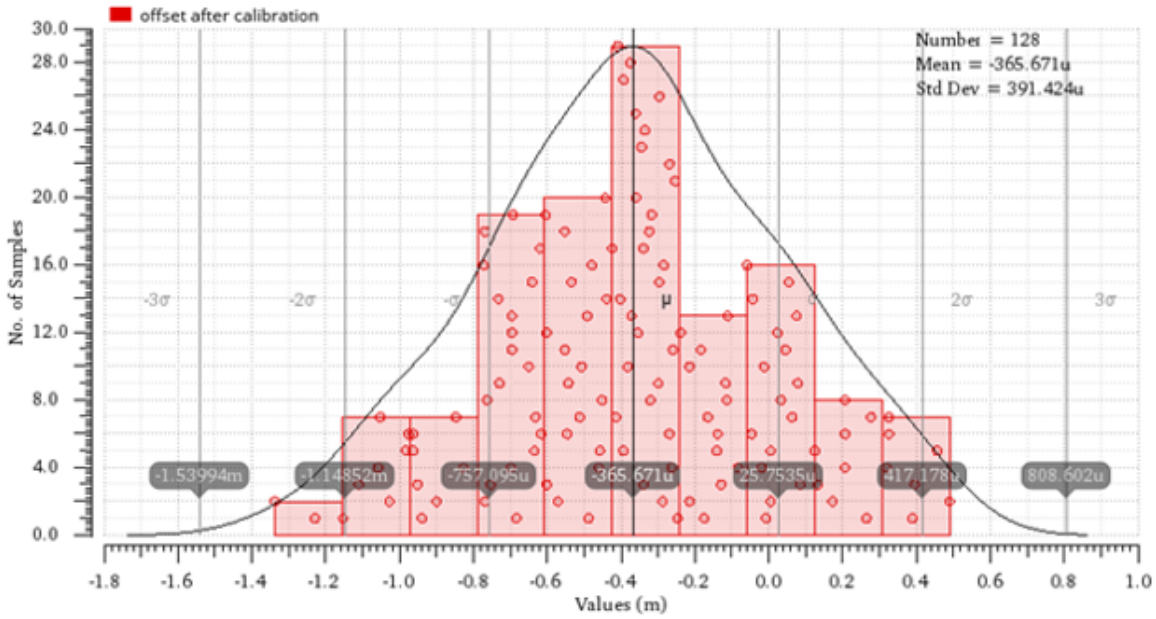

Figure 7.76: Offset error after the calibration

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