Cairo University

DESIGN OF A BLUETOOTH LOW-ENERGY CURRENT MODE RECEIVER FOR IOT APPLICATIONS IN 65nm CMOS TECHNOLOGY

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Abstract

With the increasing need for the Internet of things (IoT) in daily lives, Bluetooth (BT) technology has become a popular solution for portable devices. It is used in mobile phones, medical sensors, and many other consumer electronics. The main reason that BT was the best candidate for IoT compared to other wireless devices was the introduction of the energy saving feature, BLE. The key elements that allow BLE to have the lowest cost possible are the industrial, science, and medical (ISM) band, IP license, and low power. Low power is necessary for mobile devices because consumers are expected to use the devices for extended periods without charging or changing the power source. In cooperation with Si-Vision Inc., we were working to design state of art integrated CMOS RF receiver extracting the required specifications from Bluetooth Core V.5 standard and going through the complete circuit design.

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1 Chapter 1: Introduction to Bluetooth Low Energy (BLE)

1.1 Introduction

Bluetooth is a wireless technology standard. Bluetooth was developed as a way to exchange data over a short range without the need for wires. That's why Bluetooth is used for wireless headsets, hands-free calling through your car, and wireless file transfers. When considering the difference between Bluetooth and Bluetooth Low Energy (it's newer sibling), it's important to talk about power consumption. Bluetooth was originally designed for continuous, streaming data applications. That means that you can exchange a lot of data at a close range. That's why Bluetooth is such a good fit for consumer products. People like to receive data and talk at the same time, and exchange videos from one device from another. Here are some machine-to-machine (M2M) and Internet of Things (IoT) uses for Bluetooth wireless handsets, file transfer between devices, wireless keyboards and printers, and wireless speakers.

1.2 Bluetooth Vs. BLE

Bluetooth Low Energy hit the market in 2011 as Bluetooth 4.0. When talking about Bluetooth Low Energy vs. Bluetooth, the key difference is in Bluetooth 4.0's low power consumption. Although that may sound like something negative, it's actually extremely positive when talking about M2M communication. With Bluetooth LE's power consumption, applications can run on a small battery for four to five years. Although this isn't ideal for talking on the phone, it is vital for applications that only need to exchange small amounts of data periodically.

Just like Bluetooth, BLE operates in the 2.4 GHz ISM band. Unlike classic Bluetooth, however, BLE remains in sleep mode constantly except for when a connection is initiated. The actual connection times are only a few mS, unlike Bluetooth which would take ~100mS. The reason the connections are so short, is that the data rates are so high at 1 Mb/s.

In summary, Bluetooth and Bluetooth Low Energy are used for very different purposes. Bluetooth can handle a lot of data, but consumes battery life quickly and costs a lot more. BLE is used for applications that do not need to exchange large amounts of data, and can therefore run on battery power for years at a cheaper cost. It all depends on what you're trying to accomplish.

1.3 Key Factor of BLE

The key elements that allow BLE to have the lowest cost possible are the industrial, science, and medical (ISM) band, IP license, and low power. One major advantage of using the ISM band is that a permit or fee is not required, although it must follow a specific power requirement for data transmission. The maximum power fed into the antenna must be lower than 30 dBm (equivalent to 1W). The BT special interest group (SIG) provides a reasonable price for an IP license, which is relatively lower than other competitors. The cost of the license can be reduced, because an increasing number of customers and users are supporting BLE devices.

Low power is necessary for mobile devices because consumers are expected to use the devices for extended periods without charging or changing the power source. Making a sustainable device requires more energy storage, low power consumption, or both. However, the energy storage in the device demands additional space. The large device size also meant that manufacturing costs were higher, so increasing the energy storage was an inefficient solution for long-period usage. Therefore, lowering the power of the device not only reduces manufacturing cost but also improves battery usage. Since more power is needed for the device, more space is preserved for the power source or battery.

Even though low power is suitable for the device, sometimes the device needs to operate at high speeds for some specific applications. Therefore, BT version 4.0 was introduced to combine the needs of different usage modes, which led to a solution that allowed for BT to have three operation modes.

1.4 Operation Modes

After BT had evolved to version 4.0, it had three different modes, which are classic BT, BLE, and dual-mode. The Bluetooth Smart Ready mark represents the dual mode, the Bluetooth mark represents the classic BT mode, and the Bluetooth Smart mark represents BLE mode.

Classic BT was initially designed to connect two devices at a short distance for transferring data, such as linking mobile phones to computers. Furthermore, the application was improved to not only transfer data but also to stream audio and video. This improvement provided a robust wireless connection between devices ranging from smartphone and car audio devices to industrial controllers and medical sensors. However, BLE became a more power efficient and cost-effective solution for many of these applications.

When comparing BLE to classic BT, the main difference is power dissipation. The BLE devices manage to operate for extended periods of time. This advantage is beneficial in machine to machine (M2M) communication because it can last for years without changing the power source once the BLE device is placed in the machine. However, to achieve this goal, the data transmission rate must be sacrificed in exchange for low power dissipation.

BLE devices slow down the data transfer rate, though it effectively decreases the power consumption. Unlike classic BT devices, BLE devices do not need to be at the highest speed possible. For example, while one uses the smartphone to switch on the air conditioner and adjust the room temperature, these applications do not have significant data to transfer. It simply needs to send the package containing “power on” and “increase/decrease temperature” from the transmitter to the receiver. On the other hand, while one uses a smartphone to stream television through a BT connection, it is not a simple package containing a single command; instead, it can be a high definition (HD) video or high quality (HQ) music file that must be smoothly played on television. Otherwise, the user will never replace the wired connection with wireless.

1.5 Summary

Chapter 1 discussed the specifications of BLE compared to BT. The structure is slightly different from the structure of BT because of the low energy requirements. The ISM band, IP license, and low power are key elements that allow BLE to have the lowest cost possible. The design of BLE was introduced to have an overview of the technology that is utilized in this paper.

2 Chapter 2: Receiver architectures for BLE

2.1 Direct Conversion Receiver

A study for different receiver architecture to achieve the highest level of integration, lowest power consumption, and best performance. Of course, all these requirements are not met in a single architecture, and therefore, trade-offs were closely studied to find the best architecture that meets the standard specifications with enough margins at lower cost. Two very common architectures are used for Bluetooth receivers, direct-conversion and low-IF.

Although the direct-conversion architecture lends itself to higher integration levels and lower power consumption, it is plagued by quadrature demodulation phase errors, quadrature gain phase mismatch, DC offsets, 1/f noise, and LO feedthrough [1]. Low-IF architecture [2] can be used to avoid the DC offset and 1/f complications associated with direct-conversion. However, Low-IF architecture suffers from the image problem due to the non-zero IF frequency.

The choice of the most suitable receiver architecture depends on many parameters in the wireless standard (e.g. channel bandwidth, preamble time, blocking specifications, sensitivity, modulation format, etc..). In the following two sections, both possible architectures of the Bluetooth receiver will be discussed in some detail.

2.2 Direct-Conversion Receiver Architecture

In direct-conversion receiver (DCR) architecture, the signal is down-converted directly from RF to baseband. A low-pass filter is then employed to suppress nearby interferers as shown in the simplified diagram in Fig.2.1. The use of quadrature I and Q channels is necessary in the Bluetooth case because the signal is frequency-modulated, and therefore the two sidebands of the RF spectrum will carry different information. The spectrum of the complex output signal I+jQ will be a replica of the signal spectrum at RF, but down-converted around dc. Despite the simplicity of the DCR architecture, it suffers from some serious design issues that do not exist or are not as serious in low-IF receivers.

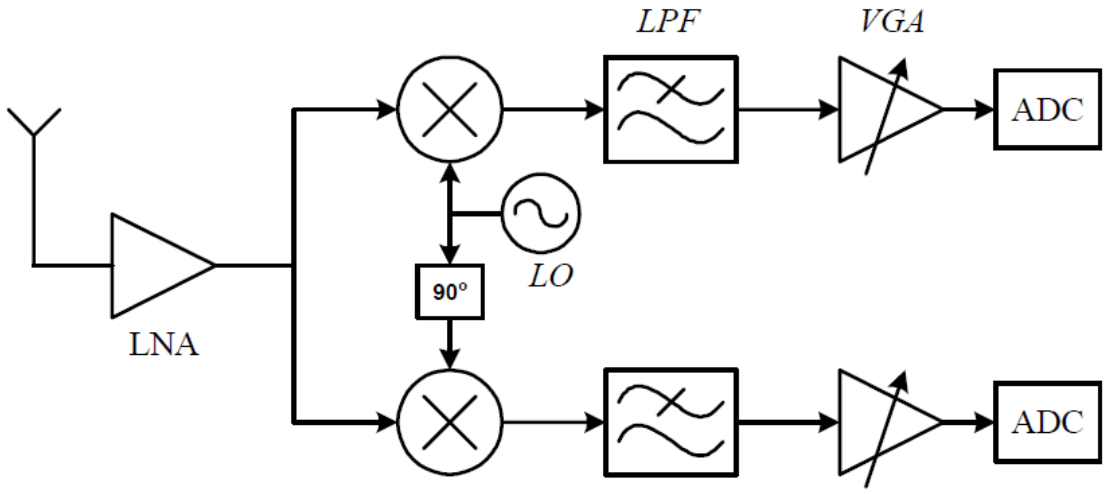

Figure 2–1: Direct-Conversion receiver architecture

2.2.1 DC Offsets

There are different sources of DC offsets in an integrated receiver; (1) components mismatches, (2) LO self-mixing, and (3) interferers self-mixing. These sources are explained as follows: (1) Typical MOS transistor VT mismatches are in the order of few millivolts. This might be quite higher than the desired signal level at the mixer output. (2) Due to capacitive and substrate coupling, isolation between the LO port and the inputs of the mixer and the LNA is finite. This effect is called LO leakage. The leakage signal appearing at the input of the LNA and the mixer is now mixed with the LO signal thus producing a dc component at the mixer output. If the LO signal level is 0dBm, and isolation between LO and LNA input is 60dB, then the LO signal at the LNA input is about -60dBm, quite substantial compared to the minimum signal (sensitivity) level at the receiver input. (3) This effect is similar to LO self mixing. When a large interferer leaks from the LNA or mixer input to the mixer LO port, it mixes with itself and generates a low frequency beat at the mixer output corresponding to amplitude variations in the interferer. This resulting offset is even harder to reject since it is varying with time.

This means that if the desired signal level at the end of the receiver chain is at the full swing of the final stage, the dc offset generated by mismatches will saturate the receiver stages. Therefore, this dc offset has to be rejected before it gets amplified by the receiver stages. A possible approach to removing the offset is to employ ac coupling, i.e.

high-pass filtering, in the down-converted signal path. However, since the spectrum of the Bluetooth GFSK signal exhibits a peak at dc, such signal may be corrupted if filtered with high cutoff frequency.

2.2.2 Flicker Noise

In modern technologies and for the minimum gate-length transistors required by RF circuits, the 1/f noise (also called flicker noise) component might exceed the white noise up to several megahertz. On the one hand, flicker noise is not a limiting effect for linear RF circuits, as in the low noise amplifier (LNA) since the operating frequency is much higher than the corner frequency. On the other hand, since minimum length transistors are used in the switching transistors and due to the nonlinear operation of the mixer and the finite slope of the LO signal, flicker noise of the switches appears at the baseband output of the mixer. Flicker noise of the transistors used in the baseband circuits also falls in the signal band and degrades the system noise figure (NF). NF degradation depends on the flicker noise corner frequency and the channel bandwidth. In the case of Bluetooth, the -3dB bandwidth of the signal is about 500kHz, while the 1/f corner frequency is about 1MHz or even larger for smaller transistor lengths. This NF degradation might be so significant that it disqualifies DCR architecture as the optimum choice for Bluetooth. The effect of flicker noise can be reduced by a combination of techniques. As the stages following the mixer operate at relatively low frequencies, they can incorporate longer devices to minimize the magnitude of the flicker noise. Moreover, periodic offset cancellation also suppresses low-frequency noise components through correlated double sampling.

2.2.3 Even Order Distortion

Unlike other architectures, even-order distortion in the LNA and mixer input transistor becomes problematic in DCR architecture. Suppose, as shown in Fig. 2.2, two strong interferers ($A_1 \cos(w_1 t) + A_2 \cos(w_2 t)$) close to the desired channel experience a second order nonlinearity in the LNA represented as $y(t) = \alpha_1 x(t) + \alpha_2 x^2(t)$, then y(t) contains a low frequency term $\alpha_1 A_1 A_2 \cos(w_1 - w_2)$t . Upon multiplication by cos(W_{Lo}t) in an ideal mixer, such a term is translated to high frequencies and hence becomes unimportant. In reality, however, mixers exhibit a finite direct feedthrough from the RF input to the IF output due to mismatches between transistors and deviation of LO duty

cycle from 50%. The natural solution to suppress even-order distortion is to use differential LNA and mixer. However, two issues arise here. First the antenna and the duplexer filter are usually single-ended. This necessitates the use of a balun (transformer) to do the single-ended to differential conversion. Baluns typically exhibit several decibels of loss at high frequencies. This loss directly raises the overall system noise figure. Second, differential LNA requires more power consumption than the single ended counterpart to achieve the same noise figure.

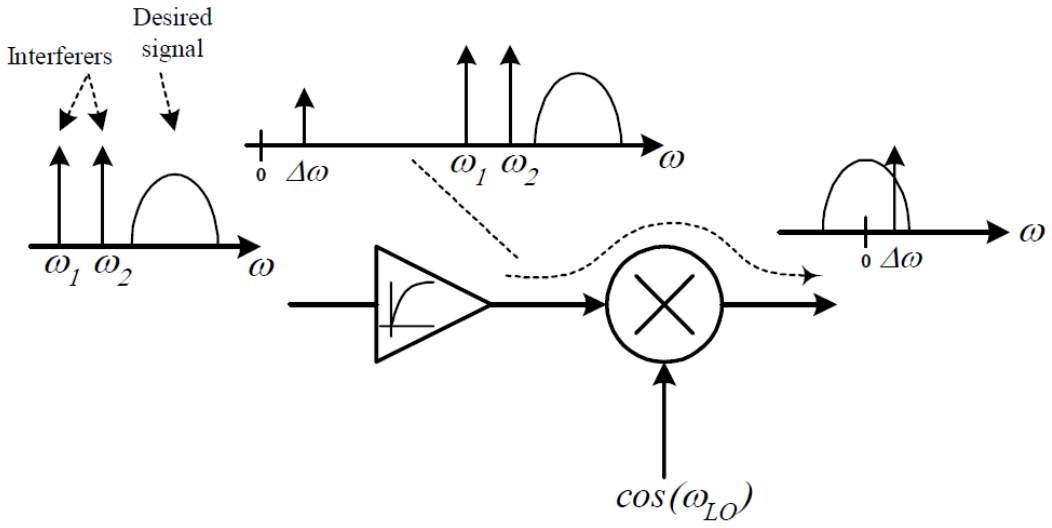

Figure 2–2: Effect of even order distortion

2.2.4 I / Q Mismatch

Phase and magnitude mismatches between I and Q branches corrupt the Down-converted signal. However, in the case of Bluetooth, since the modulation format in binary GFSK, I/Q mismatch is not a serious problem. Therefore, I/Q mismatch is much.

2.3 Low-IF Receiver Architecture

IF receivers have been in use for a long time, and their principle of operation is very well known. In an IF receiver, the wanted signal is down-converted to from its carrier to the IF by multiplying it with a single sinusoidal signal as shown in Fig.2.3. The main disadvantage here is that apart from the wanted signal, an unwanted signal at a frequency called the image frequency (which is 2 f IF away from the wanted frequency) is down-

converted to the same IF frequency. To avoid corrupting the wanted signal, the image signal must be suppressed before down-conversion by means of a band-pass RF filter. The Q of such filter is proportional to RF IF f_{RF}/f_{IF} . High Q external SAW or ceramic filters (typically 50 or more) are used for this purpose. Such filters are bulky and require impedance matching at input and output, which usually raises the power consumption that is needed in order to drive this low impedance. Furthermore, the IF frequency cannot be made arbitrarily small due to the limited Q of the external filter, and hence, raising the power consumption of the circuits operating at the IF frequency. The image frequency problem can be mathematically explained as follows. When RF signal is multiplied by a single sinusoidal signal $\cos(\omega_{LO})$, it is equivalently multiplied by two exponentials $e^{-j\omega_{LO}}$ and $e^{j\omega_{LO}}$. Considering the signal diagram in Fig. 2.4, the spectrum of the down-converted signal is constructed by shifting the RF spectrum to the left and to the right by ω_{LO} and add the two shifted replicas. The result is two overlapping spectra, of the signal and the image, at the IF frequency.

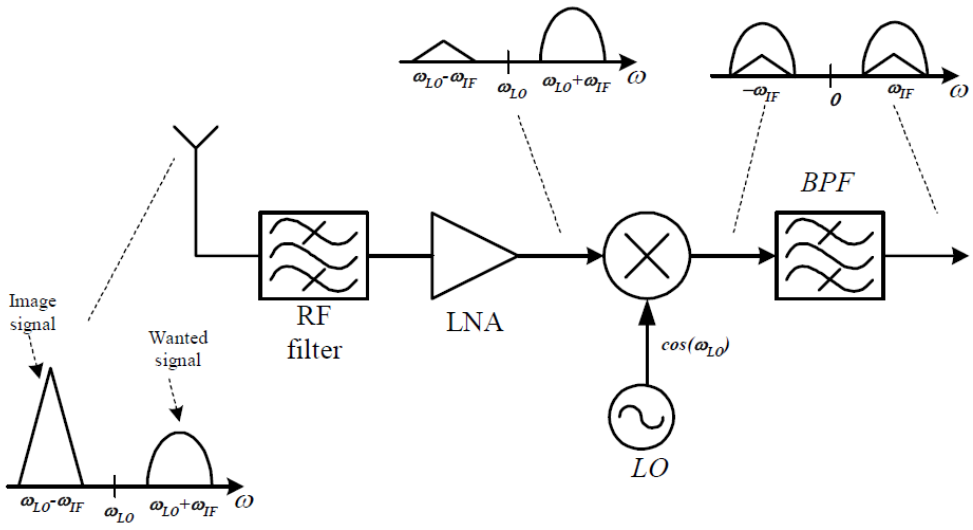

Figure 2–3:IF receiver architecture

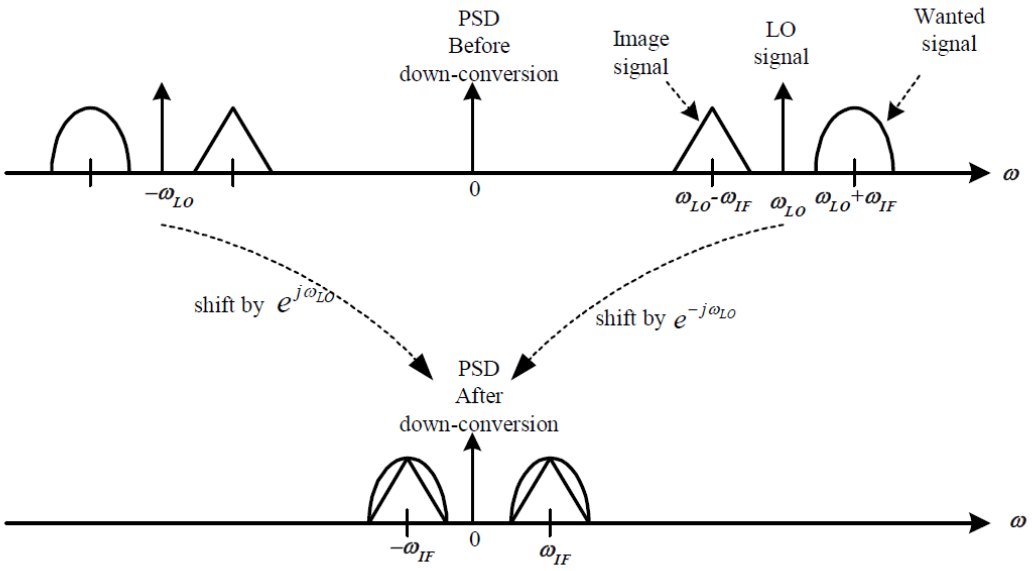

Figure 2–4: Down-conversion with a single sinusoidal signal

An obvious solution to avoid this problem is to multiply the RF signal by only exponentials, say $e^{-j\omega_{LO}}$, which means that the down-converted signal is simply a single shifted replica of the RF signal and therefore, no overlapping of signals spectra. The only problem now is that the signal $e^{-j\omega_{LO}}$ is a complex signal with real part ($\cos(\omega_{LO})$) and imaginary part ($\sin(\omega_{LO})$). To implement this complex multiplication using real components, two signal branches I and Q must be constructed. In the I (in-phase or real) branch, the RF signal is multiplied by $\cos(\omega_{LO})$, while in the Q branch (quadrature-phase or imaginary), the RF signal is multiplied by $\sin(\omega_{LO})$. Fig. 2.5 shows the signal diagram of the complex down-conversion operation. It is important to note that in each branch, the down-converted signal contains both the wanted and the image signals at the same IF frequency. However, the complex signal $I_o + j\ Q_o$ has the wanted signal at IF ω and the image signal at $-\omega_{IF}$. The image signal can then be rejected by means of a complex filter, which will be described in detail in the following section. The same filter is also used for channel selectivity. Therefore, the Q of such filter is proportional to $^{-\omega_{IF}}/_{BW}$ (BW is the channel bandwidth) which is small for low IF frequencies. This is the basic idea behind low-IF receiver architecture.

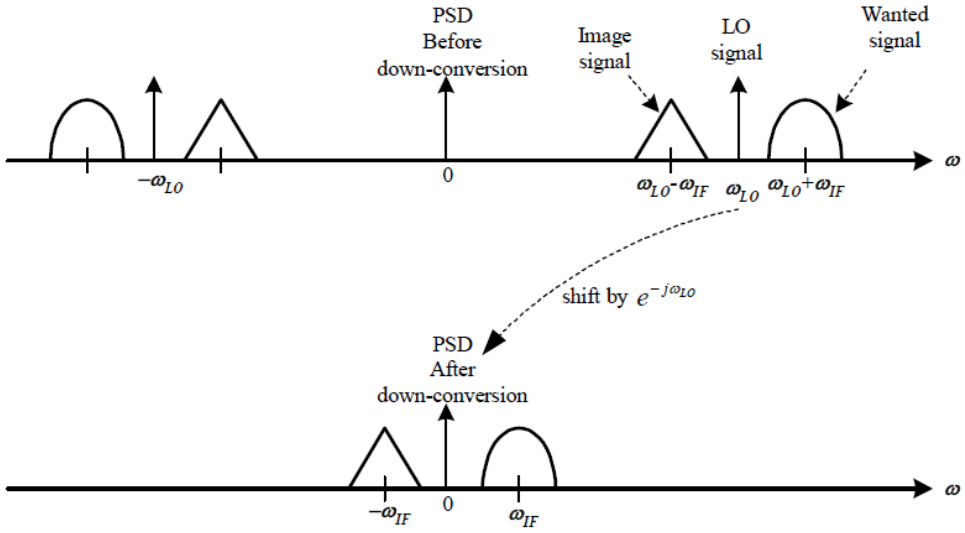

Figure 2–5: Down-conversion with a single exponential

Fig. 2.6 shows the basic low-IF receiver architecture. Although low-IF receiver avoids the problems that exist in DCR and high-IF architectures, it has some design issues. Namely, its image rejection capability is limited by matching between I and Q branches and between the quadrature LO outputs. The effect of these mismatches is studied in the following section.

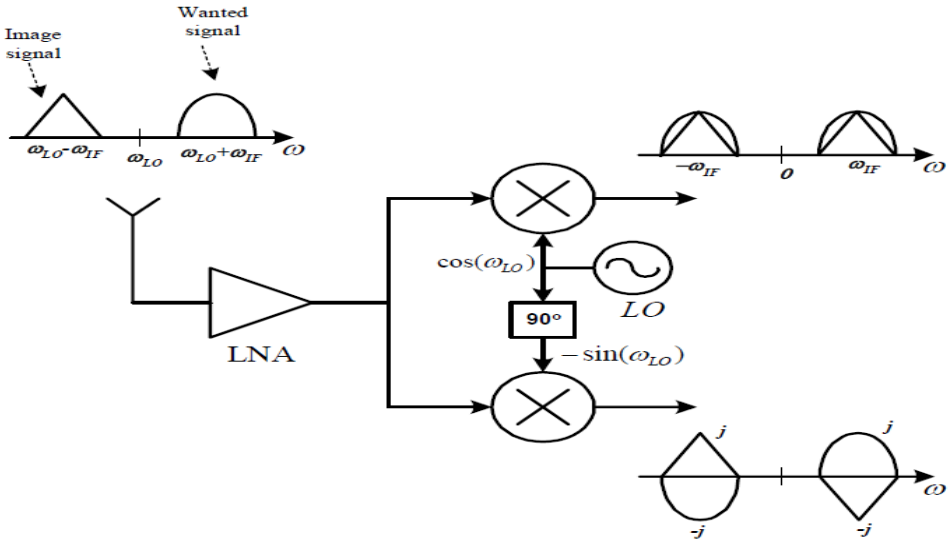

Figure 2–6: Basic low-IF receiver architecture

2.4 BLE Receiver Architecture

In a baseband Bluetooth signal, 99% of the signal power is contained within the DC to 430kHz bandwidth. Therefore, if direct-conversion architecture is used, the flicker noise and DC offset might significantly degrade the signal-to-noise ratio (SNR). Hence, a low-IF architecture seems to be a suitable architecture in Bluetooth, especially when considering the relaxed image rejection requirement in the Bluetooth standard [3]. To relax the image rejection requirement and reduce the folded-back interference level, a very low-IF is preferable, i.e. half of the channel bandwidth. However, such a very low- IF requires a sharp cut off from the channel selection filter to reject the DC offset and flicker noise. On the other hand, a higher IF improves the demodulator performance, but the required selectivity of the channel selection filter will increase, and power consumption will be higher. As a good compromise, an IF of equal the channel bandwidth is chosen, i.e. 2 MHz for the two-mega mode and 1MHz for the one-mega mode. For a low-IF Bluetooth receiver, the image signal is an in-band Bluetooth modulated adjacent channel interference, which becomes co-channel interference after frequency down-conversion.

Nowadays, current-mode receiver are preferred for the following reasons: (1) Low power consumption at higher frequencies, (2) Less affected by voltage fluctuations as the voltage swing is low, (3) High speed, (4) Voltage suffers from attenuation for long distance but, Current do not, (5) Current-mode RF receivers have simpler architecture due to lower supply voltage, and better linearity.

For voltage mode circuits, impedance of internal nodes is usually large so, the signal information could be carried with the time varying voltage signal. Therefore, large voltage swing is required to keep signal information that’s why voltage mode circuit is not preferred for low voltage supply. In contrast with current-mode circuit, low-impedance node and signal information is carried by the time varying current signal so, voltage at each node could be small.

2.5 References

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[3] Specifications of the Bluetooth System, Version 1.0 B, Overland Park, KS, Bluetooth SIG, 1999

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3 Chapter 3: Low Noise Amplifier

3.1 Introduction

Low Noise Amplifier (LNA) is the most critical part of a receiver front end, in terms of the receiver performance. LNA design represents one of the biggest challenges facing the RF transceivers designers, where they have to choose the best topology that meets the required specifications. The main function of LNA is to amplify a very low power signal without significantly degrading the signal to noise ratio (SNR). The design of LNA is concerned by many parameters that determine the choice of suitable topology.

3.2 Design parameters

The key factors of LNA, such as noise figure, gain, stability, and linearity are introduced to understand what compromises are needed to achieve the goal. It is essential for the BLE front-end circuit to be equipped with high noise immunity, low-power consumption, and reasonable gain. The details of the LNA design factors will be elaborated in the following subsections.

3.2.1 Noise

The performance of RF systems is limited by noise. Without noise, an RF receiver would be able to detect arbitrarily small inputs, allowing communication across arbitrarily long distances.

3.2.1.1 Main Noise Sources

In order to analyze the noise performance of circuits, we wish to model the noise of their constituent elements by familiar components such as voltage and current sources. Such a representation allows the use of standard circuit analysis techniques.

Thermal Noise of Resistor the ambient thermal energy leads to random agitation of charge carriers in resistors and hence noise. The noise can be modeled by a series

voltage source with a PSD given by Eq. (3.1) [Thevenin equivalent, Fig. 3.1(a)] or a parallel current source with a PSD given by Eq. (3.2) [Norton equivalent, Fig. 3.1(b)]. The choice of the model sometimes simplifies the analysis.

$$V_n^2 = 4\,kTR_1 \tag{3.1}$$

$$I_n^2 = V_n^2/R_1^2 = 4\,kT/R_1 \tag{3.2}$$

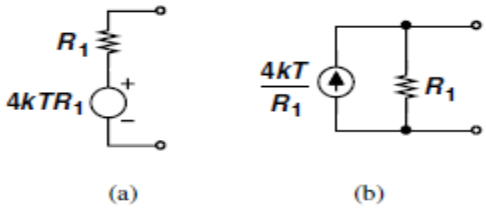


Figure 3–1: (a) Thevenin and (b) Norton models of resistor thermal noise

Noise in MOSFETs the thermal noise of MOS transistors operating in the saturation region is approximated by a current source tied between the source and drain terminals [Fig. 3.2(a)]:

$$I_n^2 = 4\,kT\gamma g_m \tag{3.3}$$

Where γ is the "excess noise coefficient", the value of γ is 2/3 for long-channel transistors and may rise to 2 for short-channel devices [1]. The noise can be also modeled as a voltage at the input gate of the transistor as shown in Fig. 3.2(b), where the current is divided by g_m^2. The noise voltage is given by

$$V_n^2 = 4\,kT\gamma/g_m \tag{3.4}$$

Another type of noise in MOSFETs is the flicker noise. The origins of flicker noise are varied, but it is caused mainly by traps associated with contamination and crystal defects. These traps capture and release carriers in a random fashion and the time constants associated with the process give rise to a noise signal with energy concentrated at low frequencies [2].

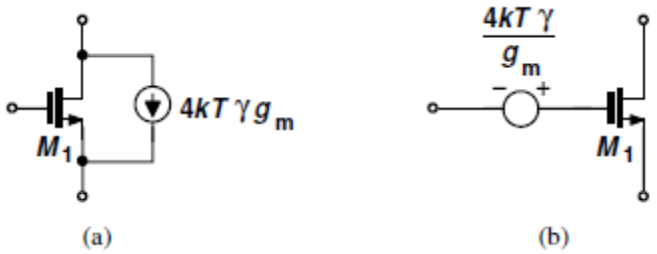


Figure 3–2: Thermal channel noise of a MOSFET modeled as a (a) current source, (b) voltage source.

3.2.1.2 Noise Figure

The noise figure is considered a measurement of the noise performance of a circuit. It is the ratio between the input SNR & the output SNR of the LNA. From Eq. (3.5), it is shown that by increasing the gain of the circuit, the NF is decreased. This is done by increasing g_m, but this also increases the current, which in turn causes the power dissipation of the circuit to go up.

$$NF = 1 + \frac{v_{n,out}^2}{A_v^2 \cdot v_{n,Rs}^2} \tag{3.5}$$

3.2.2 Gain

The gain of LNA should be large enough to minimize the noise contribution of the subsequent stages. Also, a compromise between noise figure and linearity of the receiver should be taken into consideration as a higher gain make the nonlinearity of subsequent stages more pronounced.

3.2.3 Input Return Loss

The interface between the antenna and the LNA entails an interesting issue that divides analog designers and microwave engineers. Considering the LNA as a voltage amplifier, we may expect that its input impedance must ideally be infinite. From the signal power point of view, we may realize conjugate matching between the antenna and the LNA. From the noise point of view, we may precede the LNA with a matching network to get minimum NF by obtaining a voltage gain from this matching network which is given by [3]

$$\frac{V_{out}^2}{V_{in}^2} = \sqrt{\frac{R_{lna}}{R_s}} \tag{3.6}$$

Where, Rlna is the real input resistance of LNA and Rs is the source resistance.

The quality of the input match is expressed by the input "return loss," defined as the reflected power divided by the incident power. For a source impedance of RS, the return loss is given by

$$S_{11} = \left|\frac{Z_{in} - R_s}{Z_{in} + R_s}\right|^2 \tag{3.7}$$

Where Zin denotes the input impedance. An input return loss of -10 dB signifies that one-tenth of the power is reflected—a typically acceptable value.

3.2.4 Stability

LNA must remain stable for all source impedances at all frequencies. If the LNA begins to oscillate at any frequency, it becomes highly nonlinear and its gain is very heavily compressed [1]. A parameter often used to characterize the stability of circuits is the "Stern stability factor," defined as

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \tag{3.8}$$

Where, $\Delta = S_{11}S_{22} - S_{12}S_{21}$. The system is stable for $K > 1$.

3.2.5 Linearity

Linearity of LNAs is usually judged by two main tests: a single-tone test to determine its 1 dB compression point, and a two-tone test to determine its third-order intercept point. Gain compression occurs when the amplitude of the input signal becomes very large, leading to a decrease in the gain. Therefore, $P1dB$ is very important to define the maximum input power to the LNA before which the gain is compressed. Also the LNA should have an acceptable $IIP3$.

3.2.6 Power Consumption

The LNA typically exhibits a direct trade-off among noise, linearity, and power dissipation. Nonetheless, in most receiver designs, the LNA consumes only a small fraction of the overall power. In other words, the circuit's noise figure generally proves much more critical than its power dissipation.

3.3 LNA Topologies

LNA circuits in CMOS technology are designed as Common Source (CS) or Common Gate (CG) stages. Choosing proper circuit depends on the specific application for which the LNA is designed. In this section, Famous LNA topologies will be discussed based on the previous design parameters.

3.3.1 Common Gate Stage

The low input impedance of the common-gate (CG) stage makes it attractive for LNA design. We consider only a CG circuit with inductive loading [Fig. 3.3]. Here, L1 resonates with the total capacitance at the output node (including the input capacitance of the following stage), and R1 represents the loss of L1. If channel-length modulation and body effect are neglected, Rin = 1/gm. Thus, the dimensions and bias current of M1 are chosen so as to yield gm = 1/RS. The voltage gain from input node to the output node at the output resonance frequency is then equal to

$$\frac{V_{out}}{V_{in}} = \frac{R_1}{2\,R_s} \tag{3.9}$$

However, the main drawback is the relatively high NF given by Eq. (3.10)

$$NF = 1 + \gamma + 4\,\frac{R_S}{R_1} \tag{3.10}$$

Even if 4RS/R1 << 1+ ɣ the NF still reaches 3 dB . The main trade-off here is between NF and Input matching where, a higher gm yields a lower NF but also a lower input resistance.

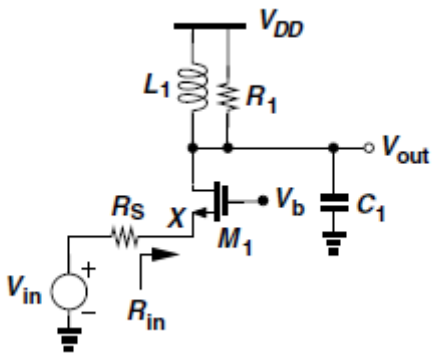


Figure 3–3: Common Gate LNA Stage

3.3.2 Common Source Stage with inductive degeneration

Common source (CS) topology, shown in Fig. 3.4, is the most widely used in LNA designs. The secret behind their popularity is simplicity and that they permit simultaneous noise and input impedance matching, making it possible to achieve noise figure values closely approaching the $NFmin$ of the transistor itself [4].

The input impedance of the common source stage is given by the following equation

$$\frac{V_x}{I_x} = \frac{1}{SC_{GS1}} + SL_1 + \frac{g_m L_1}{C_{GS!}} \tag{3.11}$$

Therefore, input impedance matching can be satisfied by equating the real part of Eq. (3.11) to the required matching impedance and equating the reactive part to zero. The noise figure can be calculated as follow

$$NF = 1 + \frac{R_g}{R_s} + g_m R_s \left(\frac{\omega}{\omega_T}\right)^2 \tag{3.12}$$

The NF is minimized by decreasing gate resistance, and using a high ω_T device.

The trans-conductance gain of CS stage is given by

$$\frac{I_{out}}{V_{in}} = \frac{1}{\omega_o\left(L_1 + \frac{R_S C_{GS1}}{g_m}\right)} \tag{3.13}$$

Which could be approximated to g_m so, increasing g_m leading to an increase in trans-conductance gain, power consumption, and noise figure. An optimum point is chosen to get a compromise between the mentioned parameters.

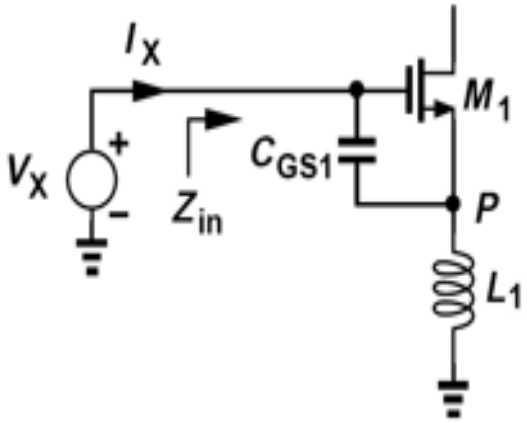


Figure 3–4: Inductive-degenerated CS LNA Stage

3.3.3 Common Source (Resistive Feedback)

Another topology here is the common source with resistive feedback. The resistive feedback here is put to achieve an input impedance suitable for matching as the input impedance of the common source connecting the input directly through the gate is very large. So, this input resistance value can be tuned to obtain a value near 50 ohms (to achieve matching).

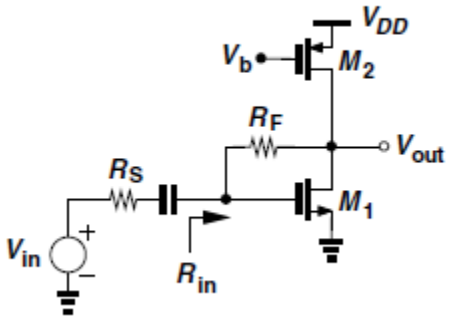


Figure 3–5: CS resistive feedback

Again, nothing is free here. This addition of this resistor may ease the matching part but this will come over the noise figure because now we have another element that contributes in the thermal noise.

After the analysis, the noise figure of the circuit can be shown as in Fig 3.6

$$NF \approx 1 + \frac{R_S}{R_F} + \gamma + g_{m2} R_S \gamma \tag{3.14}$$

Which can be noticed that a full term is added here due to the existence of the feedback resistor and this term would equal to zero if the feedback resistor is equal to infinity (didn't exist).

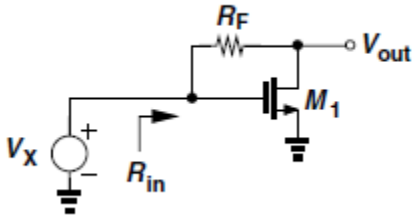


Figure 3–6: Noise Figure analysis for CS resistive feedback

3.3.4 Summery for LNA Topologies

	CS (Inductive load)	**CS (Resistive Feedback)**	**CG**
Pros.	Low noise figure	-	High bandwidth
Cons.	Low Bandwidth which is used for Narrow-Band applications	High NF	Worst in matching Slightly high noise figure

Table3.1Pros. and Cons. Of Cascode CS (IL), CS (RF) and CG

3.4 Design of LNA

The physical schematic design will be presented and simulated in the Cadence ADE with TSMC 65 nm process Technology. The entire LNA circuit will be broken into two stages. The first stage consists of: Topology, source degeneration, input matching network, biasing circuit, and parallel LC tank as a load. The second stage is implemented using inverter-based amplifier. The key performance factors, such as NF, gain, P1dB, IIP3 and, S11 will be considered simultaneously to ensure that the design satisfies the criteria of the BLE front-end receiver.

3.4.1 Topology Selection

It is clear that in modern receivers, an LNA with minimum NF, high gain and, high linearity is required. The proposed architecture is based on the required specifications.

3.4.1.1 LNA 1st Stage

A common source with inductive degeneration is used as the input stage to minimize the NF, and using a cascade stage is used to boost the gain of the LNA and to achieve high isolation between the input and the output. Fig. 3.7 shows the LNA 1st stage schematic. Gain of the matching network given by Eq. (3.6) improves the noise figure however, this gain can degrade IIP3 of the LNA. Biasing circuit is followed by a Low pass section to prevent M3 from contributing in NF. A parallel LC tank is added to get a higher rejection out of the band of interest.

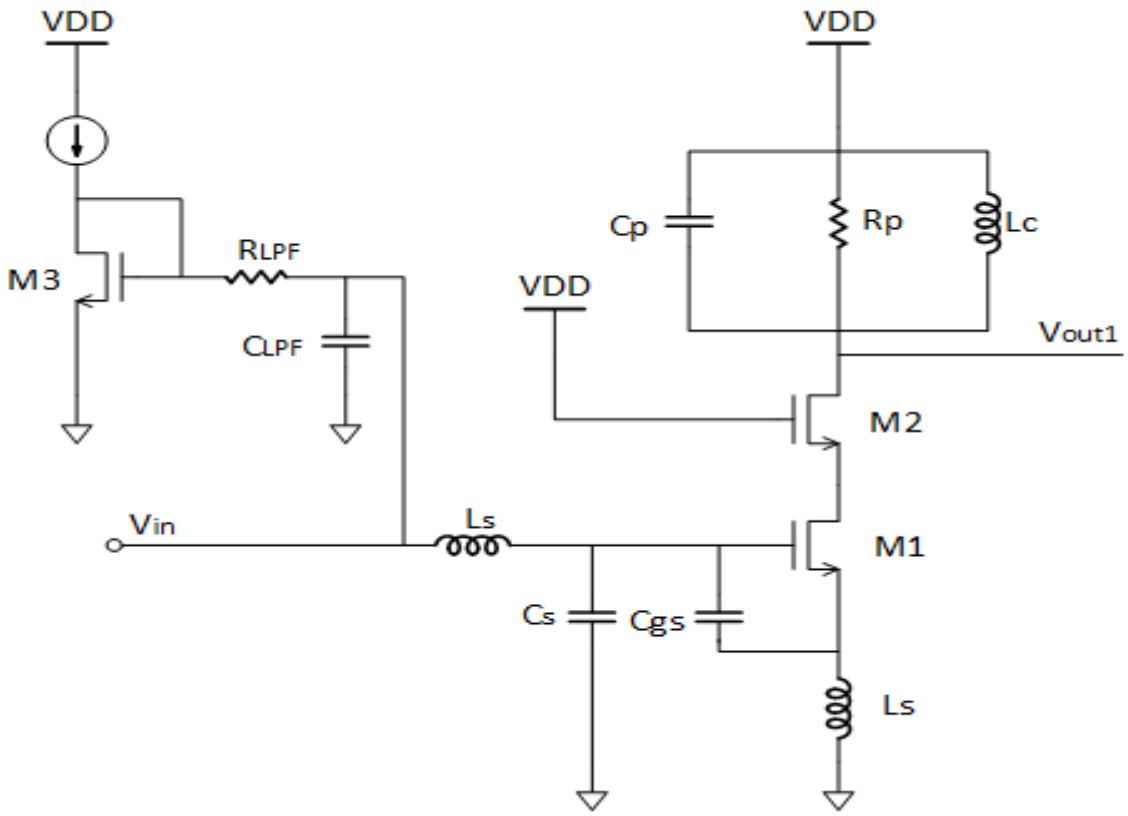


Figure 3–7: Schematic of inductively- degenerated CS preceded by L-matching section

3.4.1.2 LNA 2nd Stage

A stacked inverter-based amplifier, shown in Fig. 3.8, is used as the second stage for the proposed LNA to double gm for the same current. The achieved amplifier, based on an inverter, uses stacking to achieve high output resistance [5] [6]. The output common-mode, shown in Fig. 3.8, is set at $V_{DD}/2$ using Common mode feedback circuit (CMFB). The output node voltage is sensed through a resistor and compared with the common-mode reference voltage, and the output of the CMFB circuit is returned to bias the PMOS such that keeping the output common-mode at mid supply [7].

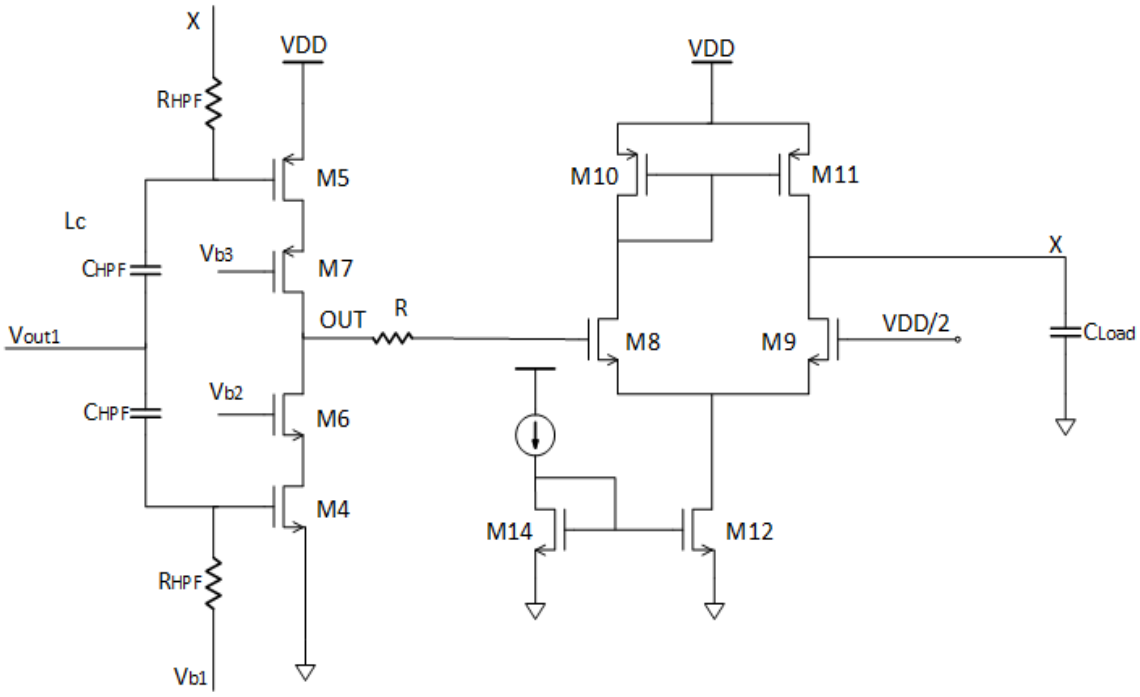


Figure 3–8: Inverter-based amplifier followed by a CMFB circuit

3.4.2 Gain Switching

Since we deal with multiple gains, we have to seek for the proper method to apply the gain switching technique. Mainly there are three techniques, we will discuss each one and choose the most suitable in our case.

Starting with the load switching, as shown in Fig. 3.9, its shown that it replaces the load resistor with the PMOS triode resistor parallel to the load. But there exists an issue here, as the triode resistor isn't linear enough as a resistor so it degrades the linearity.

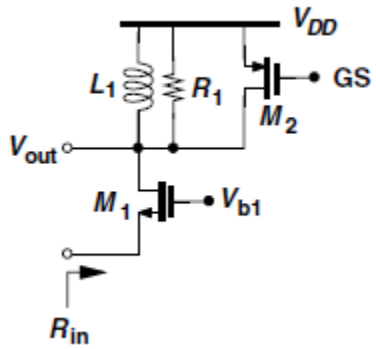


Figure 3–9: Load switching Method

Another method is by gm switching, as shown in Fig. 3.10, its shown that it divides the g_m of the main input MOSFET into number of MOSFETs so it can digitally choose one of them or add them all or whatever was its choice of using them. This doesn't affect the linearity as the previous one did but it changes the return loss with each gain step. Which may make the matching a little hard to achieve.

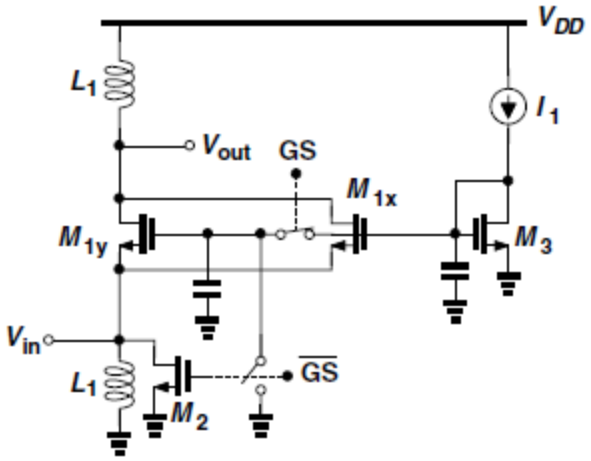


Figure 3–10: gm Switching

Finally, the Parallel to Cascode method, as shown in Fig. 3.11, which mainly focuses on dividing the current with the ratio of the gain. This method is considered the most suitable of them as it won't affect negatively on the linearity or change the input impedance much as the g_m switching did.

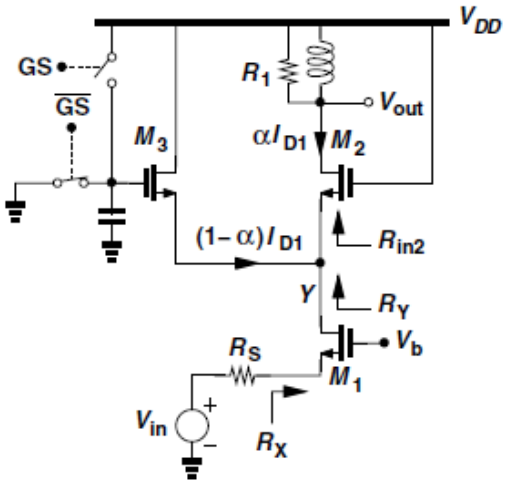


Figure 3–11: Parallel to cascode method

The chosen topology, as shown in Fig 3.12, should be the parallel to cascode method to keep the drain voltage of the main device almost constant. This approach keep current and g_m constant which maintain the matching as before.

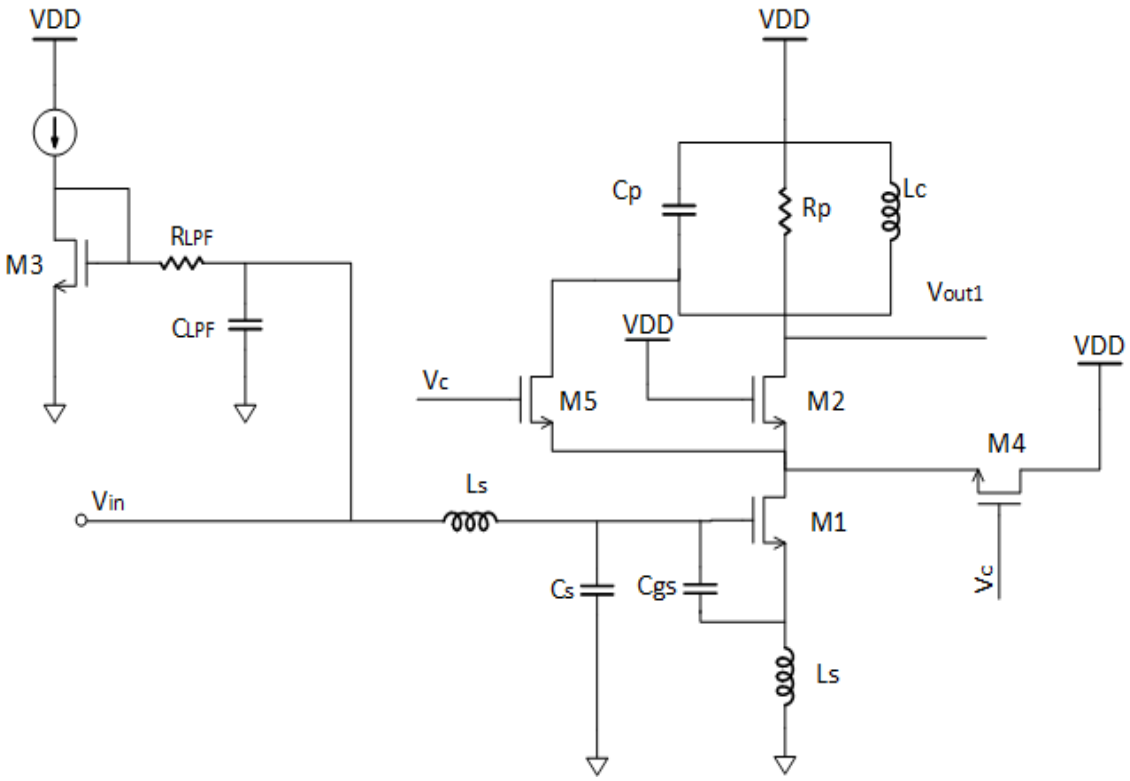


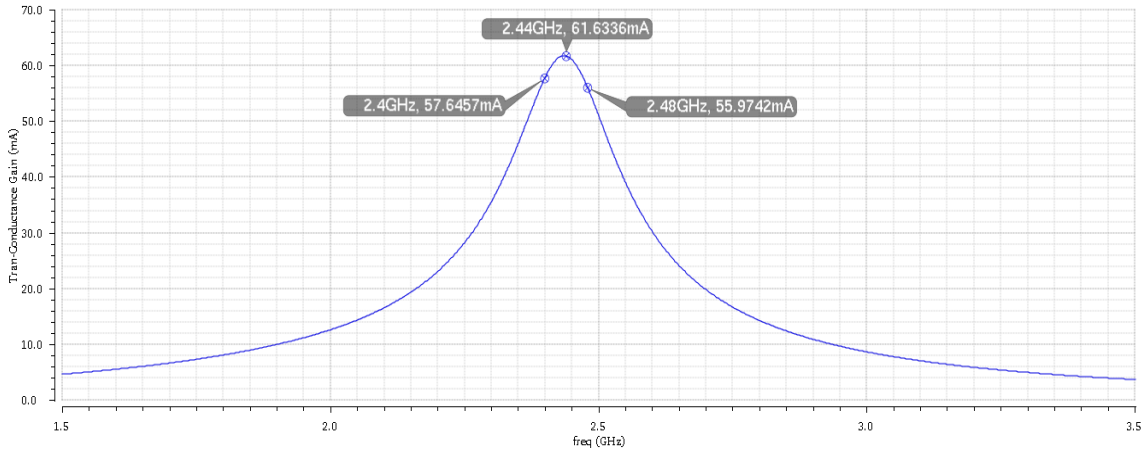
Figure 3–12: LNA 1st Stage with the added gain switching devices

3.4.3 Typical Simulation Results of the proposed LNA architecture

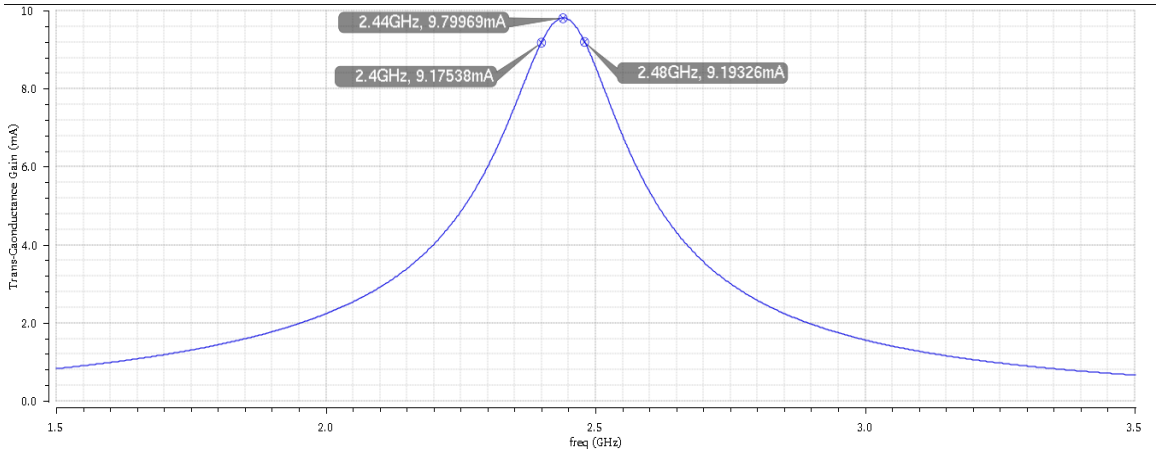
The proposed LNA architecture had been simulated and debugged to reach the required specifications. The design was based on $^{g_m}/_{I_d}$ curves and was optimized to get the optimum point among the required specifications.

3.4.3.1 Trans-conductance Gain

The AC analysis is performed to observe the AC gain of the LNA. In current mode signaling receiver, information is represented as current signal so, the desired gain is the trans-conductance gain. As shown in Fig 3.13, the achieved gain for 1st and 2nd mode are 61.6 mA/V and 9.7 mA/V respectively.



(a) First trans-conductance gain Mode of the whole LNA architecture

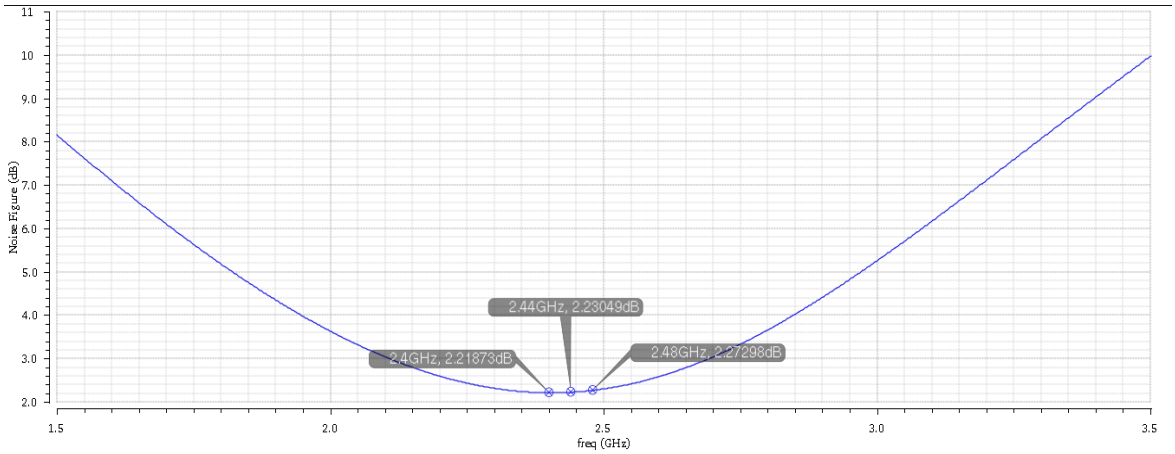


(b) Second trans-conductance gain Mode of the whole LNA architecture

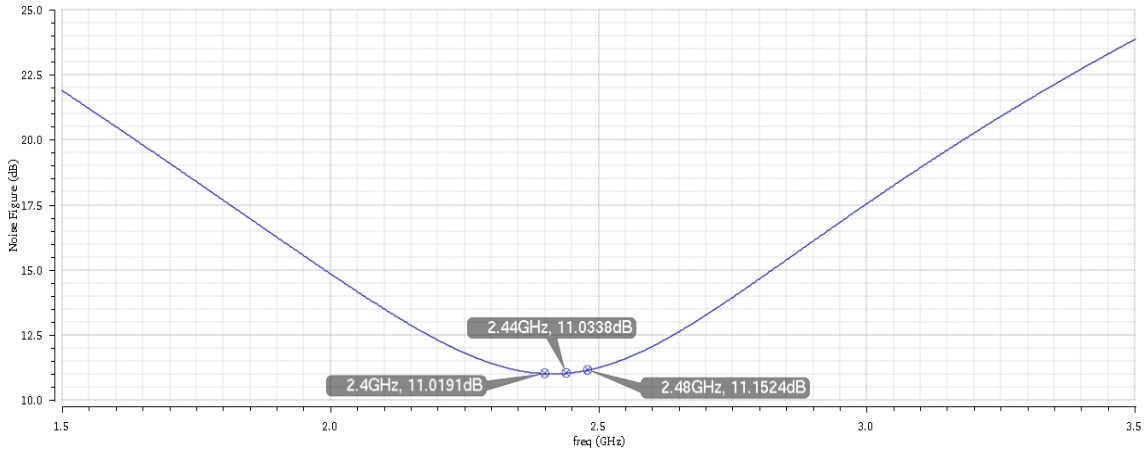
Figure 3–13: First and second trans-conductance gain Mode of the whole LNA architecture

3.4.3.2 Noise Figure

Signal to noise ratio is desired to be enhanced to improve the receiver sensitivity. The achieved noise figure for 1st and 2nd mode, as shown in Fig 3.14, are below 2.5 dB and 11.5 dB across the entire band respectively.



(a) First mode noise figure of the whole LNA architecture

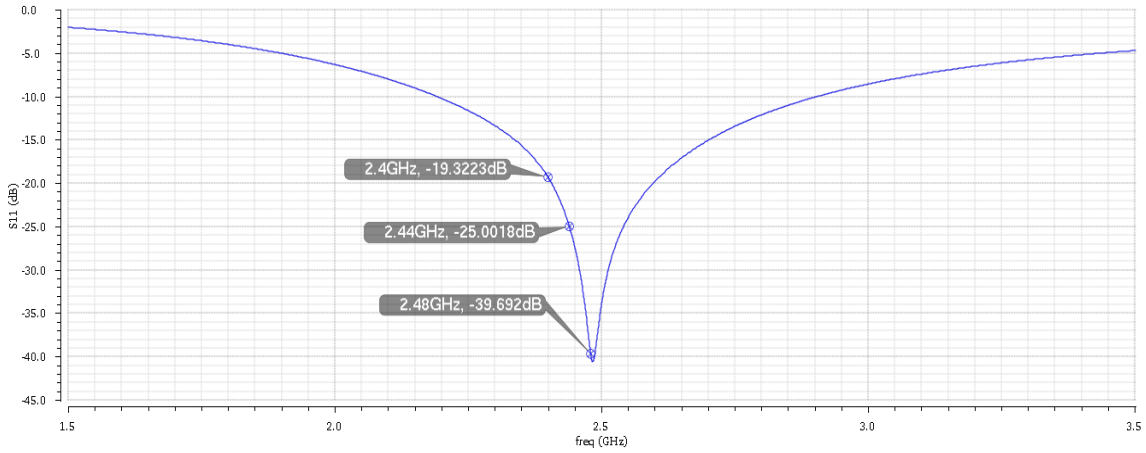


(b) Second mode noise figure of the whole LNA architecture

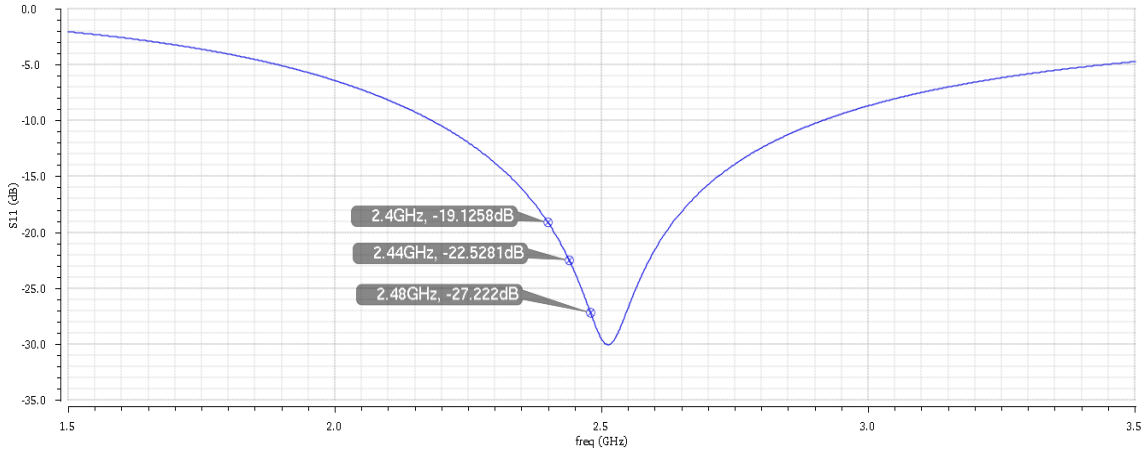
Figure 3–14: First and Second mode noise figure of the whole LNA architecture

3.4.3.3 Return Loss

The return loss factor or S11, as shown in Fig 3.15, describe how good the matching is and is desired to be below -12 dB across the band of interest for the two modes.



(a) First mode Return Loss factor of the whole LNA architecture

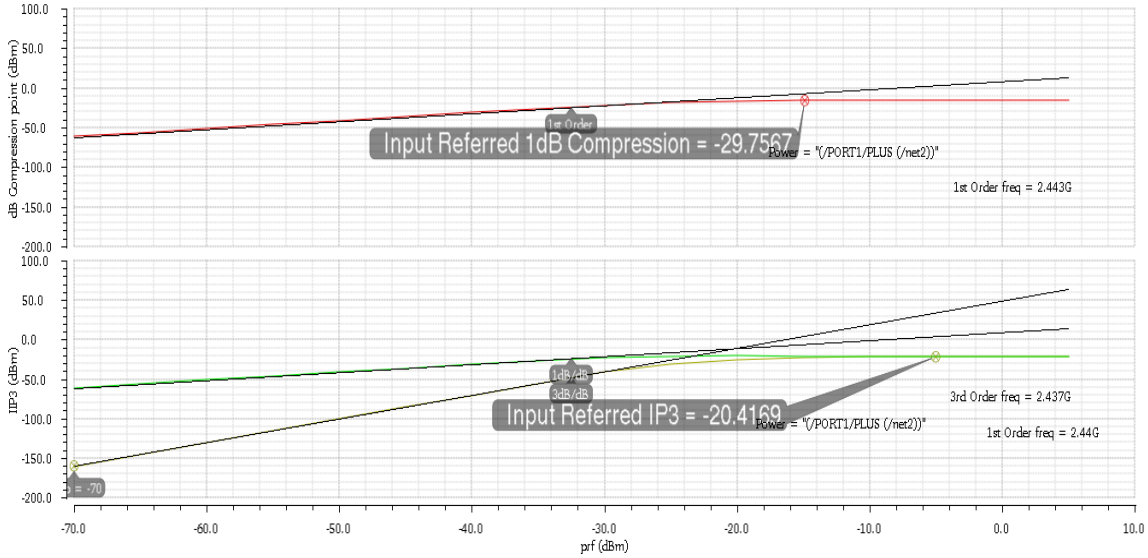


(b) Second mode Return Loss factor of the whole LNA architecture

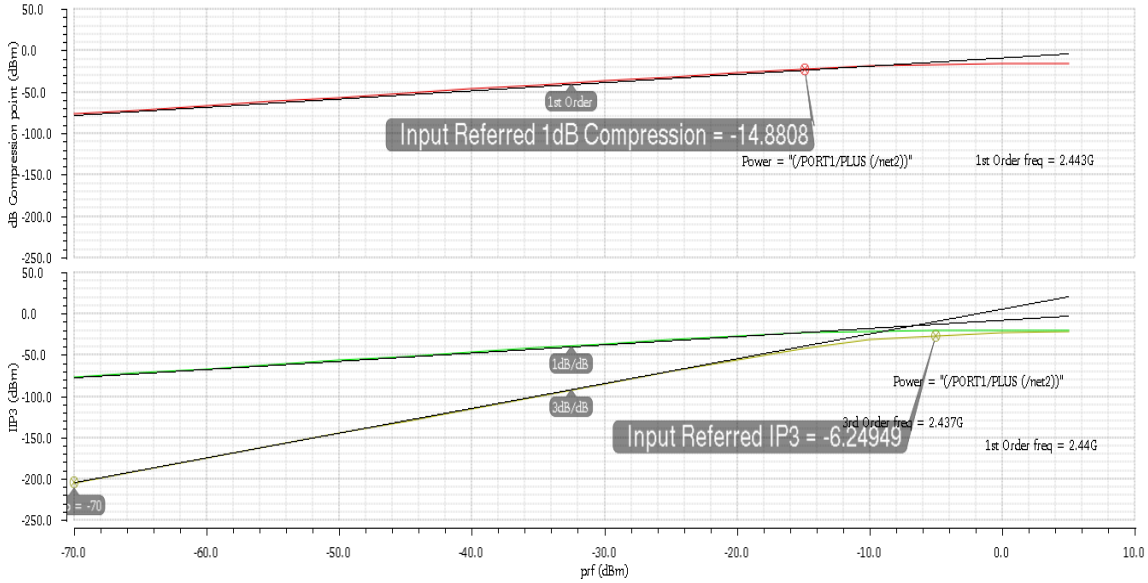
Figure 3–15: First and Second mode return loss factor of the whole LNA architecture

3.4.3.4 Third-Order Intercept Point & 1-dB Compression Point

The 1-dB compression point is found by drawing the input power against the output power, then comparing the resulting curve with the linear case using the PSS analysis. The achieved 1-dB compression point and IIP3 for first mode the two stages of LNA, as shown in Fig 3.16(a), are -29.7 dBm and -20.4 dBm respectively which hardly fit the required. The linearity, as shown in Fig 3.16(b), has been improved for the second mode due to the lower gain.



(a) First mode linearity factors of the whole LNA architecture



(b) Second mode linearity factors of the whole LNA architecture

Figure 3–16: First and Second mode linearity factors of the whole LNA architecture

3.4.3.5 Output Impedance

The achieved Rout and Cout at the output node, as shown in Fig 3.17, are 4.7 KΩ and 24 fF respectively at the mid band.

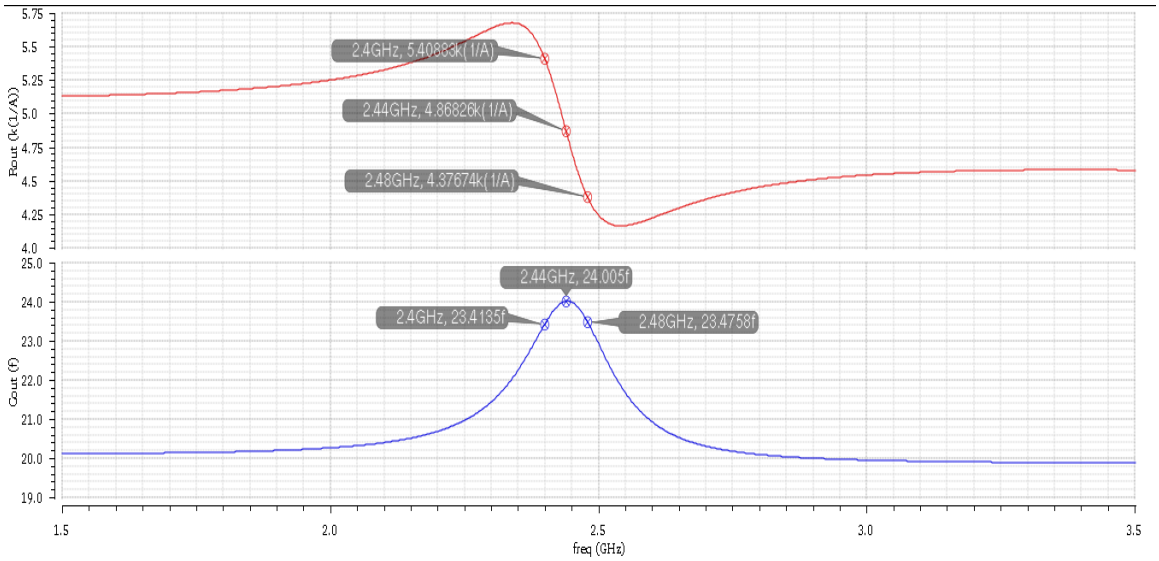


Figure 3–17: Rout and Cout of the whole LNA architecture

3.4.3.6 Stability analysis of CMFB circuit

The stability of CMFB loop had been tested, as shown in Fig 3.18, to have phase margin and gain margin of 74.8 degree and 22.5 dB respectively.

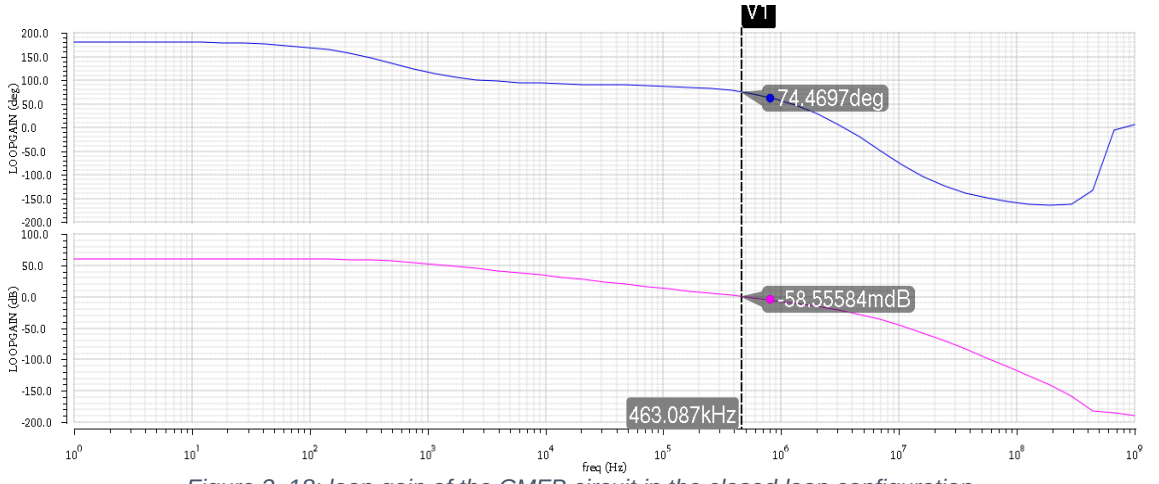


Figure 3–18: loop gain of the CMFB circuit in the closed loop configuration

3.4.4 Corner Simulation Results of the proposed LNA architecture

Corner simulations are consider to model process variations. The Considered cases in the following simulation is as shown in Table 3.1.

To improve the performance across corners, a capacitor bank, shown in Fig 3.19, had been implemented with a compromise between the following trades-off: (1) The ratio between ON capacitance to OFF capacitance is desired to be maximized. (2) The ON resistance of the switch should be as small as possible to keep the quality factor of the capacitor array being large.

Temperature	{-40°C,125°C}
Supply	{0.95,1.05}
Transistors	{SS,TT,FF,FS,SF}
Inductor	{SS_rfind, TT_rfind, FF_rfind}
Capacitor	{SS_rfmom, TT_rfmom , FF_rfmom }

Table 3.2 Used Combined Sets

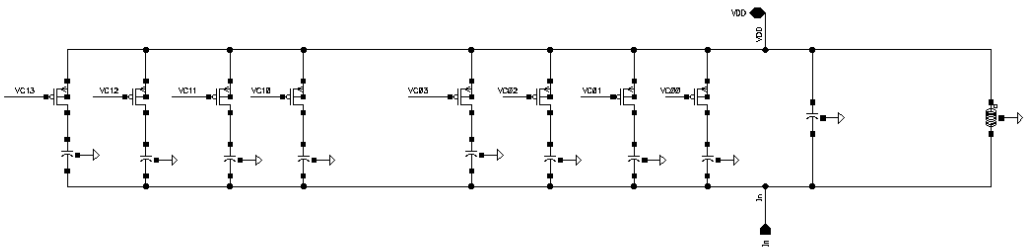


Figure 3–19: Capacitor array as a part of Parallel LC Tank

3.4.4.1 Trans-conductance Gain

A capacitor Bank had been implemented to re-adjust the resonance of the gain back to the original resonance frequency at the corners will change due to the effect of the temperature, inductor corner cases, and capacitor corner cases. As shown in Fig 2.19, the peak of the gain is shifted away from the desired band leading to a lower gain in the band on interest so, the capacitor array solves this issue, as shown in Fig 3.20.

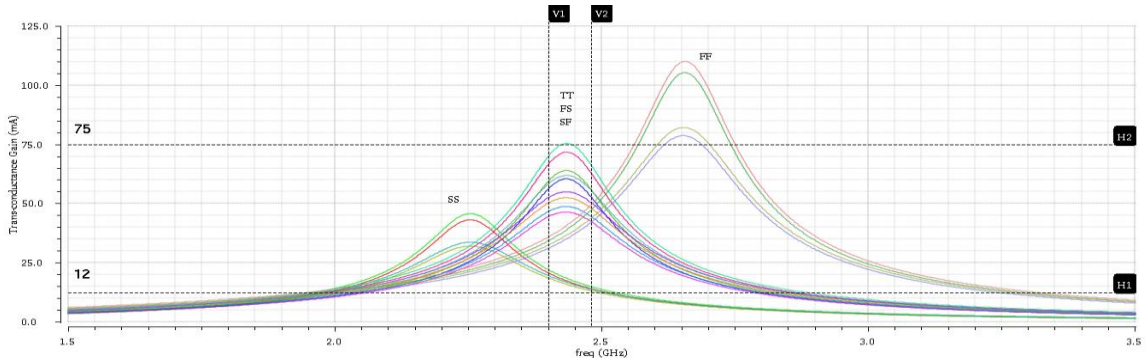
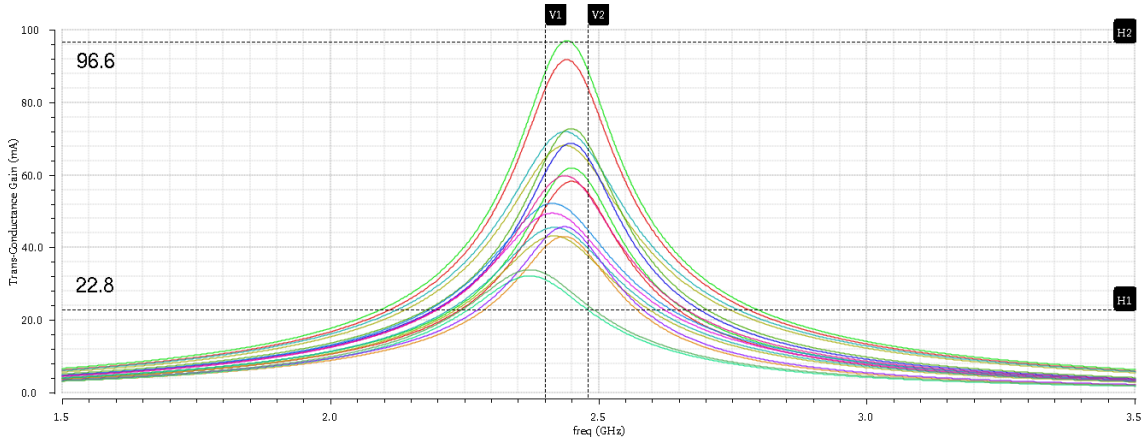
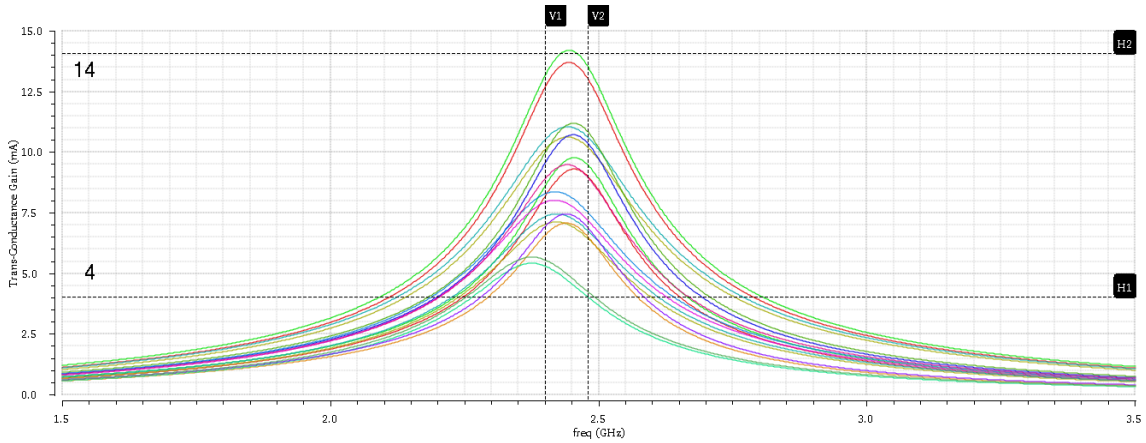


Figure 3–20: Gain across corner without Cap array



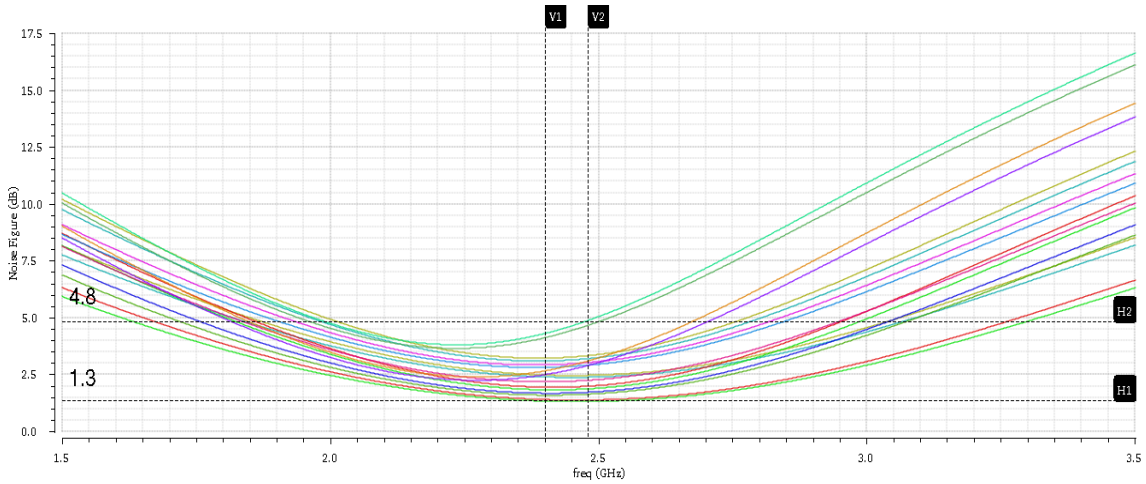
(a) First Mode Gain



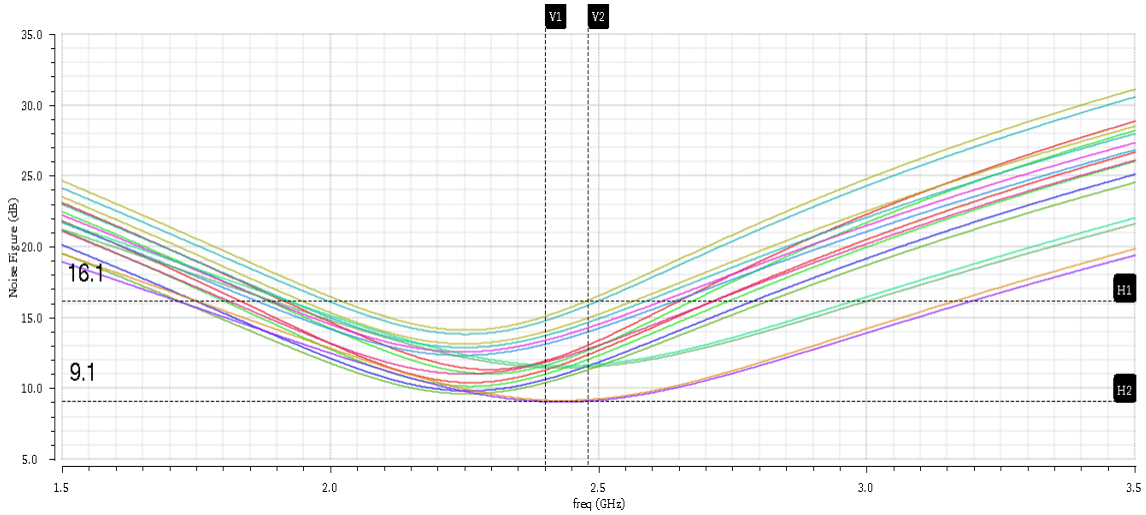
(b) Second Mode Gain

Figure 3–21: First and Second mode gain

3.4.4.2 Noise Figure



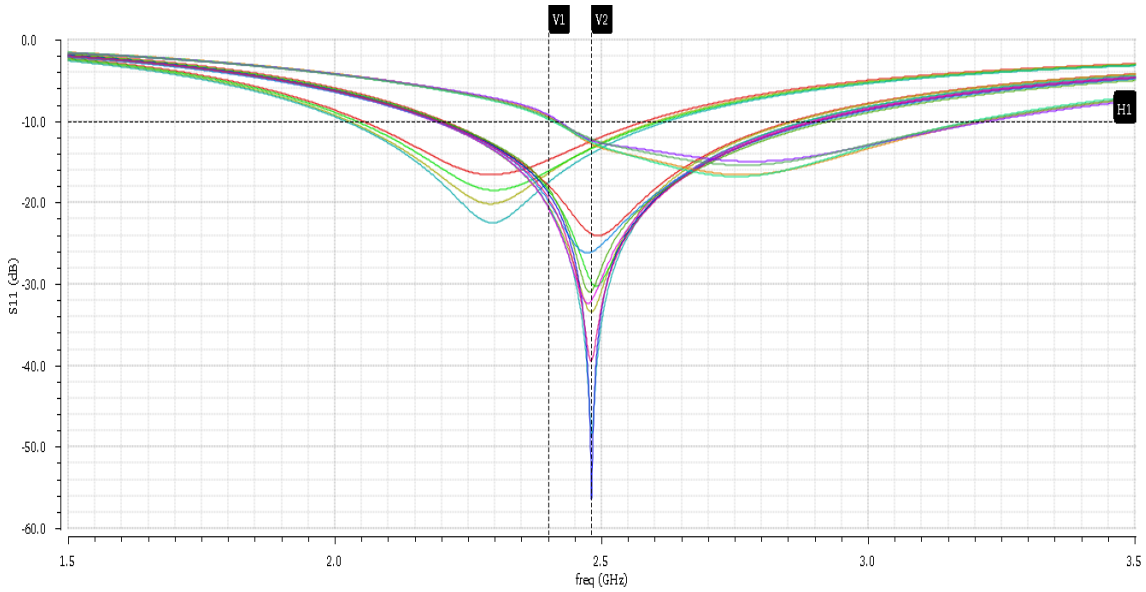
(a) First Mode Noise Figure



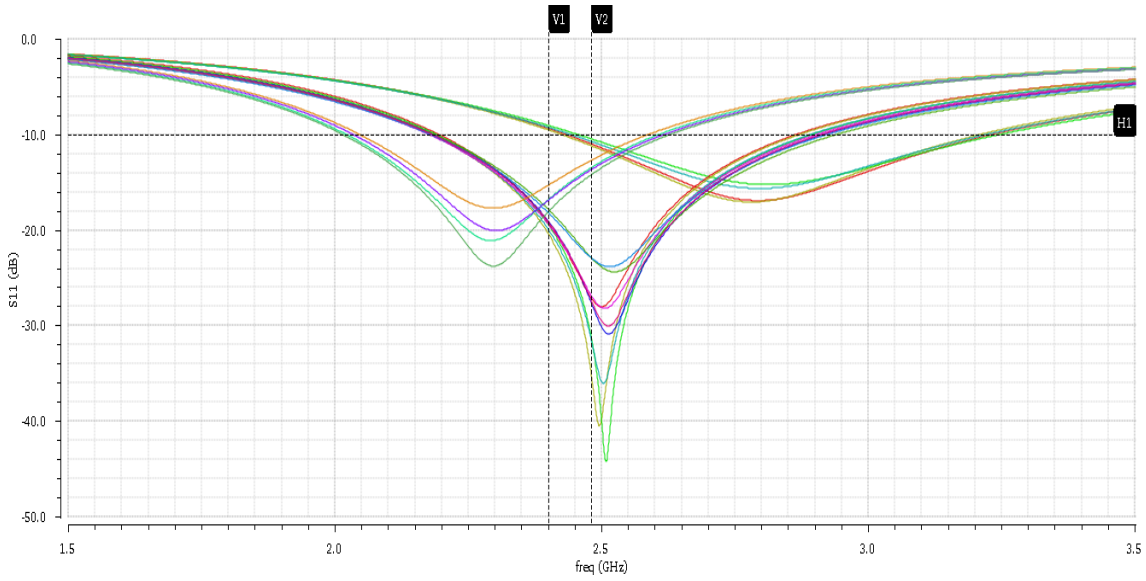
(b) Second Mode Noise Figure

Figure 3–22: First and Second mode noise figure

3.4.4.3 Return Loss



(a) First Mode S11



(b) Second Mode S11

Figure 3–23: First and Second mode S11

3.4.4.4 Third-Order Intercept Point & 1-dB Compression Point

Output	Spec	Weight	Pass/Fail	Min	Max
Input Referred 1dB Compress...				-22.55	-18.73
Input Referred IP3 Point				-10.93	-8.187

(1.a) First Mode 1-dB Compression Point and IIP3 for SS Case

Output	Spec	Weight	Pass/Fail	Min	Max
Input Referred 1dB Compress...				-29.62	-27.25
Input Referred IP3 Point				-21.32	-18.77

(2.a) First Mode 1-dB Compression Point and IIP3 for FS, TT, and SF

Output	Spec	Weight	Pass/Fail	Min	Max
Input Referred 1dB Compress...				-30.58	-28.96
Input Referred IP3 Point				-23	-20.46

(3.a) First Mode 1-dB Compression Point and IIP3 for FF

Output	Spec	Weight	Pass/Fail	Min	Max
Input Referred 1dB Compress...				-5.748	-4.53
Input Referred IP3 Point				-6.87	-4.808

(1.b) Second Mode 1-dB Compression Point and IIP3 for SS

Output	Spec	Weight	Pass/Fail	Min	Max
Input Referred 1dB Compress...				-15.07	-13.35
Input Referred IP3 Point				-13.32	-7.313

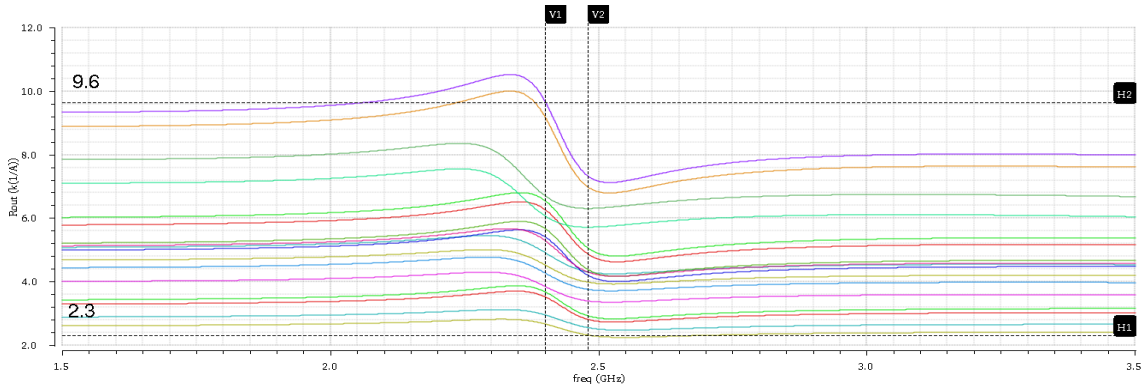
(2.b) Second Mode 1-dB Compression Point and IIP3 for FS, TT, and SF

Output	Spec	Weight	Pass/Fail	Min	Max
Input Referred 1dB Compress...				-16.44	-14.62
Input Referred IP3 Point				-6.722	-5.382

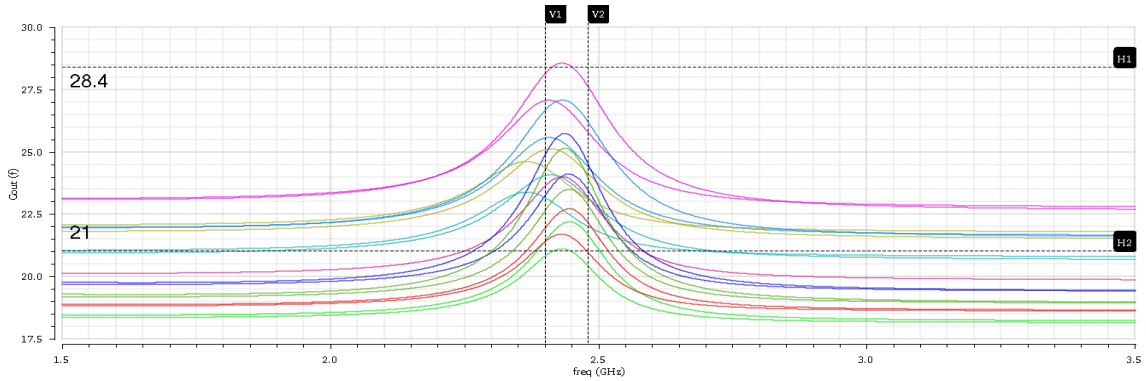
(3.b) second Mode 1-dB Compression Point and IIP3 for FF

Figure 3–24: Third-Order Intercept Point & 1-dB Compression Point Results

3.4.4.5 Output Impedance



(a) Output Resistance



(b) Output Capacitance

Figure 3–25: Output Resistance and Capacitance

3.5 Performance Summery

The LNA performance across typical and corner simulations for the 1st mode are summarized in Table 3.2 and Table 3.3 respectively.

Parameters	Required Specifications	Achieved Specifications
Current Consumption	<1.2 mA	1.28 mA
Trans-conductance Gain	>65.3 mA/V	62 mA/V
S11	< -12 dB	-25 dB
1 dB Compression point	-	-29 dBm
IIP3	>-20 dBm	-20 dBm
Noise Figure	< 3 dB	2.2 dB
Output Resistance	>5 kΩ	4.88 kΩ
Output Capacitance @ 2.44 GHz	<20 fF	24 fF

Table 3.3: LNA Design Specifications across Typical simulations

Parameters	Required Specifications	Achieved min.	Achieved max.
Trans-conductance Gain	>65.3 mA/V	22.8 mA/V	96.6 mA/V
S11	< -12 dB	-10 dB	-48.5 dB
1 dB Compression point	-	-32 dBm	-18 dBm
IIP3	>-20 dBm	-23 dBm	-8 dBm
Noise Figure	< 3 dB	4.8 dB	1.3 dB
Output Resistance	>5 kΩ	2.3 kΩ	9.6 kΩ
Output Capacitance @ 2.44 GHz	<20 fF	21 fF	28 fF

Table 3.4: LNA Design Specifications across Corner simulations for Mode1

3.6 Future work

The last mentioned capacitor array should be controlled through AGC or a process monitor circuit which will be serving the whole chip. Also, layout of the whole block is considered to be as a future work.

3.7 References

[1] B. Razavi, RF Microelectronics (*2nd Edition*) (Prentice Hall Communications Engineering and Emerging Technologies Series), Prentice Hall Press, Upper Saddle River, NJ, USA, 2nd ed., 2011.

[2] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, Analysis and Design of Analog and Integrated Circuits (fifth Edition).

[3] Y. Han and D. J. Perreault, "Analysis and Design of High Efficiency Matching Networks," in *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1484-1491, Sept. 2006.

[4] Voinigescu, S. (2013). In High-Frequency Integrated Circuits (The Cambridge RF and Microwave Engineering Series, pp. 439-502). Cambridge: Cambridge University Press.

[5] M. M. Tarar, M. Wei and R. Negra, "Stacked inverter-based amplifier with bandwidth enhancement by inductive peaking," 2014 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC), Leuven, 2014, pp. 1-3.

[6] Alpana Agarwal, Akhil Sharma, "Inverter Based Gain-Boosting Fully Differential CMOS Amplifier,"2017 World Academy of Science, Engineering and Technology International Journal of Electrical and Computer Engineering.

[7] L. Lah, J. Choma and J. Draper, "A continuous-time common-mode feedback circuit (CMFB) for high-impedance current-mode applications," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, no. 4, pp. 363-369, April 2000.

4 Chapter 4: Down-Conversion Mixer

The mixer is the main block in the receiver chain as it is the block responsible of down converting the signal from radio frequency (RF) to the base band.

As being preceded by the LNA, the mixer required noise figured has been relaxed in order to pay more attention to the linearity.

The challenge in mixer is to provide such high linearity with minimum power for the given local oscillator (LO) signal. In addition; the mixer is required to have acceptable gain, acceptable noise figure, small area and be suitable to be driven by the LO.

4.1 Introduction

Mixers perform frequency translation by multiplying two waveforms (and possibly their harmonics). As such, mixers have three distinctly different ports. Figure 4.1 shows a generic transceiver environment in which mixers are used. In the receive path, the down-conversion mixer senses the RF signal at its “RF port” and the local oscillator waveform at “LO port.” The output is at the baseband port in a direct-conversion RX or “IF port” in a heterodyne and Low-IF RX (our case).

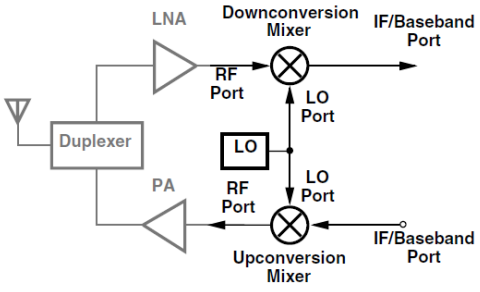


Figure 4–1: Role of mixers in a generic transceiver

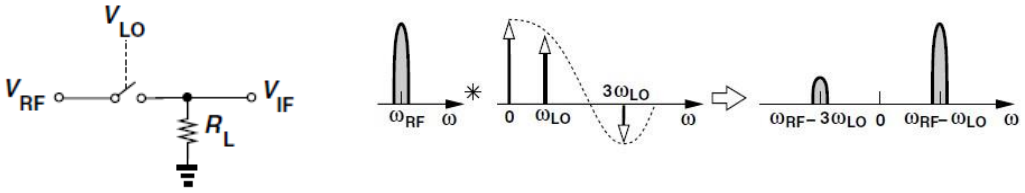


Figure 4–2: (a) Realization of mixer as ideal switch, (b) input and ouput spectra

A mixer can simply be realized by a switch as depicted in figure 4.2(a), where the LO turns the switch on and off yielding an IF output equals the RF input when the switch on and zero when off. With abrupt switching, the operation can be viewed as multiplication of the RF input by a square wave toggling between 0 and 1 even if LO waveform itself is a sinusoid. Thus, as illustrated in figure 4.2(b), the circuit mixes the RF input with all of the LO harmonics, producing what is called (mixing spurs). The question now is; Should the LO port of mixers be linearized so as to avoid mixing with the LO harmonics? In practice, mixers suffer from a lower gain and higher noise as the switching in the LO port becomes less abrupt. We therefore design mixers and LO swings to ensure abrupt switching and deal with mixing spurs at the architecture level.

4.2 Performance Parameters

4.2.1 Gain

The gain of mixers must be carefully defined to avoid confusion. The gain in down-conversion mixer is called “conversion gain” and defined as the ratio of the rms of the IF output signal to the rms of the RF input signal. In modern RF design, we prefer to employ voltage or current quantities rather than power quantities because the input impedances are mostly imaginary, making the use of power quantities difficult and unnecessary.

4.2.2 Noise and Linearity

The design of down-conversion mixers entails a compromise between the noise figure and the IP3 (or P1dB); since the mixer noise and IP3 are divided by different gains. So, the designs of the LNA and the mixer are extremely linked, requiring that the cascade be designed as one entity.

4.2.3 Port-to-Port Feedthrough

Due to the parasitic capacitance of the used devices, mixers suffer from unwanted coupling (feedthrough) from one port to another [Figure 4.3].

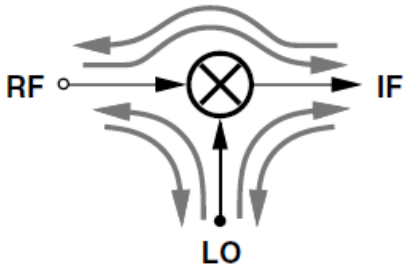


Figure 4–3: Feedthrough in mixer

The effect of mixer port-to-port feedthrough on the performance depends on the architecture. For Low-IF (our Rx):

1. The RF-LO feedthrough is critical because in-band interferers are near to the LO frequency, creating injection pulling and may desensitize the mixer.

2. Both the RF-IF and IF-RF feedthroughs proves benign because high-frequency components appearing at the IF port can be removed by low-pass filtering and vice-versa for RF port with ac coupling cap that works as high-pass filter.

3. The LO-IF feedthrough is negligible because it is heavily suppressed by the baseband low-pass filter.

4.3 Mixer Architecture

Mixers perform frequency translation by multiplying two waveforms (and possibly their harmonics). As such, mixers have three distinctly different ports. Figure 4.1 shows a generic transceiver environment in which mixers are used. In the receive path, the down-conversion mixer senses the RF signal at its “RF port” and the local oscillator waveform at “LO port.” The output is at the baseband port in a direct-conversion RX or “IF port” in a heterodyne and Low-IF RX (our case).

4.3.1 Single-Balanced and Double-Balanced Mixers

In single balanced mixer [figure 4.6]; two switches are driven by differential LO phases, thus commutating the RF input to the two outputs. That name is because of the bal- anced LO waveforms, this configuration provides differential outputs even with a single- ended RF input, easing the design of subsequent stages and increasing the conversion gain rather than the simple switch. Also, the LO-RF feedthrough at ωLO vanishes if the circuit is symmetric. On the other hand; the single-balanced mixer suffers from significant LO-IF feedthrough.

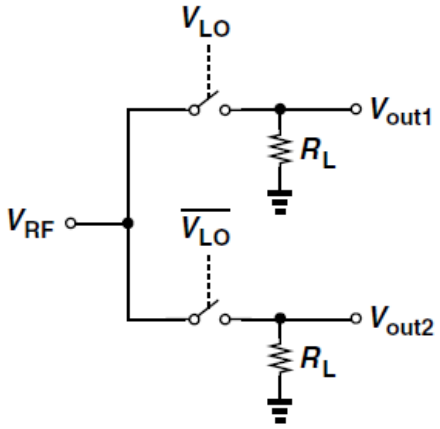


Figure 4–4: Single balanced passive mixer

In the double balanced mixer [figure 4.7]; the circuit operates with both balanced LO waveforms and balanced RF inputs. The advantage of such topology is the cancellation of the LO-IF feedthrough.

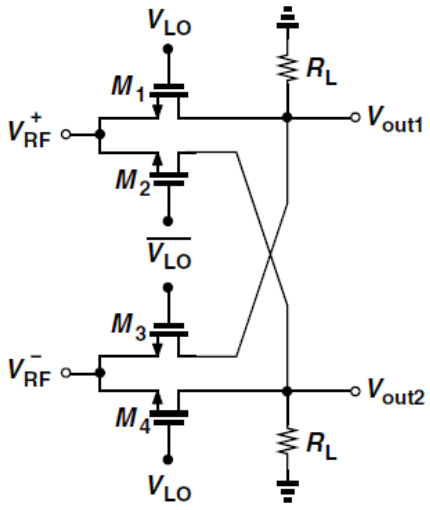


Figure 4–5: Double balanced passive mixer

4.3.2 Passive and Active Down-Conversion Mixers

Mixers can be generally classified as passive topologies (their transistors do not operate as amplifying devices) and active topologies (achieving conversion voltage gain higher than unity); each can be realized as a single-balanced or a double-balanced circuit.

4.3.3 Duty cycle 25% and 50%

Mixers are driven with LO signals that can be with duty cycle (d). The most common duty cycles used are 25% and 50%.

4.4 Mixer Topology Choice

4.4.1 Assigned Specs

Gain	-14 dB
Noise Figure	<55 dB
IIP3	>50 dBm

Table 4.1: Assigned Mixer Specs

4.4.2 Topology Survey and Choice

4.4.2.1 Active vs. Passive

The first decision we had to take is the choice between active topologies and passive topologies. So, we examined the advantages and the disadvantages of the two approaches and found them as follow:

	ACTIVE TOPOLOGIES	PASSIVE TOPOLOGIES
ADVANTAGES	- High gain and hence low noise figure	- Low power consumption - High linearity - More simple than active topologies
DISADVANTAGES	- High power consumption - Low linearity	- Low gain and hence high noise figure - Require high LO power (rail to rail) and sharp transitions to ensure abrupt switching.

From the standard, we design the receiver for low power applications. Moreover, from the given specs, both the noise figure and gain are relaxed and the main concern is the linearity.

So, passive mixer is the pursued one.

4.4.2.2 Single-Balanced vs. Double-Balanced

Most mixers are configures as double-balanced mixers. But in some cases, it is fine to just pick the single-balanced topology.

	Single-Balanced	Double-Balanced
ADVANTAGES	- LO-RF feed-through vanishes except for circuit mismatches	- Provides both LO-RF and LO-IF rejection. - Increased linearity compared to singly balanced - High intercept Points
DISADVANTAGES	- Lo-IF feed-through is still significant	- Require two baluns especially one after the LNA. - Relative high noise figure. - More problems that appear at very high frequencies.

From the survey, we find that the main advantage for the double-balanced mixer is the LO-IF isolation; which is not very dangerous in for Low-IF receivers. Moreover, the double-balanced mixers -system wise- need a balun after the LNA which needs more hard effort in design because of matching issues, and in fabrication as it needs inductors that have large area.

So, single-balanced topology is chosen for design.

4.4.2.3 Duty cycle 25% vs. 50%

According to the frequency multipliers theory regarding their efficiency vs duty cycle, it can be seen that there is dependency of harmonic level vs duty-cycle of the signal, phenomenon that most probably affect also the switching mixers. From the plot in fig.5 can be seen that 2nd harmonic has highest amplitude at 25% duty-cycle, and a minimum of amplitude at 50% duty-cycle which means 50% duty-cycle is the best choice for 2nd order linearity (IIP2) and DC offset problems.

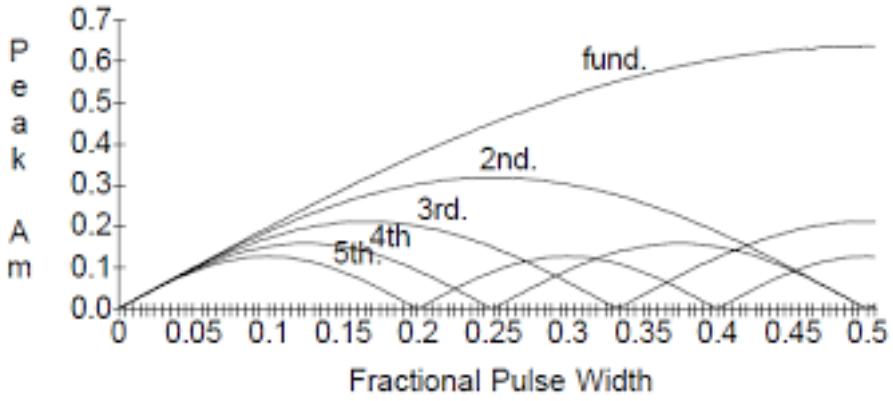


Figure 4–6: frequency multipliers theory

However, in our receiver we use I/Q architecture in order to perform image rejection. Using 50% duty cycle with I/Q architectures causes overlapping between the I and Q channels. On contrary, the 25% duty cycle removes the overlapping of the "on" state of both channels, and reduces the averaging window of the RF voltage. Moreover, it provides a higher gain, smaller noise and nonlinearity.

So, we use 25% duty cycle LO signals.

4.4.3 Conclusion

Our Topology for the down conversion mixer is a current-driven single-balanced passive mixer with 25% LO duty cycle with two channels I/Q.

4.5 Passive Mixer Design

The circuit shown in figure 4.6(b), is the implementation of a current-driven single-balanced passive mixer, and figure 4.6(a) is its symbol. The RF input current enters the RF port and is switched to exit through the I/Q differential channels by four phases of an LO signal with 25% duty cycle (0°, 180° for the I channel & 90°, 270° for the Q channel) as shown in figure 4.7. Then we design the driver gates to produce the 25% duty cycle as we receive a 50% duty cycle from the PLL, the symbol is shown in figure 4.8(a) and the implementation in figure 4.8(b).

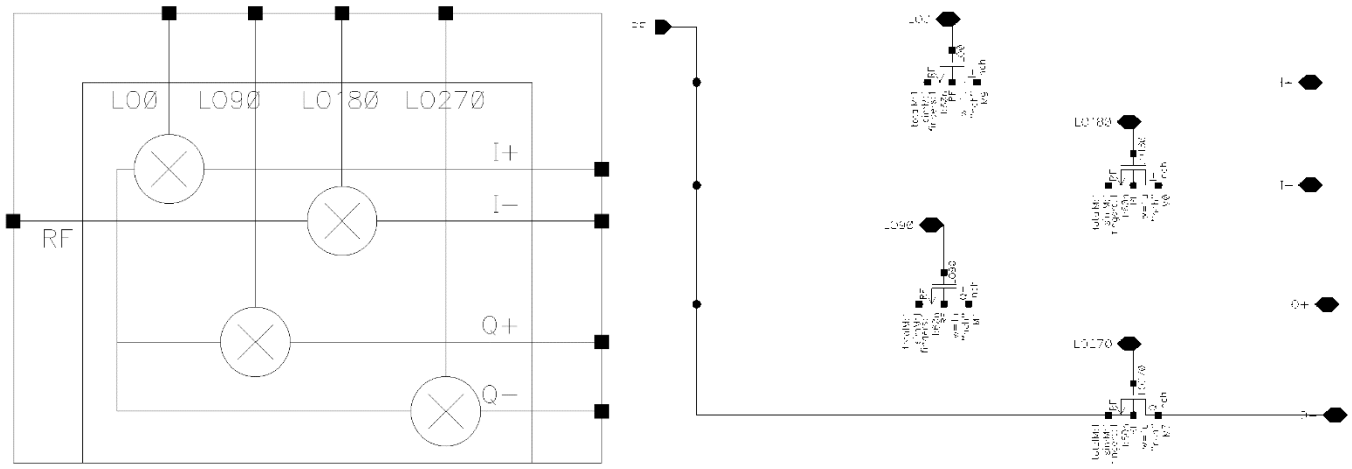


Figure 4–7: proposed mixer (a)symbol (b)schematic

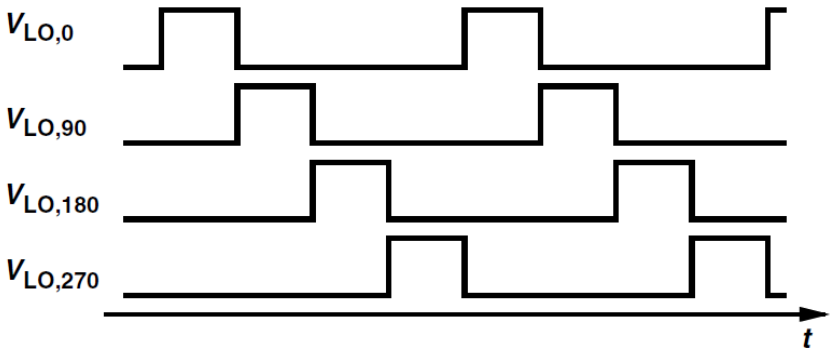


Figure 4–8: waveforms of LO ports

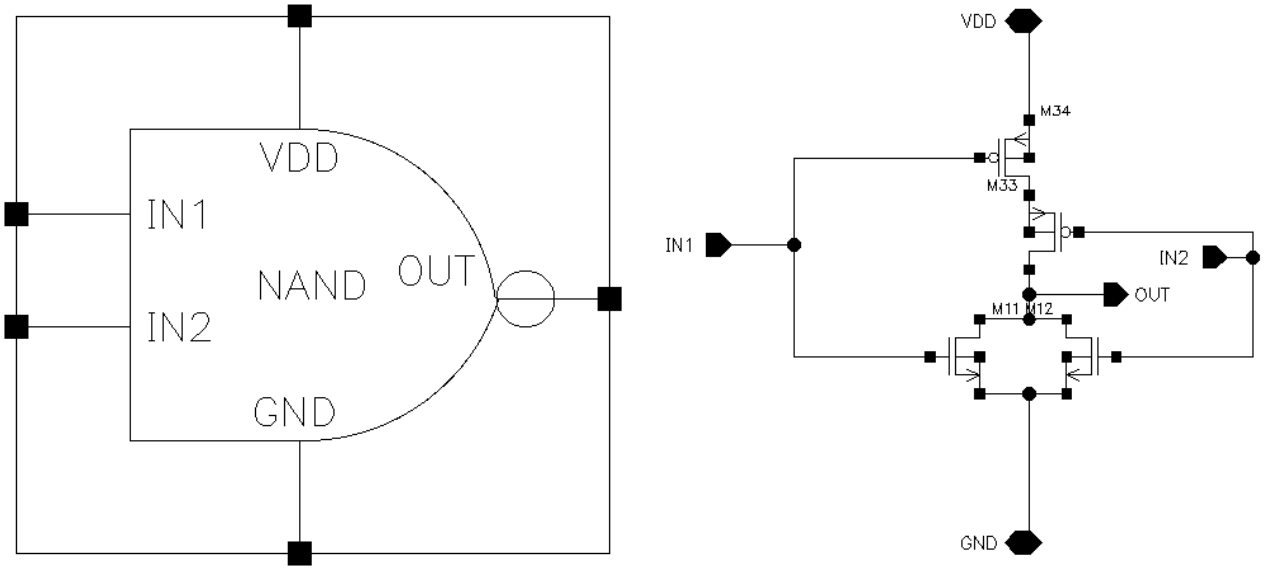


Figure 4–9: driving NAND gates (a)symbol (b)schematic

4.5.1 Design parameters

Mainly, we have three design parameters; gain, noise figure, and linearity. The conversion gain is expressed in (1) while the IM3 product signal at the baseband is expressed in (2).

Where;

C : the coupling capacitor between the LNA and the mixer

Rp : the resistive component of the LNA output impedance

ZBB : the baseband (TIA) input impedance

RSW : the switch on resistance

Vm,φm: are the intermodulation product values at ωm = (2ω1 - ω2)

$$conversion\ gain = \frac{\sqrt{2}}{\pi} \frac{X_C}{\frac{X_C^2}{R_p} + R_{SW} + \frac{2}{\pi^2} R_{BB}} \quad (1)$$

$$I_{BB,I} = I_{BB,Q} e^{-j\pi/2} = -\frac{1}{\pi^2} \frac{V_m e^{j\varphi_m}}{\frac{Z_C^2}{2R_p} + R_{SW} + \frac{1}{\pi^2} Z_{BB}(\omega_m)} \quad (2)$$

Hence, the only design variable is the RSW, i.e. the sizing of the mixer transistors.

4.5.2 Design procedure

We start with a certain transistor width (W = 200nm), and then we test the circuit, iterate the width and debug the limitations till we meet the specs.

For the driving Gate, We design for the transient waveform to have minimum off duration at switching instances, i.e. it is not desirable the all the transistors are off at the same time for too long. Hence, we increase the fall time and decrease the rise time, which is achieved by increasing width of PMOS transistors and decreasing the width of NMOS transistors.

4.6 Passive Mixer Simulation

Since the passive mixer does not have a bias not consume power, we should model the blocks before and after it in the chain, i.e. the LNA and the TIA.

The LNA is modeled by a VCCS with parallel impedance (5KΩ//20fF) to represent the LNA output impedance. Between the LNA and the mixer we have ac coupling capacitor that should have lower impedance than Zout of the LNA at 2.44GHz so that the input current sees low impedance and flows through it.

The output of the mixer should have the same common mode voltage as the TIA, as we cannot use coupling capacitors for low frequency (at the IF port after down conversion). So, the TIA is modeled by a VCVS with high gain and feedback resistance that is equal to the input impedance of the TIA (1.2KΩ).

The transconductance of the VCCS that models the LNA is set to be 1/1200 so that the total gain of the test chain (GMLNA*CGMIXER*1/RTIA) is equal to the conversion gain of the mixer only. Figure shows the test circuit

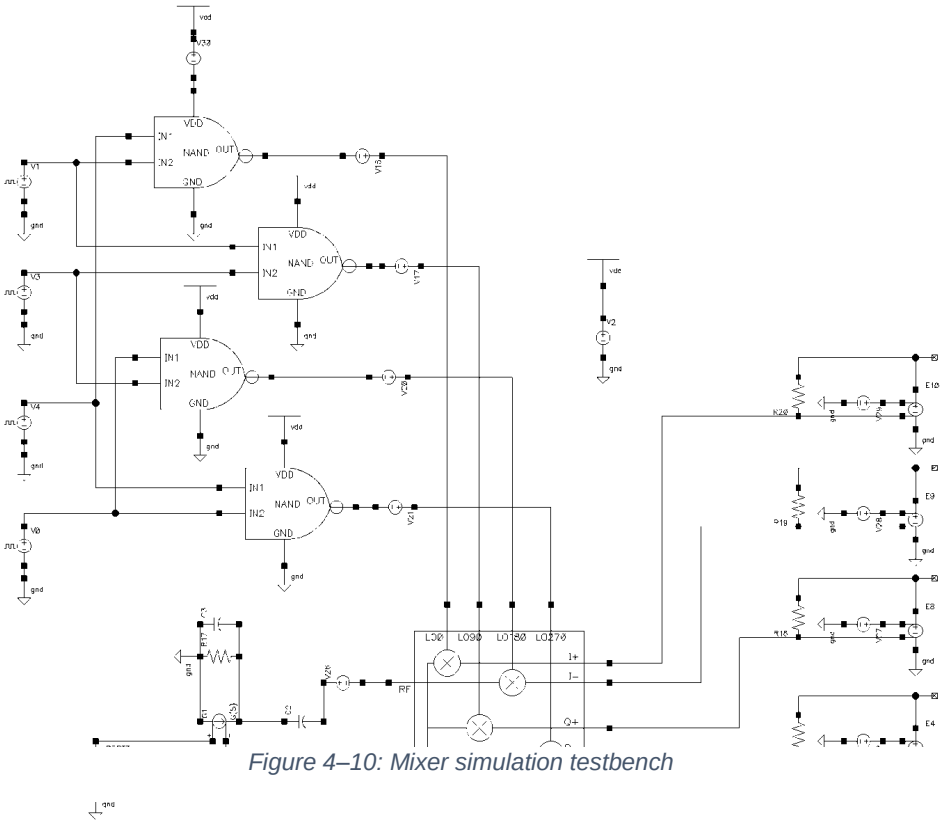


Figure 4–10: Mixer simulation testbench

4.6.1 Final Element's Values

The mixer is designed in TSMC 65n technology. The following table shows the final values and specifications of each component found in figure 4.8.

Device	Type	Specs
RF switching transistors	Nch_mac	$w = 1\mu m$, $L = 60\,nm$
Driving gates NMOS trs	Nch_mac	$w = 120\,nm$, $L = 60\,nm$
Driving gates PMOS trs	Pch_mad	$w = 600\,nm$, $L = 60\,nm$
Coupling Cap		*Cap = 2pF*

Table 4.3: Final values of passive mixer component

4.6.2 Current consumption

The mixers circuit does not consume any current and The average current consumed by the driving gates is less than **50uAmps**

4.6.3 Gain

Figure 4.9 shows the mixer conversion gain. In mixer, we are interested only in the gain component at the IF frequency. That conversion gain is -7.6 dB at 1MHz.

We plotted the conversion gain vs the RF input power to get the 1dB compression point, which is >5dBm.

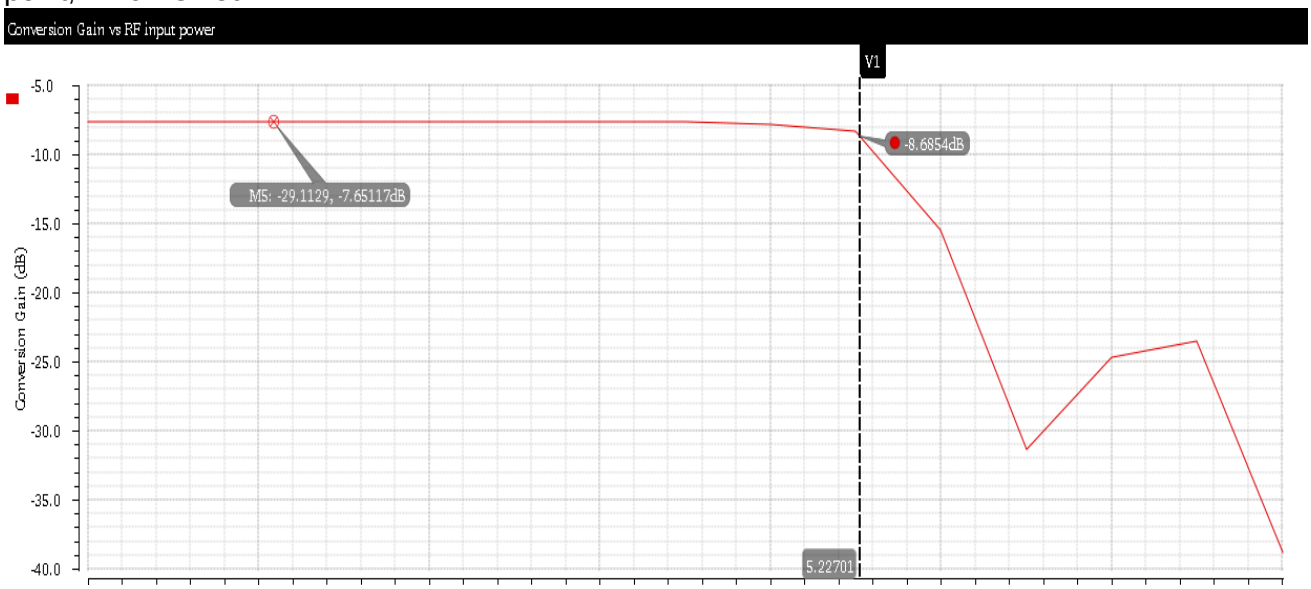


Figure 4–11: conversion gain and 1dB compression point

4.6.4 Noise Figure

The noise figure of the mixer is lower than 28dB. We are interested in the noise figure at frequency 1MHz ±0.5MHz as the channel bandwidth extends to 1M so, it is important to make sure that all frequencyin the band satisfies the noise requirements.

Figure 4.10 shows the NF variations versus frequency from 200K to 5G

1)at RF input power =1dBcompression point(5dBm)

2) and at a normal input power level (-20dBm).

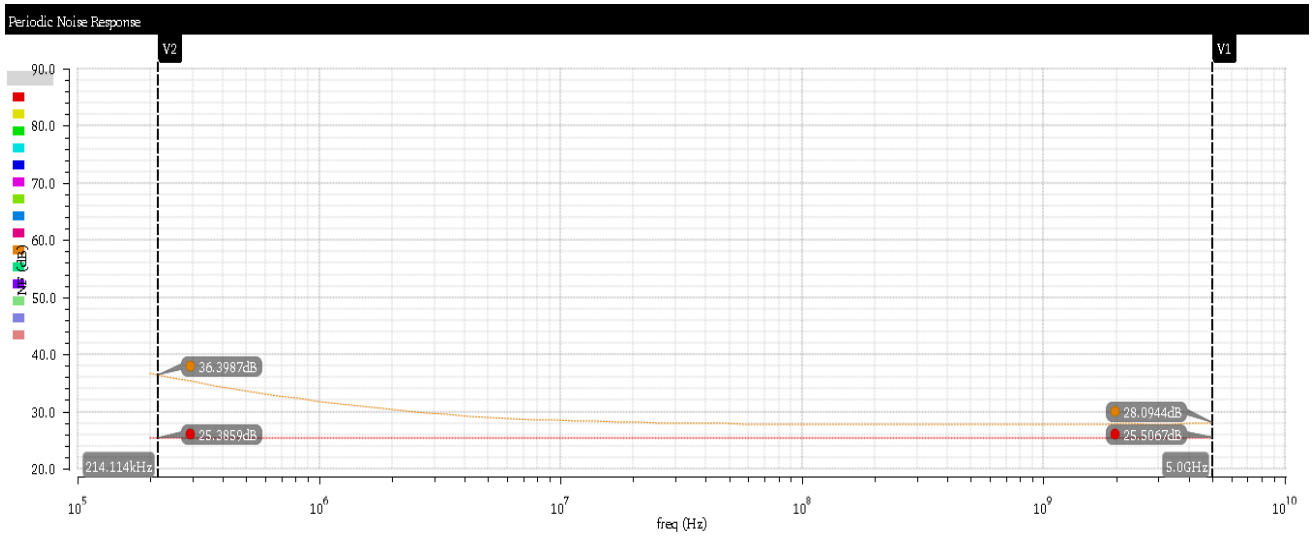


Figure 4–12: Noise Figure

4.6.5 IIP3

Since the mixer has input at frequencies different from the output frequencies, we get the IIP3 by measuring the OIP3 at the IF port and subtracting the conversion gain. First, we put two tones at the RF port spaced by 3MHz from each other and from the LO signal.

Then, we receive them at 3MHz and 6MHz at the IF port, with their IM component at 9MHz.

Then, we measure the OIP3 as seen in Fig. to be 16dBm. Finally, IIP3 = OIP3 – CG = 16 – (-7.6) = 23.6dBm.

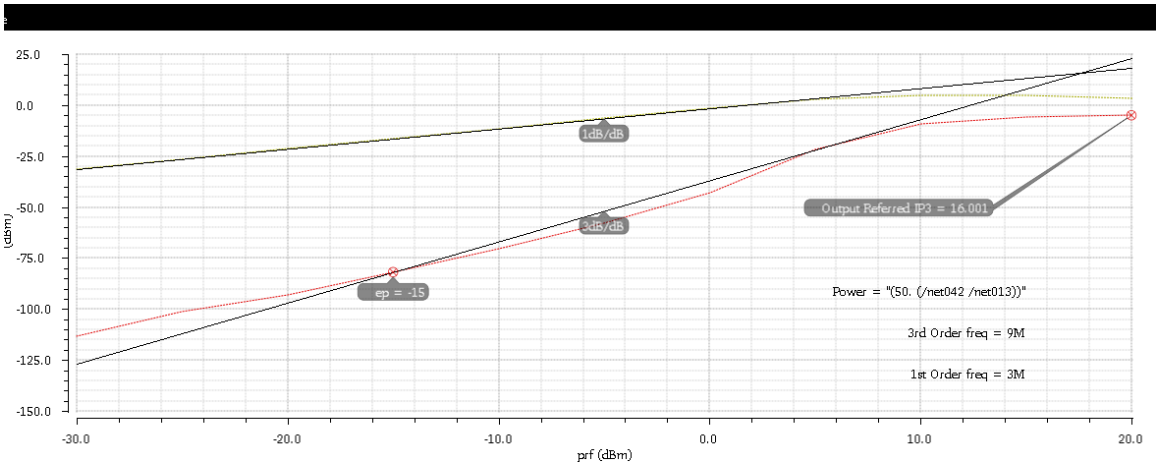


Figure 4–13: IIP3

4.7 References:

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[2] B. Razavi, “Design of analog CMOS integrated circuits”. Boston, Mass. McGraw-Hill.

[3] Yun-Yong Yu, Si-Zheng Chen, Tong Li and Hao Min (2016) Design of a Low Power Current-Driven Passive Mixer, IEEE.

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5 Chapter 5: Complex-Filter.

5.1 Overview

Complex filter is usually used in the low-IF wireless receiver to filter out the image signal, for its easy integration on chip. Active-RC filter is superior for the relatively large dynamic range comparing with OTA-C filter and since our input signal is current so we can merge the TIA and the complex filter in one block using the Active-RC implementation. The common way to synthesize the active-RC complex filter is to connect the complex pole in series, but it is sensitive to the variation of the parameters like resistance and capacitance. This characteristic is similar to the cascade-bi-quad method for the real filter. A synthesis method based on leapfrog low-pass prototype is proposed here, and it is less sensitive to components values variation compare to cascade-bi-quad or cascade-poles method.

5.2 Complex Filter theory

Complex filters are not new; they were invented by Sedra et al in 1985. However, to justify how to implement them, a brief theoretical discussion follows. To understand the ability of complex filters to reject the image signal, consider the complex representation of the receiver block diagram shown in Fig. 5.1. For the sake of illustration, we will assume that only the desired signal and its image are present at the mixer input. Without loss of generality, we will assume the signal and the image frequencies are $\omega_{LO} + \omega_{IF}$ and $\omega_{LO} - \omega_{IF}$, respectively. After eliminating the double LO frequency term by the mixer output low-frequency pole, the result of mixing the LO and RF signals in the complex domain is

$$B = G_{mixer}\left(x_{sig}\, e^{j\omega_{IF}t} + x_{image}\, e^{-j\omega_{IF}t}\right) = B_I + jB_Q \quad (5.1)$$

Where B_I and B_Q are the real and imaginary parts of the mixer output and can be expressed as:

$$B_I = G_{mixer}\left(x_{sig}\ \cos(\omega_{IF}t) + x_{image}\ \cos(\omega_{IF}t)\right) \quad (5.2a)$$

$$B_Q = G_{mixer}\left(x_{sig}\ \sin(\omega_{IF}t) - x_{image}\ \sin(\omega_{IF}t)\right) \quad (5.2b)$$

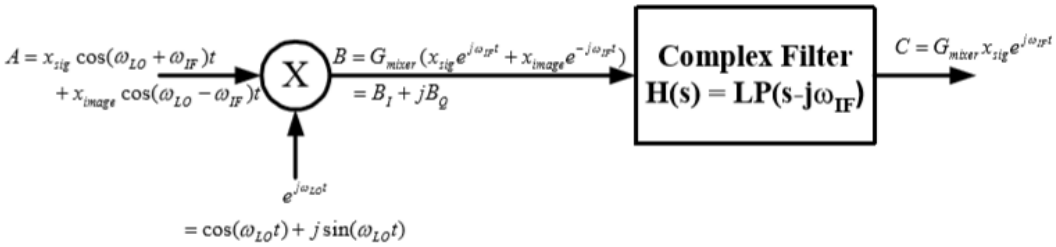


Figure 5–1: Receiver image rejection architecture in the complex domain

Note that in the above equation the desired (image) signal in the I branch leads (lags) the Q branch by 90º.

Fig. 5.2 illustrates the complex mixing operation on the desired signal and its image. Note that after down-conversion, the $2\omega_{IF}$ frequency separation between the signal and the image is still preserved. The complex channel select filter is then a frequency-shifted version of a low pass filter response. This means that the filter can pass the signal at ω= ω_{IF}, while attenuating the signal at ω=$-\omega_{IF}$. Since the filter has unsymmetrical frequency response around the jω axis, its time domain response is complex (here comes the name complex filter). However, the complex filter frequency response is symmetrical around the ω_{IF}. Since the blocking specifications of a receiver are symmetrical around the desired signal frequency, this is considered an advantage of complex filter over real BPF that has unsymmetrical frequency response around its center frequency.

These complex operations are practically performed as follows. Multiplication of the real RF signal by $e^{j\omega_{LO}}$ is practically performed using a quadrature mixer, which basically consists of two mixers whose LO inputs are in quadrature phase, as shown in Fig. 5.3. In the complex signal representation in Fig. 5.1, the desired signal at the mixer output is located at the positive IF frequency while the image signal is located at the negative IF frequency. In the real implementation in Fig. 5.3, the desired (image) signal in the I branch leads (lags) the Q branch by 90°.

The complex filter, in turn, is able to make the distinction between the signal and the image based on the phase difference between the I and Q branches. In the complex domain, the complex BPF is a frequency-shifted version of an LPF. To convert an arbitrary LPF to a complex BPF centered at ω_{IF}, every frequency dependent element in the LPF should be altered to be a function of s- jω_{IF} instead of s. The basic frequency dependent element in a filter is the integrator. Consider the simple case of converting a first order LPF with cut-off frequency ω_{LP} , to a complex filter BPF centered at ω_{IF}. The LPF response is shifted in frequency by placing it in a complex feedback loop as shown in Fig. 5.4(a). The complex input-output relation is given by:

$$x_o = \frac{\omega_o}{s+\omega_{LP}-j\omega_{IF}} x_i \quad (5.3)$$

Where $x_i = x_{iI} + jx_{iQ}$ and $x_o = x_{oI} + jx_{oQ}$ then from the above equation:

$$x_{oI} = \frac{\omega_o}{s+\omega_{LP}} \left(x_{iI} - \frac{\omega_{IF}}{\omega_o} x_{oQ}\right) \quad (5.4a)$$

$$x_{oQ} = \frac{\omega_o}{s+\omega_{LP}} \left(x_{iQ} + \frac{\omega_{IF}}{\omega_o} x_{oI}\right) \quad (5.4b)$$

Equation (5.4) is implemented as shown in Fig. 5.4(b). an active-RC implementation of this first order complex filter is shown in Fig. 5.4(c). Note that an inverting amplifier is needed in the cross feedback from Q branch to I branch. If a differential implementation is used, this extra inverting amplifier can be avoided by exchanging the differential signals.

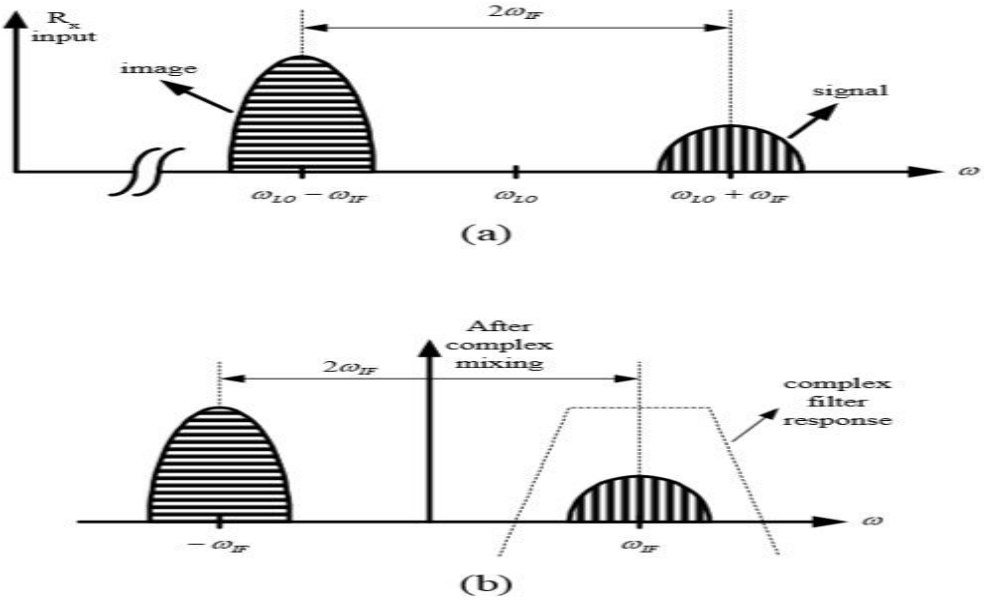


Figure 5–2: Frequency translation of a complex (quadrature) mixer (a) before complex mixing (signal A in Fig. 5.1) (b) after complex mixing (signal B in Fig. 5.1)

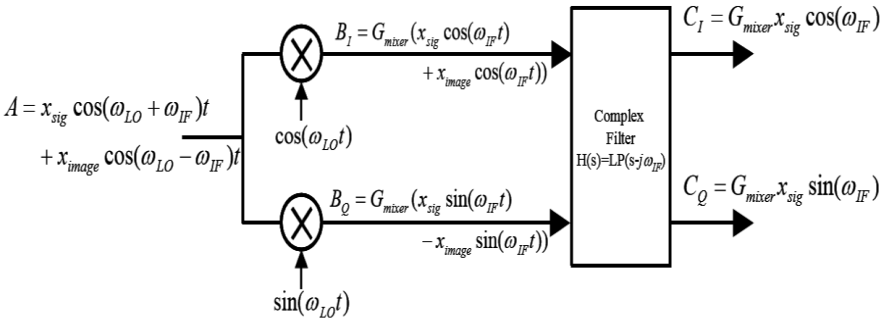


Figure 5–3: Practical implementation of the receiver image rejection

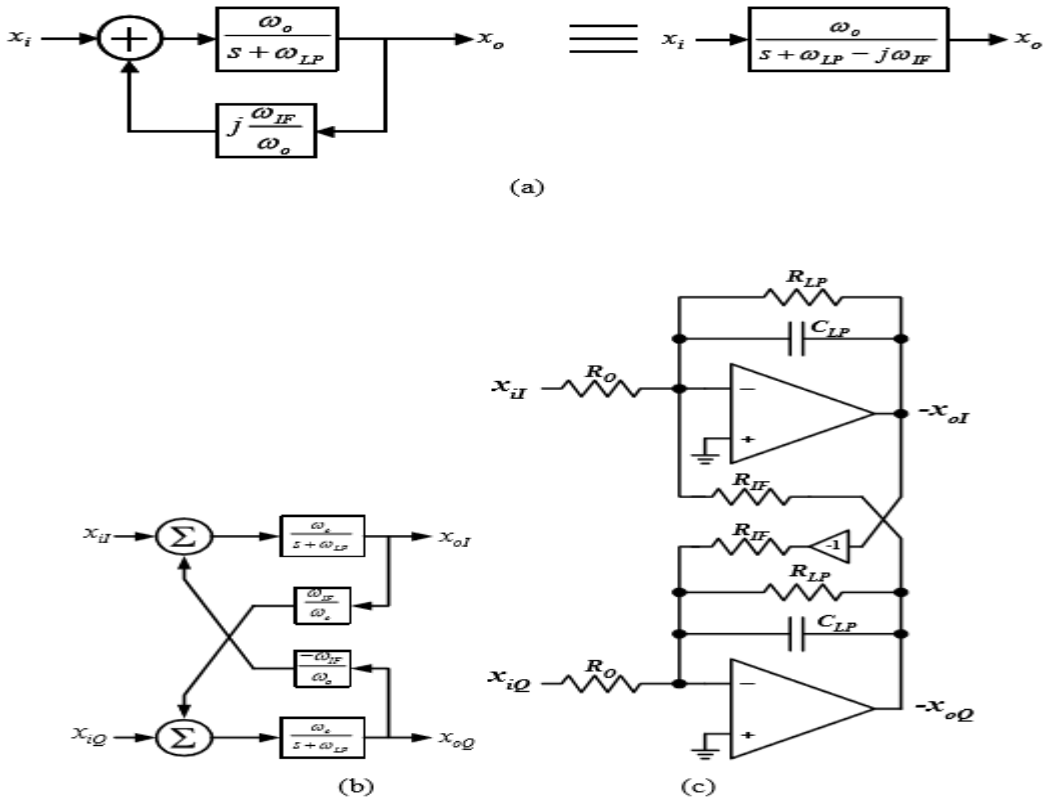


Figure 5–4: LPF shifted to ω_IF, (a) conceptual complex representation (b) actual building block implementation (c) Active-RC implementation

5.3 Complex Filter Implementation

As mentioned, before I have chosen the leap frog implementation over the cascaded biquad method because it has shown less sensitivity for components mismatch. I have also chosen the filter approximation to be Butter-worth because it has small group delay variation (0.6 µs), as group delay is critical in any system.

System level simulations show that a complex filter based on a 3rd order Butter-worth LPF is sufficient to achieve the required selectivity. In figure 5.5 and 5.6 I made the simulations on 3rd, 4th and 5th order low pass filter for the 1-Mega mode and the Two-Mega mode and the and the 3rd order was suitable to achieve the required signal to noise ratio.

1	Frequency offset	1M,-1M	2M,-2M	3M,-3M	Image freq(-2M)
2	Level of blockers	-82	-50	-40	-58
3	filter response (level)(3rd order)	-18.1306	-36.1203	-46.5675	-36.1203
4	blocker level+filter level (3rd order)	-100.131	-86.1203	-86.5675	-94.1203
5	input signal level	-67	-67	-67	-67
6	SNR(3rd order)=(sensitivity-(blocker level +filter level))	33.13058	19.12033	19.56752	27.1203
7	filter response (level)(4th order)	-24.0964	-48.1528	-62.0824	-48.1528
8	blocker level+filter level (4th order)	-106.096	-98.1528	-102.082	-106.1528
9	SNR(4th order)=(sensitivity-(blocker level +filter level))	39.09641	31.15279	35.08239	39.1528
10	filter response (level)(5th order)	-29.7017	-59.8251	-77.2434	-59.8251
11	blocker level+filter level (5th order)	-111.702	-109.825	-117.243	-117.8251
12	SNR(5th order)=(sensitivity-(blocker level +filter level))	44.7017	42.8251	50.24341	50.8251

Figure 5–5: Determining the suitable filter order for the 1-Mega Mode

Frequency offset	2M,-2M	4M,-4M	6M,-6M	Image freq(-4M)
Level of blockers	-82	-50	-40	-58
filter response (level)(3rd order)	-18.1275	-36.1337	-46.6879	-36.1337
blocker level+filter level (3rd order)	-100.128	-86.1337	-86.6879	-94.1337
input signal level	-67	-67	-67	-67
SNR(3rd order)=(sensitivity-(blocker level +filter level)	33.1275	19.1337	19.6879	27.1337
filter response (level)(4th order)	-24.1	-48.1658	-62.25302	-48.1658
blocker level+filter level (4th order)	-106.1	-98.1658	-102.25302	-106.1658
SNR(4th order)=(sensitivity-(blocker level +filter level)	39.1	31.1658	35.25302	39.1658
filter response (level)(5th order)	-30.1087	-60.2078	-77.81669	-60.2078
blocker level+filter level (5th order)	-112.109	-110.208	-117.81669	-118.2078
SNR(5th order)=(sensitivity-(blocker level +filter level)	45.1087	43.2078	50.81669	51.2078

Figure 5–6: Determining the suitable filter order for the 2-Mega Mode

Hence we get the required values of the inductors and the capacitors of the ladder that will form the low pas filter from the filter tables and constructed the ladder as shown in Fig 5.7 .

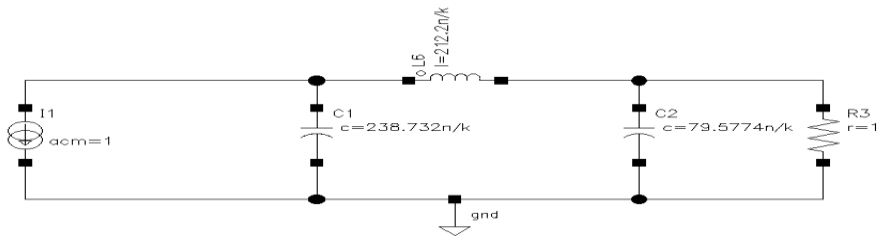


Figure 5–7: LC implementation of third order low pass filter with butter-worth approximation

C_1	L_1	C_2
$\frac{238.732n}{K*r}$	$\frac{212.2n}{K*r}$	$\frac{79.577n}{K*r}$

Where k is only a variable to translate the 3-dB cut-off frequency to be the 1-dB cut-off frequency and it was found to be 1.24.

Since we have a specification on the transimpedance gain to be 100 dB so we will scale up all the resistors by the value of 100K and scale down all the capacitors by the same value.

As shown in figure 5.8, We designed the 1dB cut-off frequency of the LC ladder to be 1 Mega so as when translating it to the given ω_{IF} , it will produce the two mega band-width needed.

After writing the conventional state equations to transform from the LC ladder implementation to the opamp-RC implementation using the leap frog technique, I constructed integrator-based filter shown in figure 5.9 which is equivalent to the above LC ladder.

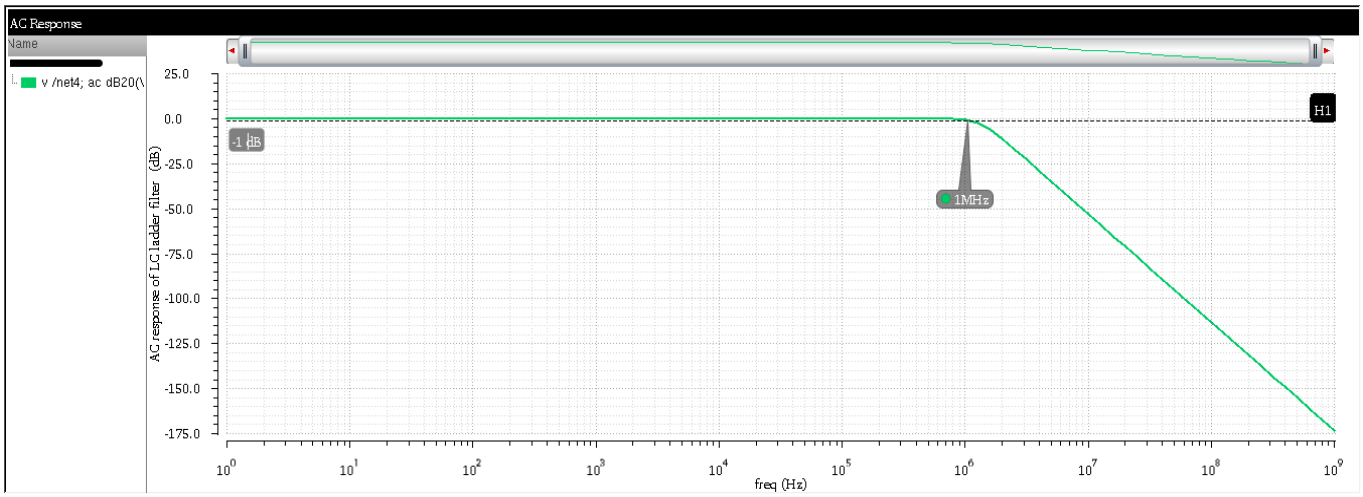


Figure 5–8: AC-response of LC ladder filter.

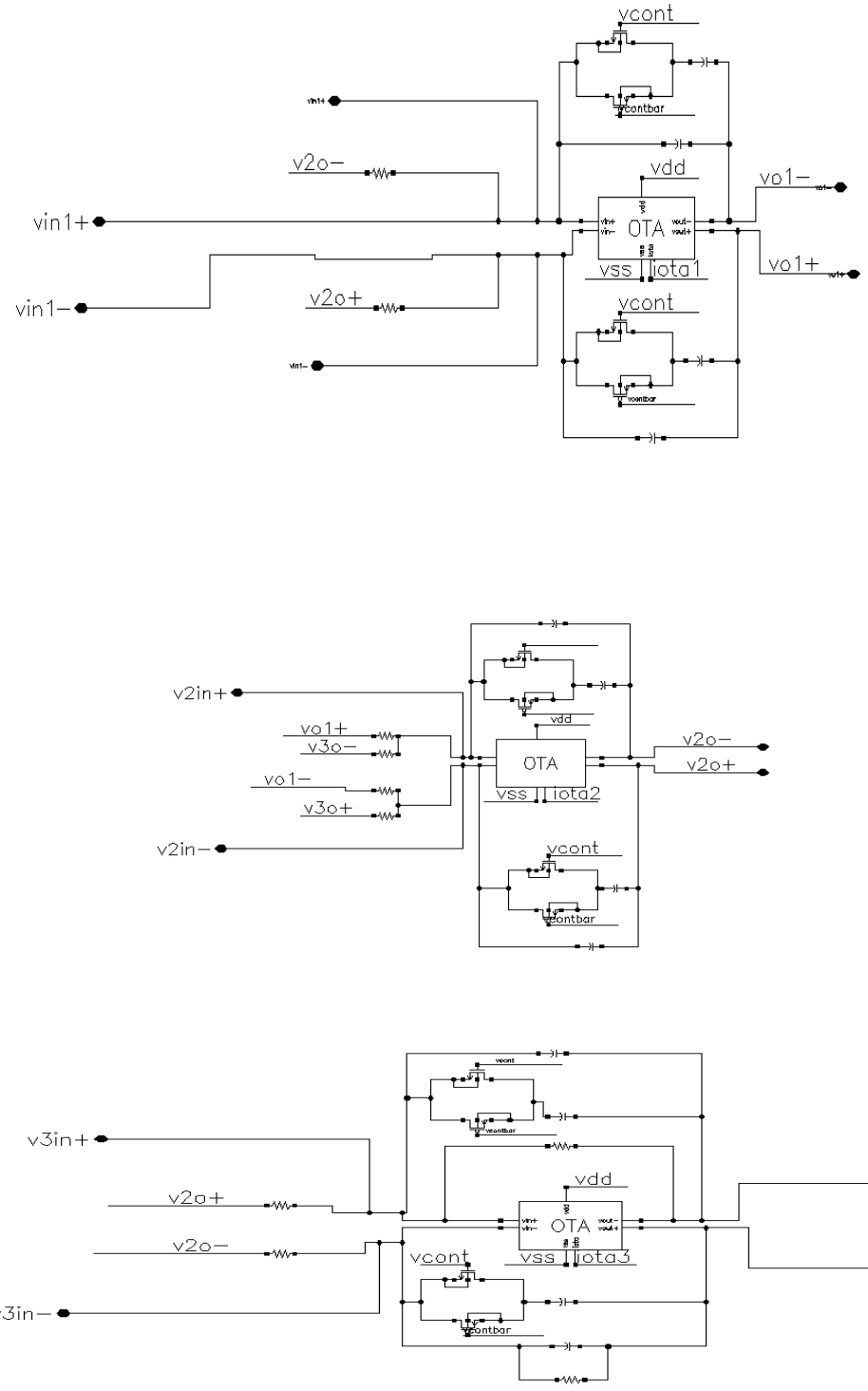


Figure 5–9: integrator based equivalent of LC ladder low pass filter.

The architecture of the complex filter is shown in Figure 5.10. It consists of two same low-pass prototypes filters. The two low-pass filters can implement the complex filter by adding three groups of 'frequency transform resistors. The frequency transform resistors can be calculated as below:

$$R = \frac{1}{\omega_c * C_i}$$

Where ω_c is the center frequency of the filter, C_i is the capacitance in the integrator section connected with the frequency transform resistors.

Positive quadrature output (V_{xoq+}) is connected to Positive in-phase input (V_{xin+})

Negative quadrature output (V_{xoq-})is connected to Negative in-phase input (V_{xin-})

Positive in-phase output (V_{xoin+}) is connected to Negative quadrature input. (V_{xiqn-})

Negative in-phase output (V_{xoin-}) is connected to Positive quadrature input. (V_{xiqn+})

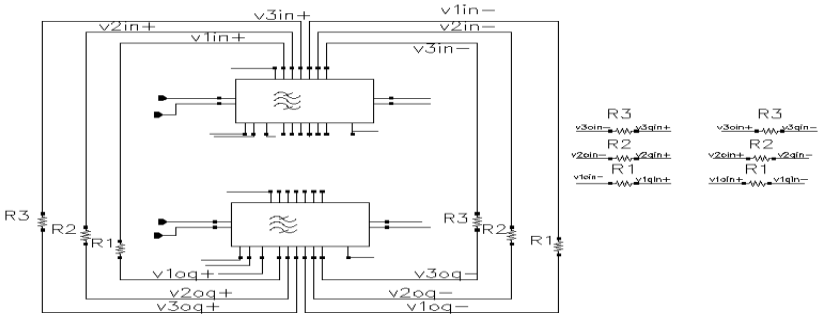


Figure 5–10: Architecture of op-amp-RC complex filter

And here are the values of the frequency transform resistors after scaling:

R_1	R_2	R_3
41.292 $K\Omega$	46.5 $K\Omega$	124 $K\Omega$

5.4 OTA Topology and CMFB

From system level simulations using the op-amp macro model it was found that in order to have a peaking with-in 1dB in the pass band a GBW of 160 MHz and a gain of > 51dB is needed.

Based on the literature survey it was found that the best OTA topology was the simple two stage OTA with miller compensation for two reasons:
1- we need high gain so it can be easily achieved with the two stages.

2- it is insensitive to the loading effect when compared to the single stage op-amp.

As shown in figure 5.11 , I have chosen the input pair to be PMOS and the output pair to be NMOS since I have a fixed current budget and for stability concerns, we need the transconductance of the second stage (g_{m2}) to be higher than the transconductance of the first stage and It is known that NMOS transistor have higher transconductance (g_m) than PMOS transistor for the same current and aspect ratio.

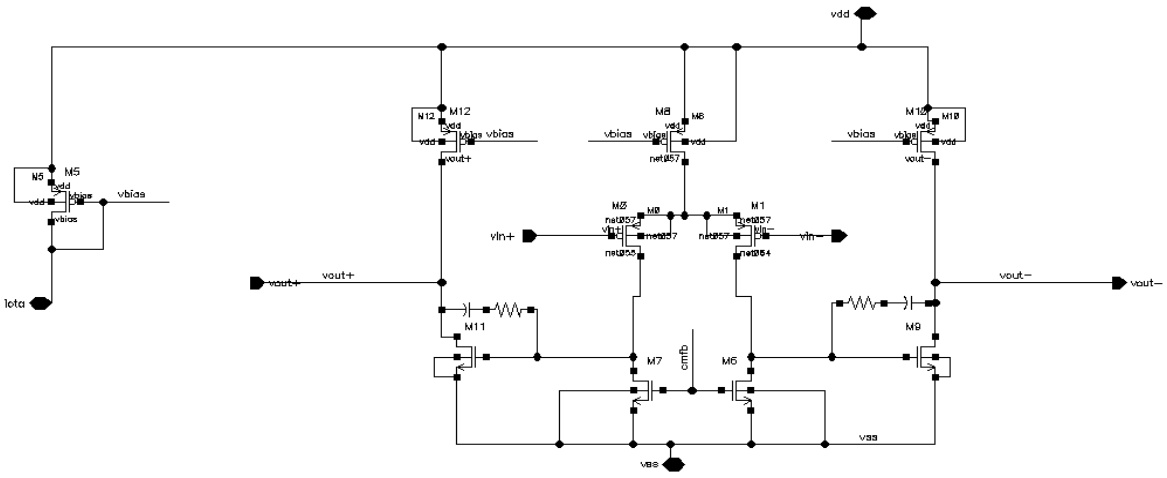


Figure 5–11: schematic of the Two-stage OTA

-since the gain bandwidth product = $\frac{g_{m1}}{C_c}$, where g_{m1} is the transconductance of the first stage and C_c is the miller compensation capacitor , therefore it is clear that the sizing of the input pair was to achieve the GBW specified .

- since we want to ensure the stability of the above OTA, we want the second non-dominant pole to be double the GBW for a phase margin of 60°.and since the second non dominant pole can be approximated as follows : $\omega_{nd} = \frac{g_{m2}}{C_L}$, therefore the second stage is sized accordingly.

The current mirrors were sized in order reduce the systematic offset effect hence we tried to increase their lengths to do so also, we needed to leave a margin of about 80 mV between $|V_{ds}|$ and $|V_{dssat}|$ to keep the current mirror transistor in saturation under the PVT corners .

5.4.1 OTA results simulation

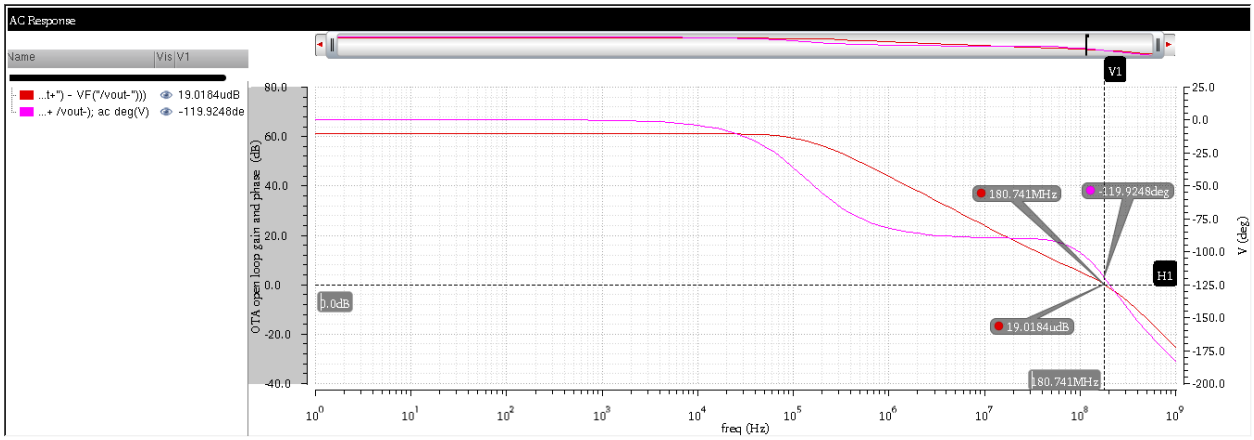


Figure 5–12: OTA open-loop gain and phase response

5.4.2 Common mode feedback

Since there is a high-impedance node at the output, a common mode feedback is needed , shown in figure 5.13 is the used common mode feedback circuit , this circuit was chosen because it will not introduce any dominant poles because the diode connected load transistors are low impedance therefore the pole at the output of the error amplifier is at high frequency .

A capacitor is added in parallel with the averaging resistor in order to enhance the phase margin of the common mode feedback loop to ensure its stability.

The added capacitor introduces a zero at frequency = $\frac{1}{C_{avg} * R_{avg}}$

Since the averaging resistors loads the OTA, therefore their values are desired to be as maximum as possible, but this is of course will be area consuming, so a value which degrades the open loop gain of the OTA by only 1dB was chosen.

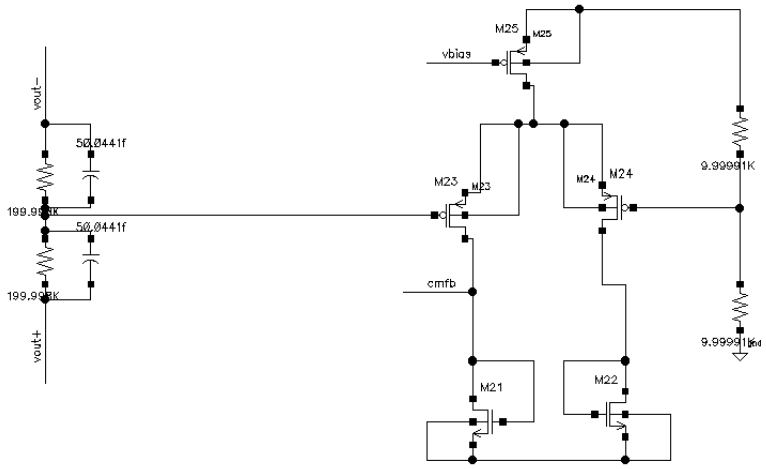


Figure 5–13: common mode feedback circuit

A stability analysis was performed for the common mode feedback loop and the results are shown in figure 5.14 and 5.15 respectively

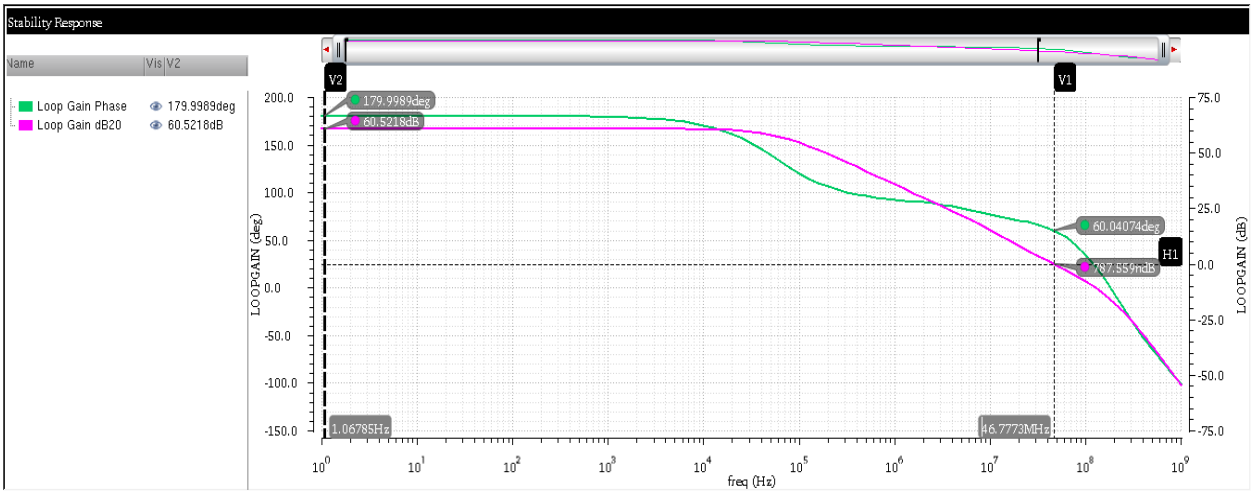


Figure 5–14: Common-mode loop phase & magnitude response

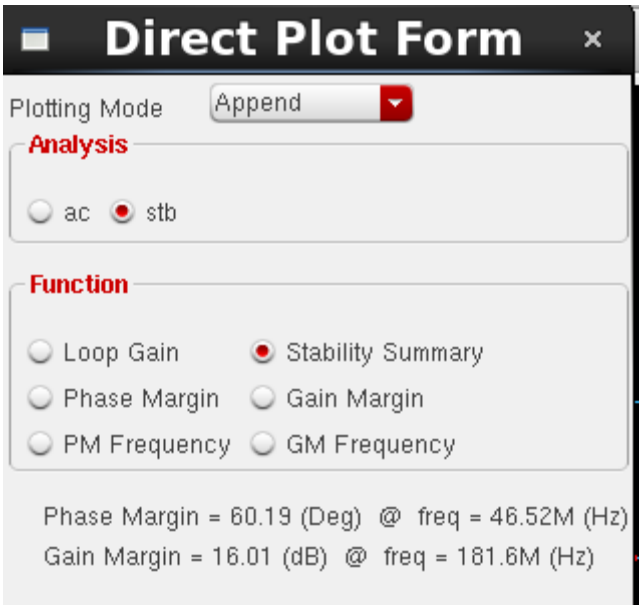
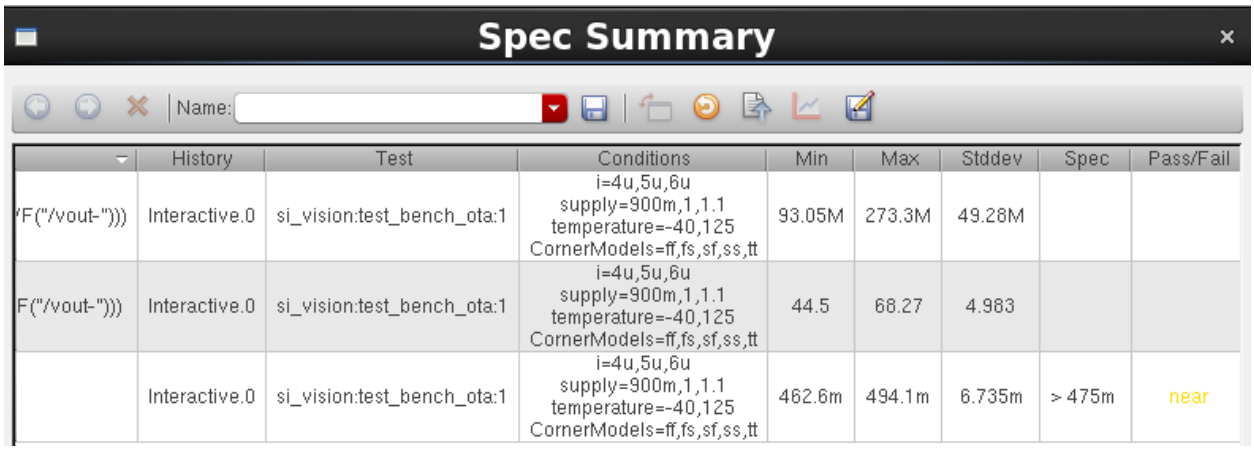


Figure 5–15: Common mode loop stability summary

5.4.3 OTA under PVT corners:

I have run PVT corners and simulated the performance of the OTA, the corners were +/- 10 % of the supply voltage and +/- 20% of the current budget. they were a total of 90 corners and figure 5.16 is a spec. summary across different corners which shows the variations of the phase margin and the variation of the common mode output level across different corners.



	History	Test	Conditions	Min	Max	Stddev	Spec	Pass/Fail
'F("/vout-")))	Interactive.0	si_vision:test_bench_ota:1	i=4u,5u,6u supply=900m,1,1.1 temperature=-40,125 CornerModels=ff,fs,sf,ss,tt	93.05M	273.3M	49.28M		
F("/vout-")))	Interactive.0	si_vision:test_bench_ota:1	i=4u,5u,6u supply=900m,1,1.1 temperature=-40,125 CornerModels=ff,fs,sf,ss,tt	44.5	68.27	4.983		
	Interactive.0	si_vision:test_bench_ota:1	i=4u,5u,6u supply=900m,1,1.1 temperature=-40,125 CornerModels=ff,fs,sf,ss,tt	462.6m	494.1m	6.735m	> 475m	near

Figure 5–16: Spec summary across different corners

Figure 5.16 shows that the worst-case phase margin is 44.5°. and the worst-case variation from the output DC level is about 30mv.

5.4.4 OTA Summary of specifications:

Spec.	Value
Open loop gain	V 61 dB
Phase margin	60.39°.
Gain bandwidth product	182.1 MHz
CMFB loop gain	60.5 dB
CMFB loop phase margin	60.19°.
Total Current consumption	214.4µA

5.5 Switching between the 1-Mega and the 2-Mega modes.

According to the BLE standard, there is two modes of operations 1) The 1-Mega mode: in which the channel bandwidth is 1-Mega

2)The 2-Mega mode: in which the channel bandwidth is 2-Mega hence we want to make the filter tunable in order for it to be compatible with the two modes of operations of the BLE standard. since the cut-off frequency of the filter varies inversely with the feedback capacitor, therefore if we doubled the value of the feedback capacitor, the cut-off frequency will decrease to half of its value. In this work we connected two feedback capacitor in parallel both of them have the same value , one of the two capacitor will be connected all the time and the other will be connected in series with a transmission gate switch and depending on the desired mode of operation the other capacitor is connected or disconnected accordingly as shown in figure 5.17 .

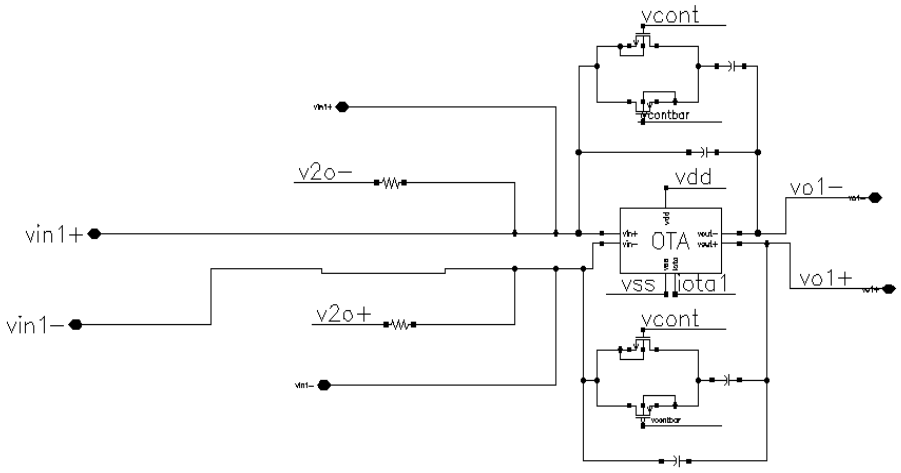


Figure 5–17: illustrating the switching between the two modes of operation

5.6 Filter simulation results

5.6.1 AC response

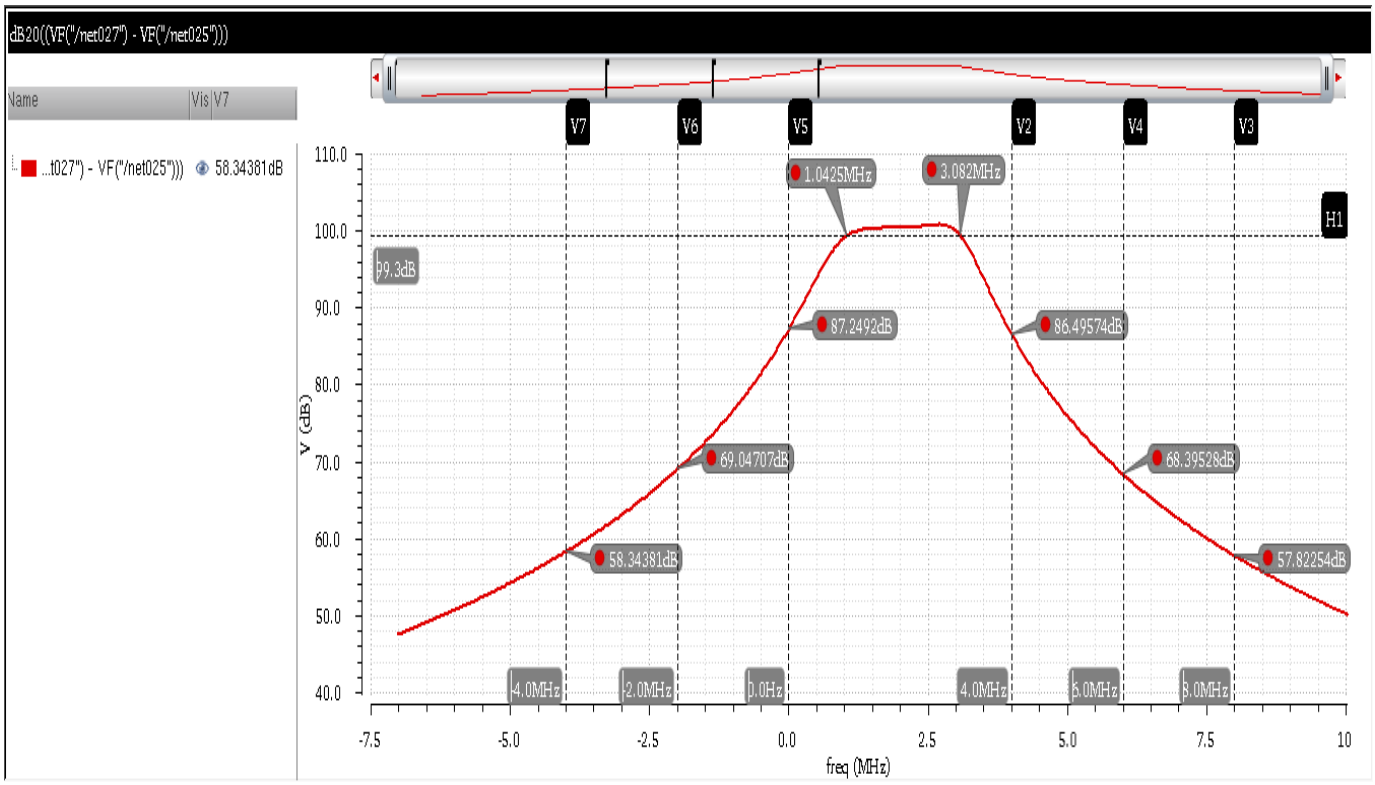


Figure 5–18: AC response of the 2-Mega mode

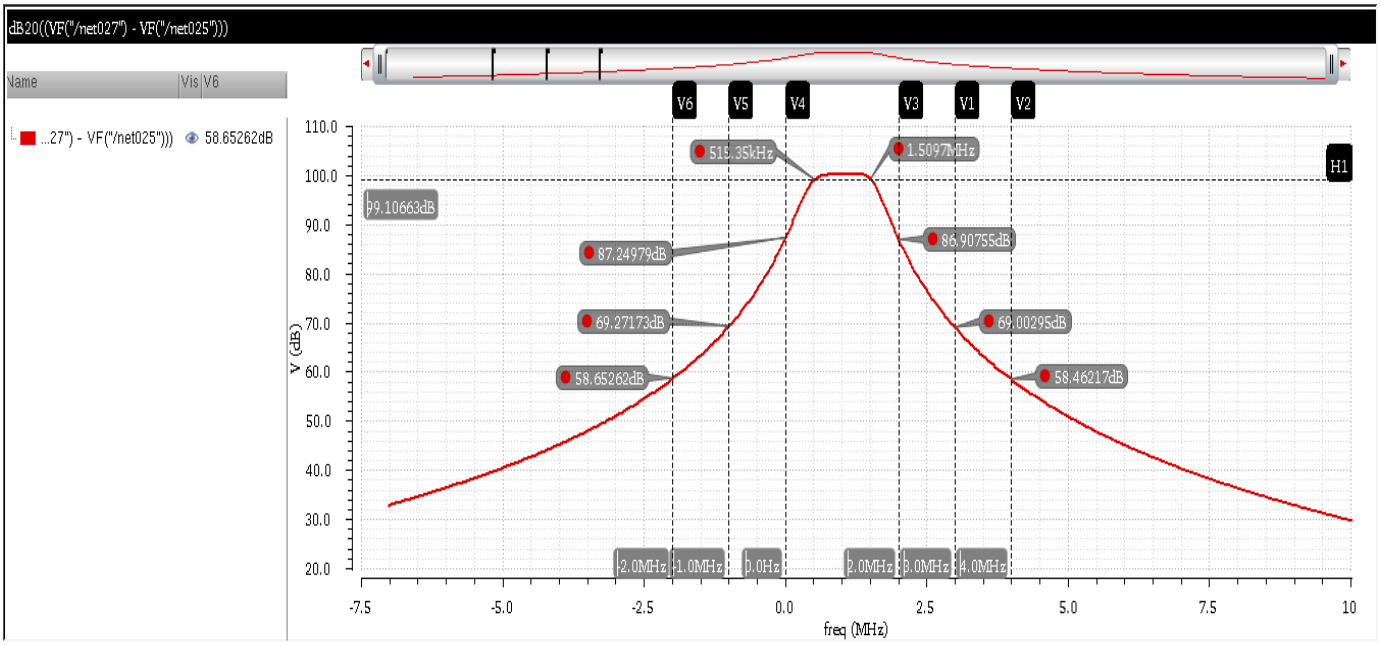


Figure 5–19: AC response of the 1-Mega Mode

5.6.2 Noise Figure:

Figure 5–20: Test bench used in simulating the noise figure and Linearity tests.

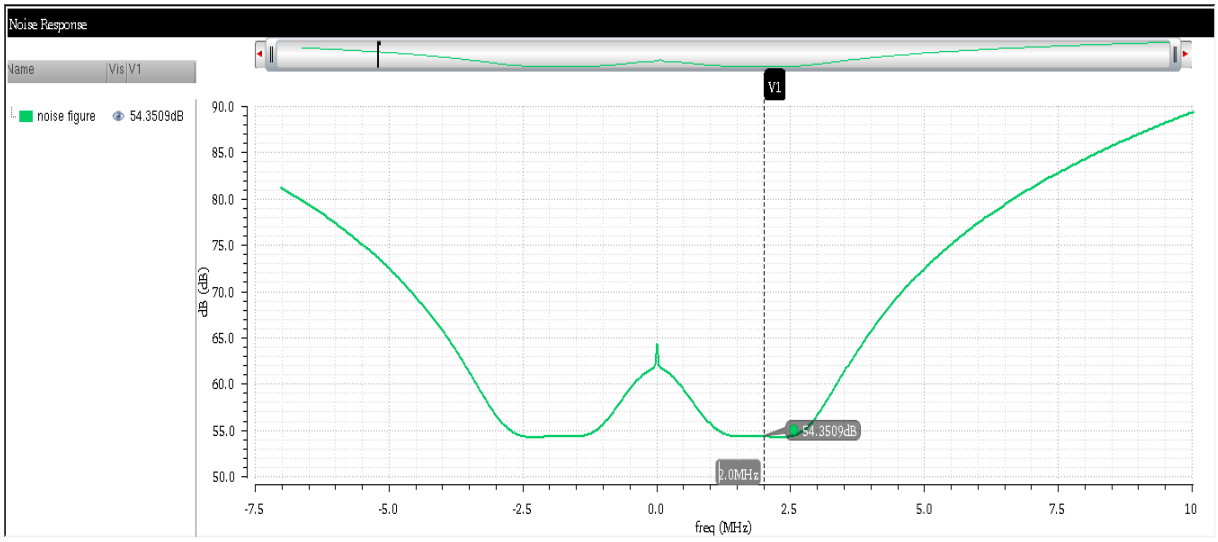


Figure 5–21: Noise Figure of the two-mega mode

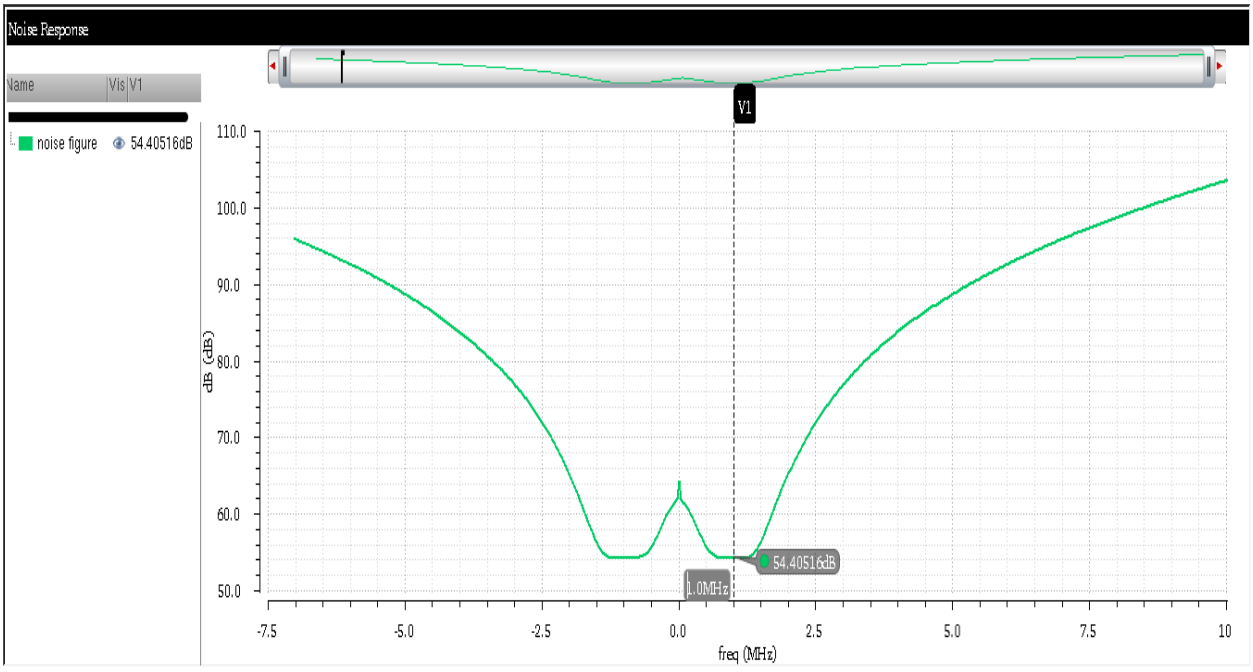


Figure 5–22: Noise Figure of the one-mega mode

5.6.3 Input impedance:

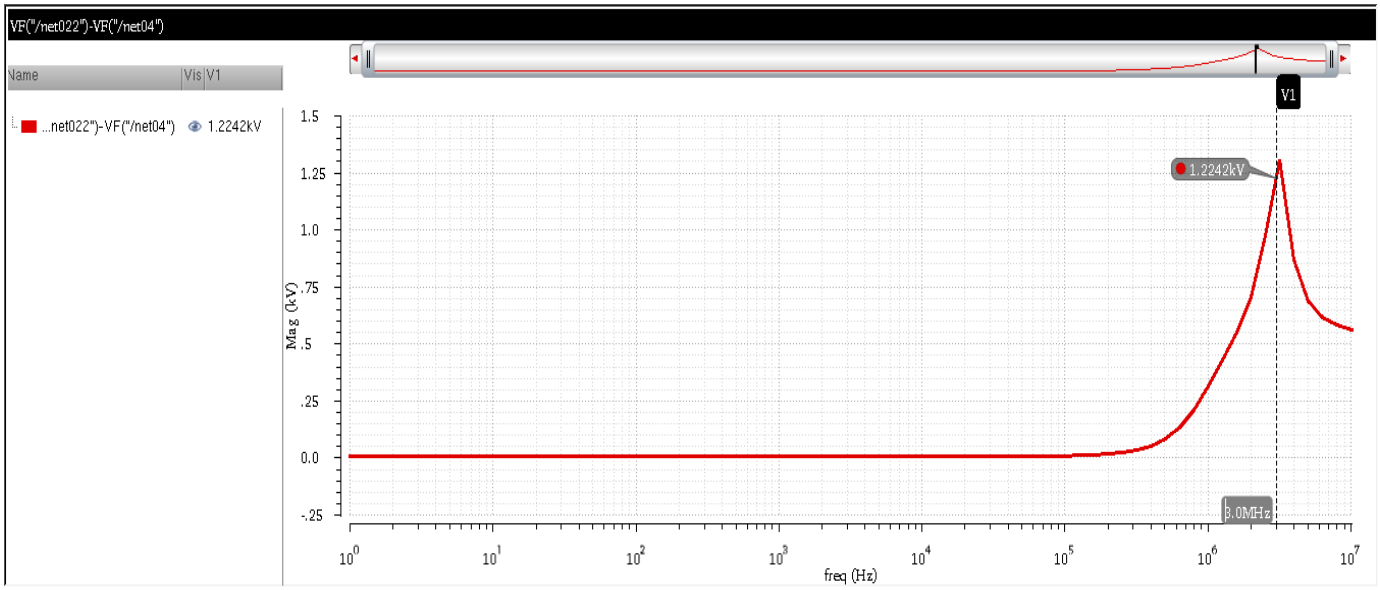


Figure 5–23: Typical Input impedance at two-mega mode

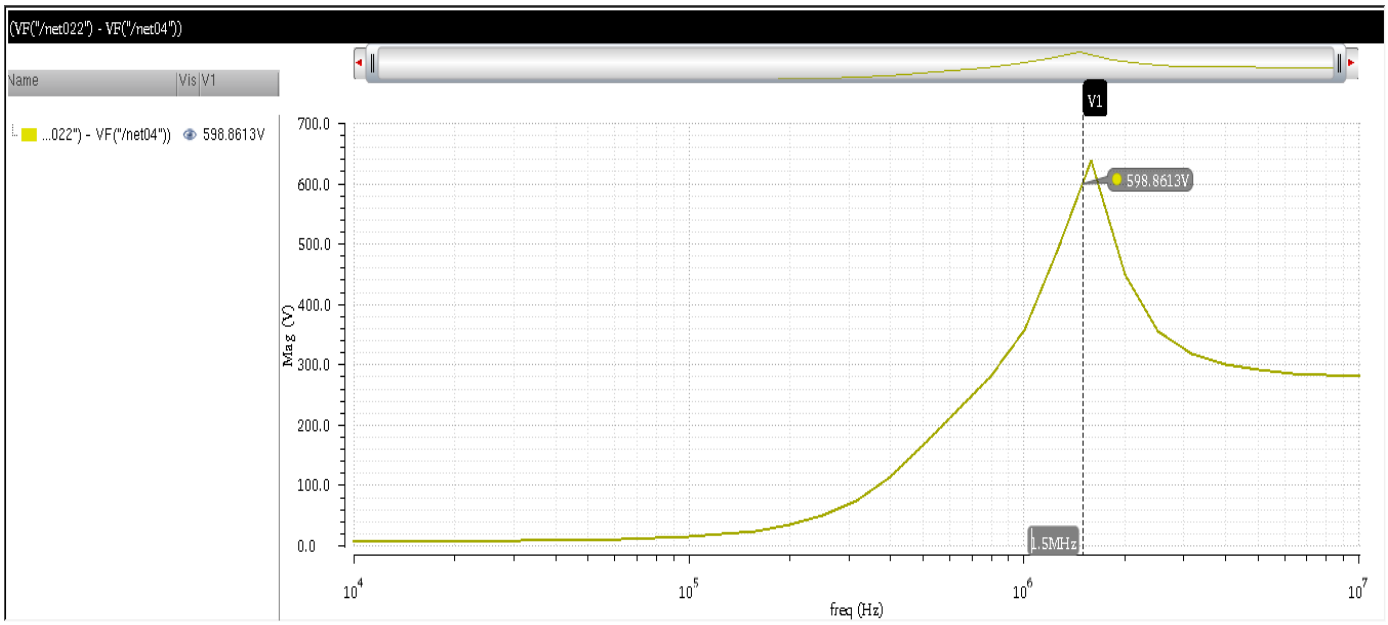


Figure 5–24: Typical input impedance at one-mega mode

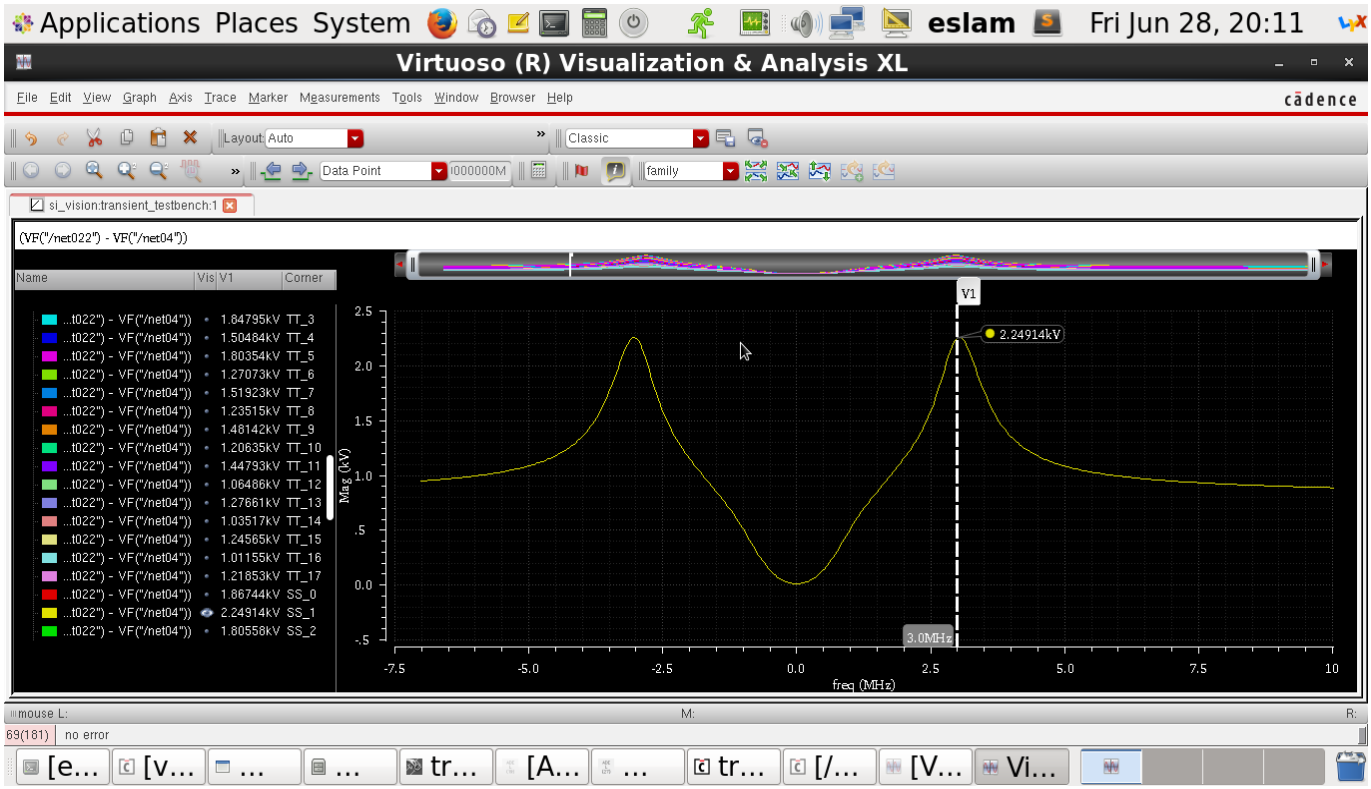


Figure 5–25: Input impedance of the two-mega mode under corners

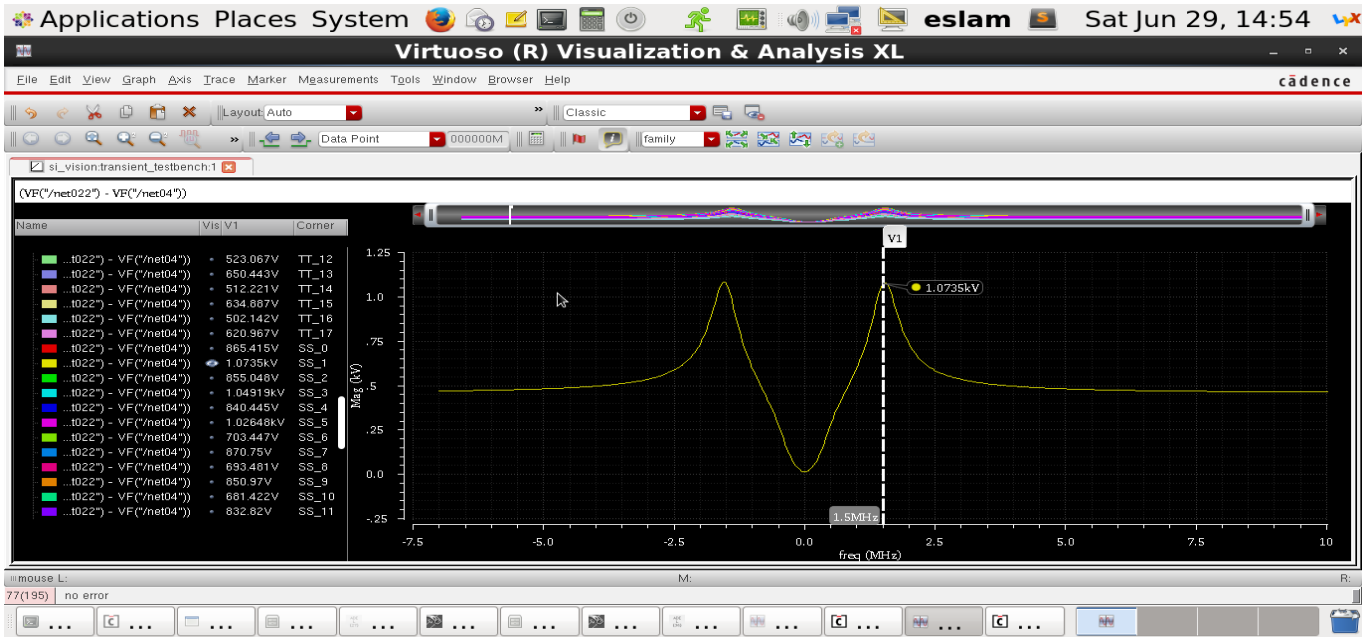


Figure 5–26: Input impedance of the one-mega mode across corners

5.6.4 Linearity tests:

The test bench used to measure the 1-dB compression point and the IIP_3 is shown in figure 5.20

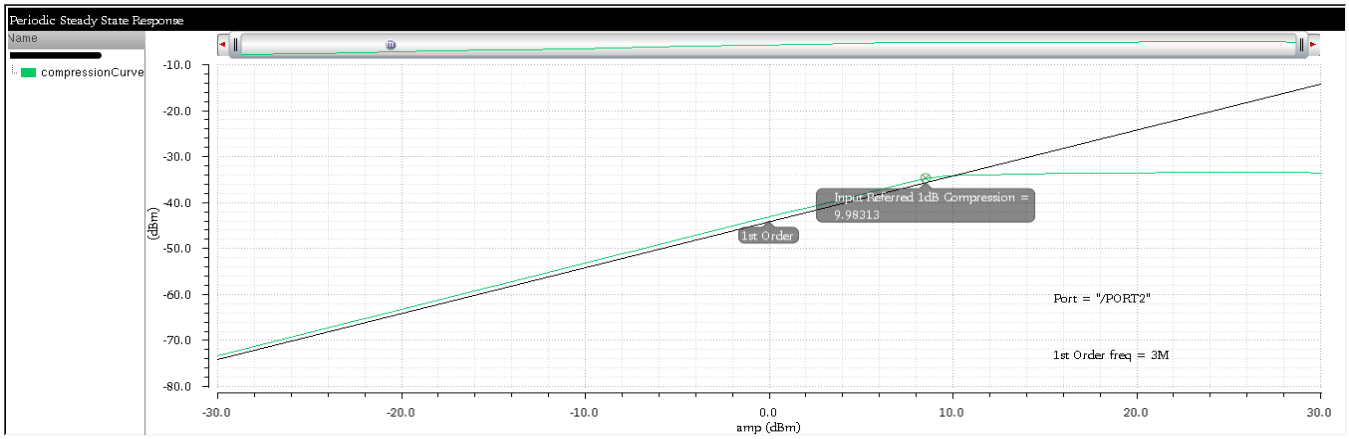


Figure 5–27: 1-dB compression point for the two-mega mode

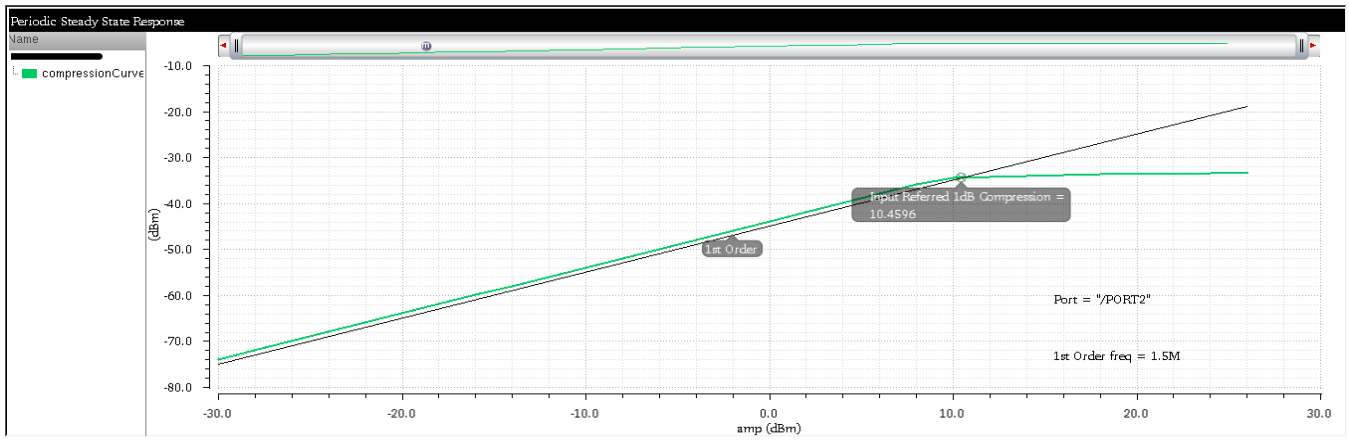


Figure 5–28: 1-dB compression point for the one-mega mode

When simulating the iip3 for the two-mega mode, a two tone test was made with a tone at 8MHz and a tone at 14 MHz so as their intermodulation will give a tone at 2MHz.

When simulating the iip3 for the one-mega mode, a two tone test was made with a tone at 4MHz and a tone at 7 MHz so as their intermodulation will give a tone at 1MHz.

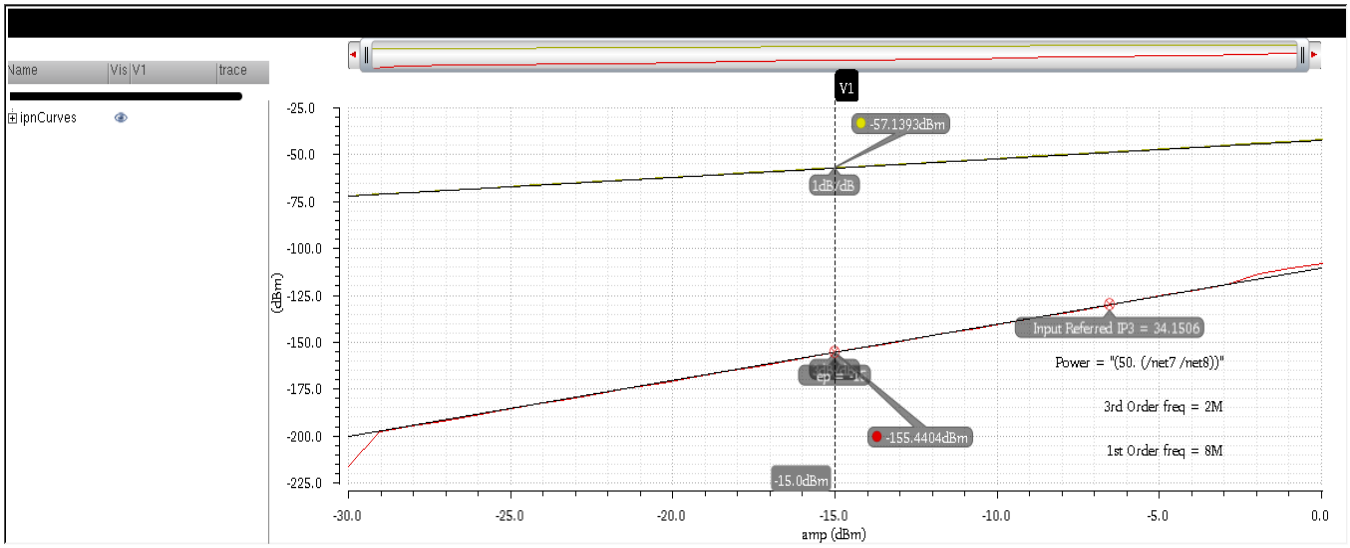


Figure 5–29: IIP3 of the two-mega mode

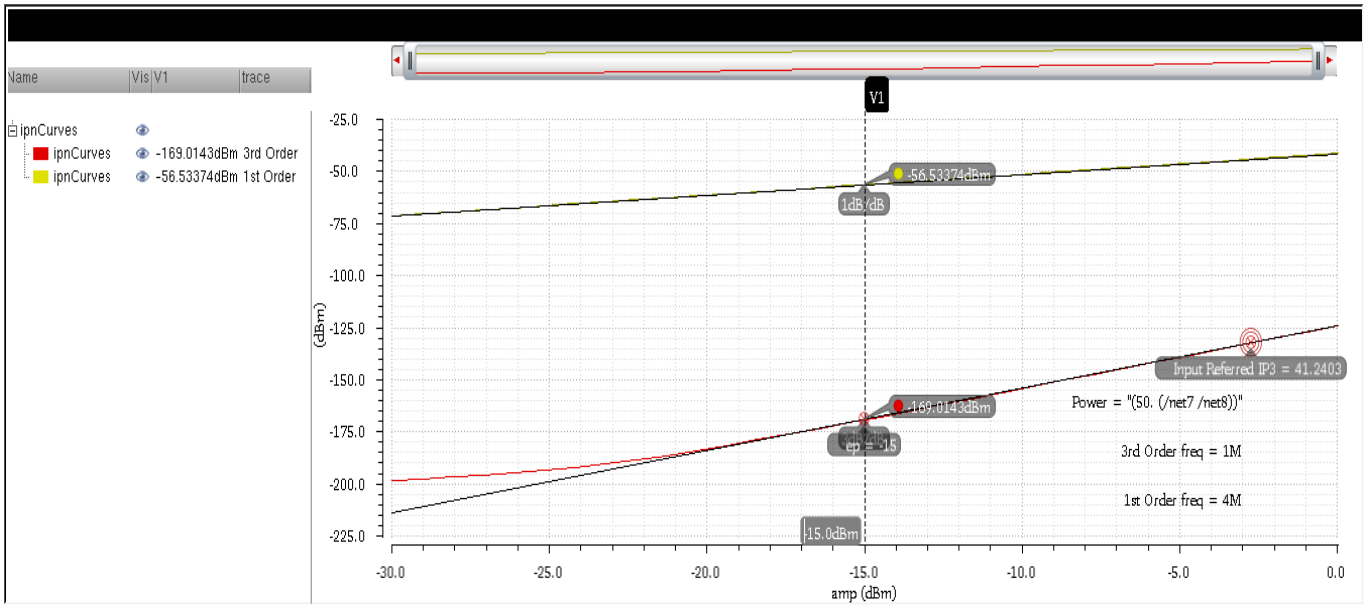


Figure 5–30: IIP3 of the one-mega mode

5.6.5 Transient Response:

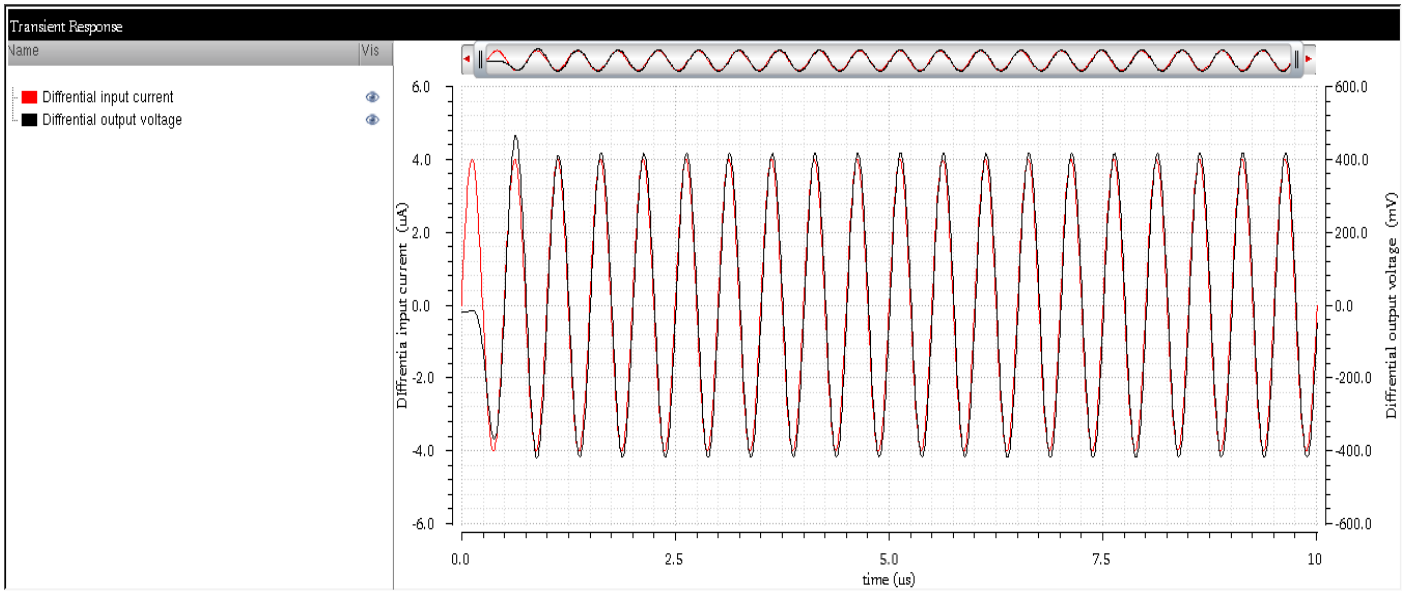


Figure 5–31: Transient response of the two-mega mode

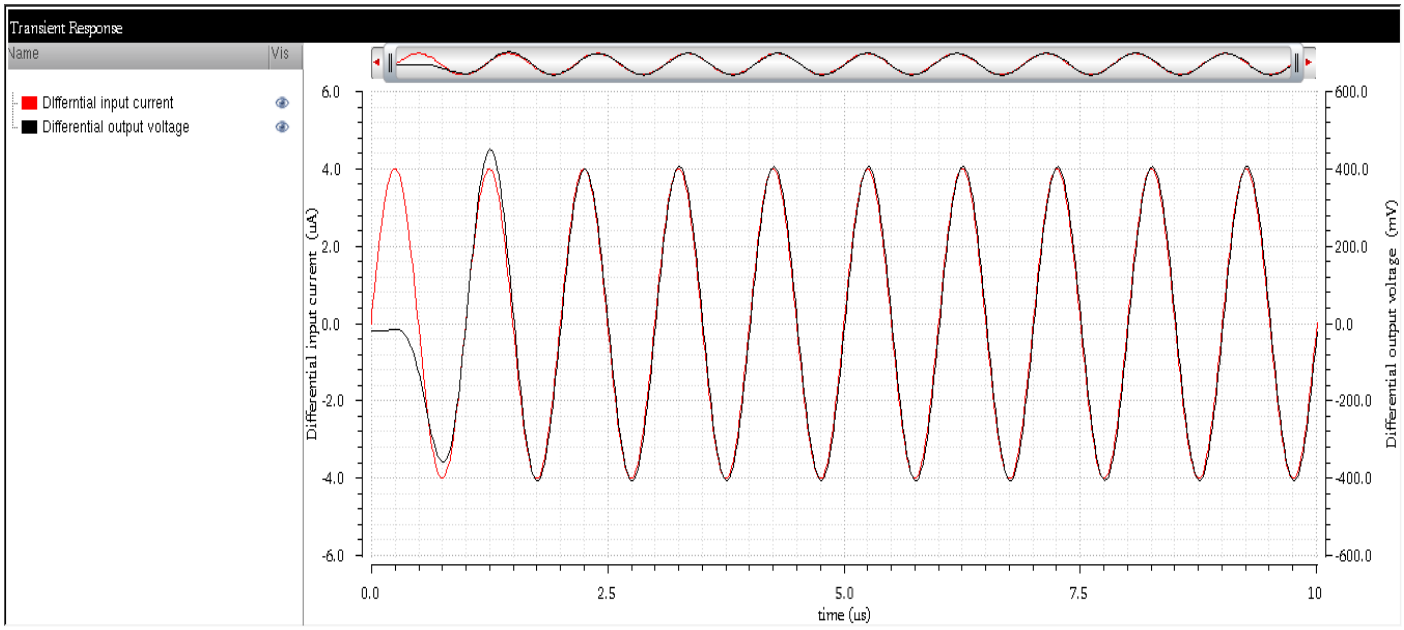


Figure 5–32: Transient response of the one-mega mode

5.6.6 AC response across Corners:

-Since there are 90 curves, I only showed the worst case for the two mega mode

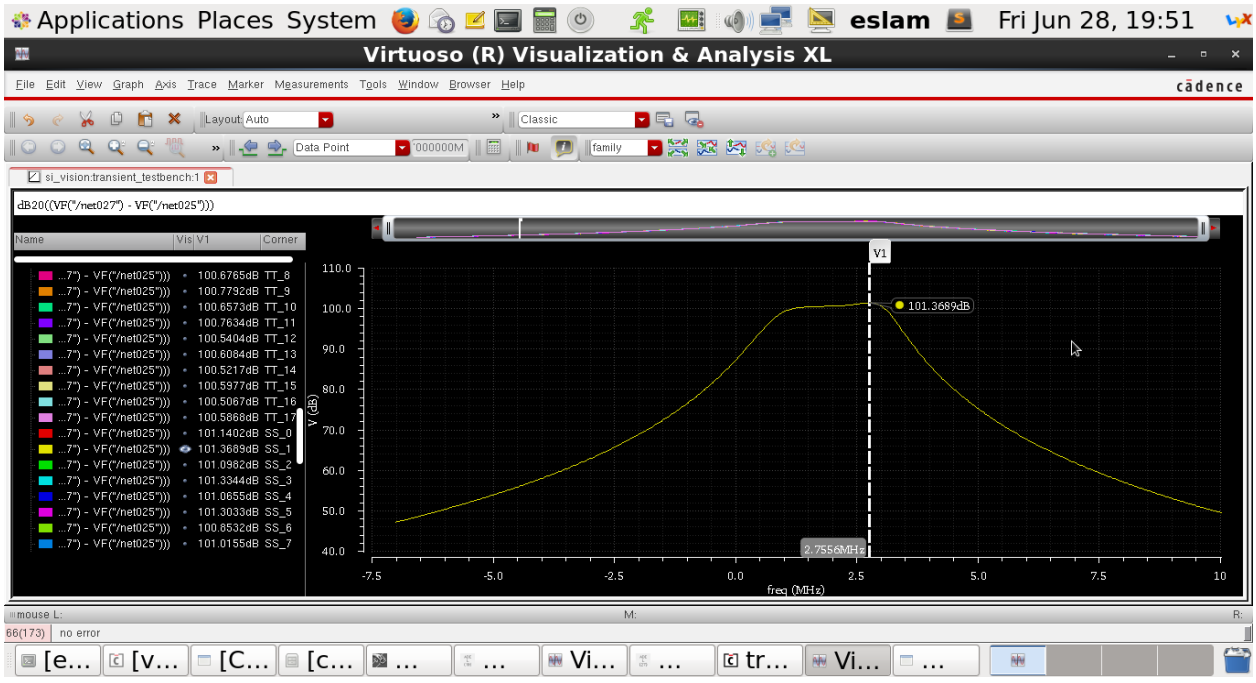


Figure 5–33: AC response of the two-mega mode across corners

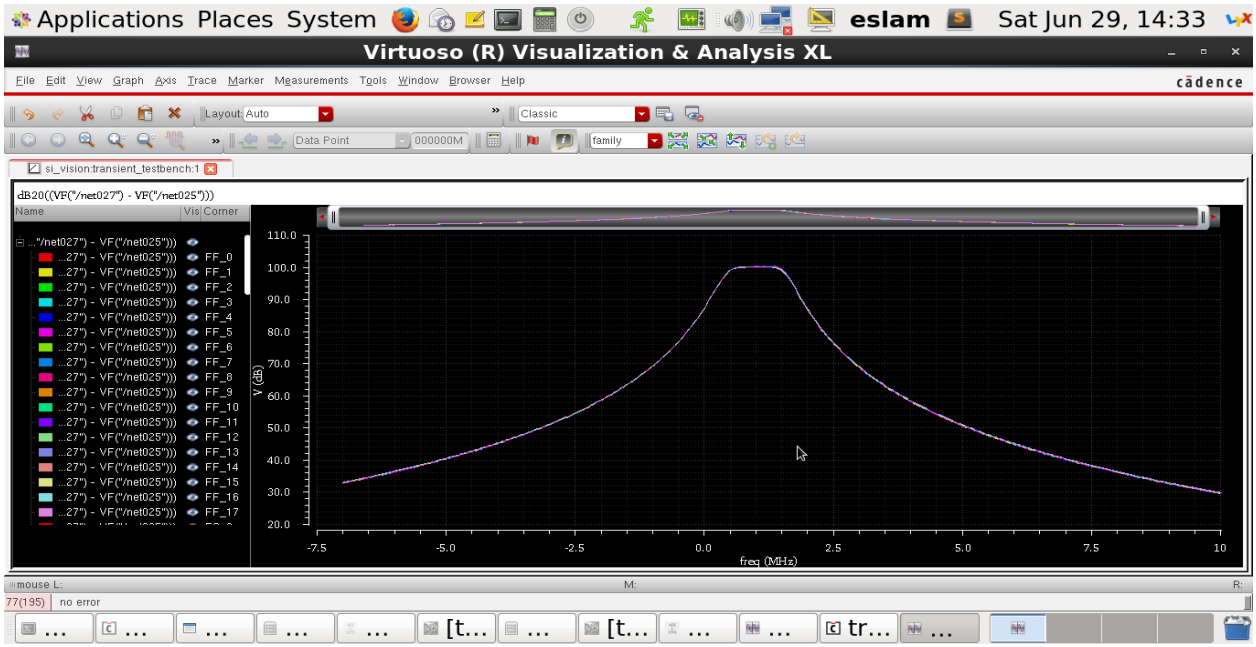


Figure 5–34: AC response of the one-mega mode across corners

5.7 Filter results summary

Spec.	Two-mega mode	One-mega mode
Bandwidth	2.03 MHz, (3.0821.0425MHz)	1 MHz (1.51-0.51MHz)
Transimpedance gain	100.3 dB	100 dB
Input Impedance	At 3MHz, 1.224 KΩ	At 1.5 MHz, 599 Ω
Noise Figure	54.3509 dB	54.4051 dB
1-dB compression point	9.98313 dBm	10.4596 dBm
IIP_3	55.239 dBm	62 dBm
Center frequency	2 MHz	1 MHz
Current consumption	1.3 mA	1.3 mA
Supply voltage	1 volt	1 volt

5.8 References

[1] D Li, Z Jing, Y Yang, X Wu, Z Shi, Y Liu, “Third-order active-RC complex filter with automatic frequency tuning for ZigBee transceiver applications” 2015

[2] “Analog Filters”, Dr. Ahmed Nader’s lecture notes, Cairo university, Giza, Egypt

[3] “Analog Filters”, Berkeley’s lecture notes

[4] Bluetooth/WLAN receiver design methodology and IC implementations, a PHD Dissertation by Ahmed ELAdawy Emira, Texas A&M university.

[5] Complex Signal Processing is Not Complex Dept. of Elect. and Comp. Engr., Univ. of Toronto, Toronto, ON Canada M5S 3G4,

6 Chapter 6: Received Signal Strength Indicator (RSSI) and Limiter.

6.1 Abstract

This chapter represents low voltage, low power Received Signal Strength Indicator (RSSI) and Limiter block for I and Q signals. The architecture is implemented using five stages limiter with total gain 61.38dB and overall bandwidth 6.2MHz. Each stage has 12.24dB voltage gain and 15.87MHz bandwidth. The implemented RSSI and limiter circuit in TSMC 65N CMOS technology consumes 406.2 µA with 1-V power supply. The RSSI output voltage is from 161mV to 662mV at low input power -50dBm over a dynamic range 45dB and the slope of RSSI curve is -11.075mV/dB.

6.2 Introduction

Nowadays, the received signal strength indicator becomes an essential building block in wireless transceiver. The RSSI can be used to adjust the gains of the RF front-end and baseband processors by measuring the power level of the received signal and indicates in it by certain voltage value which is RSSI output voltage value. The measured RSSI value affects the performance of the wireless communication systems as it travels using auxiliary ADC to digital base band receiver which returns a control signal to control total gain of the receiver. Also, RSSI used to adjust the transmitted power, monitor the link condition, manage the link setup and power down the receiver when there is no signal [3].

The signal strength must be measured and the total gain of the receiver must be adjusted as the higher gain of the receiver affects the linearity of the chain because of IIP3 inversely proportional with gain. So, when gain is increased, the linearity of the chain is decreased. On the other hand, the lower gain of the receiver lead to can't successfully receive the signals as SNR is affected. Total gain of the receiver inversely proportional with noise figure so in case of decreasing gain, noise figure is increased, so that SNR at the output of the receiver is decreased.

Bluetooth is one of the short-range transmission applications that uses GFSK modulation scheme with 80MHz bandwidth which is divided into channels. In this design of the receiver, there are two modes of operations. The first mode is 1Mbits/sec has a

bandwidth of received signal 1MHz and its IF down conversion is 1MHz. The second mode is 2Mbits/sec has a bandwidth 2MHz and its IF down conversion is 2MHz. So that RSSI should work correctly with two modes of operations. Since the data information is embedded in the carrier frequency shift no linear amplification function is needed, then using Limiter amplifier that amplifies the small input signal into a saturated level before deliver it to digital base band receiver to demodulate it. Then this design of the receiver is limiter based not ADC based because limiter is considered as one-bit ADC for Wireless low-IF GFSK Bluetooth receiver. Limiting amplifier rather than an AGC is widely employed in wireless IF because it can handle a larger dynamic range while consuming less power with simple circuitry. AGC is a closed loop structure while limiting amplifier is open loop [1],[3].

6.3 Description of RSSI and Limiter Block

The RSSI circuit based on the successive detection architecture method to realize the logarithmic transfer function as the wide dynamic variation of the received signal can be represented within a limited indication voltage range. The need of limited indication range for RSSI value is coming from low voltage supply. By using the successive detection architecture, the RSSI circuit approximates a logarithmic function in a piecewise linear manner.

As shown in the fig.6.1, the RSSI circuit based on the successive detection architecture consists of cascading (N) stages of Limiting Amplifier cell which has a voltage gain (A_s), (N+1) full wave rectifier (FWR) or peak detector (DET) circuit. FWR circuit converts output voltage of the Limiting Amplifier to full wave current then the summation and average value are taken by RC-LPF. This average value represents the RSSI value.

The cut off frequency of this filter should be much smaller than the frequency of the received signal to achieve very small ripples in RSSI output value.

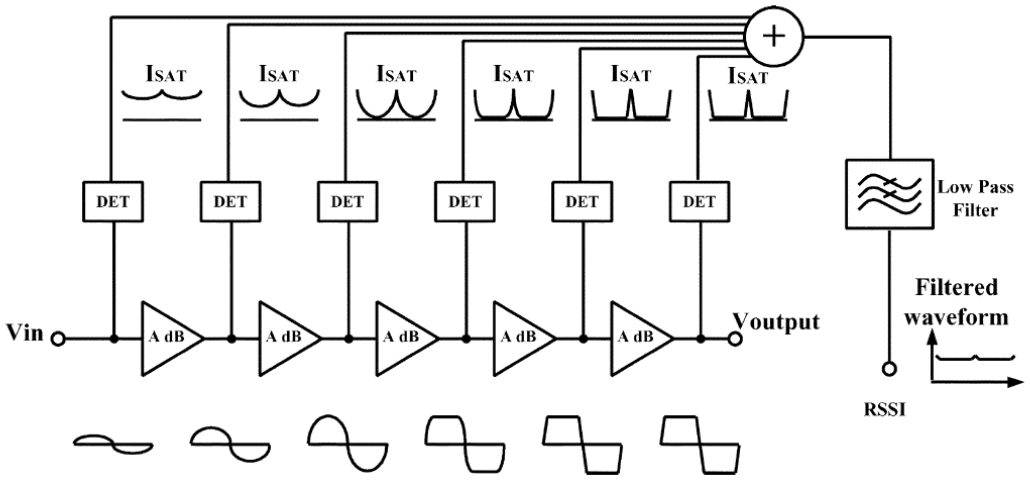


Figure 6–1: RSSI Block Diagram

As RSSI mainly consists of cascaded stages of Limiting Amplifier which saturates the received signal at certain level voltage thus a one-bit ADC (limiter) can be made from this gain stages to deliver signal to digital base band receiver. So that there are two paths of this block which are RRSI path and limiter path. First path outputs the RSSI value that indicates the power level of the signal which is an ADC input and the second path outputs a square wave which is the received signal saturated by Limiter inputs to digital receiver.

6.4 Design Consideration

6.4.1 Limiting Amplifier

The parameters of the limiting amplifier that determine optimal overall performance will be introduced briefly. These parameters are number of limiting amplifier stages (N), gain of limiting amplifier (As) and total gain of N stages of amplifier (At), bandwidth of limiting amplifier (fs) and overall bandwidth of the block (ft). The selection of number of stages is a trade-off between gain per stage, bandwidth per stage and power consumption. As number of stages increased, gain per stage decreased to achieve certain total gain, there will introduce a greater number of poles so, to achieve certain overall bandwidth of the block, bandwidth per stage has to be increased as shown in the fig.6.2. Power consumption is one of the most important parameters in currently wireless

transceiver and in limiter when the number of stages increase, power consumption increases linearly [1]. The effects of each parameter are shown in the following equations:

- $A_s = A_t^{(1/N)}$ (6.1)
- $f_s = \frac{f_t}{\sqrt{2^{(1/N)}-1}}$ (6.2)
- $GBW = \frac{gm}{c} \propto \sqrt{I_d} \propto \sqrt{\frac{P}{V_{dd}}}$ (6.3)
- $P_t = N.P_s \propto N.(GBW)^2$ (6.4)

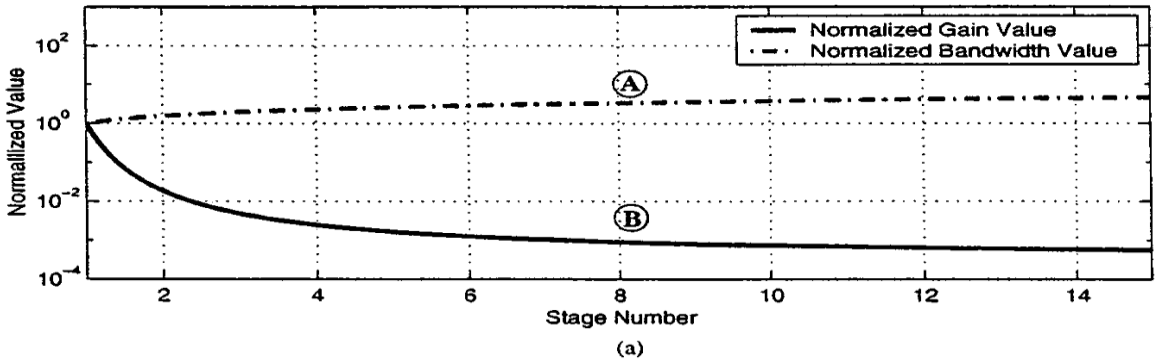


Figure 6–2: Trade-off between gain and bandwidth of the limiting amplifier.

6.4.2 RSSI Parameters and Calculations

There are three parameters that defines performance matrics of the RSSI block. These paraments will be highlighted. In addition to the calculations and trade-offs in designing RSSI which include N stages of limiting amplifier. Some considerations are taken in the calculations like:

1. The input signal is narrow band modulated signal so it can be considered as a single tone sine wave which is $V_I \sin(wt)$.

2. Each limiting amplifier stage has voltage gain A and saturate the received signal to voltage level V_s.

3. Each rectifiers outputs the absolute value of its input signal without any losses.

4. LPF which summed the output currents of FWR stages and averaged it to get a DC value with some ripples indicates to power level of the signal, consider its output as only DC voltage without any ripples.

5. Summer has the same weighting value for each branch of FWR [2].

6.4.2.1 RSSI Value

Ideally RSSI value is a logarithmic function of the amplitude of the input signal (V_I). However, in the RSSI block where it used the successive detection method, the RSSI value is obtained by summing the output of each branch as shown in equation (6.5).

$$RSSI\ (V_I) = \sum_{i=0}^{N} X_i(V_I) \qquad (6.5)$$

where N is the number of stages of the limiter and $X_i(V_I)$ is the output voltage of each branch.

$X_i(V_I)$ depends of the value of ($A^i * V_I$) , so it represented in two different ways:

1. If ($A^i * V_I$) $< V_s$, as shown in fig.6.3(a), this means signals not saturated and we can get average value of the output from the rectifier as shown:

$$X_i(V_I) = \frac{1}{T}\int_0^T \left|A^i * V_I \sin(Wt)\right| dt = \frac{2}{\pi} A^i * V_I \qquad (6.6)$$

2. If ($A^i * V_I$) $\geq V_s$, as shown in fig.6.3(b), this means output signal saturated in some time of the period of sin wave. So it can be calculated as shown:

$$X_i(V_I) = \frac{4}{T}\int_0^{\Delta T_i}\left|A^i * V_I \sin(Wt)\right| dt + \frac{4}{T}\int_{\Delta T_i}^{T/4} V_s = \frac{2}{\pi} A^i * V_I \left(1 - \sqrt{1 - \left(\frac{V_s}{A^i * V_I}\right)^2}\right) + \left(1 - \frac{2}{\pi}\sin^{-1}\left(\frac{V_s}{A^i * V_I}\right)\right) * V_s \qquad (6.7)$$

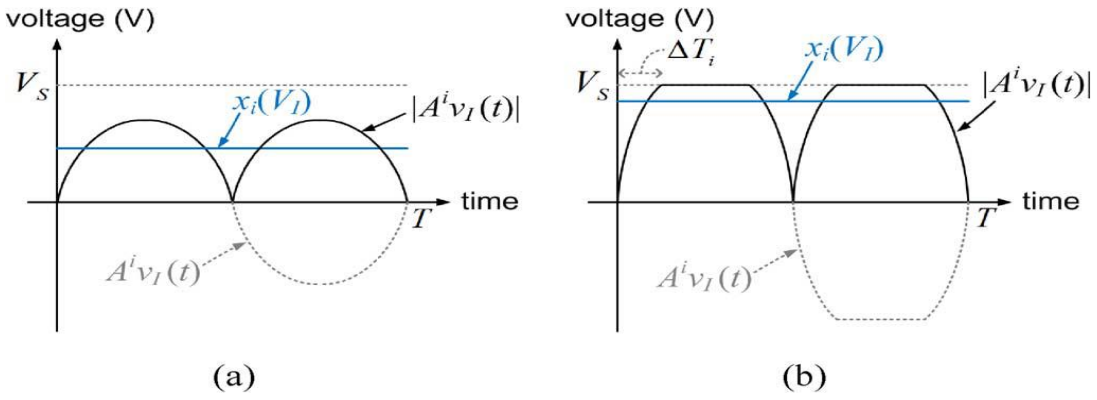


Figure 6–3 : (a) Output of the rectifier if signal not saturated (b) Output of the rectifier if signal saturated

6.4.2.2 RSSI Error

RSSI error is defined as the difference between two curves which are the ideal logarithmic RSSI curve and the piecewise linear approximation curve which is output from the RSSI block as shown in fig6.4.

RSSI error is dependent only on the voltage gain of a limiting amplifier such that gain increased error increased too. So that the number of the stages is increased in order to decrease gain per stage to get the required error. On the other hand, increasing number of gain stages decreasing the overall bandwidth so to compensate this more power consumption is needed to increase bandwidth per stage [2].

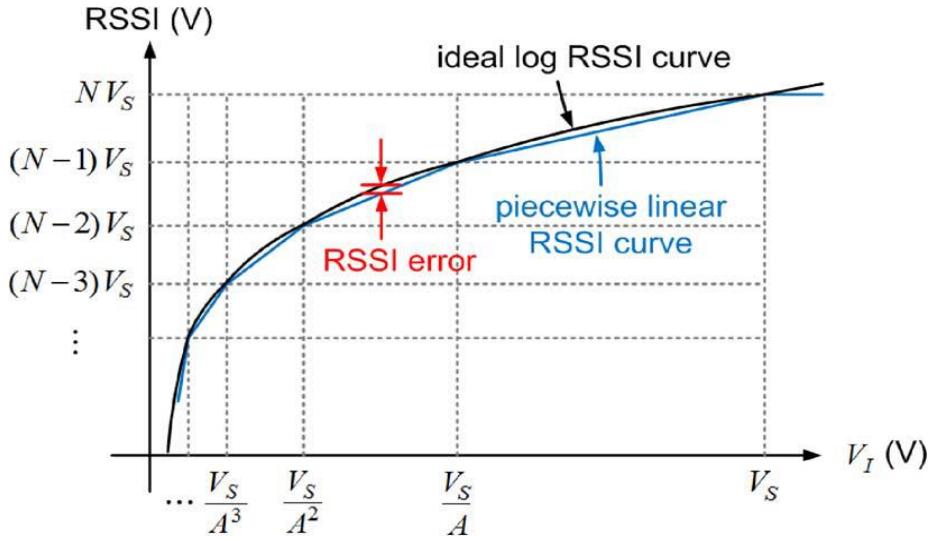


Figure 6–4 : Definition of RSSI error

6.4.2.3 RSSI Dynamic Range

RSSI dynamic range is defined as the maximum input signal range where the RSSI error is kept less than certain value as shown in fig.6.5 [2]. As discussed before according to error and its relation with gain per stage, it can be concluded that when error increased, the dynamic range is decreased as its defined for certain error. Dynamic range is dependent not only on the gain per stage but also on the number of stages too. As number to stages defined total gain and gain per stage.

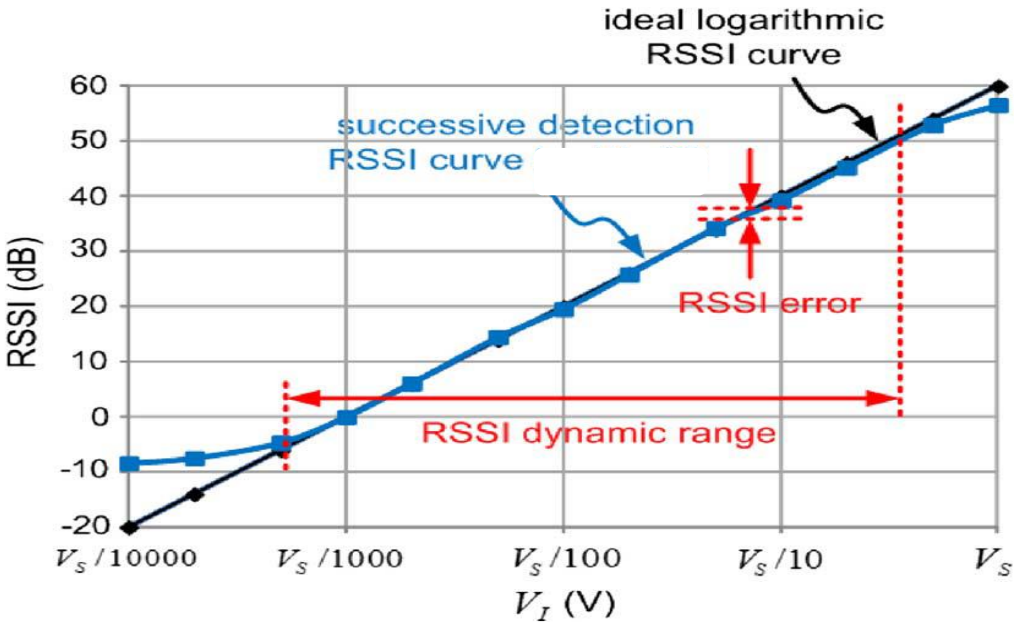


Figure 6–5 : RSSI dynamic range within certain error

6.5 Simulation of RSSI Model

According to the pervious discussion of the design consideration, the need to determine number of stages, voltage gain and bandwidth per stage to achieved the required error and dynamic range is the important part in the design of RSSI block. So that before design the RSSI block from its fundamental block using transistor level, it should be implemented first as an ideal block and simulated to determined the important parameter needed for design its circuit.

RSSI model is implemented from ideal components represented the two main blocks of it. Limiting amplifier is implemented using voltage-controlled voltage source (VCVS) has certain gain (A) and defined its bandwidth using RC filter at the output of

VCVS. The input signal is differential so output signals are taken from positive and negative terminal of VCVS. To implement FWR, it is needed to convert signal to full wave (all wave should be positive) so that it is used absolute component to do this then convert voltage signal to current signal using voltage controlled current source (VCCS) and finally summed current signals from all branches by RC filter. The entered signal to RSSI block composed of I and Q signals. So that to be able to compute level power of the signal, the I and Q branches is used and summed as shown in fig.6.6.

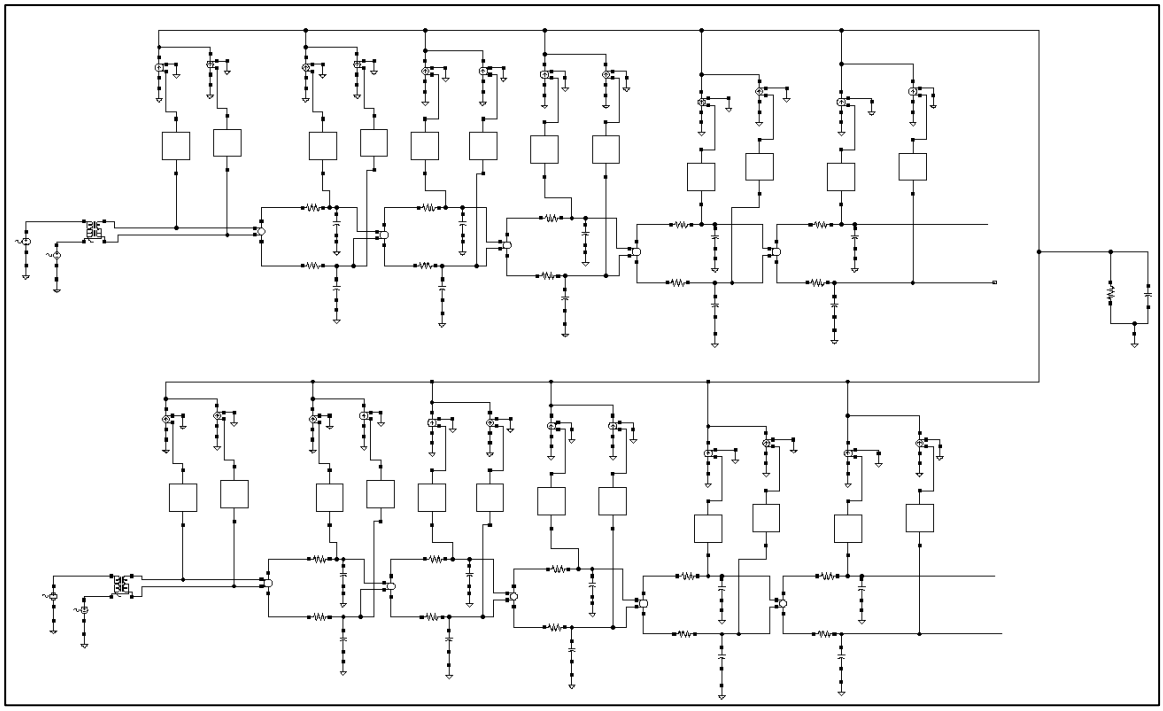


Figure 6–6 : Implementation of RSSI Model

As shown in fig.6.6, the simulation of RSSI Model is done to achieve dynamic range from -50dBm to -5dBm (45dB dynamic range) within error $\pm 1dB$. The number of stages is concluded from the simulation to be five stages from limiting amplifier and six stages from FWR. Each limiting amplifier has voltage gain equals to 4 v/v $\sim 12\ dB$. To achieve bandwidth greater than 3MHz in this model the limiting amplifier is considered to have bandwidth 13.263MHz and overall bandwidth is calculated from equation (6.2) is 5.11MHz.

Fig.6.7 shows the RSSI model output curve and compared with ideal straight line which represents the ideal logarithmic curve to calculate RSSI error and it is straight line as x axis in dBm. Fig.6.8 shows error of RSSI model and indicates that the achieved

dynamic range from -60.21dBm to -2.72dbm equals to 57.49dB and it is greater than the required.

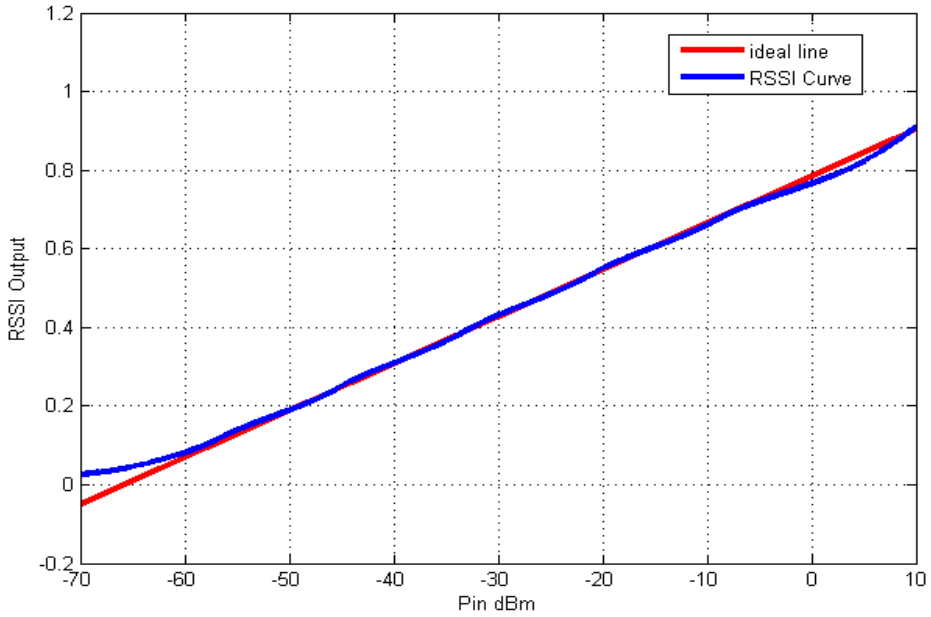


Figure 6–7 : RSSI output from the model simulation

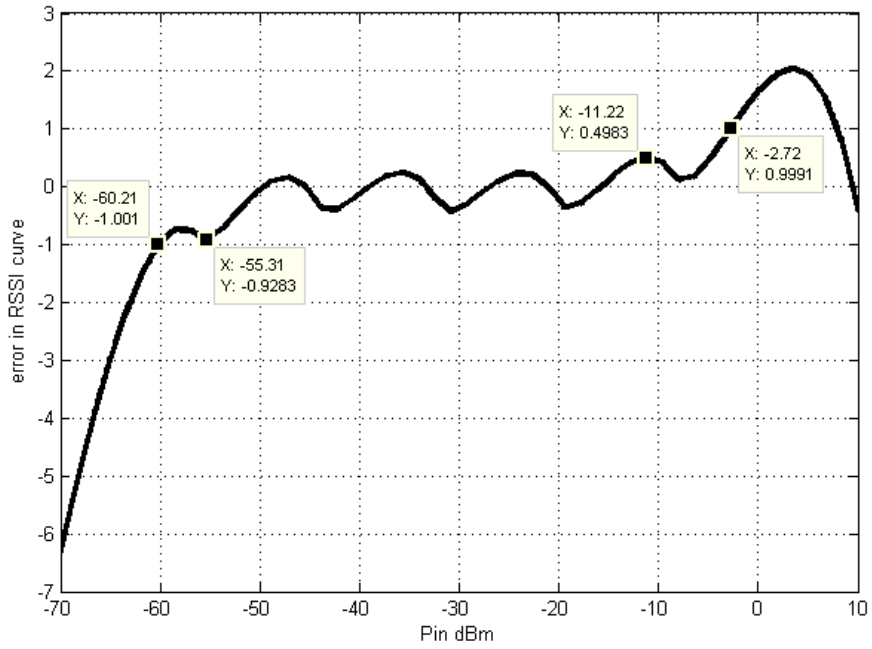


Figure 6–8 : Error of RSSI output of the model

6.6 RSSI Circuits Design and Results

Before going deep in explaining the different circuits composed the RSSI block, first needing to know that in this block there are two paths as discussed before path for RSSI output value to ADC and another path for the desired received signal to be limited to Vdd and ground which is one and zero to digital base band receiver. So that this block consists of five stages of limiting amplifier which is differential input and differential output, six stages of FWR differential input voltage and single-ended output current and RC-LPF at the output of RSSI path. In addition to another amplifier stage which is differential input and single ended and finally an inverter at the output of limiter path. This all is repeated for I signal and Q signal as shown in fig.6.9.

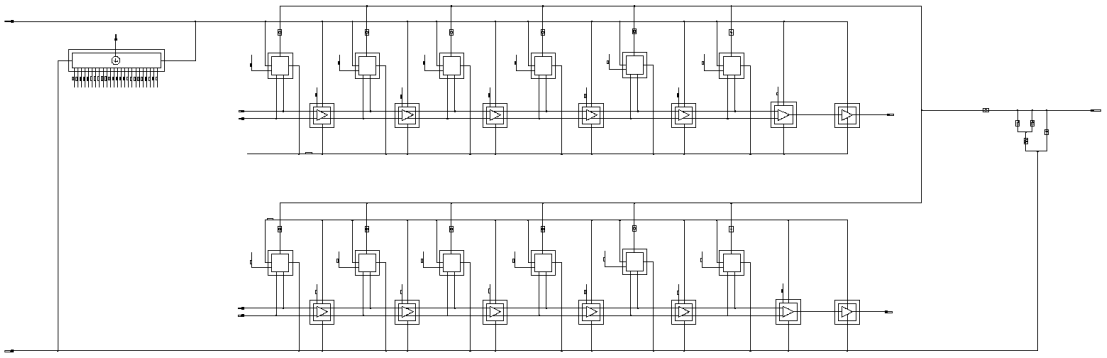


Figure 6–9: The designed RSSI block

6.6.1 Limiting Amplifier

6.6.1.1 Circuit Design

As shown in fig.6.10, the limiting amplifier consists of three main parts. The first part is the main core amplifier which is differential input pair NMOS transistors M_5 , M_6 biased using current source M_4 , mirrored from M_1 and in parallel there are diode connected transistors M_7 , M_8.The voltage gain of this circuit is as shown in equation (6.8). The difference between the circuit is used in this design and is used in [1] is the diode connected transistors which folded to ground as loads in [1], but in this design they biased like M_5 , M_6. The difference is made to enhance circuit behavior across corners thus achieving less gain variations across temperature, voltage supply and process variations. This occurs because of g_{m6} and g_{m7} can track each other across corners if they flow the

same current per multiplier from the same source but the difference is only in the ratio between their currents, the same as for transistors size they must have the same length and width per multiplier and the difference is only in the number of multiplier. So, they can get the latest variations across corner rather than in [1] which diode connected flow current from PMOS source which they M_9 , M_{10} so they have larger variations. The circuit in [1], its output node voltage is defined by diode connected but in this design the output common mode is not defined because of $V_{ds}\ of\ M_3$. So, there is a need to a common mode feedback circuit (CMFB).

$$A_v = \frac{g_{m6}}{g_{m7}} = \sqrt{\frac{\left(\frac{W}{L}\right)_6 * I_{D6}}{\left(\frac{W}{L}\right)_7 * I_{D7}}} \qquad (6.8)$$

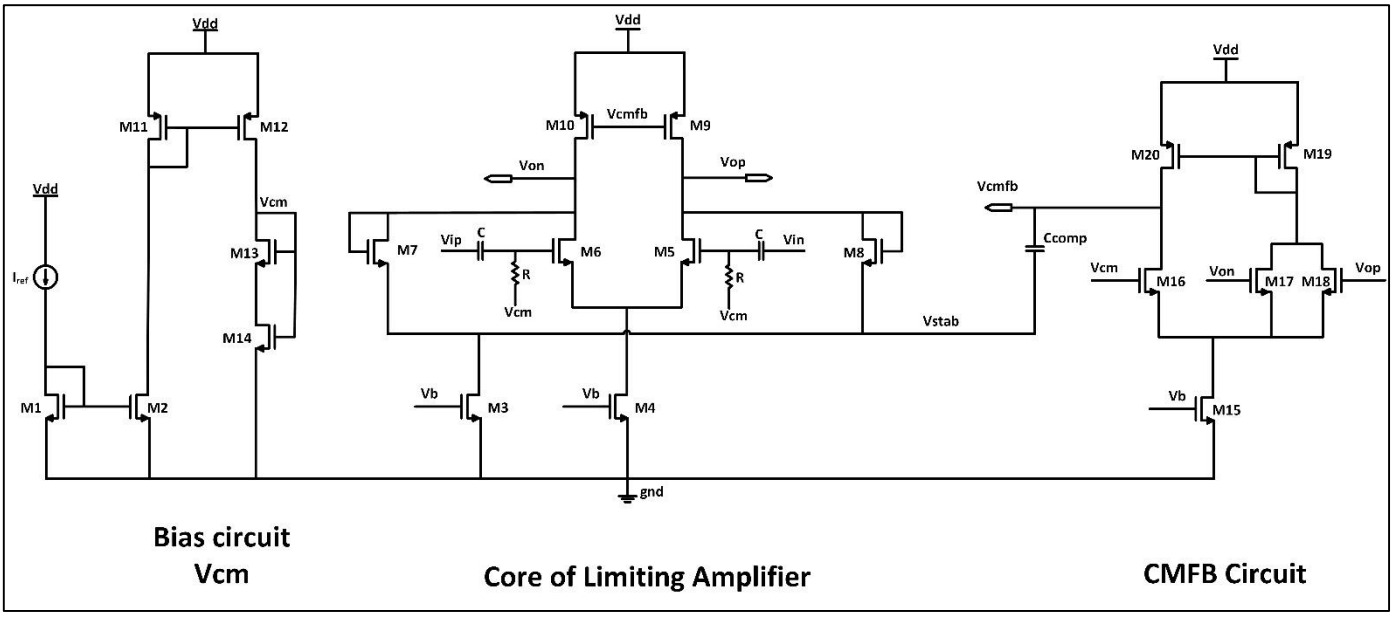


Figure 6–10 : The desired circuit of limiting amplifier

The second part of the fig.6.10 is a CMFB circuit. The Common-mode feedback circuits (CMFB) stabilize common-mode voltages for fully-differential analog systems by means of adjusting the common-mode output currents. The CMFB circuit is an op-amp with high loop gain to stabilize two differential output to the same voltage [8]. The two differential output voltages are averaged using two differential pair NMOS transistors M_{17} ,M_{18} and compared with the common-mode reference voltage (Vcm) which is the input voltage to M_{16} , and the differential voltage is converted to the common-mode output current to adjust the current of PMOS transistors M_9 , M_{10}.

By using CMFB circuit, it is leaded that there is a closed loop feedback, so the checking of stability is an important test should be done. In this design there are two poles. The first one is at output node of core of limiting amplifier which is $\frac{g_{m7}}{C_{parasitic}}$ and the second one is at output node of CMFB circuit which is V_{cmfb} and equals to $\frac{1}{(r_{on}//\, r_{op})*C_{parasitic}}$ .So that miller compensation is used by a capacitor at the output node of CMFB circuit (C_{comp}) which equals to 820fF. Using this capacitor one of two poles is become a dominant pole at low frequency and the other is a non-dominant pole at higher frequency. So that, it enhances the phase margin of the feedback system. The stability test of this circuit outputs loop gain is 60.1278dB, gain margin is 27.99dB at 96.82MHz and phase margin is 97.97℃ at 3.769MHz as shown in fig.6.11.

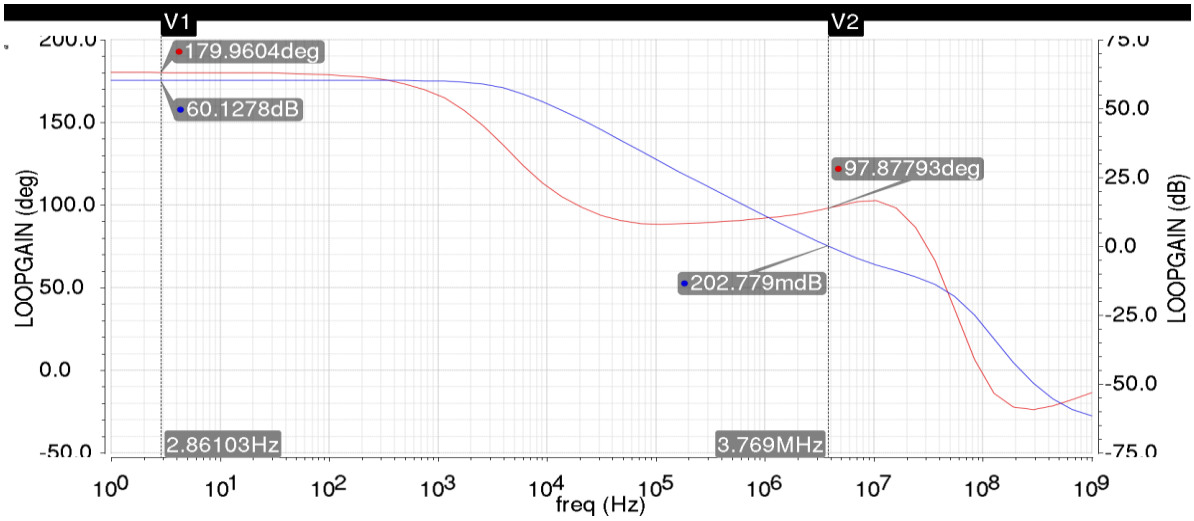


Figure 6–11: Loop gain and phase gain of the limiting amplifier circuit

The third part of the circuit of limiting amplifier is biasing circuit. Before talking about the function of this part lets talk about dc offset and ways for cancellation. Dc offset can be introduced from any mismatch in the devices of limiting amplifier circuit and very small offset can propagate from one stage to another and experiences large gain [4]. So, it may be large enough to saturate limiting amplifier which indicates the wrong results output from RSSI path. So that dc offset has to be canceled. There are traditional dynamic ways to cancel the dc offset such as auto zeroing. Auto zeroing technique uses component to store and cancel or reduce offset by using capacitors at input or at output [9]. The main disadvantages of this technique are that they require a clock signal and a calibration period. The calibration period would reduce the overall speed and prevent the amplifier to

operate in a continuous time way. There are two ways to cancel offset in continuous manner such as feedback offset cancellation and feedforward offset cancellation [4],[5]. The feedback offset cancellation is an input referred offset cancellation and it is a closed loop system that extracts dc from output signal of the last stage using LPF and feedback it to the input of the first stage and subtract it from input. So that it may suffer from stability problem as number of stages increased. On the other hand, feedforward offset cancellation it cancels the propagation of dc offset from stage to another stage using dc blocking capacitor and using resistor for biasing the circuit of the amplifier, this technique which is used in this design by RC at the input of differential input transistor M_9 , M_{10} shown in fig.5.10. So that there is a biasing circuit outputs common mode voltage to bias core of limiting amplifier. This RC filter is a high pass filter for the received signal which has low corner frequency, it should be less than 0.5MHz because it is a minimum frequency of the received signal in mode 1Mbits/sec. So that the resistor and capacitor have large values and occupies large area. Resistor is 2MΩ, capacitor is 4pf to achieve low cut-off frequency.

6.6.1.2 Results of Limiting Amplifier

Limiting amplifier has gain equals to 12.2394dB (4.092 V/V) and bandwidth equals to 15.8748MHz for each stage as shown in the fig.6.12. For the last stage which is the fifth stage of Limiter gain total is 61.38136dB and overall bandwidth is 6.2086MHz as shown in fig.6.13. Minimum frequency of the amplifier stages is less than 0.5MHz which is the minimum bandwidth of the received signal as mentioned above and also maximum frequency of them is greater than 3MHz that represent maximum bandwidth of the received signal when the receiver in mode 2Mbits/sec.

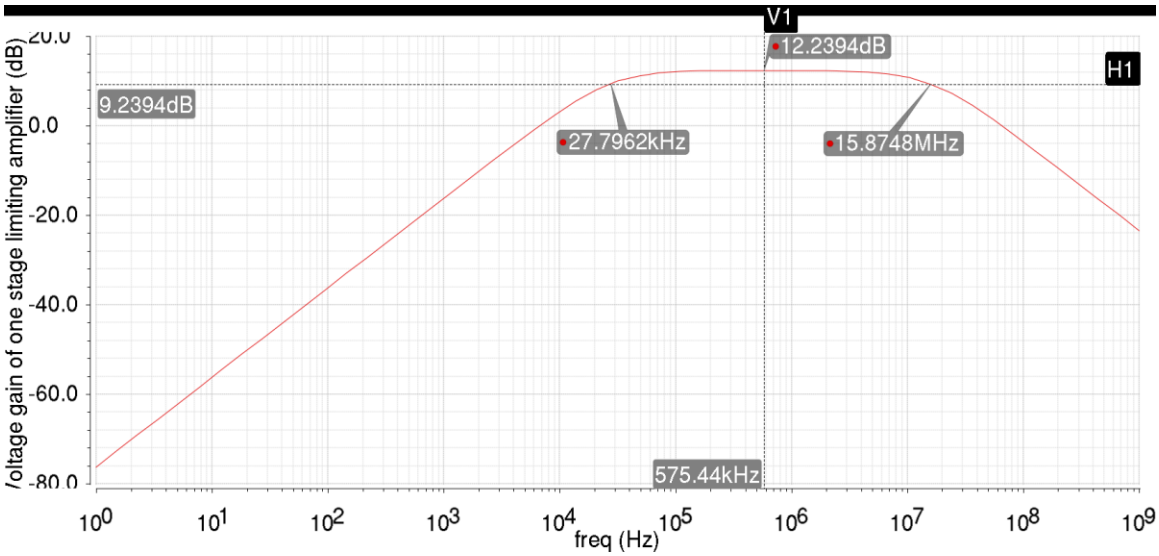


Figure 6–12: Voltage gain of one stage limiting amplifier

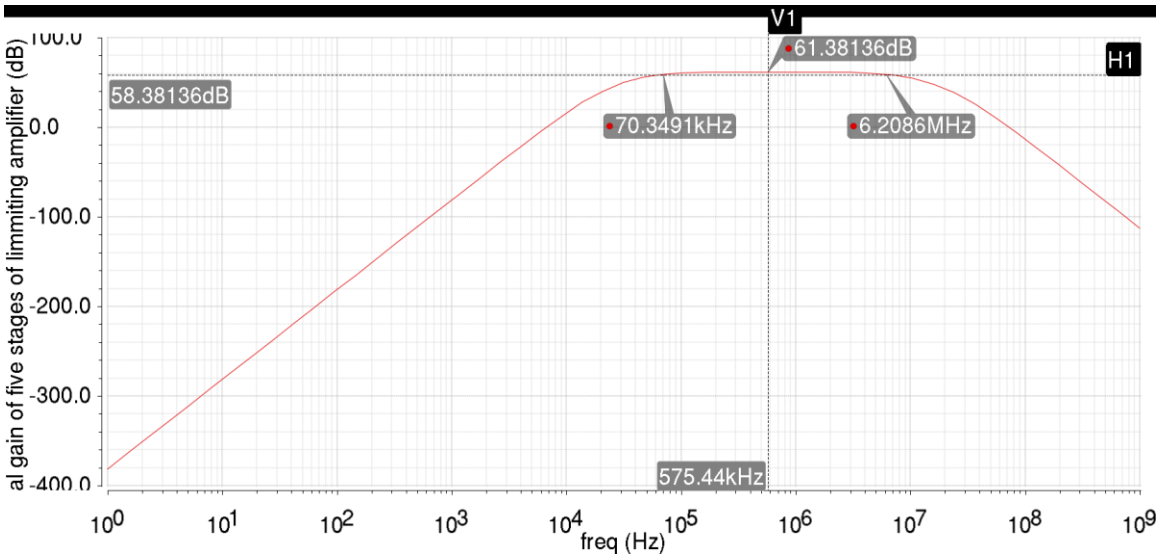


Figure 6–13: Total voltage gain of five stages of limiting amplifier

For each stage of limiter, gain variations with temperature, voltage supply and process variations should be as small as possible to achieve the final RSSI output has small variations too. The corners which are run are all the combinations from process variations of CMOS transistors (ss, ff, sf, fs), process variations of resistors and capacitors (ss, ff), voltage supply variations ($1V \pm 50mV$) and temperature variations from ($-40℃$) to ($125℃$). As shown in fig.6.14, the worst case low in gain of one stage is occurred at (ss MOS, ff res, ff cap, 0.95V, $125℃$). On the other hand, the worst case for high gain is occurred at (ss MOS, ss res, ss cap, 1.05V, $-40℃$), the variation in the gain at 1MHz is $\pm\ 0.402535dB$ and 2MHz is $\pm\ 0.403085dB$ they are almost same. For the last stage across

corners variations 0.5MHz and 3MHz are within bandwidth of limiter which is satisfied the two mode of operations of the Bluetooth receiver as shown in fig.6.15. This means in two modes of operations limiting amplifier works correctly.

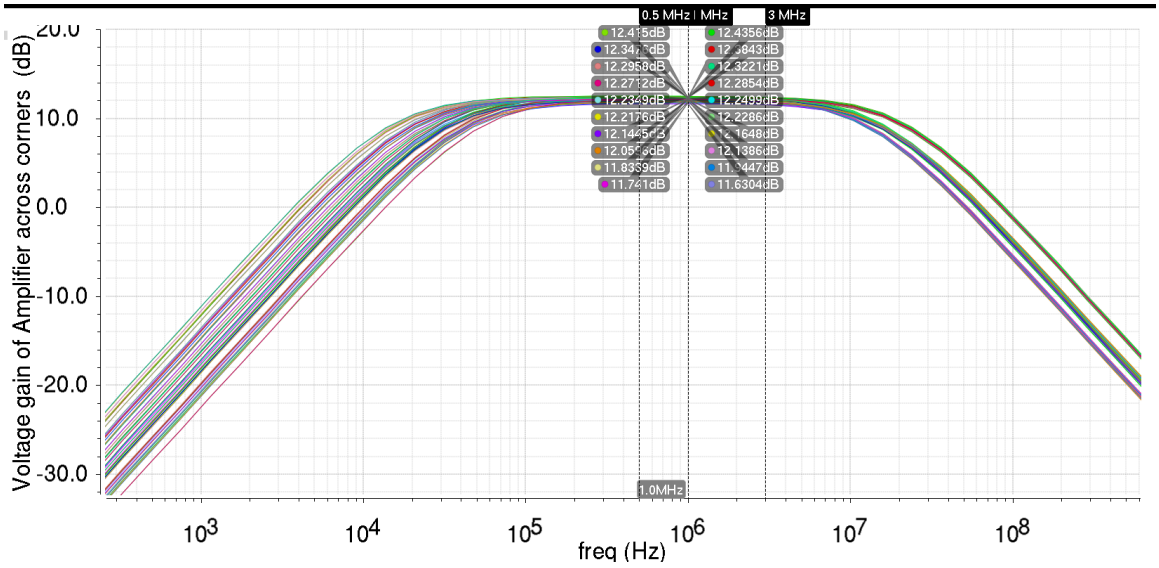


Figure 6–14 : Voltage gain variations across corners for one stage of limiter

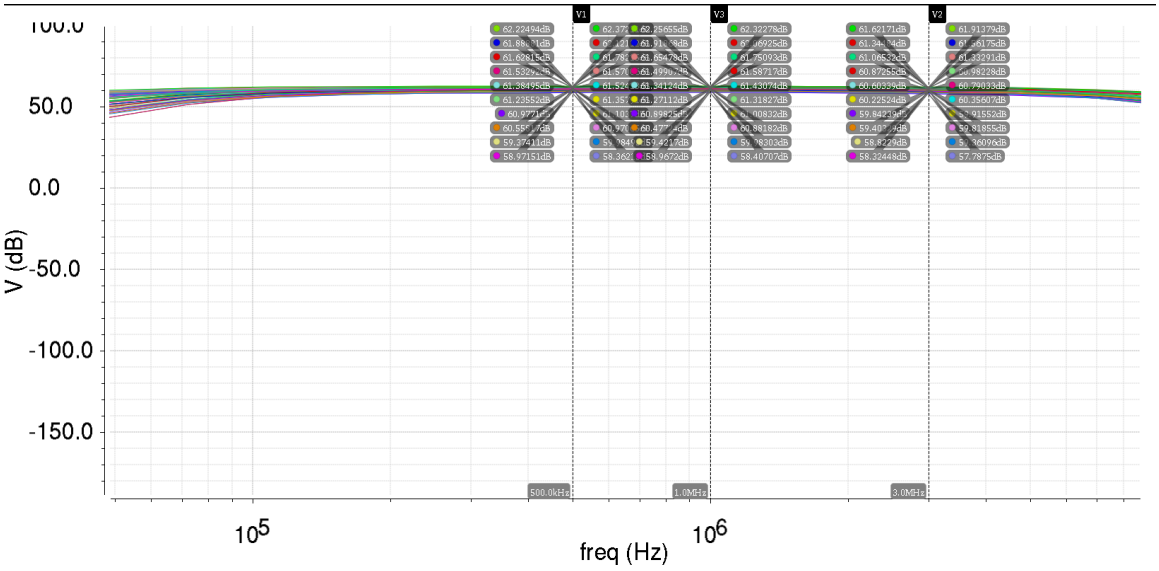


Figure 6–15: Voltage gain variations across corners for the fifth stage of limiter

6.6.2 Full Wave Rectifier (FWR)

6.6.2.1 Circuit Design

The RSSI function is implemented by connecting FWRs at the output of each gain stages. The main function of FWR is converting the input voltage to full wave output current. The output currents are summed through a resistor in parallel with capacitor to extract a dc voltage value indicates the signal strength.

The FWR circuit is shown in fig.6.16. Unbalanced source coupled differential pairs generate rectified signals. One differential pair size (M_5 , M_7) is N times as large as the other differential pair size (M_4 , M_6). And both differential pair biasing with the same current source where (M_2 , M_3) are identical transistors. The output current can be expressed as shown in equation (6.9).

$$I_{out} = (I_{D7} + I_{D5}) - (I_{D4} + I_{D6}) \quad (6.9)$$

The circuit works as follow: when there is no differential input voltage, the current of (M_5 , M_7) will be N-times larger than the current of (M_4 , M_6). When input voltage is small, most of current is flowing through larger size transistors (M_5 , M_7). Therefore, the current flow of the output current mirror (M_{10} , M_{11}) is larger than that of the left side current mirror (M_8 , M_9). Based on equation (6.9), the I_{out} will be at its maximum value. On the other hand, when the differential input voltage increases, the I_{out} decreases. As input voltage increases, smaller size transistors (M_4 , M_6) start to contribute so that the current flow in the left side current mirror increases. Therefore, the current of the output current mirror decreases, and current output is obtained depending on input voltage. The I_{out} will be almost zero when the differential input is large enough to make current flowing through (M_4 , M_5 , M_6 , M_7) equal to the maximum tail currents. Since both rectifier configurations have only three transistors stacked, they can operate in low power and low voltage supply [3],[5],[6].

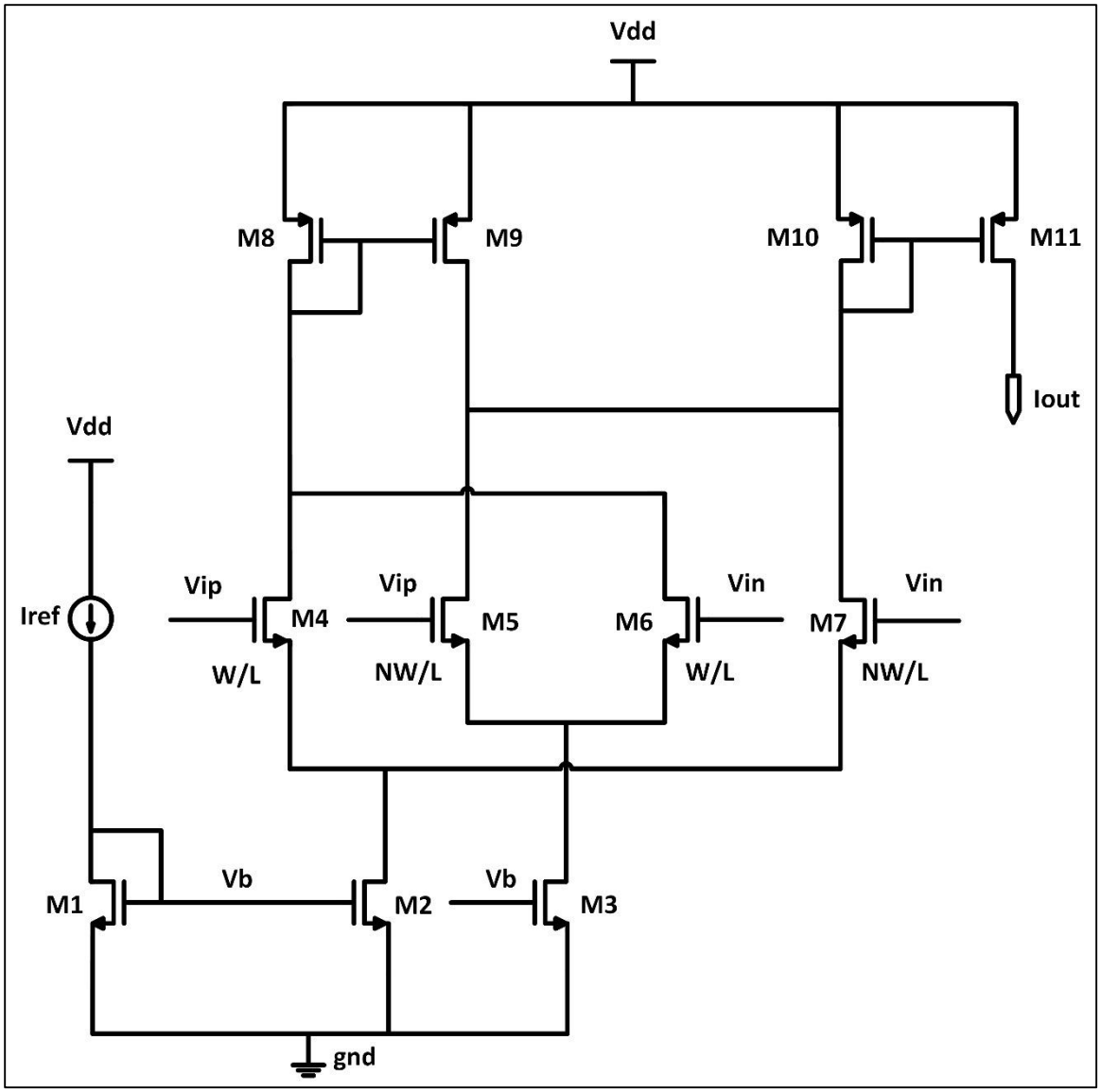


Figure 6–16: FWR circuit design

6.6.2.2 Results of FWR

This design of FWR can operate under low voltage supply and consume less power. In this block, FWR operates with 1-V and consumes 3µA currents. The main advantage of this design is the biasing technique of the differential pair transistors. They bias using current source (M_2 , M_3) so that the variations of common mode output of amplifier across corners don't affect the operating point of FWR. As shown in fig.6.17, the variations of voltage output of FWR at low input power are $\pm$ 10.123%. At high input power which is the rectification range of FWR, the variations are measured in dB and equal to $\pm 1dB$.

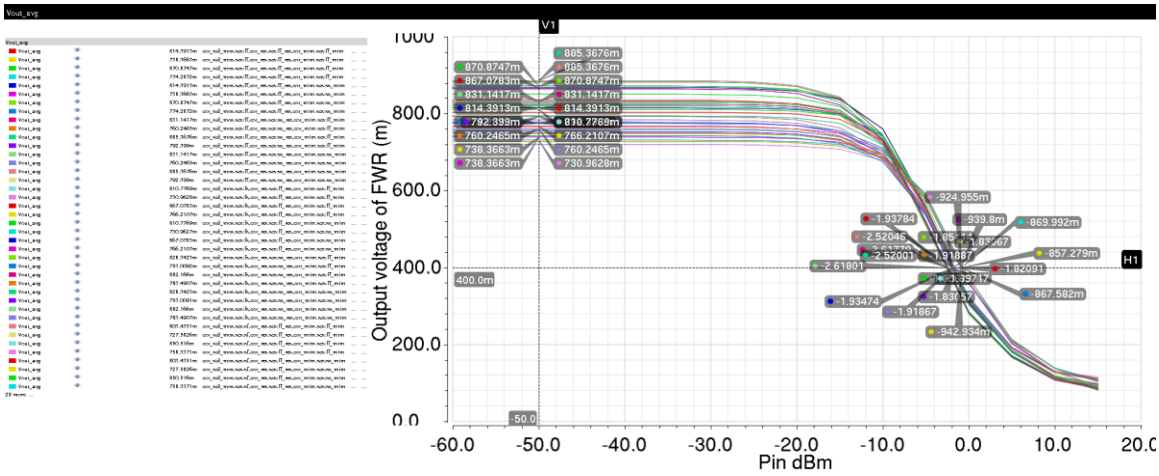


Figure 6–17: Variations of output voltage of FWR across corners

6.6.3 Differential Input Single-Ended Amplifier

The circuit of this amplifier is shown in fig.6.18. This amplifier is put in the path of the Limiter to deliver the received signal to base band digital receiver as it should be single-ended. Also, this amplifier amplifies the signal to reach rail to rail. It has 33.50674dB gain so total gain of limiter is 94.8881dB as shown in the fig.6.19.

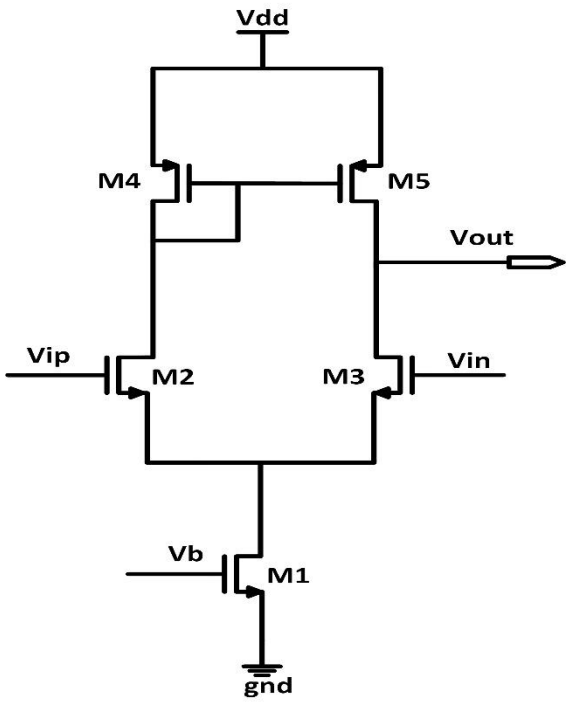


Figure 6–18: Single-ended amplifier circuit

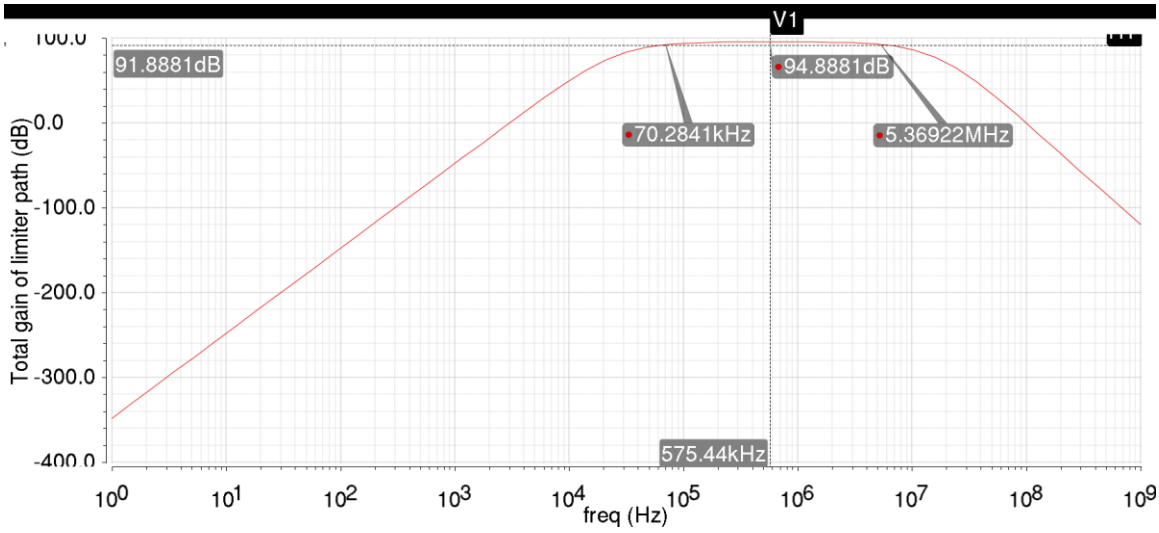


Figure 6–19: Total gain of the limiter path

6.6.4 Last Stage in Limiter and its Output Signal

To get rail to rail values for the received signal and avoid any decreasing in voltage level of high or increasing in low voltage level which make digital receiver works wrong, an inverter is used after single-ended amplifier stage to achieve rail to rail signal. The output of I and Q signals from limiter is shown in fig.6.20. Across corners as total gain decreases and increases so it may affect levels of the signal. The output of limiter path is shown in fig.6.21, and at 2MHz in fig.6.22. They are almost the same. The high level is 1.04998V rather than 1.05V and 949.981mV rather than 950mV. For low voltage level, worst case is 435.124µV, this values at low signal strength for the dynamic range of RSSI block which is -50dBm.

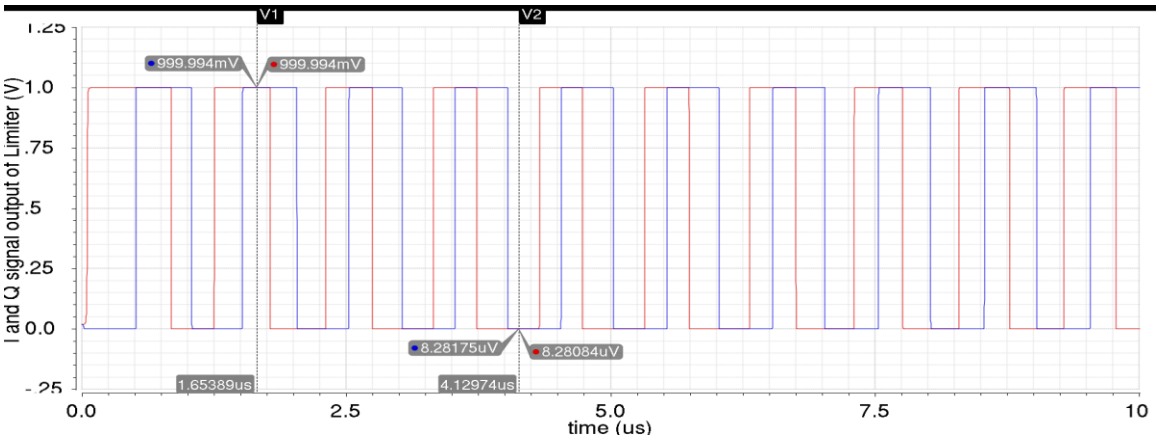


Figure 6–20: I and Q signals output from limiter path

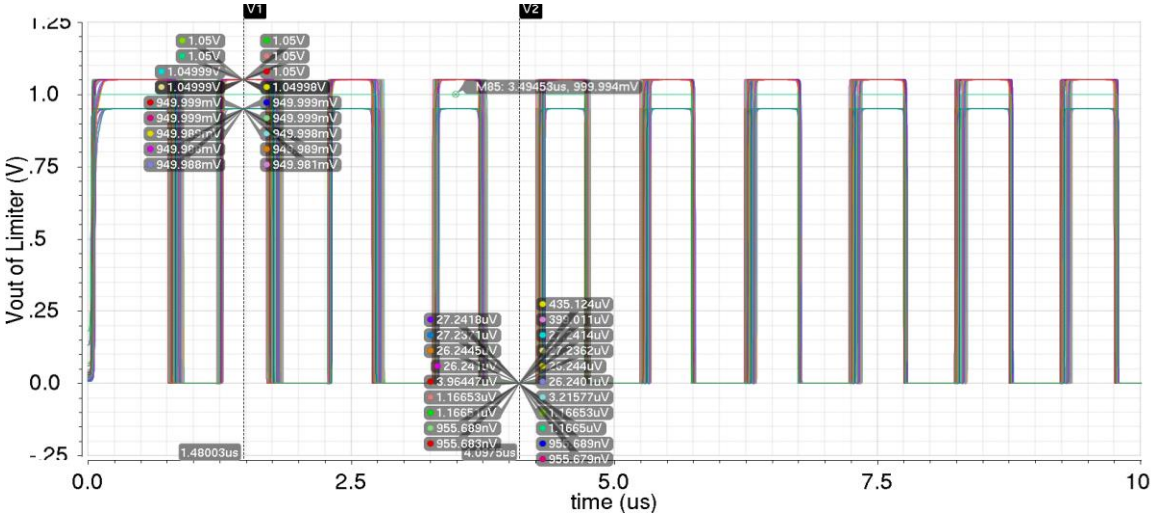


Figure 6–21: Output signal from limiter path across corners at 1MHz

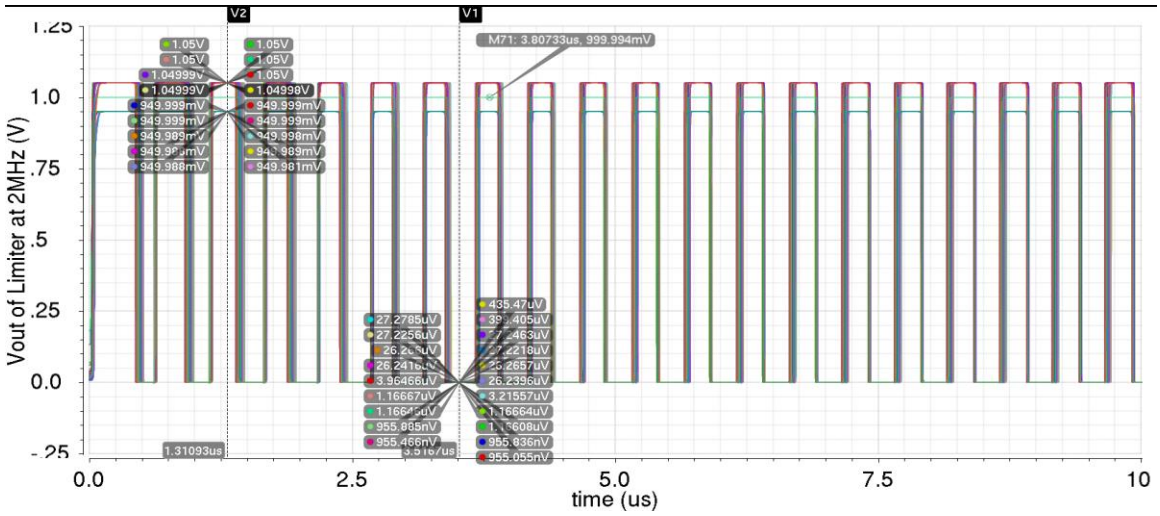


Figure 6–22: Output signal from limiter path across corners at 2MHz

6.6.5 Overall RSSI Results

6.6.5.1 RSSI Output voltage

As mentioned before RSSI output voltage will be the input of ADC, so that the output voltage for RSSI dynamic range (-50dBm to -5dBm) should be within the input dynamic range of ADC. As discussed before, there are two modes of the receiver (1MHz and 2MHz) and RSSI block should deal with two modes approximately the same. As shown in fig.6.23, RSSI output for 1MHz and 2MHz at -50dbm is less than 700mV and at -5dBm is greater than 150mV.

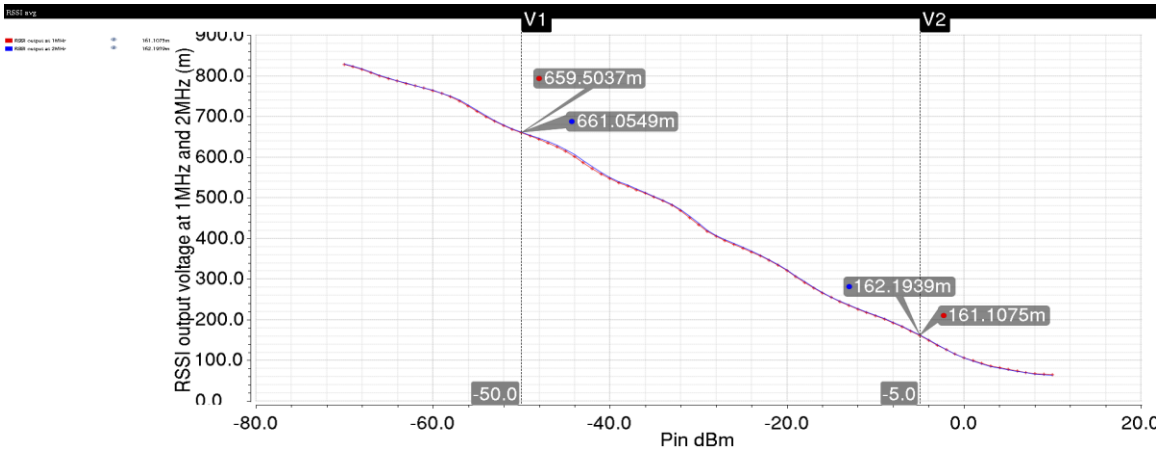


Figure 6–23: RSSI output voltage at 1MHz and 2MHz

Across corners RSSI output voltage should have an error less than $\pm 6dB$ for two modes. As shown in fig.6.24, maximum error across temperature, voltage supply and process variations at 1MHz is $\pm 4.45dB$ and worst cases are (ff MOS, ff res, ss cap, 0.95V, $-40℃$) and (ff MOS, ss res, ff cap, 1.05V, $125℃$). Also, as shown in fig.6.25. maximum error at 2MHz is $\pm$ 4.66 dB for the same worst cases of 1MHz across corners.

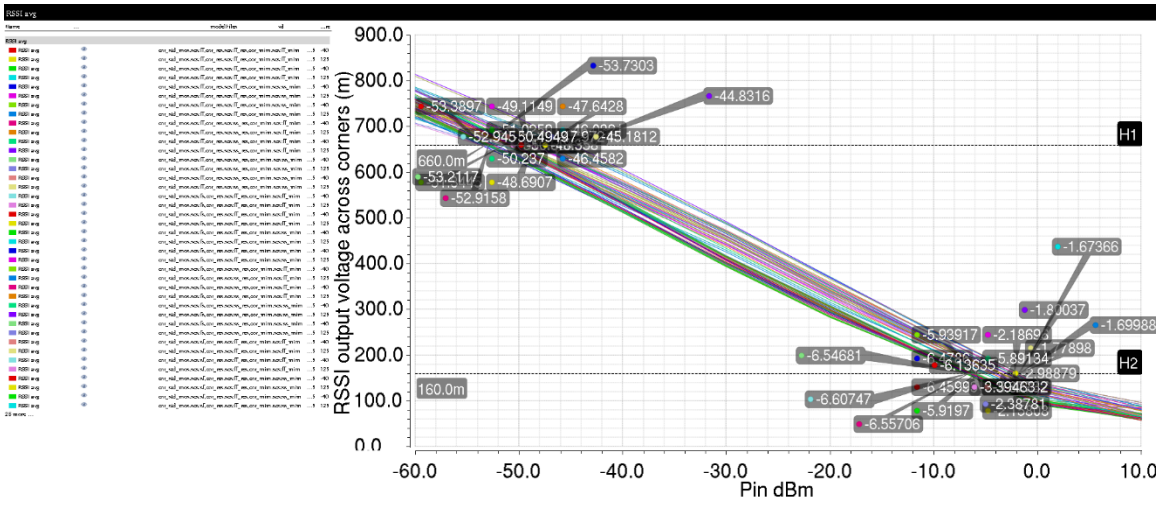


Figure 6–24: Variations of RSSI output across corners at 1MHz

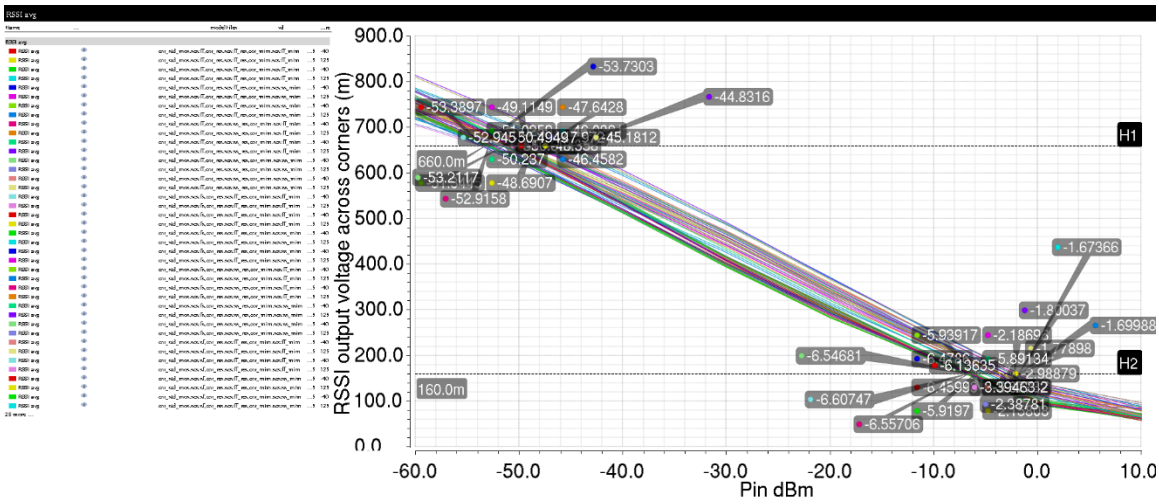


Figure 6–25: Variations of RSSI output across corners at 2MHz

6.6.5.2 Current Consumption of The Block

Fig.6.26 shows the consumed current versus input power at 1MHz and 2MHz which is approximately the same. Maximum consumed current at low input power and it is 406.1561µA at -50dBm and 2MHz.

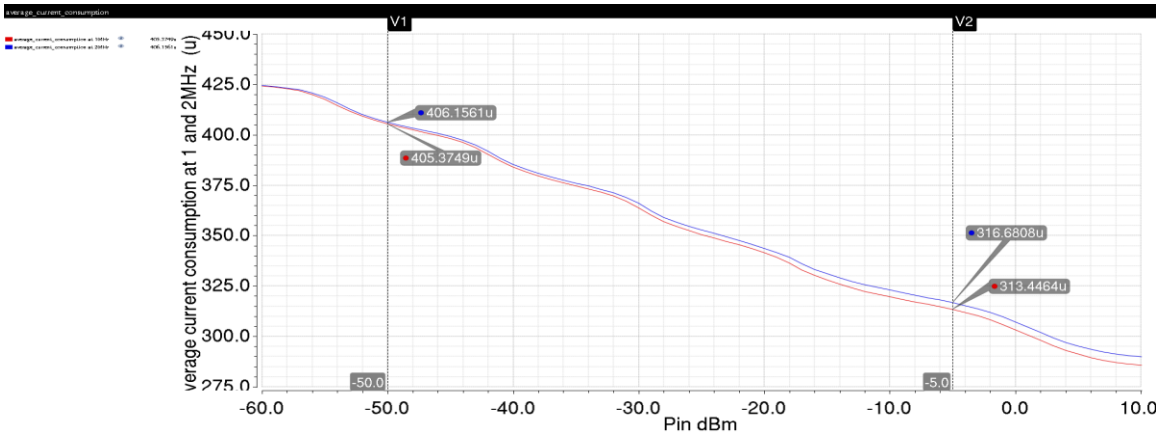


Figure 6–26: Current consumption vs input power at 1MHz and 2MHz

6.6.5.3 Time Delay of RSSI Output

There is a trade-off between time delay of output and ripples in output. They are dependent on RC filter values at output. If RC values increase, the ripples decrease but time delay increase. Time delay in typical and across corners should be less than 2µsec in this design for two modes of the receiver. As shown in fig.6.27, time delay for two modes is approximately the same it is 1.4µsec at 1MHz and 1.3µsec at 2MHz but ripples at 2MHz

equal $\pm 0.61\%$ which less than at 1MHz that equal $\pm 1.195\%$. In addition to, fig.6.28, shows best and worst case of delay and ripples for two modes of operations. Ripples and time delay for worst cases are depicted in table 6.1.

Table 6.1: Worst cases for time delay and ripples across corners at 1MHz and 2MHz

Frequency	**At 1 MHZ**		**At 2 MHz**	
Parameters	**Time Delay**	**Ripples**	**Time Delay**	**Ripples**
Worst case delay	$1.6612\ \mu sec$	$\pm\ 0.84\ \%$	$1.7304\ \mu sec$	$\pm\ 0.44\ \%$
Worst case ripples	$614.87\ nsec$	$\pm\ 1.95\ \%$	$750.8436\ nsec$	$\pm\ 1.1\ \%$

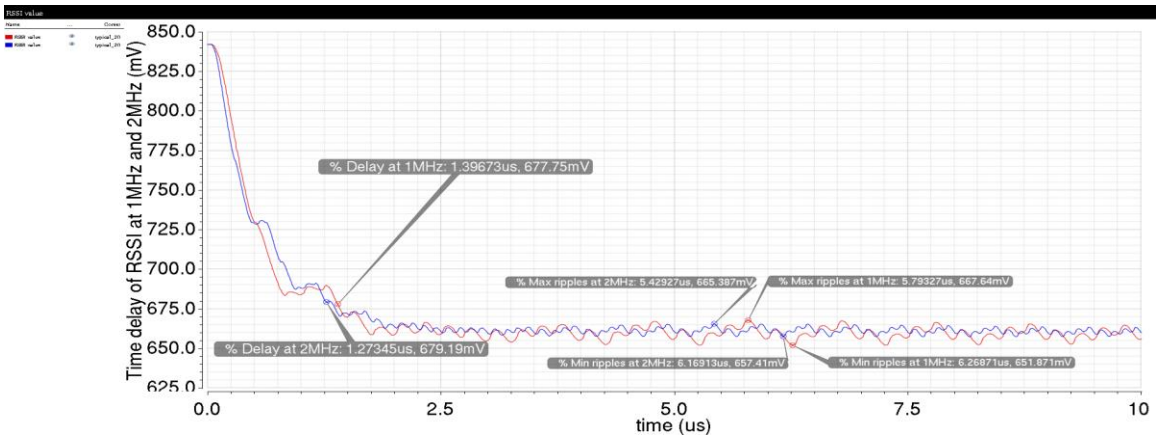


Figure 6–27: Time delay and ripples for RSSI output at 1MHz and 2MHz

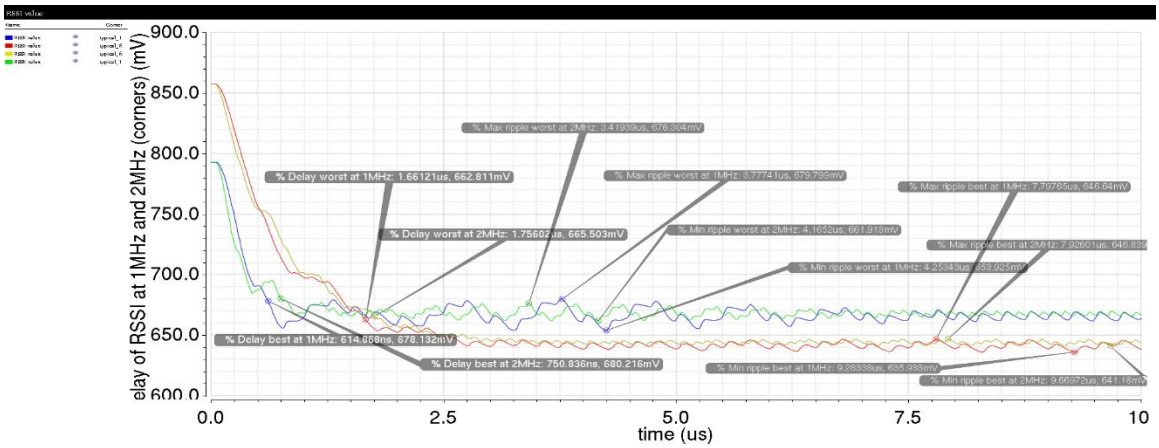


Figure 6–28: Time delay and ripples for RSSI output across corners at 1MHz and 2MHz

6.7 Conclusion

As mentioned before, this chapter includes RSSI and limiter block which operates with low voltage and low power in two modes of operations for the Bluetooth receiver. There are many specifications on this block that all discussed before and they are concluded in table 6.2.

Table 6.2: Desired vs achieved specs of the RSSI block

Name	Spec	Achieved
Bandwidth	0.5MHz to 3MHz	70.349KHz to 6.2086MHz
Limiter Output Level	Rail-to-Rail (0-Vdd)	Rail-to-Rail (0-Vdd)
RSSI Output Dynamic Range	150mV to 700mV	161mV to 662mV
Error in RSSI Value Across Corners	Less than $\pm 6\ dB$	$\pm 4.66\ dB$
Dynamic range of Input Power	-50dBm to -5dBm	-50dBm to -5dBm
Time Delay of RSSI	2 µsec	1.731 µsec
Current Consumption Within Dynamic Range for I and Q signal	500 µA	406.2 µA

6.8 References

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7 Chapter 7: Analog-to-Digital Converter

7.1 Overview

Analog-to-digital converters (ADCs) provide a link between the analog signals of the real world and the world of digital signal and data processing. Figure 7-1 shows the basic concept of an analog to digital converter: a continuous analog signal input is converted to a discrete digital signal at the output.

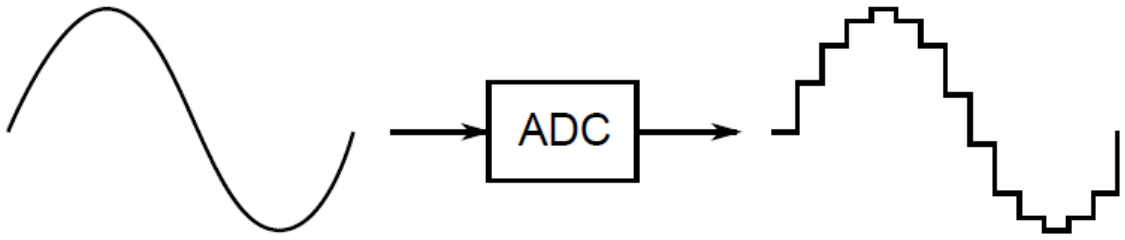

Figure 7–1: Analog to Digital Converter ADC

Data is preferred to be in digital form as digital form has many benefits over analog form. Data in digital form is more immune to noise, easier in processing, automated design for digital circuits is widely available and digital circuits directly benefit from the scaling of VLSI technology.

7.2 Main Conceptions

7.2.1 Sampling Frequency

An analog signal is converted to a digital signal through sampling. Sampling refers to how often a portion of the input voltage is converted into a digital number. Figure 7-2 displays the concept of sampling. Each of the green lines represents an instance in time when a sample is taken. When a sample is taken, the value of the input voltage is converted to a digital number. For example, the second green vertical line indicates the second sample. The input voltage has a certain value at the second sample. That value is converted into a digital representation which is designated n_2 on the figure. The distance between samples (green lines), is denoted as the sampling time, Ts. The sampling frequency is a performance specification of all ADC's and is designated speed.

The Nyquist-Shannon sampling theorem; the theorem says that you can reconstruct an analog signal completely if you sample the analog signal two times faster than the largest frequency component in the analog signal. Figure 7-3 displays the fundamental principle behind the Nyquist-Shannon sampling theorem. The figure shows a plot of the frequency components of the input signal. The highest frequency component in the input signal is denoted f_h. Therefore, the appropriate sampling frequency, f_s, is equal to $2f_h$, as indicated in the figure.

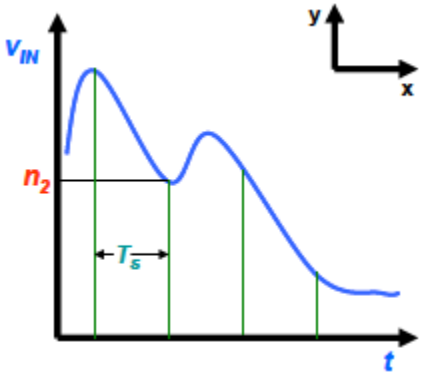

Figure 7–3: Sampling

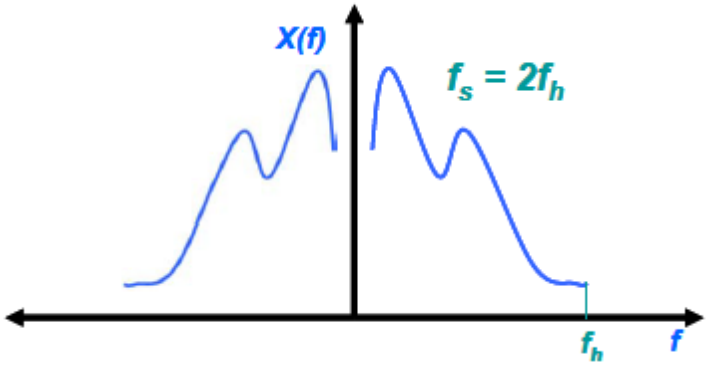

Figure 7–3: Nyquist-Shannon Sampling Theorem

An important result of the Nyquist-Shannon Sampling Theorem is that you can reconstruct an analog signal completely if you retain the value of the input voltage every time you take a sample. This is not possible with an ADC because the output is a digital signal and a digital signal can only take on certain y-values. The fact that a digital signal can only take on certain y-values leads to a very important error in ADC's called quantization error.

7.2.2 Quantization error

Quantization is also necessary for analog-to-digital converters. Quantization is the process of assigning certain ranges of values from a continuous signal range to discrete values. This assignment creates quantization errors. A quantization error is the difference between the quantized value and the original signal. In Figure 7-4a, the original signal Vin is shown in blue. If a sample of this signal is taken at time T_1, it would be quantized to n_2, as shown in Figure 7-4b. The difference between the sample of V_{in} and its quantized value n_2 is indicated by the black bar.

Quantization errors are directly related to the resolution of the ADC. An ADC that needs an accuracy within a very small margin of error is going to need more quantization levels. More levels require a larger number of digital bits to encode all the information. Higher resolution often comes at the cost of converter speed, so converters need to be optimized for required speeds and resolutions. This optimization depends greatly on the type of architecture chosen for the ADC design.

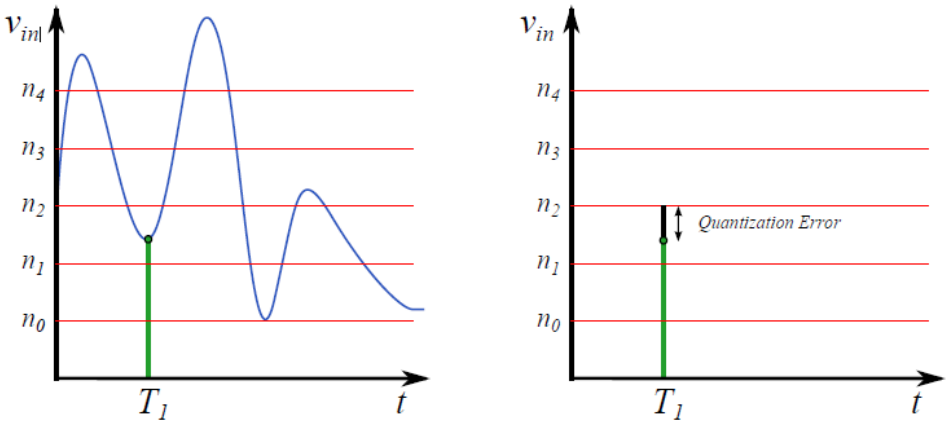

Figure 7–4: (a) Input Signal (b) Quantization Error

7.3 ADC Performance Specifications

ADC Characterization is divided into: static characterization and dynamic characterization. The importance of each kind of characterization depends on the ADC application. Some applications with very low speed requirements are specified by the static specifications which include the ADC resolution, offset, linearity, and gain error. Other applications like wireless communications systems are required to meet the dynamic specifications as Signal to Noise Ratio (SNR), Spurious Free Dynamic Range (SFDR), Total Harmonic Distortion (THD) and Signal to Noise and Distortion Ratio (SNDR).

7.3.1 Static Characterization

7.3.1.1 Resolution

Typically, a converter with N-bit resolution should convert the input range of analog signal to 2^N-1 discrete levels. Noise and non-linearity limits the resolution of a converter.

7.3.1.2 Offset error

Offset is defined as deviation of first converter threshold level from ½ LSB. The input/output transfer function of an ideal ADC can be represented by a straight line. The ADC offset is the vertical intercept of this straight line illustrated in Figure 7-5.

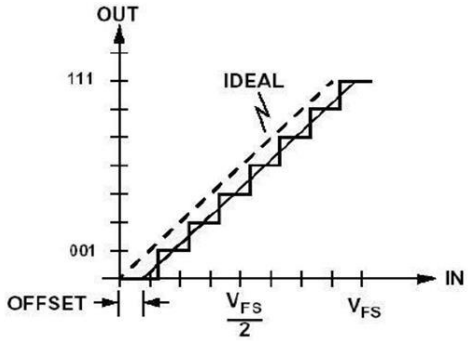

Figure 7–5: Offset error for ADCs

$$E_{offset} = \frac{V_{trans.first}}{V_{LSB}} - 0.5 * LSB$$

7.3.1.3 Gain error

Gain error is defined as the deviation of the slope of the input/output characteristic from the ideal slope which is one illustrated in Figure 7-6. Gain error is defined as the difference in ideal an observed full scale conversion threshold, after offset has been considered.

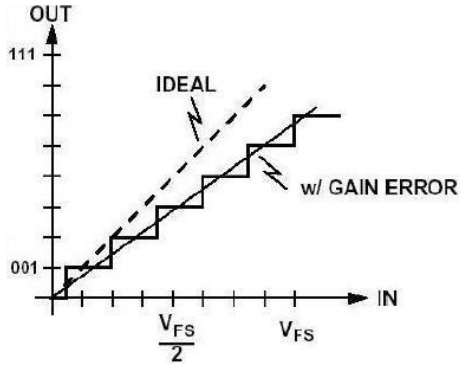

Figure 7–6: Offset error for ADCs

7.3.1.4 Differential Non-Linearity (DNL)

When the step size of an ADC's output is not equal to the ideal step size, the ADC is said to have differential nonlinearity. The DNL measurement for an ADC is classified based on amount of least significant bit (LSB) values that the actual transfer function deviates from the ideal transfer function. If the DNL is greater than 1 LSB ($|DNL| \geq 1$ LSB), a non-monotonic transfer function will cause missing codes. Figure 7-7 shows the deviation of a real transfer function from the ideal.

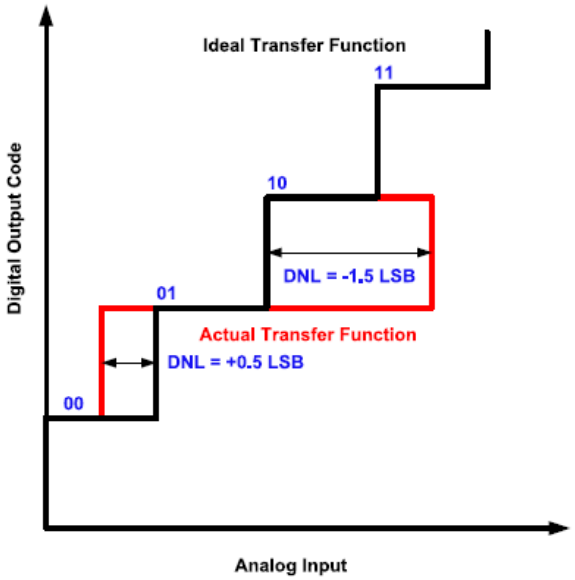

Figure 7–7: Differential Non-Linearity

7.3.1.5 Integral Non-Linearity (INL)

INL (Integral Nonlinearity) is the total deviation of an analog value from its ideal value in LSB. An ADC that exhibits integral non-linearity will have a transfer function that is not a perfect line. The maximum difference between the actual and ideal transfer characteristic is the INL. This concept is illustrated in Figure 7-8.

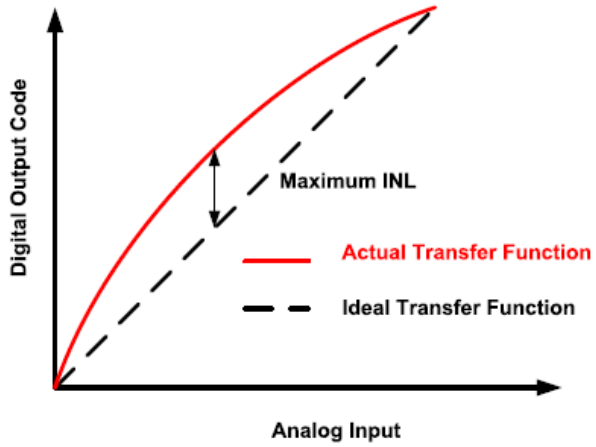

Figure 7–8: Integral Non-Linearity

The relation between DNL and INL is as follows:

$$INL_i = \sum_{1}^{i-1}\left(DNL_j\right)$$

7.3.1.6 DAC Monotonicity

A DAC is said to be monotonic if the analog amplitude level increases with increasing the digital code, for a monotonic DAC if DNL ≤ LSB or INL ≤ 0.5 LSB, Figure 7-9 illustrates DACs non-monotonicity.

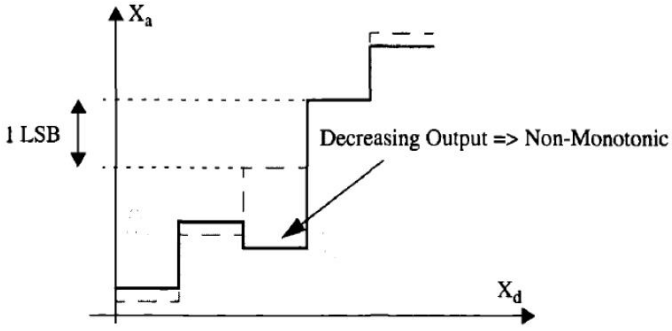

Figure 7–9: A non-monotonic DAC

7.3.2 Dynamic characterization

Dynamic characterization measures the ADC performance based on the frequency spectrum of its output. Figure 7-10 shows a general frequency spectrum of the output of an ADC.

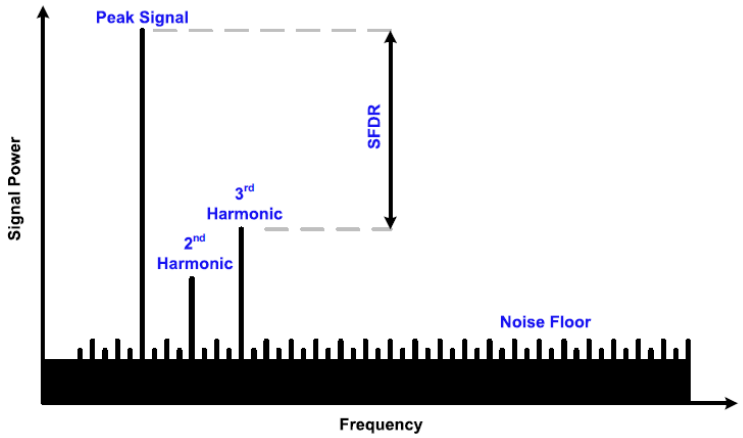

Figure 7–10: General ADC output spectrum

7.3.2.1 Signal to Noise Ratio (SNR)

SNR is the ratio between the signal power and the noise power at the output of the ADC. The output noise includes the quantization noise, thermal noise, and all other random noise sources of the devices used. The SNR is expressed as:

$$SNR_{dB} = Signal\ Power_{dB} - \ Noise\ Power_{dB}$$

For an N-bit ADC the SNR is given by:

$$SNR_{dB} = 6.02N + 1.76$$

7.3.2.2 Spurious Free Dynamic Range (SFDR)

SFDR is the ratio between the maximum signal component and the largest distortion component at the output of the ADC as illustrated in Figure 7-10. This is one of the most important specifications for ADCs used in wireless communications systems. SFDR indicates the usable dynamic range of the ADC beyond which distortion becomes dominant over noise.

7.3.2.3 Total Harmonic Distortion (THD)

THD is the root mean square sum of all the harmonic components (except the fundamental) of the output signal of the ADC. In general, up to 5^{th} or 7^{th} harmonics are used to measure the THD.

7.3.2.4 Signal to Noise and Distortion Ratio (SNDR)

SNDR is the ratio between the maximum signal power to the total root mean square noise power contributed by harmonic distortion, quantization noise and devices noise.

7.3.2.5 Effective Number of Bits (ENOB)

ENOB of an ADC is a measure to compare different ADC designs. The ENOB is defined by:

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

7.3.2.6 Figure-of-Merit

A popular Figure-of-Merit (FOM) used to compare different ADCs is given by:

$$FOM = \frac{Power\ Consumption}{2^{ENOB} \times f_s}$$

where f_s is the sampling rate in Nyquist-rate ADCs. This figure of merit is commonly used to compare different ADCs as it is based on easily measured quantities, and calculates a value that has a meaningful unit (i.e. energy required per conversion step, thus lower FOM means a better ADC).

7.4 ADC architectures

Many different ADC types and architectures can be found in the literature. Each architecture represents trade-offs between resolution, conversion speed, power and die area. As an ADC can be one of the main power hungry blocks in a system, it is very important to minimize its power consumption. Several architectures have been developed to achieve optimal power consumption for different sampling rates, and resolutions as shown in Figure 7-11 and Table 7-1. A brief discussion of the basic ADC architectures is given followed by a discussion on ADC specifications and parameters.

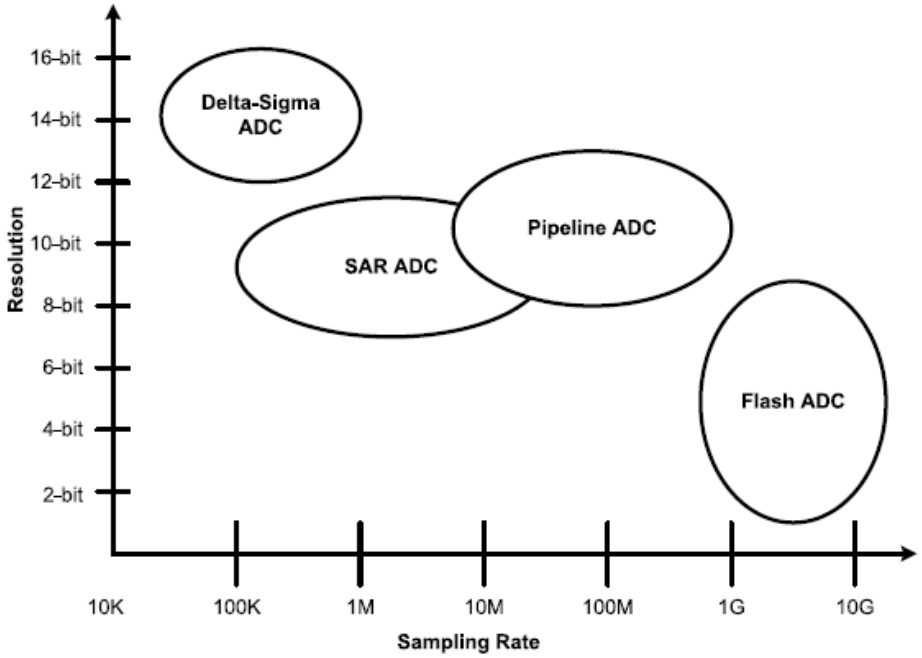

Figure 7–11: ADC architecture comparison

Architecture	Speed	Accuracy	Area
Flash ADC	High	Low	High
SAR ADC	Low-Med	Med-High	Low
Delta-Sigma ADC	Low	High	Med
Pipeline ADC	Med-High	Med-High	Medium

Table 7–1: ADC architectures comparison

7.4.1 Flash ADC

Flash ADC, which is the fastest and one of the simplest ADC architectures, is shown in Figure 7-12. It performs 2^N-1 level quantization with an equal number of comparators. The reference voltages for the comparators are generated using a resistor ladder, which is connected between the positive ($+V_{ref}$) and the negative ($-V_{ref}$) reference voltage determining the full-scale signal range. Together the comparator outputs form a 2^N-1 bit code, where all the bits below the comparator whose reference is the first to exceed the signal value are ones, while the bits above are all zeros. This so-called thermometer code is converted to N-bit binary word with a logic circuit, which can also contain functions for removing bit errors (bubbles).

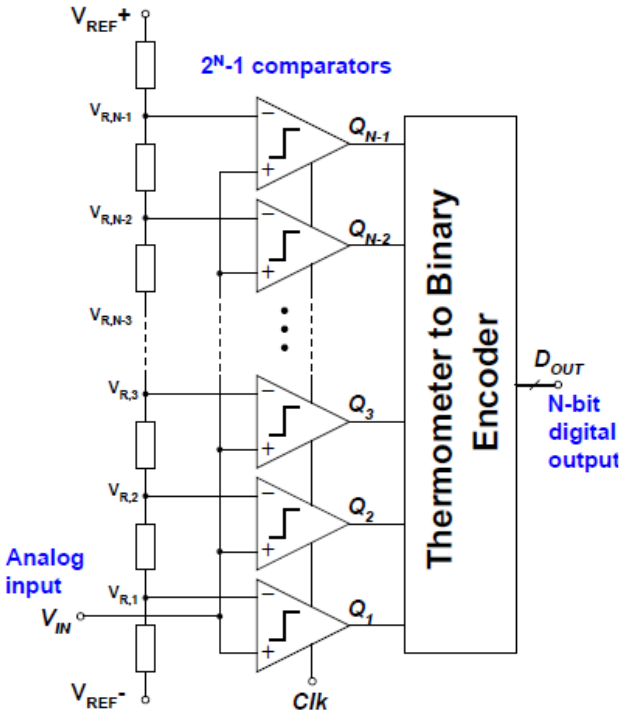

Figure 7–12: Flash ADC

Since the input signal is directly connected to the inputs of the comparators, flash architecture is very fast; the speed is only limited by the comparators. Thus, the fastest reported ADCs are realized with this architecture. Flash ADC also has very low latency typically one to two clock cycles, which allows it to be utilized in applications using feedback (e.g. gain control loop).

The most prominent drawback of flash ADC is the fact that the number of comparators grow exponentially with the number of bits. Increasing the quantity of the comparators also increases the area of the circuit, as well as the power consumption. Thus, very high resolution flash ADCs are not practical; typical resolutions are seven bits or below.

7.4.2 Delta-Sigma ADC

Noise shaping ADCs ($\Delta - \sum$ ADCs) use oversampling, modulator and digital filtering to achieve high resolution from a single bit quantizer. As shown in Figure 7-13 the basic noise shaping ADC has an integrator, comparator (1-bit quantizer), digital filter and 1-bit DAC. When the input signal is oversampled, the noise shaping structure transfers most of the quantization noise outside the signal band. Thus post filtering in digital domain to remove to remove the noise can be used to achieve very high SNR. Typical applications for this kind of ADC have been audio fidelity (16-20 bit).

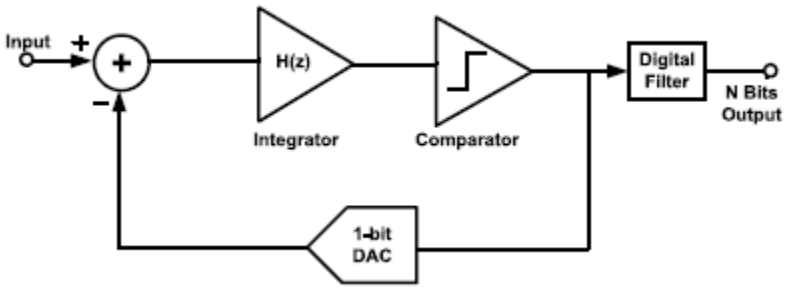

Figure 7–13: Sigma-Delta ADC

7.4.3 Pipeline ADC

The concept of pipelining has been used in digital circuits to achieve high speed by inserting registers between different stages which are operating simultaneously on successive sets of data. This concept has been extended to ADCs, where identical stages with low resolution ADCs are separated by analog registers (Sample & Hold). Each stage of the ADC is operating on successive samples of the input signal.

Figure 2.14 shows the block diagram of a pipeline ADC. Each stage has a Sample & Hold circuit (S & H), n-bit Flash ADC called Sub ADC, n-bit DAC, a subtractor and an amplifier with gain A. The sampled input signal is first quantized by the Sub-ADC to generate the output digital code of this stage. Then the output digital code is converted back to analog signal by the DAC. This quantized analog signal is subtracted from the input signal, resulting in a residue that is amplified and then passed to the next stage.

Each stage does not need to resolve the same number of bits. The resolution of the ADC is the sum of the bits resolved by each stage. Since each stage is working on successive samples, the digital output bits need to be appropriately delayed and then combined to produce the corresponding digital value for the analog input signal through the Digital Correction Logic as shown in Figure 7.15.

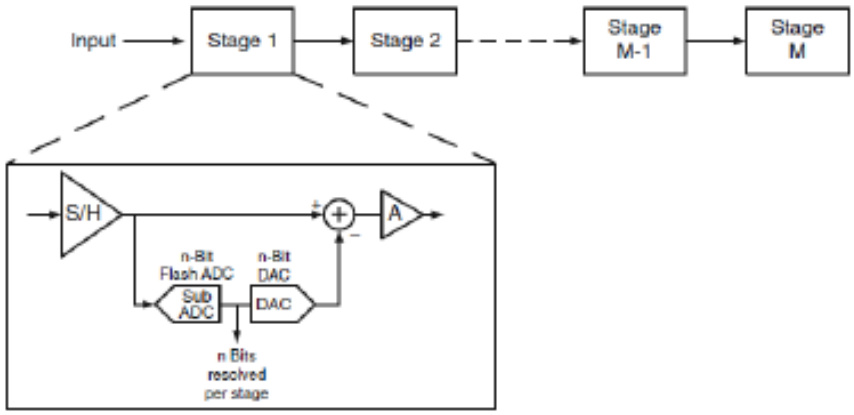

Figure 7–14: Pipeline ADC

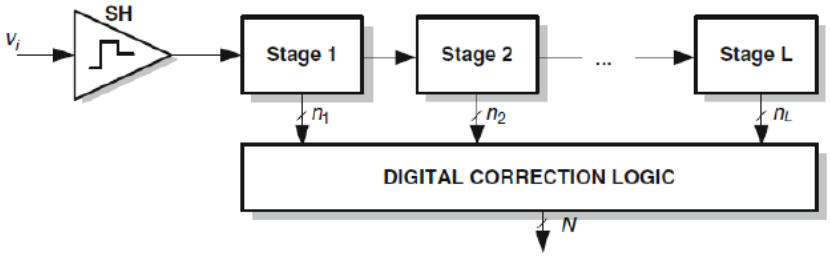

Figure 7–15: Pipeline ADC basic block diagram

7.4.4 Successive Approximation Register (SAR) ADC:

The algorithm used in successive approximation register (SAR) ADC is based on a binary search algorithm. Figure 2.16 shows the standard topology of a SAR ADC. In SAR ADC, an analog input voltage is sampled on a sample/hold circuit. To implement the binary search, an N-bit code register in SAR logic block is first set to midscale where MSB is logic 1. This changes the DAC output to be half of the reference voltage. Then the comparator performs a comparison between V_{in} and V_{DAC}. If V_{in} is greater than V_{DAC}, the comparator output is a logic high and the MSB of the N-bit code register remains at logic 1. If V_{in} is less than V_{DAC}, the comparator output is a logic low and the MSB of the register cleared to logic 0. The SAR logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete and the N-bit digital word is available in the SAR's code register as shown figure 2-17. Figure 2-18 shows an example of 4-bit SAR conversion. The final digital code (and the output from the ADC) is 0101.

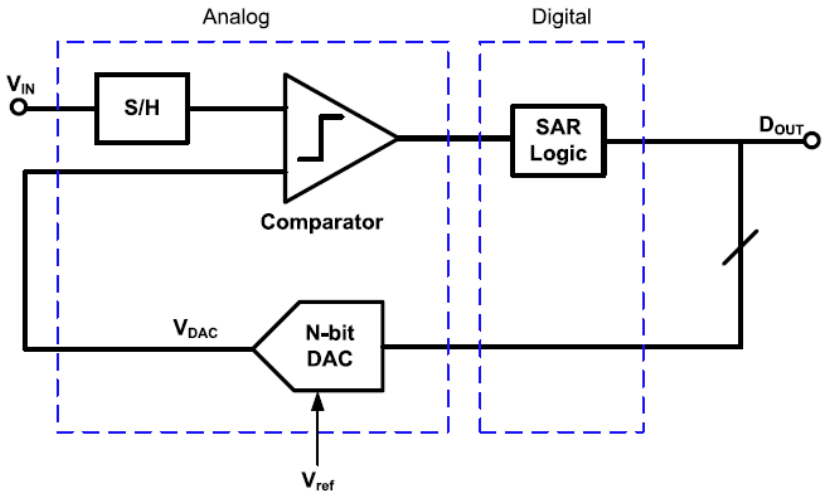

Figure 7–16: SAR ADC

SAR ADCs achieve very low power consumption due to its simple structure based mostly on digital blocks. SAR ADCs do not require an amplifier, so they are advantageous in CMOS technology scaling. The main limitation of SAR ADCs is the low sampling rate, which is linked to its serial decision making nature.

Most SAR ADCs use a capacitive DAC that provides an inherent sample/hold circuit, as well as, charge-redistribution DACs which are based on switched capacitor circuits. SAR ADC′s speed is limited by the DAC settling time, by the comparator which must resolve small voltage difference within the specified time, and by the SAR logic operation.

The overall accuracy and linearity of the SAR ADC is determined mainly by the DAC. Component matching limits the linearity of SAR ADCs in practical DAC designs.

The main advantage of the SAR ADC is that it uses a few number of analog blocks which results in a small area and simple design. SAR ADCs are often the best choice for battery-powered applications which need only medium resolution and medium speed but require low-power consumption. The architecture is widely used in low energy communications systems, in portable sensor systems, and in many biomedical applications.

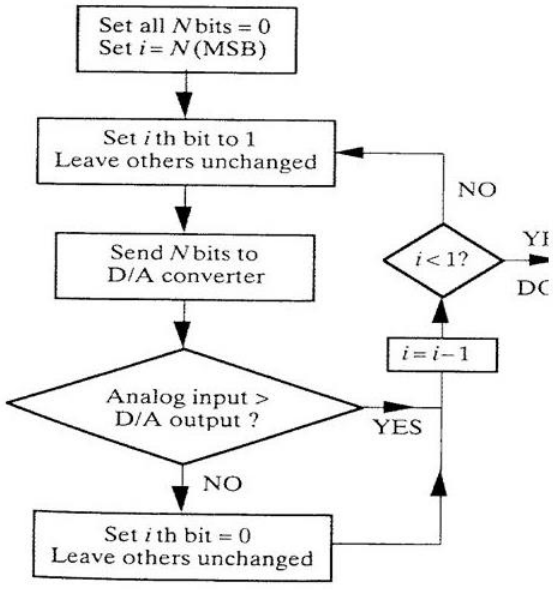

Figure 7–17: SAR ADC Operation Flowchart

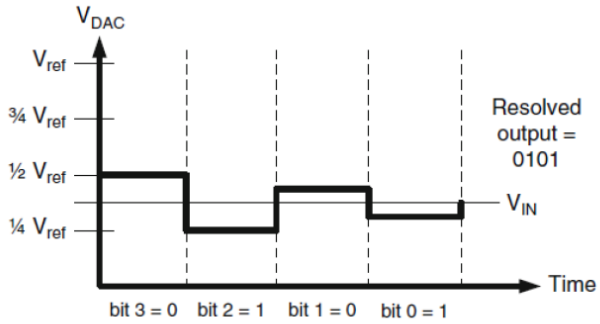

Figure 7–18: SAR ADC Operation

7.5 DAC Architectures

The main building block in every DAC is a component that creates an appropriate analog output level by dividing a reference voltage. Elements such as resistors split the reference voltage into smaller voltage or current levels. Transistor current sources can also create output currents that are converted to the analog output voltage by the load resistors. Capacitors are also used in some architectures to store charge from the reference voltage and discharge it to the output.

There are 3 types of DACs as follows, thermometer (unit element), Binary weighted and hybrid. Combined with the 3 architectures of Resistor, current source or capacitive charged. The following are explanation of some of those architectures.

7.5.1 DAC Examples

7.5.1.1 Resistor string DAC

It is considered the simplest DAC architecture as seen in Figure 7-19. It is made up of 2^N resistors in series, a reference voltage is connected at one end of the resistor string, and ground at the other. Switches are connected after each resistor, the output of each switch is tied together to form the DAC output. This structure results in good accuracy and is inherently monotonic. It is also fast for less than 8 bits DAC. The disadvantage of this topology is that when resolution becomes a big value, large parasitic capacitance appears at the output and conversion speed becomes much slower. Also this architecture occupies large area and needs large settling time especially for DAC with 8 bit or higher resolution. Matching this large number of resistors properly is also a very difficult task.

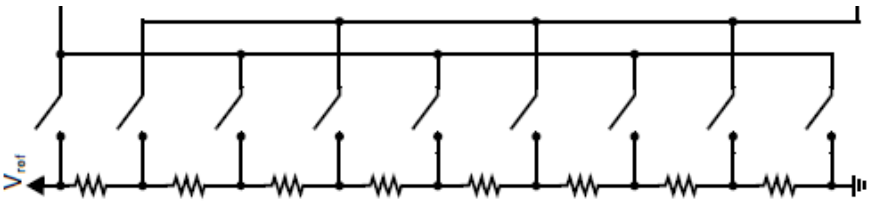

Figure 7–19: 3 bit Resistor string DAC

7.5.1.2 Current Steering DAC

The current steering DAC is the preferred architecture for high speed converters. This architecture is shown in Figure 7-20. It works by summing the current produced by an array of current sources. A load resistor is connected to the output of the current sources on one end, and the supply voltage at the other. When the current source is enabled, current flows through the load resistor. This current is dumped by the current source, thereby converting the current into a voltage eon the resistor. The output voltage is formed from the voltage division between the power supply connected to the resistor, and the voltage drop produced by the current draw from the current sources. Since an op amp is not required to form the output voltage, higher performance can be achieved.

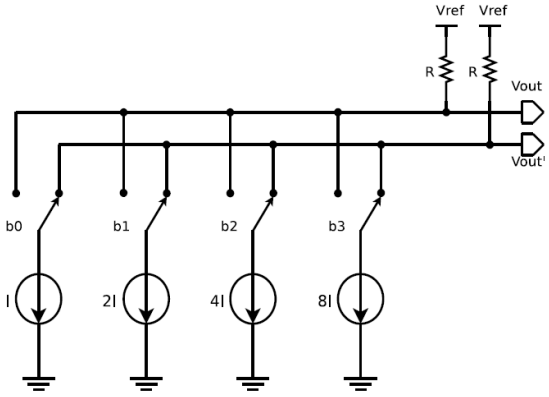

Figure 7–20: 4 bit Current steering DAC

7.5.1.3 Capacitive binary weighted DAC

In reset phase all capacitors are discharged. No encoder needed. In evaluation phase, depending on the digital word, the caps either remain connected to ground or are connected to V_{ref}, and DAC operates as a capacitor divider as shown in Figure 7-21. DAC output sensitive to parasitics and can be avoided by operational amplifier. Monotonicity depends on element matching.

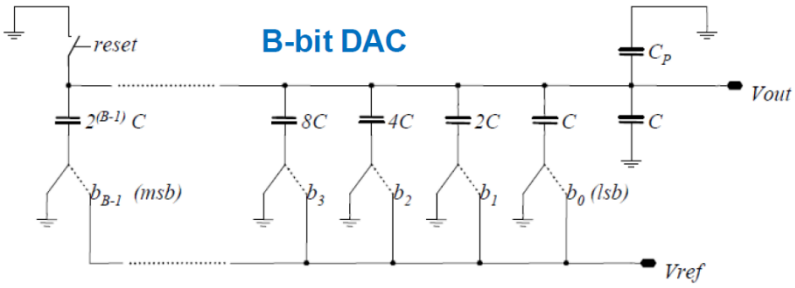

Figure 7–21: B-bit Capacitive DAC

$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{2^B C + C_P} V_{ref}$$

7.5.2 Switching schemes

7.5.2.1 Conventional vs. Monotonic Switching

DAC capacitors are switched to (V_{dd}) and may be re-switched to (Gnd) based on comparator decision Inefficient capacitor network switching energy.

In Monotonic switching, initially all Caps bottom plate connected to V_{CM}. SAR is the control unit which takes the output of the comparator and sends control signals to the switches in DAC. In addition to that, MSB capacitor of the DAC array is eliminated. Therefore, the capacitor array is reduced by 50% (power/area saving). No re-switching considerable reduction in switching power is saved, however in (a) DAC signal CM varies during bit cycling. However, varying CM induces varying comparator offset and hence non linearity occurs.

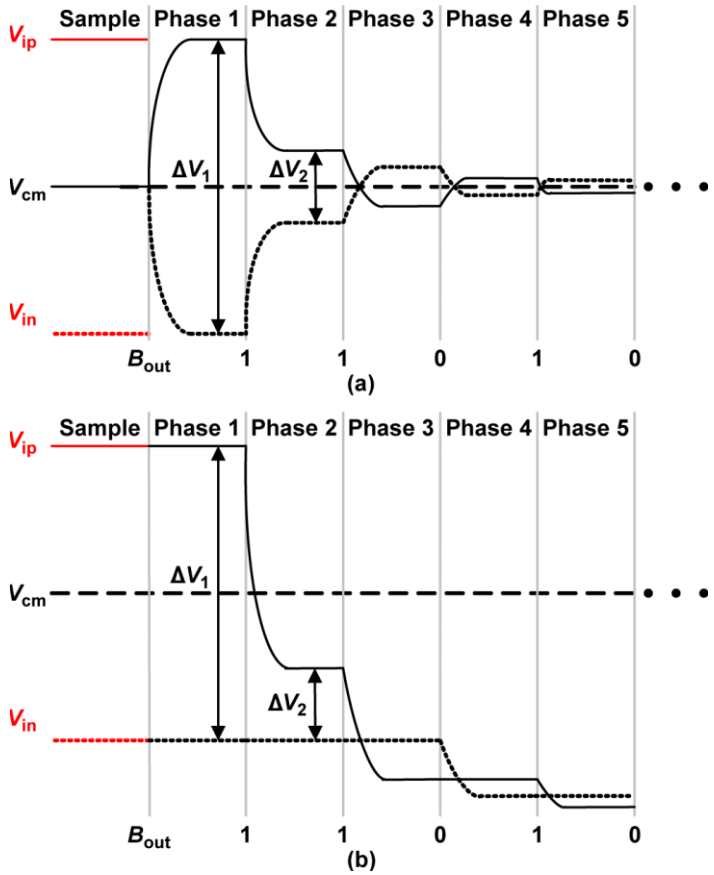

Figure 7–22: (a) Waveform of conventional switching procedure. (b) Waveform of monotonic switching procedure.

7.6 Switches

7.6.1 A MOSFET:

A MOS transistor can serve as a simple switch when working in linear region. Its Ron is given by the following equation:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{Gate} - V_{in} - V_{Th})}$$

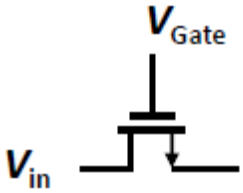

Figure 7–23:NMOS Switch

The main disadvantages:

- Ron is input dependent.

- Output is distorted due to the On-Resistance variation over large input ranges.

- In order to have a very small resistance we need a very large transistor.

7.6.2 Transmission Gate Switch:

NMOS and PMOS on-resistances move in opposite directions as shown in the following Figure 7-24.

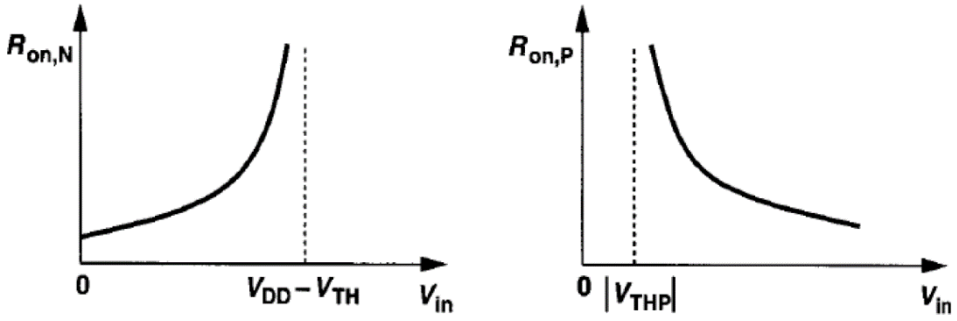

Figure 7–24: NMOS and PMOS Ron

Using Transmission Gate Switch provides us with smaller on-resistance and full rail to rail input swing as shown in Figure 7-25 and 2-26.

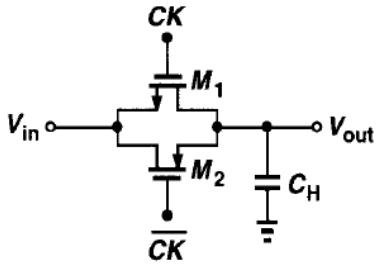

Figure 7–25: Gate Switch

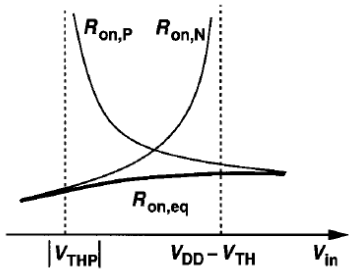

Figure 7–26: Gate Switch Ron

7.7 Comparators

The comparators are the decision makers in the analog circuits, they compare the instantaneous values and generate a digital “one” or “zero” indicating the polarity of the difference between the voltages. There are various types of analog circuits that can perform as comparators.

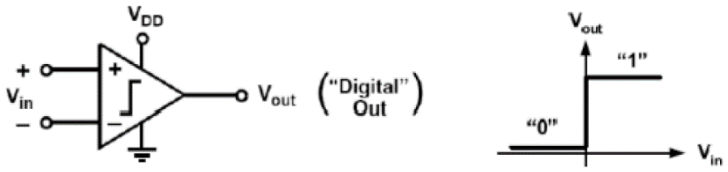

Figure 7–27: Decision Maker Concept

7.7.1 High Gain Amplifiers

Their idea of operation is to have very high gain that can amplify minimum input (which in case of ADCs determined by ADC resolution) to V_{dd}. But increasing gain of an amplifier decrease its bandwidth due to gain-bandwidth trade-off, so single stage high gain amplifier is often slow for majority of applications. Cascaded amplifiers with lower gain can achieve the desired gain, this allows a larger bandwidth for every stage, however the more stages with a certain bandwidth $\boldsymbol{\omega_o}$ are cascaded, the lower the overall bandwidth $\boldsymbol{\omega_{3dB}}$, but there is an optimum number of stages “N” at which the $\boldsymbol{\omega_{3dB}}$ is maximized for the cascaded stages.

$$H(s) = \frac{A_o}{1+\frac{s}{\omega}} \text{ (per stage)}$$

$$\omega_{3dB} = \omega_o\sqrt{\sqrt[N]{2}-1}$$

$$\omega_o = GBW / \sqrt[N]{A_{Total}}$$

$$\omega_{3dB} = GBW\frac{\sqrt{\sqrt[N]{2}-1}}{\sqrt[N]{A_{Total}}}$$

- For max. $\boldsymbol{\omega_{3dB}}$:

$$N_{opt} = 2\ln(A_{Total})$$

7.7.2 Latched comparators

Latched comparators depend on positive feedback, latched comparator consists of two inverters back to back to achieve the positive feedback, amplification stage is sometimes needed for the comparator to latch. The latched comparator output can reach the supply rails and its output grows exponentially so it has much faster response than cascaded amplifiers. Latched comparator operation has two main phases:

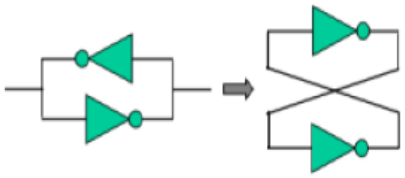

Figure 7–28: Latched Comparator Basic Concept

1- Reset phase (tracking phase): in this phase the input is tracked and sampled at the end of the phase.

2- Latch phase (regeneration phase): in this phase, the sampled input sets the initial condition for the positive feedback latch which amplifies the input exponentially.

However, the latched comparators have great advantages, they suffer from two issues which greatly affect their operation. The first is the high offset, and this high offset can be solved by adding a pre-amplifier stage, Figure 7-29 shows a latched comparator with a preamplifier stage. The second issue is called kick-back noise, and this occurs because the output nodes reach supply rails very fast, this large swing is coupled to the input signal through parasitic capacitances and this may affect the result of the following comparisons. Kick-back noise can be avoided by isolating output and input nodes.

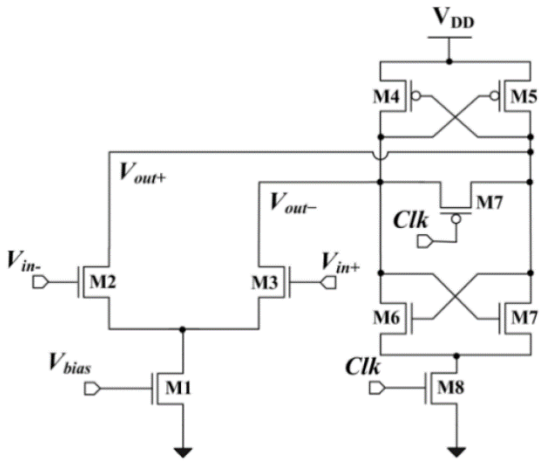

Figure 7–29: Latched comparator with Preamplifier

7.8 System Required Specifications:

Quantity	Value
Effective Number of Bits	8 bits
Supply	1 volt
Input range	150m-700m
Clock Frequency	26 MHz
Throughput	2 MSPS
Current Consumption	<350 µA
Offset error	< 5 LSB
Gain error	< 2 LSB
Latency	<500 ns
Delay	<0.25 $cycle$

Table 7–2: System Requirements

7.9 Proposed Design

According to the required specifications, we chose SAR ADC due to its low power consumption with capacitive binary weighted DAC and monotonic switching scheme with constant common mode to avoid non-linearity complications. And a strong arm comparator (explained later) with a differential preamplifier. NMOS for DAC switches and Transmission Gate for the sampling switches. A fully differential architecture suppresses the substrate and supply noise and has good common-mode noise rejection.

7.10 Ideal Design and Simulations

First of all, we have $\frac{26M}{2M} = 13\ cycles$ for each output. We will divide them as follows: 5 for sampling and 8 for bits as shown in Figure 7-30. Keeping in mind that all SAR decisions are positive edge triggered while Comparator decisions are negative edge triggered.

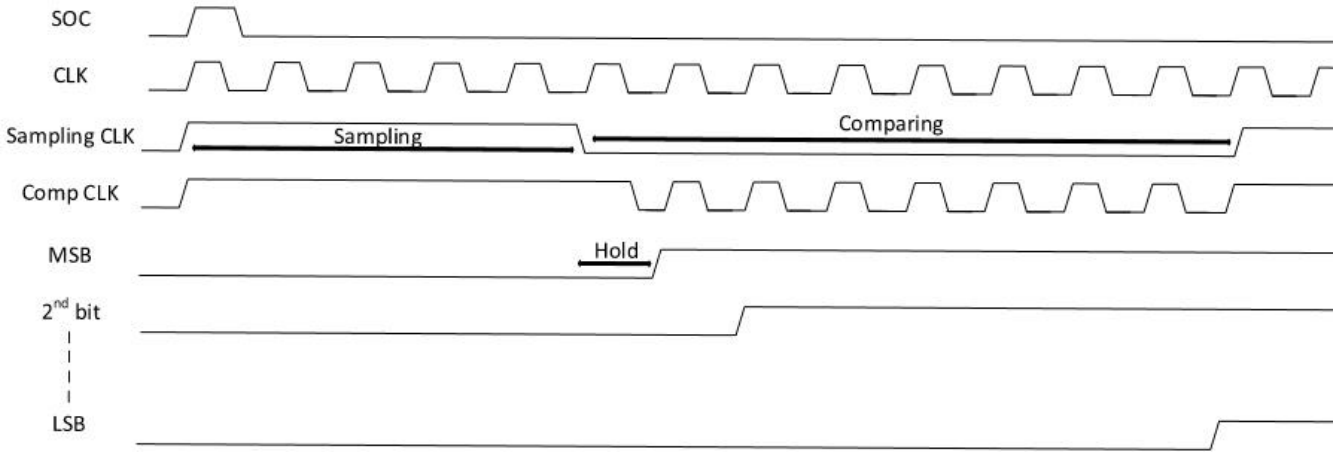

Figure 7–30: Detailed Timing Diagram of Operation

With SAR, Comparator and Ideal DAC Verilog-A models and Ideal Switches. Taking V_{ref}= 275mv and V_{CM}= 137.5mv. A test with a Sine wave of frequency $(\frac{29}{512}) \times 26M$, amplitude of 275mv and offset of 425mv on the positive input of comparator. A constant DC input of value 425mv on the negative input of comparator.

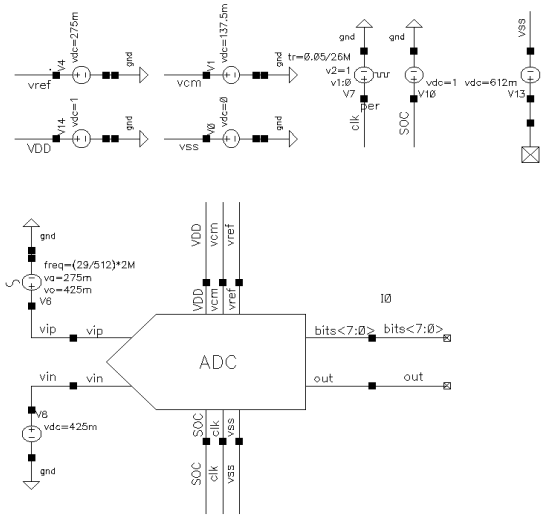

Figure 7–31: ADC Block

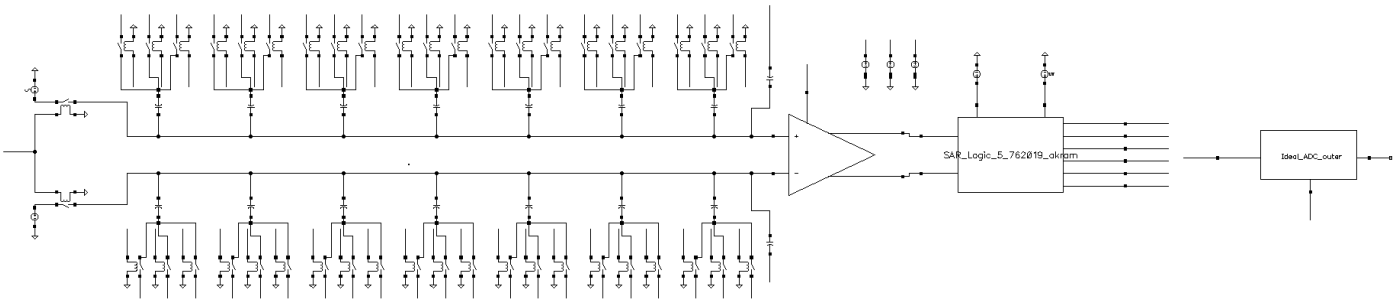

Figure 7–32: Ideal ADC Test bench

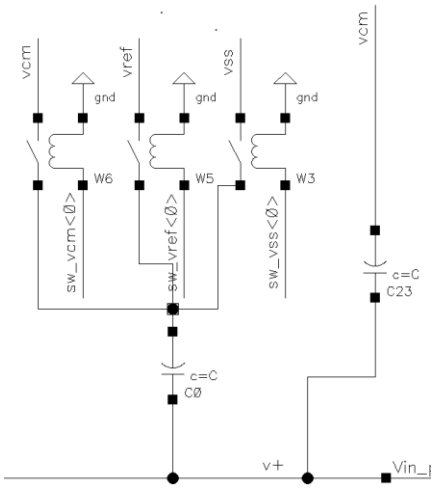

Figure 7–33: Ideal DAC Switch Schematic

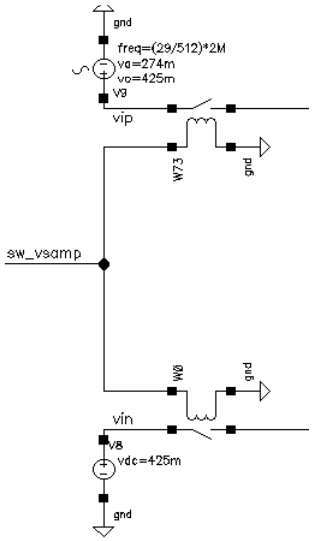

Figure 7–34: Ideal Sampling Switches Schematics

Figure 7-32 shows the test bench of the Ideal ADC schematics and Figure 7-33 shows the capacitive DAC switches schematic, where each capacitor is connected to 3 switches, each with different control produced by the SAR logic and connected to either V_{cm}, V_{ref} or V_{ss}. While the sampling switches are connected directly to the input terminals as illustrated in Figure 7-34. And Figure 7-35 shows the timing diagram as the explained in Figure 7-29.

Figure 7-36 shows the steps and the holding time (1.5 cycle) in order for the comparator to compare. Holding time can be decreased till 0.5 cycle if the input buffer needs more time to settle so this gives the buffer more flexibility.

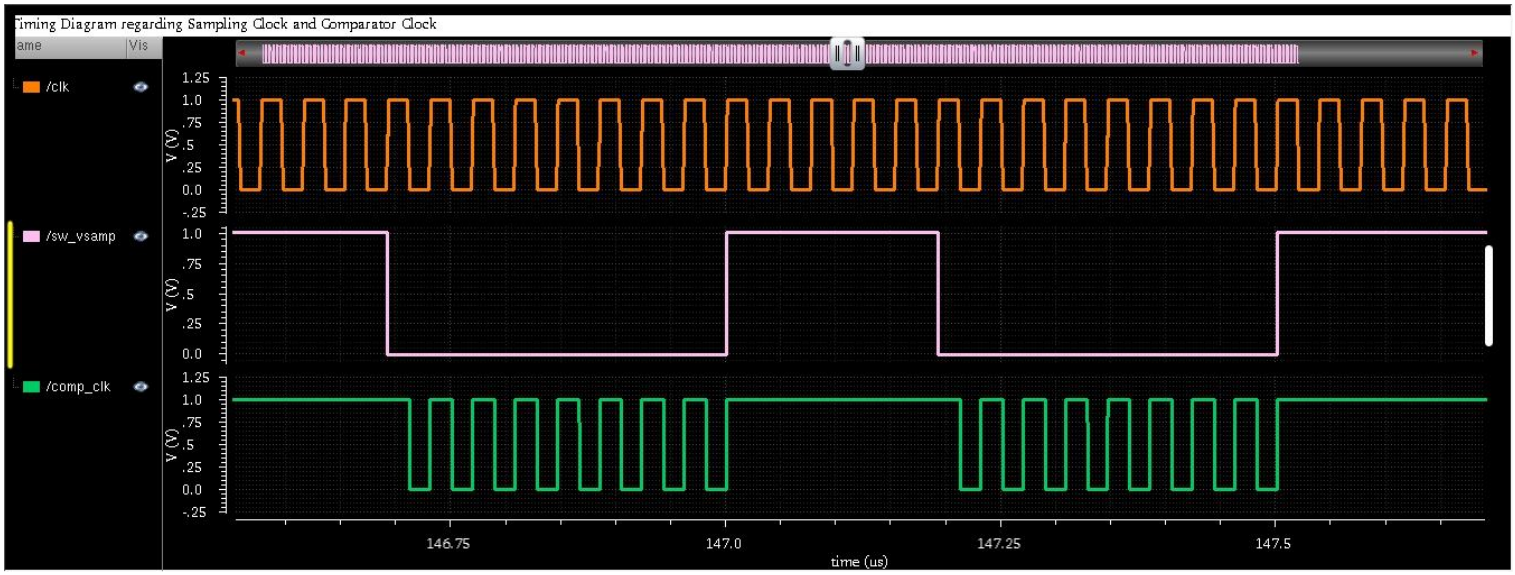

Figure 7–35: Timing Diagram regarding sampling clock and comparator clock

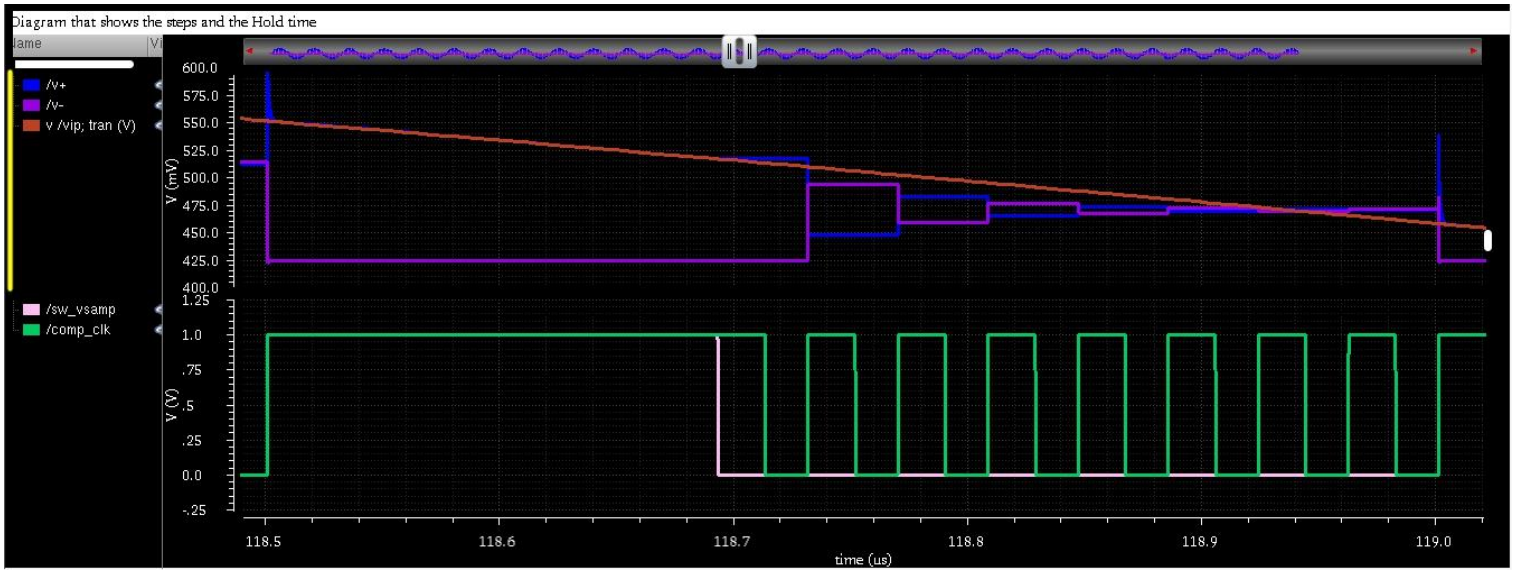

Figure 7–36: Diagram that shows the steps and hold time

Figure 7-37 shows the PSD of the quantized output signal with SFDR = 72.7 dB, SNDR = 49.68 dB and ENOB = 7.96.

ENOB Expression:

```
(dB10((integ((mag(dft(v("/out" ?result "tran") 2.5e-06 (2.5e-06 + (512.0 / 2000000.0)) 512 "Hanning" 1 "default"))**2) ((28.0 / 512) * 2000000.0) ((30.0 / 512) * 2000000.0)) / (integ((mag(dft(v("/out" ?result "tran") 2.5e-06 (2.5e-06 + (512.0 / 2000000.0)) 512 "Hanning" 1 "default"))**2) ((2.0 / 512) * 2000000.0) ((27.0 / 512) * 2000000.0)) + integ((mag(dft(v("/out" ?result "tran") 2.5e-06 (2.5e-06 + (512.0 / 2000000.0)) 512 "Hanning" 1 "default"))**2) ((31.0 / 512) * 2000000.0) ((256.0 / 512) * 2000000.0))))) - 1.76) / 6.02
```

PSD Expression:

```
dB10((mag(dft(v("/out" ?result "tran") 2.5e-06 (2.5e-06 + (512.0 / 2000000.0)) 512 "Hanning" 1 "default"))**2)
```

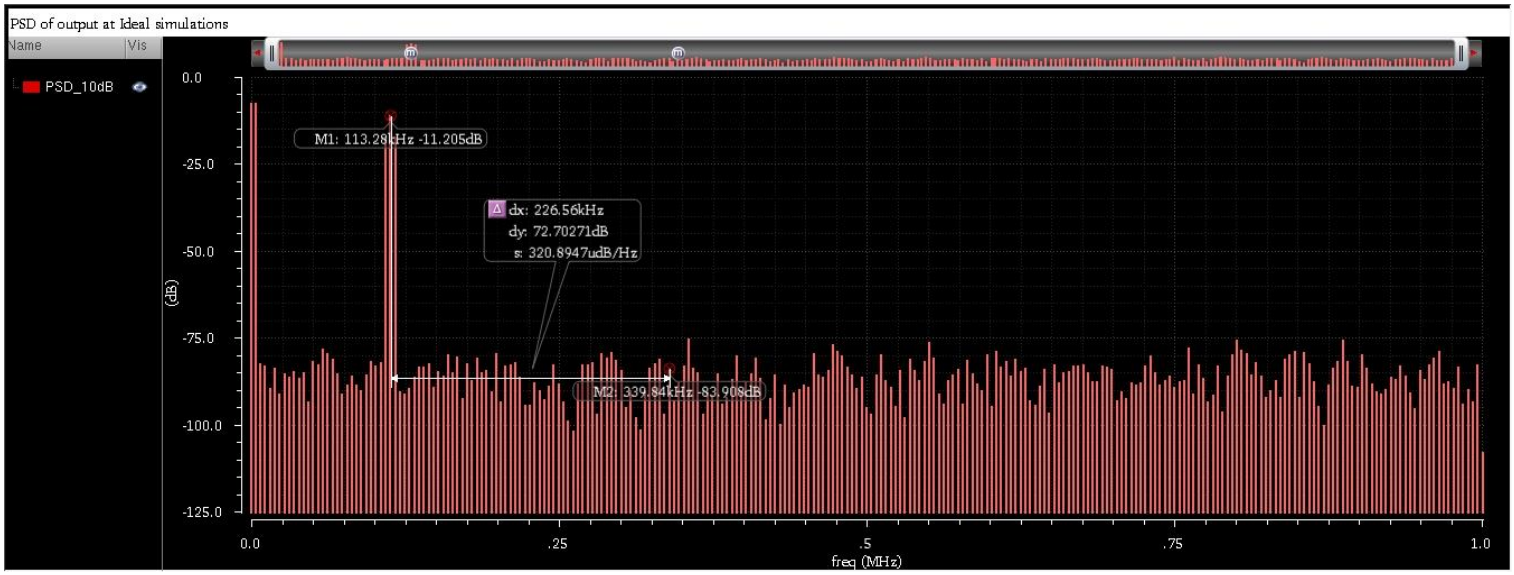

Figure 7–37: PSD and SFDR in dB

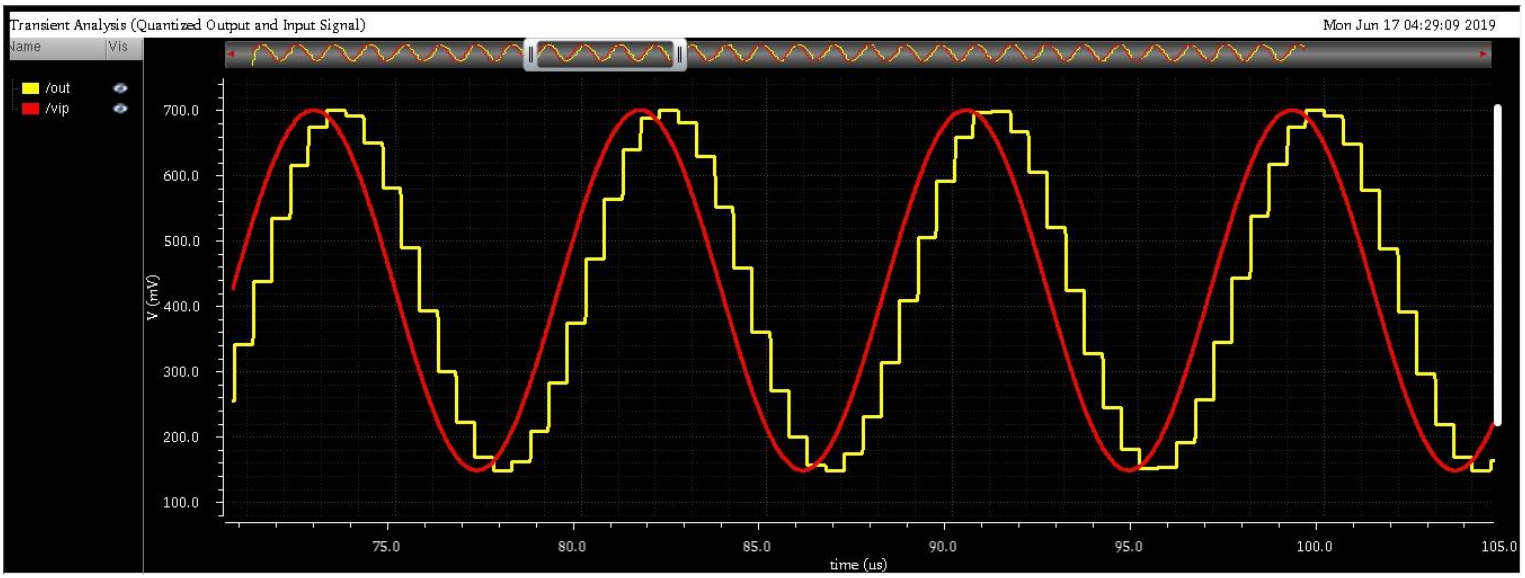

Figure 7–38: Quantized output and Input signal

7.10.1 Ideal Verilog-A Models

7.10.1.1 SAR Logic Verilog-A

```
// VerilogA for Akram_isa, SAR_Logic, veriloga
`include "constants.vams"
`include "disciplines.vams"
module SAR_Logic(SOC,comp_out,comp_out_bar,clk,sw_vsamp,sw_vcm,sw_vref,sw_vss,result,comp_clk);
// sw_Vref turns on Vrefp switch and turns on Vssn of the same Cap array
// sw_Vss turns on Vssp switch and turns on Vrefn of the same Cap array
// sw_Vcm turns on Vcm switches of DAC (Upper plates)
// sw_Vsamp turns on sampling switches for both terminals of comparator

input SOC;
input comp_out;
input comp_out_bar;
input clk;

output sw_vsamp;
output [6:0] sw_vcm;
output [6:0] sw_vref;
output [6:0] sw_vss;

output [7:0] result;
output comp_clk;


electrical comp_out;
electrical comp_out_bar;
electrical clk;
electrical SOC;

electrical sw_vsamp;
electrical [6:0] sw_vcm;
electrical [6:0] sw_vref;
electrical [6:0] sw_vss;

electrical [7:0] result;
electrical comp_clk;

parameter real vhigh = 1;
parameter real vlow = 0;
parameter real vth = 0.5;
parameter real trise = 0.1n from (0:inf);
parameter real tfall = 0.1n from (0:inf);
parameter real tconv = 0.1n from [0:inf);

real vsamp;
real vcm[6:0];
real vref[6:0];
real vss[6:0];
real finalresult[7:0];

integer SOC_in;
integer counter, i, j, k;

analog begin

        if (V(SOC)>vth) begin
                SOC_in=vhigh;
        end

        @(initial_step) begin
                                i=0;
                                j=1;
                                k=1;
                                counter=0;
                                vsamp=vlow;
```

```
                        generate i (6,0) begin
                                vcm[i]=vhigh;
                                vref[i]=vlow;
                                vss[i]=vlow;
                        end
end

@(cross(V(clk)-vth,1)) begin
        if (SOC_in==vhigh) begin
                        if (counter==0) begin
                                if (V(comp_out)-vth>0) begin
                                        finalresult[0]=vhigh;
                                end
                                else if (V(comp_out)-vth<0) begin
                                        finalresult[0]=vlow;
                                end
                                vsamp=vhigh;
                                generate i (6,0) begin
                                        vcm[i]=vhigh;
                                        vref[i]=vlow;
                                        vss[i]=vlow;
                                end
                        end

                        if (counter>0 && counter<5) begin
                                vsamp=vhigh;
                                generate i (6,0) begin
                                        vcm[i]=vhigh;
                                        vref[i]=vlow;
                                        vss[i]=vlow;
                                end
                        end

                        else if (counter == 5) begin
                                vsamp=vlow;
                        end

                        else if (counter == 6) begin
                                vsamp=vlow;
                                if (V(comp_out)-vth>0) begin
                                        finalresult[7]=vhigh;
                                        vcm[6]=vlow;
                                        vref[6]=vlow;
                                        vss[6]=vhigh;
                                end
                                else if (V(comp_out)-vth<0) begin
                                        finalresult[7]=vlow;
                                        vcm[6]=vlow;
                                        vref[6]=vhigh;
                                        vss[6]=vlow;
                                end
                        end

                        else if (counter>6 && counter<12) begin
                                vsamp=vlow;
                                if (V(comp_out)-vth>0) begin
                                        finalresult[7-k]=vhigh;
                                        vcm[6-j]=vlow;
                                        vref[6-j]=vlow;
                                        vss[6-j]=vhigh;
                                end
                                else if (V(comp_out)-vth<0) begin
                                        finalresult[7-k]=vlow;
                                        vcm[6-j]=vlow;
                                        vref[6-j]=vhigh;
                                        vss[6-j]=vlow;
                                end
                                j=j+1;
                                k=k+1;
                        end
```

```
                else if (counter == 12) begin
                        if (V(comp_out)-vth>0) begin
                                finalresult[7-k]=vhigh;
                                vcm[6-j]=vlow;
                                vref[6-j]=vlow;
                                vss[6-j]=vhigh;
                        end
                        else if (V(comp_out)-vth<0) begin
                                finalresult[7-k]=vlow;
                                vcm[6-j]=vlow;
                                vref[6-j]=vhigh;
                                vss[6-j]=vlow;
                        end
                        k=1;
                        counter=-1;
                        j=1;
                end

                //else if (counter>12) begin
                //      counter=-1;
                //      i=0;
                //      j=0;
                //      k=1;
                //      vsamp=vhigh;
                //      generate i (6,0) begin
                //              vcm[i]=vhigh;
                //              vref[i]=vlow;
                //              vss[i]=vlow;
                //      end
                //end

                //if (j>6) begin
                //      j=0;
                //end

                //if (k>7) begin
                //      k=1;
                //end
                counter=counter+1;
        end
    end

    generate i (7,0) begin
        V(result[i])<+ transition(finalresult[i], tconv, trise, tfall);
    end
    generate i (6,0) begin
        V(sw_vcm[i])<+ transition(vcm[i], tconv, trise, tfall);
        V(sw_vref[i])<+ transition(vref[i], tconv, trise, tfall);
        V(sw_vss[i])<+ transition(vss[i], tconv, trise, tfall);
    end

    V(sw_vsamp)<+ transition(vsamp, tconv, trise, tfall);
    V(comp_clk)<+ transition((V(clk) || vsamp), tconv, trise, tfall);

end

endmodule
```

7.10.1.2 Comparator Verilog-A

```
// VerilogA for Akram_isa, Comparator_1, veriloga

`include "constants.vams"
`include "disciplines.vams"

module C_1(Vout,Vout_bar,Vin_p,Vin_n,clk);

input Vin_p;
input Vin_n;
input clk;

output Vout;
output Vout_bar;

electrical Vout;
electrical Vout_bar;
electrical Vin_p;
electrical clk;
electrical Vin_n;

parameter real vhigh = 1;
parameter real vlow = 0;
parameter real vth = 0.5;
parameter real trise = 0.1n from (0:inf);
parameter real tfall = 0.1n from (0:inf);
parameter real tconv = 0.1n from [0:inf);
real Vout_val;
real Vout_val_bar;
integer act_comp= vlow;

        analog begin


                // Reset phase:
                //if (V(clk)==vhigh) begin
                        //Vout_val = vlow;
                        //Vout_val_bar= vlow;
                //end

                // Compare phase:
                @(cross(V(clk)-vth, -1)) begin
                        if ( (V(Vin_p)) - (V(Vin_n)) >= 0 ) begin
                                Vout_val = vhigh ;
                                Vout_val_bar = vlow;
                        end
                        else if ( (V(Vin_p)) - (V(Vin_n)) < 0 ) begin
                                Vout_val = vlow ;
                                Vout_val_bar = vhigh;
                        end
                end

                V(Vout) <+ transition ( Vout_val , tconv, trise, tfall );
                V(Vout_bar) <+ transition (Vout_val_bar, tconv, trise, tfall);

        end

endmodule
```

7.10.1.3 Ideal DAC Verilog-A

```
// VerilogA for Akram_isa, Ideal_ADC_outer, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Ideal_ADC_outer(resultbits,out,ctrl);

input ctrl;
input [7:0] resultbits;

output out;

electrical ctrl;
electrical [7:0] resultbits;

electrical out;

parameter real vhigh = 1;
parameter real vlow = 0;
parameter real vth = 0.5;
parameter real trise = 0.1n from (0:inf);
parameter real tfall = 0.1n from (0:inf);
parameter real tconv = 0.1n from [0:inf);

real out_in;
real resultbits_in[7:0];

integer i;

analog begin

        if (V(ctrl)>vth) begin
                generate i(7,0) begin
                        if (V(resultbits[i])>vth) begin
                                resultbits_in[i]=vhigh;
                        end
                        else if (V(resultbits[i])<vth) begin
                                resultbits_in[i]=vlow;
                        end
                end

                out_in=((0.55/255)*(resultbits_in[0]*1 + resultbits_in[1]*2 + resultbits_in[2]*4 +
resultbits_in[3]*8 + resultbits_in[4]*16 + resultbits_in[5]*32 +
resultbits_in[6]*64+resultbits_in[7]*128))+0.15;
        end

        V(out)<+ transition (out_in, tconv, trise, tfall);

end

endmodule
```

7.11 Actual Design and Simulations:

7.11.1 Unit Capacitor (C_u) choice

Choosing the unit capacitor value of the capacitive DAC depends on Thermal Noise, Capacitor mismatch and parasitic capacitances.

Regarding the thermal Noise, thermal noise must be less than quantization noise.

$$Quantization\ noise = \frac{\Delta^2}{12} = \frac{(\frac{V_{ref}}{2^8})^2}{12} = 384.6486\ nJ$$

$$Thermal\ Noise = \frac{KT}{2^8 \times C_u}$$

Where T= 125 C, for mimcap technology the minimum value is 10fF and the following table shows sweeping the value of capacitor and calculated thermal noise.

C_u (fF)	Thermal Noise (nJ)
10	2.147366
15	1.431577
20	1.073683
25	0.858946
30	0.7157886
35	0.613533
40	0.5368415

Table 7–3: Sweeping Capacitor value and corresponding thermal noise

From the above table, it is observed that any value of capacitor will satisfy the thermal noise condition.

Regarding capacitor mismatch, the condition is as follows:

$$\sigma_{DNL} < \frac{1}{2}$$

$$3\sigma_u\sqrt{2^8 - 1} < \frac{1}{2}$$

$$\sigma_u < \frac{1}{6 * \sqrt{2^8 - 1}}$$

$$\sigma_u < 0.0104$$

In order to calculate the value of σ_u, we construct the following test bench as Figure 7-39 illustrates and measure the value of the capacitor at frequency of 26 MHz, then run Monte Carlo mismatch simulation with different values of capacitor.

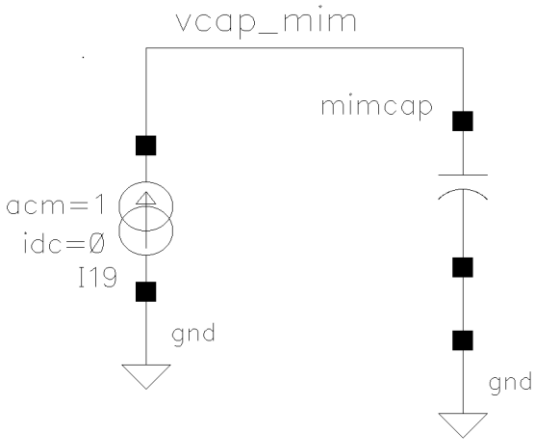

Figure 7–39: Capacitor mismatch test bench

$$Z = \frac{V}{I} = \frac{V}{1} = \frac{1}{j\omega C}$$

$$C = \frac{Imj\ (\frac{1}{V})}{2\pi f}$$

Capacitor value expression:

```
value((imag((1 / VF("/vcap_mom"))) / (2 * 3.1415 * 26000000)) 26000000)
```

C_u (fF)	σ_u
10	0.003117
15	0.00254
20	0.0021805
25	0.001938
30	0.001761333
35	0.0016257
40	0.00151575

Table 7–4: Sweeping Unit Capacitor and corresponding Mismatch value

Since all the values are less than the required σ_u, so any value is acceptable.

Regarding the parasitic capacitance, the C_{gg} of the differential pair in the preamplifier restricted as to take C_u > 35fF (explained later) in order to be less affecting and gain a good ENOB. However, increasing the value of the unit capacitor will increase the load on the reference buffer and affects the GBW negatively (Trade-off between C_u and C_L on the reference buffer).

7.11.2 DAC Switch:

As explained before, the DAC switches are going to have 3 probabilities: either connected to V_{ref}, V_{cm} or V_{ss}. Bearing in mind that the control signal that closes the switch is V_{dd} which is connected to the gate of the MOSFET. So our worst case here is when it is connected to V_{ref} = 0.275mv, so V_{GS} = 0.725mv. So taking the switch as NMOS Switch is the most suitable choice.

One thing left to calculate is its on-resistance as follows:

$$V_o(t) = V_{FS}\,(1 - e^{\frac{-t}{\tau}})$$

$$error < 0.5\ LSB$$

$$V_{FS}\ e^{\frac{-t}{\tau}} < 0.5\ LSB$$

$$550\ x\ 10^{-3} e^{\frac{-t}{\tau}} < 0.5\ x\ 2.1484\ x\ 10^{-3}$$

$$\frac{t}{7\ x\ C} <\ R_{on}$$

Since, $t = 0.25x\frac{1}{26M}$ and $C = 35\ fF$

$$R_{on} < 39.246\ K\Omega$$

In order to simulate the R_{on} of the NMOS the following test bench is used and measuring the worst case on-resistance as illustrated in Figure 7-40.

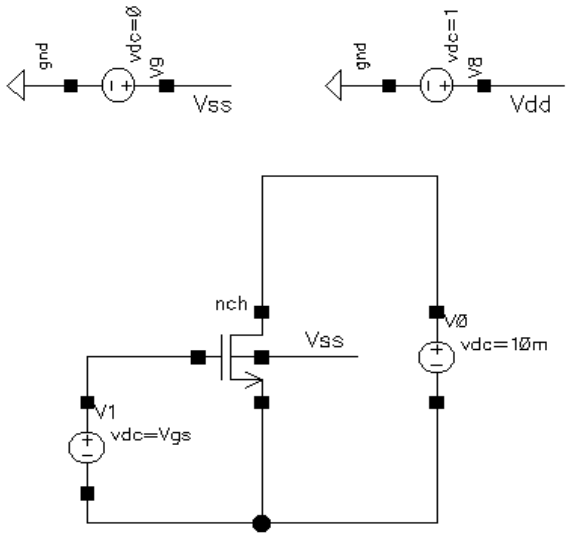

Figure 7–40: NMOS on-resistance Test bench

And by running ENOB simulations with smaller R_{on}, it gives better ENOB. So we decreased the required R_{on} more than the condition. And we swept the fingers of NMOS and choose N=4.

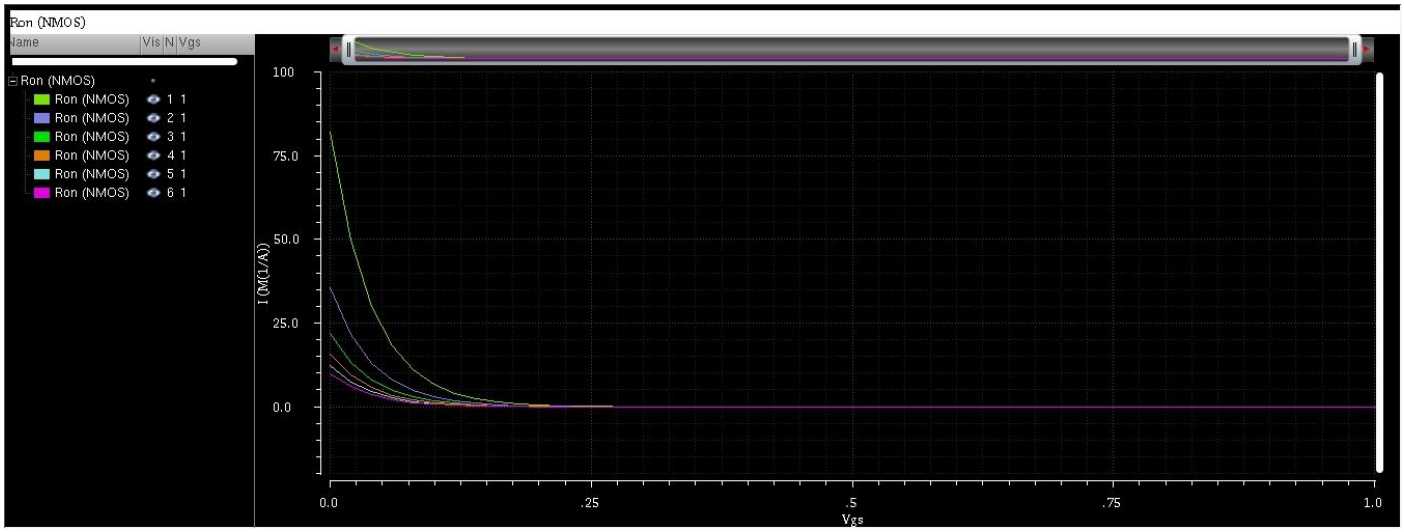

Figure 7–41: Ron of NMOS with different Fingers (N)

Transistor	L	W	Fingers
NMOS	60n	600n	4

Table 7–5: DAC Switch NMOS Sizing

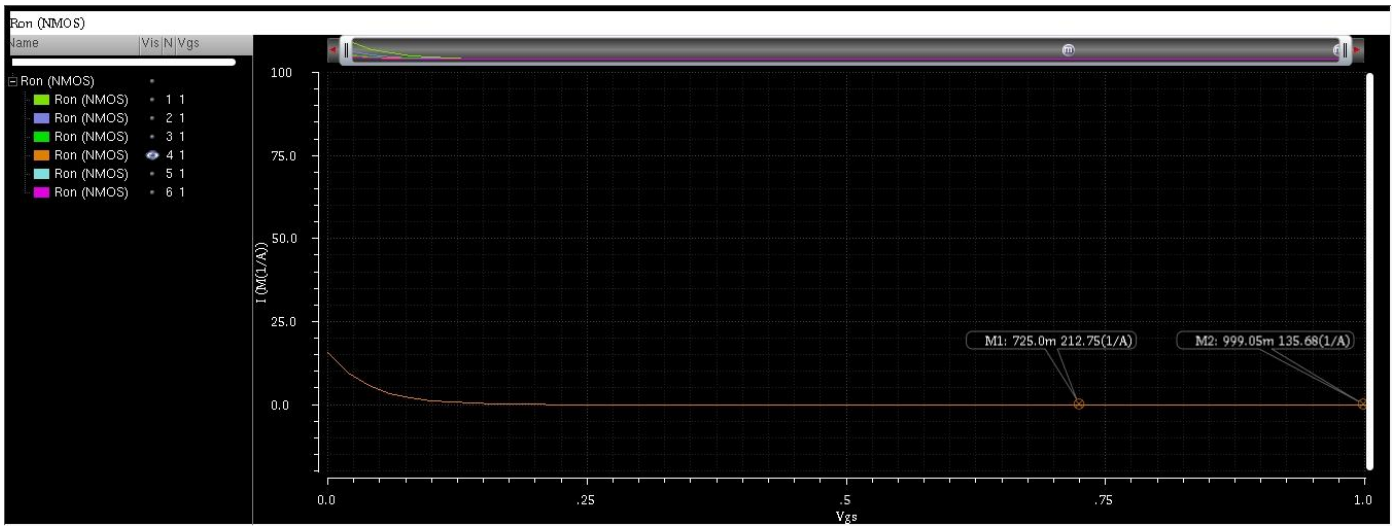

Figure 7–42: Ron of selected NMOS

Figure 7-43 and Figure 7-44 show the unit capacitor symbol with NMOS switches and its schematics.

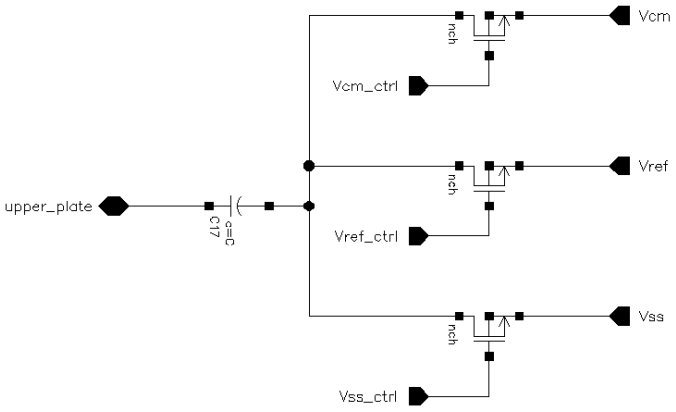

Figure 7–43: NMOS as switches in DAC

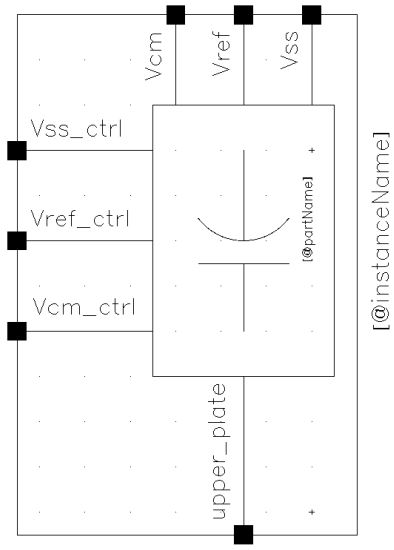

Figure 7–44: Unit Capacitor with switches Symbol

And the following figures show the DAC using the previous symbols and its symbol.

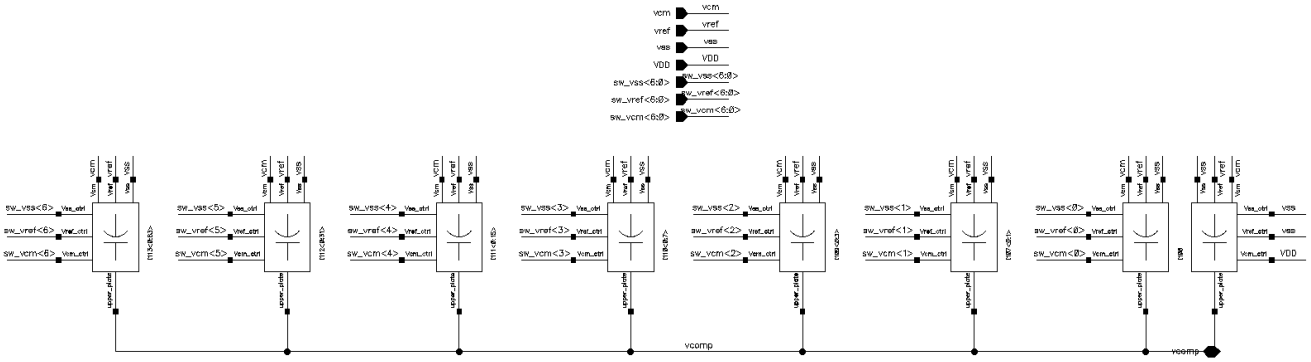

Figure 7–45: Schematic of DAC using Unit Capacitor

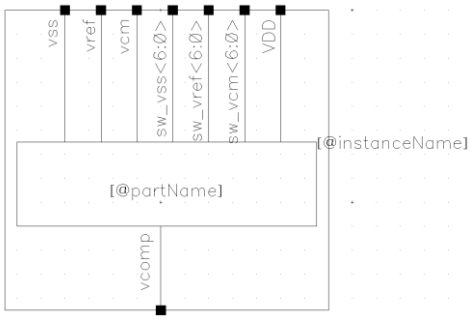

Figure 7–46: DAC symbol

Simulating ENOB with only DAC switches and mimcap gives ENOB = 7.96, SNDR =49.68 dB, SFDR = 72.2 dB

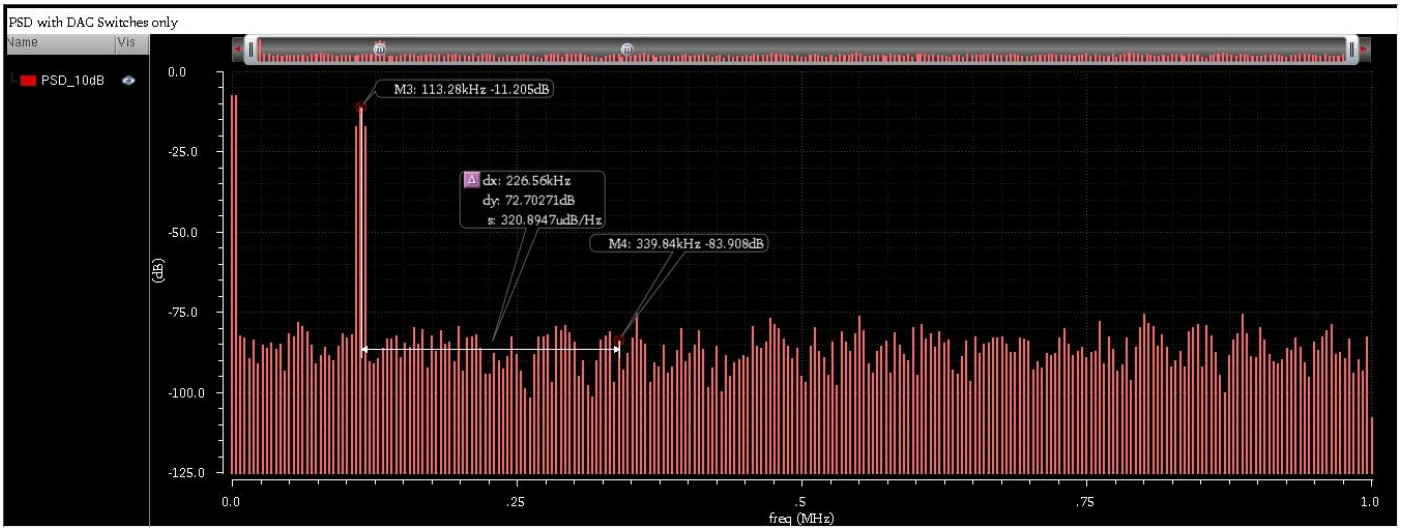

Figure 7–47: PSD and SFDR with DAC Switches only

7.11.3 Sampling Switch

Since out input range is from 150mv to 700 mv, so Transmission Gate is a logical choice of switch. As for low input, NMOS samples the input. As for high input, PMOS samples the input. While for input in the middle range, both NMOS and PMOS samples the input and act as parallel MOSFETs. One thing left to calculate is its on-resistance as follows:

$$V_o(t) = V_{FS}\,(1 - e^{\frac{-t}{\tau}})$$

$$error < 0.5\ LSB$$

$$V_{FS}\, e^{\frac{-t}{\tau}} < 0.5\ LSB$$

$$550\ x\ 10^{-3} e^{\frac{-t}{\tau}} < 0.5\ x\ 2.1484\ x\ 10^{-3}$$

$$\frac{t}{7\ x\ C} < R_{on}$$

Since, $t = 2.5x\frac{1}{26M}$ and $C = 2^8 \times 35\ fF$

$$R_{on} < 1.533\ K\Omega$$

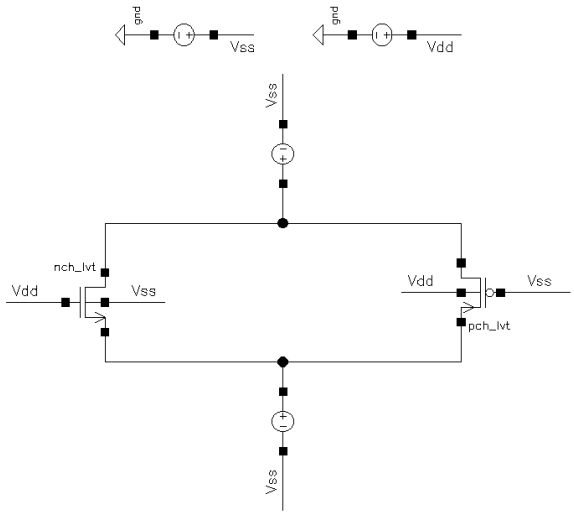

Figure 7–48: TG LVT Test Bench

In order to simulate the R_{on} of the TG, the following test bench is used as illustrated in Figure 7-48, where the bottom DC source is V_{gs} and the top DC source is V_{gs}+10mv in order to keep the voltage drop over the transistor constant and equals to 10mv, where $R_{on} = \frac{0.01}{I_{dc_{NMOS}} + I_{dc_{PMOS}}}$.

We used LVT to reduce the peak of the bell-shaped R_{on} and sizing was decided to make R_{on} as symmetric as possible along the range of input while keeping the condition above even at corners. First we swept the fingers of the TG until we reached the sizing that gives the required R_{on} as shown in Figure 7-49.

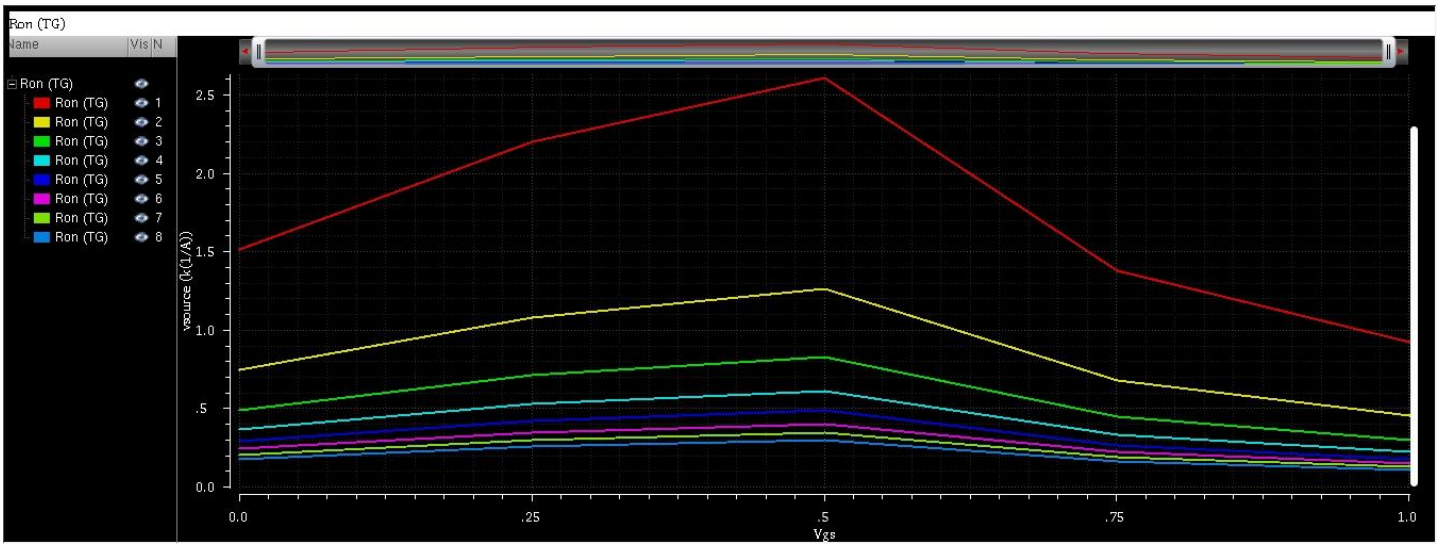

Figure 7–49: TG Ron with different Fingers

N=6 satisfies the condition and shows a good symmetric behavior for different input ranges. Figure 7-50 shows the critical corners for the TG and Table 7-6 shows the final sizing.

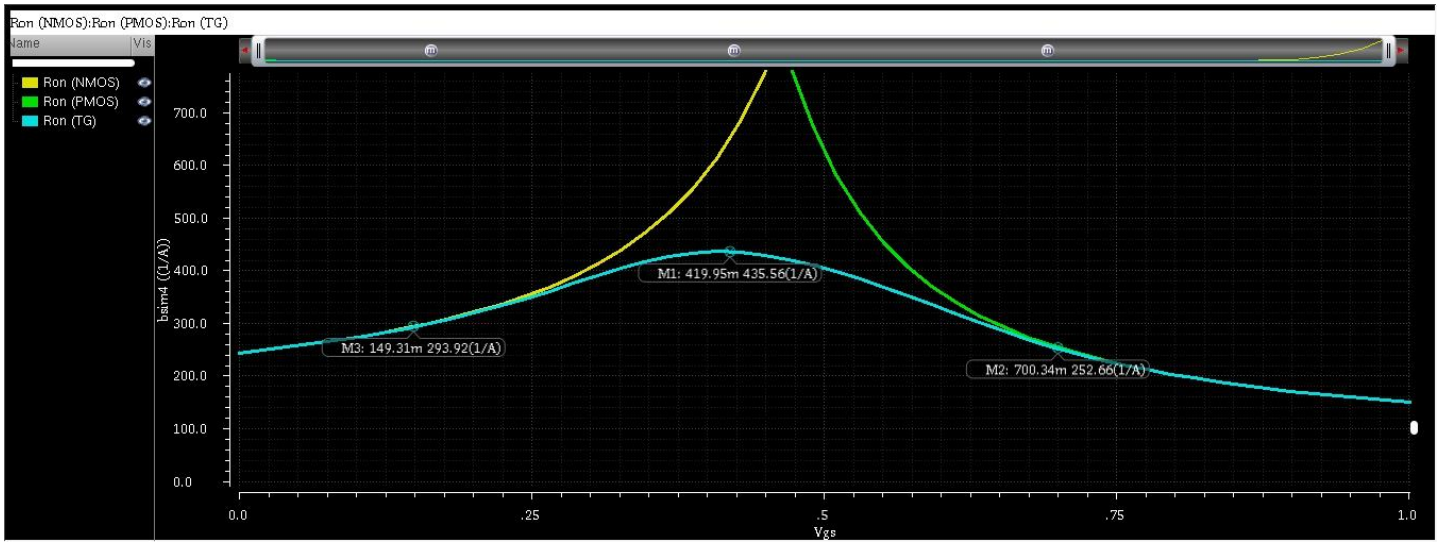

Figure 7–50: Ron at Fingers N=6

cor_std_mos.scs	temperature	Pass/Fail	Ron (TG)
ff	-40		241.3
ff	125		252.5
ss	-40		1.171k
ss	125		793.6
tt	-40		481.4
tt	125		419.1

Figure 7–51: Ron at corners

Transistor	L	W	Fingers
NMOS	60n	200n	6
PMOS	60n	1µ	6

Table 7–6: TG LVT Sizing

After testing corners and closing the decision on the sizing, Figures 7-52 & 7-53 illustrate the Transmission Gate schematics and its symbol.

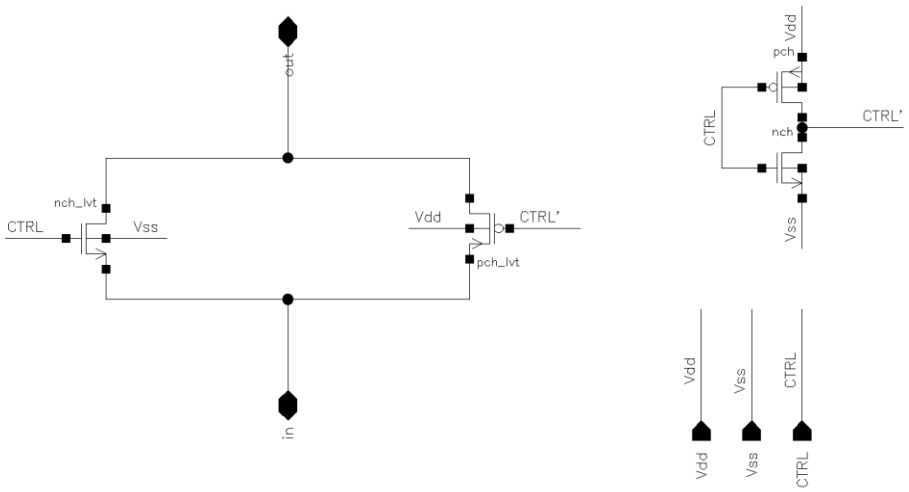

Figure 7–52: Transmission Gate Schematics

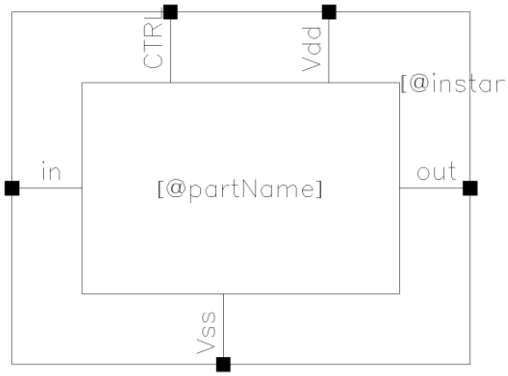

Figure 7–53: Sampling Switch symbol

As observed from the Sampling switch schematics, there is an inverter used to invert the control signal. In order to work properly, the NMOS and PMOS must have same speed when inverting. So in Figure 7-54, a test bench with an input of ramp from 0 to 1 volt, to decide the ratio of width between NMOS and PMOS to have similar speed. And Figure 7-55 shows that a width of 466n for PMOS should be correct (ratio of 2.33).

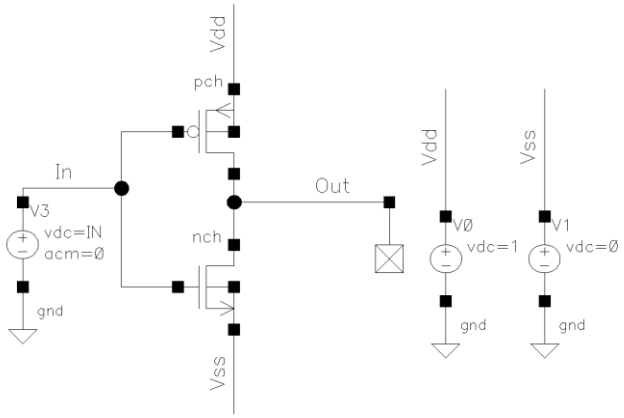

Figure 7–54: Inverter Test bench

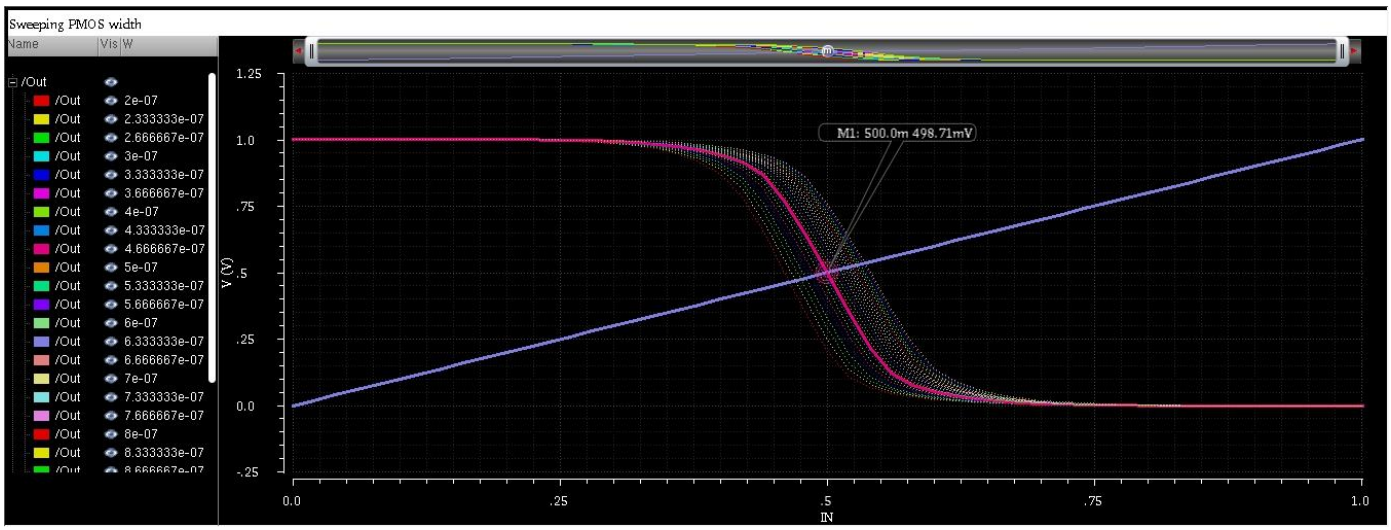

Figure 7–55: Sweeping PMOS width to determine proper ratio in an inverter

Transistor	L	W	Fingers
NMOS	60n	200n	1
PMOS	60n	465n	1

Table 7–7: Inverter proper sizing

Simulating the Sampling switch only, turns out with ENOB=7.962, SNDR=49.69 dB and SFDR= 80 dB

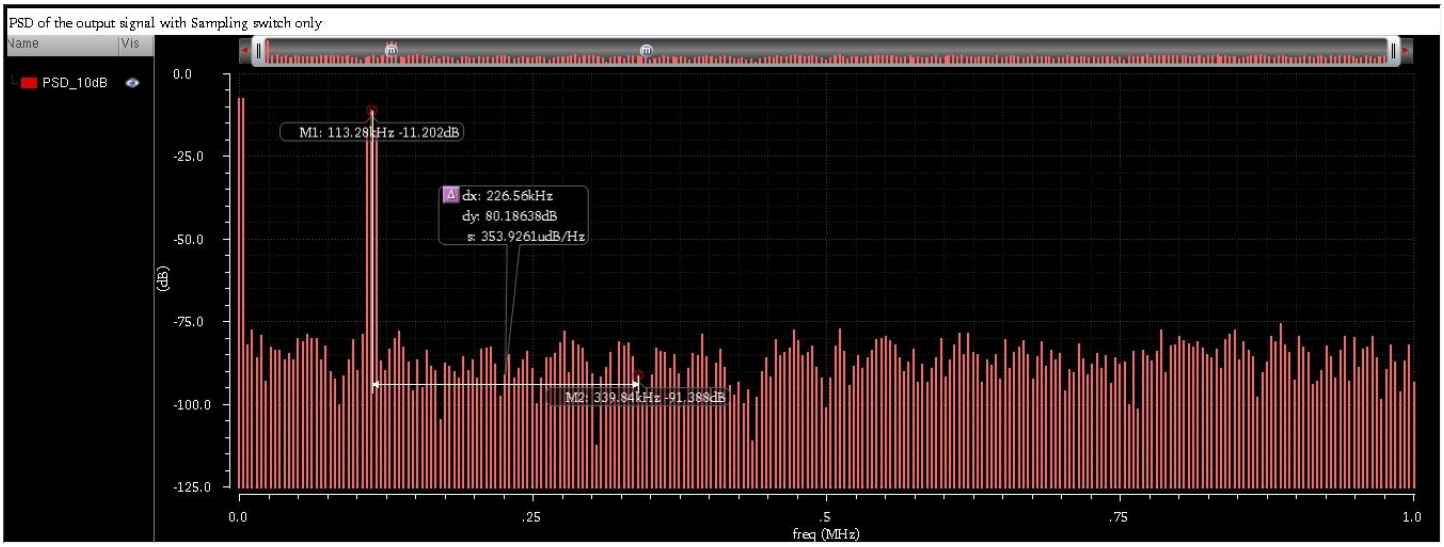

Figure 7–56: PSD of the output signal with Sampling switch only

With Sampling switch delay ~ 110psec

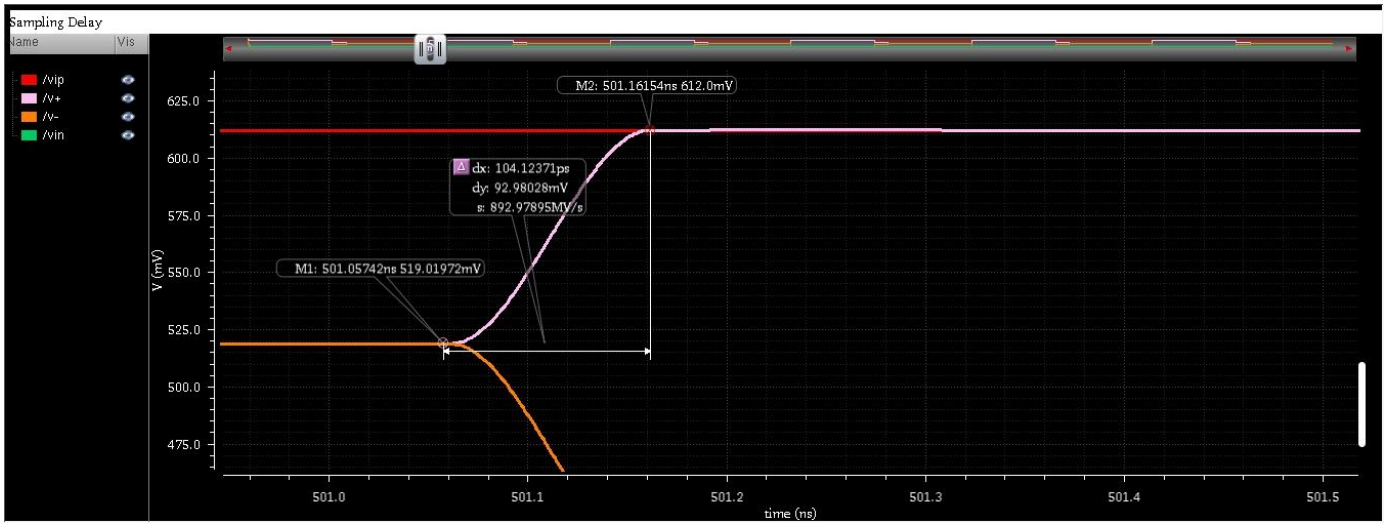

Figure 7–57: Transient Simulation to measure the sampling delay

7.11.4 Comparator

For the comparator design, StrongArm Latch is chosen with a differential preamplifier. The StrongARM latch has become popular for three reasons:

1) It consumes zero static power

2) It directly produces rail-to-rail outputs

3) Its input-referred offset arises from primarily one differential pair.

We used a modified StrongArm latch topology and it is explained as follows:

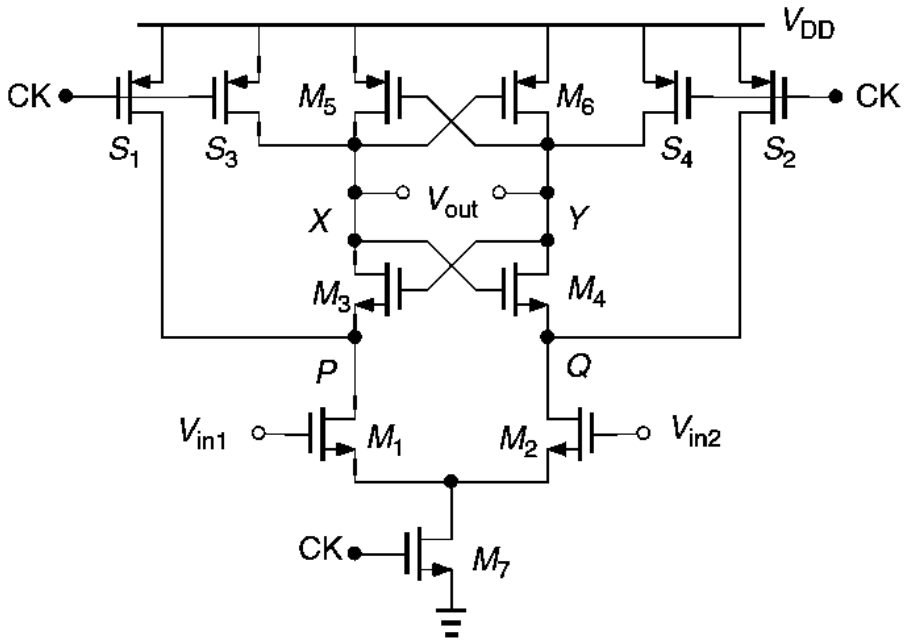

Figure 7–58: Modified StrongArm Topology Schematics

The latch of Figure 7-58 consists of a clocked differential pair, M_1–M_2, two cross-coupled pairs, M_3–M_4 and M_5–M_6, and four pre-charge switches, S_1–S_4. The circuit provides rail-to-rail outputs at X and Y in response to the polarity of V_{in1} - V_{in2}. We describe the operation in four phases:

In the first phase, CK is low; M_1 and M_2 are off; nodes P, Q, X, and Y are pre-charged to V_{dd}.

In the second phase, CK goes high, S_1–S_4 turn off, and M_1 and M_2 turn on, drawing a differential current in proportion to V_{in1} - V_{in2}. With M_3–M_6 initially off, this current flows from C_P and C_Q, thereby allowing V_P - V_Q to grow and possibly exceed V_{in1} - V_{in2}. That is, this phase can provide voltage gain. We call this phase the amplification mode. Since the tail current is fairly constant during this period.

As V_P and V_Q fall to V_{dd} - V_{THN}, the cross-coupled NMOS transistors turn on (third phase), allowing part of the drain currents of M_1 and M_2 to flow from X and Y.

The output voltages V_X and V_Y continue to fall until they reach V_{dd} - V_{THP}, at which point M_5 and M_6 turn on and the circuit enters the fourth phase. The positive feedback around these transistors eventually brings one output back to V_{dd} while allowing the other to fall to zero.

First, the pre-amplifier is used to isolate the input and output nodes to avoid the kick-back noise and also to decrease the offset error. Figure 7-59 shows the schematic of the differential amplifier, PMOS is used due to the fact of V_{cm} = 425 mv, also the addition of helper NMOS mirror is to decrease the current passing through the resistor and enable us to get more gain.

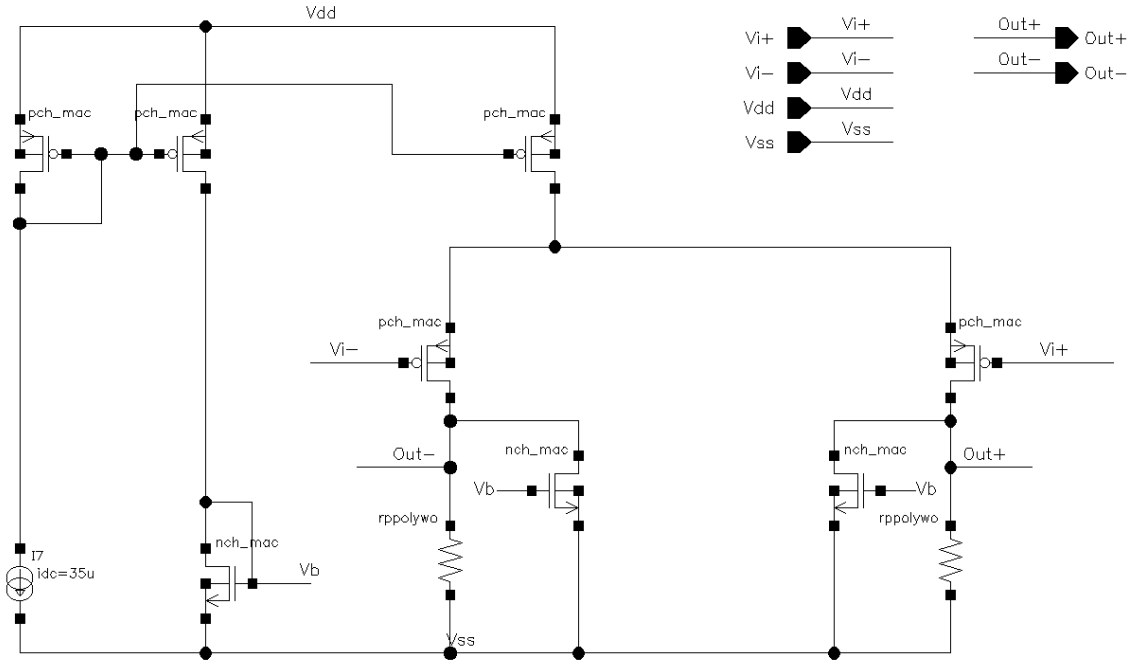

Figure 7–59: Pre-amplifier Schematic

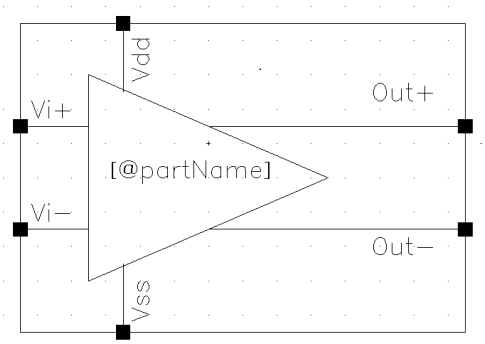

Figure 7–60: Pre-amplifier symbol

Transistor	L	W	Fingers
Main PMOS Mirror	600n	19µ	1
Tail PMOS	600n	19µ	4
PMOS Mirror for NMOS	600n	10µ	1
Main NMOS Mirror	200n	400n	1
PMOS Diff. Pair	130n	7.5µ	1
NMOS Helper	5µ	25µ	1
Resistor	40KΩ		

Table 7–8: Pre-amplifier Sizing

The process of sizing the pre-amplifier was tricky due to many important trade-offs. For example, for high gain, high gm is required and to get high gm you have to increase W and current, and increasing W leads to increasing the area which in return give high parasitic capacitances (C_{gg}) but on the other hand in favour of the mismatch and input referred noise. So satisfying gain, BW, input referred noise, minimum parasitic capacitances and mismatch conditions were not easy.

In this design C_{gg} which is the non-linear parasitic capacitance that affects the DAC directly was achieved to be 11.33fF, and that was a reason behind not choosing Unit Capacitor with value of 10fF as it passed all thermal and mismatch conditions but it must be of higher ratio from the parasitic capacitances in order to obtain correct steps and better ENOB. Also gm = 801.5µ , $r_{0_{DiffPair}} = 30\text{K}\Omega$, $r_{0_{Helper}} = 71\text{K}\Omega$.

Figure 7-61 shows the gain at 26 MHz which is 20.5 dB and the BW of the preamplifier.

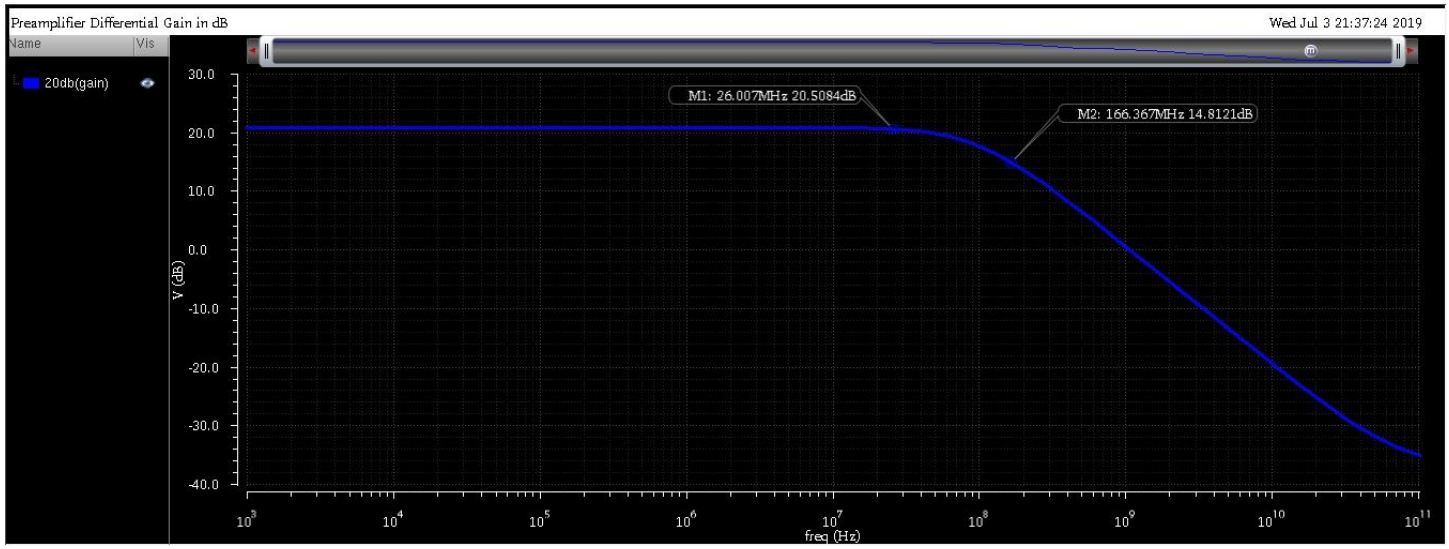

Figure 7–61: Preamplifier Gain and BW

As a result of the high gain, Input referred noise can be calculated from the preamplifier only and it must be less than $\frac{\Delta^2}{12} = 384.6\ nJ$.

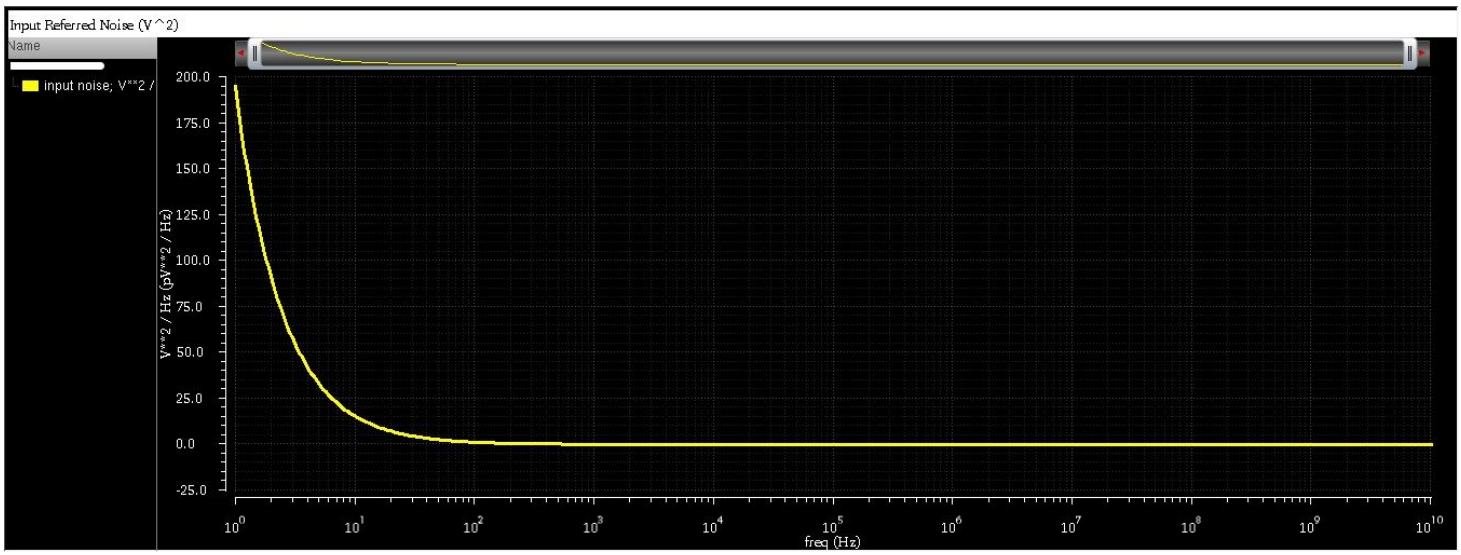

Figure 7–62: Input referred noise of preamplifier

```
Device    Param    Noise Contribution    % Of Tot
/M2       id       5.4278e-07            34.81
/M1       id       5.4278e-07            34.81
/M6       id       1.63856e-07           10.51

Integrated Noise Summary (in V^2) Sorted By Noise
Total Summarized Noise = 1.55942e-06
Total Input Referred Noise = 3.82588e-07
The above noise summary info is for noise data
```

Figure 7–63: Summery and contributors of the Input Referred Noise

Regarding the StrongArm latch, we have increased its size a little in order to help in giving more flexibility with mismatch system requirement. Figure 7-64 illustrates its schematics along with the SR Latch that holds the value of the comparator for 1.5 cycle in our case. Inverters are added between the comparator output and the SR latch to make it hold the value.

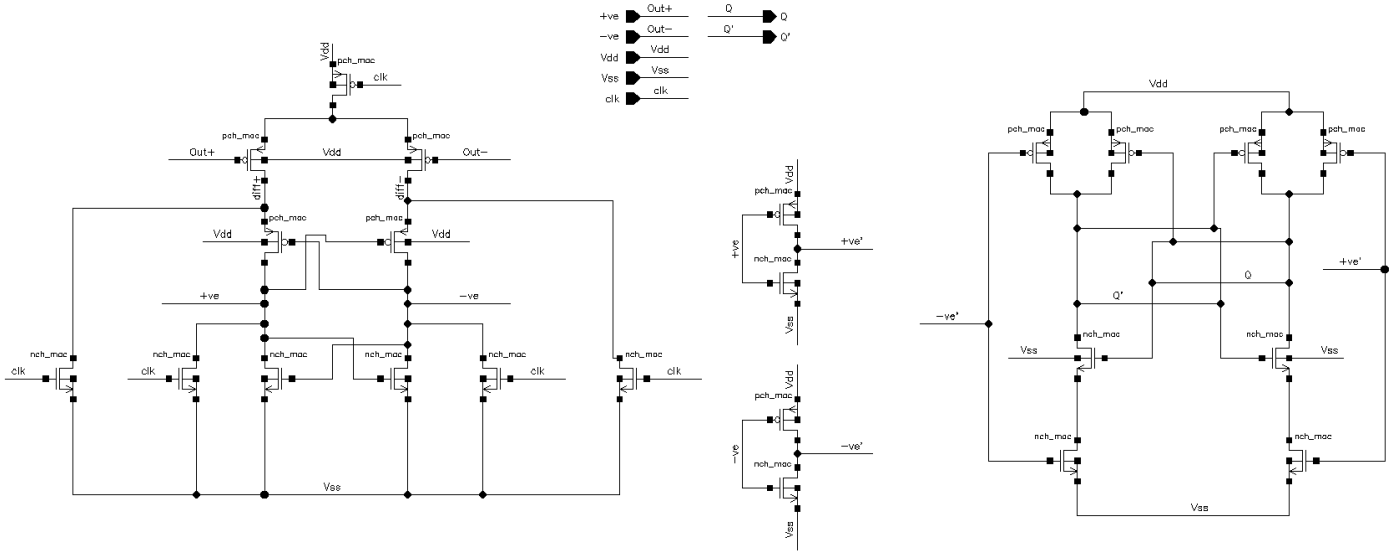

Figure 7–64: Latch with SR latch schematics

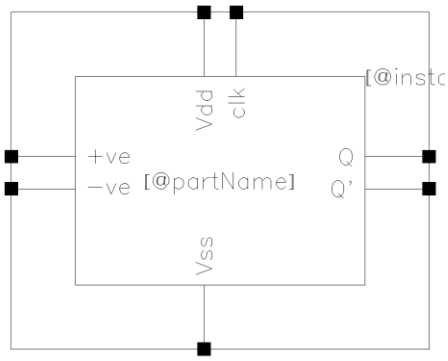

Figure 7–65: Latch Symbol

Transistor	L	W	Fingers
PMOS Enable	120n	930n	1
Diff Pair	120n	930n	1
PMOS Latch	120n	930n	1
NMOS Latch	120n	400n	1
Reset NMOS	120n	400n	1
Inverter NMOS	60n	200n	1
Inverter PMOS	60n	465n	1
SR PMOS	60n	465n	1
SR NMOS	60n	200n	1

Table 7–9: Latch & SR latch sizing

Figure 7-66 shows the transient analysis that shows how nodes behave concerning that the comparator works at the negative edge of clock. Also stating that the transient current consumption of the comparator = 179µA.

Figure 7–66: Transient analysis of comparator nodes

Concerning Mismatch, to evaluate the offset error mismatch using Monte Carlo, an input of a very slow ramp is put (starts at 400mv till 450 mv in 10µsec). At first here's the mismatch of the comparator without the preamplifier in Figure 7-67.

Offset error expression:

```
(value(v("/Vi+" ?result "tran") cross(clip(v("/Q" ?result "tran") 2e-06 8e-06) 0.5 1 "rising" nil nil)) - 0.425)
```

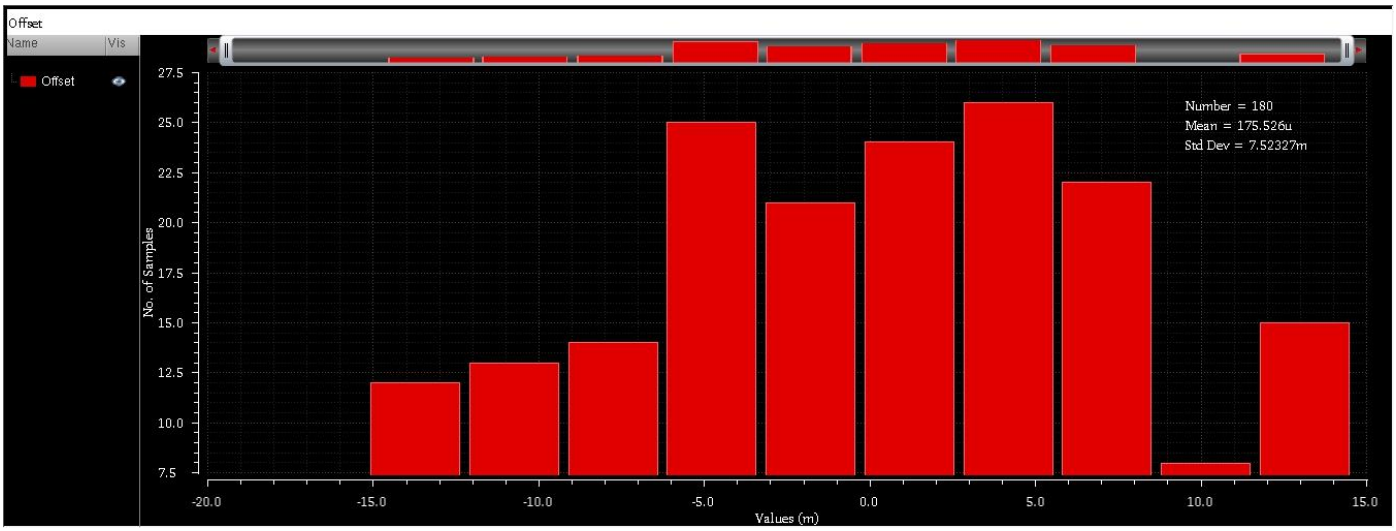

Figure 7–67: Offset error histogram (Mismatch) Without preamplifier

The condition for offset error is:

$$Offset\ error < 5\ LSB$$

$$3\sigma < 5\ \times 2.1486\ mv$$

$$3\sigma < 10.743\ mv$$

The simulated gives:

$$3\sigma < 22.56\ mv$$

Which obviously fails the condition and shows the need of the pre-amplifier to solve the offset error problem.

And the mismatch with the preamplifier gives the following

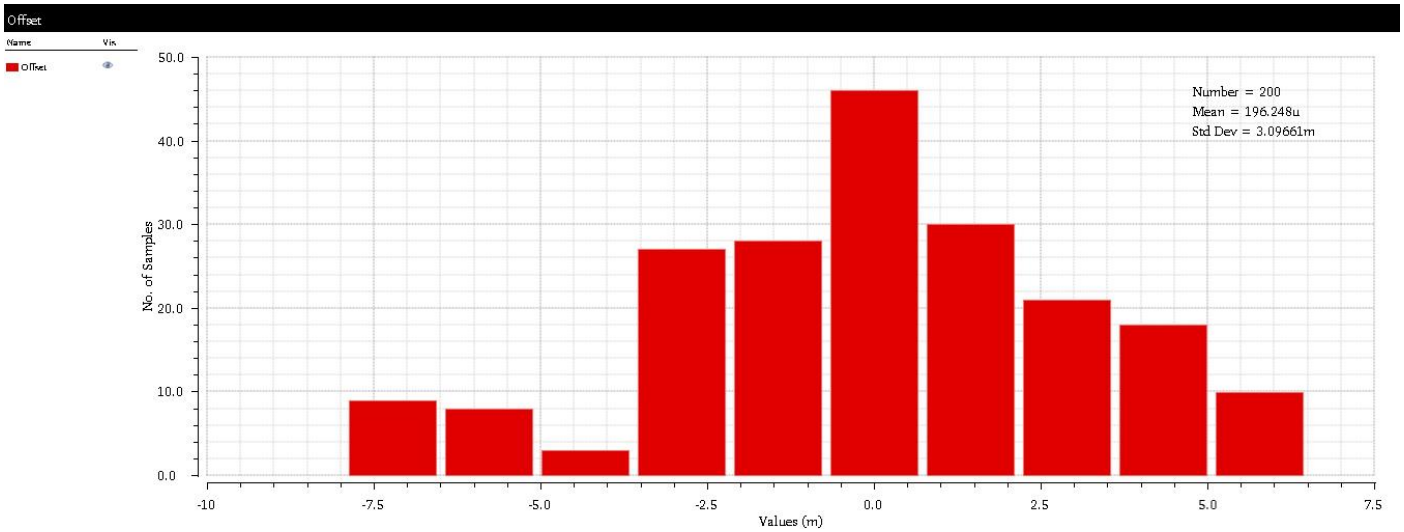

Figure 7–68: Offset error histogram (Mismatch) With preamplifier

The simulated gives:

$$3\sigma < 9.29001\, mv$$

Regarding the delay, the condition of delay is to be less than 0.25 cycle. To calculate it, we calculate the recovery time which is the delay when the comparator has the maximum input (700mv) and then suddenly the minimum difference in the opposite direction (424.75mv) as Figure 7-69 shows, which gave 196.8 psec.

<u>Recovery time delay:</u>

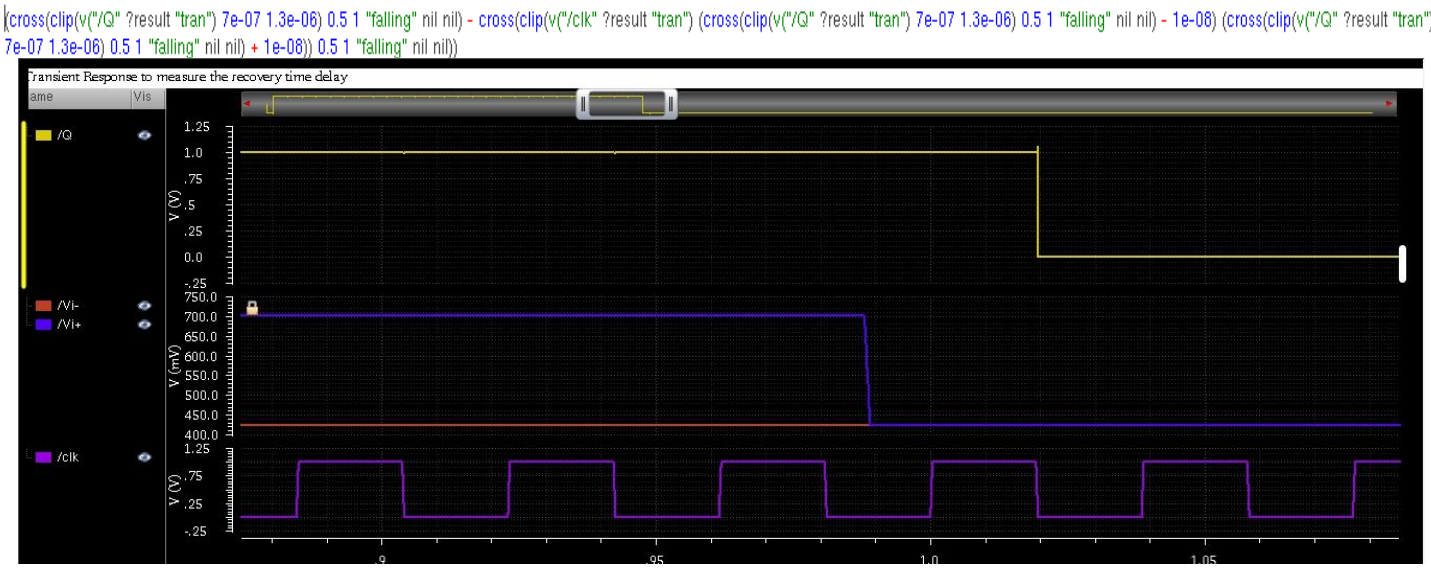

Figure 7–69: Transient Response to measure the recovery time delay

Regarding both of the previous parameters (Offset and Recovery Time Delay) but from the transient noise aspect gives the following in figure 7-70 and figure 7-71.

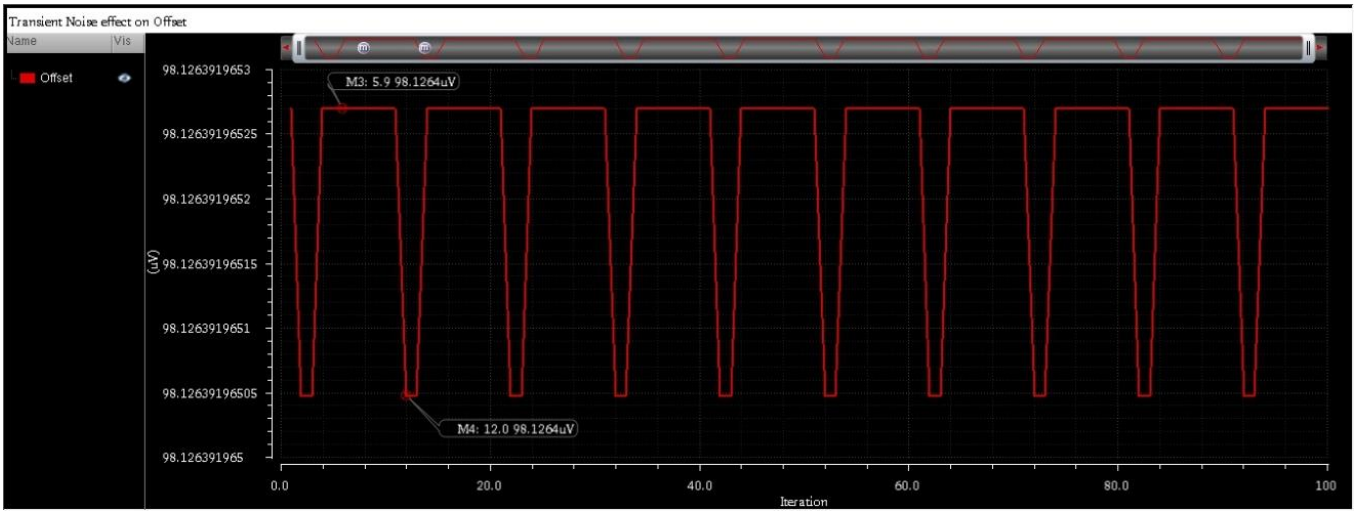

Figure 7–70: Transient Noise effect on offset

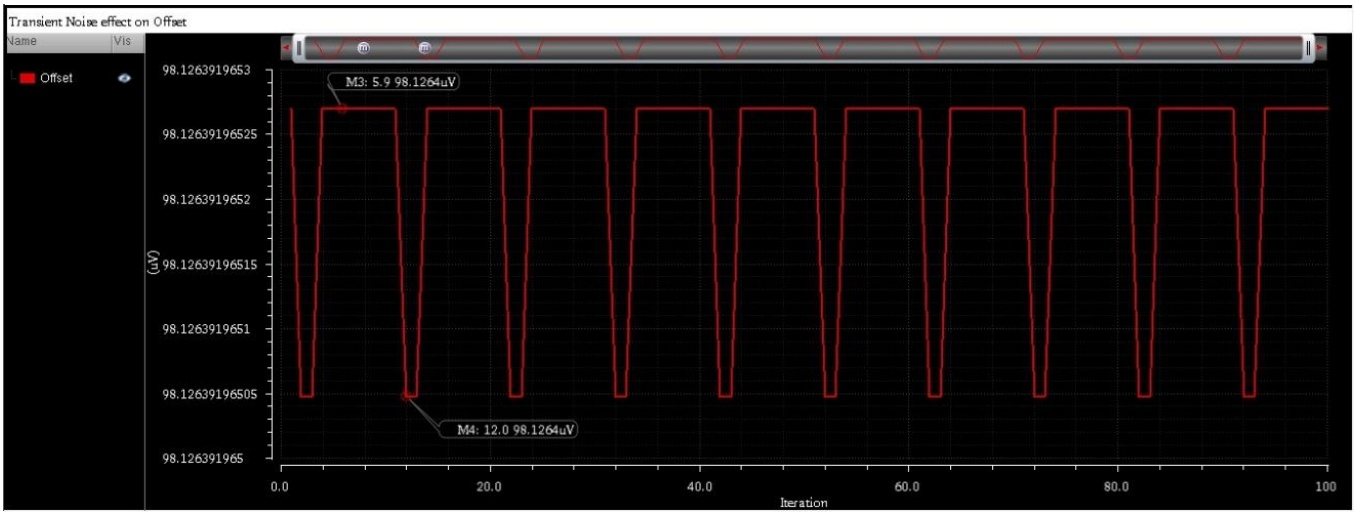

Figure 7–71: Transient Noise effect on Recovery Time delay

It's obvious from the above figures that the variations due to noise are not that effective and the maximum values are far from the condition.

Recovery time delay always faults in corner simulations, so the following are simulations of corners concerning recovery time delay as shown in Figure 7-72. We ran TT, FF, SS, FS and SF for hot and cold for low supply and high supply.

cor_std_mos.scs	temperature	Delay 2
ff	-40	236.9p
ff	125	247.8p
ff	-40	168.2p
ff	125	299.8p
ff	-40	127.5p
ff	125	305.1p
ss	-40	558p
ss	125	337p
ss	-40	335.8p
ss	125	287.6p
ss	-40	228.5p
ss	125	368.3p
tt	-40	230.3p
tt	125	326.9p

Output	Min	Max	Mean	Median	Stddev
Delay 2	127.5p	558p	289.5p	293.7p	90.25p

Figure 7–72: Recovery Time Delay Corners and its summary

Obviously, it passes the condition as 0.25 cycle = 9.61nsec.

Simulating with comparator only give ENOB = 7.807, SNDR = 48.76 dB, SFDR = 66.97 dB.

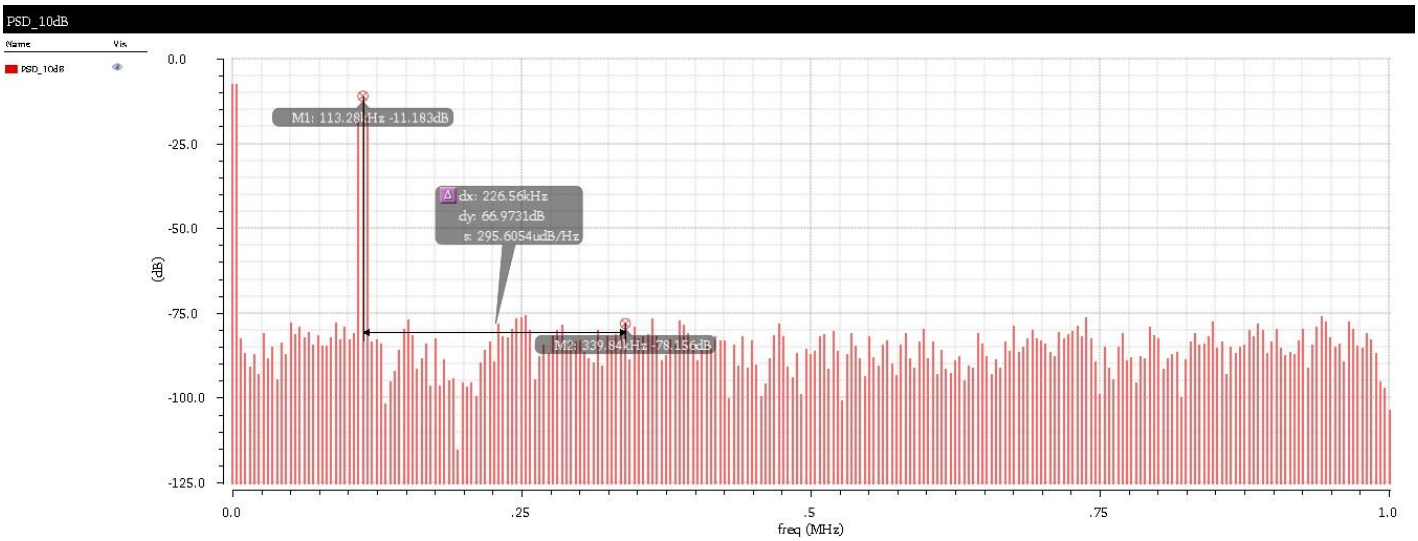

Figure 7–73: PSD of the output using comparator only

7.11.5 Final Output

Using all the previous schematics in the test bench illustrated in Figure 7-74 to calculate the final ENOB.

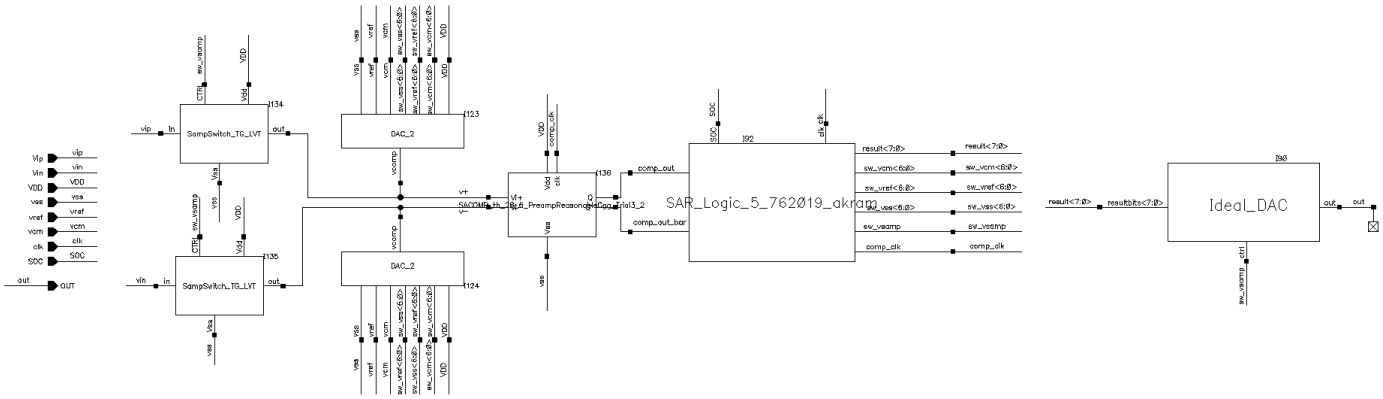

Figure 7–74:Full ADC schematic

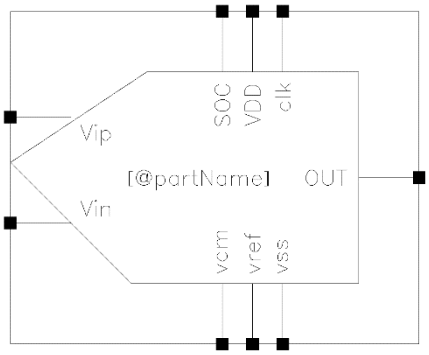

Figure 7–75: Full ADC Symbol

The previous test bench gives final values of ENOB = 7.761, SNDR = 48.48 dB, SFDR= 61.1 dB as illustrated in figure 7-76.

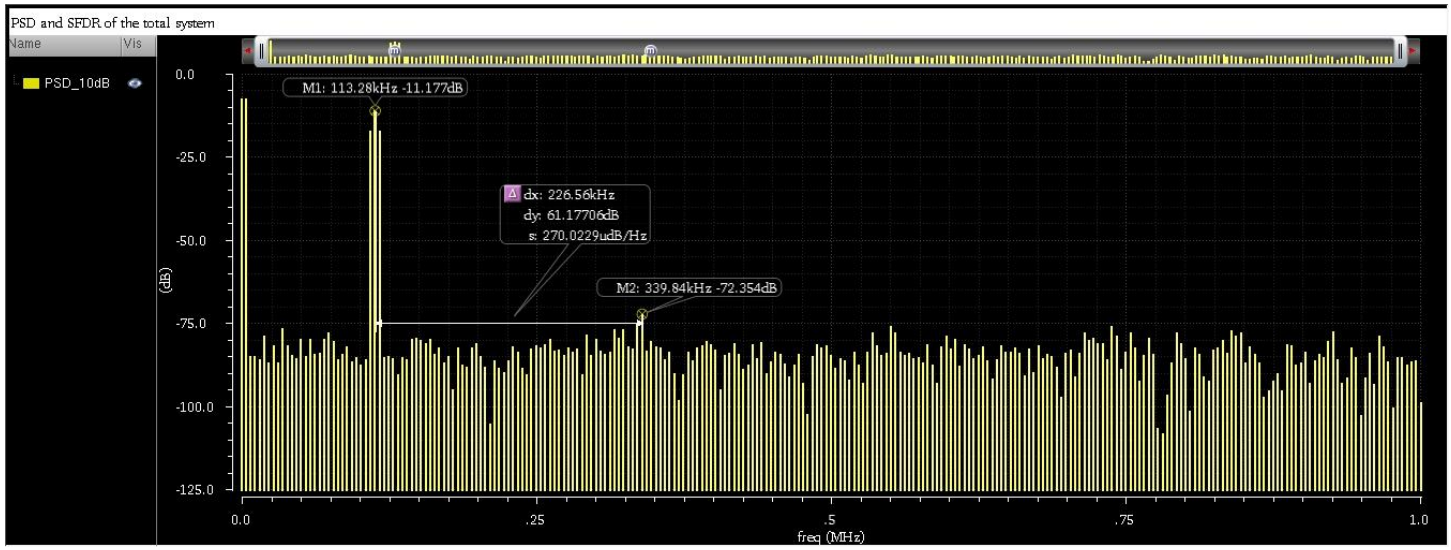

Figure 7–76: PSD & SFDR of all system

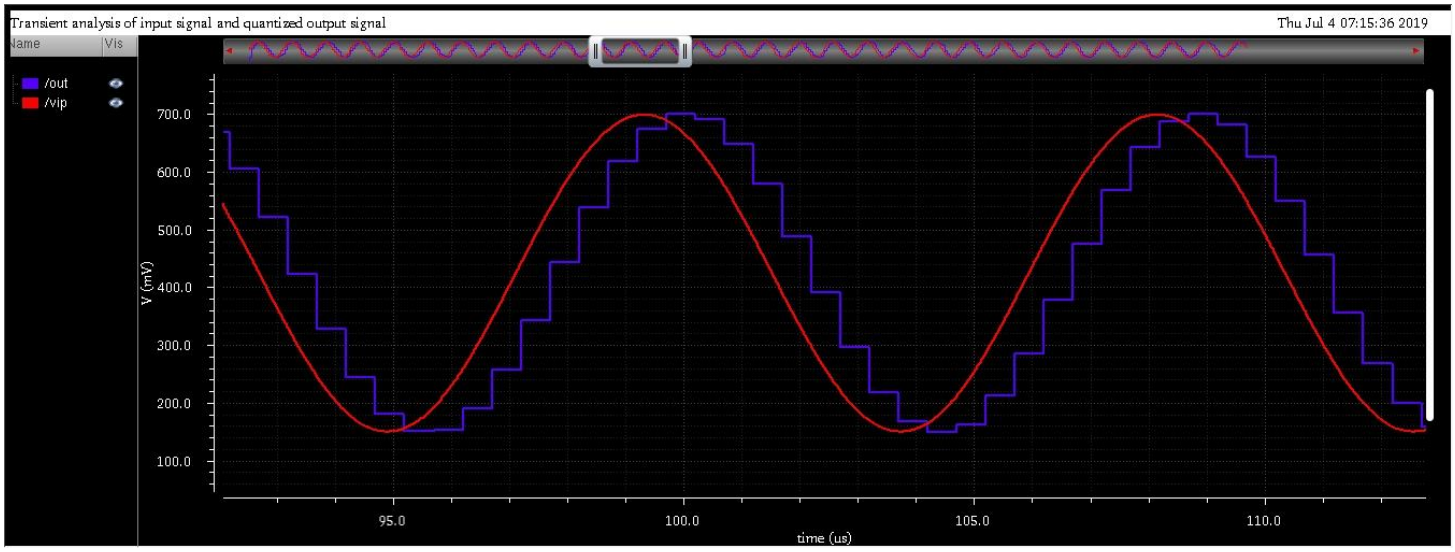

Figure 7–77: Input signal and quantized output signal of all system

7.12 Conclusion

As mentioned before, this chapter includes the ADC design which was designed using SAR topology with capacitive binary weighted DAC that operates with monotonic switching with constant common mode scheme and a StrongArm latch comparator with a differential preamplifier. The following table concludes the achieved requirements.

Quantity	Achieved
Effective Number of Bits	7.761
Current Consumption	179 µA
Offset error	4.324 LSB
Delay	196.8 psec
SNDR	48.48 dB
SFDR	61.1 dB

Table 7–10: Conclusion Table

7.13 Future work

The next steps should be designing the Reference buffer, and there is going to be some challenges regarding the amount of current consumption and the capacitive load on the reference buffer due to of the value of the unit capacitor used.

7.14 References

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