DESIGN OF AN RF ENERGY HARVESTING PMIC

A Dissertation
Presented to
The Academic Faculty

by

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PFM	Pulse Frequency modulation
PWM	Pulse width modulation
PDM	Pulse density modulation
MPPT	Maximum power point tracking
DCM	Discontinuous conduction mode
CCM	Continuous conduction mode
BG	Bandgap
DCO	Digital controlled oscillator
PMIC	Power management Integrated circuit
RF	Radio frequencies
WSN	Wireless sensor network
SOC	System on chip
PV	Photovoltaic
TRX	Transceiver
IOT	Internet of thing
LDO	Low drop-out regulator
FOCV	Fractional Open circuit voltage
PVT	Process voltage temperature
FF	Fast Fast
SS	Slow Slow
CP	Charge Pump

ABSTRACT

This Work presents an Ultra-low-power PMIC design for RF energy harvesting applications. The PMIC works with a two loops regulation for input and output regulations, and utilizes an MPPT using a hill climbing approach, operating with a PFM mode of operation and maximizing for rectifiers operating for output in range of 100 Ω-500Ω, with input power in range of -18dBm to 0 dBm, the output regulation loop act with a mixed operation between PWM and PDM modes, and regulate the output at 1.2 V DC support, the design reach a quiescent power below 1µW, the system has a self-start up unit operating from 200 mV and boosting to 1.2V forming the VDD, the PMIC interfaces with a digital controller for the operation of MPPT and other digital signals within the IC, the peak efficiency of the MPPT reaches up to 64% and the tracking efficiency reach up to 97% while the output regulation loop operate reaching efficiency > 65% for different Vin at $6K\Omega$ load with max efficiency 72% at $Vin = 200mV$, the IC is built using TSMC 130nm CMOS technology , the PMIC is simulated typically and with corners for pre-layout simulations, and post-layout simulations are performed for the layout design.

Index Terms ___ Energy harvesting, Hysteresis comparator, DCO, Cold-Start, Output regulations, RF rectifiers, low power applications, IOT applications.

CHAPTER 1. INTRODUCTION

In This chapter, an overview on the system used and the motivation behind choices of specifications is presented, by the end of this chapter, the reader should understand the overall idea of the PMIC design and its purpose of operations.

1.1 Motivation

Energy harvesting is a fast-growing technological advances that has manifested itself in many of our applications, this growing demand is invested in the IOT, those applications include biomedical applications, communication systems as WSN, military applications and other applications, those applications require to be self-sustainable, reliable and cheap, one way of reaching those goals is to use the power carefully, or by other means get free energy, so this would require to integrate both energy harvesting and power management units, PMU is able to regulate the output of the energy harvesting units which allow more clean and efficient DC support to SOC circuitry, in return allowing those components to reach higher efficiencies and higher specifications, for such regulation to exist, PMU lineup and system design is critical to define the levels required in regulation, several industrial PMIC designs for energy harvesting from different sources as PV, Piezo or thermal harvesters, can support efficiencies higher than 90% and can operate with very low quiescent power, supporting higher power capability and support for preceding circuitry, for such design to exist, designer should define the levels of leakage, the loss paths and many other aspects within the system design, and hence, define a suitable system block diagram to achieve his specifications.

RF energy harvesting is one of the energy harvesting types, that operate on signals within air supported by different frequencies using different rectification models, those models prove their efficiency, but they may lead to large ripples and changing levels of DC output relative to the power input to their system, this would require relative to any other harvester a certain PMIC to regulate such point and allow it's operation within the requirements of the final product, the degrees of regulation may differ relative to the needs of the product, so different lineups can be define, in certain systems[1], RF energy harvesting is used as a start-kick and then operation of PMIC support another stronger harvester, other systems are built as an SOC to fully support a TRX system[2].

each PMIC design is built for a certain requirements and hence it's applications and design specifications are defined, our system is required to operate at low power levels of -18dBm to 10 dBm for the support of different IOT applications, the system is built with an MPPT for input regulations to allow the maximization of input power, and then another loop is defined for the output to perform output regulations, and a start-up unit is defined to allow the formation of the VDD of operation, as the speed of the system is low, technology is relaxed to 130 nm to avoid proximity effects and layout problems, and system lineup is defined for such points.

1.2 Problem statement:

RF Energy harvesters and rectifiers an converter from an AC signal to DC signal, but the output signal is not regulated, which means that it is not sustainable and can't be used to provide any support as a DC source or biasing source, adding on that, the problems of ripples would be critical for blocks of low PSRR, this would require a PMIC to be used to regulated such output from rectifiers and support the required blocks with a good DC source and biasing source, but to achieve this requirements, certain considerations are defined within the PMIC as the type of regulation loop, the stability of the loop, the start-up capability, self-operation, and most importantly the power consumption within such system.

The PMIC design take many forms as system level design which is essential to define the requirements vs the topologies, PMIC can operate with different modes as PFM, PWM, and PDM, each mode of operation is define relative to the operation of the loop and the requirements, and dropped if a violation to specs took place, also the type of regulators as boost, buck, buck boost, CUK and LDO, all those are defined relative to the requirements and needs of loops or overall loop.

1.3 ***Solution***

1.3.1 RF Energy harvesters and rectifiers

To define the PMIC operation, we define the harvester, the harvester level of ripples, performance with a certain output load and levels of power at which good efficiency is achieved, all those concerns are important to define the specs of a PMIC, this required a certain Survey to allow us to define those specs.

Table 1.3-1 Surveying different rectifiers

Points of Comparison	[2]	[13]	[14]
Device type	GaAs HEMT	CMOS 130 nm	E- PHEMT
Input Power	16 dBm (39.8107 mW)	10 dBm (10 mW)	17 dBm (50.1187 mW)
Load Resistance	1 to 10kΩ	N/A	10 to 500Ω
Peak Efficiency	51 %	30%	83% (Eff. From 10% to 83%)
Output Power (input power to our system)	20.303 mW at max efficiency	3 mW at max eff.	41.598 mW @ max eff.
Frequency	985 MHz	2.4 GHz	900 MHz and 2.45 GHz

For the levels desired, the survey included different Energy harvesting designs, each design operates with different technology and certain frequency as shown in table 1.1-1.

The results shown in the table describe different categories of rectifiers, for an adaptive IC, considerations are made for both on-chip and off-chip models, also by comparing the specs and definitions within the next sections, the optimum model chosen was the CMOS model, and hence a certain input specs are defined accordingly.

1.3.2 Industrial ICs

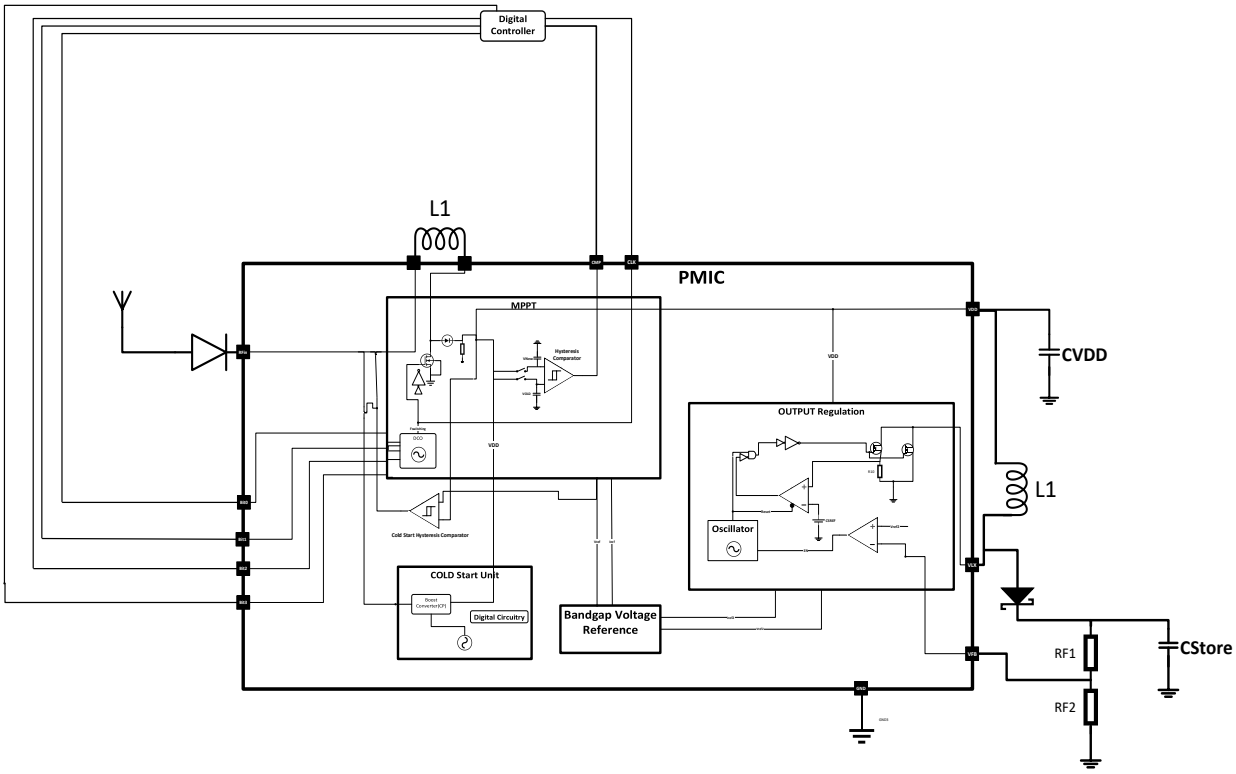
For more generalized and precise definition of specifications, another survey is made on different systems in the industry, as we have defined the rectifier model, so a certain starting point specs are set, to define an optimum system to match those specs with respect to the blocks capabilities and the system design, certain industrial PMIC for energy harvesting were surveyed, those ICs are a generalized input sources IC, which configure on different sources, and from those sources is RF energy harvesting, only one industrial IC that may consider using only RF energy harvesting which is AEM 30940, the survey is presented in table 1.2-1.

Table 1.3-2 Industrial ICs Survey

	ADP 5091-5092	**BQ25570**	**Max17710**	**AEM30940**
Input voltage	0.08 V to 3.3 V	0.1 V to 5.1 V	75 mV to 5.7 V	50 mV to 5 V
Input Source	PV-PZT-TEG-AC(RF)	PV-PZT-TEG-RF	PV-PZT-TEG-RF	PV-PZT-TEG-RF
Input Power	6 μW to 600 mW	5 μW to 510 mW	1 μW to 100 mW	-18.5dBm to 10dBm
Output voltage	1.5 to 3.3V	2 to 5.5 V	1.8, 2.3 or 3.3V	1.2, 1.8 or 4.1V
Rating Current	150 mA @1.5-3.6V	110 mA		20mA@1.8V 80mA@1.8-4.1V
Cold Start	380 mV - 6 μW	330 mV - 15 μW		380 mV - 3 μW
Operating Temp	−40°C to +125°C	−40°C to +125°C	−40°C to +125°C	-40 ◦C to +125 ◦C
Primary BATT	Yes	Yes	Yes	Yes
MPPT	Yes	Yes	NO	Yes
Regulators moods	PFM Hysteresis (LDO)	PFM Hysteresis (general)	PFM	PFM
MPPT sensing time	16 Sec.	16 Sec.		0.33 sec
Battery Types	LI-ION, Thin-film, Super-capacitor, or a conventional capacitor	LI-ION, Thin-film, Super-capacitor, or a conventional capacitor	LI-ION, Thin-film, Super-capacitor, or a conventional capacitor	LI-ION, Thin-film, Super capacitor, or a conventional capacitor

From our point of view and the requirements, we defined the BQ22570, from the data sheet we defined a system that is comparable to the BQ22570 system and defining our specs.

1.3.3 System Block Diagram



To define the PMIC, we define a set of specifications and requirements as illustrated above, the specs hence define the modes of operation of the loop and its ability to maintain the required output and operation to achieve the required level of DC, and relative to the Industrial PMIC and literature point of view, we define the block diagram, our proposed system consists of two regulating loops, an input regulation loop presented by the MPPT operating as a boost converter with a PFM control loop for tracking the maximum power, and output regulation loop that regulate output at 1.2 V as required using PFM operation,

and within the system design a reference generator is required for the generation of reference voltage and biasing current for different blocks, a start-up unit is considered to allow the system to operate with the required VDD, so it start to charge the VDD capacitor at the initial operation then the MPPT continues, to allow the differentiating between the MPPT and the Start-up circuit, a hysteresis comparator is set to define two different points of operation, one is defined for the MPPT and other for the Start-up unit.

Specs of each block is defined relative to the specs of the overall system, and the ability of each loop to achieve certain points of functionality, in table 1.3-1 general specs of such system is defined and in the next chapters, each block would be defined with respect to general considerations in system and circuit levels.

Table 1.3-3 General Specs of PMIC

Points of Specifications	Specifications
Input power to system	-18 dBm to 10 dBm (RF)
Input resistance range (Rectifier)	100Ω-1000Ω (choose 100Ω) as intermediate value
Input voltage range	100mV - 800mV
Output Voltage	1.2 V
Power consumption	500nW-1µW
Quiescent current	10 nA-100nA
MPPT Required	Yes
Regulatory Mood	PFM/PWM/PDM
Battery Type	Super Capacitor(2µF-4µF)

1.4 Organization

The thesis is defined into chapters that define the block diagram expressed above, the system design of each block with respect to other blocks is defined within each chapter, and sections within each chapter define the circuits and integration, the design is built using a TSMC 130 nm KIT, the chapters are defined as follow:

Chapter 2, introduces the system design and circuit design of blocks within the MPPT Loop and integration of the loop, also the chapter include the corner simulations and layout simulations for certain blocks within the loop, by the end of this chapter the reader should understand the functionality of MPPT and the topology used, also the low power consumption techniques and corner and layout calibration techniques.

Chapter 3, introduces the design of the output regulation loop, this loop is analogic to that of the MPPT but targeting to keep the output on a certain desired level of 1.2 V, the loop operates with a PFM opertation, and use a DCM and simulation for the loop are included within this chapter.

Chapter 4, introduces the BG circuit design and specification of its circuits, simulations for the loop for corners and typical cases are included, layout simulations and techniques are presented as well.

Chapter 5, introduces the start-up circuit design and definition, the circuit design of such unit is a boost-based design similar to that presented in chapter 3 and 4 but replacing the inductor topology by a CP topology.

Finally, Chapter 6 and it introduces a conclusion for the full PMIC design.

CHAPTER 2. MPPT

Background and related work

As we operate with a low Power RF signals in the range of -18 dBm to 0 dBm, we require to operate on maximum power point to allow an efficient harvesting profile and also high overall system efficiency, maximum power point can be achieved by different approaches such as perturb and observe, Hill climbing and fractional open circuit voltage, each method requires a certain flow of tracking to the MPP (Maximum Power Point), this is done by a flow chart and such flow chart defines the design flow of the MPPT such as Selection of Blocks such as oscillators, comparators, Digital controllers and logic, type of DC-DC converters as boost, buck or buck-boost, a good flow chart would allow the designer to have a good MPPT and hence an efficient PMIC, a bad flow chart would lead to a high complexity in design and high quiescent power within the blocks of choice, in this chapter we would discuss the design of the MPPT and the novelty in its flow chart and system design, hence, the design of each block and results and simulations for such blocks with respect to typical conditions, corner conditions and layout considerations.

2.1 Design of MPPT (Concepts point of view):

2.1.1 Approach Definition and novelty:

The MPPT used is defined for a Hill Climbing approach which depends on climbing the curve of power vs voltage till reaching the MPP and then going back and forth around such point to allow the tracking of the MPP, in Fig. 2, the Hill Climbing approach is illustrated in further sections.

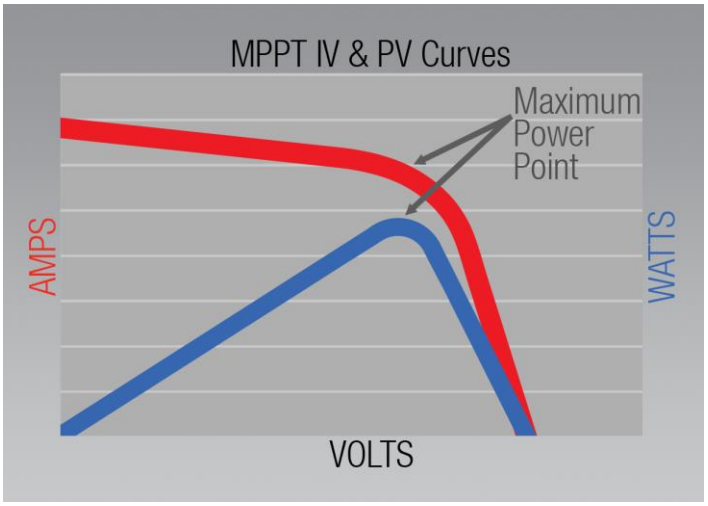


Figure 2-1 MPPT IV and PV Curves

To illustrate the different approaches of MPP Tracking, in Fig.2 there exist two curves, a curve defines I vs V and other is P vs V, the I vs V curve introduce P where P=IV, as V increase, I flow such increase till reaching the MPP where I*V reaches its maximum value, such a point is required to be tracked and it is translated also in power as shown in the PV of blue, the style of motion on the curve to detect the MPP is what is so called an MPPT Methodology, the MPPT methodologies are defined as Follow:

1. **Indirect:**

1.1**. Fixed voltage method:** with implies that a certain calculation is done to find MPP and then a voltage is applied to get such MPP, this method is very static and it is not used widely as it has proved is inefficient action with respect to many occasions.

1.2. **Fractional Open Circuit Voltage Method:** it is defined that VMPP is related the open circuit voltage calculated at the input of the MPPT Block, for each Harvesting method a certain K factor is defined, as 0.6-0.8 for PV and 0.5 for RF, piezo and TEG, so such method calculate the OCV and then relate it to such K factor and hence is calculate the VMPP required for MPP tracking, such method is widely used and it proved its

efficiency in many Papers in literature as [3]-[6] and products in industry as the algorithms used in BQ25570 and AEM30940 (check Appendix), the FOCV assume that the power source is linear so in case of **RF Energy harvesting** such method can't be used as the Harvesting include a rectification using a nonlinear device (i.e. diode).

2. **Direct:**

2.1. **Hill Climbing:** it is a method that increment steps of voltage relative to the measured power till reaching the MPP and then is oscillates around the point till other perturbation case.

2.2. **Perturb and Observe:** it is a method that depend on perturbing the level of voltage and observing the power, if the power of the new perturbation is lower than that of the old, another perturbation level is taken into account to reach the MPP.

Hill Climbing Approach Explanation [7]:

The method used within this design of MPPT is the Hill climbing, for the illustration of the Hill climbing approach the following flow chart is presented for the general approaches of Hill climbing, this flow chart illustrates the hill climbing approach steps to achieve an MPP, first we start the sensing cycle, so we measure input voltage and current, then we measure the power, and from the power we set certain step of decision making, the first ask a question, is the old power and the new power are equal, if this is true then the algorithm is fixed on the MPP or a dummy point so we need to check again for the value of the power till a change occur and no action is taken, if a change took place in the power, as example the power is increased or decreased a decision is required in such occasion, this is translated into two other question to make a wise decision, so we ask for the new power and old power, is the new power larger than old power or it might be smaller, so depending on the answer of the question, if the answer is yes to we ask for the level of voltage in such case

and if no we ask also for the level of voltage, in case the answer is yes, we would introduce a certain step controller step M (i.e. frequency step as introduced in the next sections), and a ΔM as a certain change in such step, if the recent voltage is higher than the previous voltage then the perturbation direction is in the direction of increase so require to receive such direction, so an order of M-ΔM is defined, and vice versa with M+ΔM, same is for the case of No, this can be explained by referring to equation (2.1), (2.2) and (2.3).

$$if\ \frac{dP}{dV} < 0 \quad \rightarrow \quad (2.1)$$

The direction of perturbation of voltage vs the change in power is opposing so the voltage is required to be opposed, so M=M-ΔM.

$$if\ \frac{dP}{dV} > 0 \quad \rightarrow \quad (2.2)$$

The direction of perturbation of voltage is with the direction of the change in power so the change in voltage is encouraged, so M=M+ΔM.

$$if\ \frac{dP}{dV} = 0 \quad \rightarrow \quad (2.3)$$

At case of MPP no change is defined either for the voltage or for the power.

Relatively the flow chart of the Hill climbing is defined.

2.1.2 System Design, Definition and Specifications of MPPT [8],[9]:

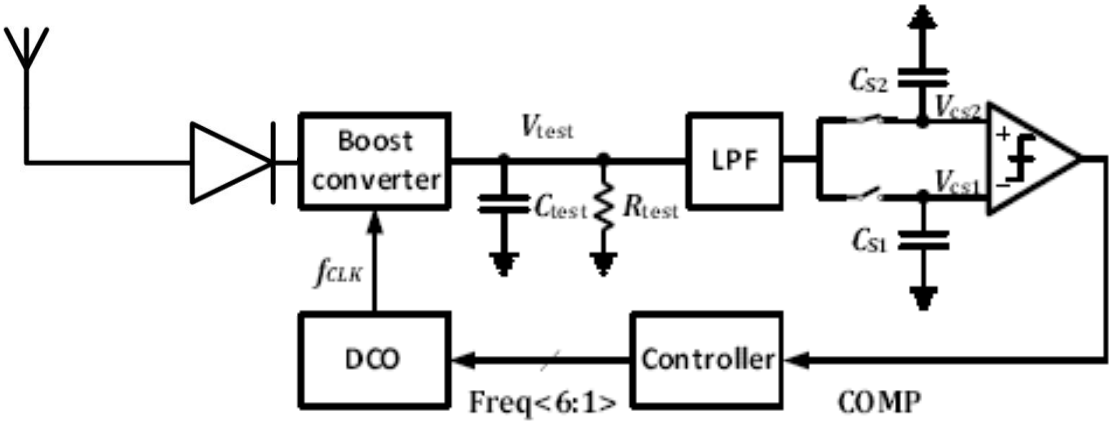


Figure 2-2 Block Diagram of MPPT

Fig.3 Shows the block diagram of MPPT design, as explained in chapter 1, the system design of the full RF energy harvesting PMIC is dependable on the choice of the RF rectifier and the level is supports and same is for the MPPT, the MPPT is the first block to interface with the RF rectifier, and relating to the theory of maximum power, to achieve the maximum power transfer between any two points, matching is required, for RFIC matching is defined for a signal, in the PMIC matching is defined for DC level harvested power, So the matching is achieved by which $Z_{out}=Z_{in}$ with respect to rectifier and boost converter, respectively, the output impedance of the rectifier is of which the maximum power is achieved, in this Design we defined certain impedance values as Thevenin models of rectifiers assuming the maximization of power at such points, each test case for each point targets the matching with that impedance for maximization of power as explained in the next sections.

To illustrate the functionality of loop and the functionality of each block, we start first with the explanation of how the loop works:

1. The loop tries to match the input impedance of boost converter that allow the output load seen by rectifier to go into the curve at maximum power.

2. This is done by perturb and observe using a PFM loop.

3. The loop changes the frequency of switching each major cycle and hence change the output voltage of the boost

4. Using the loop matching is achieved

5. A major cycle for MPPT operation is defined to include certain integer multiples of minor cycle.

So relative to such steps of operation the blocks are defined to allow those steps to be in action, the blocks are defined as follow:

1. Boost Converter: it is a DCM Boost Converter, DCM mode is used for the low power levels of the input, the Boost converter is used to be the perturbation unit of voltage as illustrated, in the section of the DCM Boost Converter, the perturbation in the boost is dependable on the frequency, so that the loop is called a PFM loop, the art of operation would be defined.

2. DCO: an oscillator is required for any boost converter to operate, a VCO is needed in this loop to define the perturbation relative to the decision made by the used controller, as the controller used is a digital controller so it is required for the system to have a DCO instead of VCO, to operate on the output bits used.

3. Digital Controller: the controller is a digital controller, but on a certain logic flow, to allow the fulfillment of the flow chart used, the digital controller is built using a Verilog-A code, and it would be defined by certain Verilog code using an external IC as illustrated in the first chapter.

4. Hysteresis Comparator: to make a decision using digital controller, we require to know the voltage level between new and old case, this block is used as to approach matching, ideally if input and rectifier are matched, this is relative to the conventional flow chart defined for Hill Climbing approach, as to check on the most recent voltage and the previous voltage, as the boost converter introduce a rippling output so in result to avoid any problems in defining the change in voltage a hysteresis window is introduced to avoid racing in the output of comparator, the width of hysteresis window is defined relative to the ripples level of the boost converter, and as the boost converter is connected to a DCO of different frequencies, as the maximum ripples occur at maximum frequency, the ripples in voltage level is defined for the maximum frequency.

5. LPF and Storage units: Cs1 and Cs2 are two storage caps to store values of the old and new and the signal overlaps on them relative to the major cycle, the LPF is used to decrease the ripple and so make the specifications on the hysteresis window more relaxed, the order of the filter is dependable on the level of voltage ripples.

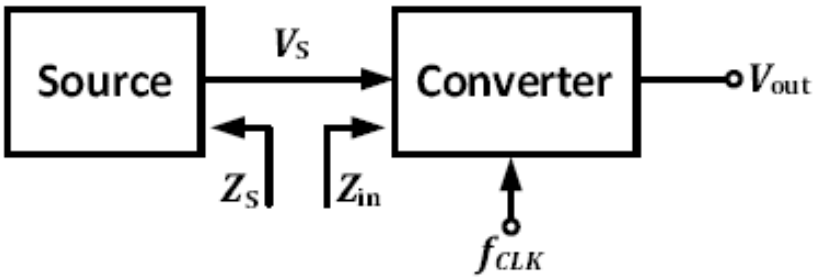


Figure 2-3 Matching the source and load impedance

To match the source and load we must define the value of the impedance in the converter and from the analysis of the converter the following equation (2.4) is defined:

Input impedance for DCM boost:

$$Z_{in} = \frac{2L}{D^2} * f_{clk} \rightarrow \quad (2.4)$$

L: value of inductor used in the boost converter.

D: value of the duty cycle of the output clock signal of the DCO.

For a fixed L and D, to change the input impedance the value of clock frequency is changed and so this loop is called a **PFM controlled loop**.

2.1.3 DCM Boost Converter [10]:

2.1.3.1 Art of work and Design concepts:

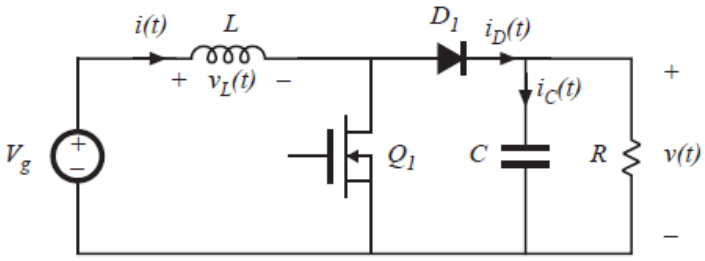


Figure 2-4 DCM Boost Converter

For a DCM Boost converter, as the level of voltage is very low, the level of current charging the L and then passing to charge C is very low, as the level of the DC is low, the ripples may go into negative values, this lead to an opposing direction of flow of charges from the capacitor into the circuitry leading to increase in losses, which is very critical in our case, so it is required to cut the negative levels as shown in Fig.7, this is done by using **D_1.**

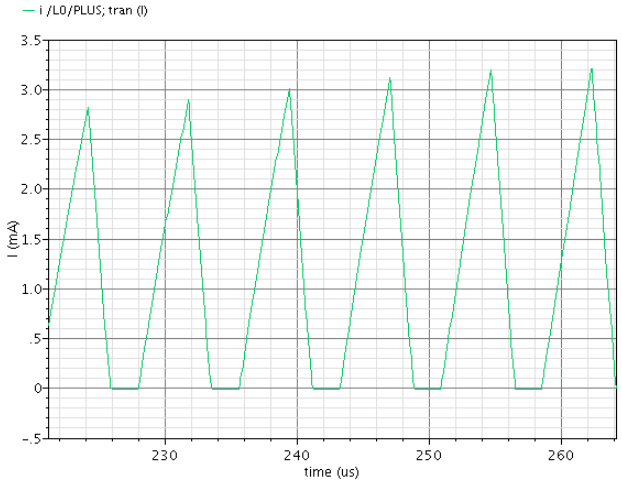


Figure 2-5 DCM Boost action on current ripples

To analyze such structure we define two modes, a charge and discharge modes, also we should define the CCM (continuous charging mode), referring to [10] for the analysis of the CCM, we define the CCM and DCM as follow:

CCM:

$$\because V_L = \frac{Ldi}{dt} \rightarrow i = \int \frac{V_L}{L} dt \rightarrow \quad (2.5)$$

in CCM, we only have two modes of operation, a charge and discharge, in case of diode is off (L charge mode):

$$V_L = V_g \quad \& \quad i_c = -\frac{V}{R} \rightarrow \quad (2.6)$$

While in case of L discharging and C charging:

$$V_L = V_g - V \quad \& \quad i_c = I - \frac{V}{R} \rightarrow \quad (2.7)$$

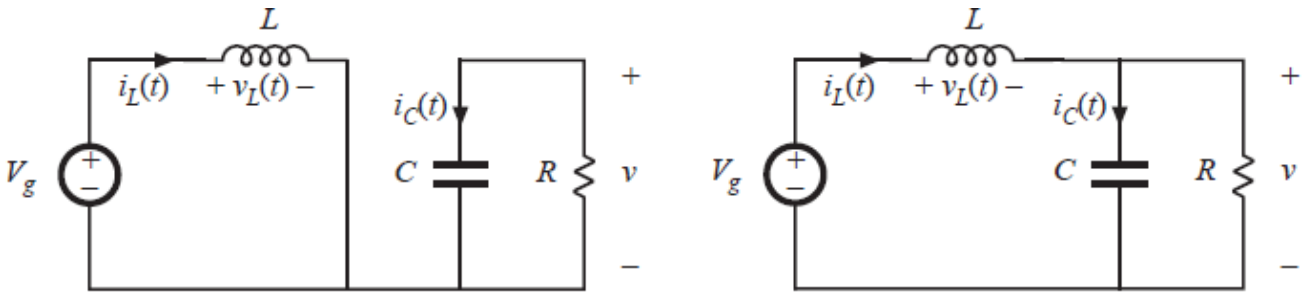


Figure 2-6 Modes of operation a CCM Boost converter

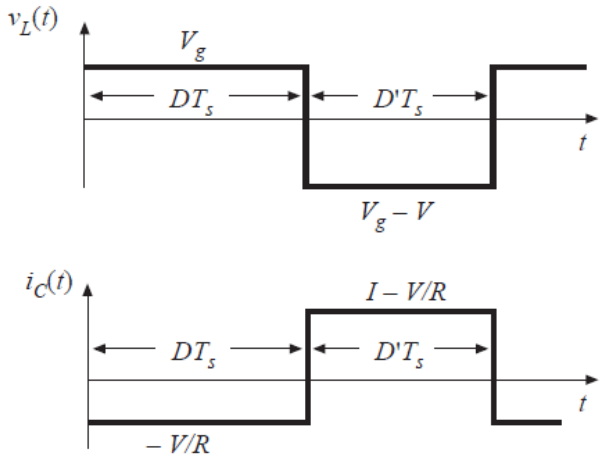


Figure 2-7 combining the two modes with the duty cycle action

In Fig.9, by combining both the voltage on inductor and current in capacitor, for full cycle of the input switching signal, two output curves are introduced as shown, consider first curve of inductor, it is desired to for the second balance of inductor voltage:

$$\int V_L(t)\,dt = V_g DT_s + \big(V_g - V\big)D'T_s \quad where \quad D' = 1 - D \quad \rightarrow (2.8)$$

For balance to take place, the output of equation 2.8 is equated to zero, and the result of the equation define the conversion ratio in case of CCM,

$$\frac{V}{V_g} = \frac{1}{1-D} \quad \rightarrow \quad (2.9)$$

Equation 2.9 highlights the effect of the duty cycle, as the duty cycle increase the conversion ration increase allowing higher boosting action **(action 1).**

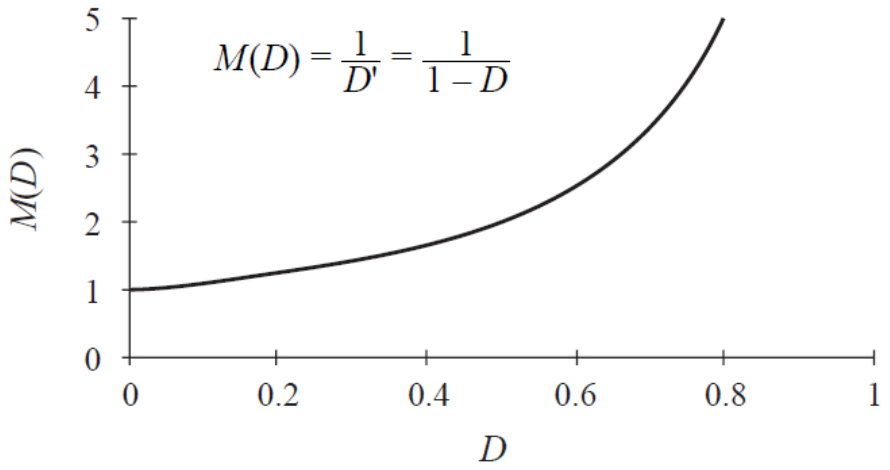


Figure 2-8 action of duty cycle vs the conversion ratio value

To determine the inductor current dc component, a capacitor charge balance is performed.

$$\int_0^{Ts} i_c(t)dt = \frac{-V}{R} DT_s + \left(I - \frac{V}{R}\right)(1-D)T_s = 0 \quad \rightarrow (2.10)$$

From equation 2.10 =, the capacitor charge balance is done to equate 2.10 to zero and hence the dc component is found,

$$I = \frac{V}{RD'} \rightarrow \ (2.11)$$

$$I = \frac{V_g}{D'^2 R} \rightarrow (2.12)$$

From the equations defined above, it is desired to find the ripples on inductor current and voltage to define, when we should define a DCM Boost converter and the levels of ripples allowed in the output and the tuning parameters in the design.

To define the ripples on the inductor current, define the equations as follow:

$$V_L(t) = L\frac{di_L}{dt} \rightarrow (2.13)$$

$$\frac{di_L}{dt} = \frac{V_L(t)}{L} = \frac{V_g - V}{L} \rightarrow (2.14)$$

$$\Delta i_L = \frac{V_g}{2L} DT_s \rightarrow \quad (2.15)$$

So, from equation 2.15, it is defined that the parameters affecting the ripples level is L, V_g, D and T_s, this would hence require to increase L to decrease the ripples, the input voltage range is a low voltage range so it doesn't support a large ripple case, as the frequency of switching is decrease to allow lower switching losses this would contribute in the ripples to increase it and the duty cycle is kept 0.5 to compromise, we compromise with value of L vs frequency, and to determine the voltage ripples, we define the ripples on capacitor, this is by checking the following:

$$\frac{dv_c(t)}{dt} = \frac{i_c(t)}{C} \rightarrow (2.16)$$

For first interval,

$$\frac{dv_c(t)}{dt} = -\frac{V}{RC} \rightarrow (2.17)$$

For second interval,

$$\frac{dv_c(t)}{dt} = \frac{i_c(t)}{c} = \frac{I}{C} - \frac{V}{RC} \rightarrow (2.18)$$

From both equations, and integrating and computing the change in the voltage, we achieve the following result:

$$\Delta V = \frac{V}{2RC} DT_s \rightarrow (2.19)$$

From equation 2.19, we set certain points and definitions, the value of ripples on the output is relative to the value of output voltage V, so as the output voltage increase, the ripples increase, the value of C and R used also decrease level, the controllable here is C as it takes the value of the super capacitor, the D and T_s are pre defined for the ripples on inductor current, so also as they increase ripples on output voltage, they increase ripples on output current.

From the previous equations we defined set of values of some parameters as defined in the table 2.1-1.

To account for the effect of the DC resistance of the boost converter another level of analysis is made, the model for this analysis is presented in fig. 2.1-10

Table 2.1-1 Values of components of the Boost converter

L	**4.7 mH, DCR=8.5Ω (coil craft)**
C	**Super capacitor (Murata) 2μH**
R	**Seen from the Next Block (~10KΩ)**

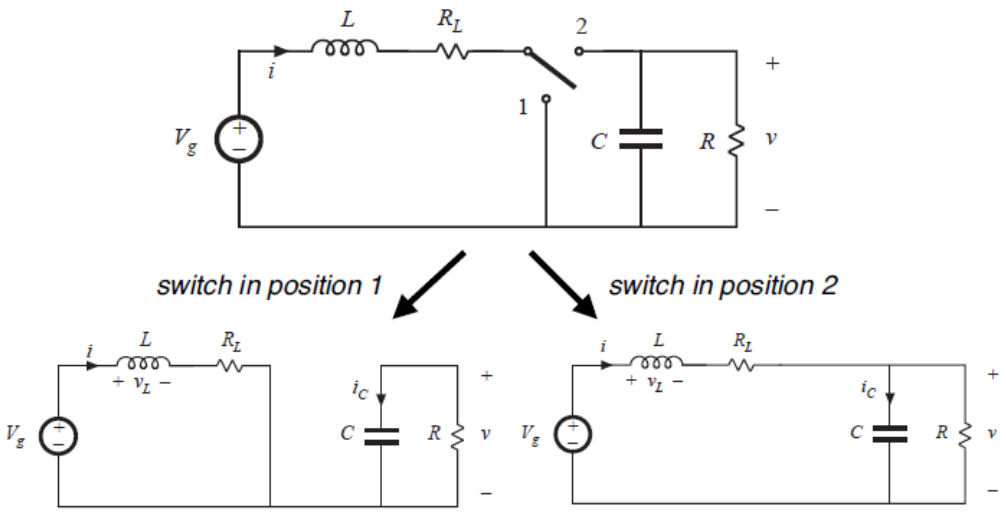


Figure 2-9 Model of the DC resistance

The DC resistance is defined with respect to certain analysis points, where its action is taken into account to allow the system to adapt to what it takes.

For the charging model of L (2.20) and discharging of L for C (2.21), we define the analysis points as follow:

$$v_L(t) = V_g - IR_l - V \rightarrow (2.20)$$

$$i_c(t) = I - \frac{V}{R} \rightarrow (2.21)$$

By calculating the charge balance on inductor and capacitor we achieve the conversion ratio as follow:

$$\frac{V}{V_g} = \frac{\frac{1}{D'}}{1 + \frac{R_L}{D'^2 R}} \rightarrow (2.22)$$

A factor is added defined by $\frac{R_L}{R}$ which introduce to change the functionality of the conversion ratio defined before, this is defined by certain curves that define the stability of any control loop, the curves are presented in following figure.

To allow the circuit to stabilize without any problems, we may go for two approaches as D at high values push to an opposite change leading to a positive feedback loop and an oscillation condition may appear so we define the D for small values and check for this in a PWM system, but for the proposed MPPT we define a PFM based loop which is stabilized by nature choosing a reasonable value.

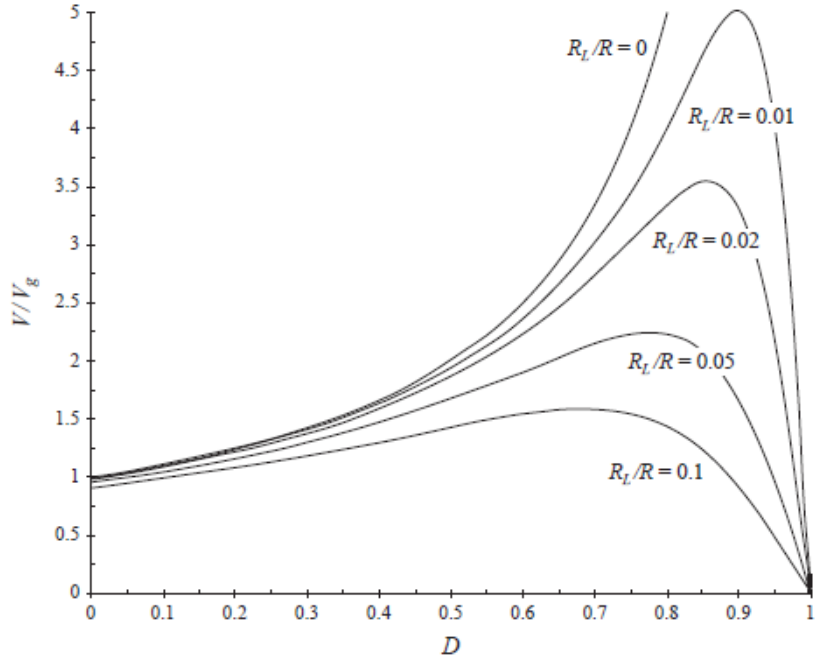


Figure 2-10 Stability curves vs the dc resistance relativity values

Using certain equivalent models, we can define the efficiency of the boost converter:

$$\eta = \frac{P_{in}}{P_{out}} = \frac{V_g I}{V D' I} = \frac{V}{V_g} D' \rightarrow (2.23)$$

As duty cycle increase, relative to the relation, the efficiency decrease, and as the output voltage increase, the efficiency increase, and if we take into account the inductor resistance, we find that efficiency achieved is expressed in equation 2.24.

$$\eta = \frac{1}{1 + \frac{R_L}{D'^2 R}} \rightarrow (2.24)$$

As expected from the simple definition of the inductor resistance, that as it increases the efficiency would decrease, so Low DCR series of coil craft is selected as explained in table 2.1.

To extend the used model to be matching a full real case of boost converter, we should consider within the efficiency the factors of the switching losses and the conduction losses, the conduction losses would be due to the non-ideal resistance of the switches(MOS or Diode), while the switching accompanies the switching done on one of the gates.

Those models would complicate the form of efficiency, so to illustrate we define the critical tuning parameters that may affect the system.

$$P_{loss_{switching}} = CVDD^2 f_{switching} \rightarrow (2.25)$$

$$P_{loss_{conduction}} = I^2 R_{on_{Mos}} \rightarrow (2.26)$$

From equation 2.25 and 2.26, as switching frequency decrease, losses decrease but the ripples would increase and so we defined a certain tradeoff to compromise, the second tradeoff is between the sizing of the MOS for low on resistance and low gate capacitance to define low losses.

$$C_{gate}\ \alpha\ WL\ , R_{on}\ \alpha\ \frac{L}{W}$$

So, for the best case, we minimize the L, and then we simulate for the optimum value of W.

For the DCM boost operation, also a certain point of analysis is required to define certain constrains to allow such mood to operate with no worries or problems, for the DCM we define 3 modes of operation in the system, and with a condition on DC current vs the ripple level for those modes to exist.

$$I > \Delta i_l \rightarrow CCM$$

$$I < \Delta i_l \rightarrow DCM$$

As we defined previously the value, for the $I < \Delta i_L$, $DD'^2 > \frac{2L}{RT_s}$, so from those equations we define two other parameters, $K\ and\ K_{crit}$, and relatively we set a condition on the R value which is the input load of the preceding block.

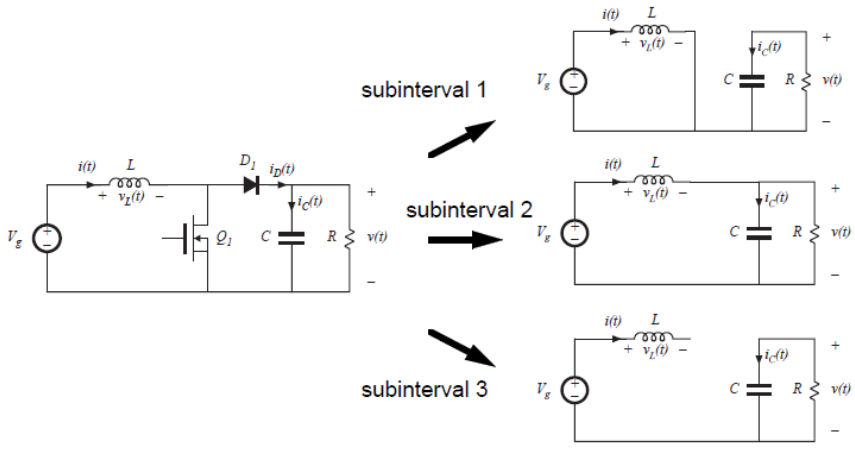


Figure 2-11 Modes of operation of DCM boost converter

the extra mode of operation is the hold mode, which means that no charging or discharging of the inductor or capacitor would occur, so we hold the charge and avoid any reverse motion leading to extra losses, by solving the voltage-second balance, a new expression is acquired, same as what was made previously, same for the capacitor charge balance, and by calculating the values of those calculations, a new conversion ratio is acquired.

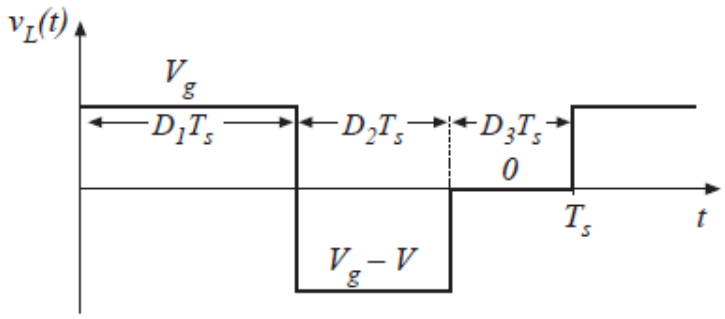


Figure 2-12 the voltage across time on the inductor

$$\frac{V}{V_g} = \frac{1 \pm \sqrt{1 + \frac{D_1^2}{K}}}{2} \; where \; K = \frac{2L}{RT_s} \rightarrow (2.27)$$

And from the conversion ratio and the current values across the load we can define the input load seen by the converter as:

$$Z_{in} = \frac{2L}{D^2} f_s \rightarrow (2.28)$$

This equation is the soul of the MPPT as what was discussed in the first section.

2.1.3.2 Diode implementation and switching MOSFET:

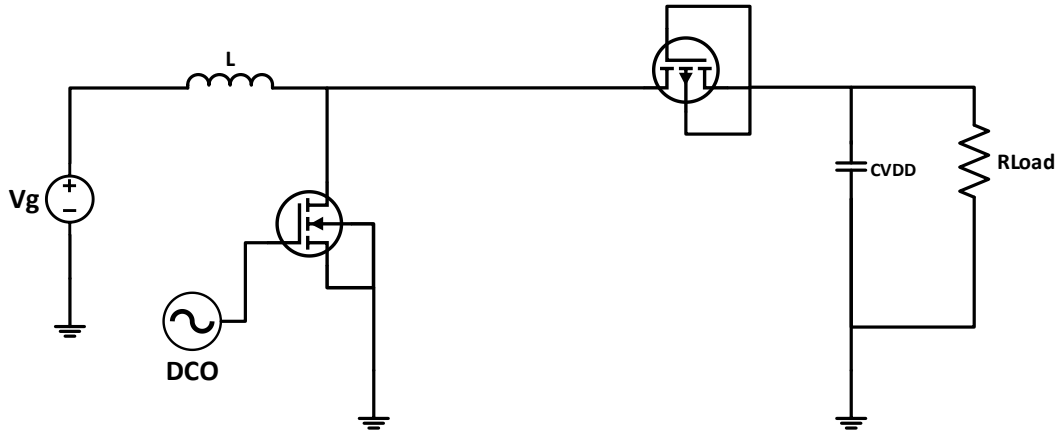


Figure 2-13 DCM with diode implemented as PMOS

The diode is modeled as a diode connected PMOS, the bulk is connected on the capacitor of the VDD formation to keep the diodes between bulk and source or drain in reverse biasing action, and as $R_{on} \propto \frac{L}{W}$, we are required to minimize the on resistance for conduction losses so the L is set to its minimum level, since we might have an overshoots in the start of the MPPT loop operation so we use high gain devices (thick oxide devices) to keep the MOS and Loop safe at operation, and for its switching action in the DCM operation, the W is simulated to get the min. net losses for this device and reported in table 2-2, this is made for the PMOS, while the NMOS as a switching MOS, there is two aspects of design, the conduction losses and the switching losses, so we define the device as standard device not subjected to high overshoots as it is isolated from the path of the capacitor, the L is set to its min. value, while the W is simulated for optimum losses.

Table 2.1-2 Sizing for boost converter

Transistor	W	L
M1	**8 mm**	**350 nm**
M2	**4 mm**	**130 nm**

The simulations to get this optimum value of sizing is done across the band of frequencies used, it is logical that the highest frequency point is the point of highest losses and hence at designing this loop we start perturbation from lowest frequency to avoid reaching the highest losses, which lead to highest quiescent power.

Another method for implementing the diode, is active diode implementations using a level sensitive comparator and other devices helping the system to operate with an active diode implementation.

To sum up for the design aspects of the boost converter, we define a table of parameters that define the requirements for such block.

Table 2.1-3 List of specs for Boost operation

Parameter	Achieved Spec
f_{clk}	1266 Hz: 17838 Hz
Perturbation steps	16
Major Clock division	64
Input voltage range	50 mV: 500 mV
Matching Range	100: 800 Ω

2.1.4 Switching circuitry, filtering and storing:

A LPF is used so that it can filter the ripples of the output of boost and decrease them to help the hysteresis comparator to have more relaxed design specifications, the LPF is a simple RC filter, where value of R and C is set relative to the frequency of filtering, since the lowest frequency for boost operation is 1266 Hz, which is low so that R and C are set off-chip, the output of the filter is feed to a switching circuit with major cycle, where new and old voltage are compared, the switch design is critical for power consumption, so we compromise between different switch types.

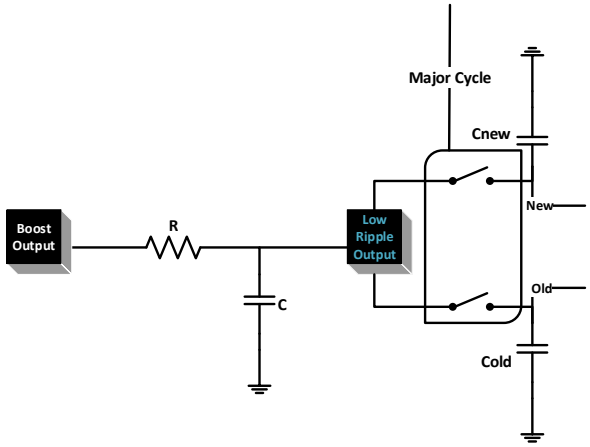


Figure 2-14 Switching circuitry

A switch can be NMOS, PMOS or transmission gate, for an NMOS switch, the definition of the V_{gs} is defining the NMOS as a strong logic '1' creator but a poor logic '0' adapter, this is defined for the requirements of gate, drain and source relative to that of threshold, same applies for the PMOS, but in a reverse way, so the PMOS is a strong '1' but a weak '0', so for a strong '1' and strong '0', we combine both cases using a transmission gate, in

our case as the transmission gate would reflect a complexity and more power consumption, so we used a conventional NMOS switch, that would not introduce a large error in the loop.

2.1.5 Hysteresis comparator [11]:

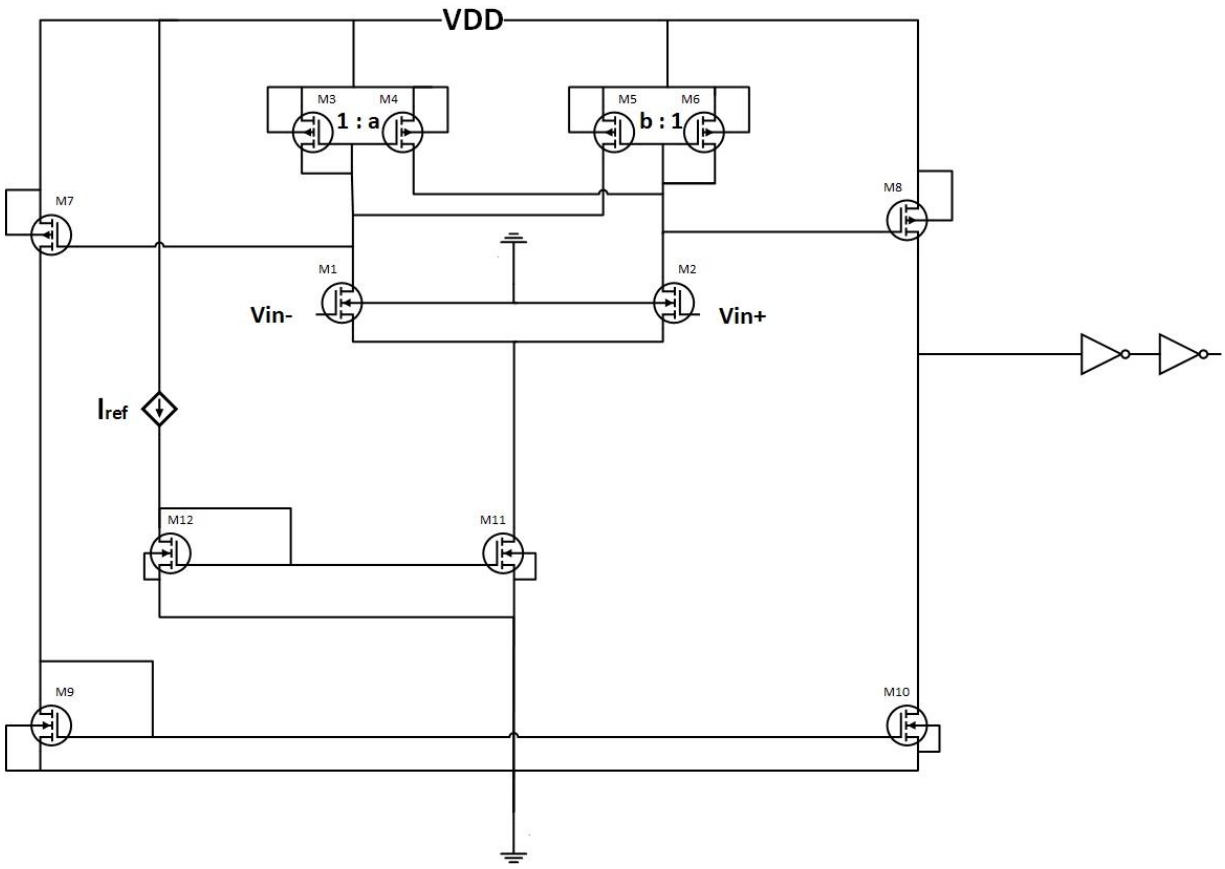


Figure 2-15 Hysteresis comparator using current unbalance

To define the functionality of the hysteresis comparator, the following analysis is made into use, where each transistor is set in a certain operation pattern and mode to allow the operation with reasonable hysteresis window at bias of 10 nA.

For $V_{in}^{+} > V_{in}^{-} + V_{hys}^{+}$, we require the output to go high as indication for the output voltage is high enough to be differentiated from the low level, the output of derived by inverters that define a strong logic'1' and logic '0' for proper operation of the digital controller.

For $V_{in}^{+} < V_{in}^{-} - V_{hys}^{-}$, the output is low, and hence the controller would define the large and the small changes within the voltage to take the decision of perturbation.

To define the hysteresis levels and the window with respect to the design aspects and steps, the following analysis is defined:

$$I_4 = aI_3\,, I_5 = bI_6\,, and\ I_3 = I_6\ @\ equilibrium \rightarrow (2.29)$$

$$I_{M_1} = I_3 + bI_6, I_{M_2} = aI_3 + I_6, I_{M_1} + I_{M_2} = I_3 + bI_6 + aI_3 + I_6 = I_{bias} \rightarrow (2.30)$$

From equation 2.29 and 2.30 we defined the current distribution and the equilibrium that may lead to cross the borders of the hysteresis window, to fully define those points and the window design aspects, we should go further in defining the operation of each transistor.

For M1,$0 < V_{gs_1} < V_{th}$ for subthreshold operation, this can be defined relative to the level of current subject to M1, same apply for M2, the difference between M1 and M2 in the gate voltage define a change in the value of the current across the two branches which lead to the loss in equilibrium, and so output goes positive or negative with a gain relatively, as the used operation is subthreshold so the gain of first stage is the highest gain and approach the intrinsic gain.

At subthreshold,

$$g_m = \frac{I_d}{nv_t} \rightarrow (2.31)$$

Where n is a certain constant and v_t is a temperature dependant voltage, $v_t = \frac{KT}{q}$

And to define the requirements of other transistors,

$$M1, M2 \rightarrow subthershold\ operation$$

$$M3, M4, M5, M6 \rightarrow Saturation\ operation$$

Our concerns is the Systematic offset and random offset so, for systematic offset, dependency goes for λ, the L is set to its maximum limit ($20\mu m$), and hence the speed is not a requirement this can be done, and as random offset is defined for $\frac{A_{v_t}}{\sqrt{WL}}$, so the W is hence increased to redefine this at the input pair.

By solving the equations and the current balance we can reach the final form of the hysteresis comparator:

$$as\ I = I_{D_o}\frac{W}{L}\mathrm{e}^{\frac{V_{g_s}}{v_t}}, and\ from\ equation\ 2.29\ and\ 2.30,$$

$$V_{hys_+} = \xi v_t \ln\left(\frac{a+1}{b+1}\right), and\ V_{hys\_} = \xi v_t \ln\left(\frac{b+1}{a+1}\right) \rightarrow (2.32)$$

The hysteresis window is set for certain b and a factor to compensate on the ripples in the boost converter, relative to the different changes and frequency levels that require such action to be taken.

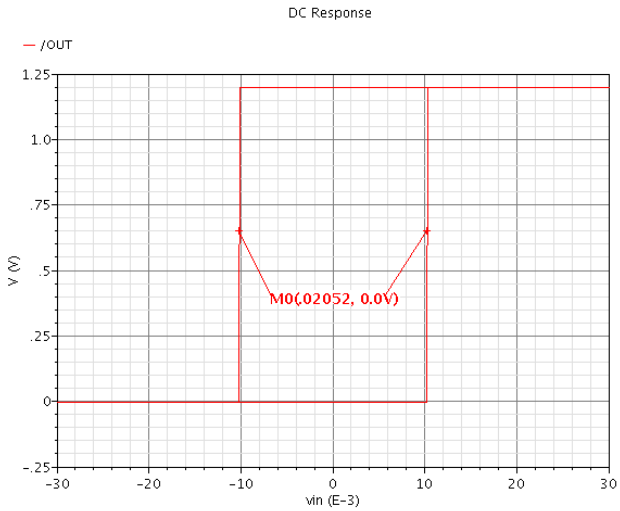


Figure 2-16 typical hysteresis window

The optimum window of compensation is defined for 20 mV, and as shown in Fig.2.1-17, the window suffer no offset relatively, Monte Carlo simulations are performed to define the change in random offset, the 3σ is 6 mV obtained by a simulation on another technology of 130 nm UMC due to the failure of this kit to provide a Monte Carlo simulations.

Table 2.1-4 Process variation for hysteresis comparator

Fast Fast	Vth-n, Vth-p Decreased M1, M2 may shift from subthreshold	Gain, V_{hys_+}, and $V_{hys\_}$
Fast Slow	Vth-n dec and Vth-p increase, this may shift M1,M2 from Subthreshold and M3,M4,M5,M6 from Saturation	Gain, Current Mirroring Ratio, V_{hys_+} and $V_{hys\_}$
Slow Fast	Vth-n increase and Vth-p Decrease, M1, M2 may shift from subthreshold to off	Failure in performing the comparing
Slow Slow	Vth-n and Vth-p increased M1, M2 may shift from subthreshold to off	Failure in performing the comparing
High Temp (120)	$V_{hys_+} = \zeta V_T \ln\frac{a+1}{b+1},\ V_T \alpha Temp$ Vth- n, p decrease	Hysteresis window increase Gain, Current Mirroring Ratio, V_{hys_+} and $V_{hys\_}$
Low Temp (-40)	$V_{hys_+} = \zeta V_T \ln\frac{a+1}{b+1},\ V_T \alpha Temp$ Vth- n, p increased	Hysteresis window decreased, Failure in performing the comparing

*2.1.6 **Digital Controller:***

The digital controller is defined to perform the flow chart and the steps for the perturbation in the loop, a good controller can allow the system to track the required MPP without losing it or oscillating in the processes, the controller is very critical in the loop as it is what connect everything and define every point.

A digital block is critical to stand beside an analog block, a digital block is critical in a system and it need to have a consideration for it's routing and for it's power lines, so to avoid all those problems, digital controller is built using a VerilogA modeling code, and it is proposed to be written using a Verilog or VHDL code on an FPGA interfacing with the PMIC or on an Arduino nano within the SOC.

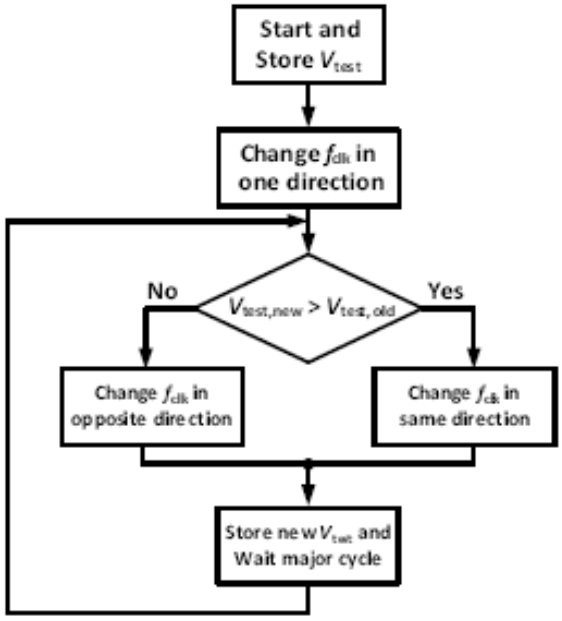


Figure 2-17 Flow chart of the MPPT loop

From the flow chart shown, we defined the states of the controller that would help it to operate the loop, those states are introduced in steps as follow:

1. Start and Store $V_{test.}$
2. Perturb DCO frequency in one direction (chosen as increase).
3. Check if New Vs Old voltage is larger or smaller (check CMP is 1 or 0).
4. Perturb according to the CMP.
5. Store new V_{test} and cycle up from step 3.

To translate those steps in logic functions we defined the step in a new shape as follow:

1. Initialize code as All 0's.
2. Increment code by 1 at start up cycle.
3. If CMP=1, increment code.
4. If CMP=0, decrement code.
5. If Code is All 1's, no increment and only decrement.
6. If Code is All 0's no decrement and only increment.

This can be defined by a 4-bit synchronous up/down counter with hold states at all 0's and all 1's, and a reset point, synchronous reset and asynchronous reset.

The counter start up point differs from different cases as to start at all 1's or all 0's or intermediate, as what was brought in earlier sections that it is required to get a low power start point to avoid losses, so with respect to the design of the DCO defined in the next section, the start point is defined as all 1's instead of all 0's while maintaining all other control steps and states.

2.1.7 DCO:

The digital controller oscillator topology used is a current starved ring oscillator with a switched capacitor bank to set the frequency relative to the input bits, to define this topology it is required to define the functionality of a simple ring oscillator and then a current starved ring oscillator.

2.1.7.1 Ring oscillator functionality:

A simple ring oscillator is defined as a cascaded inverter of ODD number to define a negative feedback topology, a simple inverter has gain of $-(gm_n + gm_p)(ro_n//ro_p)$ so an odd cascaded ring oscillator produce a negative feedback case, the originality in the oscillatory profile of such topology is defined as follow:

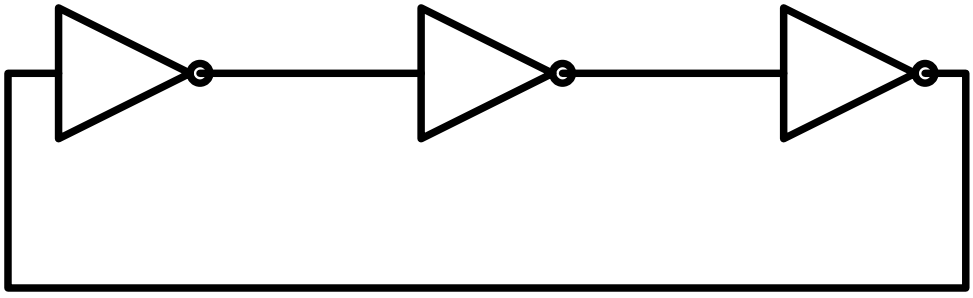


Figure 2-18 3 stages ring oscillator

to define the functionality of such structure, let's consider the relation between two simple stages:

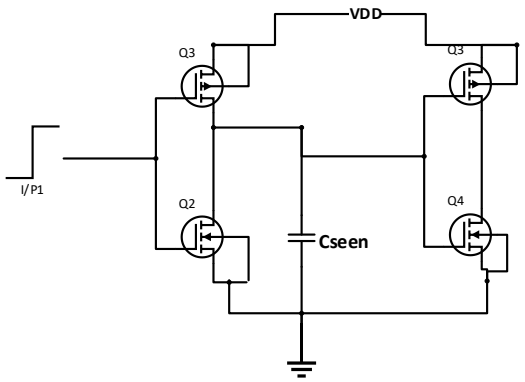


Figure 2-19 simple two stages of the ring oscillator

1. Assume NMOS and PMOS are matched, $\frac{W}{L})_P = 2\frac{W}{L})_N, \mu_n = 2\mu_p, K_n = K_p$, so the drive capability is equal, as subjecting a step function on input , the output would be defined to charge a capacitor with respect to the resistance seen within the branch, a simplification is made for the capacitor seen to have the form of $C_L = \frac{5}{2}C_{ox}(W_nL_n + W_pL_p) \rightarrow (2.33)$

While the resistance of the branch is defined as a simple on resistance branch

$$R_{on} = \frac{1}{\frac{\mu_n C_{ox} W}{L}(V_{gs} - V_{th})} \rightarrow (2.34)$$

A simple inverter would be subjected to the charging of the load capacitor and relative to the on resistance we define a certain delay time $\tau_p \alpha RC$, for a 3-stage ring oscillator, we define 3 τ_p for on state, and 3 τ_p for off state, so the frequency of oscillation is define as:

$$f_{osc} = \frac{1}{6\tau_p} \rightarrow (2.35)$$

2.1.7.2 Current starved ring oscillator:

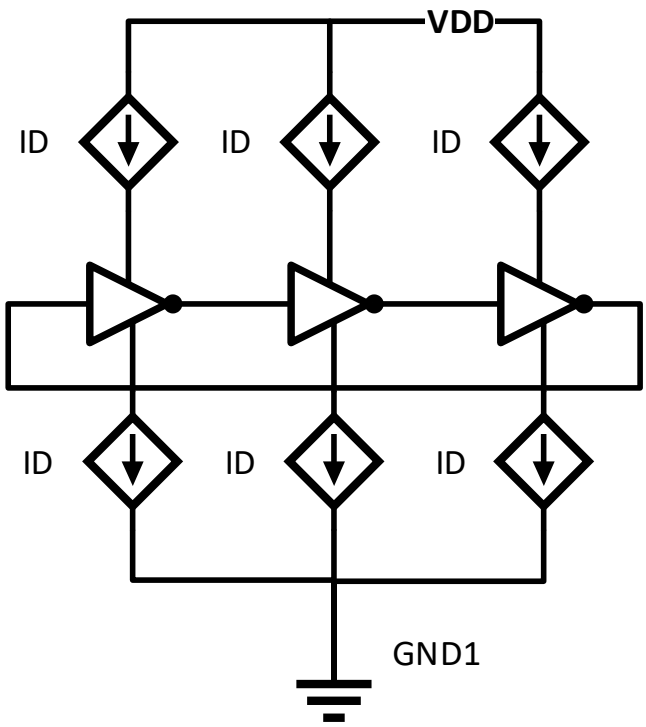


Figure 2-20 current starved VCO model

The current starved VCO is a ring oscillator controlled by set of current mirrors(sources) that increase or decrease the frequency by increasing the action of charge and discharge, this can be defined relative to the conventional ring oscillator where by defining the current action with respect to the regions of operation of such system relating to the analysis given in [12]:

$$\tau_p \propto \frac{C_{tot} V_{ctrl} N}{I_D} \rightarrow (2.36)$$

$$f_{osc} \propto \frac{I_d}{N C_{tot} V_{ctrl}} \rightarrow (2.37)$$

It is defined that the oscillation frequency is dependent on the current used and the number of stages and total capacitance which is defined by equation 2.33 and the control voltage, there exist relative to such equation numerous numbers of design procedures to defined such DCO, one is to use a DAC that control the control voltage, but relatively DAC is a power hungry block which violate the requirements of the power consumption, then we can make a switching criteria of stages where different stages is added, but also this would add up to the power consumption and power budget, it was found that the optimum way of perturbation is to change the total capacitance seen by each stage using a bank of capacitors, the full circuit is shown in fig.2.1-22.

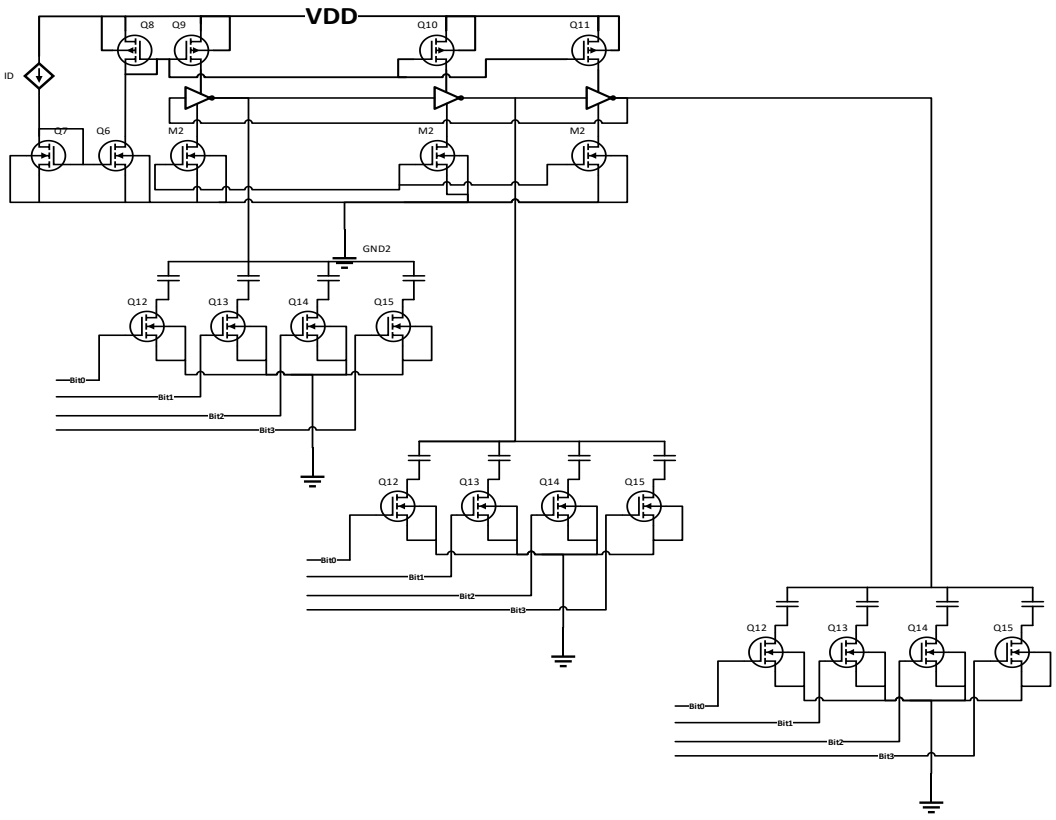


Figure 2-21 DCO implementation

Relating to equation 2.37, defining the bank of capacitors is relative to what C_{tot} resembles as a value, the W_n and L_n relatively also the PMOS sizing is set low for a low total gate capacitance and in simulation C_{gs} is measured to identify the value of total capacitance as it is the highest contributor, at biasing of 75 nA, it is found to be of 2.6 fF value, the value of the capacitors are chosen relative to the division value (1pF,2pF,4pF,8pF) those values are set to have a relative constant step and equal spacing in the matching between each two points of perturbation, and the pF value fully eliminate the total gate capacitance contribution leading to a good termination. \

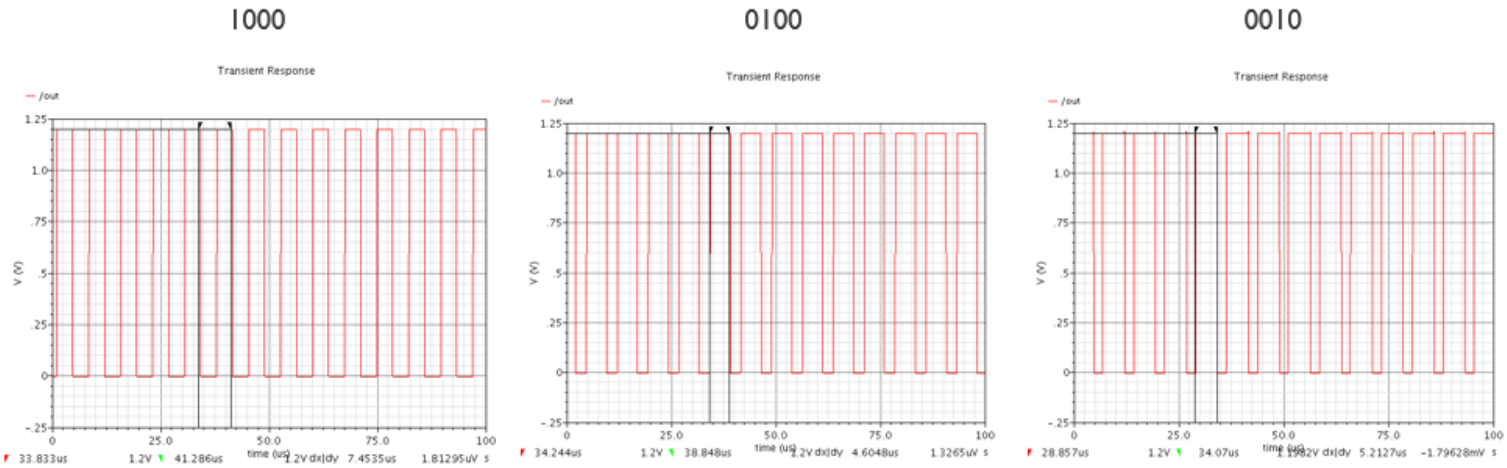


Figure 2-22 Perturbation in frequency vs bits of the digital controller

2.2 Integration of the MPPT Loop:

Reaching the specs of each block, integrating the blocks with a clever technique is essential for a good operation, this means analyzing the load effects on different points, building the MPPT loop to be compatible with other block in system, and testing the full loop as input and output, and defining the overall efficiency and tracking efficiency and limits of matching and full specs of the system.

2.2.1 Gate driver:

To define loading problems, we define what is the blocks within the loop that may have a malfunctioning profile due to loading, a very critical point in the system is between the switching NMOS in the boost and the DCO, the switching NMOS would have a very large capacitance due to the large values of width, this mat lead to a capacitive loading on the DCO, shifting the frequency range into a different location that may lead to very critical problem, to help solve this problem, a gate driver is used to drive the large capacitance, this is illustrated as follow:

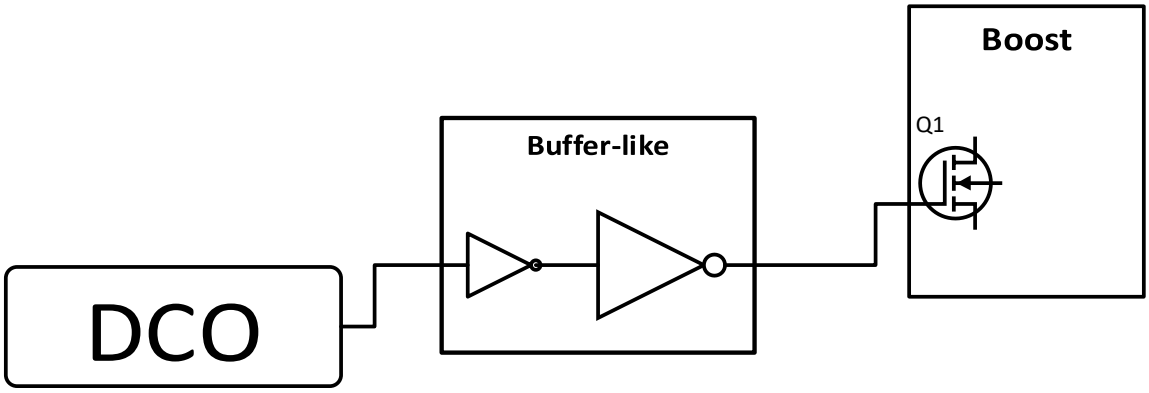


Figure 2-23 Gate driver between boost converter and DCO

For a gate driver, we cascade the inverters in a pattern where the sizing is taken into an ascending pattern in sizing, this is to decrease the action on the on resistance, and to allow a stepped isolation without leading to any glitches in the system.

2.2.2 Results and simulations of the loop:

To test the loop of MPPT a Thevenin model is used to model the antenna and rectifier existing before the PMIC, 5 test cases are made, 3 are from the survey presented in the first chapter, and two extremes for very low and very high levels of power, those tests set the general specs and description of the system used.

Shown in table 2.2-1, the results of each test case and it's description, where each test is compared with respect to the maximization occurred, the output power and loop efficiency, the quiescent power and the output voltage.

Table 2.2-1 Comparison between different models of testing

Test Number	V_{th}	R_{th}	Max. Power	Input Power	Tracking η	System η	Quiescent power	Output voltage	Power Output
1	400 mV	250 Ω	160 µW	155 µW	97%	55%	393 nW	981 mV	84.8 µW
2	500 mV	500Ω	125 µW	121 µW	97%	63%	380.5 nW	874 mV	76.37 µW
3	500 mV	250 Ω	250 µW	246 µW	98%	44%	372.4 nW	1 V	108.3 µW
4	200 mV	300 Ω	33.3 µW	30 µW	91%	64%	372.6 nW	442 mV	19.55 µW
5	700 mV	300 Ω	408.33 µW	406 µW	99%	40%	386.7 nW	1.265 V	160 µW

*2.2.2.1 **First Test:***

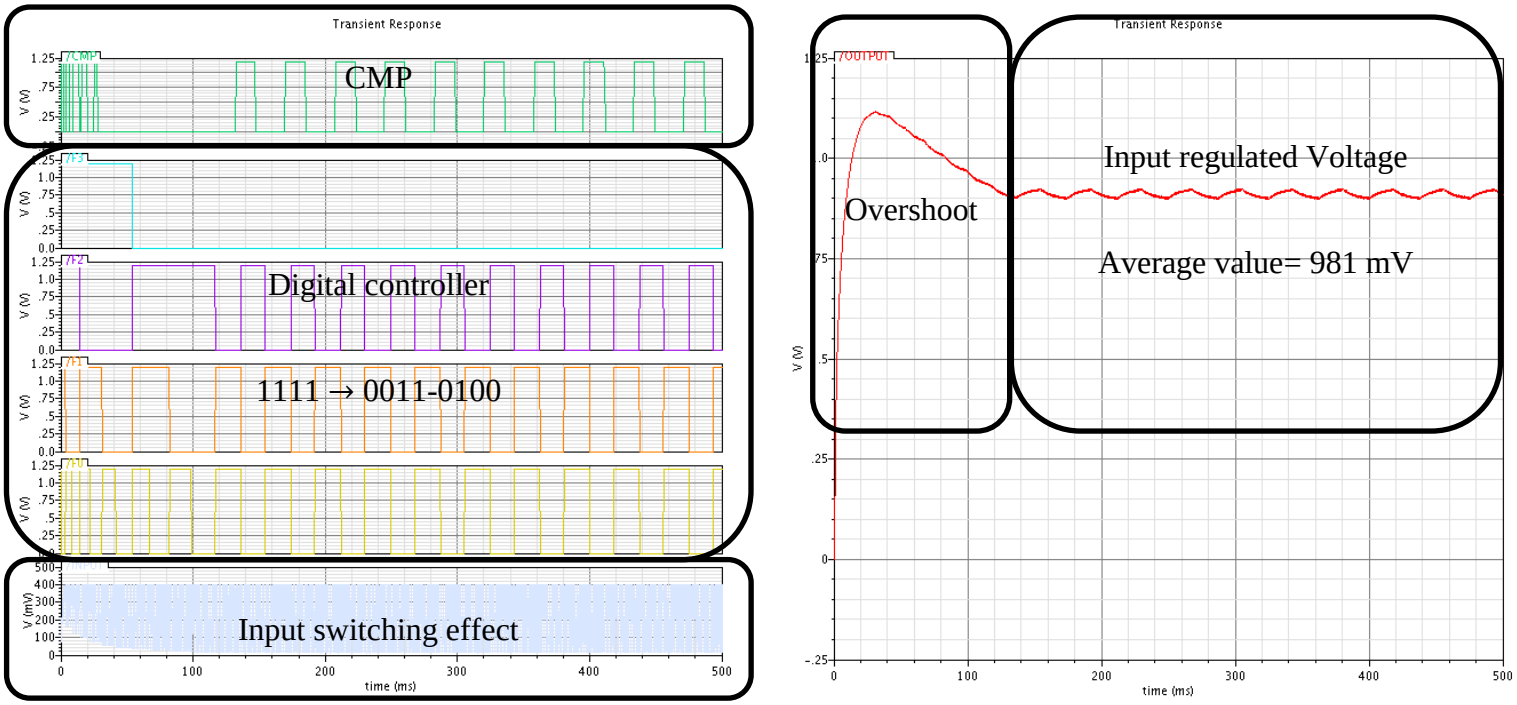


Figure 2-24 400 mV, 250 Ω test model results

In Fig. 2.2-2, the results of the simulation for the Loop at the defined model is shown, at the first steps of operation, the controller start with all 1's and then it decrements till reaching 0011 and then increment to 0100 and ripple between those two numbers, this means that the loop reached an MPP point and made a hold point on it, the hold point is a rippling point, the comparator action is shown within the simulation, it ripples continuously at first as a start up of boost is analogic to that of a LPF which lead to a fighting new and old voltage, as the division in the major clock is high enough to pass such ripples, yet, an overshoot occur at startup, this is a very critical action that may lead to a disastrous break down effect to the circuits supported by such VDD, the option to solve such action is a

battery protection block to model al voltage changes and avoid the overvoltage condition introducing a fourth mode of operation to the DCM at output voltage greater than 1.2v, and to avoid this action to harm the boost converter, thick oxide devices are used.

As the art of operation is defined, for the spec's definition, we define certain calculation steps as follow:

1. For maximum power, $P_{max} = \frac{V^2}{4R_{in}} = 160\ \mu W$.
2. For the calculation of the input power, we can define $P_{in} = V_{avg} \times I_{avg} = 155.2\ \mu W$, An important point of interest is to differentiate between different values of input power calculations as rms or average, at DC, rms and average are the same, they are defined for same case, but their definition differs in case of finding a certain point of change as ripples, that is why most of the power management systems fight over which definition of both wins, it is widely defined that the average is taken instead of the rms, as it defines the ripples better and hence the DC component of the V and I.
3. $\eta_{matching} = \frac{P_{in}}{P_{MPP}} = 97\%$
4. Quiescent power is defined instead of current, as there exists a path of switching that consume extra power than that of the current consumed in the system, so defining a power term is better in this case than current, it is measured in this test to be 393 nW.
5. $\eta_{System} = \frac{P_{out}}{P_{in}+P_Q} = 54.5\%$, where $P_{out} = 84.8241\ \mu W$, and output voltage is 981 mV as average.

2.2.3 Other Test cases:

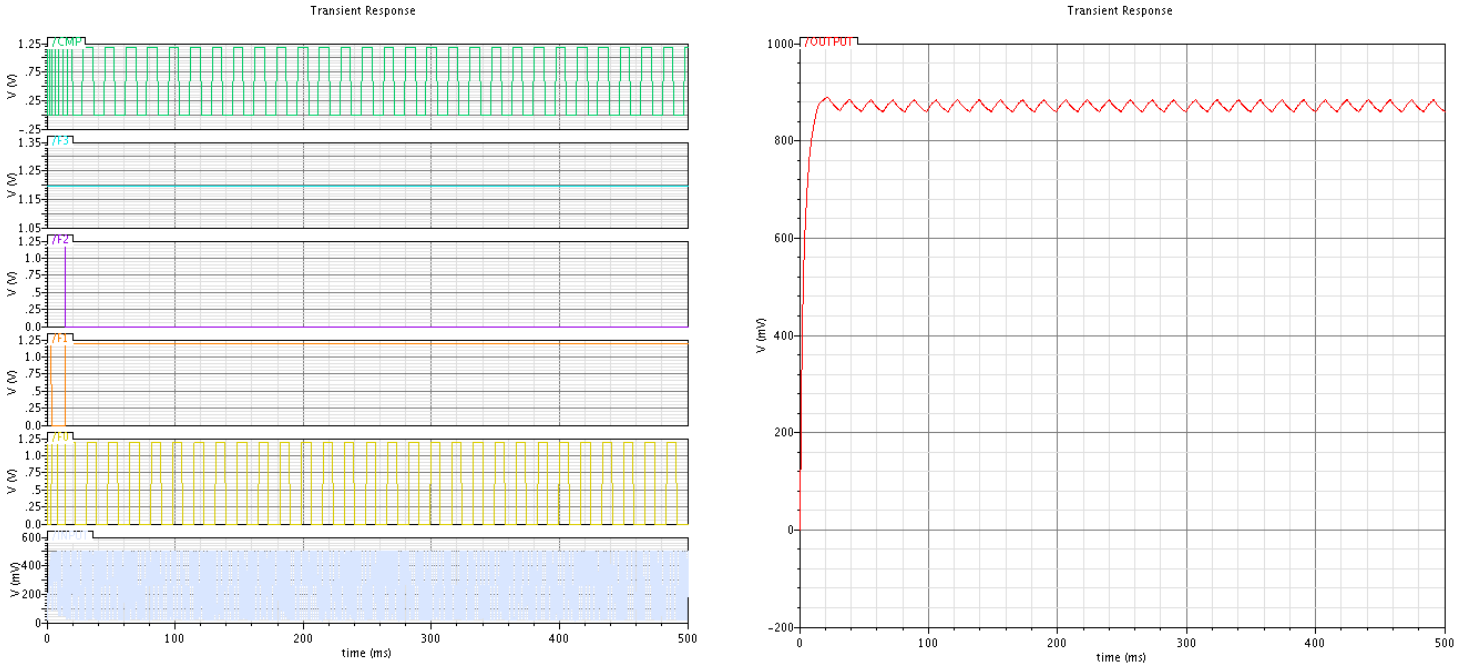


Figure 2-25 Test 2 simulation results

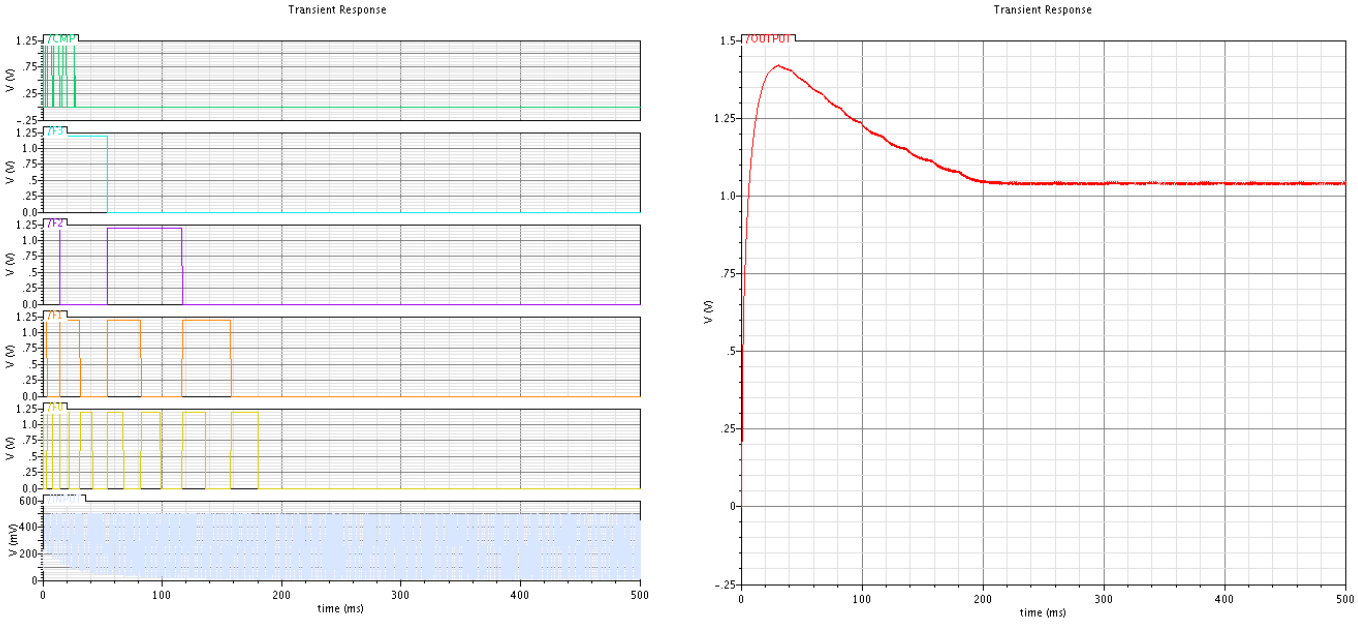


Figure 2.2-4 test 3 Simulation results

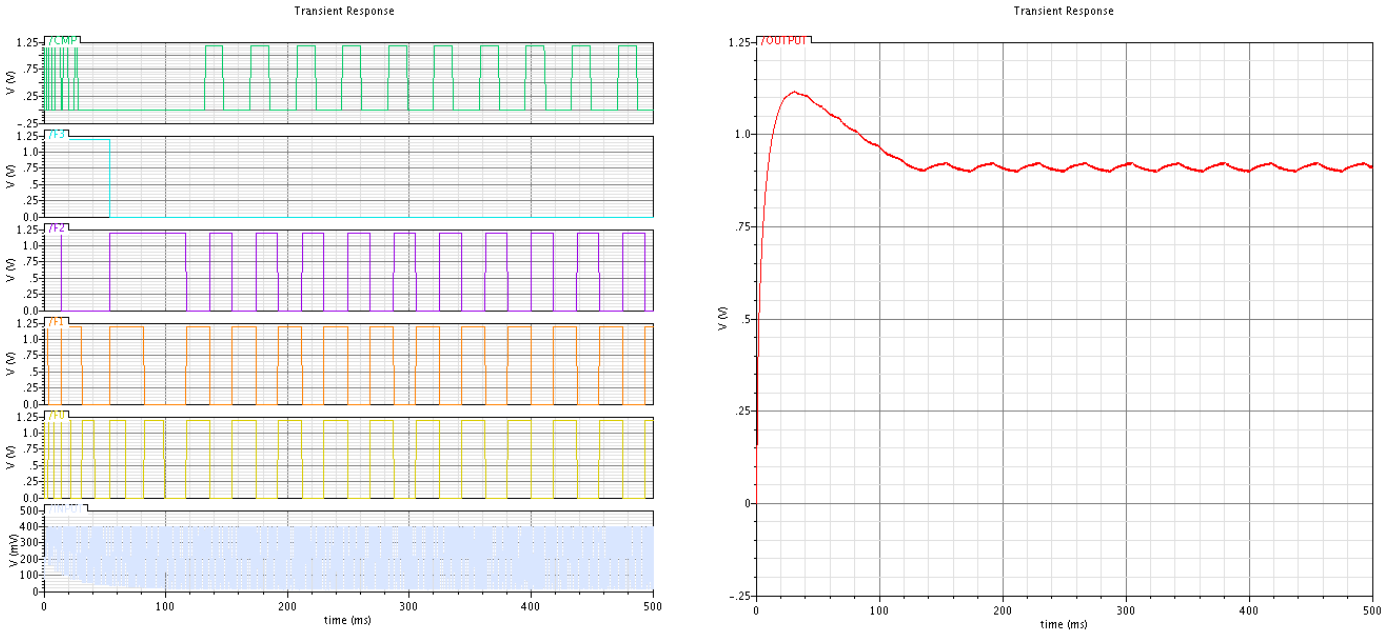


Figure 2-26 Extreme test case for low power

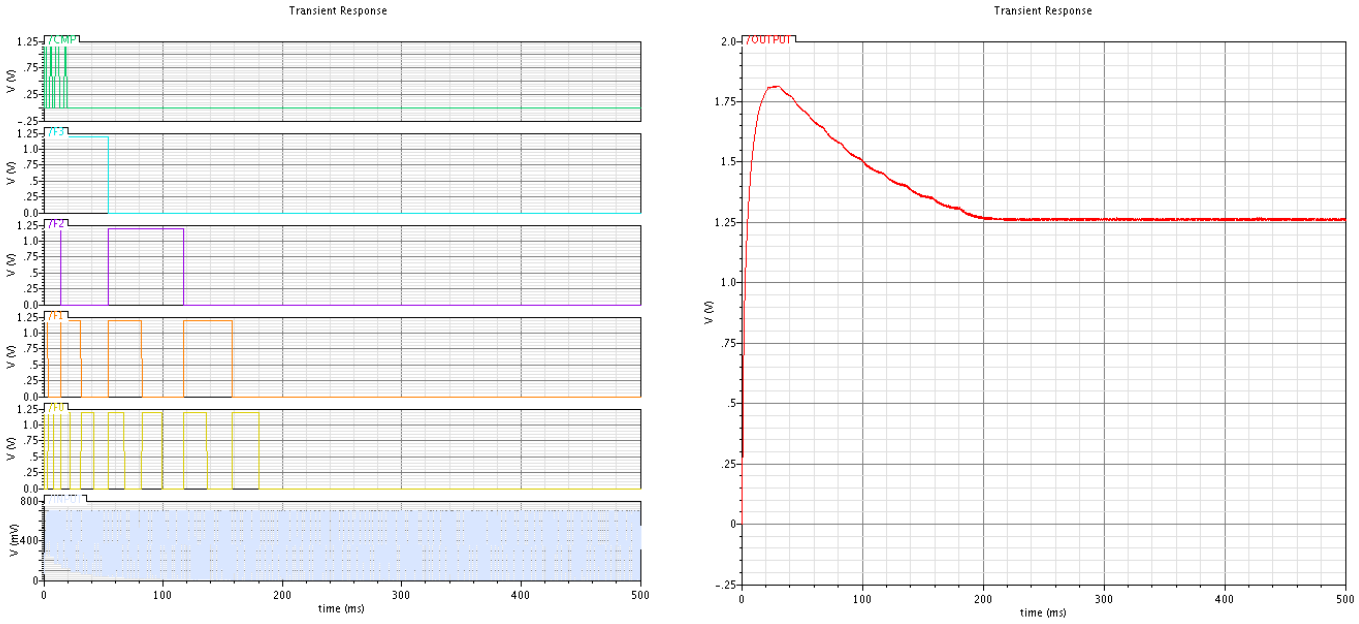


Figure 2.2-5 extreme test case for high power

for the shown four test cases, we can define different specs as shown in table 2.2-1, those specs are defined relative to the ability of the loop to approach matching, for test case 2, we can find that the system efficiency has highly increase, and the quiescent power decreased than that of first test, the matching efficiency is the same as first test, there exist no overshoots and the output voltage is within our specs and requirements with value of 873.9 mV, at boosting up the power to its maximum limit, it is found that the last point in regulation is that of test 3, the third test is defined at such point, with power of 250 µW, reaching a high matching efficiency, but high system losses due to the high frequency action, going beyond this extreme would be critical as found in the extreme test of high power, the matching in this test is very good reaching around 99%, but due to the subjection of this point to a high frequency action continuously with no regulations, losses are high enough to get a system efficiency of 40%, and at low power extreme case the losses would be very low, and hence we boost up the efficiency of system to 64% but the matching efficiency is 91%, the best test case is the second test, so this point is defined as the highest capability of such MPPT at the typical design case.

Table 2.2-2 General achieved specs of the MPPT loop

Parameter	Specifications Achieved
f_{clk}	1266 Hz: 17838 Hz
Perturbation steps	16
LPF order	2^{nd}
Hysteresis window	15 mV
Major Clock division	64
Tracking Efficiency	95%
Highest achieved Efficiency	64% at -5 dBm

2.2.4 Corner simulations:

A corner simulation is defined as a simulation to define the changes occurring within a certain process and temperature actions, this is defined in process for four cases as fast fast, fast slow , slow fast, slow slow, the fast and slow is relative to the NMOS and PMOS, and it is defined as fast or slow relative to an inverter model, defining its speed action as fast or slow, this is relative to the threshold voltage, as threshold increase, speed decrease, while as the threshold decrease, the speed may increase, this can be related to the rules of the on resistance and the total gate capacitance.

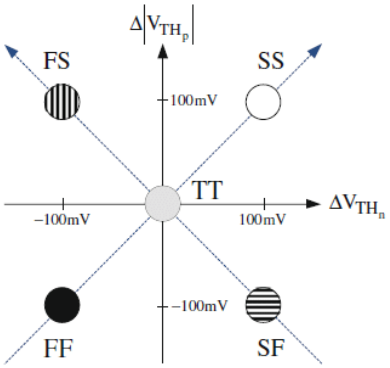


Figure 2-27 corner simulations vs change in threshold voltage

For the temperature, we define another two extremes, one is a -40^oC and 125^oC, those levels of temperature are the points where the subjection of the IC may go, the threshold voltage is function in temperature as a inverse response action, this also define a change in the circuits operation relatively.

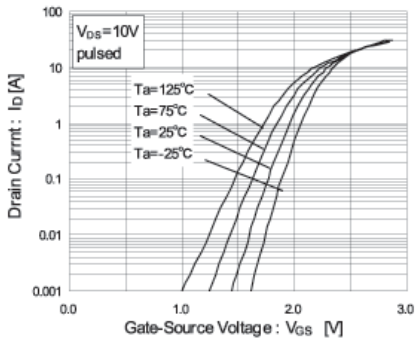


Figure 1: I_D-V_{GS} Characteristics

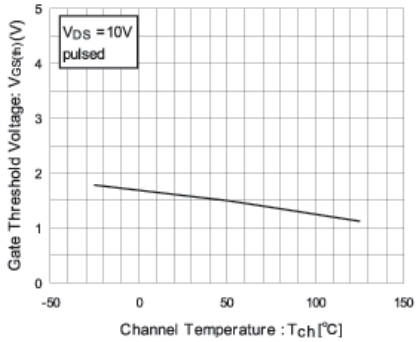


Figure 2: Threshold Temperature Characteristics

Figure 2-28 threshold voltage change with temperature

Summing up both those actions, we defined different simulations for the different blocks of the system, each block is simulated for the four actions, and the following results are defined for each block.

2.2.4.1 DCO corner simulations:

To define the changes in DCO due to corners, the threshold voltage does lead to cause certain changes in the operation of the current mirror, as changes in the compliance voltage and in the mirror ratio, also the inverters operation would differ as the threshold voltage is a contributor in the on resistance value hence it directly changes the frequency, summing up all those point, we can reach an estimation for the changes observed in the simulation.

we defined the fast fast, and the slow slow as they are the most significant to define, the fast fast variations vs the temperature variation, at fast fast, the frequency variation at -40 degrees is -254.3 Hz while at 125 degrees it takes value of 600 Hz, those variations are defined for the range reports in the previous section, which define shifts that are not that much, this variations would also be compensated by the adaptivity of the loop.

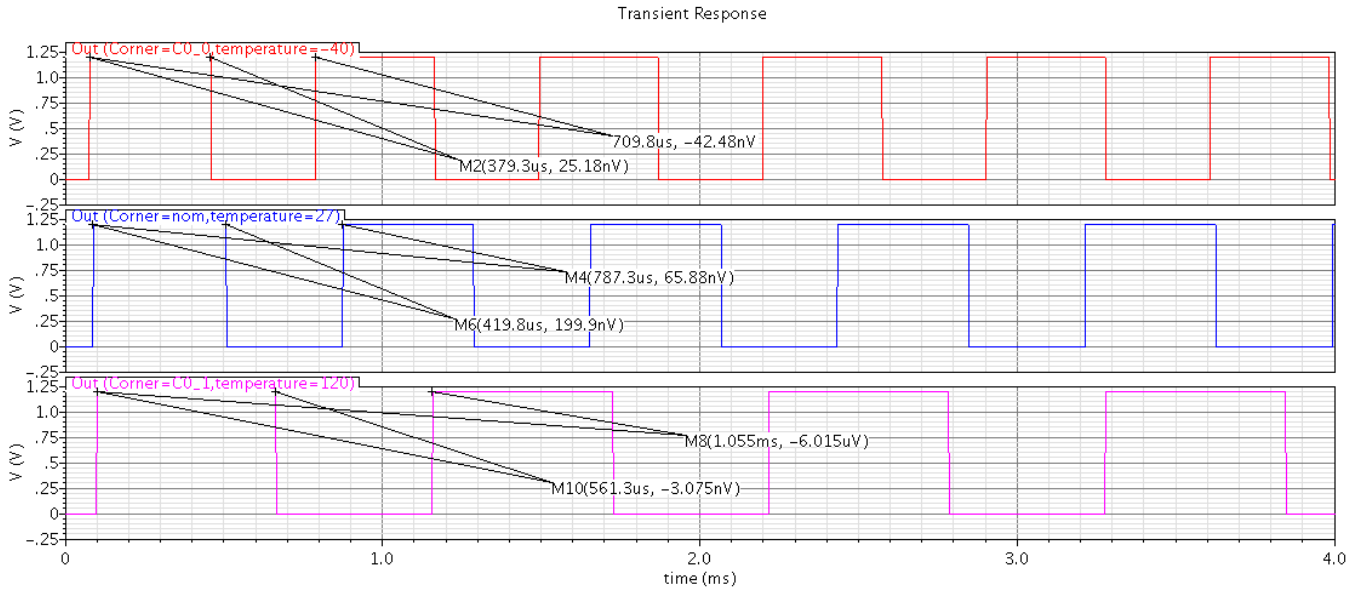


Figure 2-30 DCO fast fast simulations for -40 and 125^{o}C

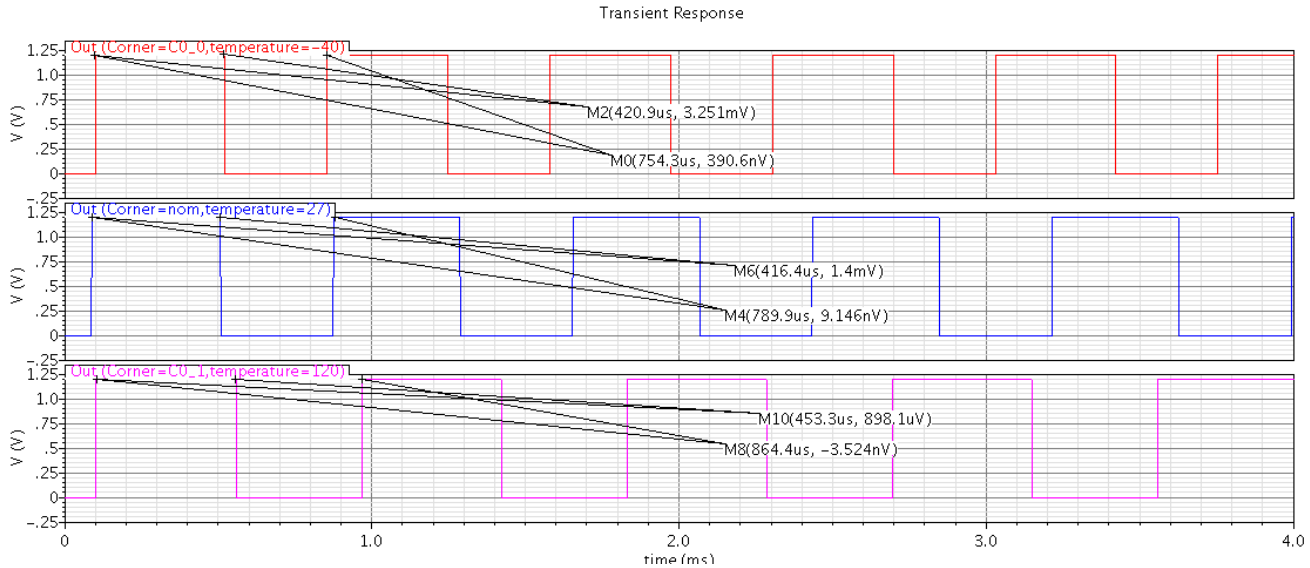


Figure 2-29 DCO slow slow simulations for -40 and 125^{o}C

To define if the corner simulations are critical or no, we define if the matching is violated or no, and the matching is not violated as the change in the steps would no break the matching sequence by any means, also the values of the capacitors may vary with the PT actions on the system.

2.2.4.2 Hysteresis comparator changes:

Same simulations apply for the comparator, the hysteresis window as defined in equation 2.32 is fully dependable of the temperature due to the V_t factor, so if we defined the variations of temperature, we find that they would contribute very harshly on the window, not only the temperature but the variations in the current balance due to threshold voltage may lead to critical problems of the window, the problems existing are defined with two aspects, the hysteresis window would increase very large, or the hysteresis window would decrease very large, if increased very large, the decision making is of large errors, while for the small window, ringing may occur due to the large ripples, so we compromise in the hysteresis comparator and define which is better, and also a calibration loop is proposed that may be added in further versions of such IC.

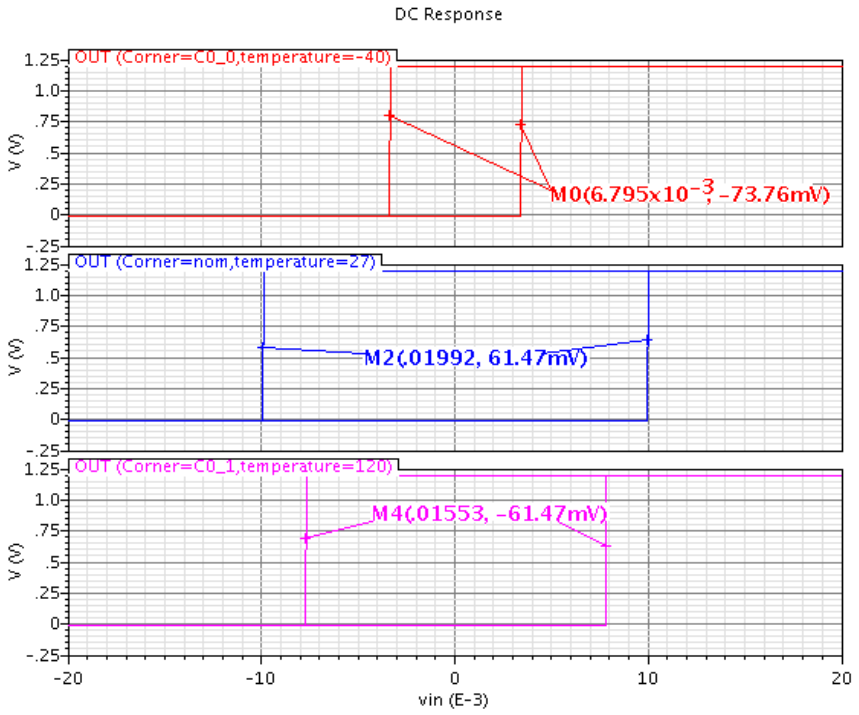


Figure 2-31 Hysteresis comparator Fast Fast variations

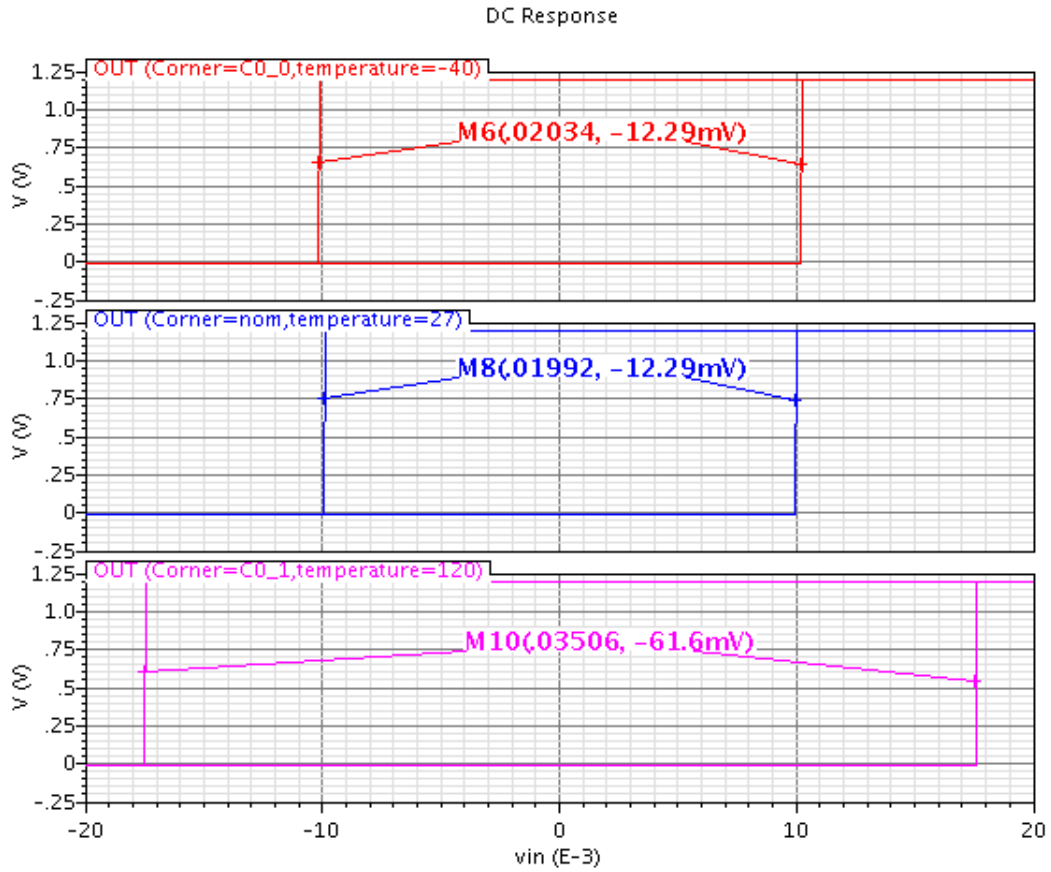


Figure 2-32 Hysteresis comparator Slow Slow variations

It is shown in fig. 2.2-9 and 2.2-10, that the variations reach critical values even after calibration in the design, some variations may indeed lead to the failure of the loop, so a sensing loop was proposed to compensate on such system and design the system for better operation, this loop is planned to be in our future work within this PMIC design.

*2.2.4.3 **Boost converter simulations:***

For the boost converter, it is defined that the system used is dependable on two MOSFETS, the level of ripples and the power consumption depend mainly on there setting, so the process and temperature variations may by all means, affect such system, defining certain changes, the least to be affected by those changes is the boost, but they may lead to changes in it's performance, this can be analyzed by the values seen in Fig. 2.2-11 and 2.2-12.

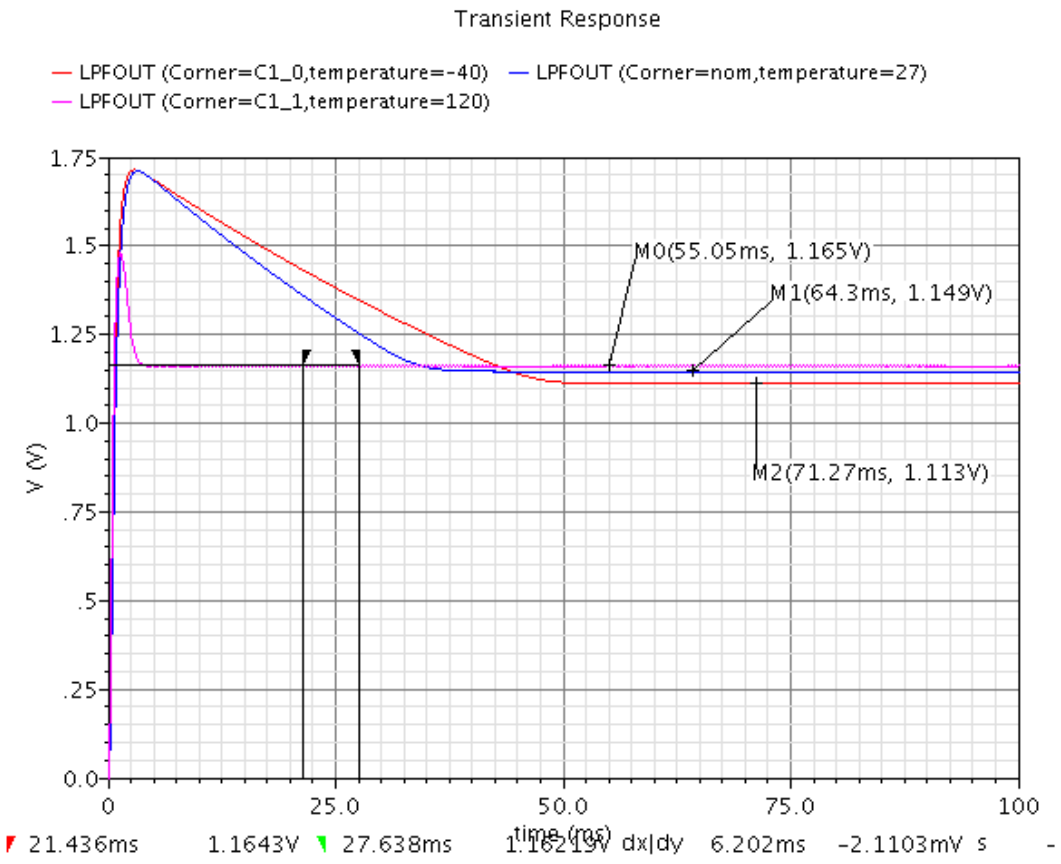


Figure 2-33 Fast Fast variations of boost converter

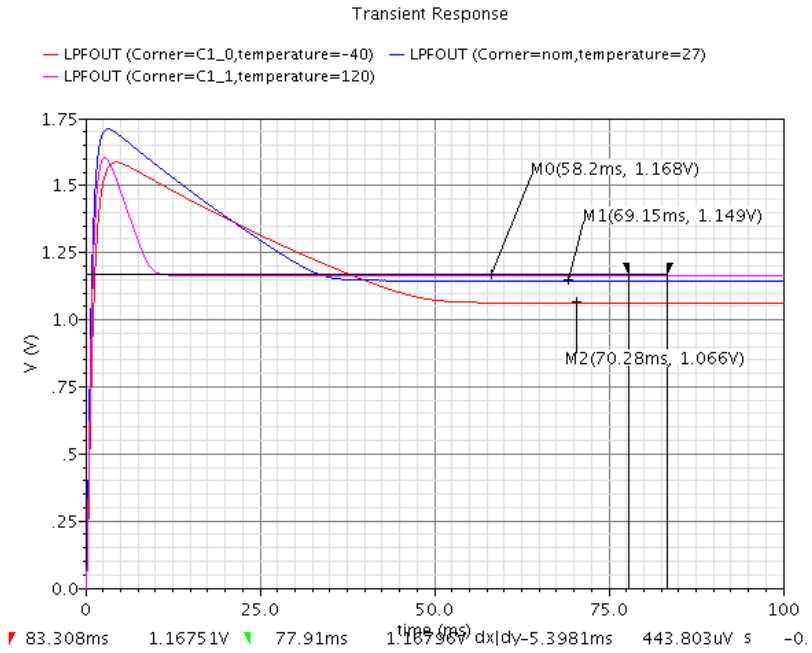


Figure 2-34 Slow Slow variations of Boost converter

2.2.5 Layout:

2.2.5.1 Layout of Hysteresis comparator:

To define a layout, set of rules and techniques are required to be followed to get a perfect layout satisfying the conditions, one of the most important layout considerations, is parasitic introduced in lines, between lines, in MOS devices, in Capacitors and between on-chip and off-chip devices, also matching between devices and decreasing the spacing and allowing the actions on the IC to be consistent on all points, noise considerations and avoidance of cross talk between lines, floor planning, all of those points define a perfect layout or a bad layout, so those considerations are the basic starting point for any layout design to reach it's requirements, in this layout design, parasitic are considered in decreasing the length of lines, and trying to work on upper metals for critical paths, for the matching common centroid is considered with a cross-quad sequence, and decreasing the

spacing between all devices, power lines and different lines are tapered to allow higher power capability and improve performance, an other aspects are defined with in the layout design.

For our design of hysteresis comparator, Different considerations are made, first and most important was the antenna rule, due to the large dimensions of certain mosfets than others, long lines are used to make the interconnections, those lines more than they may contribute certain resistance that lead to losses and bad contribution, they lead to antenna effects, so before each line interfacing with a gate of a MOS, we go higher in layers and then lower to the poly layer, this allow the termination of problems of antenna effect.

Another consideration is the layer fill rule or the density errors, those are solved by certain CAD tools to allow a consistent distribution of metal all over the IC.

Matching is defined as illustrated in the first of this section using cross-quad by using sequence of A B B A and then B A A B for the input pair, while the current mirrors already contribute the min. width so no matching is defined relatively.

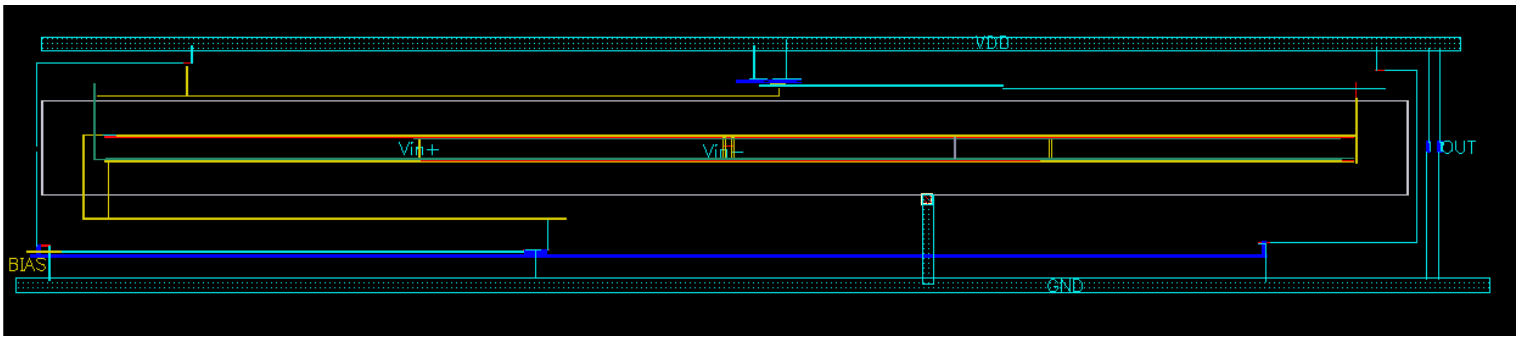


Figure 2-35 Layout of hysteresis comparator

To avoid parasitic routing is done to keep coupling between lines as low as possible and avoid the ripples on the power lines to contribute for the input pair lines to avoid the ringing of the comparator and hence the instability of the entire loop.

The design is define to pass all the DRCs that are considered with our standards and certain DRCs are not passed as layer fill, vertex error and IC corners errors, LVS is performed and the layout fully matches the schematic with all it's nodes and points, and the as no triple well technology is used, no source is connected to body and this action is simulated for the typical and designed for the required specs, and hence the layout is expected to match the requirements of the schematic, PEX simulations are performed to extract the parasitic and simulations for hysteresis comparator is made, the result in Fig. 2.2-14 illustrate the changes and actions of layout.

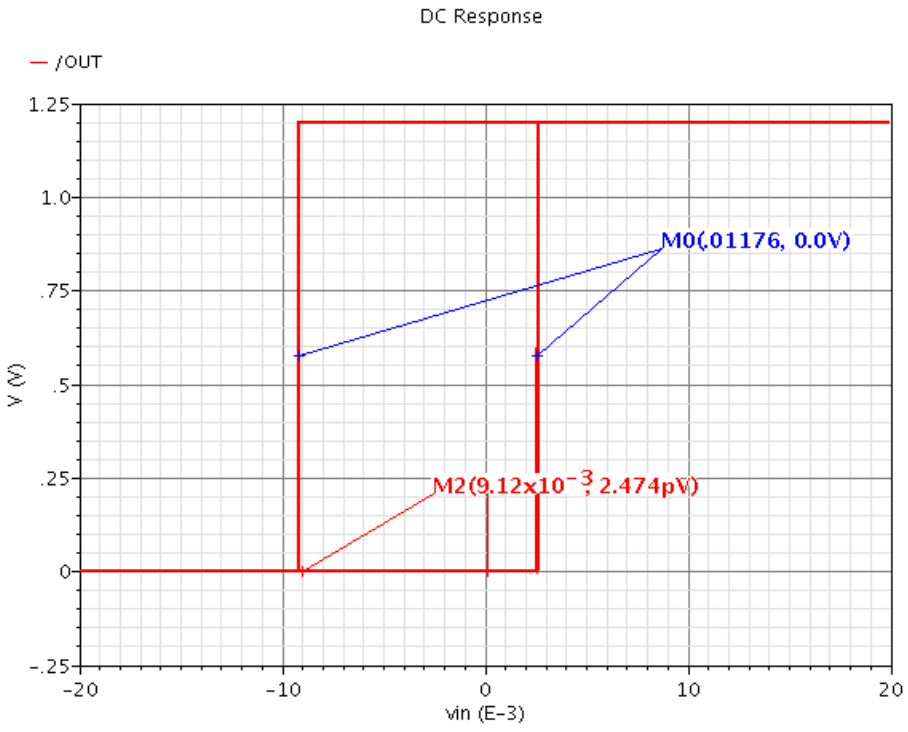


Figure 2-36 Post-Layout simulations for hysteresis window

2.2.5.2 DCO Layout

Same aspects of design for the Comparator is subjected to the DCO, the DCO layout design and results are define with respect to the change in the on resistance and the capacitance leading to change in the frequency, also glitches or ripples that may exist within the cycle of the DCO, the DCO layout have solved that no glitches would occur, the frequency at 0000 decrease from 1266 to 932 Hz while at 1111 the frequency decrease from 17838 Hz to 15213 Hz, the deviation may lead to change in the decision region from input impedances shifting the range further to lower values, also the sharpness leaking would lead to problems in switching so this action should be compensated by using extra inverter stages or modifying the layout, this is planned for future work on the PMIC.

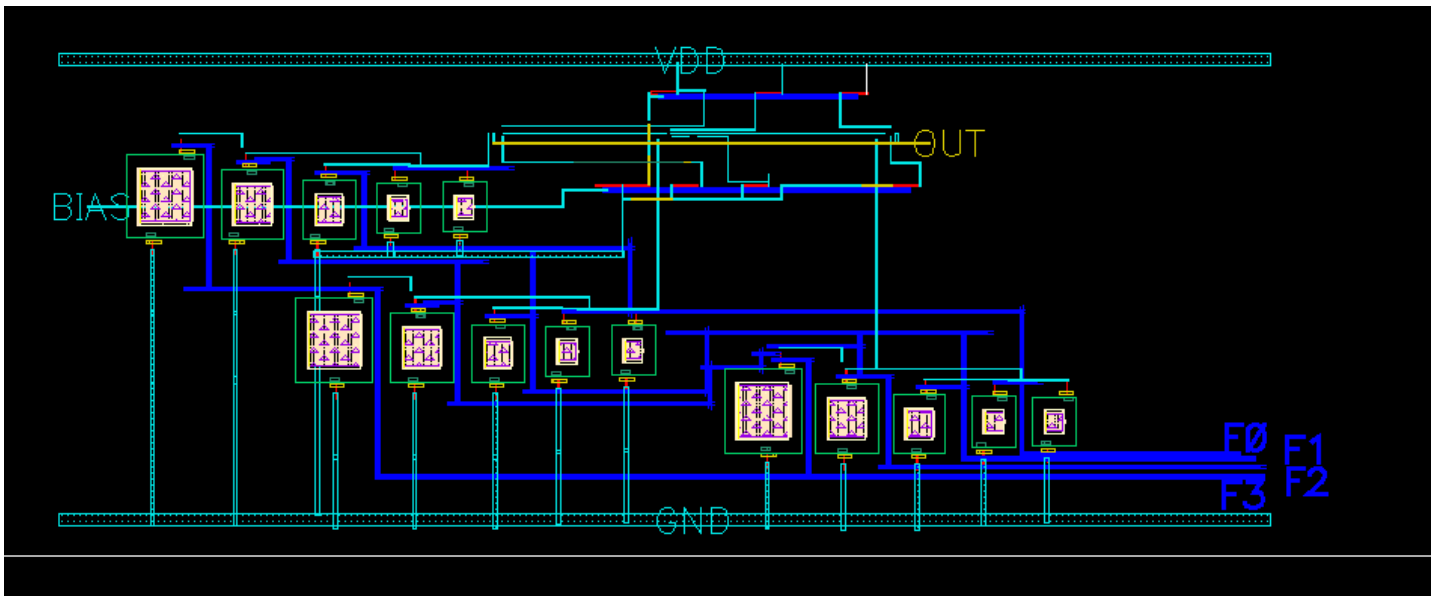


Figure 2-37 DCO layout

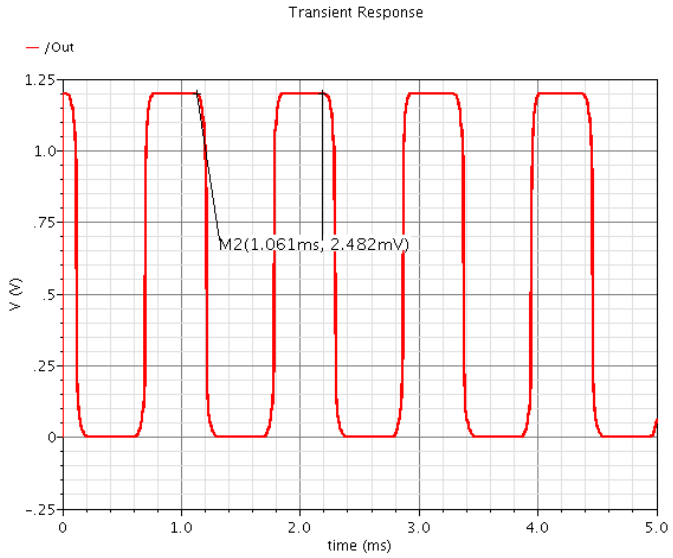


Figure 2-38 Post-layout result for DCO output for 0000 digital input

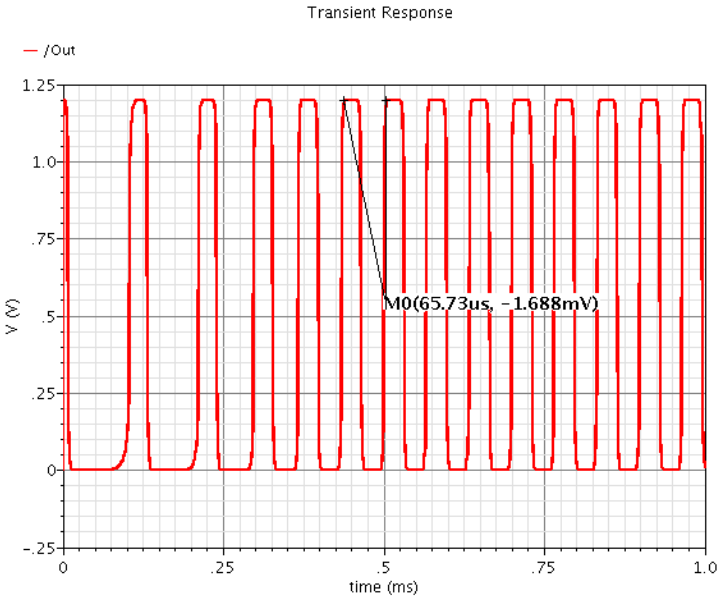


Figure 2-39 DCO output for 1111 input

CHAPTER 3. OUTPUT REGULATION LOOP

This chapter discusses the design of the ultra-low power output regulation loop that is used to regulate the output voltage of the IC since the output of the MPPT stage is not regulated. it demonstrates harvesting with acceptable efficiency (~ 65%) starting from 210 mV input sources. Design of the system used as output regulation loop and each block used in it are presented along with its layout and post-layout simulation results.

3.1 Problem Statement

The challenge is to design an ultra-low power output regulation system that regulates the output voltage at 1.2 V over wide input voltage range (output from MPPT block) and wide load current range with acceptable efficiencies and acceptable voltage ripples.

3.2 DC-DC Conversion Topologies

This section shows different dc-dc conversion topologies and different control techniques used to regulate the output at certain desired output voltage. The advantage and disadvantages of each topology are discussed and based on this the architecture used in the output regulation block is decided according to the requirement discussed in the problem statement.

To regulate the output, a voltage regulator is needed. A voltage regulator is an electronic device that produces a steady and fixed output voltage, independently of its input voltage and output current. In reality, any voltage regulator has a range of input voltages for which

it works, a certain level of efficiency and a limited amount of power it can handle. Therefore, a careful selection of the voltage regulator must be made depending on the application it is for [14].

As shown in Figure 3-1, a voltage regulator consists of a power processor, a controller, and a voltage reference. The input power coming from the supply is converted by the power processor and provided to the load [15]. It consists of power electronic devices like MOSFETs, BJTs, Diodes, ... etc. In order to keep the output at a certain set point, the feedback loop compares the output voltage of the power processor with a reference voltage value, and acts on the power processor so that the error between the two are minimized. Voltage regulators can be roughly divided in two categories: linear regulators and switching regulators. While linear regulators dissipate power when dropping the voltage

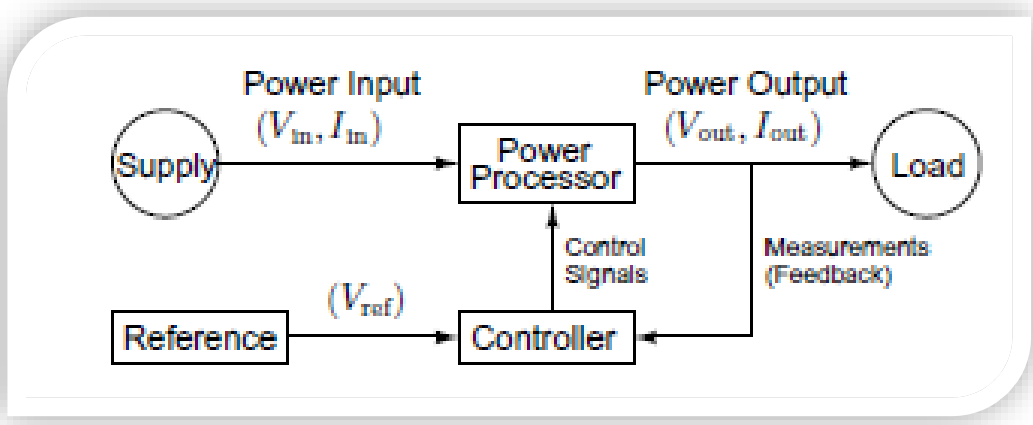


Figure 3-1: Block diagram of a typical electronic power conversion system.

level, switching regulators transfer almost all energy from input to output. We'll discuss each of them and show their pros and cons. Then choose from them the better match for the requirements.

3.2.1 Linear Voltage Regulators

To understand how linear regulators work, imagine that the output voltage is the level of water in a tank and the output current is a leakage. To maintain the level in the tank, the same flux of water must enter the tank as the one that is leaking. To control the influx, we have two options: either strangle the influx to match the leakage or divert any influx that may be exceeding the leakage to another path.

Similarly, linear regulators can work in two ways. The circuit shown in Fig. 3-2 shows the concept of a linear regulator, where RL is the load resistance. The equation that model this circuit is:

$$\mathrm{V_{out}} = \mathrm{V_{in}} - R_s(I_l + I_z)$$

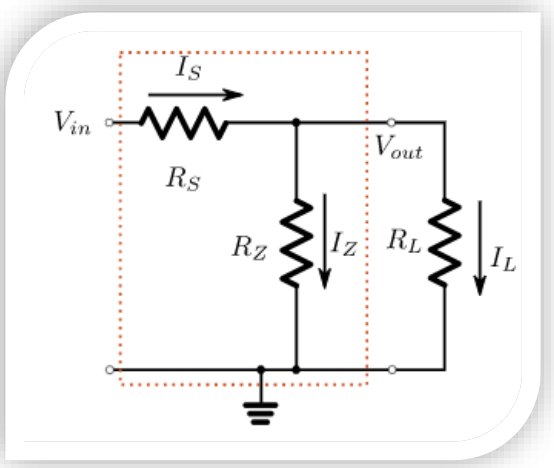


Figure 3-2: Linear regulator core

The variables the regulator does not control are Vin and I_l. So, V_{out} can be regulated at the desired value regardless of Vin and I_l by varying either R_s or by varying I_z (can be varied by varying R_z). Therefore, it can either "strangle the input current" (change R_s) or

divert any extra current from the input current to ground (change I_z) to keep V_{out} always at the same value. The regulators that have R_s as a variable resistance, which is in series with the load are called series regulators, while the ones that fix R_s but create a shunt through I_z are called shunt regulators.

Let's consider the case of series linear regulator. A series regulator controls the voltage drop between input and output nodes by actively controlling the value of the series resistance as shown in Figure 3-3.

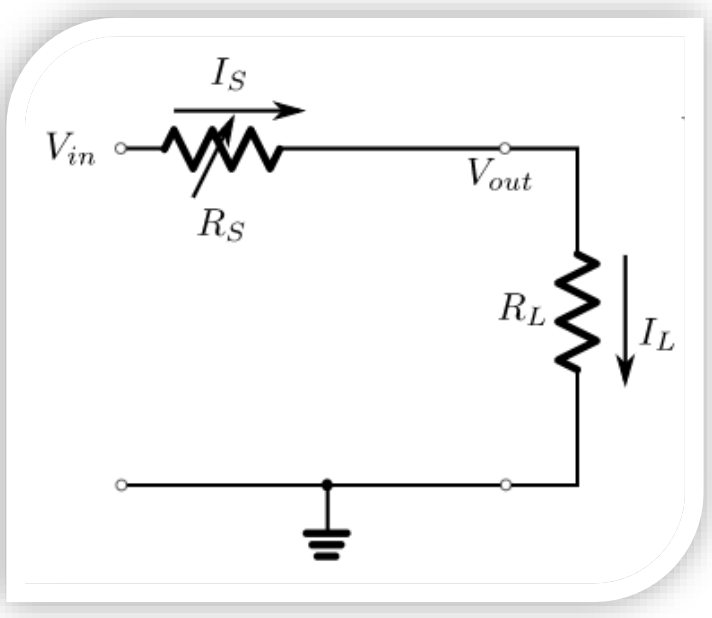


Figure 3-3: Linear series regulator

An active device such as a Bipolar Junction Transistor or Field Effect Transistor (MOSFET) is used as a variable series resistor. The details vary for different implementations, but it boils down to this: the output is compared with a voltage reference by means of error amplifier and the series resistance is changed in a way that the voltage

drop maintains the output voltage close to that voltage reference as shown in Fig 3-4. This Figure shows a special type of series linear regulator called Low-Dropout Regulator. Low-dropout (LDO) regulators work in the same way as all linear voltage regulators. The main difference between LDO and non-LDO regulators is their schematic topology. Instead of an emitter follower topology, low-dropout regulators use open collector or open drain topology. In this topology, the transistor may be easily driven into saturation with the voltages available to the regulator. This allows the voltage drop from the unregulated voltage to the regulated voltage to be as low as the saturation voltage across the transistor [16].

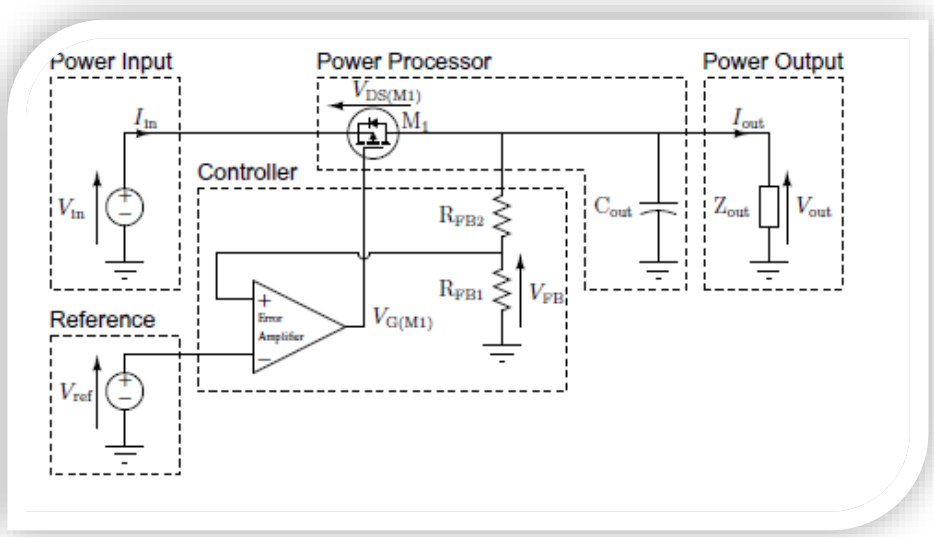


Figure 3-4: Block diagram of a typical LDO using a PMOS

As shown in the figure, it is constituted of a pass-device (power transistor M1), a voltage reference (V_{ref}) and an error amplifier with a voltage divider composed of R_{FB1} and R_{FB2} used to sense the output voltage. The capacitor C_{out} is used for adjusting the stability in the loop compensation. The power PMOS M1 acts as an adjustable resistor. The error

amplifier adjusts the gate voltage $V_G(M1)$ so that the voltage drop $V_{DS}(M1)$ across the power transistor M1 gives the desired output voltage value V_{out}. The regulated voltage value is controlled by the gain of the resistive feedback loop. The error amplifier tends to equalize the voltage at its inputs, and therefore, the load voltage V_{out} is given by eq (3.1)

$$V_{out} = V_{ref} . \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \qquad (3.1)$$

Regardless the current drawn by the control loop (Quiescent current), all current from the source flows to the load.

$$\therefore I_{out} \approx I_{in}$$

Hence, the efficiency is only defined by the ratio of voltages as show in eq (3.2).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} . I_{out}}{V_{in} . I_{in}} \approx \frac{V_{out}}{V_{in}} \qquad (3.2)$$

So, the power is lost mainly in the series resistance and is calculated by eq (3.3)

$$P_{loss} = P_{in} - P_{out} = (V_{in} - V_{out}) . I_{out} \qquad (3.3)$$

That's the main disadvantage of linear regulators, the difference between V_{in} and V_{out} lead to power loss. As this difference increases, power loss increases which lead to lower efficiency. So, their efficiency is poor, which means the power dissipated is generally high. This has a negative consequence on the circuit size, because huge heatsinks are mandatory. While their main advantage is that they offer very low output ripple to the load. Therefore, they are well suited to supply noise sensitive circuits. Also, they are cheap and easy to use.

Linear regulators provide excellent line and load regulation, and react very fast to transient load and line changes. Since they are non-switching regulators, they do not emit electromagnetic interferences (EMI).

3.2.2 Switching Voltage Regulators

Switching regulators generally use an oscillator for generating a clock signal, active elements as switches, and reactive passive elements (like capacitive and magnetic devices) for storing the energy to convert. If the switching elements are considered without their parasitics, the efficiency of switching converters can theoretically reach 100%. Practically, unlike linear regulators in which the pass-device is used as an adjustable resistor, in switching converters only the parasitics lower the power conversion efficiency.

There is a main type of switching regulators which is the DC-DC converter using both capacitive and magnetic passive devices, in combination with active switching devices. The capacitive devices are integrated or discrete capacitors, while the magnetic devices are generally discrete power inductors or power transformers. Different active devices are used to design such converters, depending on the application's needs. These devices are mostly transistors, diodes and thyristors.

The basic circuits used to design DC-DC converters consist of three main topologies, which are the step-down topologies, the step-up topologies, and the topologies able to perform both step-up and step-down conversion. The step-down topologies are only able to provide an output voltage lower than the input voltage, while the step-up topologies are only able to provide an output voltage higher than the input voltage. The combination of a step-up

and a step-down topology enables both voltage reduction and voltage increase with a single switching converter.

The energy storage devices (i.e., capacitors, inductors or transformers) are the heart of any switching-mode power supply. Switching regulators use inductors which are usually wound on toroidal cores, often made of ferrite or powdered iron core with distributed air-gap to minimize core losses at high frequencies.

Since we're concerned with low input voltages, we use the step-down topology which is called Boost converter and it was discussed in section 2.1.3.

Generally, DC-DC converters could be synchronous or asynchronous. Asynchronous DC-

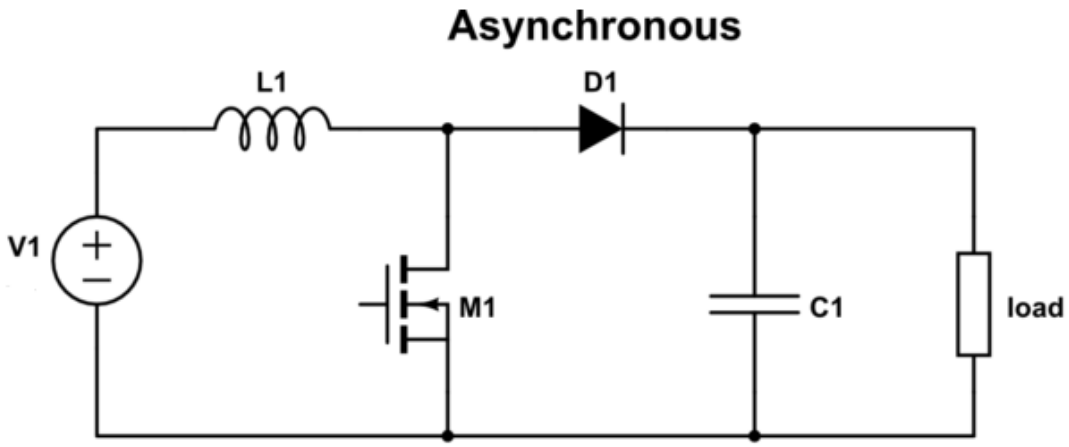


Figure 3-5: Asynchronous Boost Converter

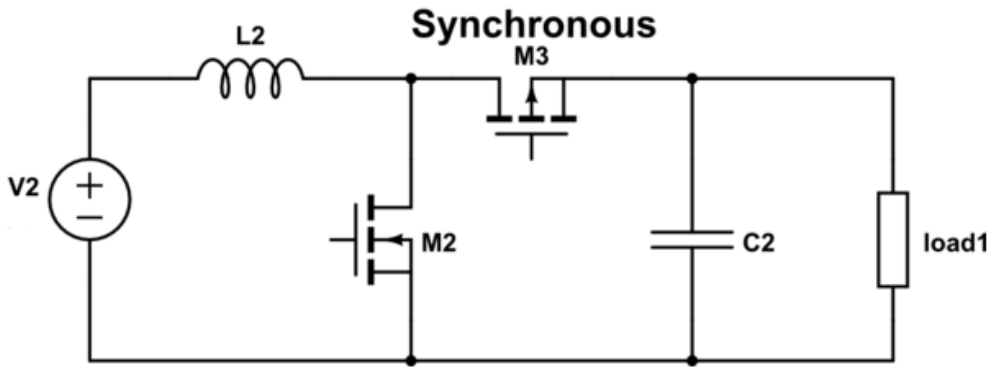


Figure 3-6: Synchronous Boost Converter

DC converters use a MOS switch and a DIODE as shown in Figure 3-5. While Synchronous DC-DC converters use an NMOS switch and a PMOS switch, they don't use a DIODE as shown in Figure 3-6. Synchronous topology refers to the practice of using an active element such as a MOSFET switched at the appropriate instants in place of a diode. In the synchronous case it's important that the two MOS switches are never both turned on at the same time, as this would short the capacitor to ground, possibly damaging the transistors, and severely decreasing efficiency. The advantage of the synchronous topology over the asynchronous is that the conduction losses through a MOSFET (M3) may be less than that through a diode (D1). However, Synchronous topology has a disadvantage that care has to be taken to ensure both MOSFETs are not turned on at the same time. Ensuring this does not occur requires more complexity for the driver circuit and more cost. So, using asynchronous topology, the IC tends to be smaller, relatively inexpensive and quite effective at low power levels since the conduction losses are low. So, in case of low power and low load currents its better to use asynchronous topology since in this case it's more important to decrease the current consumption of the driver circuit.

In a switching converter, the controller pilots the power devices, and therefore acts directly on the power conversion efficiency. Several tasks are accomplished by the controller. One of them consists of protecting the power devices against destructive effects (e.g., overcurrent, temperature overstress) by monitoring the currents, the voltages, and the temperature. However, its main role is to regulate the output voltage V_{out} to the desired voltage value. To do this, the controller can be designed to use different operation control methods, each of them adapted to a specific case. Among the operation control methods there are mainly two different modulations that are used in today's DC-DC converters, each optimized for a specific load condition. The first is the pulse-width modulation (PWM) operation control method, which is well suited for high power conversions. The second is the pulse-frequency modulation (PFM) operation control method, which is better suited for low power conversions. By combining both of these operation control methods into one controller, the converter can be made very efficient over a wide range of output power.

The Pulse-width modulation control is illustrated in Figure 3-7. The Figure shows the analog signal waveform V_{osc} of the sawtooth oscillator switching between the voltages V_1 and V_2. It also shows the error amplifier output voltage V_{EA}, and the digital PWM signal waveform V_G(M1) of the power transistor gate driver, which commands the MOS transistor M1 .The regulation of output voltage is achieved by varying the duty cycle D of the switching devices which changes according to the error signal V_{EA}, while keeping the frequency of operation constant. An advantage of PWM control is that because the

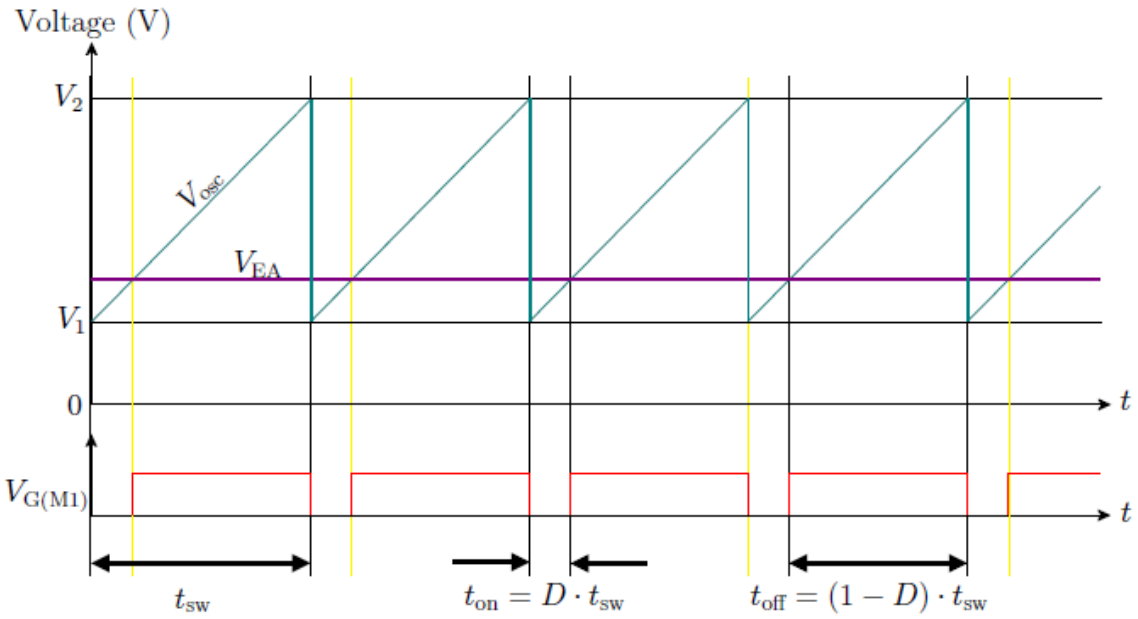


Figure 3-7: Steady-state timing diagram of a PWM switching converter

frequency is fixed, any switching noise that arises can be predicted, thus facilitating the filtering process. A drawback of the method is that also due to constant frequency, the switching losses (e.g., the losses due to the charging/discharging of the gate and output capacitances of the power transistors) are independent of the load current. Consequently, the self-consuming current does not change. As a result, at times of light loads the PWM becomes inefficient because the switching losses dominate the conduction losses, which are load dependent.

To overcome the dramatic efficiency reduction in lightly loaded PWM converters, an additional operation control scheme called pulse-frequency modulation (PFM) has been developed. PFM is a nonlinear operation scheme in which pulse trains are applied to the energizing switch to maintain the output voltage at the desired voltage value. This mode lowers the frequency of the switching-cycle events at light loads, therefore lowering the

switching losses, which are dominant to the conduction losses at light output loads. On the positive side, PFM control has become prevalent in battery-operated equipment due to its light-load efficiency exceeds that of PWM. On the negative side, because the frequency varies, the noise associated with the switching remains indefinite, making the filtering process difficult to control and the noise difficult to remove.

There are several PFM operation schemes, such as single-pulse PFM, multi-pulse PFM, and burst-mode PFM. However, all operate according to the basic principle of initiating switching cycles only as needed to maintain the output voltage. Figure 3-8 shows the waveforms produced by a burst-mode PFM controller. The pulse trains represent the PFM operation control. When the current requested by the load decreases, the idle time increases, and therefore the frequency also decreases.

Figure 3-9 illustrates the efficiency characteristics of PWM and PFM. As shown, PFM shows good efficiency over wider range of load current.

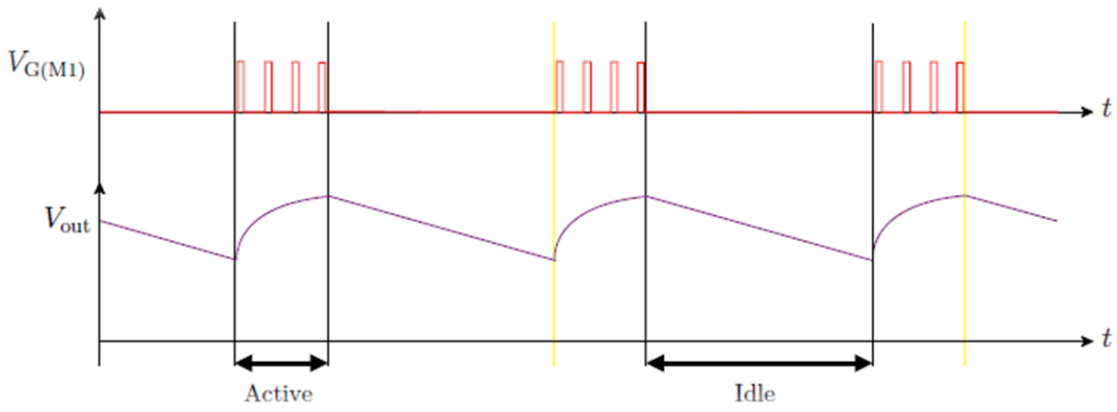


Figure 3-8: Signal waveforms of the PFM operation control in steady-state.

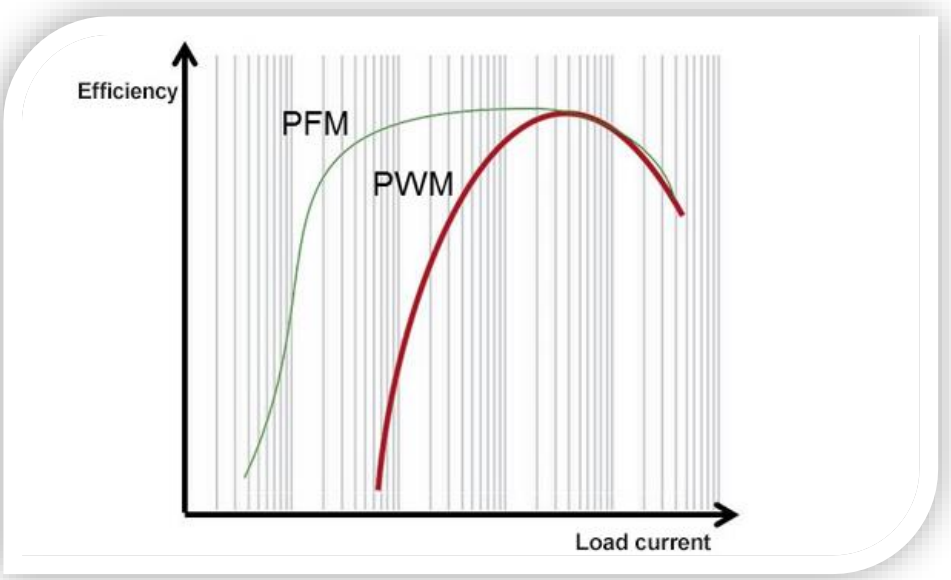


Figure 3-9: Efficiency characteristics of PWM and PFM illustrated

Since we are dealing with low power system and since we want to achieve high efficiency at light load, the designed output regulation loop uses the PFM operation control.

3.3 System Design and circuit description

Fig. 3-10 shows the functional block diagram of the system used for output regulation using a one stage PFM boost regulators to generate 1.2 V output from a low input voltage starting from 210 mV. As mentioned before in section 3.2.2, The primary advantages of the PFM over PWM are the reduction of the self-bias loss, especially during low load operations, and simpler analog control blocks. While the PWM mode converter keeps switching at all load conditions, the PFM mode skips pulses during low load conditions so the PFM topology becomes more efficient than the PWM topology in light-load conditions that this design is targeted for. In terms of transient response, the PFM produces first-order RC

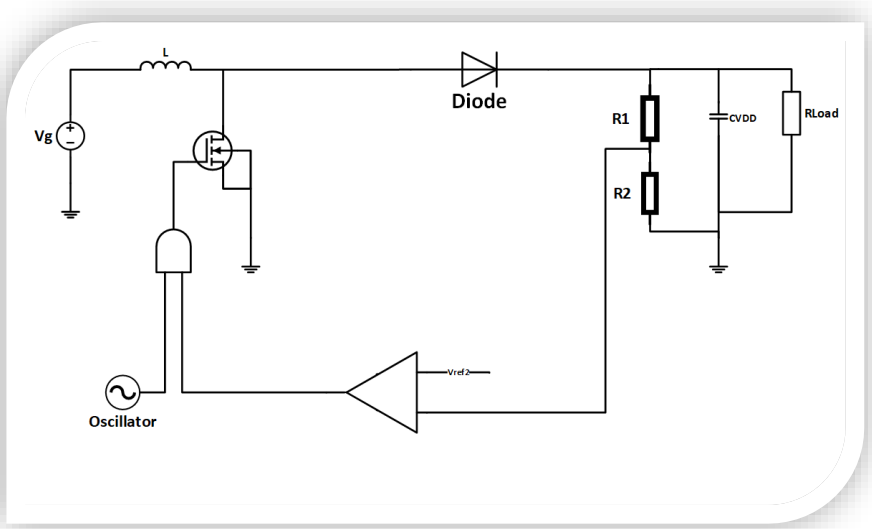


Figure 3-10: Block diagram of output regulation loop

waveform while PWM generally has second or third-order response depending on the design of the compensation network. Consequently, the design of the PFM control is much simpler allowing lower power operation of the boost converter; however, the PWM designs' transient responses are usually faster (achieved through polo-zero compensation and other aided feedforward techniques) than those of the PFM designs.

This output regulation stage is designed using asynchronous topology using an external Schottky Diode. The architecture is motivated by the current drive of this stage. And the conduction loss is less critical in this stage as it drives less current. As the asynchronous topology eliminates the PMOS switch, the switching loss (less gate drive) and bias current

(simpler control circuit) are reduced. So, asynchronous topology is used in the output regulation loop.

The boost regulator is designed to operate in DCM mode (analyzed in section 2.1.3) since it's more suitable for low power operation.

The two-stage boost regulators (one for the MPPT and the other for output regulation) increases the max possible conversion ration since the overall conversion ratio will be equal to the conversion ratio of the first stage multiplied by the conversion ratio of the second stage which leads to lower min acceptable input voltage [17].

The system design of the output regulation loop is similar to the system designed in [18] but with some modifications in the circuit design to lower the power consumption. And eliminating the current limit comparator since when designing the system for lower power the current was not overshooting that much.

The PFM boost regulator of this loop is designed with hysteresis mode voltage feedback mechanism (also known as bang-bang control). The feedback signal monitors the output voltage and compares it with the internally generated reference voltage. The output of the feedback comparator remains low when the VFB signal is higher than the VREF; a condition that happens when output is above the regulation level. In this condition, the MOS switch remains off and the output discharges under the given load condition. Once the decreasing output voltage crosses the regulation level, VFB signal falls below the VREF signal and the feedback comparators output becomes high. This allow the oscillator which produces pulse train to pass through the AND gate as long as the EN remains high (i.e., VFB remains lower than VREF). The integrated n-MOS transistor is turned on by the

positive edge of OSC and turned off by the negative edge of the OSC within OSCs single time period. The feedback comparator is designed with 15mV hysteresis on the upper side.

The conceptual waveforms of the converter with different input voltage and load current conditions are shown in Figure 3-11 and 3-12. Figure 3-11a shows a typical condition with load, $IL1$ and input voltage, $VIN1$, for which the converter is running at single pulse operation. At each switching event, given the input, the inductor current is increases to IPK $(= \frac{VIN1}{LIN}\ TON)$ and that produces an output voltage increase of $VRIPPLE$. The VRIPPLE being more than the VHYS, the feedback comparator turns off the switch (EN goes low), before starting the next pulse and forces the converter into idle mode. The no-switching mode is defined by the section of idle mode when the inductor current has reached zero

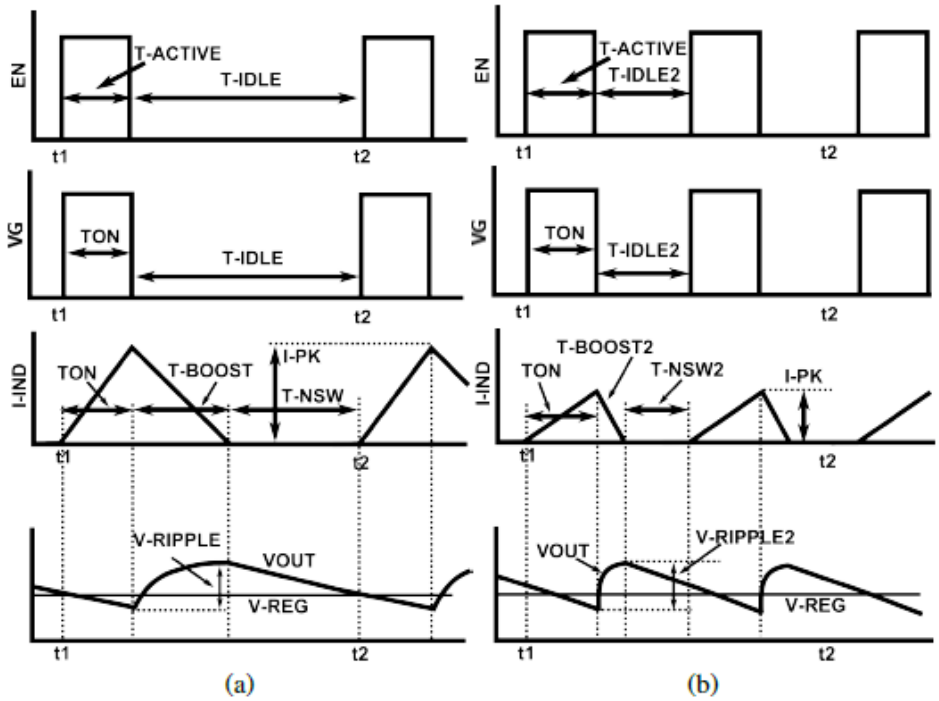


Figure 3-11: Conceptual waveform of the PFM mode converter. (a) Typical single pulse operation. (b) Single pulse operation with decreased input voltage as compared to situation shown in (a).

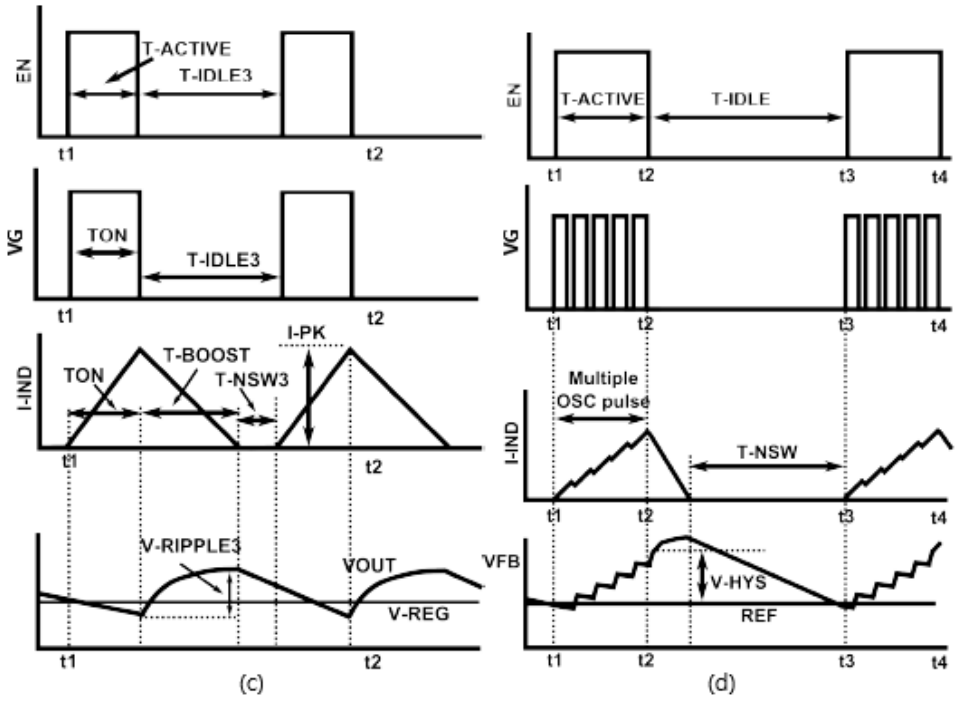


Figure 3-12: Multi pulse operation (a) Single pulse operation with increased load as compared to the condition shown in Fig. 3-11a. (b) Multi pulse operation, when the converters idle time is exhausted due to increased load or conversion ratio or for both

and output discharges under given load, IL1. The average of the inductor current during TBOOST period is equal to the load current IL1. Fig. 3-11b represents operation with decreased input voltage, VIN2 (VIN2<VIN1), as compared to Fig. 3-11a. The peak current is lower and the VRIPPLE decreases too. Consequently, the idle time is reduced and switching events happen more often, as shown in Fig. 3-11b. Fig 3-12a shows the operation with increased load as compared to Fig. 3-11a. The inductor peak current remains same as Fig. 3-11a, but to compensate for higher load current the converter reduces the idle time. Note that both with conversion ratio increment (input voltage decrease) and load current increment, the converter exhibits more frequent switching. In both cases load and input variation is compensated by modulating only the idle time. The converter switches to multi

pulse operation (Fig. 3-12b) at higher load as a single pulse cannot provide enough charge to recover the output. In multi pulse mode, for every active period, the oscillator is turned on for longer duration to allow multiple cycles. The inductor current builds up at every TON and decrease only a little during the TOFF (because TON to TOFF ratio is very high). At every successive pulse, output voltage continues to increase. Once the output voltage crosses the hysteresis value above the regulation level, the converter switches to idle mode. Note that unlike the single pulse operation, the ripple voltage in this condition is defined primarily by the hysteresis value, not by the inductor peak current. In practice, the ripple magnitude in this condition is little more than the hysteresis value, because after the converter switches to idle mode, the remaining inductor current charges the output voltage little more than the level where the decision was taken. On the contrary, the ripple magnitudes in the single pulse cases are defined by the value of the peak current, and can be much higher than the hysteresis value. The converter regulates its output voltage by modulating the frequency of the switching events. By controlling both the active and idle time, the feedback comparator (EN pulse) modulates the architectural duty cycle [TACTIVE/ (TACTIVE+TIDLE)] in response to changes in VIN and ILOAD. However, oscillator's self-duty cycle [TON/TOSC, where, TOSC is the period of the oscillator] remains constant under all input and load conditions. It is critical to have as high duty cycle as possible to achieve higher conversion ratio. A lower input voltage demands a smaller idle time (Fig. 3-11b) and the minimum idle time is the off period (TOFF=TOSC-TON) of the oscillator. Therefore, maximizing TON/TOSC helps reduce the minimum input voltage for operation. Further, note that variation in the duty cycle needs to be minimized (TOSC and TON can vary but the ratio needs to be constant) to ensure constant maximum

conversion ratio under voltage/temperature variation. In summary, oscillator with a high and well-controlled (voltage/temperature invariant) duty cycle is necessary for high conversion ratio PFM mode voltage regulator. This section shows the design of the feedback comparator and the design of a high duty cycle to enable boost operation from very low input voltage.

3.3.1 High Duty Cycle Current-starved Relaxation Oscillator

Oscillators can consume a significant fraction of the total power of a system, and often do not benefit directly from technology scaling. In light of these demands, there is a need for high performance oscillator designs which achieve optimal trade-offs between size, power efficiency and accuracy.

Crystal oscillators are the established leader in the kHz–MHz range and provide excellent frequency stability at the cost of larger physical size. In contrast, ring oscillators are area- and power-efficient but suffer when it comes to temperature stability. Relaxation oscillators offer an attractive compromise of these factors, with small size, zero start-up time, and low temperature dependence.

One recently introduced low-power oscillator topology is the current-mode relaxation oscillator [19]–[20], whose operation is illustrated in Figure 3.13. Transistors M0 and M1 are each biased with a current I_{ref} , while arranged as a source-coupled voltage comparator. One branch of I_{ref} flows through the resistor R_{ref} to generate a reference voltage V_{ref}, while a second matched current flows into capacitor C and slowly charges the voltage V_C. Initially, V_C is reset to ground, causing V_{Cmp} to be pulled low. Once V_C exceeds V_{ref}, M1

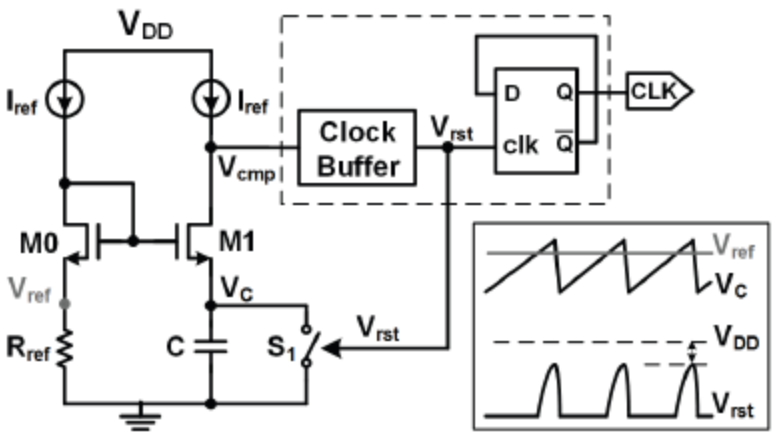


Figure 3-13: Single-phase current-mode relaxation oscillator and timing diagram

amplifies the voltage difference ($V_C - V_{ref}$) and V_{Cmp} rises, triggering a digital clock buffer to generate a pulse V_{rst} which in turn resets V_C. Unlike most voltage-mode relaxation oscillators, no additional comparator stage is required, thanks to the re-use of I_{ref} for both charging the capacitor and biasing the comparator.

Although it improves both power consumption and area, the existing current-mode relaxation oscillator has two important drawbacks. First, the duty cycle of V_{rst} is generally quite low, and dependent on delays in the comparator, digital buffer and capacitor reset, all of which are sensitive to temperature and process variations. A clock divider is usually needed to convert the narrow pulse V_{rst} to 50% duty cycle signal, halving the clock frequency and adding to the dynamic power consumption. Second, V_{rst} will generally not reach VDD, making the system vulnerable to noise and jitter. As shown in Fig. 3.13, both V_{Cmp} and V_C are reset to ground once V_{rst} is larger than the threshold voltage of switch S1. Thus, V_{rst} is usually pulled down before it reaches VDD. To address the above problems, we use a dual-phase current-mode relaxation oscillator proposed in [21].

Figure 3-14 shows the dual-phase current-mode relaxation oscillator M2–M4 are matched transistors. Two identical capacitors C1 and C2 are alternately charged by I_{ref} and reset to ground as dictated by the complementary output clocks φ and $\bar{\varphi}$, which are generated by a set-reset (SR) latch using current-starved logic.

The timing diagram of the dual-phase structure is also illustrated in Figure 3.14. When φ = 1 and $\bar{\varphi}$ = 0, V_{C2} and V_{cmpn} at the drain of M4 are reset to ground. The voltage on C1 is charged up with a slope of ($I_{ref}/C1$). Meanwhile, biased with I_{ref}, M3 compares V_{C1} with the reference voltage ($V_{ref} = I_{ref} . R_{ref}$) and provides an amplified difference V_{cmpp} to the SR latch. Once V_{cmpp} reaches the latch's threshold voltage, the SR latch changes its state to φ = 0 and $\bar{\varphi}$ = 1. In this state, there is no current flowing through M3 and C1, and I_{ref} biases M4 while charging C2. The oscillation period can be expressed as:

$$T = 2\left(\frac{V_{ref}}{\frac{I_{ref}}{C}} + \tau_{M3,4} + \tau_{SR}\right) = 2\left(\tau_{RC} + \tau_{cmp} + \tau_{SR}\right) \qquad (3.4)$$

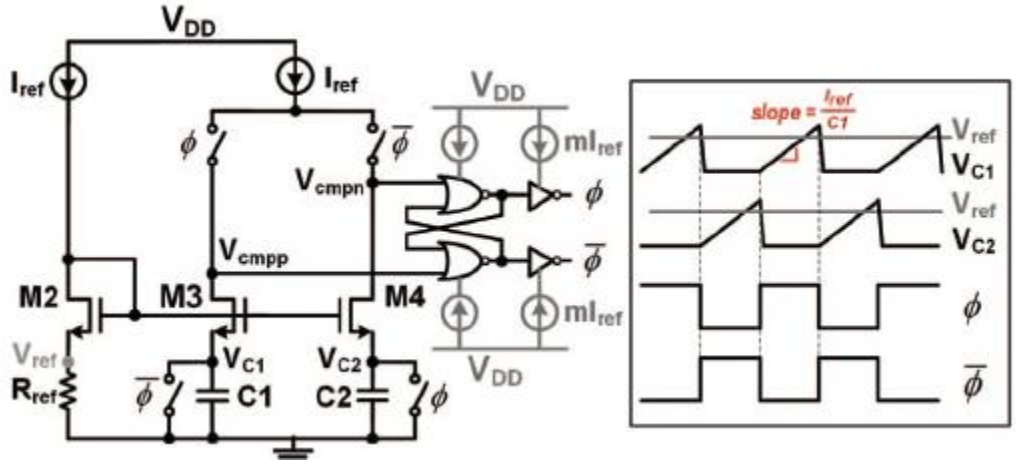


Figure 3-14: dual-phase current-mode relaxation oscillator and its timing diagram

where C1 = C2 = C, $\tau_{RC} = R_{ref}.C$, τ_{cmp} is the comparator delay caused by finite transistor gain and the parasitic capacitance at node $V_{cmpp,n}$ and τ_{SR} stands for the digital delay of SR latch.

Compared to the single-phase topology, the advantages of this proposed dual-phase structure are: (i) Since the two capacitors are charged separately at two half-cycles, the capacitor resetting delay does not add to the oscillation period, which improves the frequency accuracy. (ii) The clock outputs (φ and $\bar{\varphi}$) are square waveforms with a 50% duty cycle rather than a narrow pulse. Thus, a clock divider is not needed after the oscillation signal, which saves power. Also, the duty cycle can be increased by adjusting the ratio of C1:C2.

The dual phase oscillator is designed to have an oscillation frequency of 24 KHz and duty cycle of 70.2%. The simulation result of the oscillator is shown in Figure 3-15.

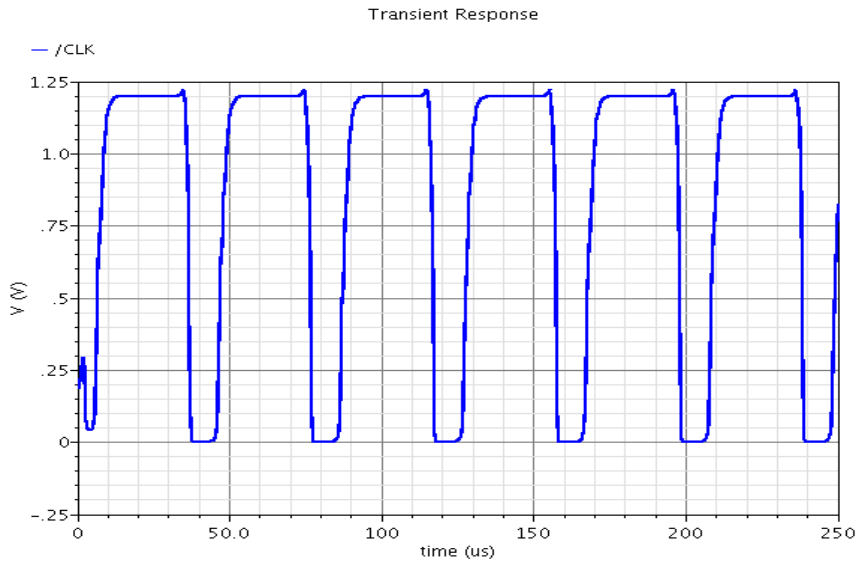


Figure 3-15: Transient response of the designed oscillator

The delay in the oscillator signal is due to the added current starving technique which is used to reduce the power dissipated by the SR latch.

The current consumption of the designed oscillator is ~140 nA.

3.3.2 Feedback comparator

Feedback comparator works as the core decision making circuitry for this hysteresis mode converter. Figure 3-16 shows the feedback comparator circuit used in the output regulation loop. The comparator circuit implementation is composed of a simple operational transconductance amplifier (OTA) stage followed by a matched inverter and finally a CMOS inverter. The matched inverter is used to make the comparator more balanced and the CMOS inverter generates the digital output level. The input differential pair has large area to reduce random offset and the load current mirror uses transistors with large length to reduce systematic offset. The hysteresis is implemented using M3 and M5 [17],[18]. Feedback voltage is sensed via the external resistive network and is compared with the

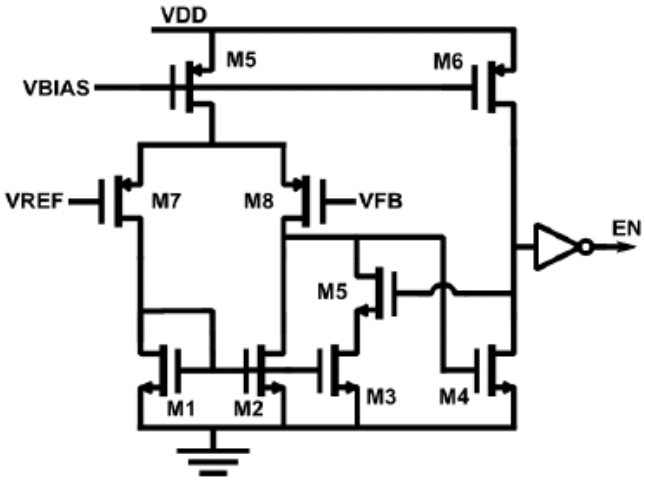


Figure 3-16: Feedback comparator circuit

internally generated reference, as shown in Fig. 3-16. The output of the comparator (EN) defines active ($V_{FB} < V_{REF}$) or idle ($V_{FB} > V_{REF}$) mode. The feedback circuit consumes < 30 nA of bias current. The design trade-off with such low bias current is the delay of the comparator response time. That is expected to result in a decrease of the regulated valley of the output voltage at different load conditions. The effect of delay is expected to be prominent at higher load condition [18]. The cascode free design allows very low operating voltage of the comparator.

Figure 3-17 show the AC simulation result of the feedback comparator.

3.3.3 System integration of the output regulation boost stage

After designing the boost regulator core, oscillator and the feedback comparator, a test bench is made as shown in Figure. 3-18 to simulate the output regulation loop at different values of V_{in} for a 6 $K\Omega$ load. The Schottky Diode is modelled using its SPICE model parameters from its datasheet.

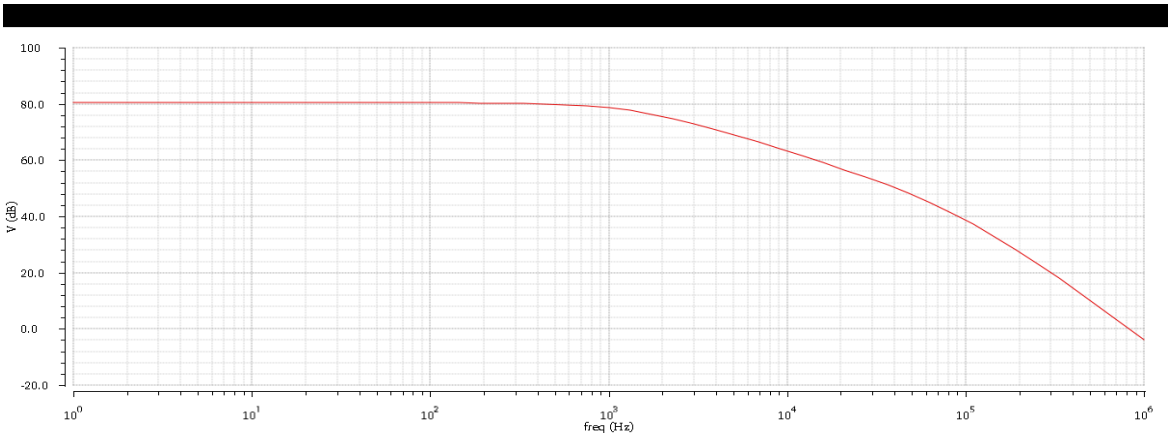


Figure 3-17: AC simulation of the Feedback Comparator

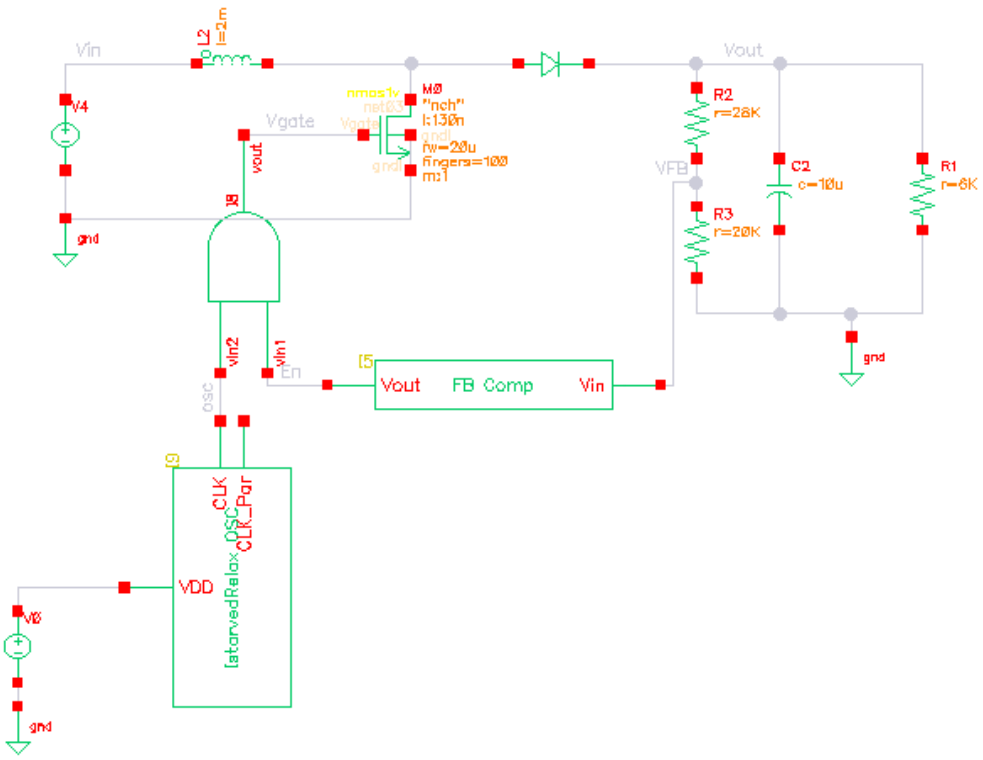


Figure 3-18: Test bench of output regulation loop

Figure 3-19 and 3-20 shows the simulation results of the output regulation stage when applying 200 mV at its input. The blue trace represents the output voltage V_{out}, the red one represents the inductor current, the purple one represents the gate voltage V_{gate} of the MOS switch, the orange one represents the enable signal En of the feedback comparator while the green one represents V_{FB}. From the simulation results at Vin = 200 mV we get 72% efficiency, 1.19 V output voltage and 1 mV output voltage ripples. As shown in Figure 3-19, the enable signal from the feedback comparator is always on since Vin is low.

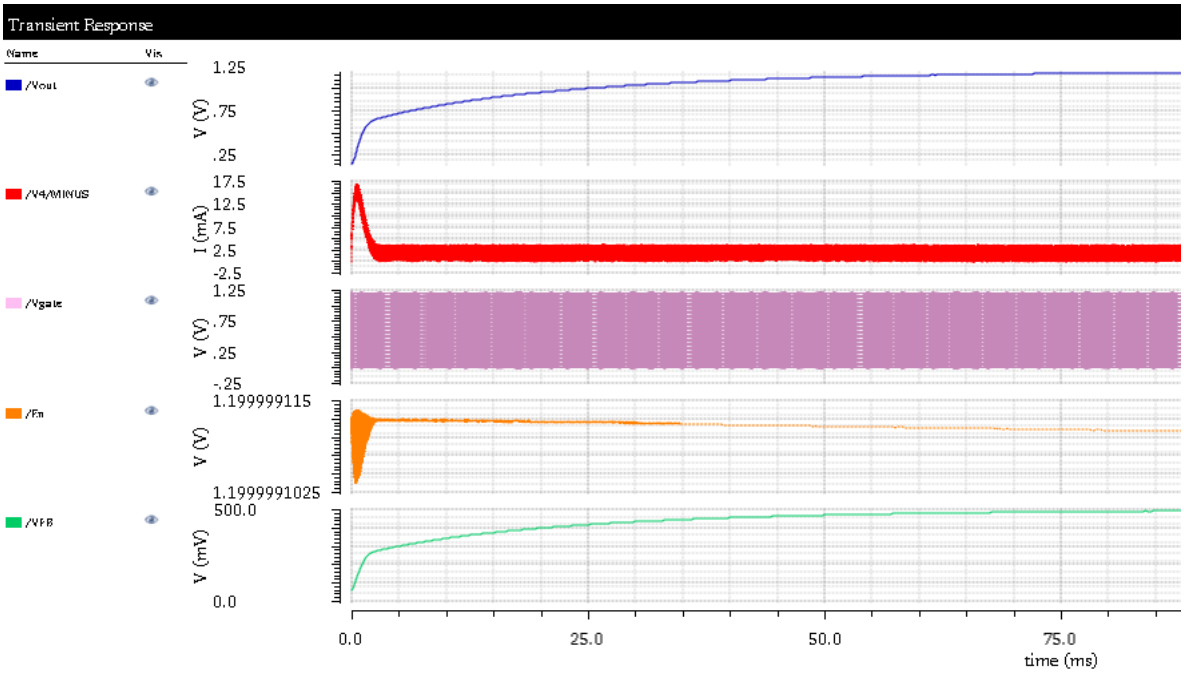


Figure 3-19: Simulation results of the output regulation stage at Vin = 200 mV

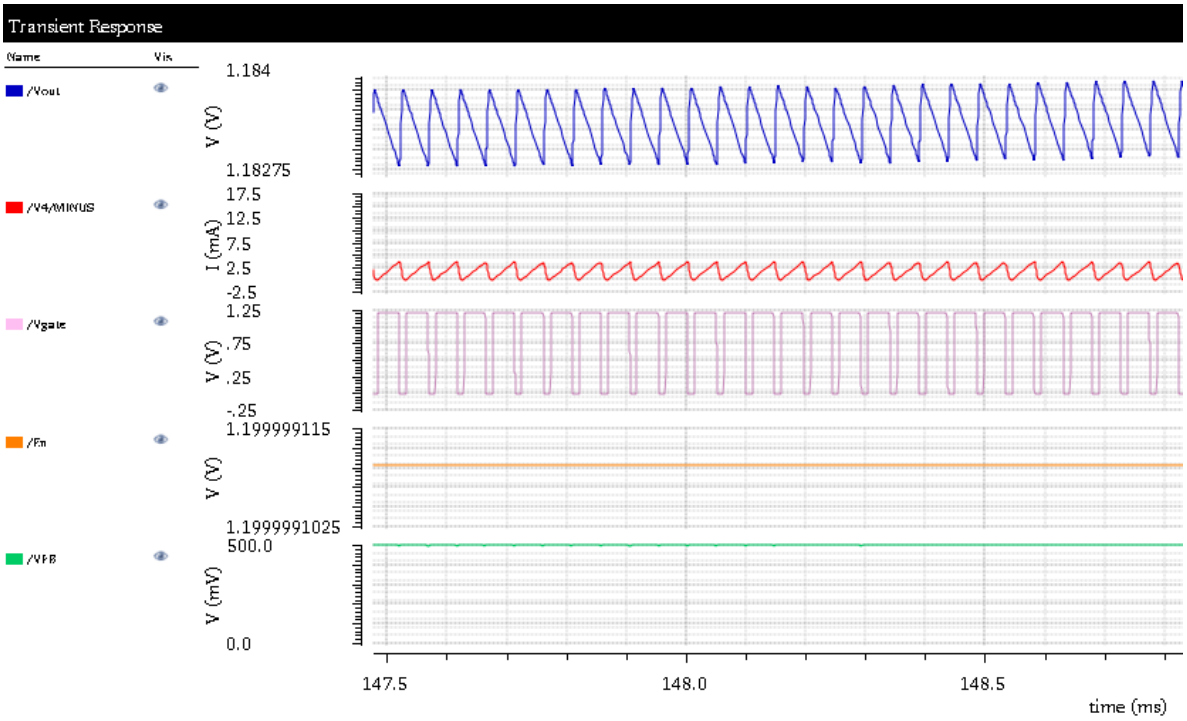


Figure 3-20: Magnifying the simulation results of the output regulation stage at Vin = 200 mV

Figure 3-21 and 3-22 shows the simulation results of the output regulation stage when applying 600 mV at its input. At $Vin = 600\,mV$ we get 68% efficiency, $1.2\,V$ output voltage and 15 mV output voltage ripples. As shown in Figure 3-21 and 3-22, the Enable signal is not high all the time, it is switching because Vin increased so in this case lower switching is needed for the PFM boost regulator. So, the enable goes low to skip some of the oscillator pulses which is equivalent to lower the switching frequency of the regulator.

Figure 3-23 and 3-24 shows the simulation results of the output regulation stage when applying 600 mV at its input. At Vin = 600 mV we get 65.4% efficiency, 1.2 V output voltage and 39 mV output voltage ripples. From Figure 3-24 its shown that starting from Vin = 900 mV the regulator starts to operate in the single-mode operation since the Vin is closer to 1.2 V (the desired output voltage).

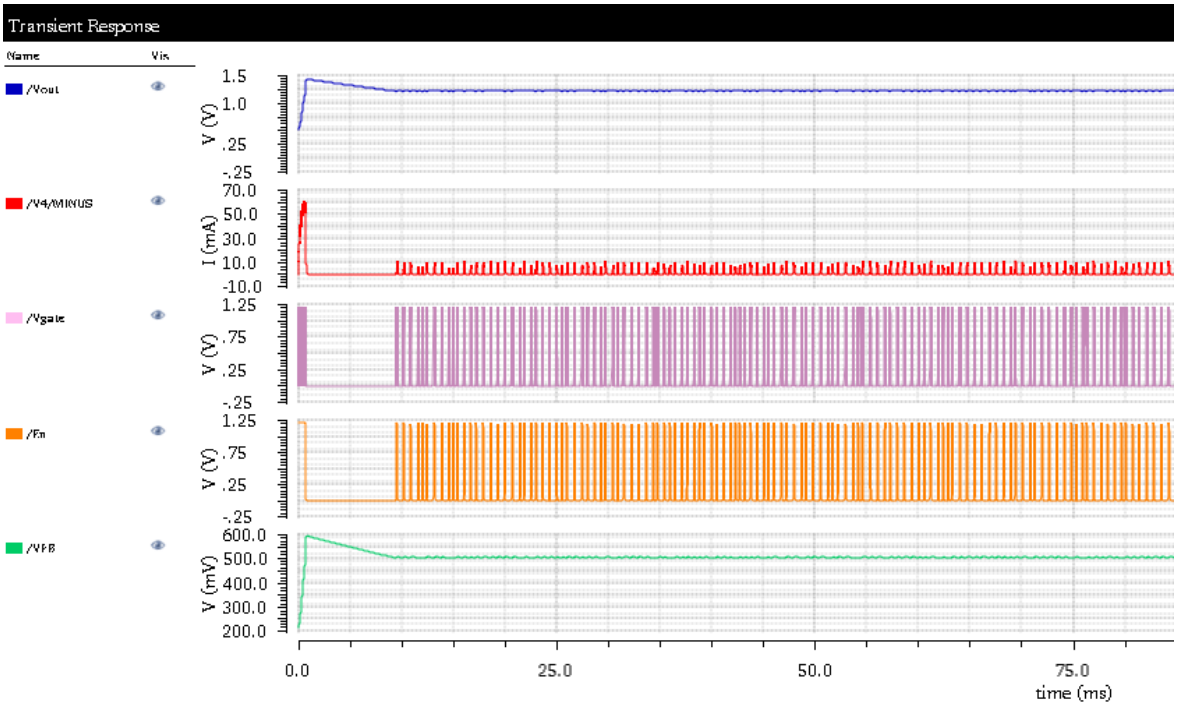


Figure 3-21: Simulation results of the output regulation stage at Vin = 600 mV

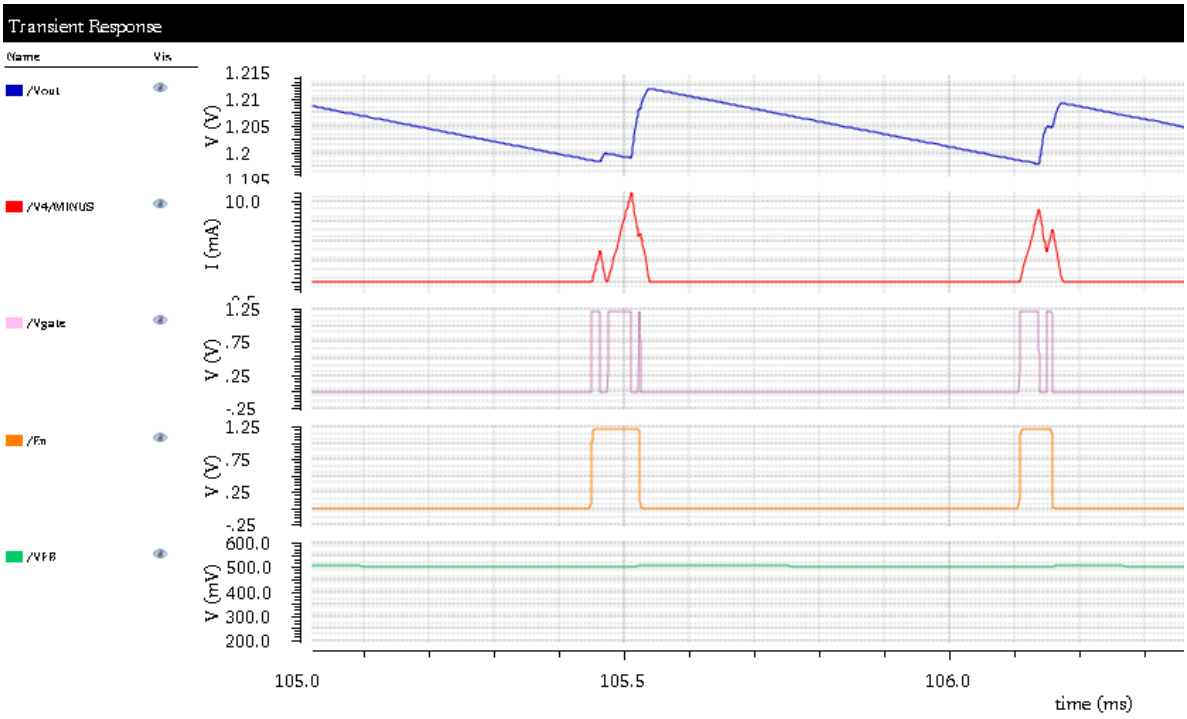


Figure 3-22: Magnifying the simulation results of the output regulation stage at Vin = 600 mV

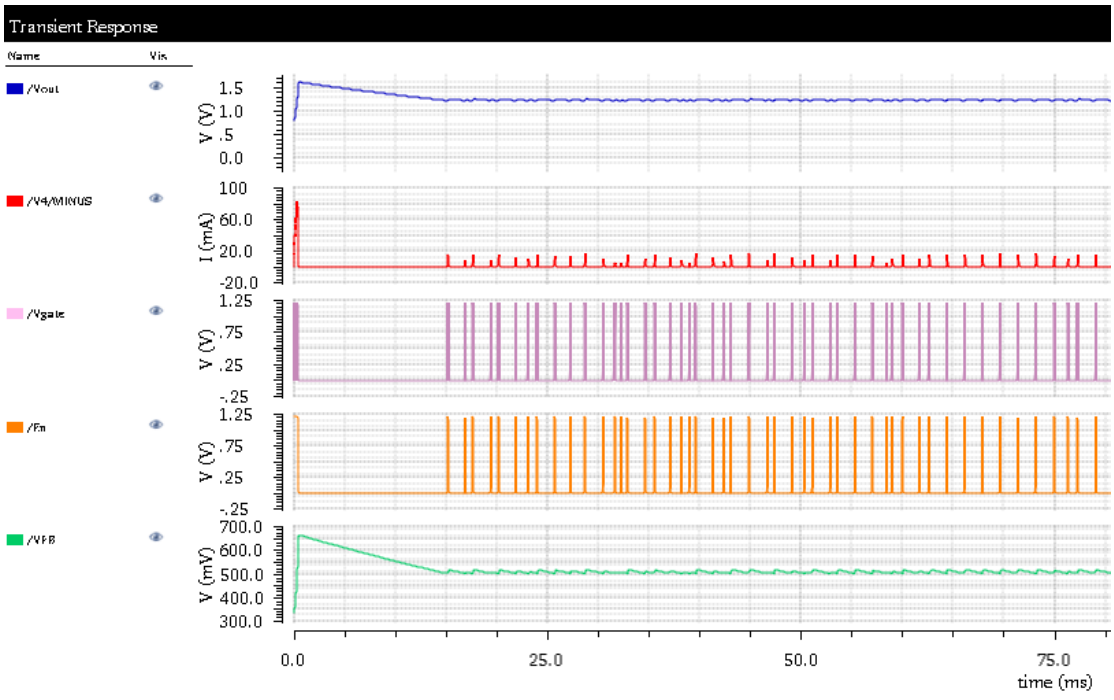


Figure 3-23: Simulation results of the output regulation stage at Vin = 900 mV

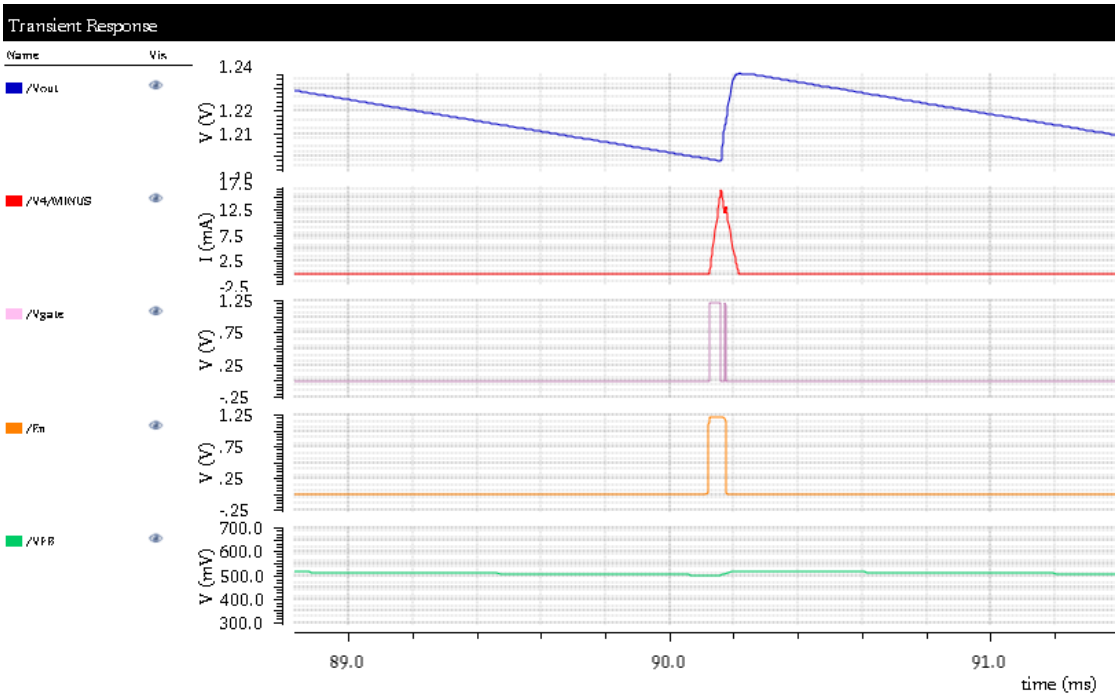


Figure 3-24: Magnifying the simulation results of the output regulation stage at Vin = 900 mV

3.4 Post-Layout Simulations

3.4.1 Post-Layout simulations of the oscillator

Show in Figure 3.3-16 is post-layout simulation of the current starved oscillator. The layout increased the delay of the oscillator. The post-layout simulations showed oscillation frequenc of 23.45 KHz, 70% duty cycle and current consumption of 136 nA

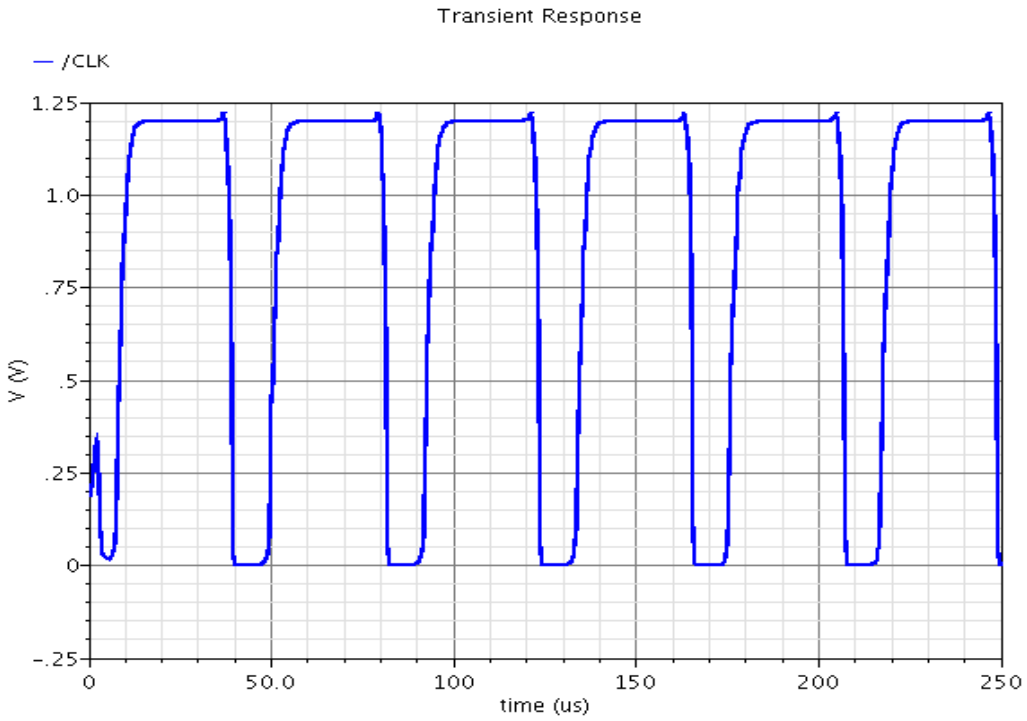


Figure 3-25: Post-layout simulations of the oscillator

CHAPTER 4. BANDGAP

4.1 Introduction

A bandgap voltage reference provides a voltage as precise as possible meaning that it must be immune to PVT variations where:

- **P:** manufacturing process variations
- **V:** supply voltage
- **T:** temperature

Semiconductor technology does not directly offer any electric quantity that is nominally independent of the ambient temperature. Thus, temperature independence has generally been envisioned in the form of combining two phenomena that have opposite temperature coefficients (TCs). for example: the negative TC can be obtained using a forward biased diode so BJT can be used as it is less sensitive to process variations than MOSFET transistors while the positive TC can be obtained by using two diode stacks biased a different current density as base emitter voltage of two transistors[25] as shown

in figure 4.1-1.

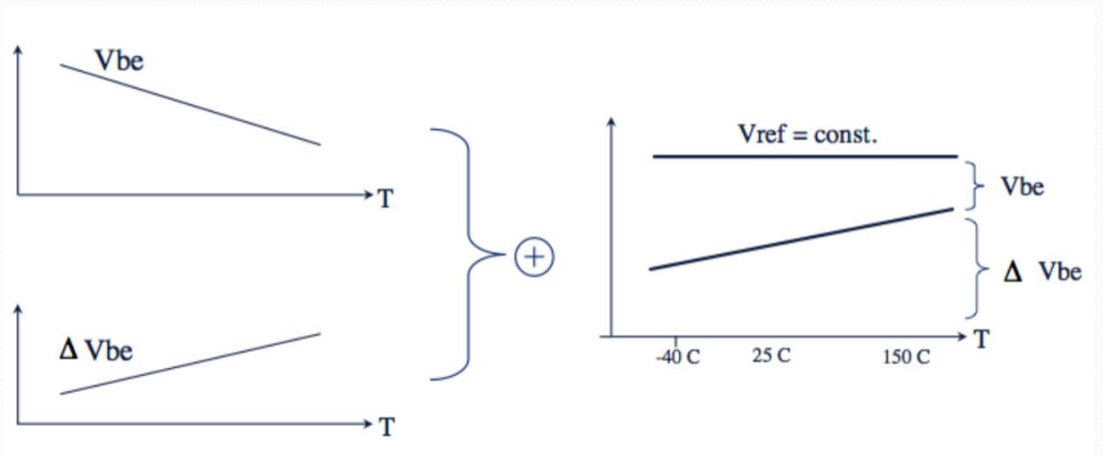


Figure 4-1 Temperature compensation using BJTS

The existing Voltage references can be roughly categorized as two types: one type related to the bandgap voltage of silicon or a fraction of it (i.e., sub-bandgap) using BJTs and resistors, the other one related to other factors such as MOS transistor threshold voltages and subthreshold parameters using MOS transistors (with or without resistors). Generally speaking, the bandgap or sub bandgap references show relatively small process variations than CMOS VRs with relatively high-power consumptions.

4.2 Proposed Design

A sub band gap was designed with a low temperature coefficient (TC) and high power supply ripple rejection (PSRR) using subthreshold MOS transistors, a single BJT and two resistors as shown in figure 4.2-1. The sub-BGR consists of a novel complementary to-absolute-temperature (CTAT) voltage generator based on a scaled emitter-base voltage of a BJT, and an improved proportional-to-absolute temperature (PTAT) voltage generator

based on stacking of _*V*GS of sub-*V*TH MOSFETs. The PTAT circuit achieves reduced power consumption without consuming a large chip area [24].

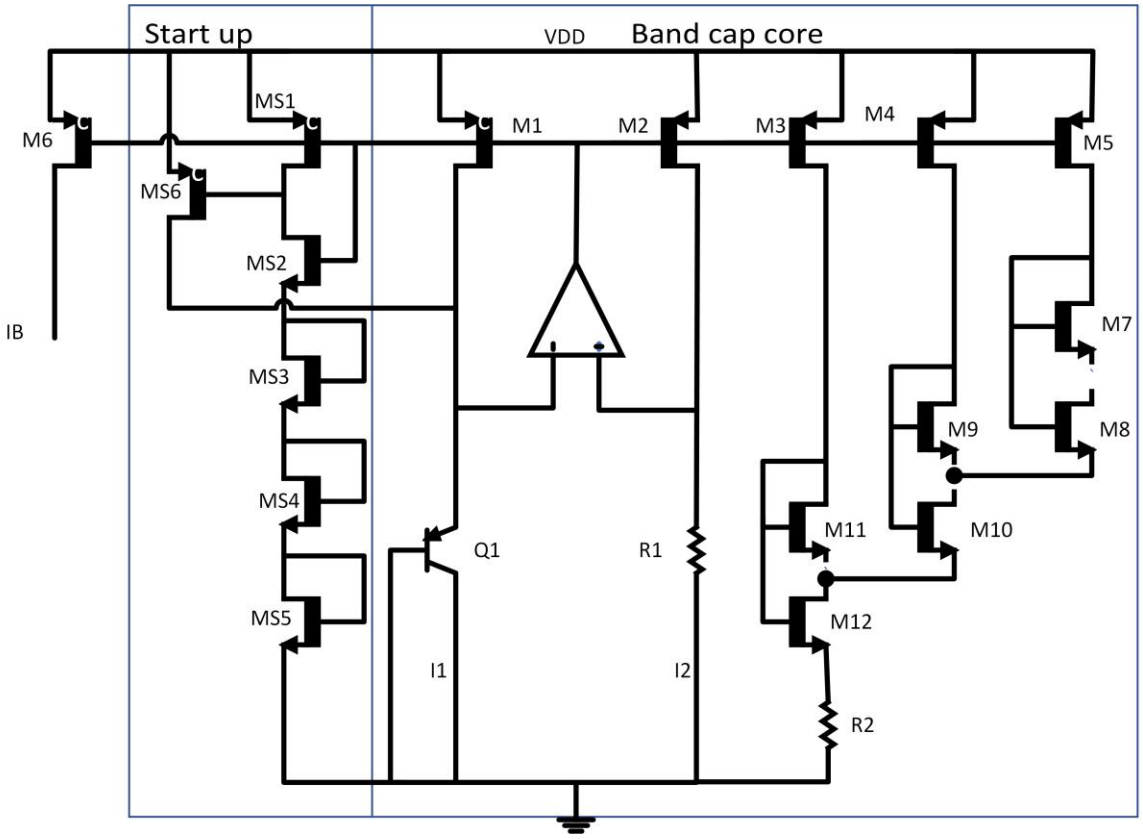


Figure 4-2 Bandgap core

4.3 Art of work for the circuitry of BG

4.3.1 Bandgap operation

The single parasitic vertical PNP BJT generates the CTAT voltage where:

$$V_{BE} = ln\left(\frac{IC}{IS}\right) \times V_T, \qquad where\ V_T = \frac{KT}{q} \rightarrow (4.1)$$

The operational amplifier OPA shown in Fig.4.3-1 enforces nodes A and B to have equal potential. To optimize the power and area, the current *IR* through *R1* is chosen to be three times of the current through Q1, and the resistance *R1* is about 17M.Transistors M1-5 act as current mirror and the size of M2 is three times of M1 and M3–M5. so that current through R2 is three times that through R1 this ratio can be used to decrease the CTAT of the circuit where:

$$V_{R_2} = \frac{R_2}{R_1} V_{EB} \rightarrow (4.2)$$

The PTAT voltage generator consists of transistors M7–M12 all which work in the subthreshold region. The subthreshold drain current *ID* of a MOSFET is an exponential function of its gate–source voltage *V*GS and drain–source voltage *V*DS. For *V*DS > 0.1 V, drain current *ID* is almost independent of *V*DS and is approximately given by:

$$I_D = \mu C ox\ (\eta - 1) V_T^2\ e^{\frac{(VGS - VTH)}{\eta VT}} \rightarrow (4.3)$$

where *K* is the aspect ratio (=*W*/*L*) of the transistor, μ is the carrier mobility, *C*OX is the gate-oxide capacitance, $V_T = \frac{KT}{q}$ is the thermal voltage, *kB* is the Boltzmann constant, *T* is the absolute temperature, and *q* is the elementary charge, *V*TH is the threshold voltage of the MOSFET, and η =1 + *Cd*/*C*ox is the subthreshold slope factor, respectively.

BY making V_{th} of M11 and M12 as similar as possible

$$V_{DS_{12}} = V_{GS_{12}} - V_{GS_{11}} = \eta VT ln\left(\frac{3K_{11}}{K_{12}}\right) \rightarrow (4.4)$$

$$V_{DS_{10}} = \eta V_T ln\left(\frac{2K_{10}}{K_9}\right) \rightarrow (4.5)$$

$$V_{DS_8} = \eta V_T ln\left(\frac{K_8}{K_7}\right) \rightarrow (4.6)$$

so, the output voltage reference is given by:

$$V_{refrence} = \frac{R_2}{R_1}\left[\eta V_T ln\left(\frac{6K_{11}K_9k_7}{K_{12}K_{10}k_8}\right)\frac{R_1}{R_2} + V_{EB}\right] \rightarrow (4.7)$$

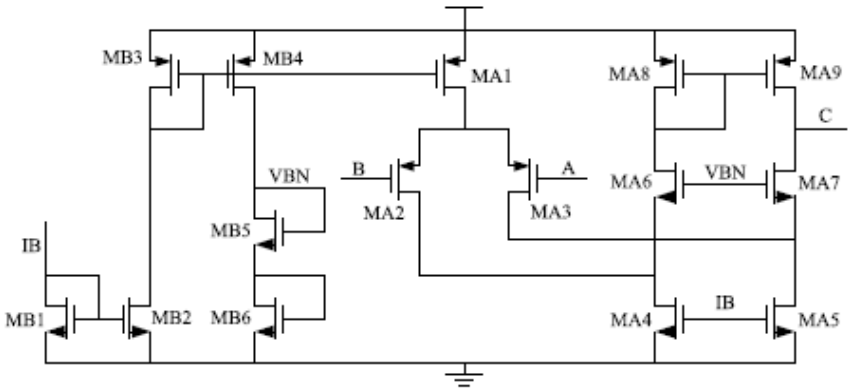


Figure 4-3 Schematic of OPA used in the proposed sub-BGR

4.3.2 Start-up problem of BG circuitry

Since there are two stable points one where I1=I2=zero and the circuit is off, and the second one where IR1=3*current passing through BJT. So, a startup circuit is used where MS6 becomes on making current move through the circuit which becomes on once more.

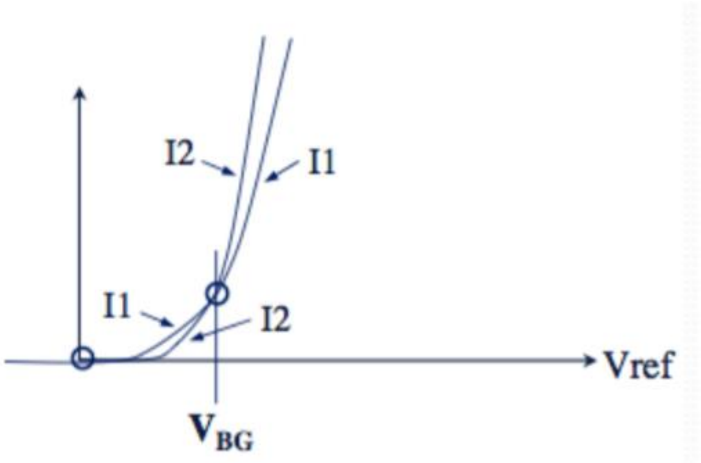


Figure 4-4 Startup problem of the BG

4.4 Results

4.4.1 Typical results

The output voltage=500mv to be used as a voltage reference in the next stages, the variations of the voltage across temperature from -40 to120 degree Celsius is ±3.5mv as shown in figure 4.4-1and 4.4-2.

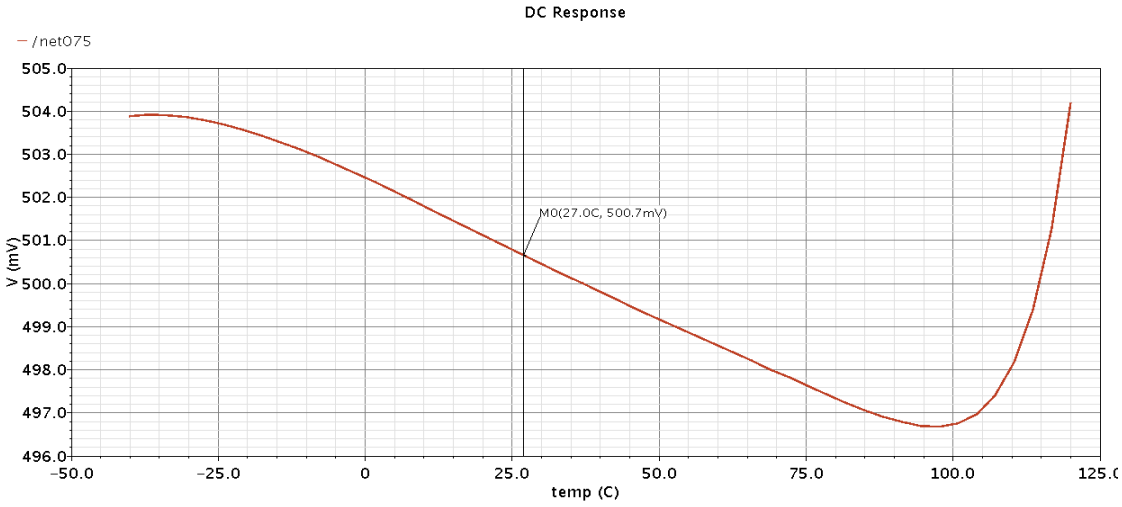


Figure 4-5 Voltage variation across temperature

The temperature coefficient of the voltage across this temperature range=

$$10^6 \times \frac{(V_{bg(max)} - V_{bg(min)})}{(T_{\max} - T_{\min}) \times V_{bg(nom)}} = 4.625 * \frac{10^{-5} v}{c} = 92.37 ppm/$$

where V_{bg} *is the output voltage of the bandgap.*

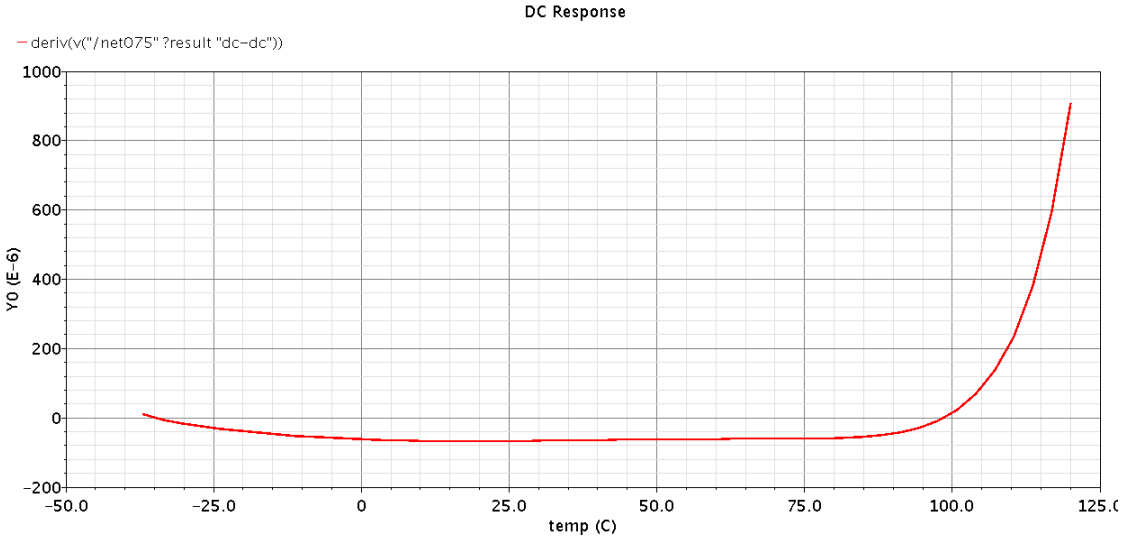


Figure 4-6 Voltage derivation across temperature

By decreasing IB supplied to the folded OPAMP so that the transistors enter subthreshold region the power consumption of the circuit do decrease approximately equals to 87.5nW.

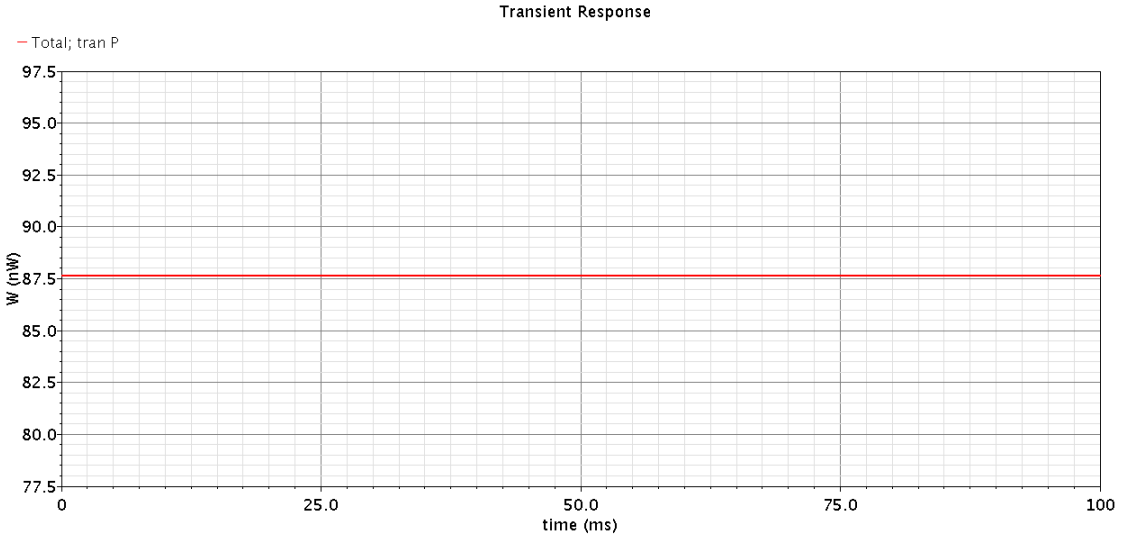


Figure 4-7 power consumption of the band gap

The power supply rejection ratio (PSRR): is defined to indicate the sensitivity of the Bandgap to VDD variations=$20\log\left(\frac{vref}{vdd}\right)$

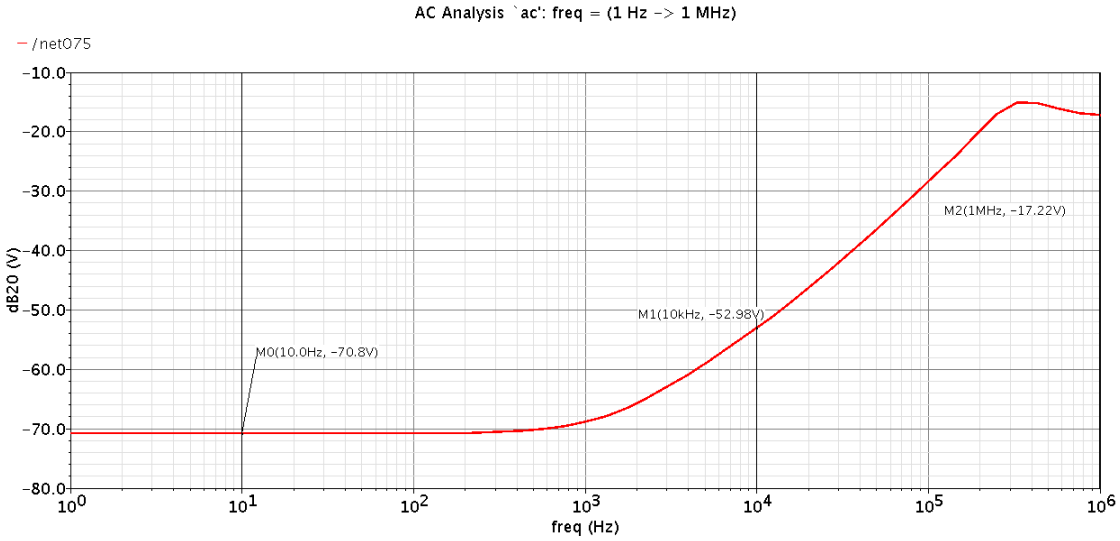


Figure 4-8 PSRR of the bandgap

The circuit is nearly immune to VDD variations within ±100mv with nominal=1.2v as shown in fig.4.4-5

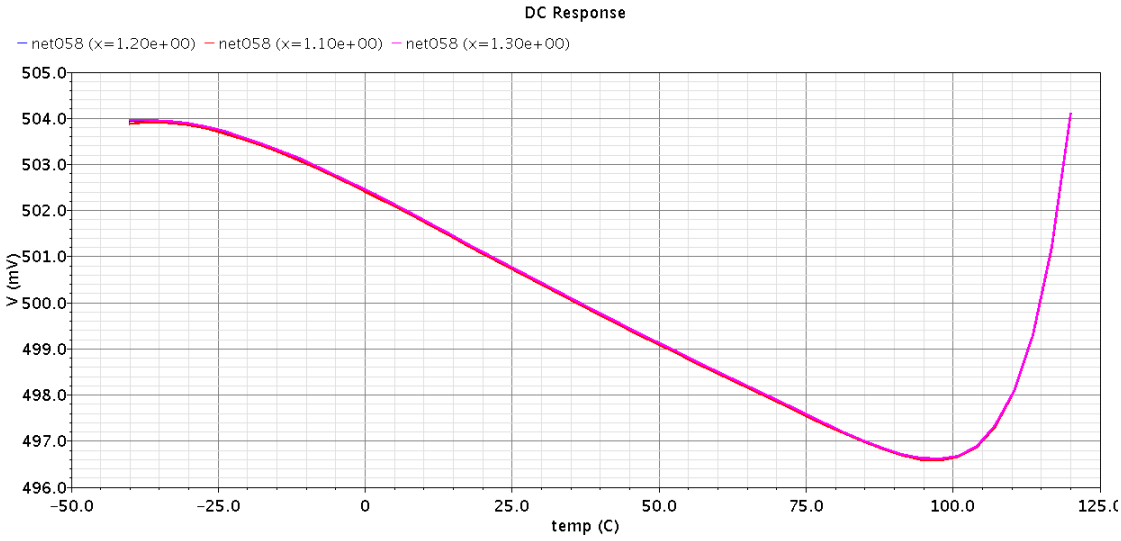


Figure 4-9 immunity to VDD variations

4.4.2 Process variations at different corners

1)AT SS corner V_{th} of transistors decreases which have a direct relation to output voltage the voltage variation is about 14mV from typical state

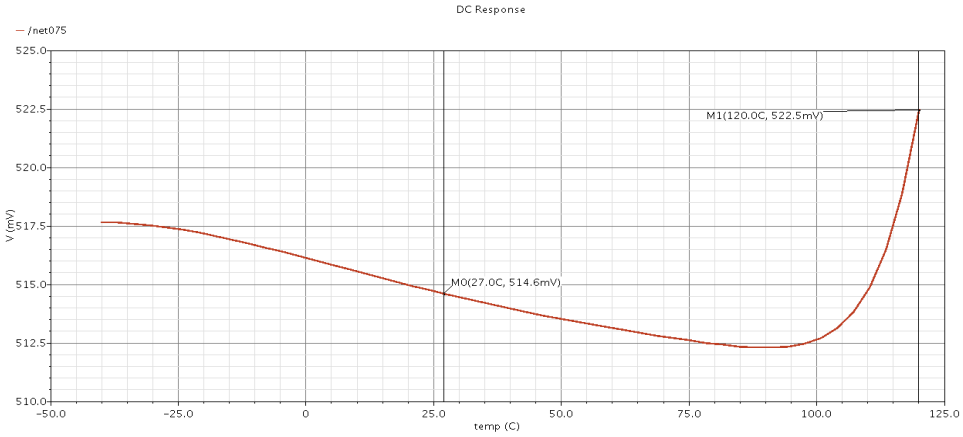


Figure 4-10 voltage variation with temperature at SS corner

2)AT FF corner V_{th} of transistors increases which have a direct relation to output voltage the voltage variation is about 14mV from typical state

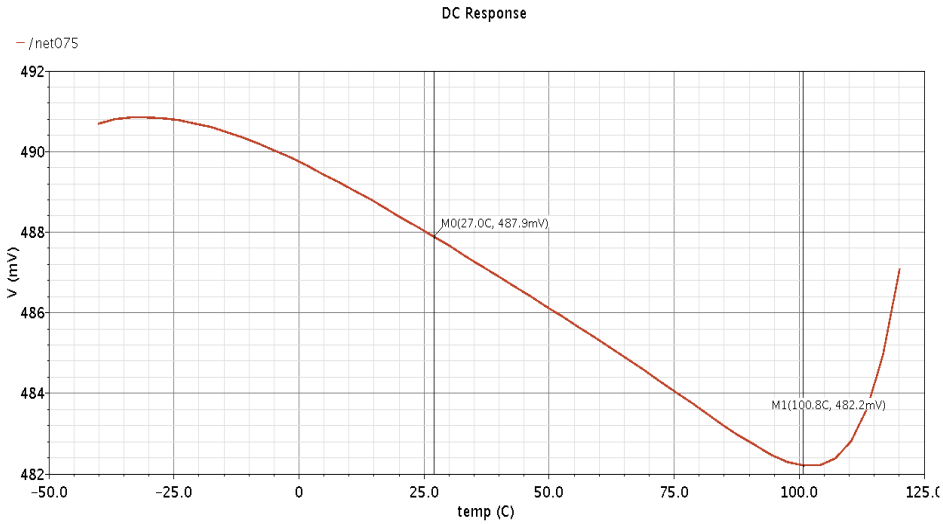


Figure 4-11 voltage variation with temperature at FF corner

The process variations in both cases is about2.5%. A trimming circuit can be used by using M11 as a calibration tool to decrease process variations down to 0.3%

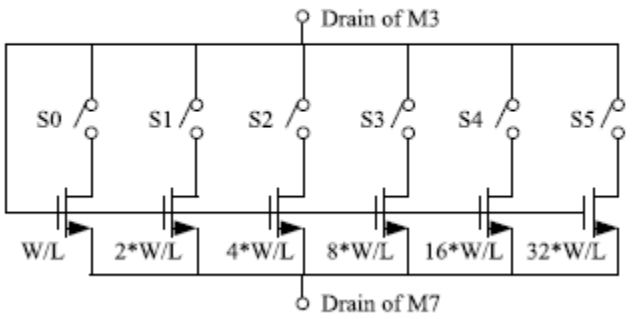


Figure 4-12 using M11 as a trimming circuit

After trimming output voltage becomes:

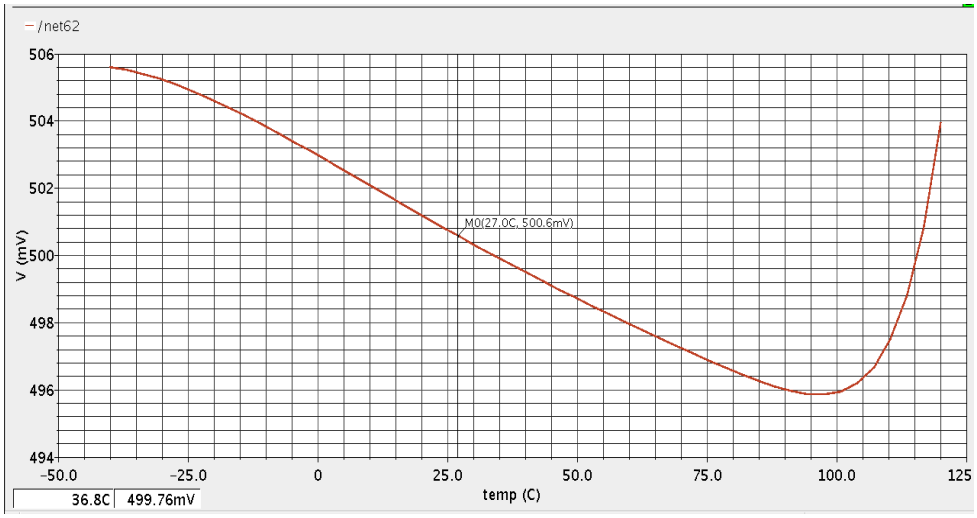


Figure 4-13 output voltage variations at SS corner after using a trimming circuit

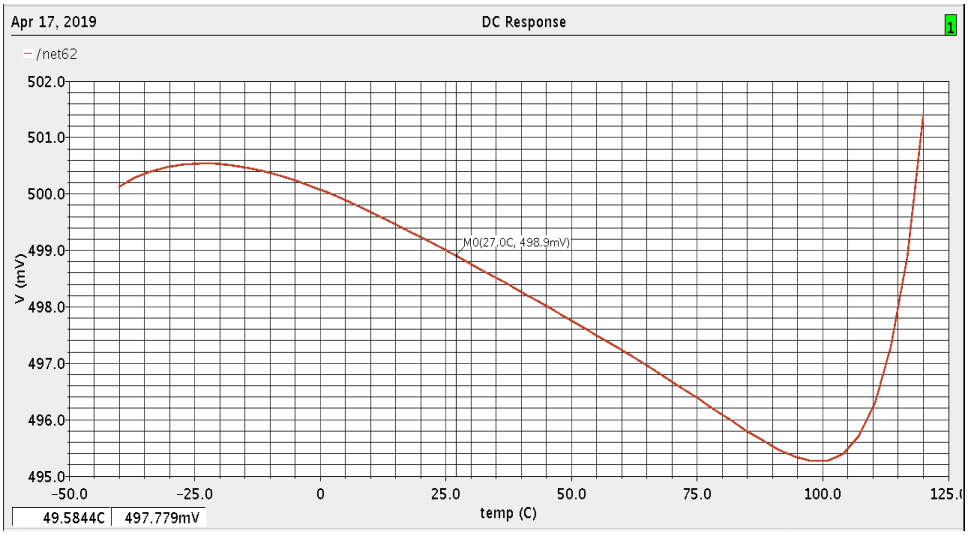


Figure 4-14 output voltage variations at FF corner after using a trimming circuit

4.4.3 Layout Results

OPAMP Layout:

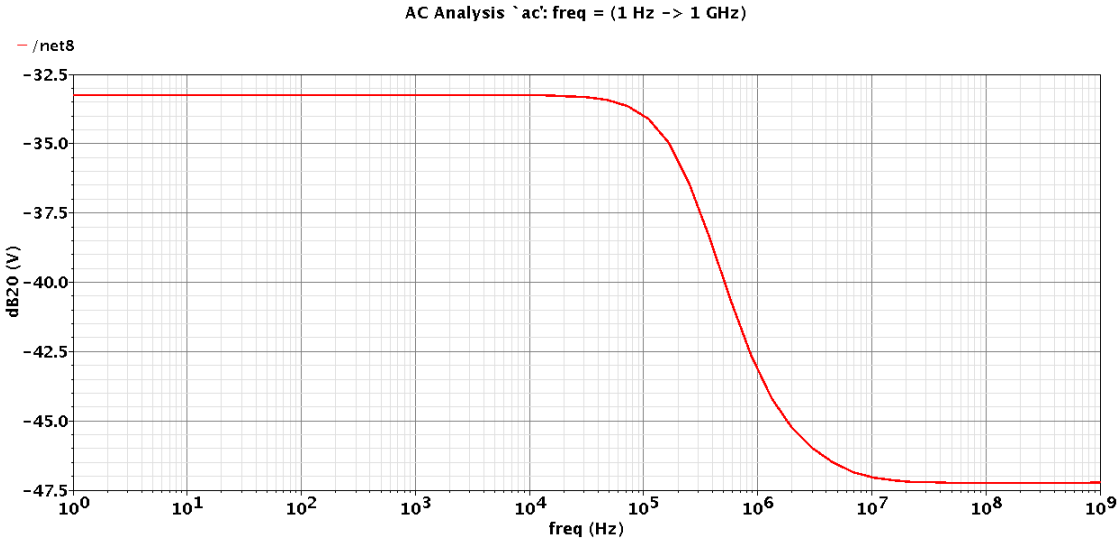


Figure 4-16 op-amp simulation DC gain

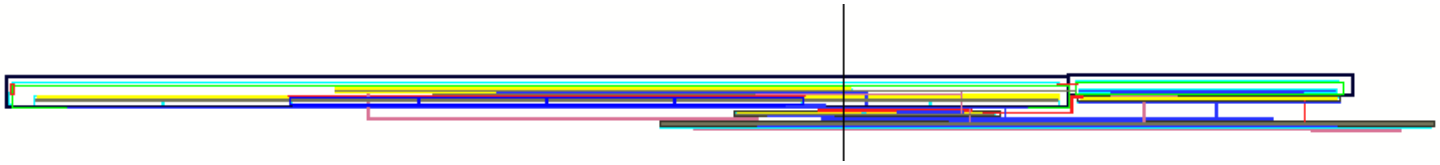


Figure 4-15 op-amp layout

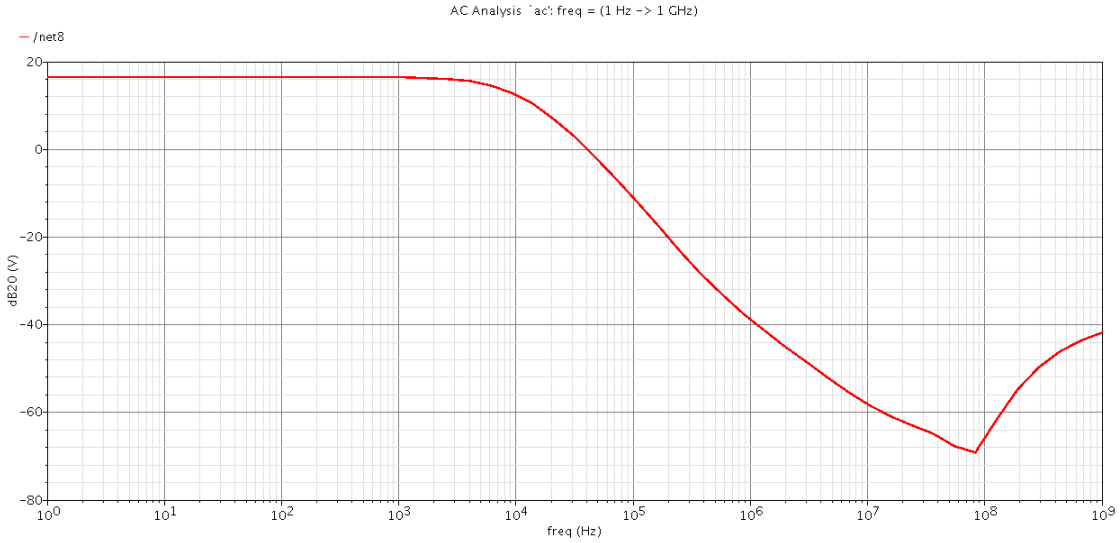


Figure 4-17 post layout simulation of DC gain

BANDGAP CORE LAYOUT:

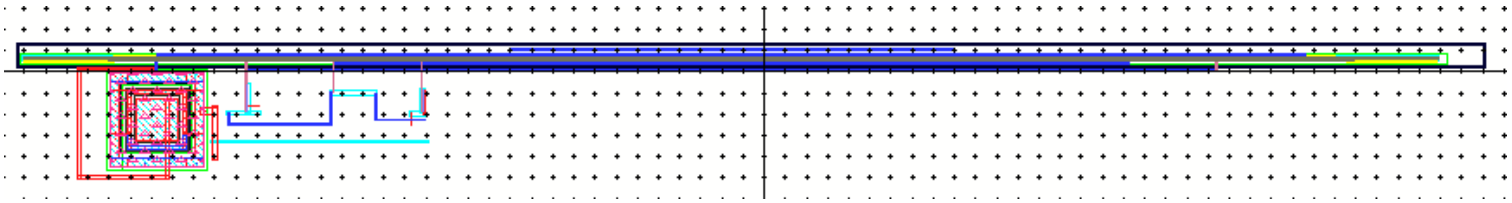


Figure 4-18 Band cap core layout

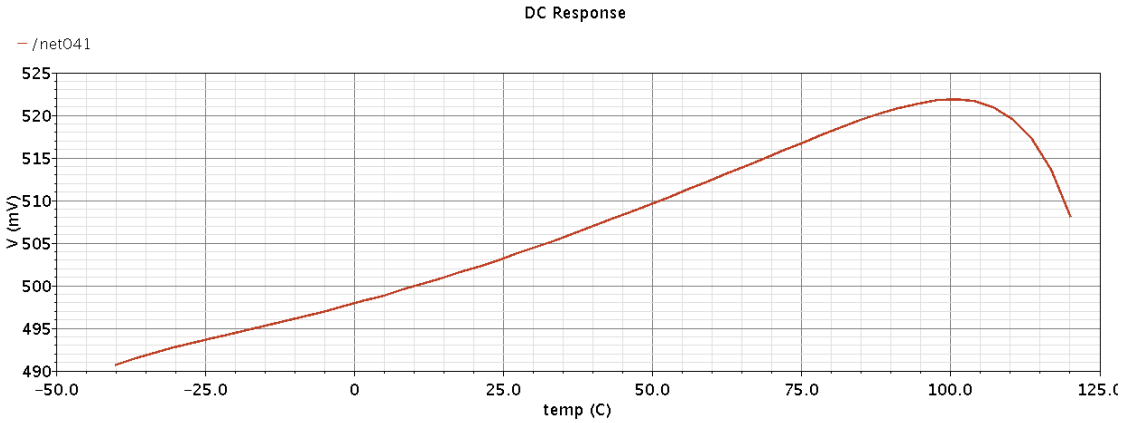


Figure 4-19 Layout simulation of Band gap core

Table 4.4-1 Specs achieved for sub-BGR vs a typical BGR

POC	**Bandgap**	**Sub-Bandgap**
V_{OUT}	1.23 V	0.5 V
TC	12.6 $ppm/^{o}c$	92.37 $ppm/^{o}c$
Power consumption	117.525 nW	87.5 nW
PSRR	@10Hz: -70.8dB @10KHz: -52.98 dB @1 MHz: -17.22 dB	@10Hz: -58.03 @10 KHz: -21.99 @1 MHz: -10.43
Minimum VDD	1.45V	1V

4.5 Voltage to current converter

A certain ideal current value is needed for biasing this value cannot be directly taken from voltage reference through a current mirror in order not to disturb output voltage through the leakage in the current mirror so a V to I converter is used.

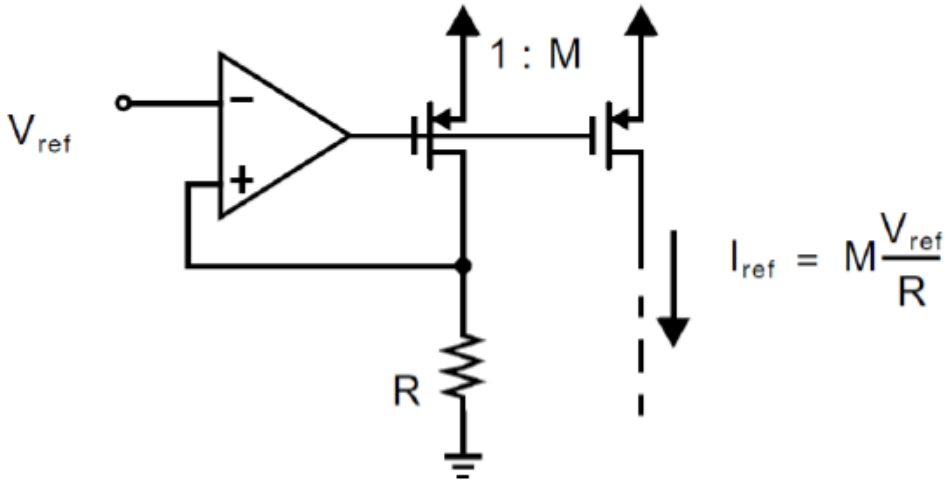


Figure 4-20 voltage to current converter

4.5.1 Operation

A folded op-amp is used to make sure that the voltage on used resistor is equal to output of the ban gap, where $I_{ref}=V_{ref}/R$. By using current mirrors different values of required current can be obtained. For a very high accuracy current an off-chip resistor can be used.

4.5.2 ***Results***

The output current with nominal = 10namp variation across temperature in the range from to $-40\ to\ 120^{o}C$.

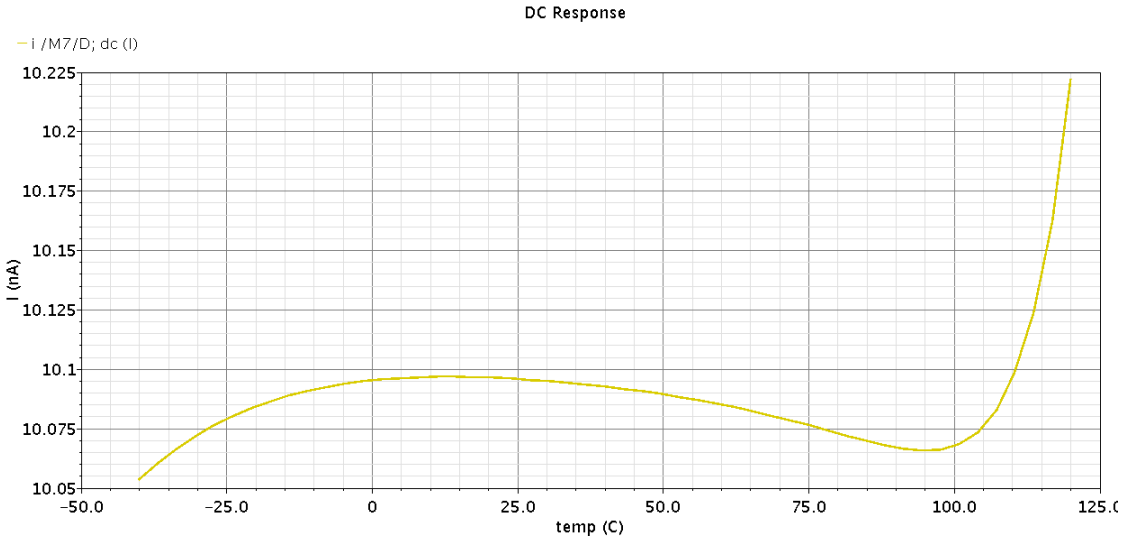


Figure 4-21 current variation across temperature

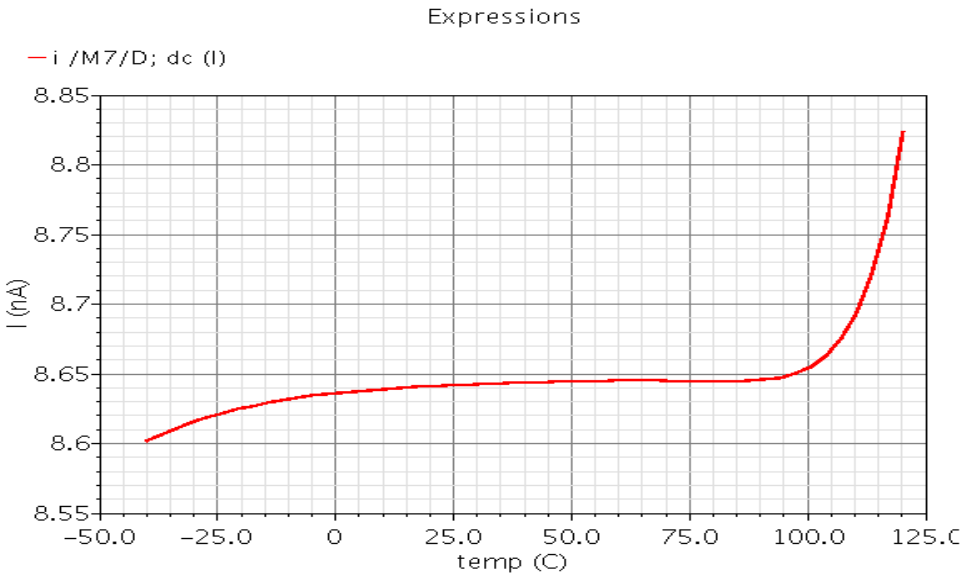


Figure 4-22 current variation across temperature at SS corner

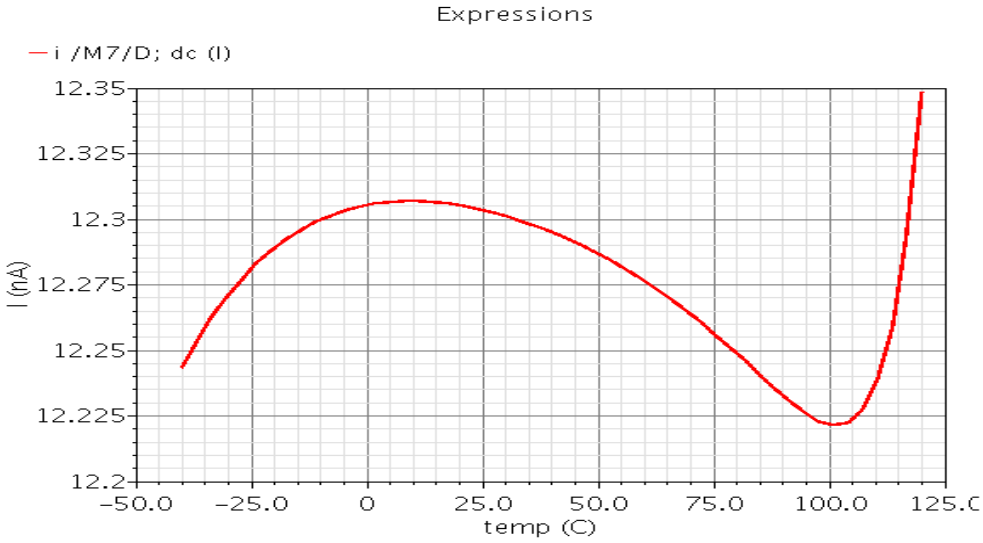


Figure 4-23 current variation across temperature at FF corner

CHAPTER 5. COLD START BLOCK

5.1 Introduction

Since the RF harvesting chip aims to collect RF electromagnetic waves from the surroundings and try to transform this collected power into useable one therefore the first challenge is that the harvested power is so small in range of -18 dBm to 10dbm which is more decreased when it passes by the RF rectifiers which converts RF to DC voltage degrading received power much more. The input voltage to the power management unit becomes a few millivolts which is too low to directly support the electronic circuits and is not enough to make transistors work where they need a minimum threshold at least and is not enough to store enough voltage to act as a power supply to the power management unit itself.

self-startup function is highly desired to kick-start the system operation from cold state. Furthermore, power hungry applications can deplete the stored harvested energy even before it can be recharged. Therefore, the major challenges in start-up circuit design are fast self-startup from low input voltages, up-conversion of the available low voltages to a higher usable voltage and executing these targets with high overall conversion efficiency [26][27].

The minimum startup voltage of a step-up DC-DC converter in standard CMOS technology is limited by the oscillator since a clock signal is required for a charge pump (CP). Practically, the minimum supply voltage of an oscillator (VDDMIN) is limited by PMOS-NMOS VTH. Figure 5.1-1 shows the structure of a cold start unit.

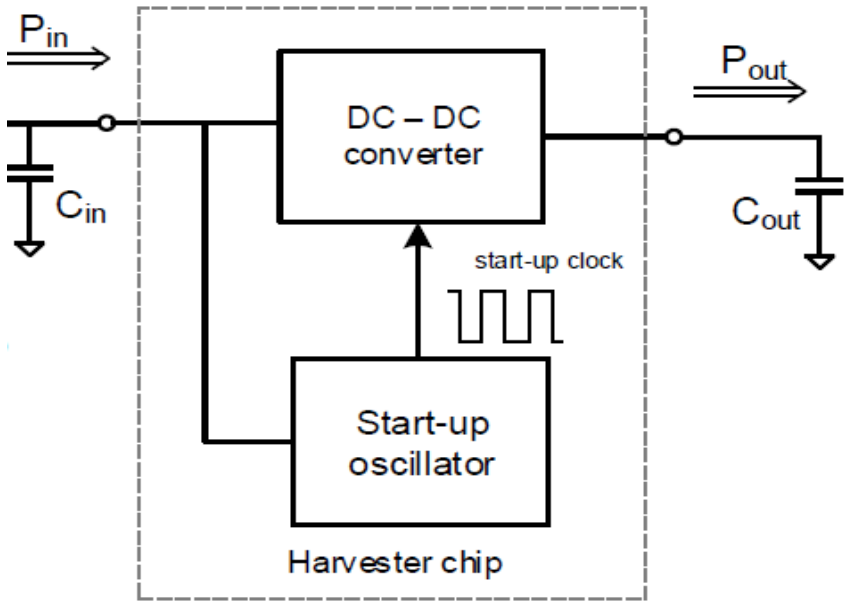


Figure 5-1 structure of a cold start unit

5.2 Cold Start Blocks

5.2.1 Start-up oscillator

One approach to boosting such a low input voltage is to use a low-voltage oscillator to start up a higher voltage DC-DC converter. low threshold MOSFET transistors are used. The oscillator stage is used to convert Dc voltage to Ac pulse to act as a clock pulse to the charge pump. This oscillator consists of 35 stages of a ring oscillator having a frequency=4. 086M. The frequency is reduced by increasing the number of stages and the delay of each to improve the overall efficiency however the settling time do increase. The minimum used volt is 0.2v so low threshold transistors are used [23]. Below are the

simulation results and the post layout simulation results.

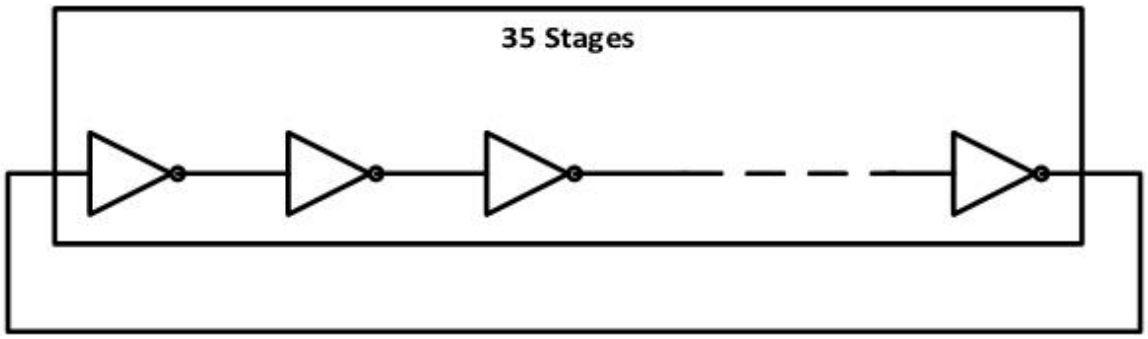


Figure 5-2 Oscillator schematic

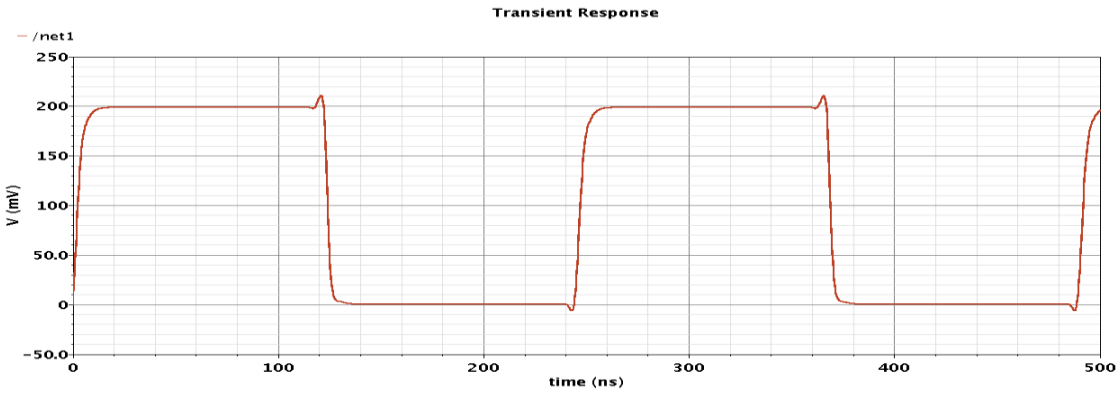


Figure 5-3 Oscillator Output

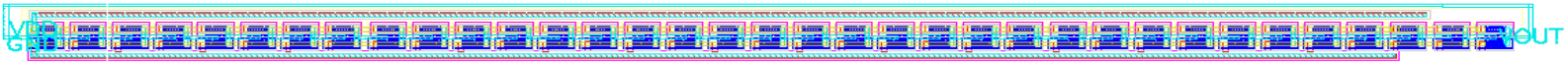


Figure 5-4 Oscillator Layout

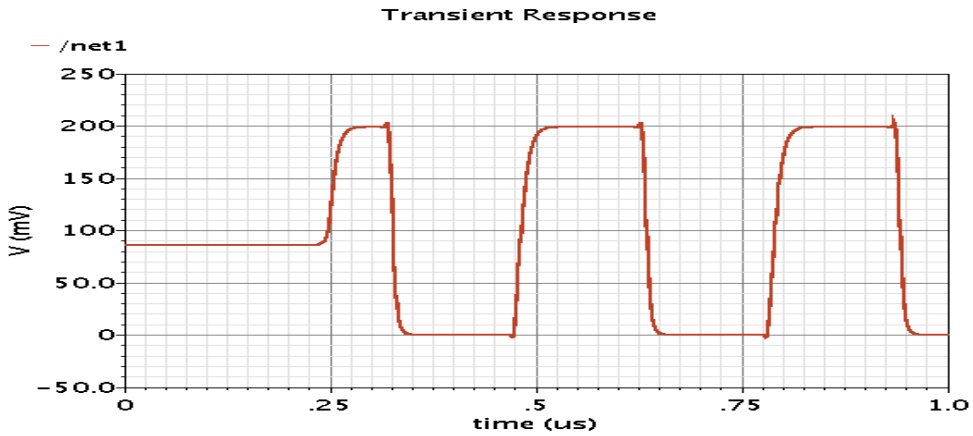


Figure 5-5 post Layout simulation of oscillator

After layout simulation output frequency became 3.682M

5.2.2 Non-overlapping clock generator and buffer

Non-overlapping clock generator is used to make sure that the clock making charge pump work doesn't overlap it consists of a NAND gate and two inverters. the buffer is used so that the circuit withstands the high capacitance load of the charge pump where each cap value equals to 3 pF.

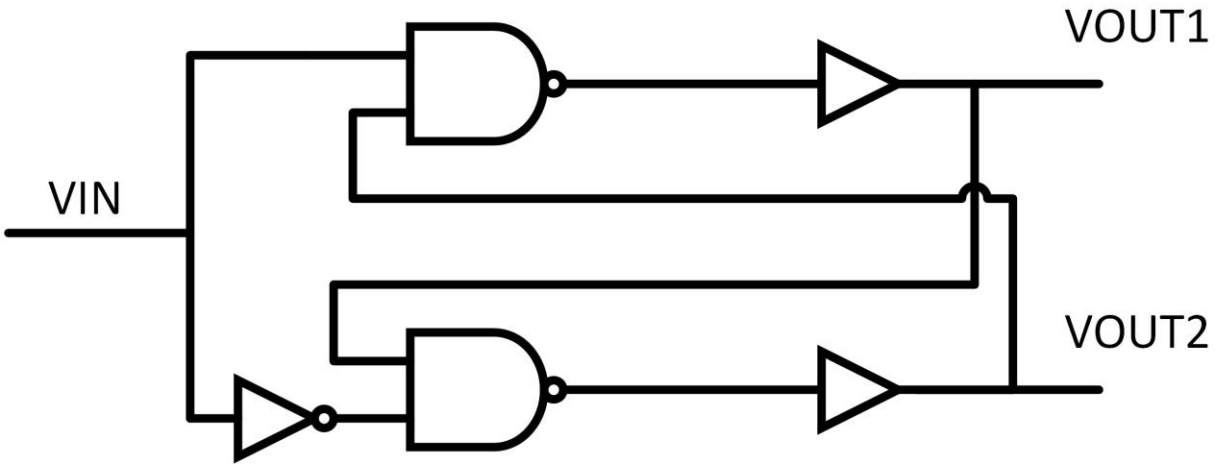


Figure 5-6 Non-overlapping clock generator schematic

The Non-overlapping clock generator consists of two halves. The input to each half is the output of the other half and output of the oscillator or its inversion. if the inputs to the NAND gate are alike then it makes output reaches zero and so on.

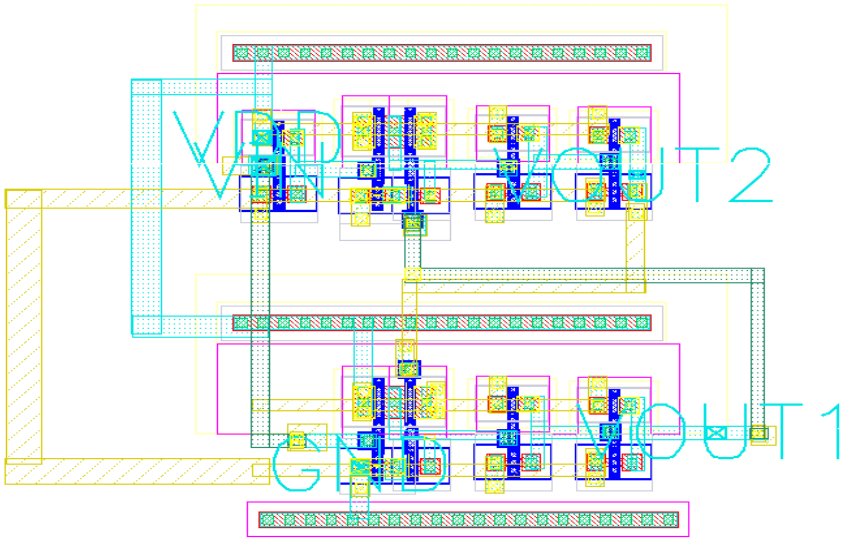


Figure 5-7 Layout of non-overlapping clock generator

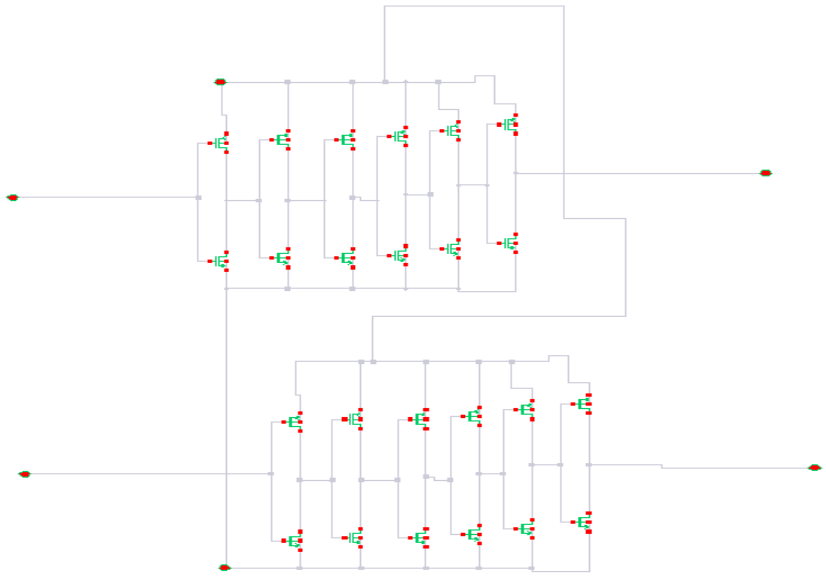


Figure 5-8 Buffer schematic

Due to the high capacitance load of the charge pump a buffer is needed to withstand it or the clock signals will be corrupted in this buffer 6 stages of inverters are used where each stage sizing is greater than previous one 5 times.

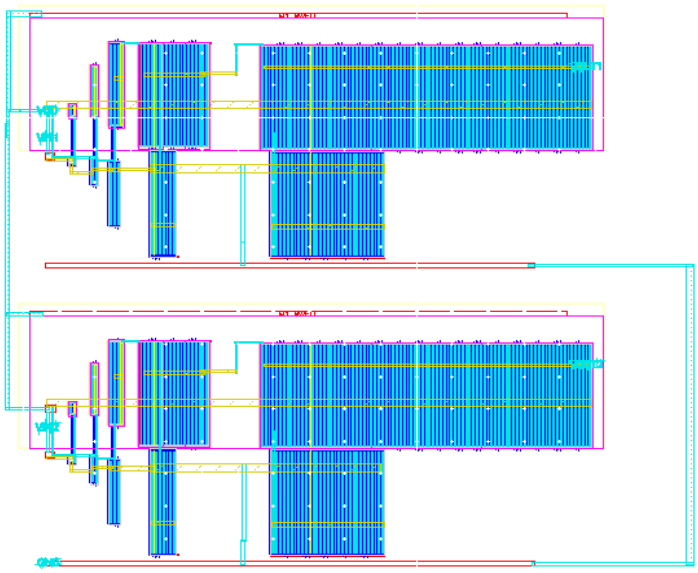


Figure 5-9 Buffer layout

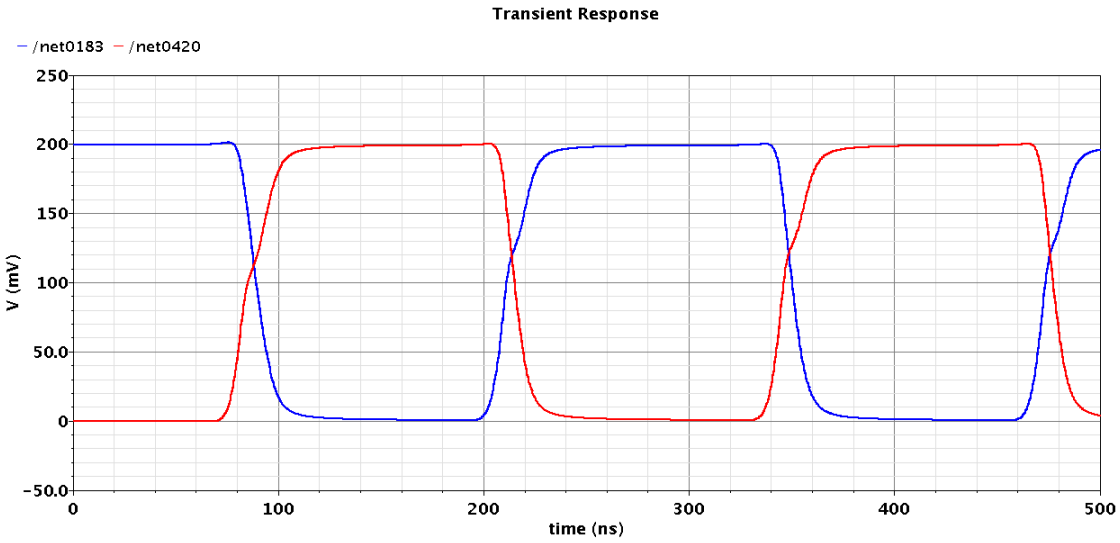


Figure 5-10 clock driving charge pump

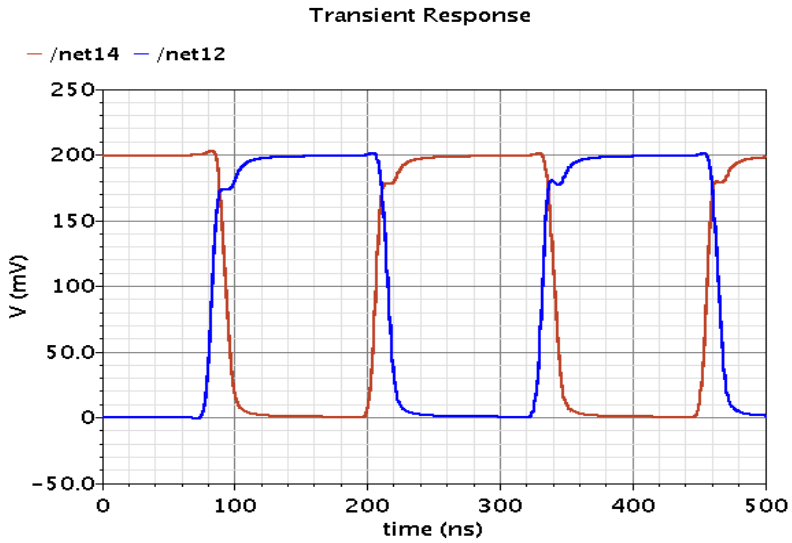


Figure 5-11 post Layout simulation of clock driving charge pump

5.2.3 charge pump

A charge pump is a kind of DC to DC converter that uses capacitors for energetic charge storage to raise or lower voltage.

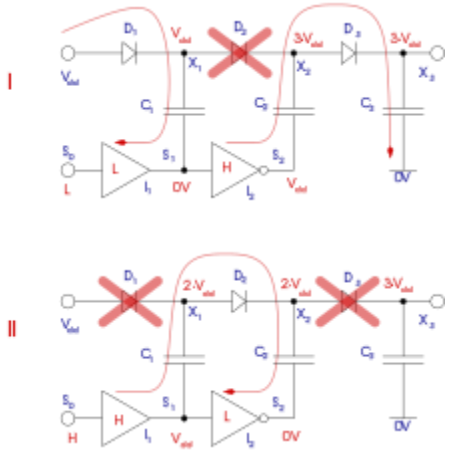


Figure 5-12 two stages of a charge pump

Charge pumps use some form of switching device to control the connection of a supply voltage across a load through a capacitor. In a two-stage cycle, in the first stage a capacitor is connected across the supply, charging it to that same voltage. In the second stage the circuit is reconfigured so that the capacitor is in series with the supply and the load. This doubles the voltage across the load - the sum of the original supply and the capacitor voltages. The pulsing nature of the higher voltage switched output is often smoothed by the use of an output capacitor.

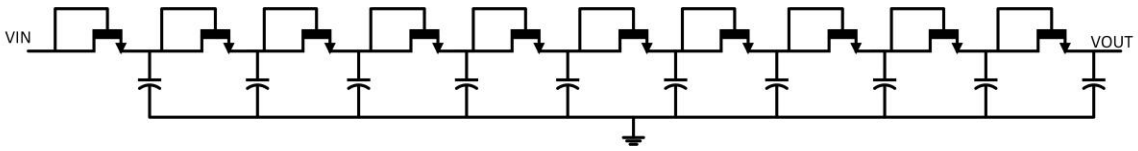


Figure 5-13 charge pump

The used charge pump is a classical one, ten stages where used to reach the required output of 1.2V at different temperature and corner effects if the voltage exceeds the required a battery protection circuit can be used. the minimum input voltage to the charge pump is 0.2V.

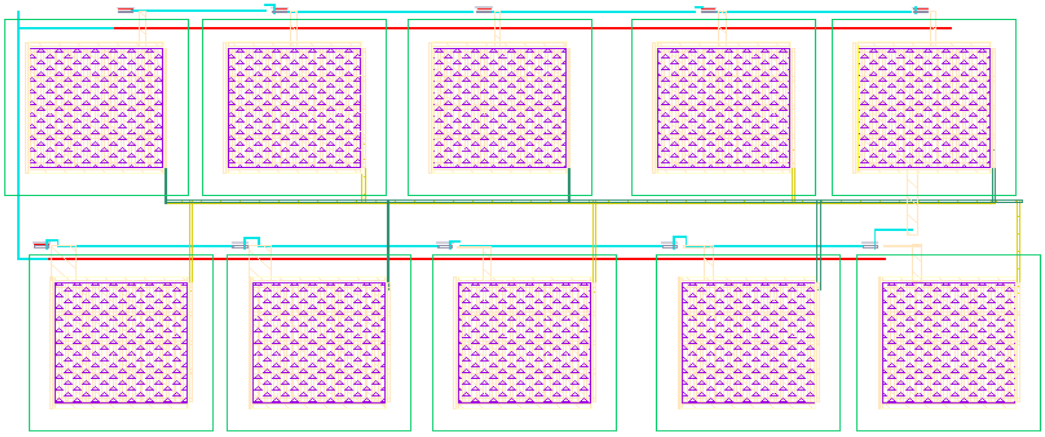


Figure 5-14 Layout of the used charge pump

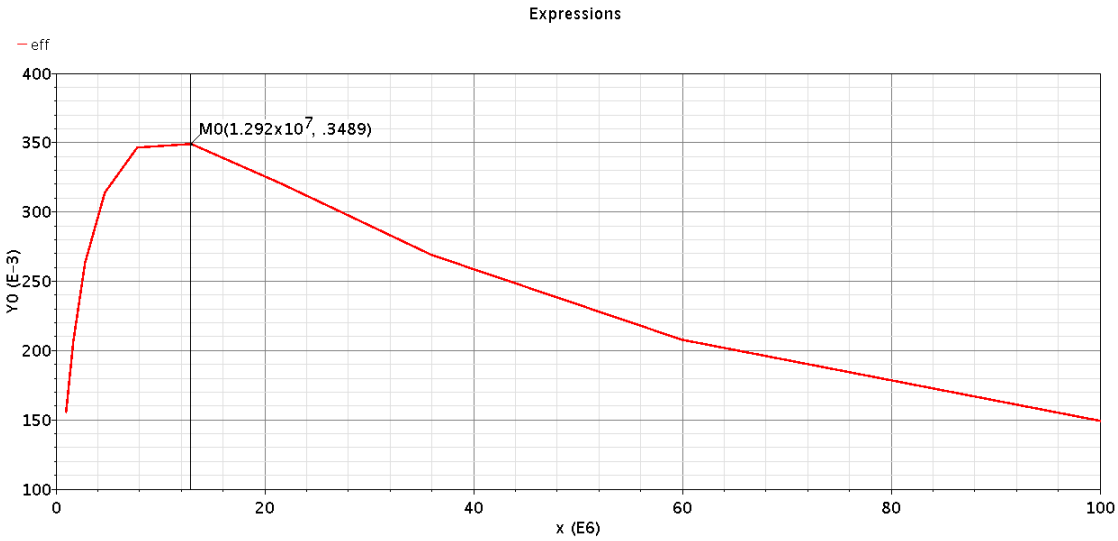


Figure 5-15 charge pump efficiency at various loads

The optimum used Rout is 13M ,so it is required to used Rout greater than 10M at input output volt=0.2.

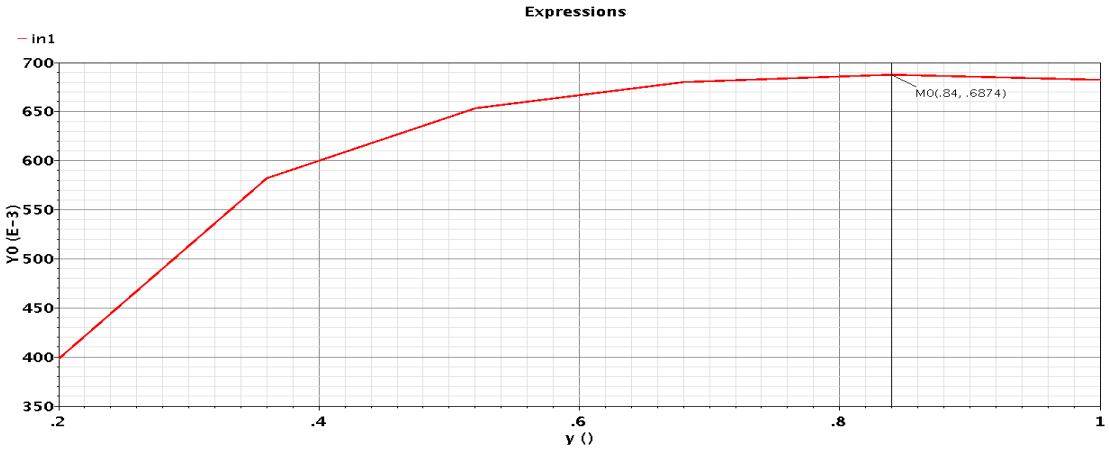


Figure 5-16 charge pump efficiency at different input voltages @Rout= 13M

5.3 Overall results of cold start unit

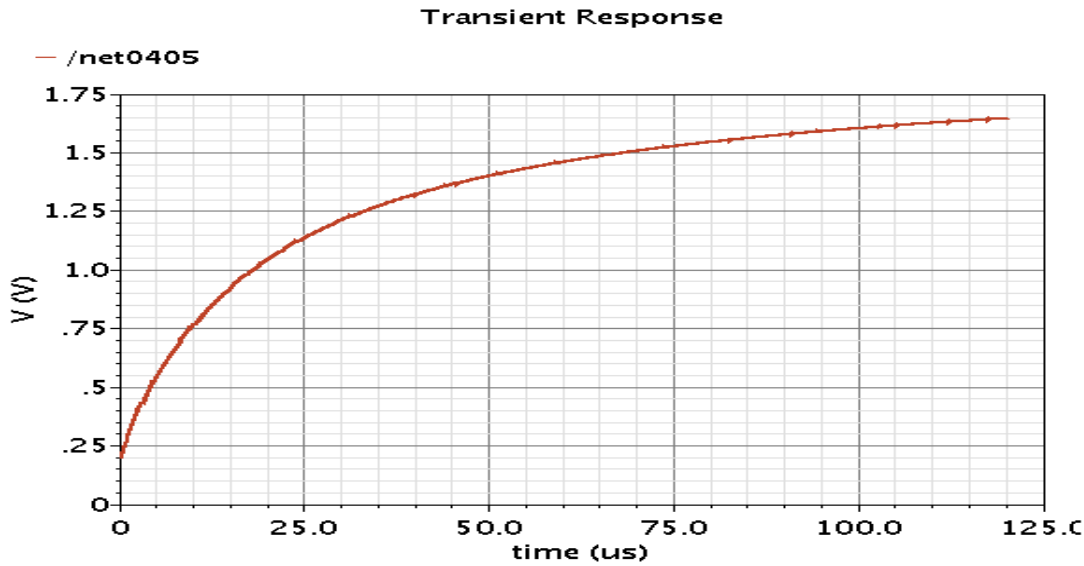


Figure 5-17 cold start output @ vin=0.2v

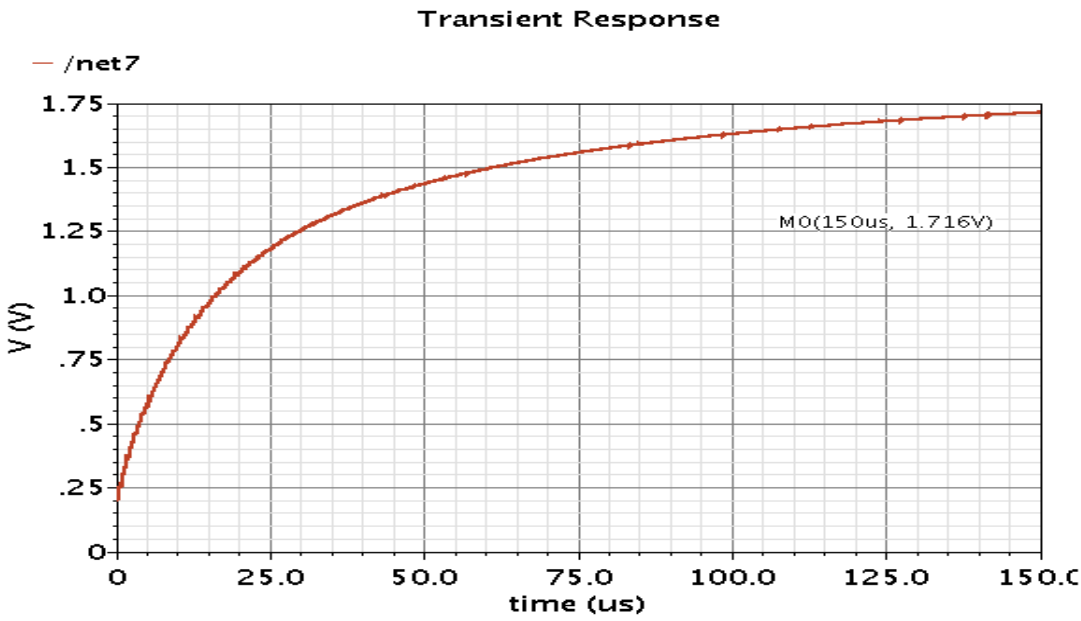


Figure 5-18 Layout simulation of cold start

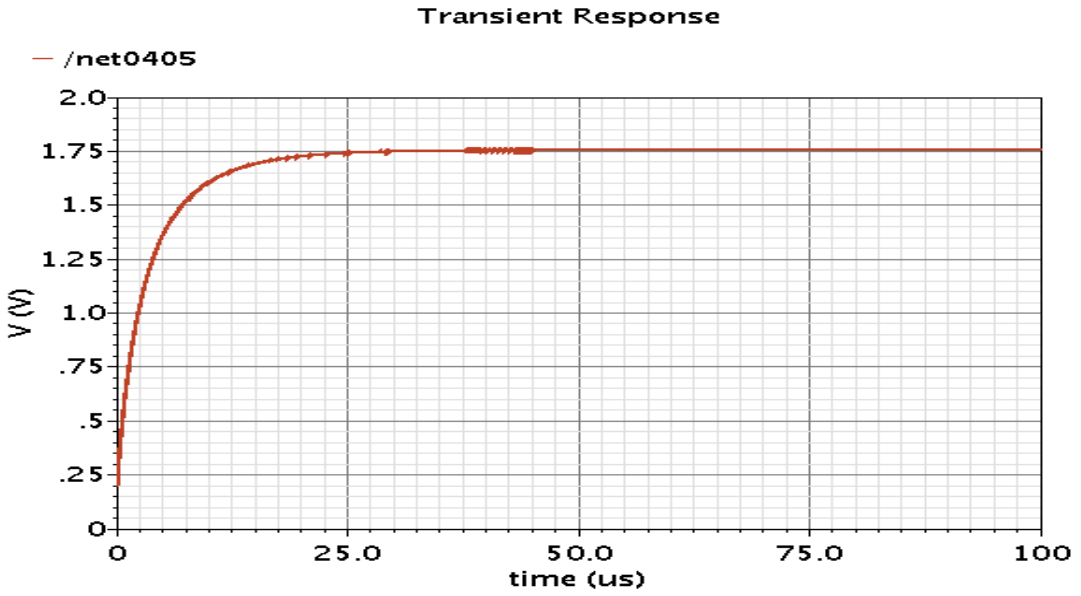


Figure 5-19 cold star output @ FF corner

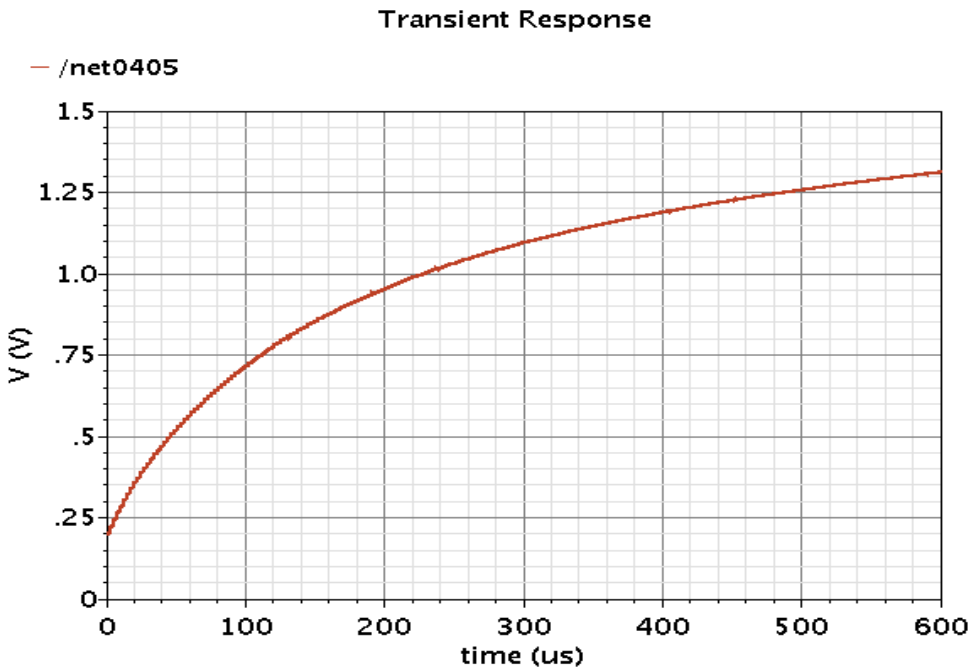


Figure 5-20 cold star output @ SS corner

Typically settling time is about 150 microseconds as frequency is reduced to increase overall efficiency by reducing switching losses, At SS corner the settling time increases and it decreases at FF corner as V_{th} is decreased as total output=number of stages*input voltage-number of stages*V_{TH}

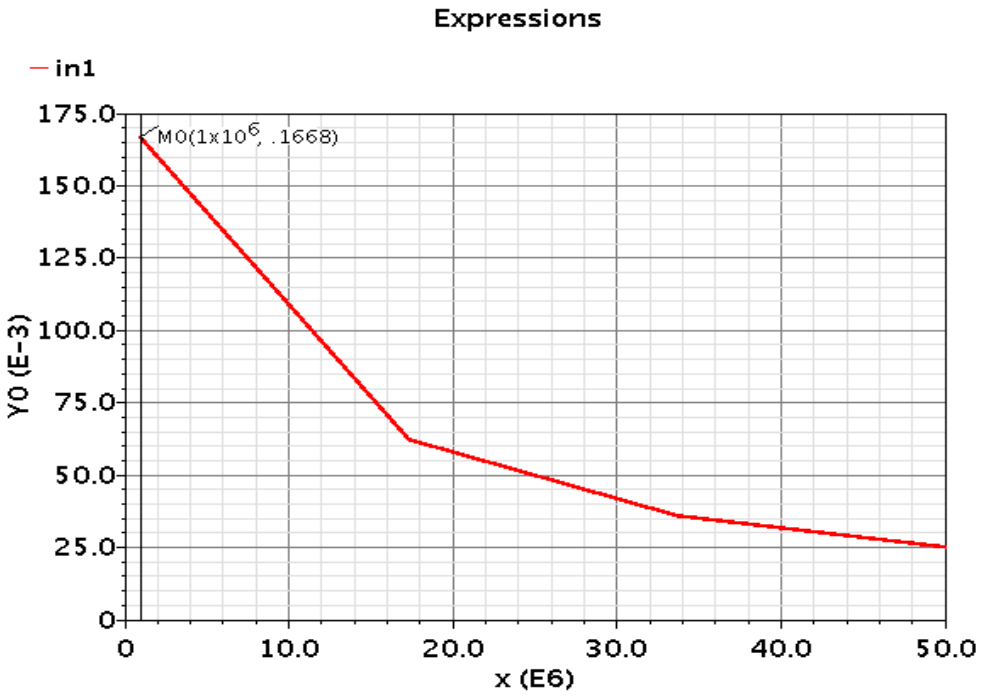


Figure 5-21 efficiency of cold start at various loads

5.4 Cold start comparator

The cold start comparator is responsible for enabling the cold-start block at the cold start mode and disable it at the primary mode. The design of the cold start comparator is proposed in [22] and is shown in Figure 1. When VLOAD exceeds a threshold voltage, the cold-start comparator makes CS_DI S high, transitioning to primary mode.

The comparator is powered from V_{LOAD}. Initially, as V_{LOAD} increases from 0 V, V_{d1} follows V_{LOAD} (since the leakage through M5 is >> the OFF-state leakage through the NMOS pull-down paths), causing CS_DIS to be low, enabling the ring oscillator and CP (Charge Pump). As V_{LOAD} continues to increase, V_{b1} at the gate of M3 increases, which pulls V_{d1} lower. The relative strengths of M3 and M5, and V_{b1} divide ratio determine the V_{LOAD} at which V_{d1} goes low enough to cause CS_DIS to go high. The threshold could be

programmable by using a variable resistance (using programmable MOS switches) as shown in Figure 1. The threshold value is determined based on minimum V_{LOAD} for

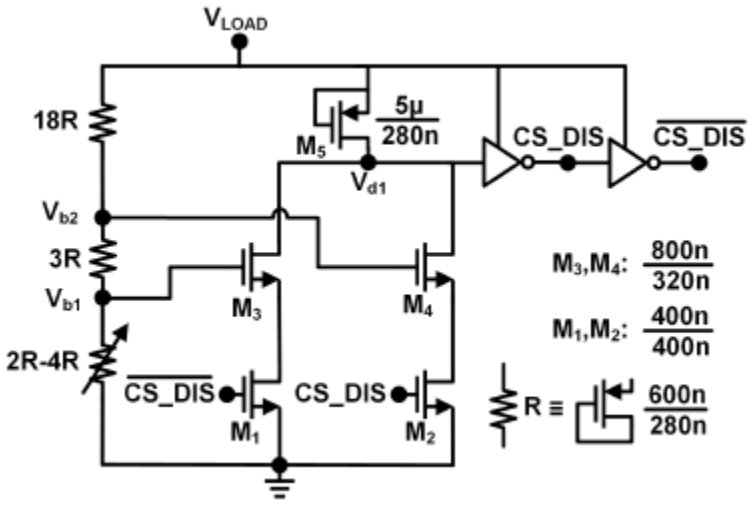


Figure 1: Cold start comparator with hysteresis

efficient converter operation and is designed to be 0.75 V. Hysteresis is built into the comparator through M4 and M2, which makes the comparator immune to incident power fluctuation. When V_{LOAD} discharges, harvester returns to cold start at 0.3 V (> min. voltage for ring osc. startup). The comparator consumes power < 15 nW.

Figure 2 shows the simulation results of the cold start comparator. As shown the CS-DIS is high starting from 0.75 V while it goes low at 0.3 V.

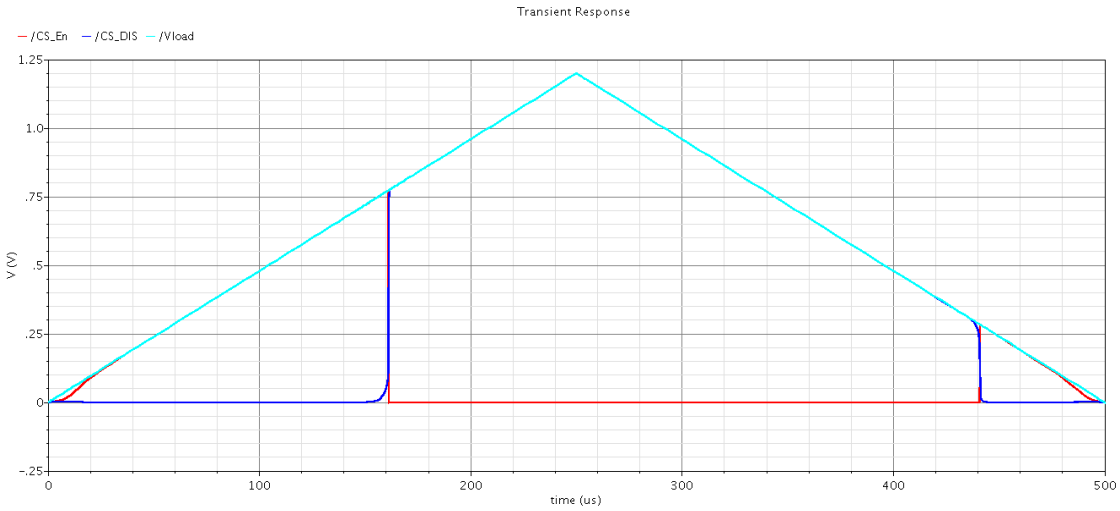


Figure 2: Transient response of cold start comparator while increasing and decreasing its VDD

CHAPTER 6. CONCLUSION

This work presents a power management IC for low-voltage RF energy harvesting in power range from -18dBm to 10 dBm that can harvest energy from the ambient surroundings at the radio frequency range of 2.4GHZ.It depends on a dedicated bootstrap circuit enabling battery-less cold start-up from input voltage down to 200 mV to produce an output of at least 1.2 volts and works with two loops for input and output voltage regulations. Once cold start-up is performed, the bootstrap circuit is automatically disabled using a hysteresis comparator and the two voltage regulators start operating, so as to increase efficiency and to limit the power absorption. A sub band gap circuit is used to provide an accurate voltage reference and biasing source for the power management unit. The first stage of voltage regulation is a MPPT stage to operate on maximum power point to allow an efficient harvesting profile and also high overall system efficiency ,based on a PFM mode of operation and maximizing for rectifiers operating for output in range of 100 Ω-500Ω with efficiency up to 64% and tracking efficiency up to 97%.The second stage is a boost converter working on both PWM and PDM modes regulating the output to 1.2v with high efficiency and small ripples .The sub band gap circuit provides a constant voltage against temperature and process variations providing less than ±3.5mV variation in the temperature range from -40 to 120 degree Celsius. The IC was tested with input voltage ranges from 100 mV up to 1 V. Thanks to nano-power design techniques and to a careful control of the energy consumption, the circuit can operate with an input power of less than 1μW.The most important aspect of this IC is that it is a RF chip where Compared to common alternative energy sources like solar and wind, RF harvesting has the least energy

density , but this doesn’t stop this IC from achieving high efficiency at the same time. Decreasing the minimum manageable power to such low levels paves the way towards the deployment of a new class of applications based on tiny and weak environmental sources that could not be efficiently Exploited up to now ,which will allow product designers and engineers to extend battery lifetime and ultimately get rid of the primary energy storage element in a large range of wireless applications like industrial monitoring, home automation, wearables.

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