Zewail City for Science and Technology
University of Science and Technology
Nanotechnology and Nanoelectronics Engineering Program

Design of a Continuous-Time Bandpass Sigma-Delta Analog to Digital Converter for Software-Defined Radio based Receivers

A Graduation Project
Submitted in Partial Fulfillment of
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Nanotechnology and Nanoelectronics Engineering

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Abstract

With the ever-growing market of mobile devices, software-defined radio (SDR) has become a promising alternative to conventional RF receiver architectures since it performs most of the signal processing in the digital domain. As a result, the proceeding analog to digital converter (ADC) is required to digitize wide-band signals without down-conversion, with a high sampling frequency, high resolution, and power efficiency.

In this thesis, a second-order continuous-time band-pass sigma-delta (CTBPSD) ADC is implemented. The ADC has a sampling frequency of $800\,MS/s$ with a bandwidth of $6.25\,MHz$ at $200\,MHz$ center frequency and an Oversampling Ratio (OSR) of 64. The circuit is designed using $65nm$ CMOS process technology, with a supply of $1.2V$.

The system consists of a differential single Operational Amplifier (Op-Amp) resonator for the loop filter followed by a modified StrongArm comparator then two current-steering digital to analog converters (DACs) in the feedback loop for noise-shaping. Finally, to compensate for the timing differences between the DACs and the comparator, a clock delay is implemented using a master-slave positive-edge-triggered register and a negative latch.

First, the ideal system is modeled in Simulink to find the optimum input amplitude and the expected ideal Signal to Noise Ratio (SNR). Then, the system is modeled in Simulink with a non-ideal resonator to find the required gain and bandwidth of the resonator's Op-Amp and the expected SNR of the non-ideal system. Second, the system is simulated in Cadence using ideal Verilog-A macro models for the Op-Amp, comparator, DACs, and delay. This ideal macro-model was used to determine the values of the resistances and capacitances of the resonator that achieve the ideal SNR and an appropriate voltage swing on the output of the Op-Amp and to determine the required output currents for the two DACs. Third, the transistor-level Op-Amp, comparator, DACs, register, and latch are designed using the specs obtained from the Simulink and Cadence models.

The final system achieves an SNR of $52\,dB$, an SFDR of $63.13\,dBc$ and an ENOB of $8\,bits$ with a power consumption of $37.7\,mW$.

Acknowledgments

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Finally, we would like to express a special thank you to our colleague Amr Nasser for his volunteer work on this project.

Declaration

This thesis is a presentation of our own work. All formulations and concepts taken from other sources have been cited. This thesis is submitted in partial fulfillment of B.Sc. degree requirements in Nanotechnology and Nanoelectronics Engineering and has not been submitted previously for the award of any academic degree. The work was done under the supervision of Prof. Hassan Mostafa and Prof. Hassan Aboushady at the University of Science and Technology at Zewail City.

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Abbreviations

Abbreviation	Definition
RF	Radio Frequencies
ADC	Analog to Digital Converter
SDR	Software Defined Radio
DSP	Digital Signal Processing
IF	Intermediate Frequency
CTBPSD	Continuous-Time Bandpass Sigma-Delta
SNR	Signal to Noise Ratio
DAC	Digital to Analog Converter
f_N	Nyquist Frequency
SAR	Successive Approximation Register
dB	Decibel
SNDR	Signal to Noise and Distortion Ratio
ENOB	Effective Number of Bits
RMS	Root-Mean Square
FFT	Fast Fourier Transform
CT	Continuous-Time
DT	Discrete-Time
S/H	Sample and Hold
MSB	Most Significant Bit
LSB	Least Significant Bit
OSR	Oversampling Ratio
f_s	Sampling Frequency
f_{BW}	Bandwidth Frequency

AAF	Anti-Aliasing Filter
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
NTF	Noise Transfer Function
Op-Amp	Operational Amplifier
RZ	Return-to-Zero
HZ	Half-Delayed-Return-to-Zero
NZ	Non-Return-to-Zero
SR Latch	Set/Reset Latch
LPF	Low-pass Filter
HPF	High-pass Filter
LHP	Left-Hand Plane
TF	Transfer Function
FF	Feed-Forward
CMFB	Common-mode Feedback
vcvs	Voltage-Controlled Voltage Source
vccs	Voltage-Controlled Current Source

Chapter 1

1.1 Introduction

With the ever-growing market of mobile devices, a common trend began to shape, which is to embed each device with multiple communication standards over-which the devices can send and receive data. Standards such as Wi-Fi, Bluetooth, and LTE, each operate in a different frequency range, which requires a unique RF receiver that is specific to this band. However, this poses a problem, as adding RF receivers to support more standards, increases area, complexity, and power consumption, which consequently affects battery life. Therefore, a single RF receiver that supports multiple standards is very attractive for wireless communication, as it will solve most of the problems associated with adding multiple receivers to the same device. However, such design requires a front-end with reconfigurability, wide bandwidth, and high resolution.

Multi-Standard Receivers

There are many approaches to realize multi-standard RF receivers, the most common is the tunable mainly-analog architectures. Such architectures perform most of the signal processing in the analog front end, before introducing it to the Analog to Digital Converter (ADC), which reduces the need for high-performance ADCs. However, controlling the tunability through rigid analog blocks comes with its limitations, such as noise, nonlinearity, and mismatch. These limitations highly affect the performance of such receivers.

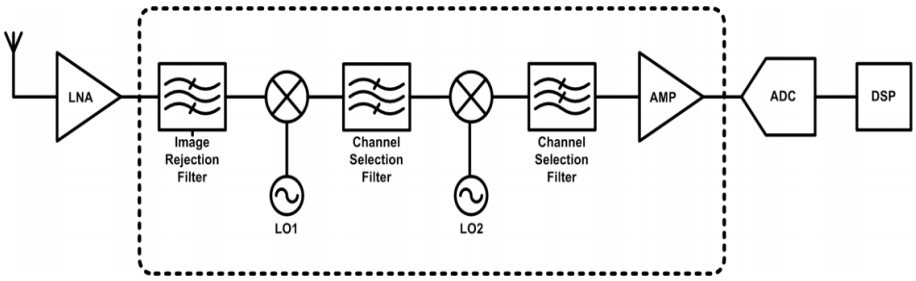


Figure 1 Super-heterodyne Receiver Architecture

The heterodyne architecture, shown in Figure 1, is one of the most popular tunable analog architectures [1]. Although this architecture is very good for frequency selectivity and sensitivity in environments with strong interferers, like most analog architectures, it suffers from complexity in the front-end receiver chain and lack of reconfigurability. Moreover, it requires several stages of amplification, filtering, and mixing, which increases both area and power consumption.

Software Defined Radio (SDR)

Software-defined radio (SDR) is a topology that performs most of the signal processing in the digital domain [2]. This enables the topology to eliminate most of the front-end analog blocks while performing most of the signal processing in the DSP block as shown in Figure 2. As a result, the ADC is now required to process wide-band signals without down conversion. The technology has been available since the 1980s [3]. However, it has been bottlenecked by designing ADCs with bandwidth, high resolution, and reasonable power consumption.

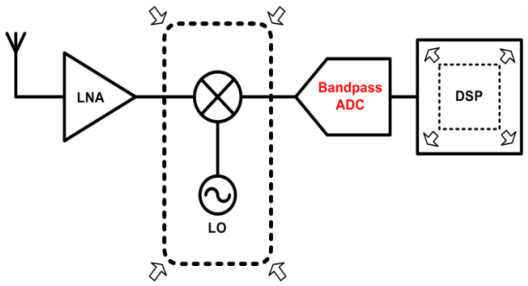


Figure 2 SDR Receiver Topology

1.2 Problem Definition

With the increase of the number of features incorporated into mobile phones, tablets, and other devices, SDR has become a promising alternative to conventional RF receiver architectures. The bottleneck to the implementation of SDR is the design of an ADC that digitizes the signal in the IF or RF, without down-conversion, with a high sampling frequency (speed), high resolution, and power efficiency.

1.3 Objectives

Generate the transistor level design of a $800MS/s$ second-order continuous-time bandpass sigma-delta (CTBPSD) ADC with a bandwidth of $6.25MHz$ at $200MHz$ center frequency. The ADC needs to achieve a high SNR value and low power consumption.

1.4 Report Organization

Chapter 2 begins with a review of the most common ADC architectures; Nyquist-rate, Flash and Successive Approximation Register (SAR), and oversampling. The delta-sigma ADCs basics are explained followed by a review of its main components; the loop filter, the quantizer, and the digital to analog converter (DAC). Chapter 3, then, describes the project's purpose and technical specifications and introduces the block diagram of the system and the functions of its components. Chapter 4 lists the project tasks and the Gnatt chart and the implementation steps. For the implementation, the system level MATLAB model is described first followed by the Cadence model of the idea system. After that, the transistor-level design of each of the blocks is presented in detail. Lastly, the final system integration and evaluation are presented. Chapter 5 reviews the cost analysis of this project and studies its environmental, social, and economic impact along with its sustainability. Finally, Chapter 6 presents the conclusion of the thesis and the discussion of possible future work.

Chapter 2

Literature Review

Real signals in nature are all in the Analog domain where it is complex to process and analyze the signal directly. As a result, it is desirable to deal with the signal in the digital domain where the transmission, storage, and processing of the signal is more efficient. According to the application, the conversion could be achieved through a suitable ADC architecture. ADCs are categorized based on the sampling rate into Nyquist rate ADCs and Oversampling ADCs. Nyquist rate ADCs sample the input analog voltage at a rate a bit higher than the double of the input maximum frequency; f_N. Oversampling ADCs sample the input analog voltage at a rate much higher than the f_N, usually 4 to 10 times higher. Most popular Nyquist rate ADCs are SAR ADC, Flash ADC, and Pipelined ADC, while Sigma-Delta ADC is the most popular Oversampling ADC. In this section, the performance metrics of any ADC are discussed. Then, the Nyquist rate and Oversampling ADCs are reviewed. Finally, the delta-sigma ADCs basics are explained followed by a review of its main components.

2.1 Performance Metrics of ADCs

To measure the performance of any ADC, the ADC should be characterized by static and dynamic characteristics. The static characteristics determine the deviations from an ideal ADC. An ideal ADC is basically a linear system where any change in the output depends only on the amount of change in the input. The dynamic characteristics determine the dynamic performance of the system in the frequency domain; mainly the speed and frequency response of the ADC. The static and dynamic characteristics are discussed in this section.

Static Characteristics:

1. Offset Error: It is defined as the positive or negative deviation in the input-output characteristic line from the ideal one as shown in Figure 3.

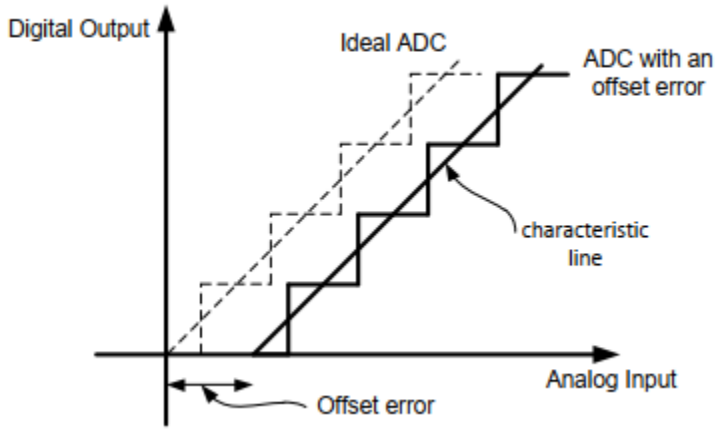


Figure 3 ADC with offset error [4]

2. Gain Error: It is defined as the positive or negative deviation in the slope of the input-output characteristic line from the ideal one as shown in Figure 4.

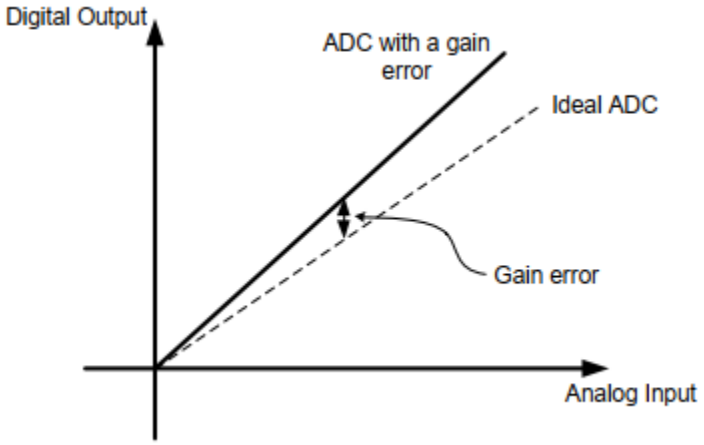


Figure 4 ADC with Gain Error [4]

3. Differential Non-Linearity (DNL): It is defined as the positive or negative deviation in the step width of the converter from the ideal step width as shown in Figure 5. DNL could be calculated from Equation 1 where $A(i)$ is the point at which the digital code trips from i to $i+1$, trip point, and A_{LSB} is the step width of the converter.

$$DNL(i) = \frac{A(i+1) - A(i)}{A_{LSB}} - 1 \qquad Eq.1$$

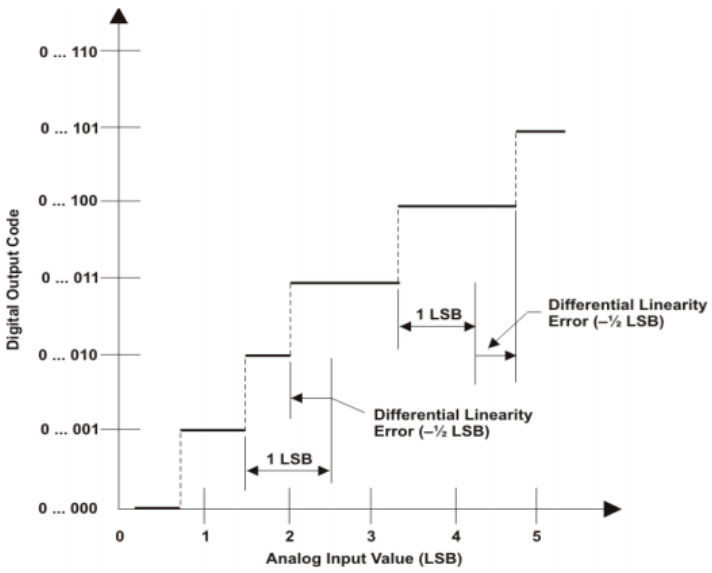


Figure 5 ADC with DNL [5]

4. Integral Non-Linearity (INL): It is the change of the position of the trip point from the ideal position, in other words, the deviation of the input-output characteristic line from a straight line as shown in Figure 6 and 7. INL could be determined as

$$INL(i) = \frac{A(i) - i * A_{LSB}}{A_{LSB}} \qquad Eq.2$$

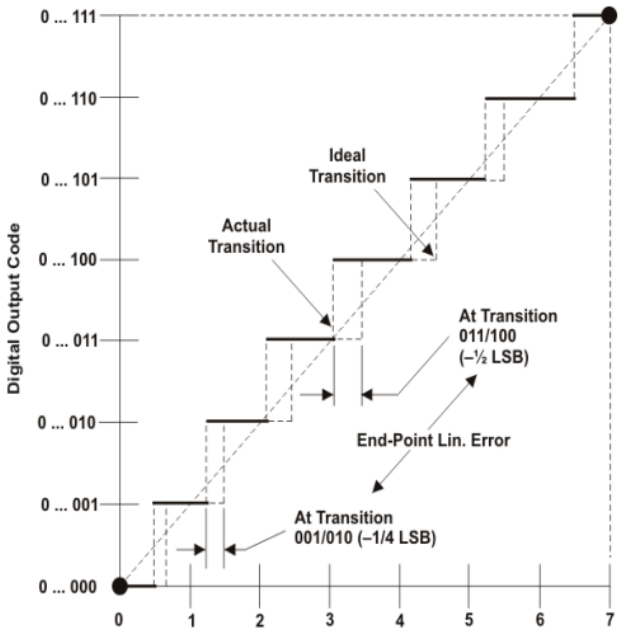


Figure 6 ADC with INL [5]

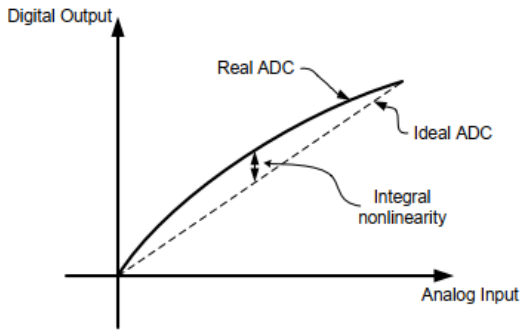


Figure 7 ADC with INL [5]

Dynamic Characteristics:

1. Signal to Noise Ratio (SNR): It is the ratio between the power of the signal and the total noise produced by quantization and the noise of the circuit. If only the quantization noise is accounted for, the SNR could be calculated from Equation 3 where it demonstrates that when the number of bits (n) increases, the system SNR increases. Usually, distortion power is added to the total noise power to get the signal to noise and distortion ratio (SNDR).

$$SNR_{dB} = 6.02n + 1.76 \qquad Eq.3$$

2. Dynamic Range (DR): It is defined as the maximum tolerable signal power divided by the minimum detectable signal power.
3. Effective Number of Bits (ENOB): It is the effective resolution of the system. From Equation 4, the effective number of bits could be determined by substituting ideal SNR (quantization noise only) with SNDR as SNDR accounts effectively for all the noise and distortion introduced.

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \qquad Eq.4$$

4. Total Harmonic Distortion (THD%): It is the ratio of the total harmonic distortion power to the signal power at the fundamental frequency. Due to the infinite number of harmonics, usually, the first 10-20 harmonics are only included in the calculation of the THD%.
5. Spurious Free Dynamic Range (SFDR): It is the ratio of the RMS voltage of the input signal to the RMS value of the largest spur, measured using FFT in the frequency domain as shown in Figure 8.

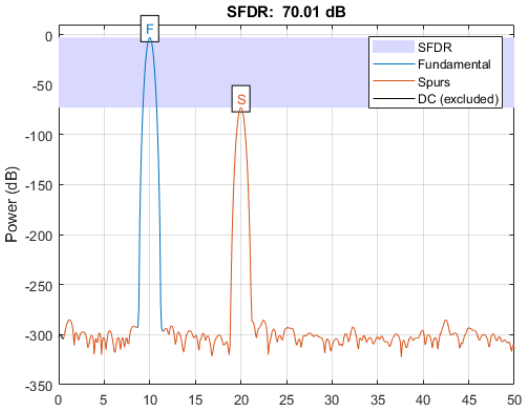


Figure 8 An example of SFDR [6]

2.2 Different Architectures of ADCs

ADCs are divided into two categories, Nyquist Rate ADCs and oversampling ADCs.

2.2.1 Nyquist Rate ADCs

2.2.1.1 Flash ADC

In Flash ADC, the input analog voltage is compared with $2^n - 1$ reference voltage levels using $2^n - 1$ comparator where n is the number of bits desired for the ADC. Using 2^n series resistors, the reference voltage levels are generated using the resistors as voltage dividers as shown in Figure 9. The inputs of each comparator are the input voltage and the reference voltage at this level. The output of each comparator is either 1 or 0 based on the input voltage whether it is higher or lower than the reference voltage. The generated $2^n - 1$ output is called the thermometer code which is then decoded to n bit binary code by a suitable decoder. Since the input voltage is fed to all the comparators at once, the conversion time is crucially small where it depends only on the delay of one comparator and the delay of the few gates in the decoder. Therefore, the Flash ADC is considered one of the fastest ADCs [4]. On the other hand, due to requiring a large number of comparators and resistors, the area and power consumption is large and the resolution is limited to 8 bits (255 comparators) [7]. Furthermore, a power-hungry buffer is required at the input terminal as the large number of comparators add large parasitic capacitances [7]. In conclusion, Flash ADCs are suitable for applications that require high frequency and large bandwidth regardless of the cost, power consumption, and area of the ADC; for instance, satellite communication and radar systems [8].

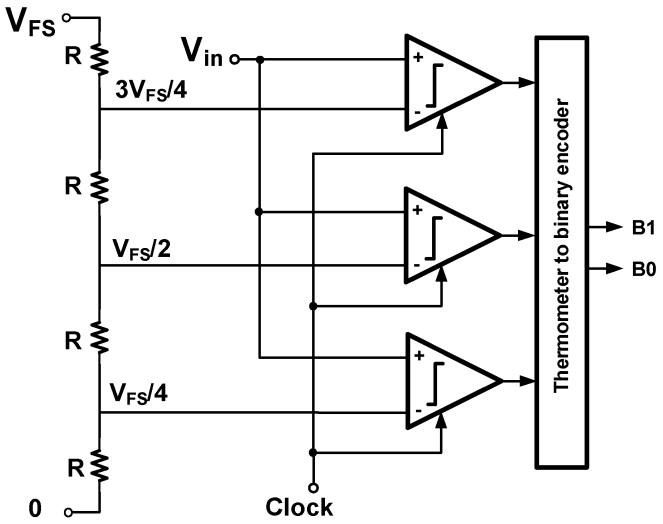


Figure 9 Flash ADC

2.2.1.2 SAR ADC

SAR ADC mainly performs a binary search through possible quantization levels by iteratively comparing the input voltage to the voltage corresponding to the binary representation until converging to the closest one to the input [9]. Figure 10 demonstrates a SAR ADC where it consists of a sample and hold block (S/H), SAR, DAC, and comparator. The conversion process iteratively determines one bit each clock cycle starting by the most significant bit (MSB). The iterative process starts with the SAR setting the bit to 1. Then, the DAC converts this binary representation, using a reference voltage, to the corresponding voltage using Equation 5. Then, the comparator compares the input voltage with the voltage from the DAC. Depending on the output of the comparator, the bit is determined to be 1 or 0. The process is then repeated until the least significant bit (LSB) is reached. Figure 11 demonstrates the waveform of a 3-bit SAR ADC to illustrate the operation and the converging of the output binary representation to the input voltage. Since one clock cycle is needed to sample the input voltage with S/H, the n-bit conversion requires $n + 1$ clock cycles. As a result, the SAR ADC is considered to have medium speed limited to $5\ Msps$ [10]. However, the simple design of SAR ADC lowers the power consumption and cost while maintaining high accuracy and fairly high resolution [10]. In addition, SAR ADCs are compatible with technology scaling as the comparator is the only analog component in the design [10].

$$V_{DAC} = V_{FS}\left(\frac{D_0}{2^N} + \frac{D_1}{2^{N-1}} + \cdots + \frac{D_{N-1}}{2}\right) \quad Eq.5$$

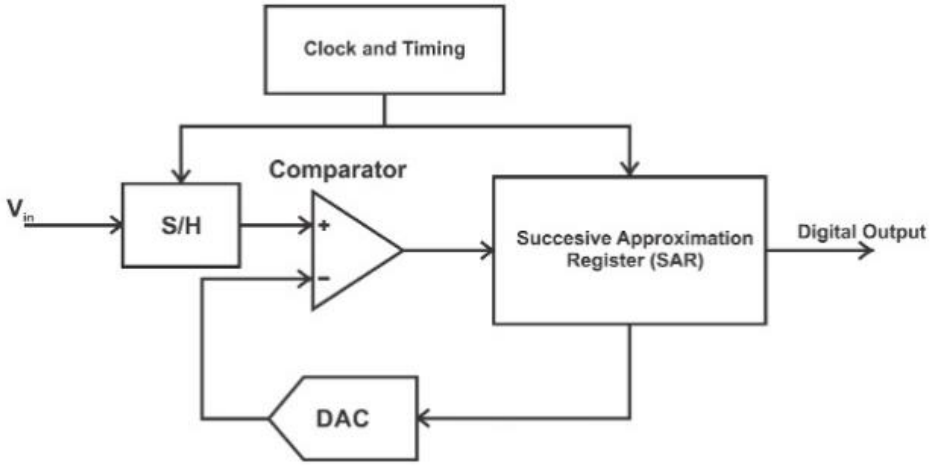


Figure 10 SAR ADC

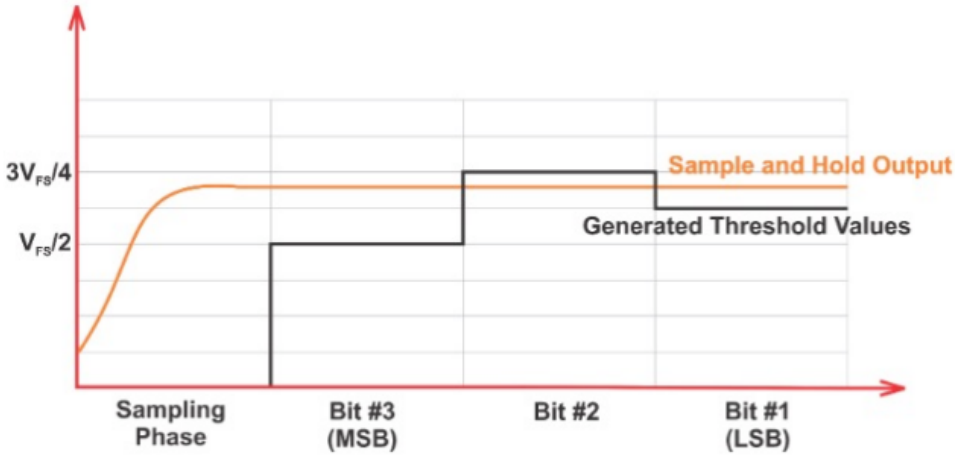


Figure 11 Waveform of a 3-bit SAR ADC

2.2.2 Oversampling ADCs

Oversampling ADCs sample at a frequency higher than the Nyquist rate. The oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{2f_{BW}} \quad Eq.6$$

f_s is the sampling frequency and f_{BW} is the bandwidth frequency expressed as $f_{BW} = f_2 - f_1$.

Oversampling ADCs have two advantages over Nyquist rate ADCs:

A. Relaxing the requirements of the anti-aliasing filter (AAF)

For Nyquist-rate ADCs, the bandwidth of the signal coincides with $\frac{f_s}{2}$, resulting in the need for an anti-aliasing filter with a very sharp transition (many poles) as shown in Figure 12(a), to be able to remove the out-of-band components. However, as $\frac{f_s}{2} > BW$ for oversampling ADCs then the signal replicas are further apart from the signal compared to the Nyquist-rate ADC's case, resulting in more relaxed requirements of the AAF as shown in Figure 12(b).

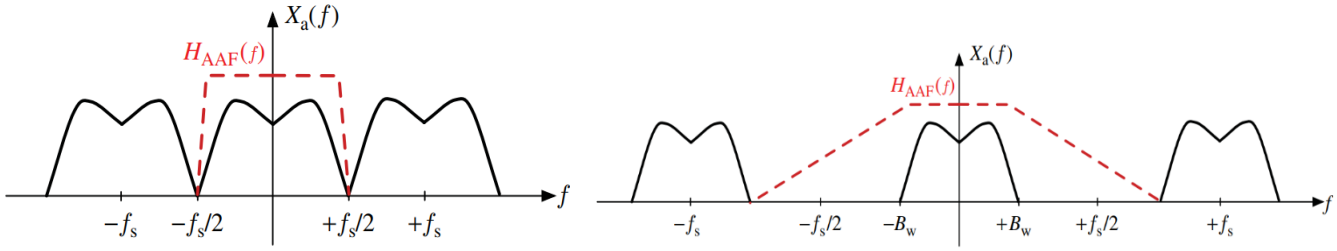


Figure 12 AAF for a) Nyquist Rate ADCs, b) Oversampling ADCs

B. Higher signal to quantization noise ratio (SQNR)

Assuming the quantization step is Δ and the quantization noise is distributed evenly between $\frac{\Delta}{2}$ and $-\frac{\Delta}{2}$, the quantization noise power can be expressed as

$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2\, de = \frac{\Delta^2}{12} \quad Eq.7$$

The quantization noise power folds in the range [0, $\frac{f_s}{2}$]. Dividing the quantization noise power by this range and assuming the quantization noise is white noise, the quantization noise density can be written as

$$N_q = \frac{2}{f_s} . e_{rms}^2 \quad Eq.8$$

The in-band noise between f_2 and f_1 is

$$n_{band}^2 = \int_{f_1}^{f_2} N_q \;\; df = \frac{2}{f_s} . e_{rms}^2 . f_{BW} = \frac{e_{rms}^2}{OSR} \quad Eq.9$$

Equation 9 illustrates that the quantization noise in the required band can be reduced by increasing the sampling frequency trading speed for resolution [11].

2.2.2.1 Sigma-Delta ADC:

The conversion process in a Sigma-Delta ADC mainly depends on the quantization of the change of the input voltage from a sample to sample rather than the absolute value at each sample. As well, the quantization resolution is improved by the feedback using 1-bit DAC. In addition to oversampling, Sigma-Delta ADCs utilize a combination of feedback and filtering to shape the quantization noise spectrum.

Noise Shaping

The goal is to suppress the in-band noise to achieve a higher SNR. Figure 13 shows the block diagram of the modulator. Assuming a linear model for the quantization error the block diagram redrawn as Figure 14. From the linearized model, the output is the sum of the input signal multiplied by the signal transfer function (STF) and the error signal multiplied by the noise transfer function (NTF) as in Equations 10 and 11.

$$V(z) = STF(z)U(z) + NTF(z)E(z) \qquad Eq.10$$

$$V(z) = \frac{L_0(z)}{1 - L_1(z)}U(z) + \frac{1}{1 - L_1(z)}E(z) \qquad Eq.11$$

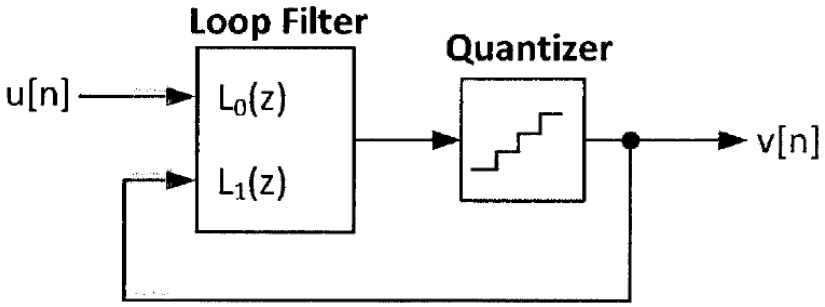


Figure 13 Block Diagram of Sigma-Delta Modulator

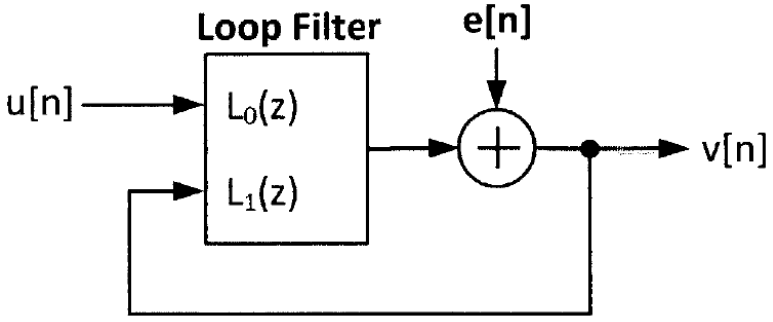


Figure 14 Updated Block Diagram of Sigma-Delta Modulator

Where STF and NTF are not equal and thus, the signal and the quantization noise are filtered in different ways. By adjusting $L_0(z)$ and $L_1(z)$, the in-band noise can be filtered out without affecting the signal spectrum. This is achieved by making $L_1(z)$ a bandpass filter which makes the NTF a band-stop filter [12].

Discrete-time (DT) and Continuous-Time (CT) Sigma-Delta modulator

Discrete-time Sigma-Delta modulator processes the signal entirely in the discrete domain. Therefore, it requires the use of a proceeding AAF and an S/H circuit. The transfer function of the DT loop filter can be derived from the desired NTF as

$$L_1(z) = 1 - \frac{1}{NTF(z)} \qquad Eq.12$$

Since $L_0(z)$ and $L_1(z)$ are implemented with the same hardware, once $L_1(z)$ is determined, $L_0(z)$ is determined as well and the STF becomes

$$STF(z) = L_0(z)\, NTF(z) \quad Eq.13$$

This DT loop filter is usually implemented by switching capacitor circuits. However, in order to achieve the required gain and bandwidth specifications, the Op-Amps of the filter end up with a settling time that does not allow high sampling frequencies. This is due to the fact that the Op-Amps are required to settle in half the sampling period for adequate functionality [12].

2.3 Loop Filter Design

The needed band-pass filter is implemented by a resonator. Conventionally either an LC tank resonator or a biquadratic resonator are used. However, a single Op-Amp is superior to both designs because it achieves a smaller area, lower noise, and lower power.

A. LC tank

A conventional LC tank resonator can be used in the filter. It provides low power low noise and high quality factor (Q). However, its area tends to be large due to the passive components, especially the inductors. With an LC tank resonator, only one summing node is available. Regardless, two DACs are needed for the feedback loop as shown in Figure 15, one of them is a return-to-zero-DAC (RZ DAC) and the other is a half-clock-delayed-return-to-zero DAC (HZ DAC). These DACs are used to map the DT transfer function to the CT transfer function of the filter.

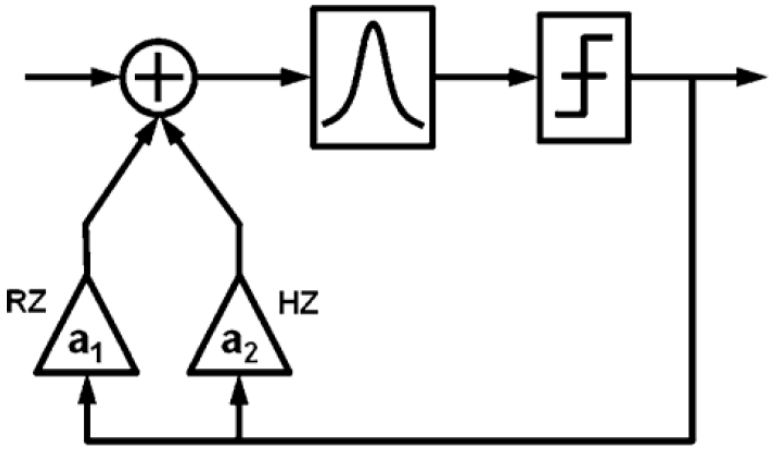


Figure 15 LC Tank

B. Biquadratic resonator

A biquadratic resonator consists of two integrators in a loop. Since the integrators are made of mainly active components, this resonator requires less area because it does not utilize large inductors. However, each integrator requires an Op-Amp. The two Op-Amps per resonator consume a lot of power and contribute to thermal noise to the system. The biquadratic resonator in Figure 16 has two summing nodes. One non-return-to-zero DAC (NZ DAC) is connected to each node.

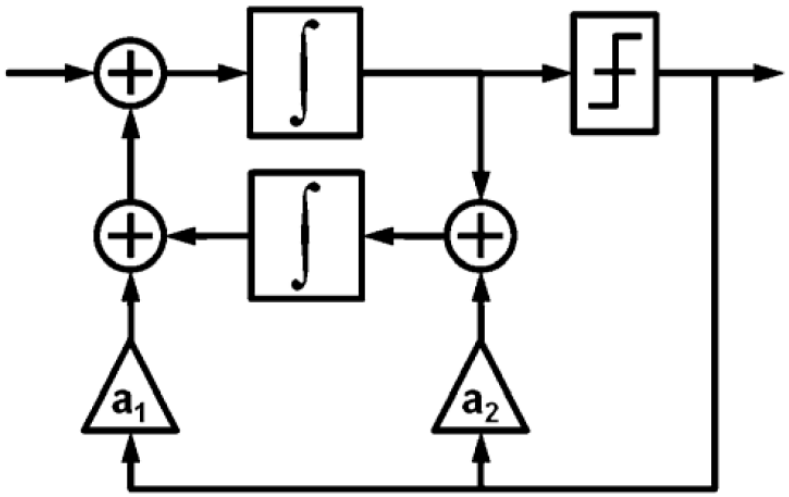


Figure 16 Biquadratic Resonator

C. Single Op-Amp resonator

This design utilizes a single Op-Amp resonator for the band-pass filter. This resonator achieves a relatively small area and utilizes only one Op-Amp per resonator which reduces the noise added to the system and the power needed for a specific noise requirement [13].

2.4 DAC Design

The DAC converts the digital output to an analog signal and feeds it back to the input of the filter. The DAC is critical because any non-linearity in its performance appears as distortion components in the output. DACs can be resistive, capacitive, or current steering.

Resistive and Capacitive DACs:

In resistive and capacitive DACs switches determine the output voltage and an output buffer is needed to provide a sufficient drive. As a result, their performance is limited by the speed of the switching and the output buffer.

Current Steering DACs:

The current steering DAC, on the other hand, redirects the current instead of switching it on and off and can directly drive the load without the need for an output buffer. As a result, it achieves the highest speed. The current steering DAC consists of an array of identical current sources, the input code switches them to either the positive output terminal or the negative output terminal depending on the input code. The redirection is achieved by a pair of complementary switches applied to a differential pair as shown in Figure 17 [14].

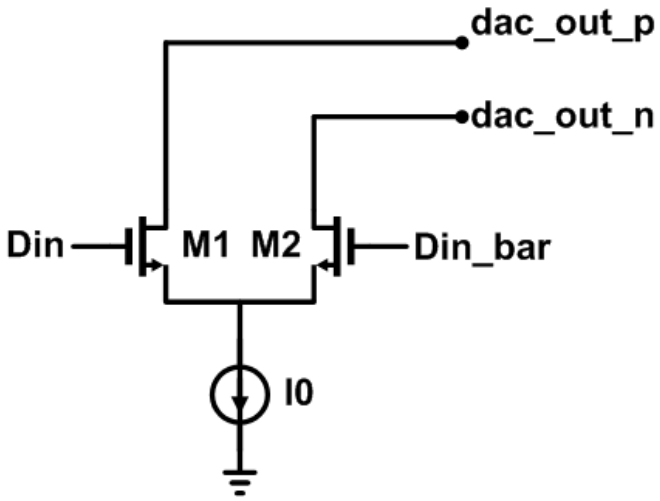


Figure 17 Current Steering DAC [14]

Chapter 3

3.1 Project Purpose

Generate the transistor level design of a $800MS/s$ second-order continuous-time bandpass sigma-delta (CTBPSD) ADC with a bandwidth of $6.25MHz$ at $200MHz$ center frequency. The ADC needs to achieve a high SNR value and low power consumption.

3.2 Project Technical Specifications

A $800MS/s$ second-order CTBPSD ADC with a bandwidth of $6.25MHz$ at $200MHz$ center frequency that employs single Op-Amp resonator as a loop filter to enhance its power efficiency is to be designed using $65nm$ CMOS process technology, with a supply of $1.2V$.

3.3 Description of the Selected Design

The system architecture is shown in Figure 18, where a single Op-Amp resonator is used to enhance the power efficiency and is followed by a high pass filter to drive resistive loads without degrading the time constant and thus quality factor. Two current-steering DACs are used in the feedback loop for noise-shaping. To compensate for the timing differences between the DACs and the comparator, a clock delay is implemented using Positive-edge triggered flipflop and negative latch.

The sampling frequency of the system is $800MHz$, and the center frequency is $200MHz$. The OSR of the Sigma-Delta modulator is 64 so that the bandwidth is $6.25MHz$. The modulator achieves an ideal SNR of $56.9\ dB$.

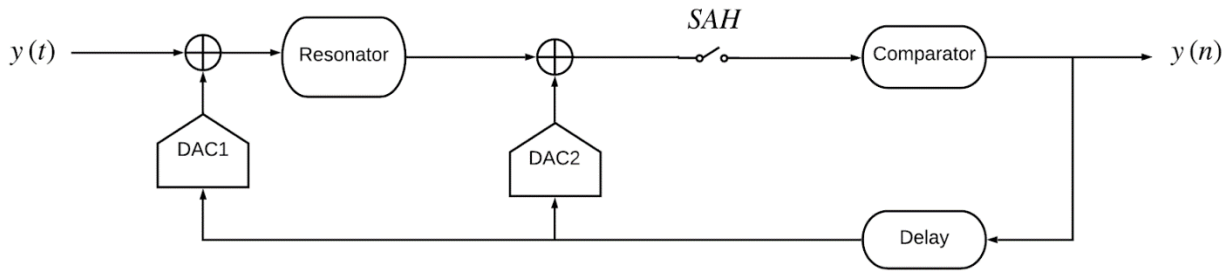


Figure 18 2nd Order CTBPSD ADC system Architecture

3.4 Block Diagram and Functions

The system consists mainly of an anti-aliasing loop filter, 1-bit quantizer, and DAC as shown in Figure 19.

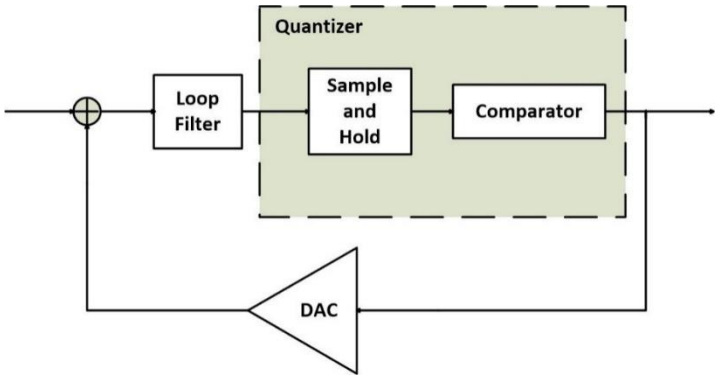


Figure 19 System Block Diagram

3.4.1 Loop Filter

The loop filter shapes the quantization noise by appearing in the denominator of the NTF. In this ADC, the NTF needs to be a band-stop function around the center frequency to reduce the quantization noise at that frequency and improve the SNR. For this purpose, the loop filter needs to be a band-pass filter which is accomplished by a second-order resonator as shown in Figure 20. The resonator is a differential single Op-Amp resonator with a center frequency of $200\ MHz$.

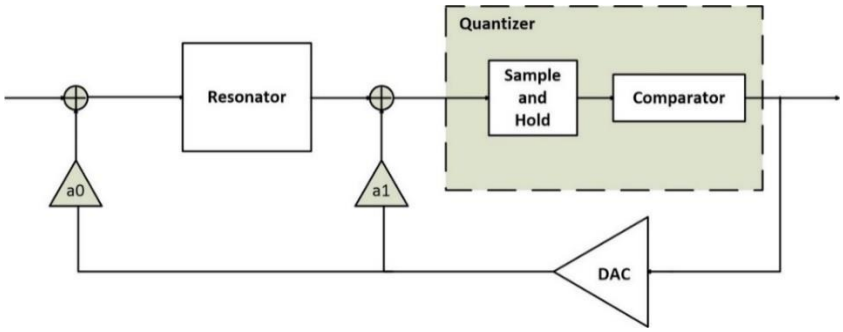


Figure 20 2nd order Resonator as Loop Filter

3.4.2 Quantizer

The quantizer is realized by an S/H circuit followed by a comparator. The S/H samples the analog output of the loop filter at a sampling frequency of $800MHz$. The comparator alternates between 1 and -1.

3.4.3 Feedback DAC

The DAC mainly feedbacks the digital output signal as an analog signal to be compared to the input signal and the difference is processed by the resonator. As the loop filter is a second-order resonator, two current-mode DACs are realized.

Chapter 4

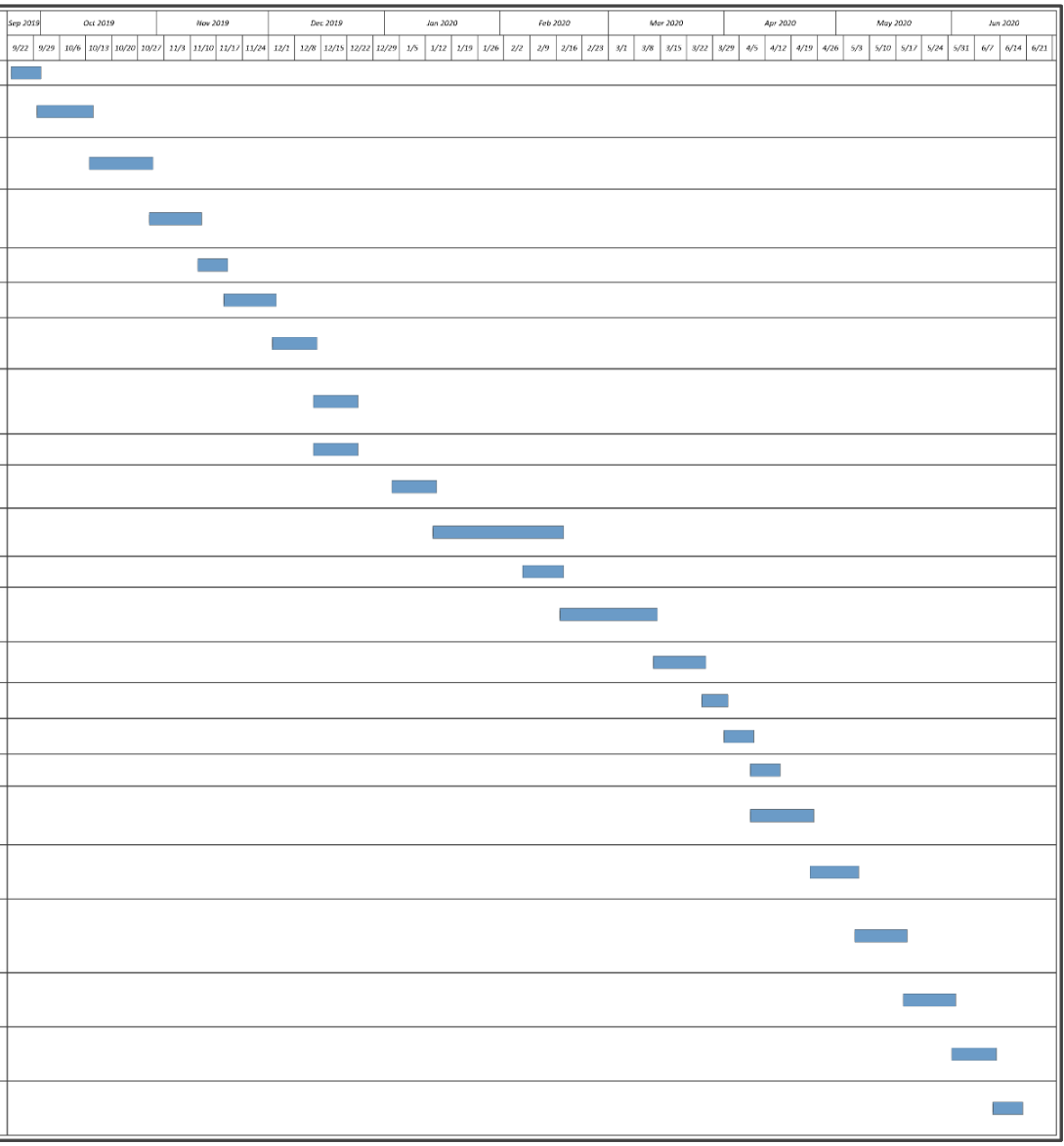
4.1 Project Tasks and Gantt Chart

The project includes the following tasks:

- The implementation of the system on Simulink and simulating it using MATLAB.
- The derivation of the analytical non-ideal transfer function of the Resonator and incorporating it into the MATLAB model.
- Extracting the specifications (Gain and Bandwidth) of the Op-Amp from the MATLAB model.
- The Design and implementation of the single Op-Amp resonator using Cadence Virtuoso to achieve a high quality factor ($Q > 400$) and a center frequency of $200MHz$.
- The implementation of the system using VerilogA macro models on Cadence Virtuoso and its optimization to achieve the required specs.
- Scaling of the coefficients of the DACs along with the input amplitude to ensure that the resonator's output swing does not exceed the supply.
- The implementation of the 3-stage feedforward-compensated Op-Amp (with a gain of $43dB$ and BW of $300MHz$) with $65nm$ technology on Cadence Virtuoso.
- The implementation of the 4-stage feedforward-compensated Op-Amp (with a gain of $60dB$ and BW of $325MHz$) with $65nm$ technology on Cadence Virtuoso.
- The design of the common-mode feedback amplifier (5T-OTA) to control the common mode of the output for both the third and fourth stages.
- The adjustment of the resistors' and capacitors' value to accommodate for the parasitic resistances and capacitances for both the 3-stage and 4 stage feedforward-compensated Op-Amps to achieve a high quality factor along with an accurate center frequency of $200MHz$ for the resonator.
- The implementation of current steering DACs with the specs extracted from the system level simulations using Cadence Virtuoso.
- The implementation of the StrongArm Comparator and SR latch with $65nm$ technology on Cadence Virtuoso.
- Integration of the whole system and performing post-layout simulations.

Gantt Chart

ID	Task Name	Start	Finish	Duration
1	Investigation of the problem	9/23/2019	9/30/2019	1w 1d
2	Conducting Literature Review about ADCs architectures, Performance Metrics, and their comparison.	9/30/2019	10/14/2019	2w 1d
3	Literature Review about Sigma-Delta ADCs and its types 1. CT, DT 2. LP, BP	10/14/2019	10/30/2019	2w 3d
4	Implementation of the LPCT Sigma-Delta ADC using ideal macromodels in Cadence Virtuoso and measuring its performance.	10/30/2019	11/12/2019	2w
5	Literature Review about the DAC Designs and Loop filter Designs	11/12/2019	11/19/2019	1w 1d
6	Implementation of the BPCTSD system using Simulink	11/19/2019	12/2/2019	2w
7	Derivation of the analytical Non-ideal TF of the resonator and incorporating it into the Simulink Model.	12/2/2019	12/13/2019	2w
8	Design and implementation of the single opamp resonator using Cadence virtuoso with a center frequency of 200MHz ad A> 400.	12/13/2019	12/24/2019	1w 3d
9	Extracting the specs of the opamp (Gain and BW) from the MATLAB model.	12/13/2019	12/24/2019	1w 3d
10	The implementation of the system using Verilog-A macromodels in Cadence Virtuoso.	1/3/2020	1/14/2020	1w 3d
11	Scaling of the Coefficients of the DACs along with the input amplitude and extracting the DAC's specs.	1/14/2020	2/17/2020	5w
12	Literature Review about the Feedforward-Compensated Opamp	2/7/2020	2/17/2020	1w 2d
13	Design of 3 stage Feedforward Opamp in Cadence Virtuoso using 65nm technology, and development of its testbench.	2/17/2020	3/13/2020	4w
14	Design of 4 stage Feedforward Opamp in Cadence Virtuoso using 65nm technology.	3/13/2020	3/26/2020	2w
15	Design of CMFB amplifier (5T-OTA) in Cadence Virtuoso using 65nm technology.	3/26/2020	4/1/2020	1w
16	Adjustment of the resonator for the 3 stage and 4 stage FF opamp	4/1/2020	4/8/2020	1w 1d
17	Integration of both the 3 stage and 4 stage FF opamp into the system.	4/8/2020	4/15/2020	1w 1d
18	The implementation of conventional and strongArm Comparators using Cadence Virtuoso and comparing their performance.	4/8/2020	4/24/2020	2w 3d
19	The implementation of two current-steering DACs with Specs extracted from Cadence.	4/24/2020	5/6/2020	1w 4d
20	The integration of the transistor-level FeedForward Opamp, DAC and comparator into the system and extracting the delay requirements of the system.	5/6/2020	5/19/2020	2w
21	Implement the transistor-level Design of D-flipflop	5/19/2020	6/1/2020	2w
22	Integration of the whole system and its simulation	6/1/2020	6/12/2020	2w
23	Writing the thesis and preparing the presentation	6/12/2020	6/19/2020	1w 1d



4.2 Description of Each Subsystem

4.2.1 Single Op-Amp Resonator

A typical resonator will have an active or passive low pass filter (LPF) followed by an active or passive high pass filter (HPF). For this resonator, an active LPF (Figure 21) is followed by a passive HPF (Figure 22). The transfer function (TF) of the resonator in Figure 23 is

$$H(s) = k_0 \frac{\omega_0 s}{s^2 + 2\omega_0 s + \omega_0^2} \qquad Eq.14$$

Where $\omega_0 = 1/R_p C_p = 1/R_n C_n \quad Eq.15$

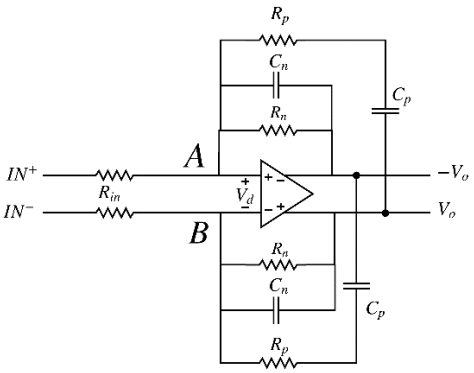


Figure 21 LPF

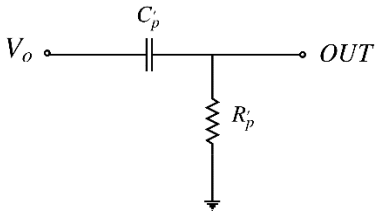


Figure 22 HPF

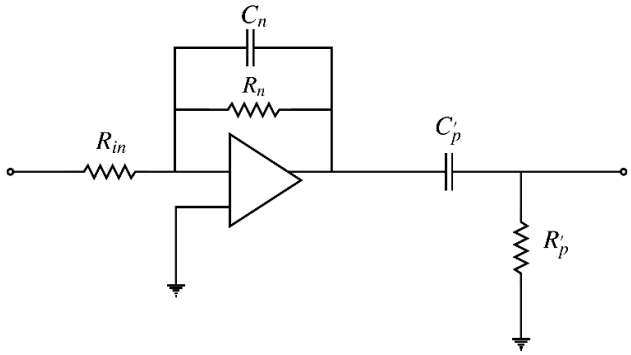


Figure 23 Resonator

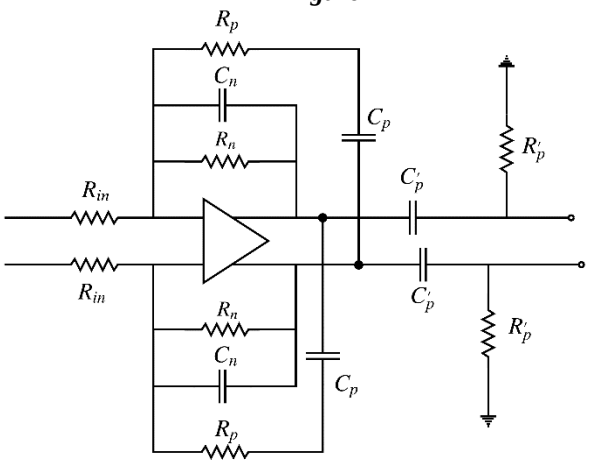


Figure 24 Resonator with differential setup

The first-order term in the numerator determines the quality factor. Adding positive feedback through the differential setup in Figure 24 results in

$$H(s) = k_0 \frac{\omega_0 s}{s^2 + k\omega_0 s + \omega_0^2} \qquad Eq.16$$

Where ω_0 is from Equation 15 and

$$k = R_n C_n + R_p C_p - R_n C_p \quad Eq.17$$

The resistances and capacitances are chosen to make $k = 0$ for the maximum quality factor.

4.2.1.1 Resonator with ideal Op-Amp

For the LPF in Figure 21, using nodal analysis at node A

$$\frac{V_d - IN^+}{R_{in}} + \frac{V_d - (-V_o)}{\frac{R_n}{sC_nR_n + 1}} + \frac{V_d - V_o}{\frac{sC_pR_p + 1}{sC_p}} = 0$$

$$V_d\left(\frac{1}{R_{in}} + \frac{sC_nR_n + 1}{R_n} + \frac{sC_p}{sC_pR_p + 1}\right) + V_o\left(\frac{sC_nR_n + 1}{R_n} - \frac{sC_p}{sC_pR_p + 1}\right) = \frac{IN^+}{R_{in}} \quad Eq.18$$

Now, doing the same at node B

$$\frac{-V_d - IN^-}{R_{in}} + \frac{-V_d - V_o}{\frac{R_n}{sC_nR_n + 1}} + \frac{-V_d - (-V_o)}{\frac{sC_pR_p + 1}{sC_p}} = 0$$

$$-V_d\left(\frac{1}{R_{in}} + \frac{sC_nR_n + 1}{R_n} + \frac{sC_p}{sC_pR_p + 1}\right) - V_o\left(\frac{sC_nR_n + 1}{R_n} - \frac{sC_p}{sC_pR_p + 1}\right) = \frac{IN^-}{R_{in}} \quad Eq.19$$

Subtracting Equation 19 from 18

$$V_d\left(\frac{1}{R_{in}} + \frac{sC_nR_n + 1}{R_n} + \frac{sC_p}{sC_pR_p + 1}\right) + V_o\left(\frac{sC_nR_n + 1}{R_n} - \frac{sC_p}{sC_pR_p + 1}\right) = \frac{IN}{2\,R_{in}} \quad Eq.20$$

For the ideal Op-Amp $V_d = 0$

$$V_o\left(\frac{sC_nR_n + 1}{R_n} - \frac{sC_p}{sC_pR_p + 1}\right) = \frac{IN}{2\,R_{in}}$$

$$\frac{V_o}{IN} = \frac{R_n}{2R_{in}}\,\frac{sC_pR_p + 1}{s^2C_nR_nC_pR_P + s\left(C_nR_n + C_pR_p - C_pR_n\right) + 1}$$

$$\frac{V_o}{IN} = Q\,\frac{\omega_0\,(s + \omega_0)}{s^2 + s\,k\,\omega_0 + \omega_0^2} \quad Eq.21$$

Where k is from Equation 17, ω_0 from Equation 15 and

$$Q = \frac{R_n}{2R_{in}} \quad Eq.22$$

For the HPF in Figure 22,

$$\frac{OUT}{R_p'} = \frac{V_o}{\frac{1}{sC_p'} + R_p'} = \frac{sC_p'R_p'}{sC_p'R_p' + 1}$$

$$\frac{OUT}{V_o} = \frac{s}{s + \omega_0} \quad Eq.23$$

Where $\omega_0 = 1/R_p'C_p' = 1/R_pC_p = 1/R_nC_n \quad Eq.24$

By multiplying Equation 21 by Equation 23, we get the TF of the single Op-Amp resonator with an ideal Op-Amp

$$\frac{OUT}{IN} = Q\ \frac{\omega_0 s}{s^2 + k\omega_0 s + \omega_0^2} \qquad Eq.25$$

By setting $k = 0$, the TF of an ideal resonator is obtained

$$\frac{OUT}{IN} = Q\ \frac{\omega_0 s}{s^2 + \omega_0^2} \qquad Eq.26$$

4.2.1.2 Resonator with non-ideal Op-Amp

For the non-ideal Op-Amp, starting from Equation 20 and knowing that

$$V_o = \frac{A_0}{2\left(1 + \frac{s}{p}\right)}\ V_d \cong \frac{A_0}{\frac{2s}{p}}\ V_d \qquad Eq.27$$

Where, A_0 is the DC gain and p is the dominant pole of the non-ideal Op-Amp.

Then, by setting k from Equation 17 to equal 0, we get Equation 28.

$$\frac{2s}{A_0\ p} V_0 \left(\frac{1}{R_{in}} + \frac{sC_nR_n + 1}{R_n} + \frac{sC_p}{sC_pR_p + 1}\right) + V_o \left(\frac{sC_nR_n + 1}{R_n} - \frac{sC_p}{sC_pR_p + 1}\right) = \frac{IN}{2\ R_{in}}$$

$$\frac{V_o}{IN} = \frac{\frac{R_n}{2R_{in}}\left(sC_pR_p + 1\right)}{\frac{2s}{A_0p}\frac{R_n}{R_{in}}\left(sC_pR_p + 1\right) + \left(sC_pR_p + 1\right)(sC_nR_n + 1)\left(\frac{2s}{A_0p} + 1\right) + sR_nC_p\left(\frac{2s}{A_0p} - 1\right)}$$

$$\frac{V_o}{IN} = Q\frac{\omega_0(\omega_0 + s)}{s^3\frac{2}{A_0p} + s^2\left(1 + \frac{4}{A_0p}\omega_0(2 + Q)\right) + \frac{2\omega_0^2}{A_0p}\ (1 + 2\ Q) + \omega_0^2} \qquad Eq.28$$

Where ω_0 from Equation 24 and Q from Equation 22.

As in the ideal case, the TF of HPF in Equation 23 is multiplied by Equation 28 resulting in the final TF of this resonator with the non-ideal Op-Amp

$$\frac{OUT}{IN} = Q\frac{\omega_0 s}{s^3\frac{2}{A_0p} + s^2\left(1 + \frac{4}{A_0p}\omega_0(2 + Q)\right) + \frac{2\omega_0^2}{A_0p}\ (1 + 2\ Q) + \omega_0^2} \qquad Eq.29$$

4.2.2 Operational Amplifier (Op-Amp) Design

Design Considerations of the Op-Amp

The Op-Amps used for CT ΔΣ ADCs need to have the following requirements to achieve the design specifications:

- High in-Band Loop Gain: To achieve a high quality factor and an accurate center frequency for the resonator in the system, the Op-Amp needs to have a high gain within the signal band ($\approx 60-70dB$) when it is loaded with both resistive and capacitive impedances [15].
- Fast settling of the Op-Amp so that the input harmonics are not introduced to the output and accordingly the SNDR is not degraded. This is translated to the Op-Amp having a gain-bandwidth product that is 3-5 times the sampling rate of the ADC [16].

Typical Amplifier Topologies

1. Telescopic Cascode Amplifier

This single-stage topology (as shown in Figure 25) can achieve a moderately high DC gain by using a cascode of transistors ($\approx 4-5$) and great dynamic behavior with excellent power efficiency due to having one current branch only; however, the output swing is greatly reduced due to the stacking making it extremely difficult to use this design in the implementation of low-voltage ΔΣ ADCs [17].

2. Folded Cascode Amplifier

This single-stage topology shown in Figure 26 is also capable of achieving a moderately high DC gain with a better output swing than that of the telescopic cascode due to reducing the number of stacked transistors. However, the power consumption is doubled due to having two current branches and its phase margin and non-dominant pole are lower than that of the telescopic cascode [17]. However, the Op-Amp used in this system of CT ΔΣ ADC is both capacitively and resistively loaded rendering all of the single-stage topologies as inadequate due to their limited gain with resistive loads [15].

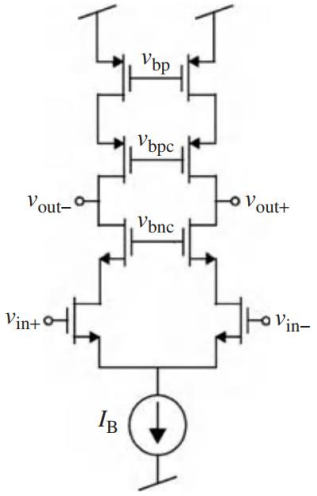


Figure 25 Telescopic Cascode Op-Amp

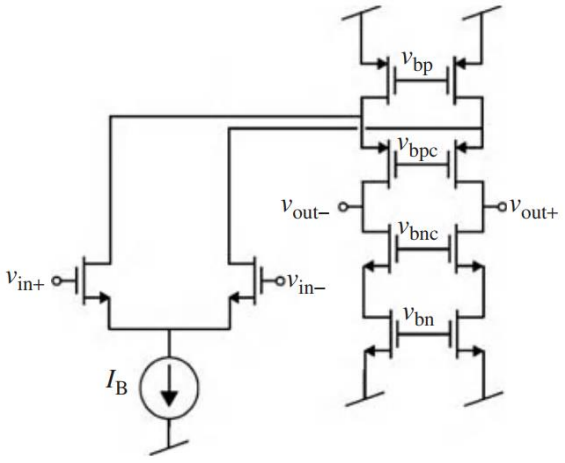


Figure 26 Folded Cascode Op-Amp

3. Two-stage amplifier with Miller Compensation

This amplifier, shown in Figure 27, is capable of achieving both high DC gain and large output swing due to the cascading of the amplification stages rather than the stacking (cascoding). However, the cascading introduces additional poles to the system which degrades the overall phase margin of the amplifier. One of the most commonly used phase-compensation schemes is the Miller Compensation technique, in which the dominant pole is pushed into lower frequencies due to the pole splitting effect of the Miller capacitor, which leads to the Op-Amp having a lower bandwidth. Also, this introduces an RHP zero that requires a nulling resistor to cancel its effects [17, 18].

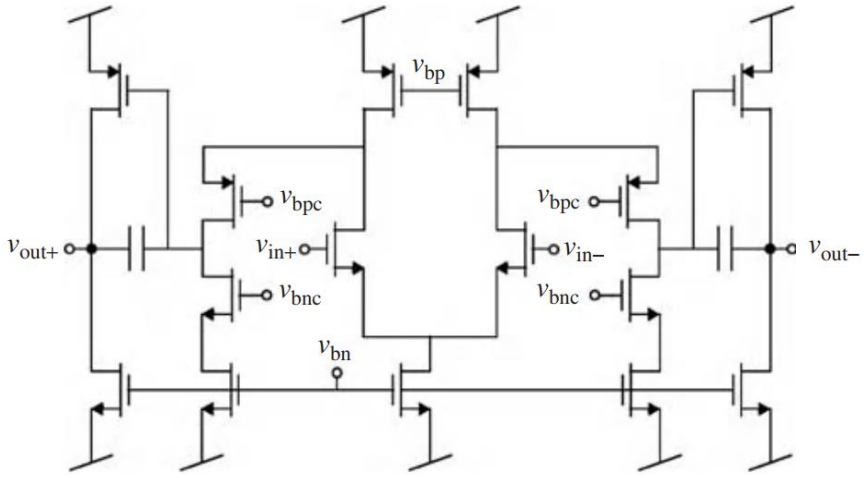


Figure 27 Two-stage Miller-Compensated Op-Amp

4. Multi-stage feedforward Amplifier:

Each stage of a multistage amplifier introduces a low-frequency pole which results in a negative phase shift and degrades the phase margin. In this topology, the feedforward path generates an LHP zero for each stage after the first. The positive phase shift of the zeros compensates the negative phase shift of the poles generated by the second to last stages.

Figure 28 shows a two-stage amplifier with a feedforward path. Each stage is assumed to have the single-pole response shown in Equation 30 where A is the DC gain and ω_p is the pole.

$$H(s) = \frac{A}{1 + \frac{s}{\omega_p}} \quad Eq.30$$

The DC gain and the poles can be written as follows,

$$A_i = \frac{g_{mi}}{g_i} \quad i = 1,2,3 \quad Eq.31$$

$$\omega_{pi} = \frac{g_i}{C_i} \quad i = 1,2,3 \quad Eq.32$$

Through the connection shown in Figure 29, the feedforward path has the same pole as the second stage and does not add any new ones. The transfer function of the amplifier becomes as follows,

$$H(s) = \frac{A_1\,A_2}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} + \frac{A_3}{\left(1+\frac{s}{\omega_{p2}}\right)}$$

$$H(s) = \frac{(A_1 * A_2 + A_3)\left(1+\frac{A_3\,s}{(A_1\,A_2+A_3)\,\omega_{p1}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \qquad Eq.33$$

The DC gain equals $A1 * A2 + A3$ and the dominant pole is the pole of the first stage ω_{p1}. The LHP zero generated by the feedback path is at

$$z = -\omega_{p1}\left(1+\frac{A_1\,A_2}{A_3}\right) \cong -\frac{g_{m1}\,g_{m2}}{C_1\,g_{m3}} \qquad Eq.34$$

As a result, this topology provides a high gain with an improved bandwidth [18].

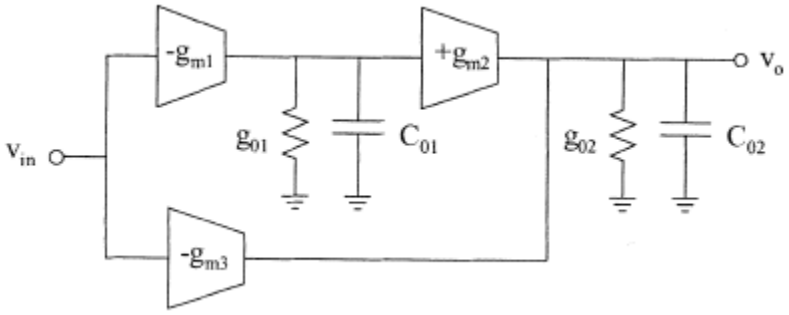


Figure 28 two-stage amplifier with a feedforward path

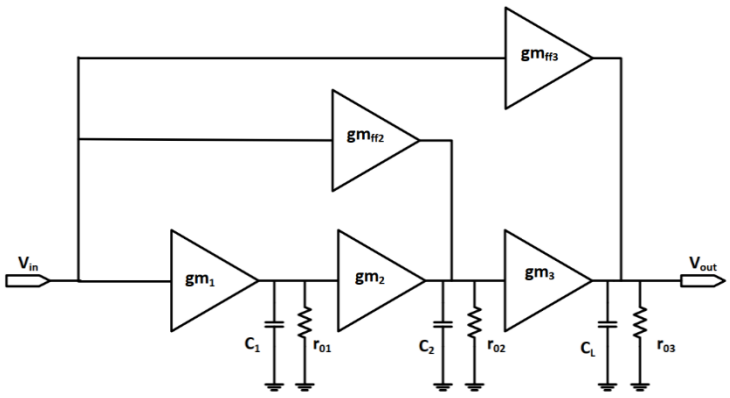


Figure 29 3-Stage feedforward-compensated Op-Amp

Analysis of the three-stage feedforward Amplifier:

To satisfy the high gain and Bandwidth needed for the system, the three-stage feedforward Op-Amp, shown in Figure 27, was selected. The feedforward compensation schemes overcome the disadvantages of the Miller scheme by creating LHP zeros, through the feedforward paths, that have a positive phase shift and thus compensates the negative phase shift created by the poles [18]. Also, the pole-zero pairs are created at high frequencies to avoid the slow settling components resulting from them if created at low frequencies [18].

The analysis of the Op-Amp's response and the transfer function is carried out assuming a single-pole response for each of the three blocks. Where A_i denotes the DC gain of the blocks and $A_i = g_{mi}r_{oi}$ $(i = 1,2,3)$ and A_{ffj} denotes the DC gain of the blocks of the feedforward paths $(j = 2,3)$ and is calculated in the same manner, and the three poles are given by $\omega_i = 1/r_{oi}C_i$ $(i = 1,2,3)$. And the ratio between the transconductances between the direct and feedforward paths sharing an output node is given by

$$k = g_{mffi}/g_{mi} \quad Eq.35$$

The Op-Amp's transfer function is found in Equation 36.

$$\frac{V_o}{V_i} = \frac{A_1A_2A_3}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})} + \frac{A_{ff2}A_3}{(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})} + \frac{A_{ff3}}{(1+\frac{s}{\omega_{p3}})}$$

$$\frac{V_o}{V_i} = \frac{A_1A_2A_3 + A_{ff2}A_3(1+\frac{s}{\omega_{p1}}) + A_{ff3}(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})} \quad Eq.36$$

To be able to find the zeros the amplifier, some mathematical manipulation is used:

$$Numerator = A_1A_2A_3 + (A_{ff2}A_3 + A_{ff3}(1+\frac{s}{\omega_{p2}}))(1+\frac{s}{\omega_{p1}})$$

$$Numerator = A_1A_2A_3 + (A_{ff2}A_3 + A_{ff3}) * \left(1+\frac{sA_{ff3}}{(A_{ff2}A_3 + A_{ff3})\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p1}}\right) \quad Eq.37$$

Noting that $(A_{ff2}A_3 + A_{ff3}) \approx A_{ff2}A_3$, so

$$\frac{sA_{ff3}}{(A_{ff2}A_3 + A_{ff3})\omega_{p2}} = \frac{sA_{ff3}}{(A_{ff2}A_3)\omega_{p2}} = \frac{sg_{mff3}}{\frac{g_{mff2}}{C_2}g_{m3}} = \frac{s}{\omega_b} \quad Eq.38$$

Where $\omega_b = g_{mff2}/C_2k_3 \quad Eq.39$

Substituting Equation 38 in Equation 37,

$$Numerator = A_1A_2A_3 + \left(A_{ff2}A_3 + A_{ff3}\right) * \left(1 + \frac{s}{\omega_b}\right)\left(1 + \frac{s}{\omega_{p1}}\right)$$

$$= \left(A_1A_2A_3 + \left(A_{ff2}A_3 + A_{ff3}\right) * \left(1 + \frac{s}{\omega_b}\right)\right) * \left(1 + \frac{s(A_{ff2}A_3 + A_{ff3}) * (1 + \frac{s}{\omega_b}))}{\left(A_1A_2A_3 + \left(A_{ff2}A_3 + A_{ff3}\right) * \left(1 + \frac{s}{\omega_b}\right)\right)\omega_{p1}}\right)$$

$$= (A_1A_2A_3 + (A_{ff2}A_3 + A_{ff3}) * (1 + \frac{s}{\omega_b})) * (1 + \frac{s(A_{ff2}) * (1 + \frac{s}{\omega_b}))}{(A_1A_2)\omega_{p1}}$$

$$= (A_1A_2A_3 + (A_{ff2}A_3 + A_{ff3}) * (1 + \frac{s}{\omega_b})) * (1 + \frac{s(1 + \frac{s}{\omega_b}))}{\omega_a}) \approx A_1A_2A_3(1 + \frac{s(1 + \frac{s}{\omega_b}))}{\omega_a})$$

$$Numerator = A_1A_2A_3\left(1 + \frac{s}{\omega_a} + \frac{s^2}{\omega_a\omega_b}\right) \qquad Eq.37$$

Accordingly, the Op-Amp has two complex, conjugate zeros that are given by

$$\omega_z = \frac{-\omega_b \pm \sqrt{{\omega_b}^2 - 4\omega_a\omega_b}}{2} \qquad Eq.40$$

Design Procedure for the Op-Amp

Based on the analysis of the 3-stage feedforward compensated Op-Amp, the following design procedure is employed to achieve the needed specifications.

1. C_1 and C_2 are implemented entirely from the parasitic capacitances of the first and second stages to push the poles to higher frequencies.
2. To overcome the tradeoff between achieving high DC gain of the Op-Amp and pushing the zeros to lower frequencies, k (Equation 35) is chosen to equal 2 in our design.
3. Choose g_{mff3} such that g_{mff3}/C_L equals 5-7 times of the sampling frequency to ensure that the unity-gain bandwidth of the Op-Amp complying by the stringent requirement of being several times f_s.
4. Choose g_{m1} such that $g_{m1}/C_1 = 2 * f_s$ to achieve moderate gain at $f_s/2$ by pushing the zeros beyond the sampling the frequency so that the Op-Amp can handle the currents injected by the DACs at $f_s/2$.
5. After implementing the stages with transistors, the transconductances of each stage shall be adjusted to account for the parasitic capacitances to be able to achieve the required specifications.

4.2.3 DAC Design

The DAC is a modified topology of the current-steering DAC in [19]. Figure 30 demonstrates the modified topology. The design is divided into a current biasing circuit and a switching circuit. The current biasing circuit provides positive and negative currents I_+ and I_-. The switching circuit consists of 2 branches, each branch has an $NMOS$ and a $PMOS$ where each branch provides the currents to the positive and negative output terminals (OUT_P and OUT_N). The current of each terminal alternate between I_+ and I_- based on the input terminals (IN_P and IN_N) which is why this topology is chosen. IN_N is the inverse of IN_P. The basic operation is that when IN_P is HIGH, MP_2 and MN_3 are ON and MN_2 and MP_3 are OFF. As a result, I_+ flows to OUT_P and I_- is drawn from OUT_N. The vice versa occurs when IN_P is LOW. Consequently, the DAC provides the desired currents to the output terminals. To maintain that I_+ and I_- be equal, the sizing of the $PMOS$ should be $2\sim3$ times larger than the $NMOS$ to account for the difference in the mobility. The drawback is IN_p during switching from HIGH to LOW or vice versa, all the switching transistors become ON, as a result, spikes in the currents occur which increases the dynamic power.

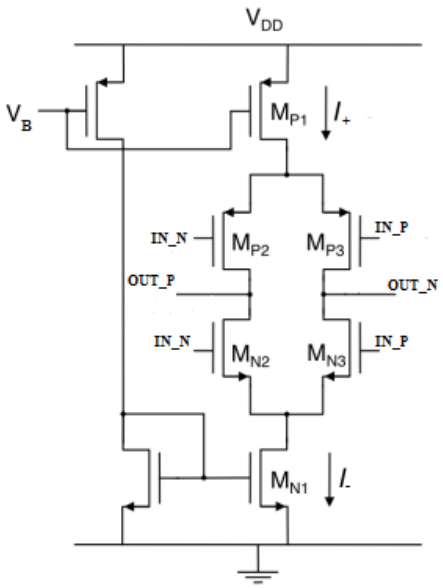


Figure 30 DAC Topology

4.2.4 Comparator Design

Topology Overview

In this work, the comparator design was based on the StrongArm topology, shown in Figure 31. Since it was first suggested by Toshiba's Kobayashi et al. [20], the topology has gained popularity due to its advantages, such as 1) zero static power consumption, 2) rail-to-rail output, and 3) input-referred offset is due to one-differential pair [20].

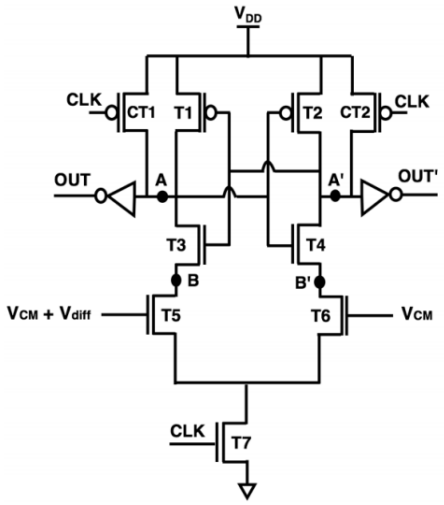


Figure 31 Original StrongArm Topology

Conventional Topology

Since the first implementation of the StrongArm topology in 1993 [21], there have been many modifications suggested to improve the robustness of the circuit. However, there was a compromise in size, speed, and efficiency. One of the most commonly used iterations of the topology is shown in Figure 32.a. The topology, suggested by [22], introduces two additional charging capacitors (CT3 and CT4) to the original two, which increases the charging speed of the internal capacitances, reducing the whole delay of the circuit. The design consists of 11 transistors, charging transistors (CT1, CT2, CT3, and CT4), cross-coupled transistors (T1, T2, T3, and T4), input transistors (T5 and T6) and one tail current transistor (T7).

The operation of the comparator consists of 3 stages as shown in Figure 32.b; *Reset, Amplification, and Regeneration.* The Reset stage begins when the CLK signal is Low, at-which, the charging transistors, CT1 to CT4 are turned on, charging the internal nodes, A, A', B, B'. The amplification stage starts on the positive edge of the CLK, as by then, the CTs are turned off to allow the capacitors to discharge through T7. In parallel, T6 and T6 are always ON as both are biased by a constant common-mode voltage (V_{cm}). Applying a small differential voltage (V_{diff}) between the gates of T and T6 causes a slight difference in the current flowing through the two transistors. As a result, the capacitors of B and B' discharge at different speeds. T3 and T4 turn ON when B and B' reach ($V_{DD} - V_{thn}$), hence, A and A' start discharging at different speeds. Regeneration stage begins when either A or A' reach ($V_{DD} - V_{thp}$) turning either T1 or T2 ON, and the other transistor remains OFF, and the values of A and A' remain fixed until the following negative edge of the CLK. The output is taken from nodes A and A' to be fed into inverters [22].

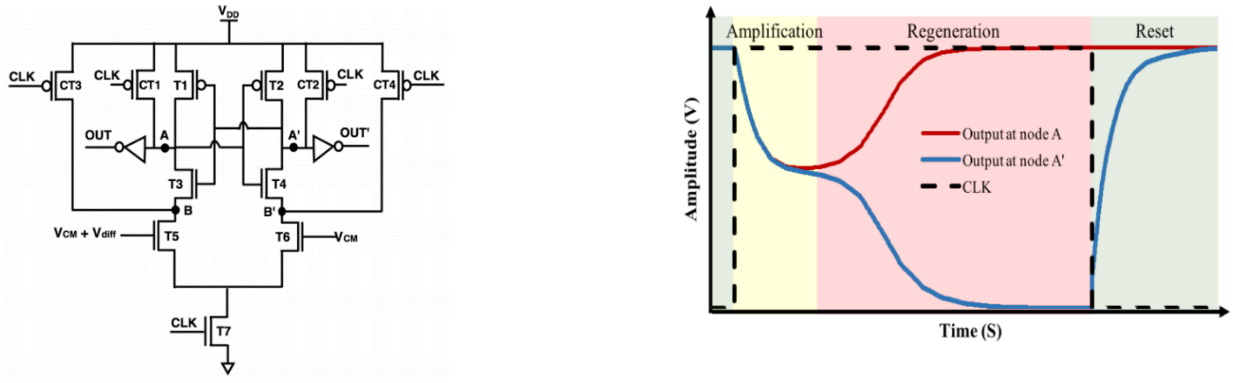


Figure 32 a) Conventional StrongArm Topology (b) Stages of Operation

One of the limitations that this topology suffers from, is the clock feedthrough problem. The voltages at A and A' follow the clock signal when it switches, resulting in a spike $> VDD$ at the positive CLK edge and a spike < 0 at the negative edge CLK, as shown in Figure 33. These spikes slow down the transition between stages which increases the overall delay of the circuit. The clock feedthrough effect is due to the gate-source (or gate-drain) coupling, through the internal capacitance. There are many solutions to the clock feedthrough problem by connecting capacitors/transistors at the gate of the charging transistor [23, 24]. However, this solution increases the total capacitance, adding more delay to the circuit.

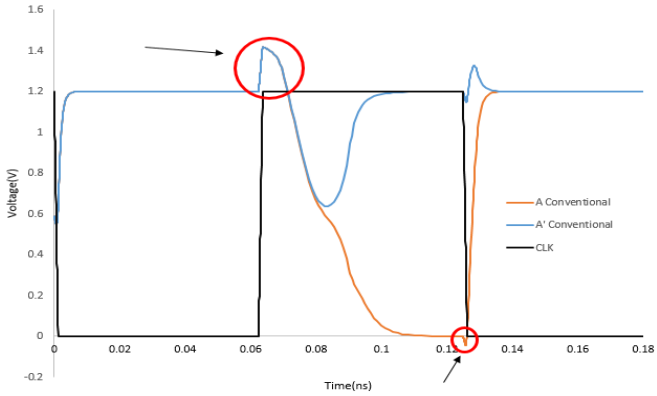


Figure 33 The clock Feedthrough Problem

Modified Topology

In general, any improvement to the circuit is through increasing the discharging speeds of the capacitors. However, changing the dimensions of the transistors can increase the internal capacitance which will add more discharging time and make the solution counter-productive. In the design in Figure 34, suggested by [23], a solution is proposed to decrease the total capacitance without affecting the current, and hence improve the circuit delay. This is achieved by placing the input transistors in the middle between the cross-coupled transistors. This will allow us to get rid of CT3 and CT4 as B and B' will instead be charged through T3 and T4 which are always ON. While improving the performance, this design also reduces the number of transistors used (9 instead of 11) and also reduces the area.

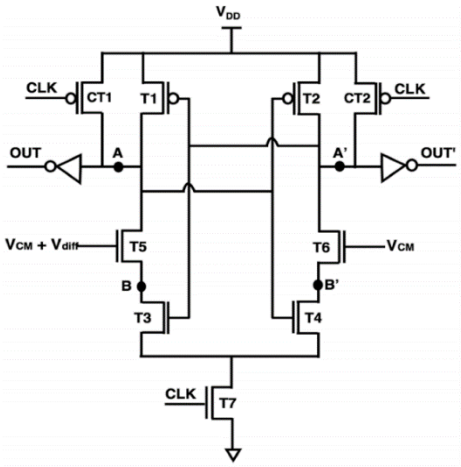


Figure 34 The Modified StrongArmTopology suggested in [22]

4.2.5 RS Latch Design

As the comparator output becomes invalid during the negative half cycle of the clock, an RS Latch is used to hold the output value of the comparator until the following positive edge of the clock, as shown in Figure 35.

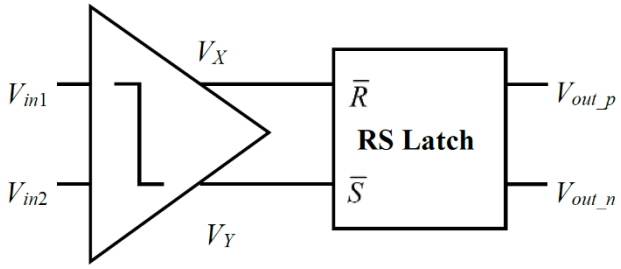


Figure 35 Latched Comparator

The conventional RS latch, as shown in Figure 36, has two inputs S (Set) and R (Reset). It is prohibited to have both of the inputs to be LOW at the same time, which is guaranteed by the comparator. If S input is low, it triggers a high output Q and hence forces $\bar{Q}$ to be LOW. Similarly, if R is low, $\bar{Q}$ becomes high and force Q to be LOW. The drawback of the said design is the fact that one of the outputs will always be delayed by the other. This Asymmetry will cause instability to the ADC system and hence cannot be used.

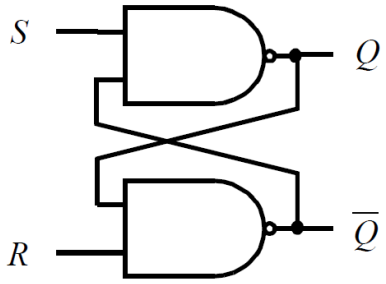


Figure 36 NAND RS Latch

To solve the outputs dependency issue, a different design is used [24], one that eliminates such dependency. The following output expression uses only the input expressions and the current states to implement RS latch

$$Q^+ = S + \bar{R}.Q \quad Eq.41$$

$$\bar{Q}^+ = R + \bar{S}.\bar{Q} \quad Eq.42$$

The first expression is implemented using an AND-OR structure, where S is an OR branch. Moreover, the second expression is implemented in the same topology. Figure 37 illustrates the topology implementation representing the above expression.

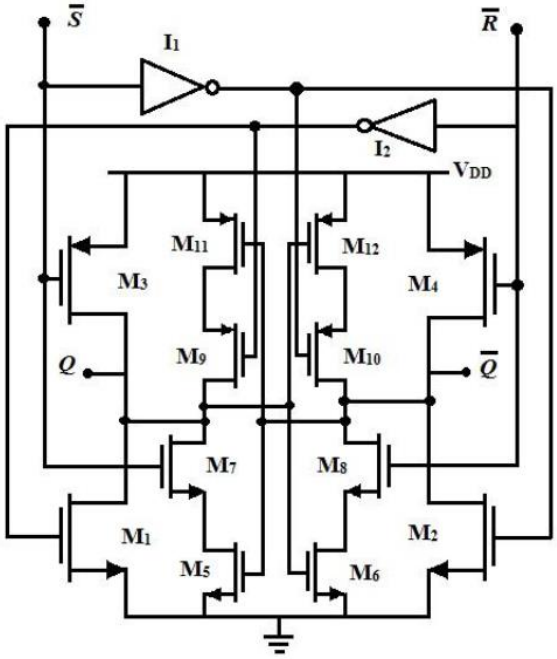


Figure 37 RS Latch Topology

There are many advantages to this topology, one of such advantages is its symmetry, which results in equal delay and equal strength of both outputs. Moreover, this topology allows the usage of small keeper transistors (M_5-M_{12}). This allows the keeper transistor to be turned off quickly during the state change, which enables the driver transistors (M_1-M_4) to change the state of the latch and provide outputs with the same strength and equal delay, which is paramount to the operation of the latched comparator.

4.2.6 Flipflop Design

To compensate for the timing differences between the DACs and the comparator, a delay of 1.5 clock cycles must exist between the output and the feedback of the DAC. Hence, a flip flop is used to produce a one-cycle delay. A negative latch is added to produce the remaining half-cycle delay and reach the targeted delay of 1.5 cycles.

As shown in Figure 38, the implemented flip flop is constructed using transmission gate multiplexers [25]. The design consists of two latches, one is positive and the other is negative. The positive latch passes the input when the clock is HIGH. When the clock is LOW, the current state is preserved using the feedback loop. The negative latch performs the opposite operation.

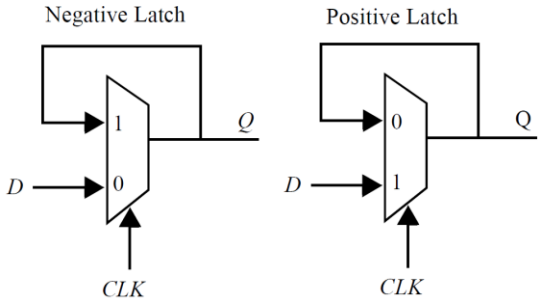


Figure 38 Multiplexer-based Latches

The flip flop is constructed by implementing the negative and the positive latches in a master-slave configuration, which is shown in Figure 39. On the LOW phase of the clock, the master latch is transparent and the slave latch is on hold, while on the HIGH phase of the clock, the slave samples the output of the master latch. Hence, D is delayed with one cycle.

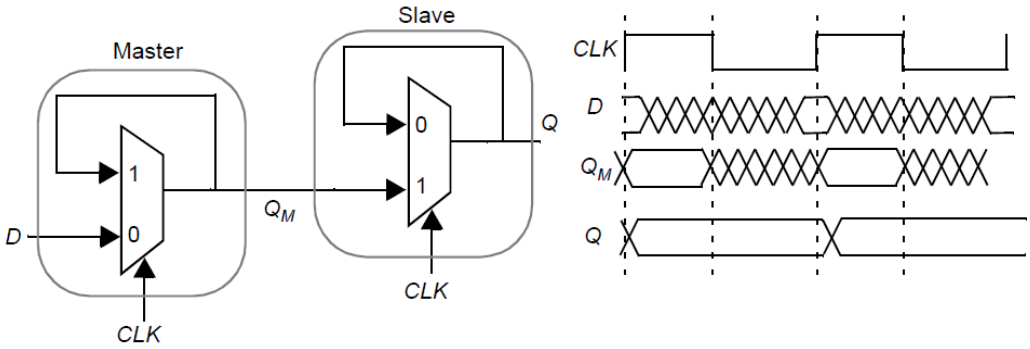
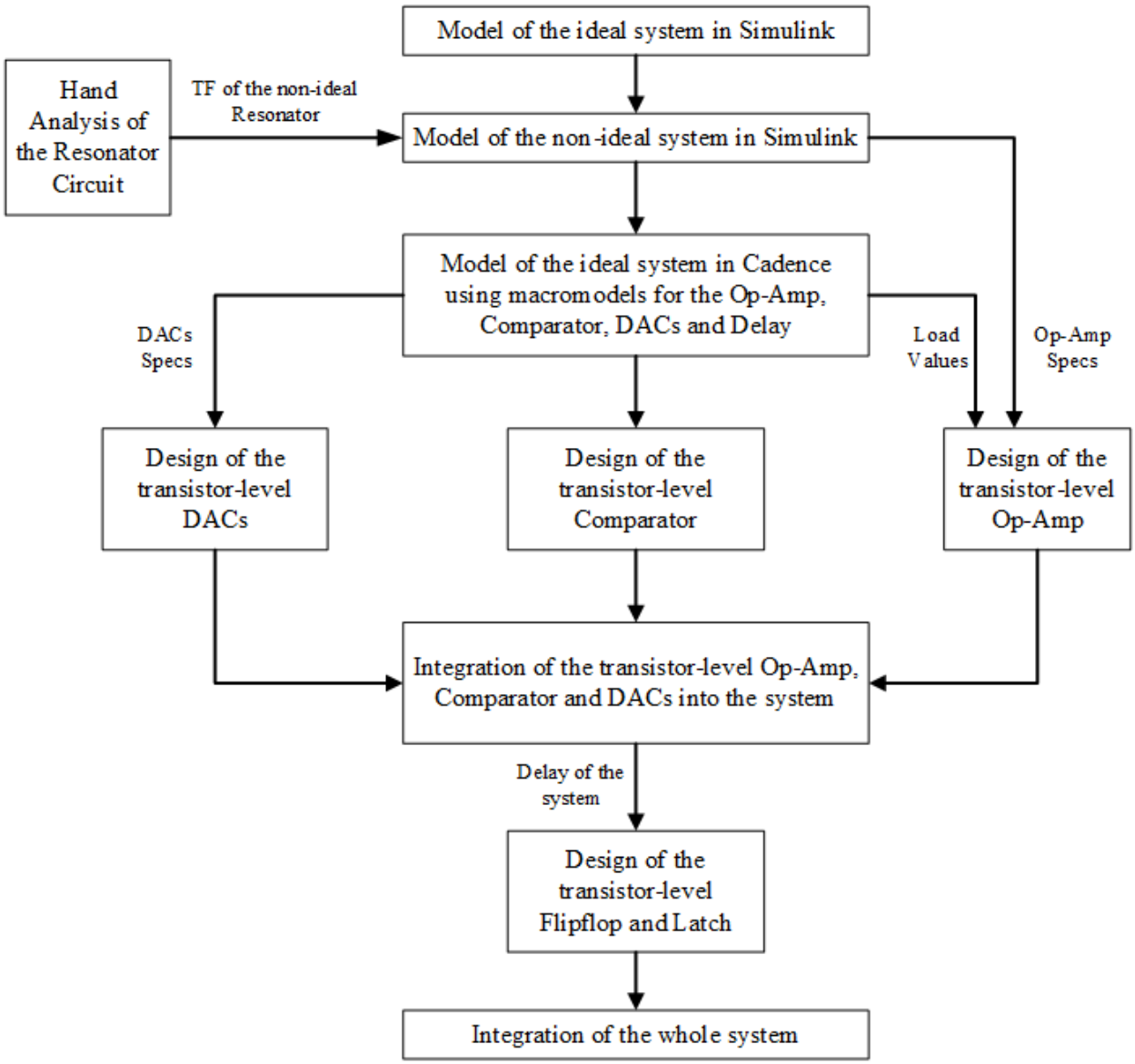


Figure 39 Master-slave implementation of flip latches

4.3 Implementation

The system implementation steps are demonstrated in the following flowchart:



4.3.1 Simulink System-Level Model

4.3.1.1 Model of the Ideal System

The system is modeled in Simulink as shown in Figure 40 using an ideal resonator with an ideal transfer function followed by a sample and hold block and a comparator block. A delay block is added in the feedback path to model the delay of the DAC and $A11$ and $A21$ are the coefficients extracted from mapping the DT system into a CT system.

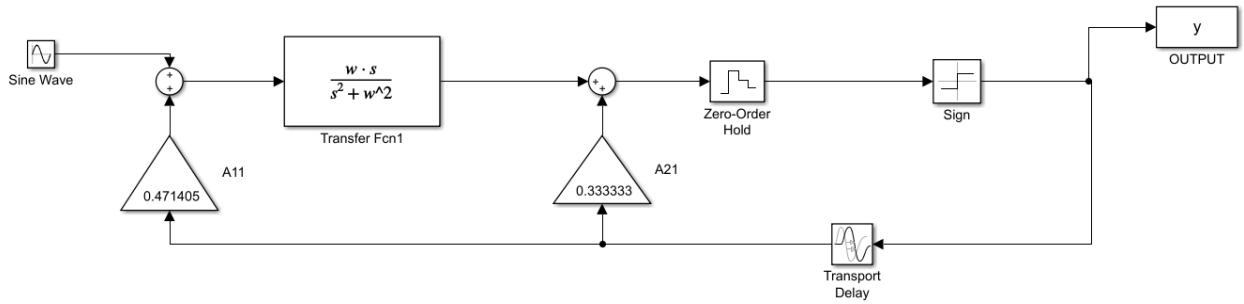


Figure 40 Simulink model of the system using ideal resonator

The amplitude of the input for the system is determined by sweeping over a range and plotting the SNR as in Figure 41. The highest SNR of $57.07\ dB$ is obtained at the optimum amplitude $-9.071\ dB$. The power spectrum is shown in Figure 42 and Table 1 summarizes the used parameters.

Table 1 Ideal model used Parameters and expected SNR

Parameter	Value
Input amplitude	$-9.071\ dB$
Number of points (N)	$16 * 1024 = 16384$
Sampling frequency (f_s)	1
Center frequency (f_0)	$0.25 * f_s = 0.25$
Input frequency (f_{in})	$f_0 + \frac{31}{N} = 0.25189$
Over sapling frequency (OSR)	64
Signal to noise ratio (SNR)	$57.07\ dB$

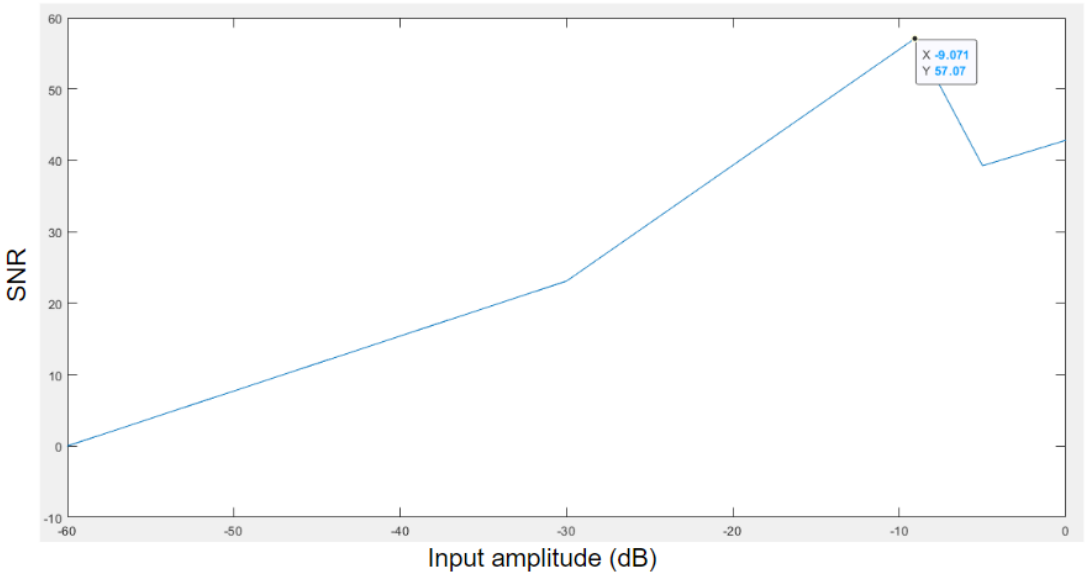


Figure 41 Input Amplitude vs SNR

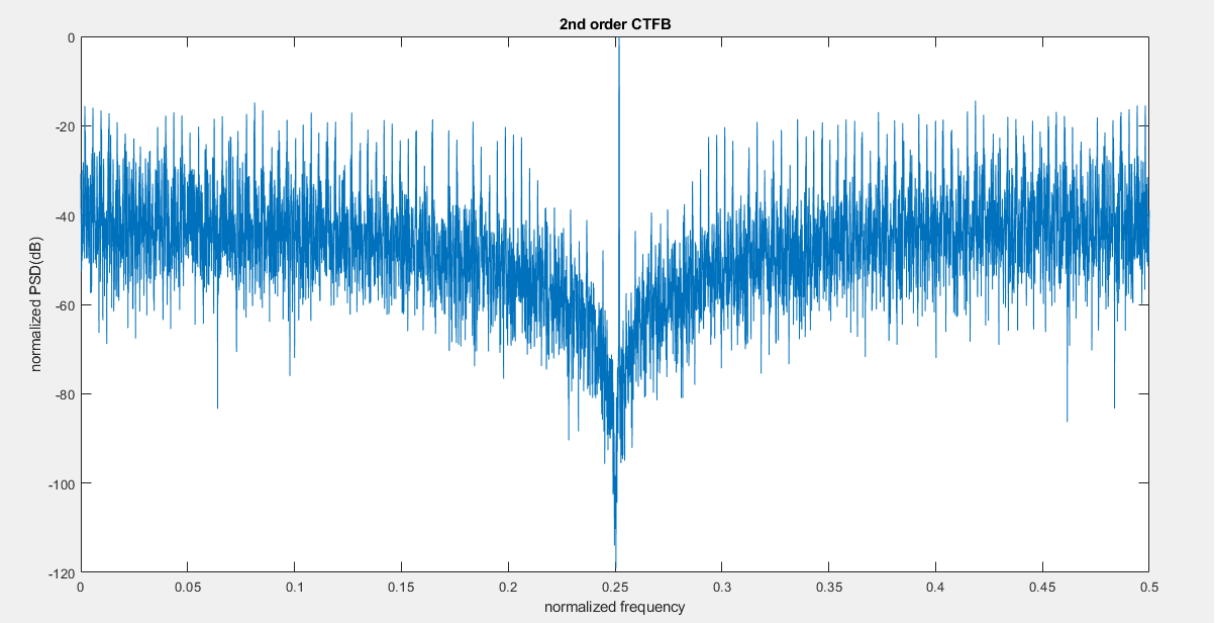


Figure 42 Power spectrum of the ideal system

4.3.1.2 Model of the Non-Ideal System

To account for the non-idealities of the Op-Amp, the system is modeled in Figure 43 using the non-ideal transfer function of the resonator (Equation 29) which is a function of the gain and bandwidth of the Op-Amp.

$$\frac{OUT}{IN} = Q\frac{\omega_0 s}{s^3\frac{2}{A_0 p} + s^2\left(1 + \frac{4}{A_0 p}\omega_0(2+Q)\right) + \frac{2\omega_0^2}{A_0 p}(1+2\,Q) + \omega_0^2} \qquad Eq.29$$

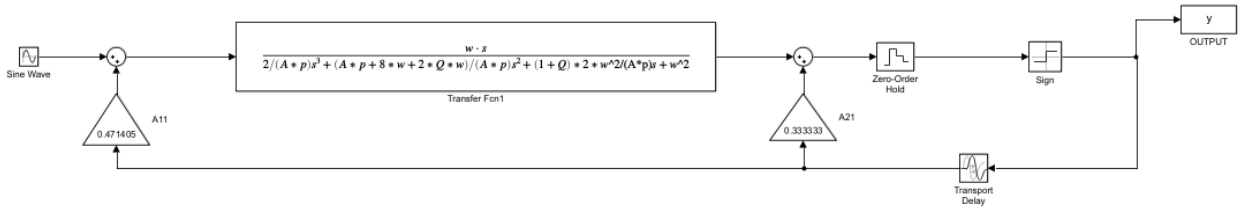


Figure 43 Simulink model of the system using non-ideal Op-Amp in the resonator

This model is used to determine the value of SNR at different combinations of the gain and bandwidth of the Op-Amp in order to determine the gain and bandwidth required for the Op-Amp to be designed. Figure 44 shows the 3D plot of the SNR vs the gain in dB and bandwidth in MHz of the Op-Amp. Table 2 shows some of the DC gain and Bandwidth values of the non-ideal Op-Amp across the SNR value of the system.

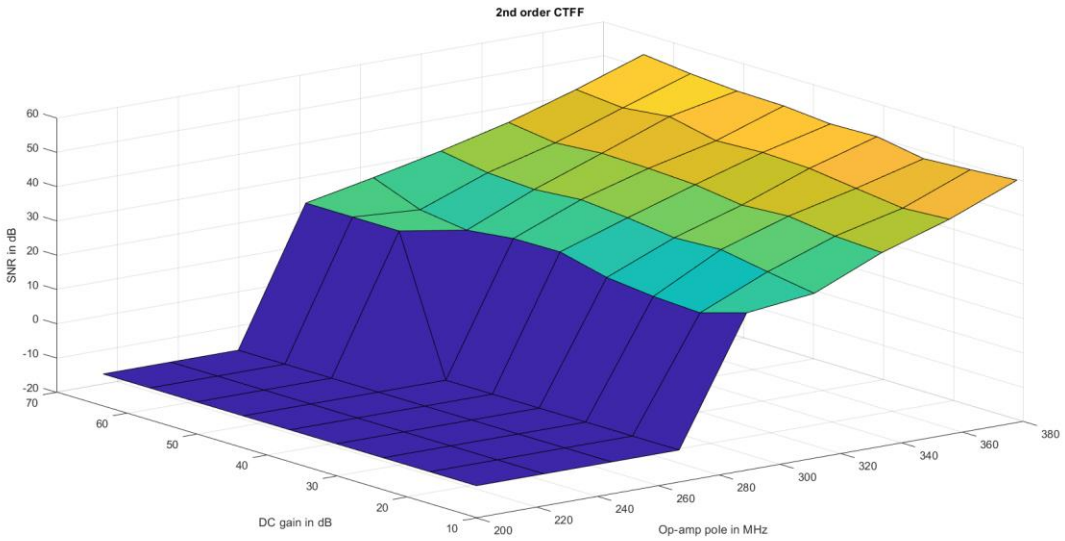


Figure 44 SNR vs Gain vs Bandwidth

Table 2 Required specs for the Op-Amp and the expected SNR

DC gain (dB)	Bandwidth (MHz)	SNR (dB)
63	378	54.8
63	355	53
60	300	50.6
57	355	49.1

For this system, we choose to design an Op-Amp with DC gain of $60\,dB$ and bandwidth of $300\,MHz$ as these are achievable specs for a four-stage Op-Amp. Figure 45 shows the spectrum of the model with an Op-Amp with DC gain of $60\,dB$ and bandwidth of $300\,MHz$. This shows that the expected SNR of the implemented non-ideal system is $50.6\,dB$. Table 3 summarizes the used parameters.

Table 3 Non-Ideal model used parameters and expected SNR

Parameter	Value
Input amplitude	$-9.071\,dB$
Number of points (N)	$16 * 1024 = 16384$
Sampling frequency (f_s)	1
Center frequency (f_0)	$0.25 * f_s = 0.25$
Input frequency (f_{in})	$f_0 + \frac{31}{N} = 0.25189$
Over sapling frequency (OSR)	64
Signal to noise ratio (SNR)	$50.06\,dB$

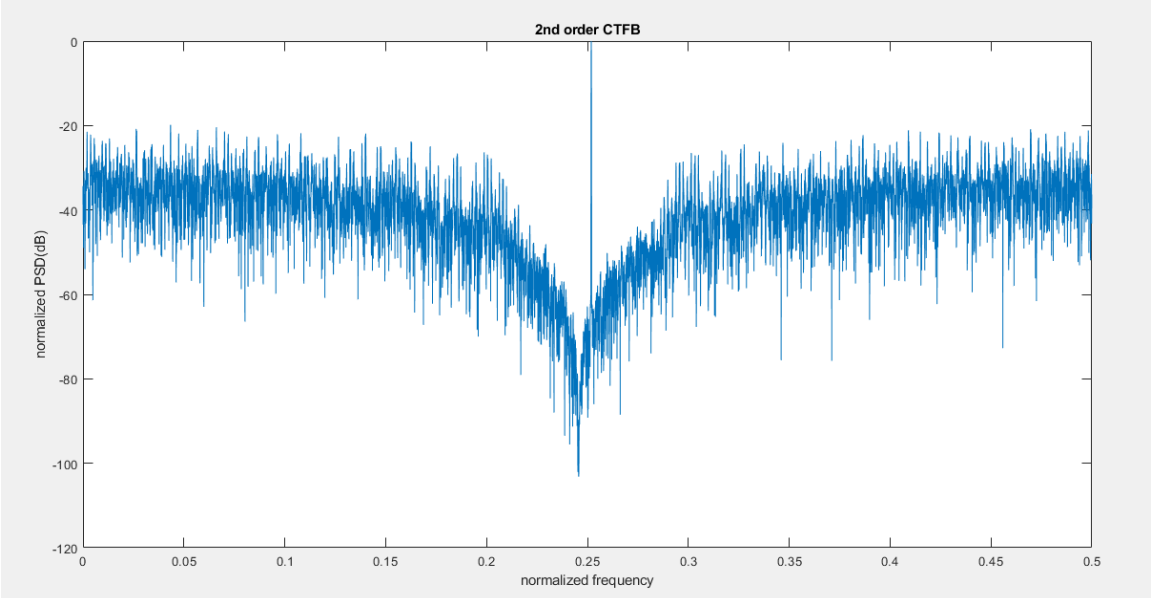


Figure 45 Power Spectrum of the non-ideal system

4.3.2 The Macro-models system-level Implementation

4.3.2.1 System Model using Ideal blocks in Cadence Virtuoso

The 2^{nd} order system is implemented in Cadence Virtuoso, as shown in Figure 46, using compact Verilog-A models for the Op-Amp (with infinite gain and Bandwidth), the comparator, the sample and hold, and the delay module where the delay $= 1.5 * T_s$, while the ideal DACs are modeled as voltage-controlled current sources (vccs) with their transconductances equal to the MATLAB coefficients normalized with respect to the first coefficient.

As well, since the DC of the ideal comparator's output is zero, a voltage-controlled voltage source (vcvs) with a gain of 1, along with a voltage source of $600mV$ are used to set the DC of the ideal comparator's output to $600mV$.

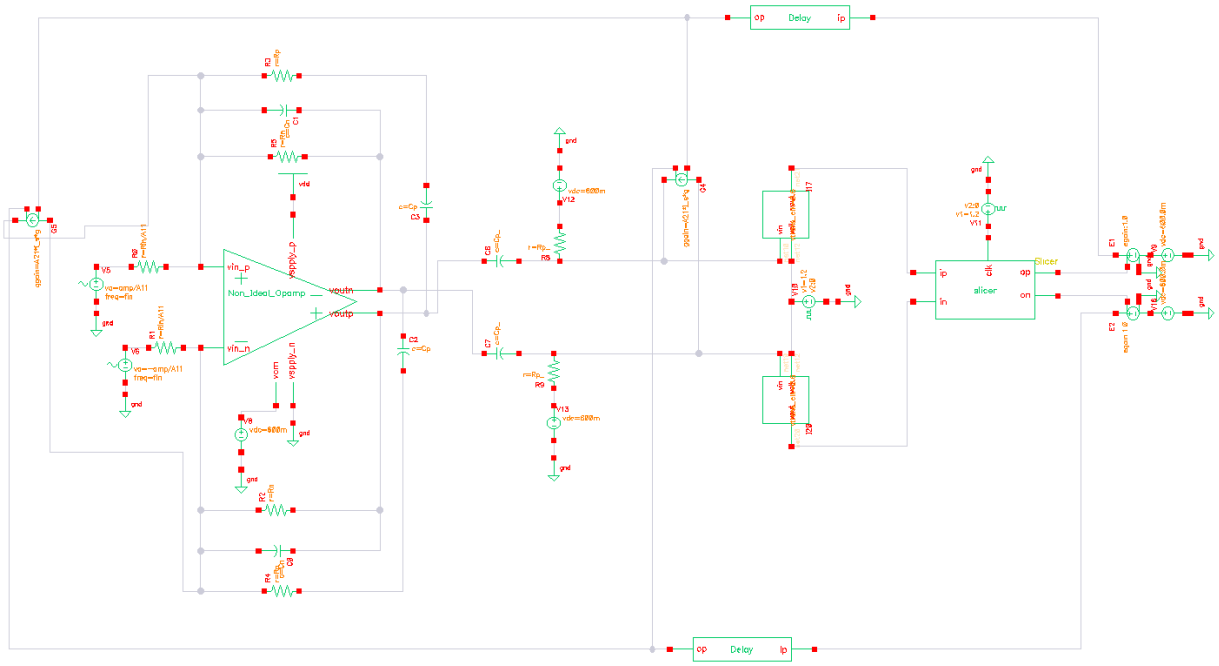


Figure 46 Macro-models System-level Model

4.3.2.2 Design of the resonator

Since the resonator is followed by an HPF to be able to drive resistive loads effectively, the DC of the output of the resonator shown in Figure 24 is zero, and thus the following blocks will not be able to function correctly. Accordingly, the resonator was adjusted as shown in Figure 47, so that its output has a common mode value of $600mV$.

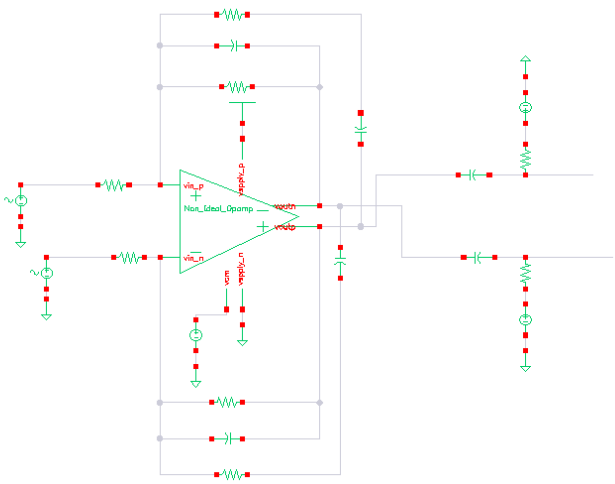


Figure 47 Adjusted Design of the Resonator

The values of the resonator's capacitors and resistors, shown in Table 4 were chosen according to Equations 17 and 24 to achieve a center frequency of $200MHz$ along with a quality factor $Q > 100$, while trying to choose small resistance values, so that their thermal noise does not limit the performance of the ADC, along with small values of the capacitances (with a maximum of $1\ pF$).

The performance of the designed resonator within the frequency range of $1 - 400MHz$ is shown in Figure 48, achieving a center frequency of $200MHz$ and the quality factor is calculated as in Equation 43

$$Q = \frac{f_c}{f_{H(-3dB)} - f_{L(-3dB)}} \qquad Eq.43$$

$$Q = \frac{200MHz}{200.0102MHZ - 199.9898} = 9803.92$$

Table 4 Values of resistances and capacitors of the resonator

R_{in}	400
R_n	1.6K
R_p	800
R_p'	4K
C_n	500fF
C_p	1pF
C_p'	200fF

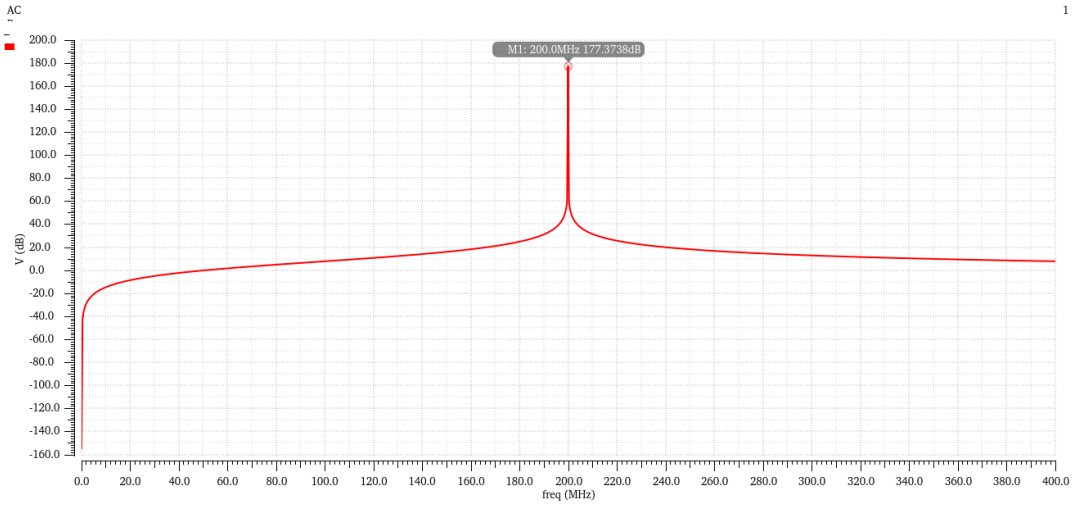


Figure 48 Performance of the resonator

4.3.2.3 System Scaling Methodology

The methodology of mapping a DT system to a CT system only takes into account the stability of the noise transfer function along with the system-level design. However, to implement the system onto the circuit-level, the system must be scaled down so that the swing of the output of the resonator becomes within the supply. The basic changes incorporated into the system are illustrated in Figure 49.

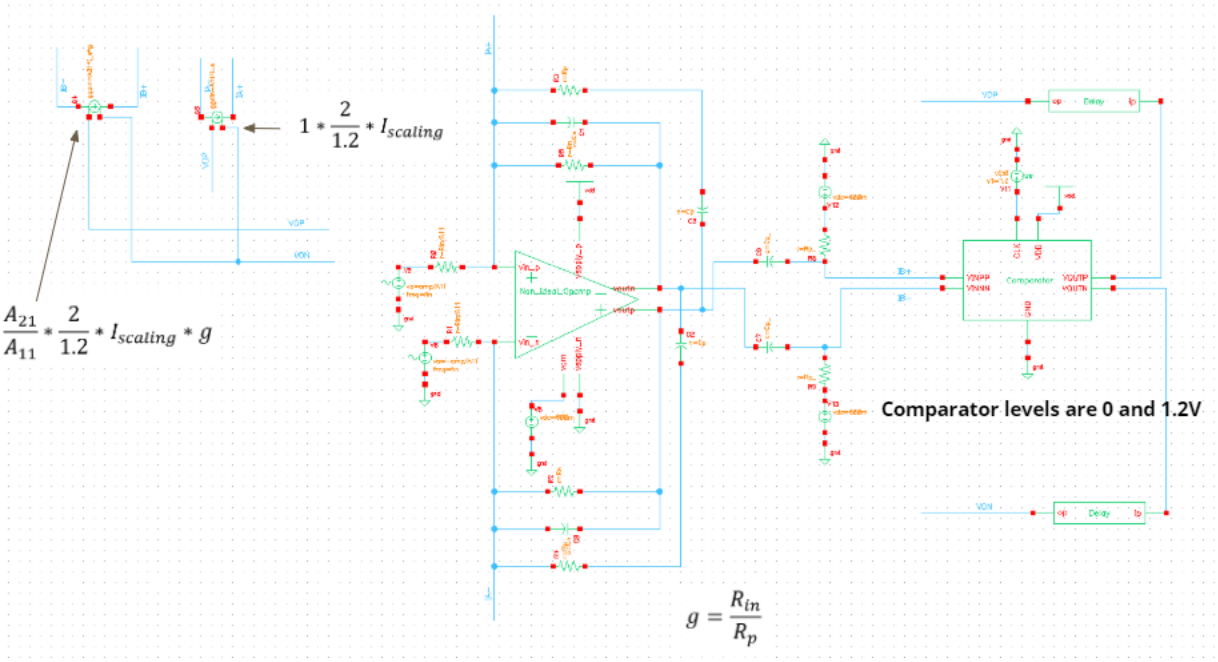


Figure 49 Methodology of the system scaling

The scaling steps aim to preserve both the noise transfer function and the signal transfer function while limiting the output swing of the resonator. First, the comparator levels are changed to match that of the circuit implementation, instead of the MATLAB model (ranging from -1 to 1), and accordingly, all of the DACs coefficients are scaled by this factor.

$$\frac{(Comp_{\ high} - Comp_{low})_{MATLAB}}{(Comp_{\ high} - Comp_{low})_{Circuit}} = \frac{2}{1.2} \qquad Eq.44$$

Then, a scaling factor ($I_{scaling}$) is multiplied by the normalized MATLAB coefficients of the two DACs. Also, to accommodate for the gain resulting from the resonator, the gain (g) is multiplied by the coefficient of the second DAC where

$$g = \frac{R_{in}}{R_p} \qquad Eq.45$$

Since the NTF is to be preserved, the same scaling factor ($I_{scaling}$) is multiplied by the input amplitude but since the input is voltage, it is multiplied along with R_{in}. Finally, using Equation 44 and 45, the scaling process is demonstrated by Equations 46, 47, and 48.

$$1st\ DAC\ Coefficient = 1 * \frac{2}{1.2} * I_{scaling} \qquad Eq.46$$

$$2nd\ DAC\ Coefficient = \frac{A_{21}}{A_{11}} * \frac{2}{1.2} * I_{scaling} * \frac{R_{in}}{R_p} \qquad Eq.47$$

$$Input\ Amplitude = Amp_{MATLAB} * I_{scaling} * R_{in} * \frac{1}{A_{11}} \qquad Eq.48$$

4.3.2.4 Results of the scaled system

The power spectral density of the scaled system, from DC to $\frac{F_s}{2}$ $(400MHz)$ is shown in Figure 50. The scaled system achieves an SNR of $53dB$ for a signal BW of $6.25MHz$ (with 16384 points for the FFT), along with the resonator's output ranging between $500mV$ and $700mV$.

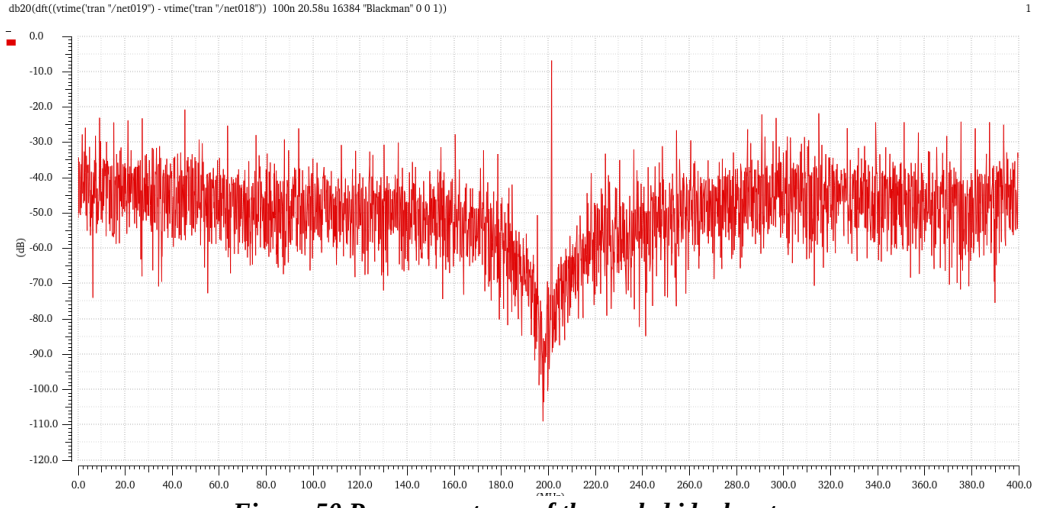


Figure 50 Power spectrum of the scaled ideal system

4.3.3 Transistor-level Implementation of the system

4.3.3.1 Op-Amp Implementation

Figure 51 shows the transistor-level implementation of the Op-Amp with the 1^{st} stage implementing gm_1 and the i^{th} stage implementing both gm_i and g_{mffi} $(i = 2,3,4)$. The design uses current-reusing techniques in the 2^{nd}, 3^{rd} and 4^{th} stages so that the same current flows in both the feedforward and original paths, which leads to improving the power efficiency of the design.

All of the transistors used in this design have an even number of fingers to ensure that the layout is symmetric. Also, all of the current mirror transistors consist of multipliers of the unit transistor chosen, to ensure that the ratios between them and thus the current will be accurate.

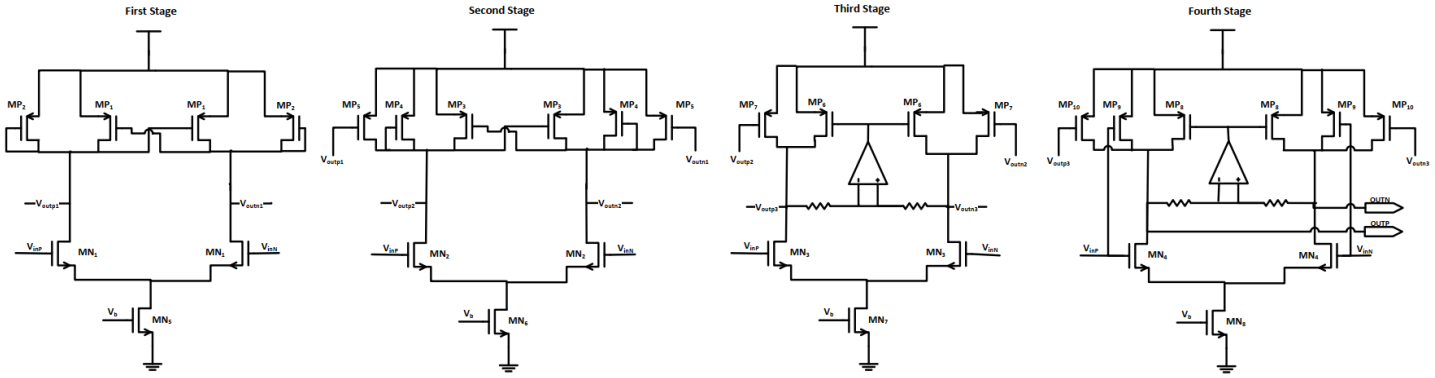


Figure 51 Transistor-level implementation of the feedforward-compensated 4-stage FF Op-Amp

I. The transistor-level implementation and performance of the stages

A. 1st stage of the Op-Amp

For the 1^{st} stage, gm_1 is realized using $NMOS$ differential pair MN_1. And the load consists of both the cross-coupled pair MP_1 and the diode-connected $PMOS$ MP_2. As proposed in [15], this load offers two main advantages: the first is providing large output impedance as the cross-coupled pair cancels the $1/g_m$ resistance of the diode-connected transistors, to ensure this MP_1 and MP_4 have the same dimensions and the same current flowing through them, thus they have the same transconductance. The second benefit is that the cross-coupled pair provides DC biasing for the next input stage eliminating the need for common-mode feedback circuitry. The sizing of the transistors used in this stage is shown in Table 5.

Simulation Results

To measure the AC response of the first stage (when loaded with the parasitics of the second stage) accurately, the test bench, shown in Figure 52, is made where a load equal to $C_{gg}(\approx 290\ fF)$ of the 2^{nd} main stage is connected to the output.

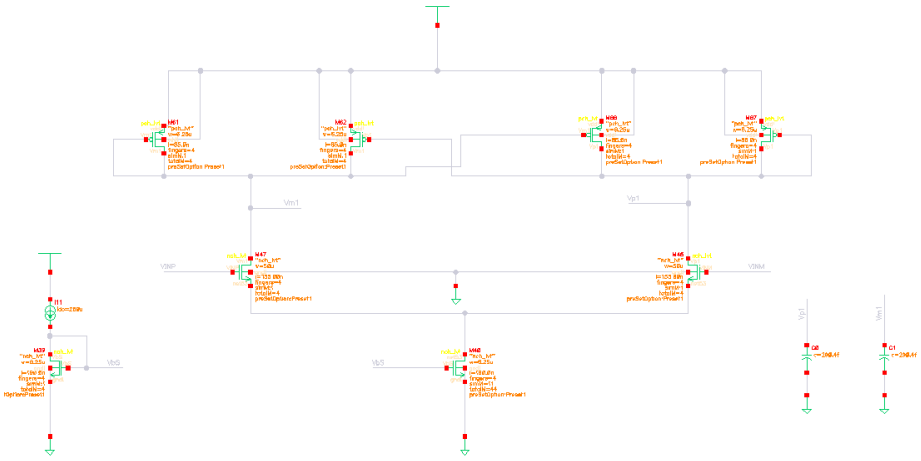


Figure 52 Testbench for the 1st stage of the Op-Amp loaded with the second stage capacitance

MN_1	200u/155n
MP_1, MP_2	25u/85n
MN_5	25u/190n (×11)

Table 5 Aspect Ratios of the transistors used in the first stage

The 1^{st} stage of the Op-Amp has a DC gain of 28 dB and a Bandwidth of 595.975 MHz as shown in Figure 53, with a biasing current of 2.5 mA and power consumption of 3 mW.

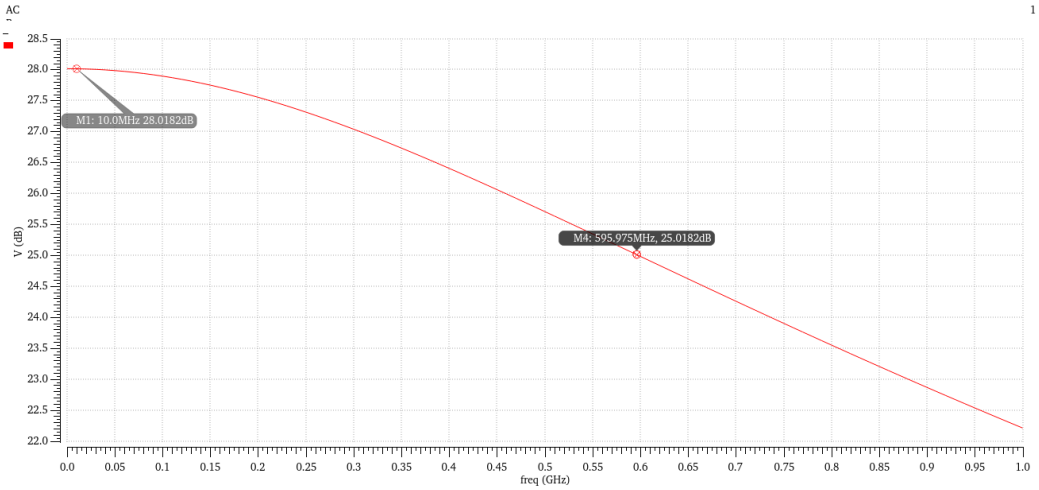


Figure 53 Simulated AC response of the 1st stage of the Op-Amp

B. 2nd stage of the Op-Amp

The second stage has a similar topology to the first one, and it employs the current reusing techniques between g_{m2} and g_{mff2}. To ensure that the feedforward path is faster than the original path, g_{m2} is implemented with $PMOS$ transistors MP_5, while g_{mff2} is implemented with $NMOS$ transistors MN_2 that have higher carrier mobility and thus higher transconductance. The aspect ratios of the transistors used in this stage are shown in Table 6.

MN_2	150u/90n
MP_3, MP_4	12u/90n
MP_5	150u/140n
MN_6	25u/190n (×36)

Table 6 Aspect Ratios of the transistors used in the second stage

Simulation Results

To measure the AC response of the second stage (when loaded with the parasitics of the third stage) accurately, the test bench, shown in Figure 54, is made where a load equal to C_{gg} ($\approx 310\ fF$) of the input $PMOS$ 3^{rd} main stage is connected to the output.

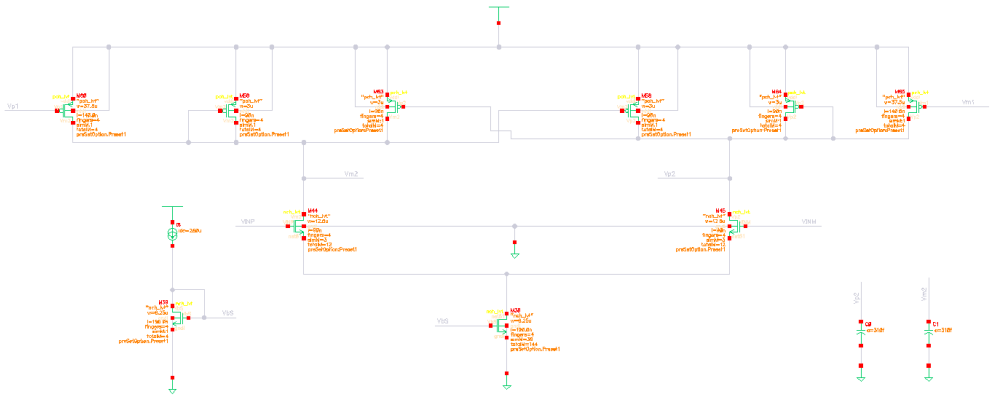


Figure 54 Testbench for the 2nd stage of the Op-Amp loaded with the main third stage capacitance

The 2^{nd} main stage of the Op-Amp has a DC gain of 20 dB and a Bandwidth of 1.662 GHz, while the second feedforward stage has a DC gain of 25.476 dB and a Bandwidth of 1.679 GHz as shown in figure 55, with a biasing current of 7.55 mA and power consumption of 9 mW.

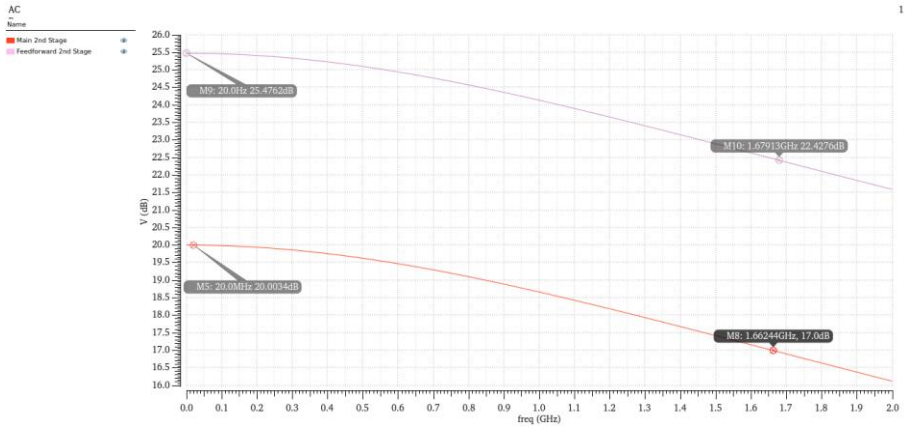


Figure 55 Simulated AC response of the 2nd stage (main and feedforward) of the Op-Amp

C. 3rd stage of the Op-Amp

For the third stage, g_{m3} is realized using the $PMOS$ pair (MP_7), and g_{mff3} is realized using the $NMOS$ pair MN_3. A large output swing is obtained by this topology through using the $PMOS$ pair (MP_6) as the load. The common-mode level of the outputs of this stage are controlled using Common-mode feedback amplifier with its output applied to MP_6. The aspect ratios of the transistors used in this stage are shown in Table 7.

Simulation Results

To measure the AC response of the third stage (when loaded with the parasitics of the fourth stage) accurately, the test bench, shown in Figure 56, is made where a load equal to C_{gg} ($\approx 155\ fF$) of the input $PMOS\ 4^{th}$ main stage is connected to the output.

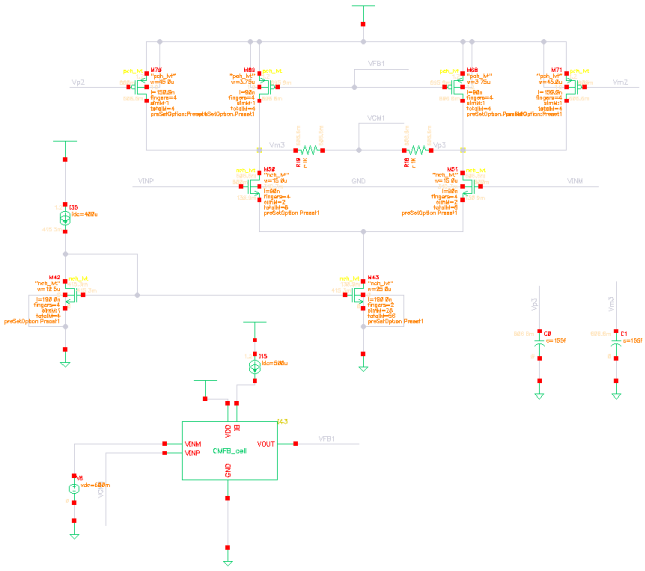


Figure 56 Testbench for the 3rd stage of the Op-Amp loaded with the main fourth stage capacitance

MN_3	120u/90n
MP_6	15u/90n
MP_7	180u/150n
MN_7	50u/190n (×28)

Table 7 Aspect Ratios of the transistors used in the third stage

The 3^{rd} main stage of the Op-Amp has a DC gain of 19.838 dB, and a Bandwidth of 3.173 GHz, while the third feedforward stage has a DC gain of 23.5927 dB and a Bandwidth of 3.16987 GHz as shown in Figure 57, with a biasing current of 7.61 mA and power consumption of 9.13 mW.

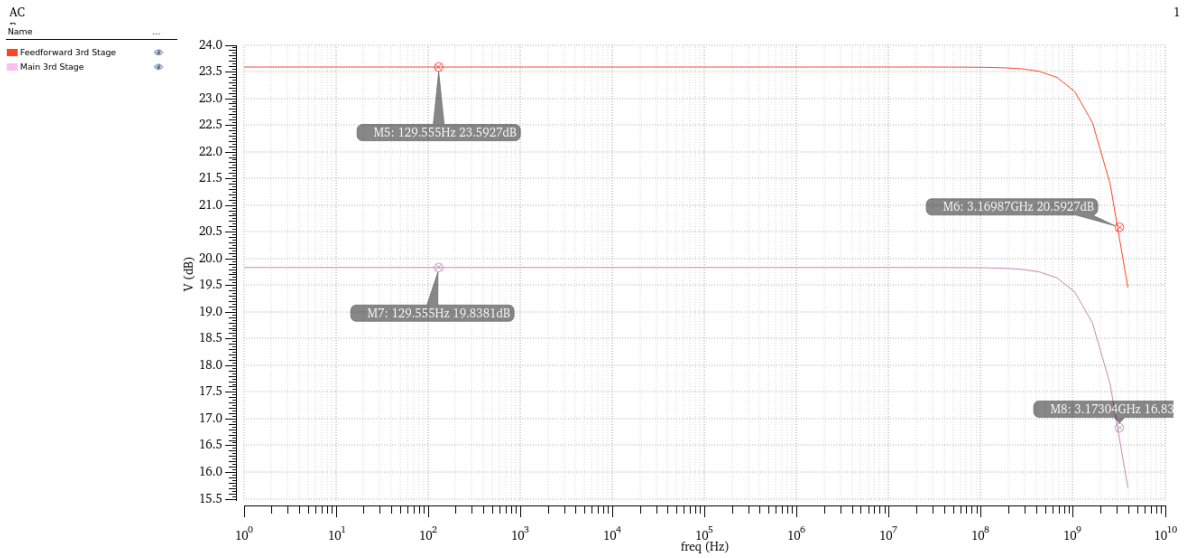


Figure 57 Simulated AC response of the 3rd stage (main and feedforward) of the Op-Amp

D. 4th stage of the Op-Amp

The 4^{th} stage uses the current reusing technique between g_{m4} and g_{mff4} and also within the implementation of g_{mff4} to further improve the power efficiency of the design. g_{m4} is implemented with MP_{10}, while g_{mff4} is implemented with both MN_4 and MP_9, so that g_{mff4} is the summation of the transconductances of the two transistors, accordingly a large g_{mff4}/C_L system requirement is achieved. A common-mode feedback (CMFB) amplifier is also used to stabilize the common mode of this stage. The aspect ratios of the transistors used in this stage are shown in Table 8.

MN_4	280u/90n
MP_8	25u/90n
MP_9	100u/90n
MP_{10}	140u/90n
MN_8	50u/190n (×35)

Table 8 Aspect Ratios of the transistors used in the fourth stage

Simulation Results

To measure the AC response of the fourth stage, the testbench shown in Figure 58, is used where the stage is loaded with the total resistive and capacitive loads of the resonator used in the system.

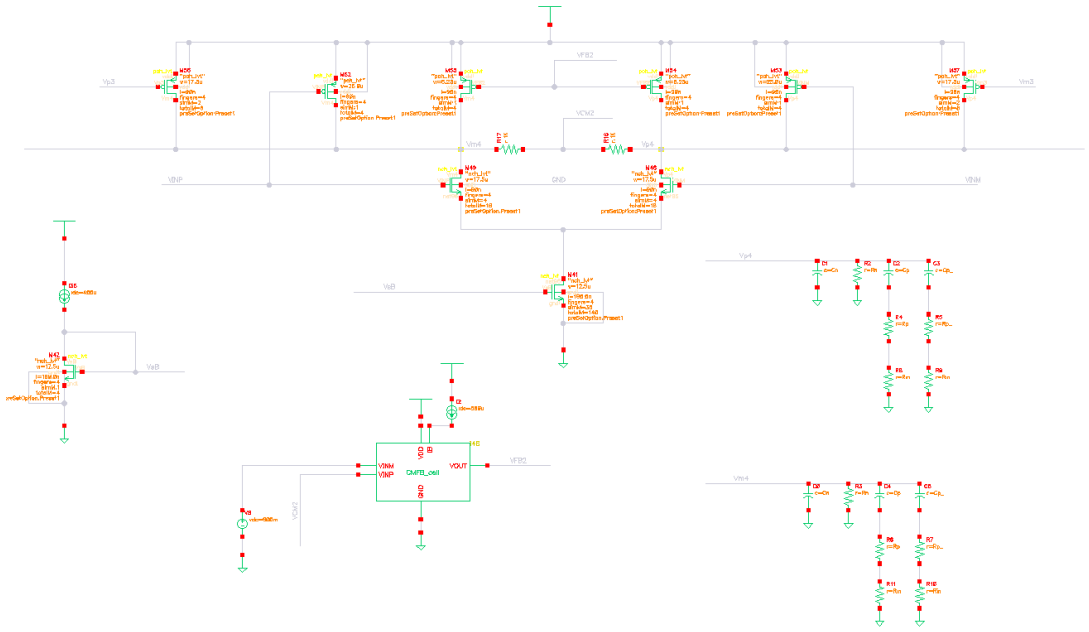


Figure 58 Testbench for the fourth stage of the Op-Amp loaded with the resonator's capacitive and resistive loads

The 4^{th} main stage of the Op-Amp has a DC gain of 14.2849 dB and a Bandwidth of 2.01 GHz, while the second feedforward stage has a DC gain of 24.7278 dB and a Bandwidth of 2.01 GHz as shown in Figure 59, with a biasing current of 11.67 mA and power consumption of 14 mW. Table 9 summarizes the biasing currents and total power consumption of the 4 stages Op-Amp.

Table 9 Biasing currents and power consumption of each stage

Stages	1^{st}	2^{nd}	3^{rd}	4^{th}	
Biasing Current	2.5 mA	7.55 mA	7.61 mA	11.67 mA	Total
Power Consumption	3 mW	9 mW	9.13 mW	14 mW	35.13 mW

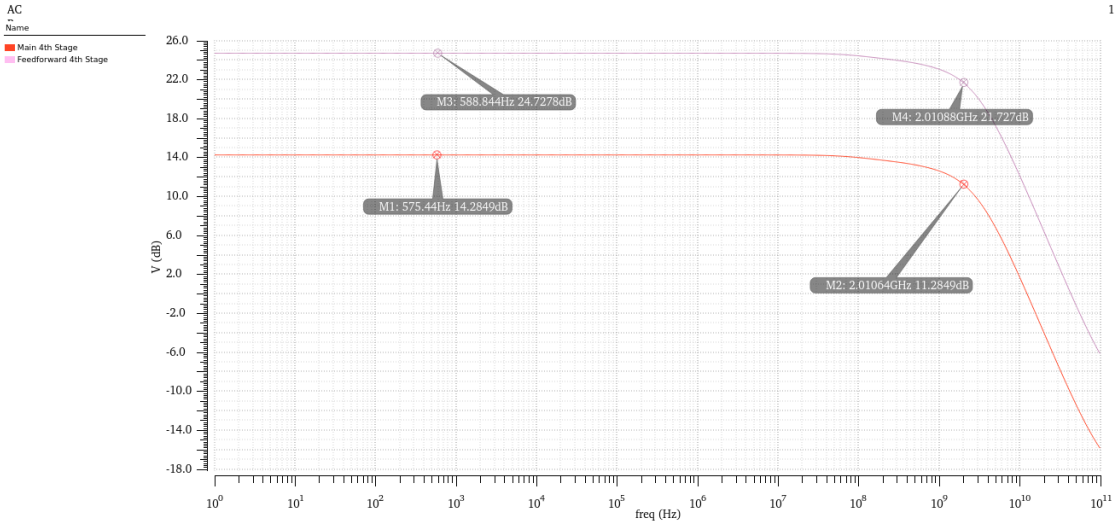


Figure 59 Simulated AC response of the 4th stage (main and feedforward) of the Op-Amp

E. Common-mode feedback (CMFB) Amplifier (5T-OTA)

The 5T-OTA (shown in figure 60) is used as a common-mode amplifier to stabilize the common-mode levels of both the third and fourth stages. The output level of the OTA is equal to the gate voltage of the current mirror $PMOS$ loads of both the third and fourth stages, to ensure that there's no offset error between the two. The aspect ratios of the used transistors are shown in Table 10.

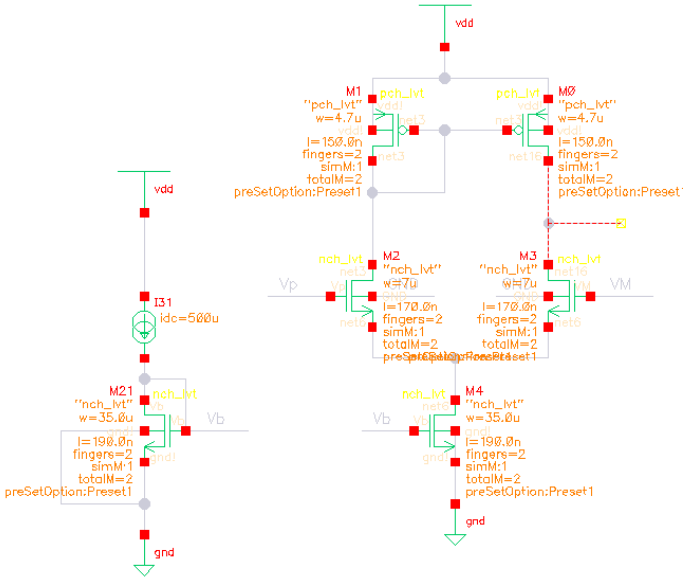


Figure 60 Schematic of the CMFB amplifier (5T-OTA)

M_2, M_3	14u/170n
M_0, M_1	18.8u/150n
M_4	70u/190n

Table 10 Aspect Ratios of the transistors used in the CMFB

Simulation Results

The AC (small signal) response of the CMFB amplifier within the range of $1\ Hz - 3\ GHz$ is shown in Figure 61. The CMFB amplifier has a DC gain of $23.44\ dB$ and a Bandwidth of $2.169\ GHz$, with a biasing current of $500\ uA$ and a DC output level of $600\ mV$.

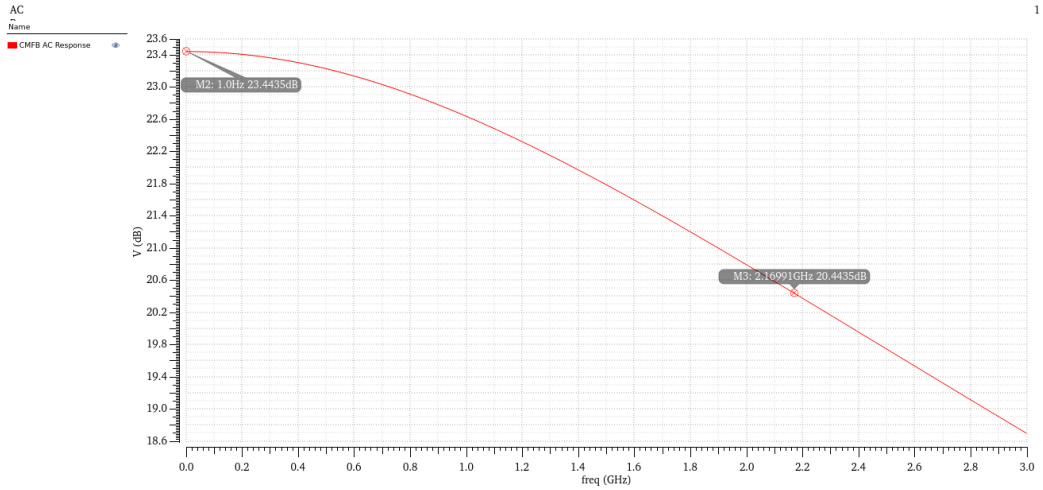


Figure 61 Simulated AC response of the CMFB amplifier

II. Three-stage Feedforward-Compensated Op-Amp

A. Frequency Response of the Op-Amp

To measure the AC performance metrics of the three-stage feedforward-compensated Op-Amp, the testbench, shown in Figure 62, was used where the Op-Amp is loaded with the capacitive and resistive loads of the resonator used in the system's design.

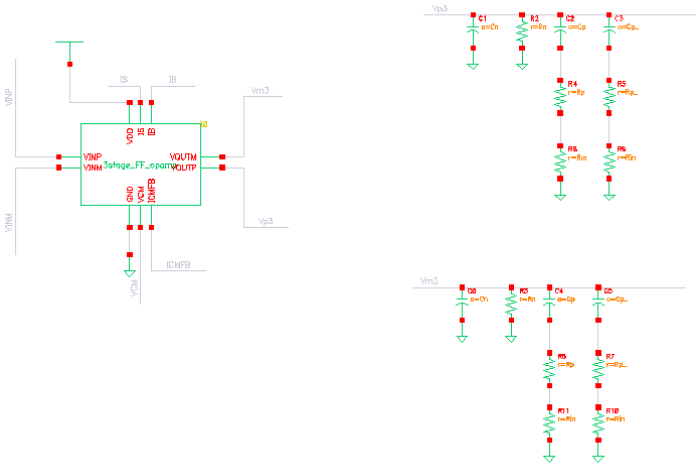


Figure 62 Testbench for the 3-stage FF Op-Amp loaded with the resonator's capacitive and resistive loads

The frequency response of the Three-stage FF Op-Amp is shown in Figure 63. The Op-Amp achieves a DC gain of 49.1 dB, a Bandwidth of 326.605 MHz, a unity gain frequency of 43.3587 GHz and a phase margin of 73.613°.

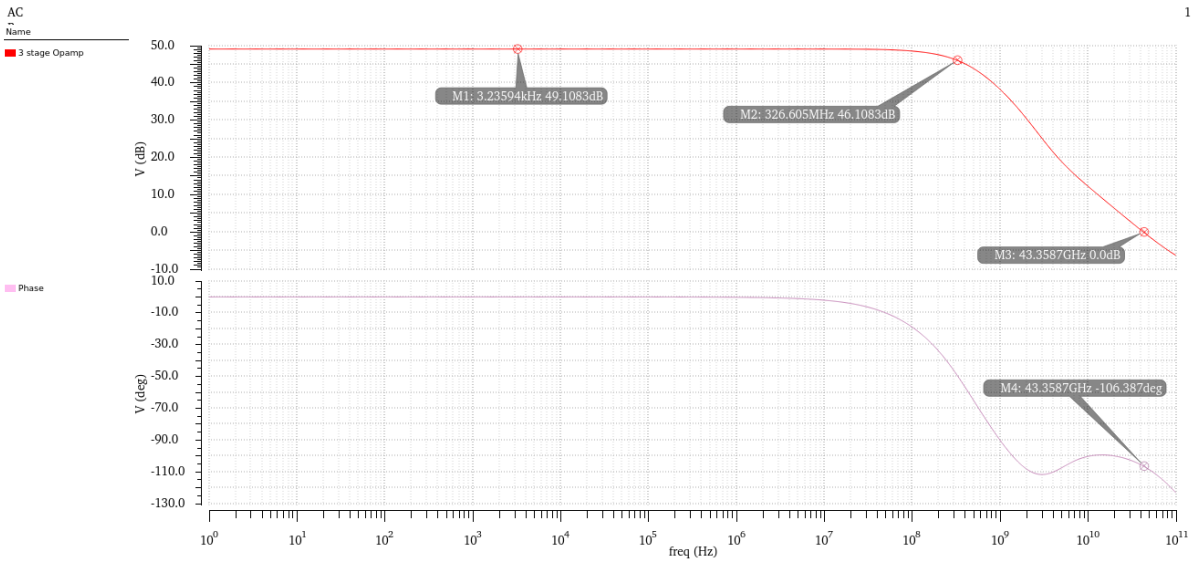


Figure 63 Frequency Response of the 3-stage FF Op-Amp resonator

B. Resonator using the Three-stage FF Op-Amp

To account for the parasitics of the Op-Amp, the values of the external capacitors and resistors of the resonator were adjusted as shown in Table 11. The frequency response of the adjusted resonator is in Figure 64. After the adjustment of the resistors and capacitors' values, the resonator has achieved a center frequency of 200 MHz and a quality factor (from Equation 43) of

$$Q = \frac{200MHz}{200.4749MHZ - 199.8382} = 314.12$$

R_{in}	400
R_n	1.91K
R_p	760
R_p'	4K
C_n	396.8fF
C_p	869.8f
C_p'	200fF

Table 11 Adjusted values for the resistors and capacitors for the resonator using 3-stage Op-Amp

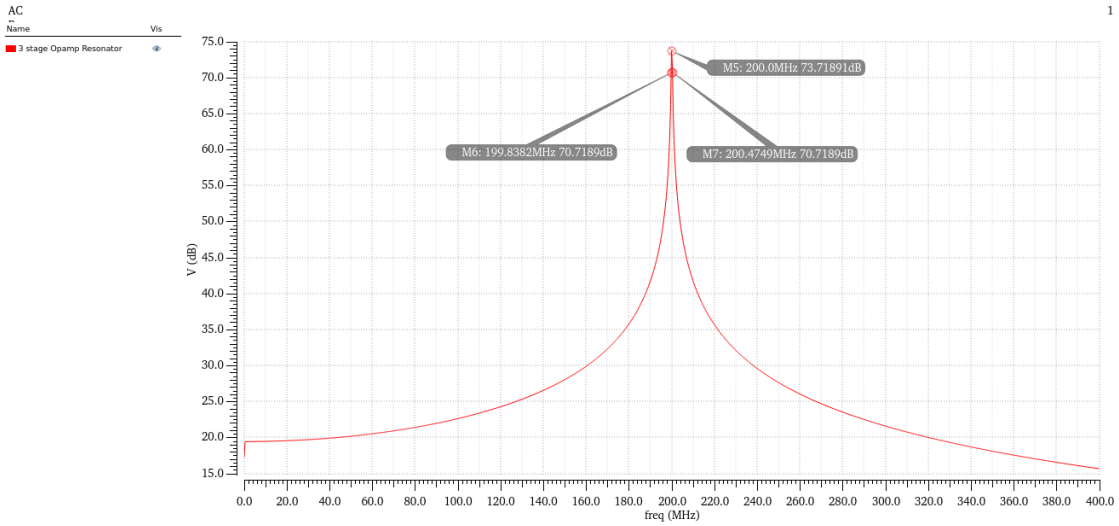


Figure 64 Frequency Response of the resonator using the 3-stage Op-Amp resonator

C. Results of the Three-stage FF Op-Amp's integration into the system

The non-ideal macro-model of the Op-Amp was replaced by the Three-stage FF Op-Amp in the system as shown in Figure 65.

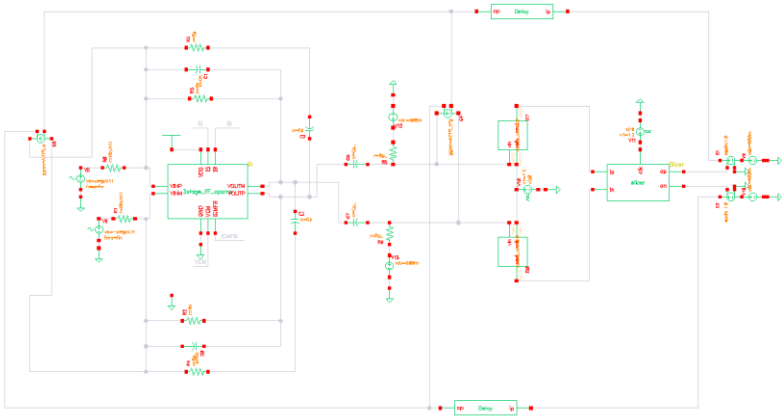


Figure 65 The 3-stage Op-Amp resonator integrated into the system

The power spectral density of the system using 3-stages Op-Amp is shown in Figure 66. The measured SNR of the system's output is $44\ dB$, operating with a supply of $1.2\ V$, and with an input amplitude of $0.335 * 0.025456 = 8.5\ mV$.

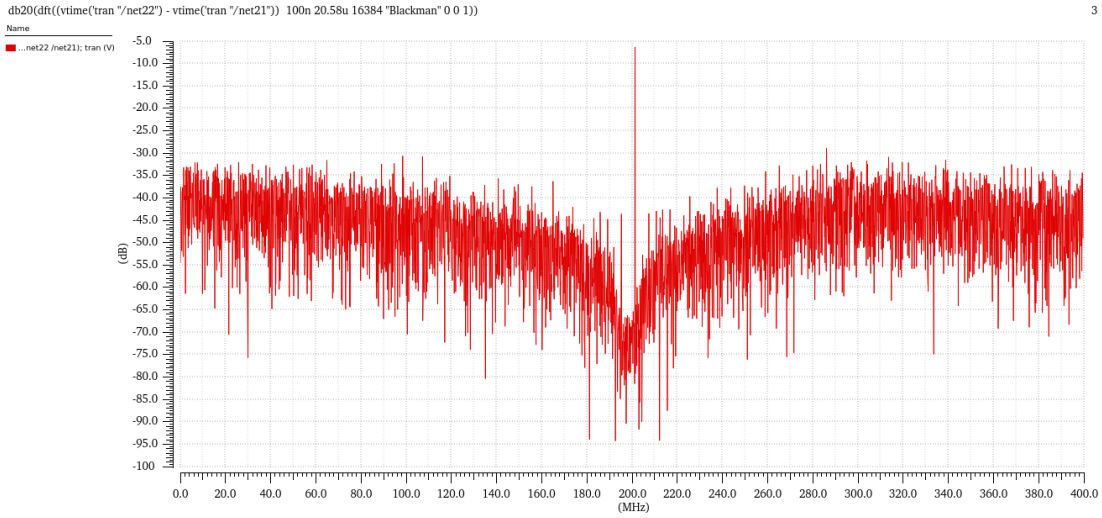


Figure 66 Output power Spectral Density using 3-stage Op-Amp Resonator

III. Four-stage Feedforward-Compensated Op-Amp

A. Frequency Response of the Op-Amp

A testbench similar to that shown in Figure 65 was also used to measure the performance of the Four-stage FF Op-Amp. The frequency response of the Four-stage FF Op-Amp is shown in Figure 67. The Op-Amp achieves a DC gain of $60\ dB$, a Bandwidth of $325\ MHz$, a unity gain frequency of $18.9762\ GHz$, and a phase margin of $74.395\ °$ (as shown in Figure 68).

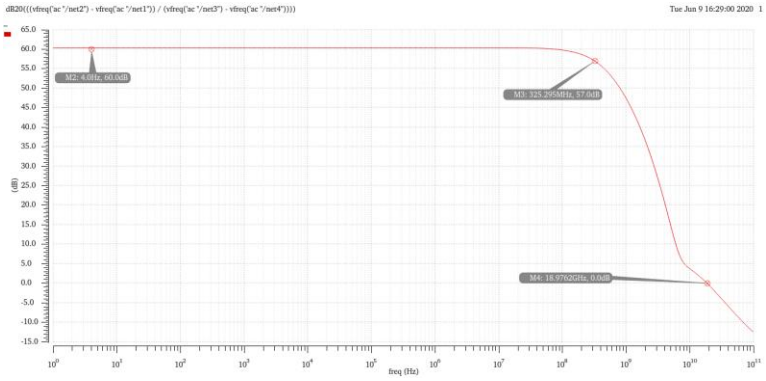


Figure 67 Frequency Response of 4-stage FF Op-Amp

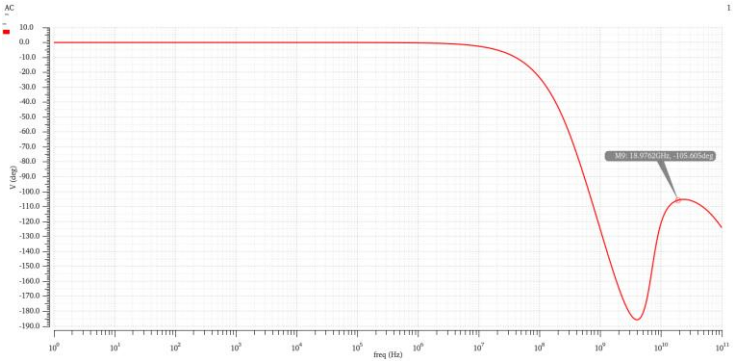


Figure 68 Phase of 4-stage FF Op-Amp

B. Resonator using the Four-stage FF Op-Amp

To account for the parasitics of the Op-Amp, the values of the external capacitors and resistors of the resonator were adjusted as shown in Table 12. The frequency response of the adjusted resonator is in Figure 69. After the adjustment of the resistors and capacitors' values, the resonator has achieved a center frequency of 200 MHz and a quality factor (from Equation 43) of

$$Q = \frac{200.4MHz}{200.4727MHZ - 200.3113} = 2259.3$$

R_{in}	400
R_n	1.62K
R_p	645
R_p'	4K
C_n	500fF
C_p	1pF
C_p'	200fF

Table 12 Adjusted values for the resistors and capacitors for the resonator using 4-stage Op-Amp

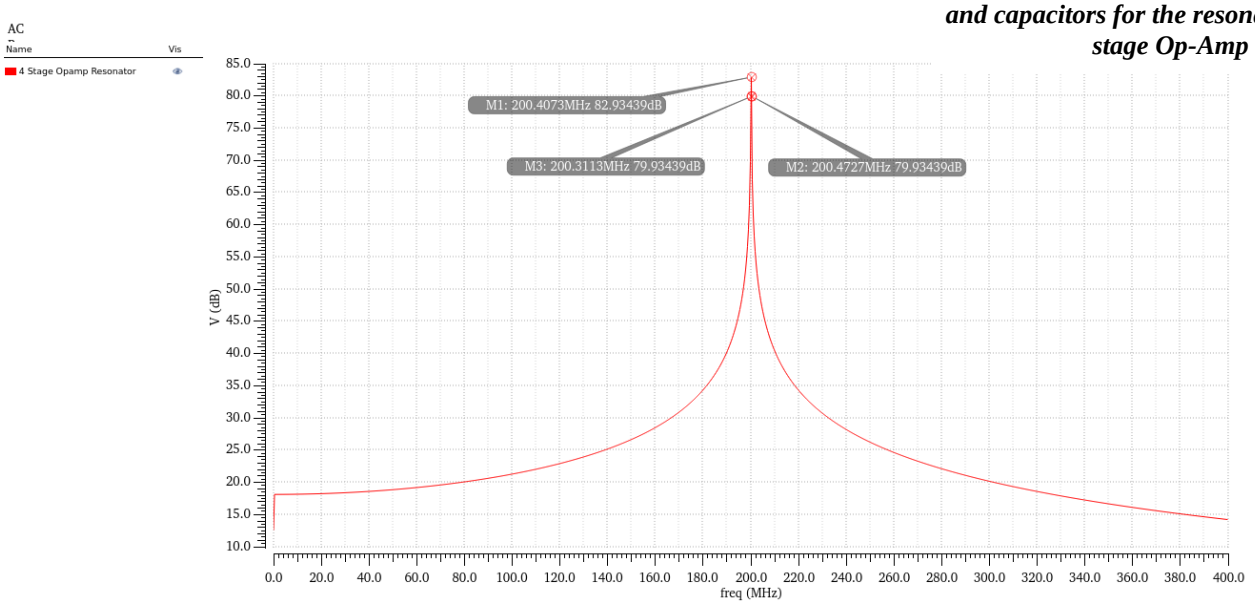


Figure 69 Frequency Response of the resonator using 4-stage FF Op-Amp

C. Results of the Op-Amp's integration into the system

As in Figure 65, the Four-stage feedforward-compensated Op-Amp is added to the system. The power spectral density of the system using Four-stage Op-Amp is shown in Figure 70. The measured SNR of the system's output is 50.7 dB, operating with a supply of 1.2 V, and with an input amplitude of $0.335 * 0.025456 = 8.5\ mV$.

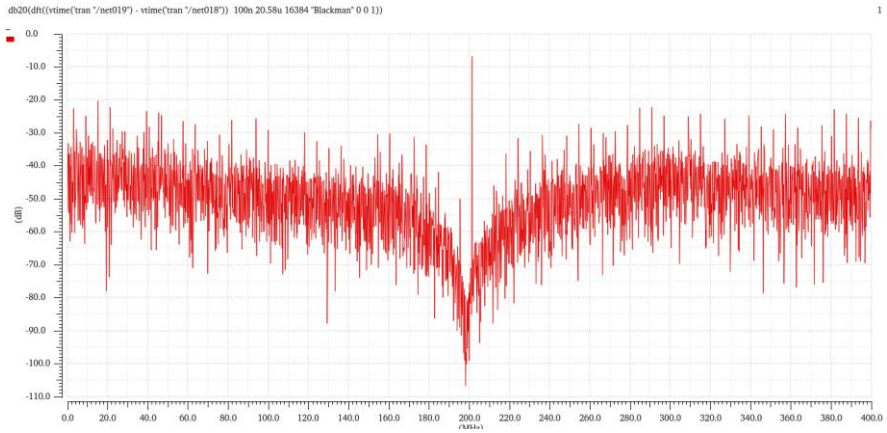


Figure 70 Output power Spectral Density using 4-stage Op-Amp Resonator

4.3.3.2 DAC Implementation

The current required to be provided by the two DACs is first determined. Since DACs used in the system are vccs, I_+ and I_- provided by them are equal. As a result, I_+ is only shown in Figure 71 and it is determined that the 1^{st} DAC should provide $I_+ = 12\ \mu A$ and the 2^{nd} DAC should provide $I_+ = 4.25\ \mu A$. The currents are quite small as the input amplitude of the system is small.

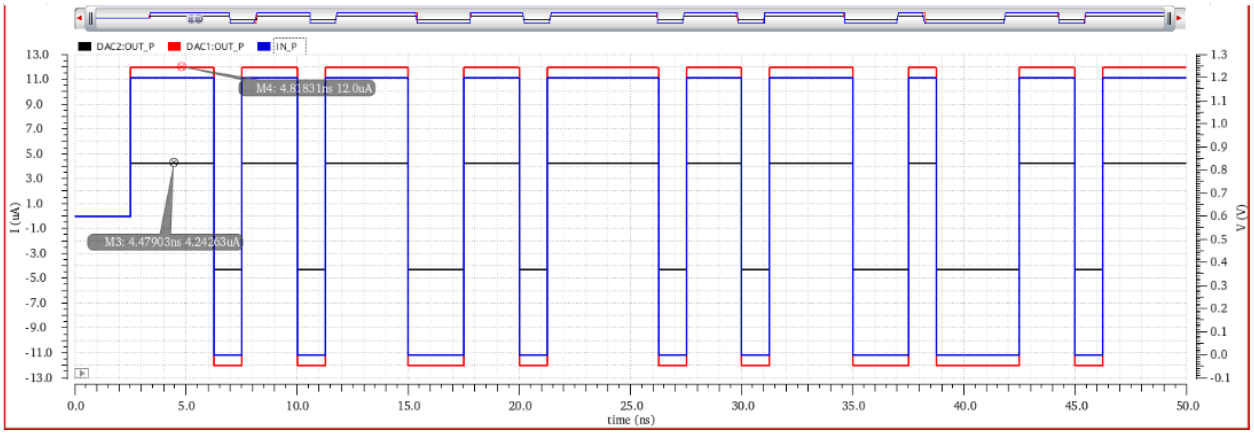


Figure 71 Current required to be achieved from each DAC: 1st DAC (red), 2nd DAC (black) and Positive input of the DACs (blue)

A testbench for the current steering DAC is implemented as shown in Figure 72 to determine the required sizing of the transistors that achieve the required currents. The sizing for the two DACs is in Table 13 and the currents achieved are in Figures 73 and 74.

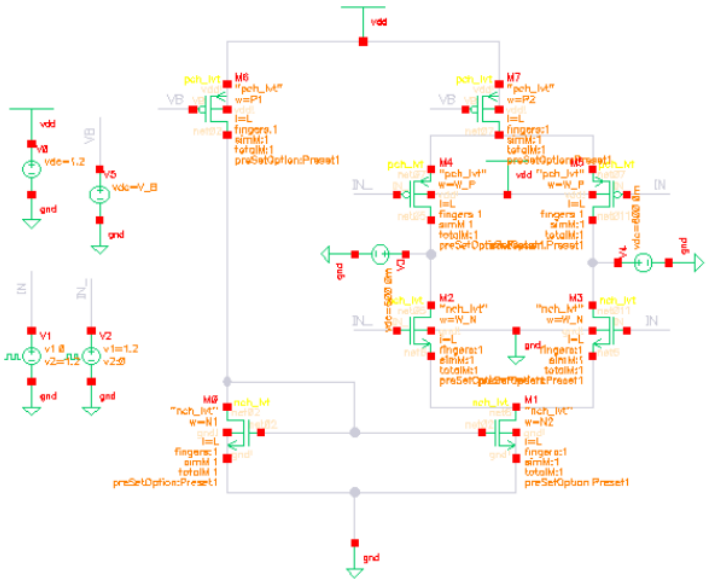


Figure 72 Testbench of the current steering DAC

Device	Aspect Ratio	
	1st DAC	2nd DAC
M0	500n/90n	200/90
M1	1u/90n	400n/90n
M2-M3	500n/90n	180n/90n
M4-M5	1u/90n	300n/180n
M6	500n/90n	200n/90n
M7	1.2u/90n	400n/90n

Table 13 Aspect Ratios of the transistors used in DACs

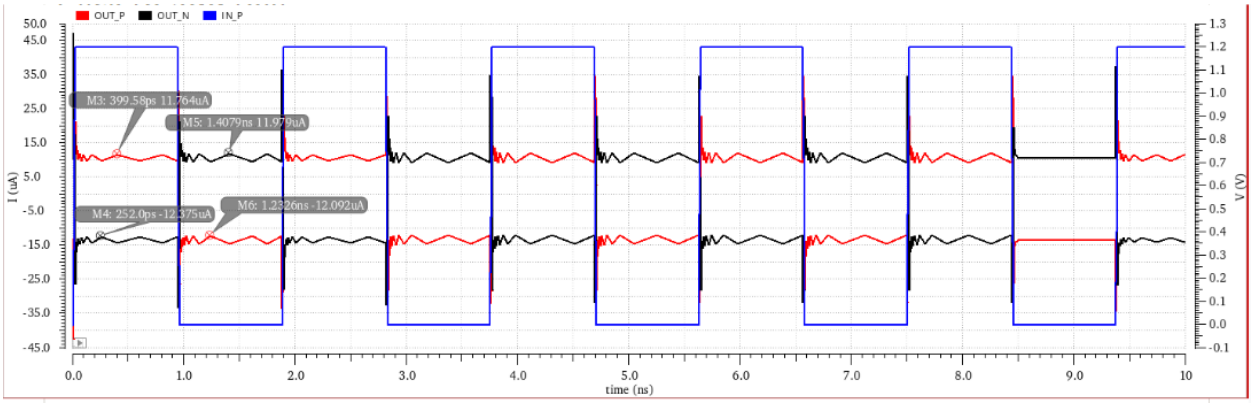


Figure 73 Current achieved by the 1st DAC: Positive terminal (red), Negative Terminal (black) and Positive input (blue)

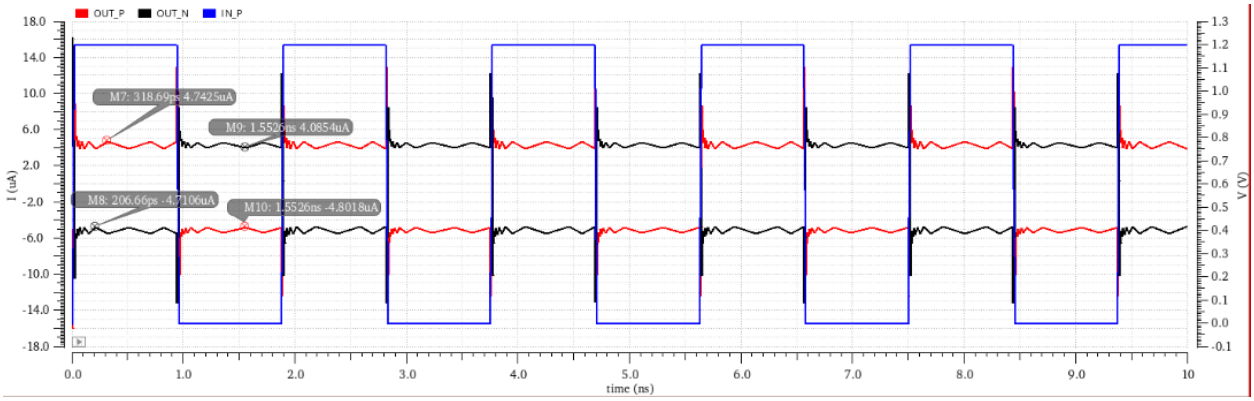


Figure 74 Current achieved by the 2nd DAC: Positive terminal (red), Negative Terminal (black) and Positive input (blue)

The two DACs are integrated into the system and the power spectral density of the system using Four-stage Op-Amp and current steering DACs is shown in Figure 75. The measured SNR of the system's output is 51.4 dB, operating with a supply of 1.2 V, and with an input amplitude of $0.335 * 0.025456 = 8.5\ mV$.

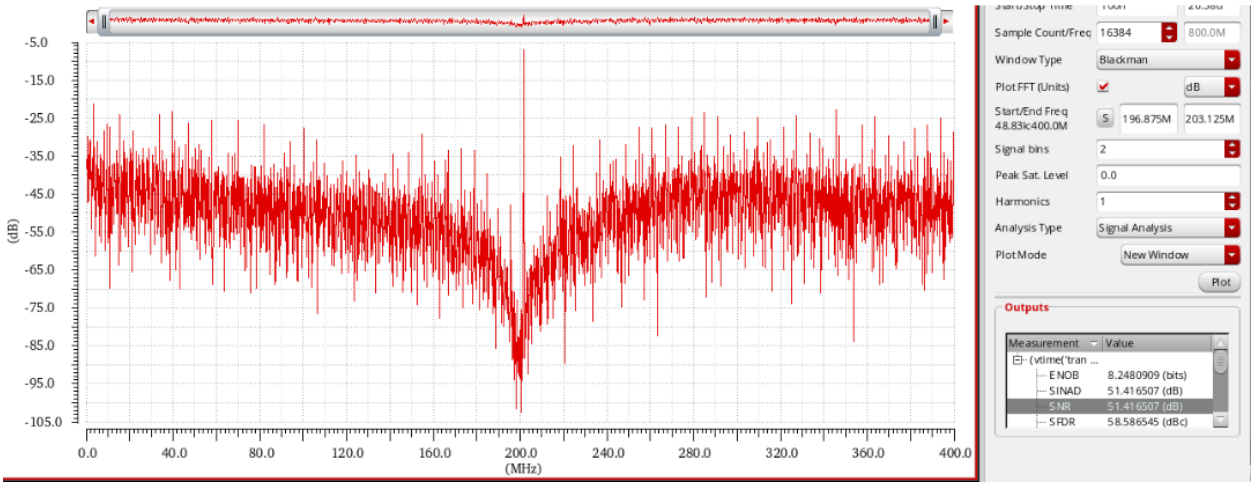


Figure 75 Output power Spectral Density employing 4-stage Op-Amp Resonator and current steering DACs

4.3.3.3 Comparator Implementation

Both systems were simulated using Cadence Virtuoso. Both designs were implemented using *tsmc 65nm* technology as shown in Figure 76.

Figure 76 Comparator implemented designs: a) Modified design, b) Conventional design

Figure 77 shows the transient response of both designs when V_{diff} of $1mV$ was used. The figure demonstrates that the proposed design produces rail-to-rail output in a shorter time while reducing the clock feedthrough problem. One drawback to the proposed design is the slow charging time when switching to the reset phase. This is due to removing two of the charging capacitors. However, this delay is not critical as the reset phase is much faster than other phases, which produces no bottleneck in performance. Figure 78 shows the speed comparison for both designs, using V_{cm} of $0.7mV$ and varying V_{diff} from $1mV$ to $100mV$. The results show that the proposed design offers faster performance while consuming less energy.

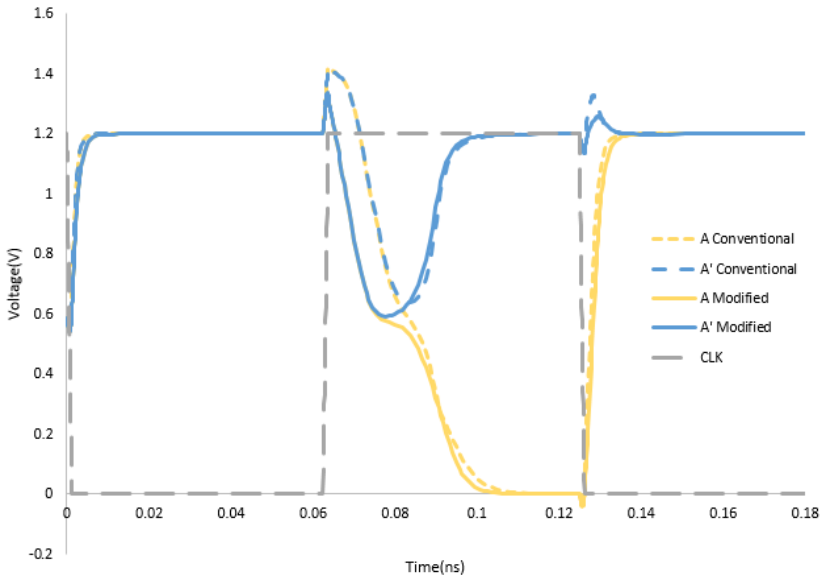


Figure 77 Transient response of both designs

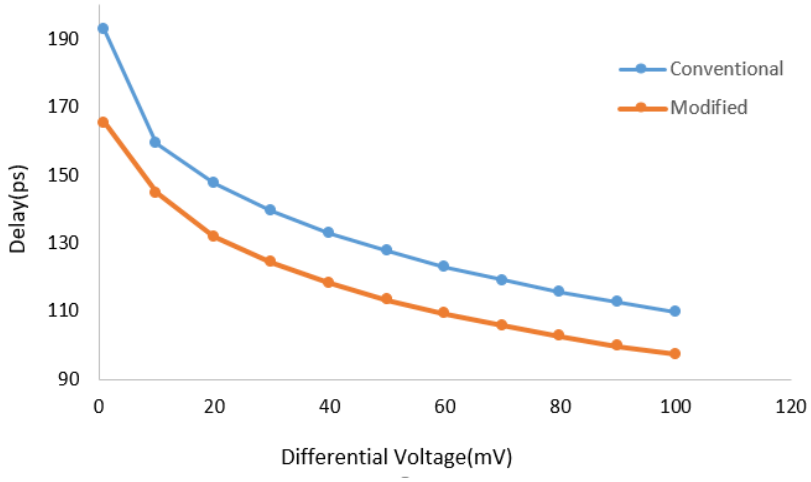


Figure 78 Delay Comparison with regards to Vdiff

4.3.3.4 SR Latch Implementation

The SR latch was implemented using cadence virtuoso in the *tsmc 65nm* technology. Figure 79 shows the implemented design inside Cadence Virtuoso.

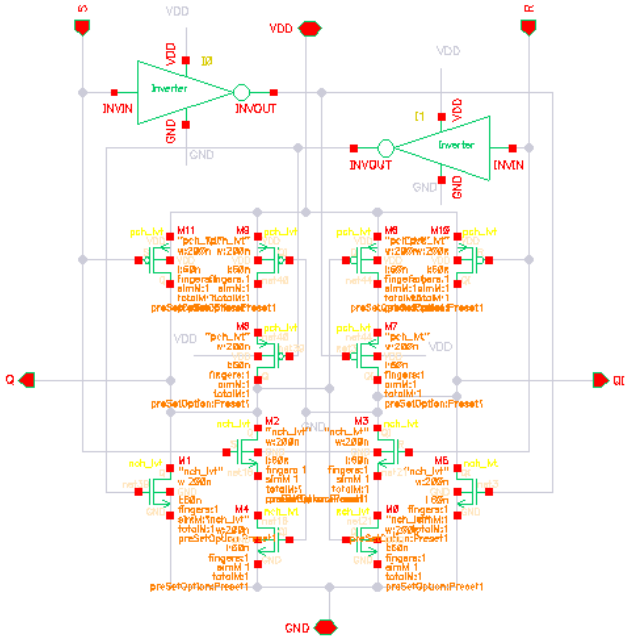


Figure 79 Implemented RS Latch Design

The latch was tested using the comparator as an input while sweeping the input to the comparator from $0.7\,V$ to $1.2\,V$. As shown in Figure 80, the latch successfully holds the value until the comparator output changes and triggers a state shift in the latch.

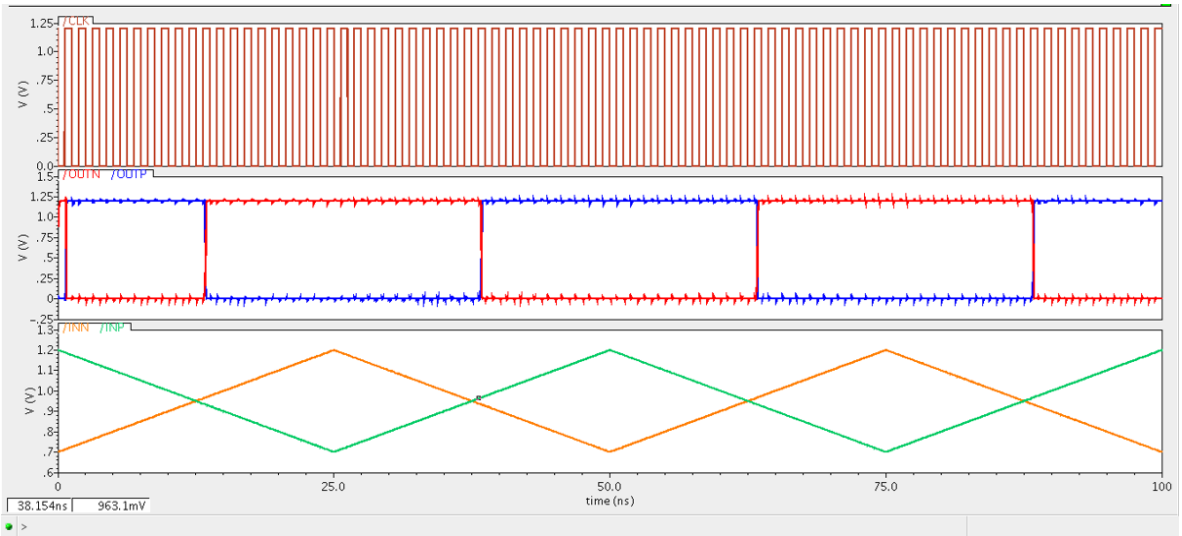


Figure 80 Simulation results of Latched Comparator

The latched comparator is integrated into the system and it introduced an $0.12\ ns$ delay to the system as shown in Figure 81. The power spectral density of the system using Four-stage Op Amp, current steering DACs, and the latched comparator is shown in Figure 82. The measured SNR of the system's output is $45.87\ dB$, operating with a supply of $1.2\ V$, and with an input amplitude of $0.335 * \ 0.025456 \ = 8.5\ mV$.

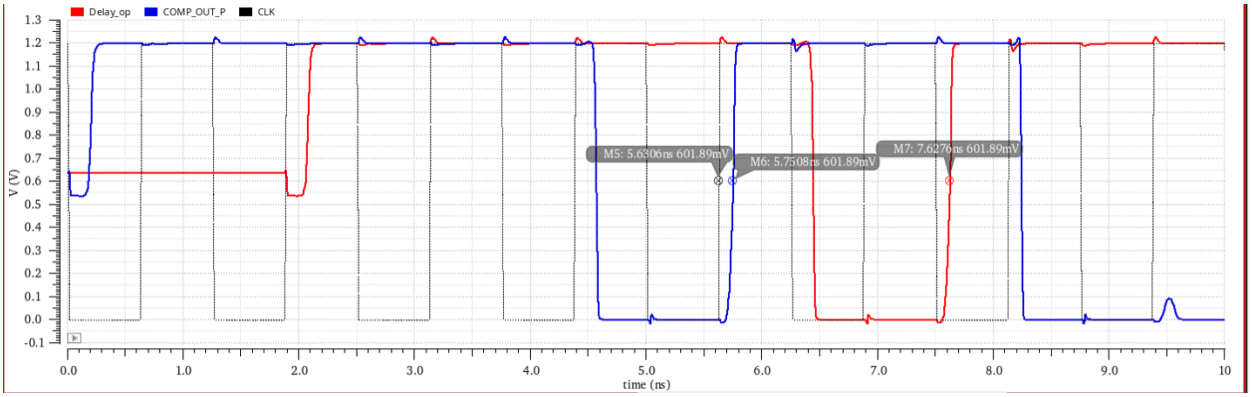


Figure 81 Simulation results of Latched Comparator delay in the system

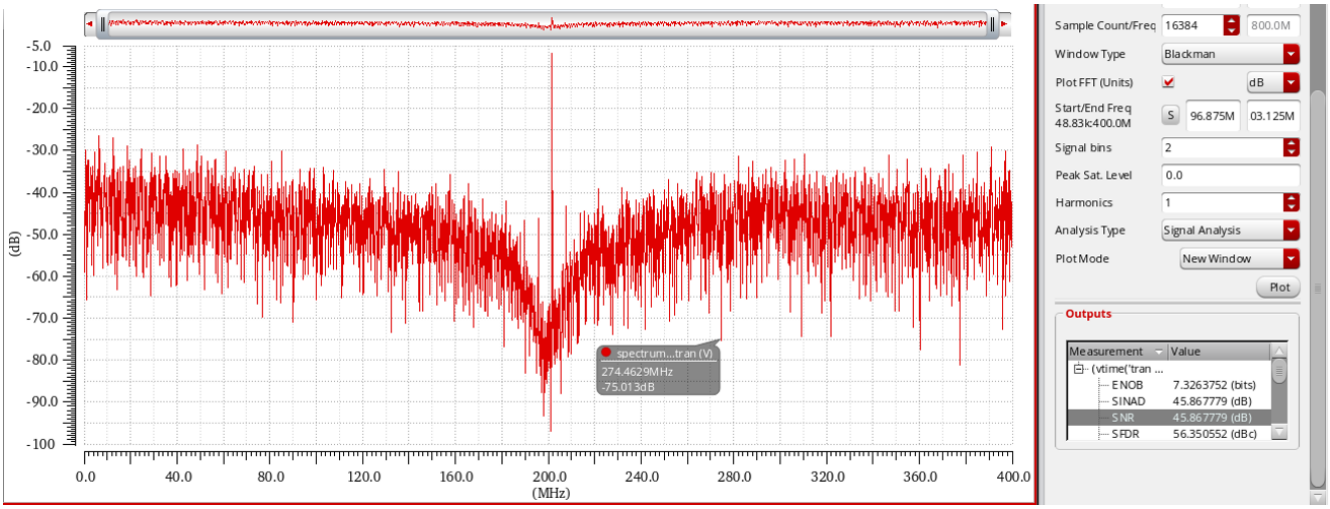


Figure 82 Output power Spectral Density employing 4-stage Op-Amp Resonator, current steering DACs and latched comparator

4.3.3.5 Flip Flop Implementation

Both the flip flop and the negative latch were implemented using the $tsmc\ 65nm$ technology as shown in Figure 83.

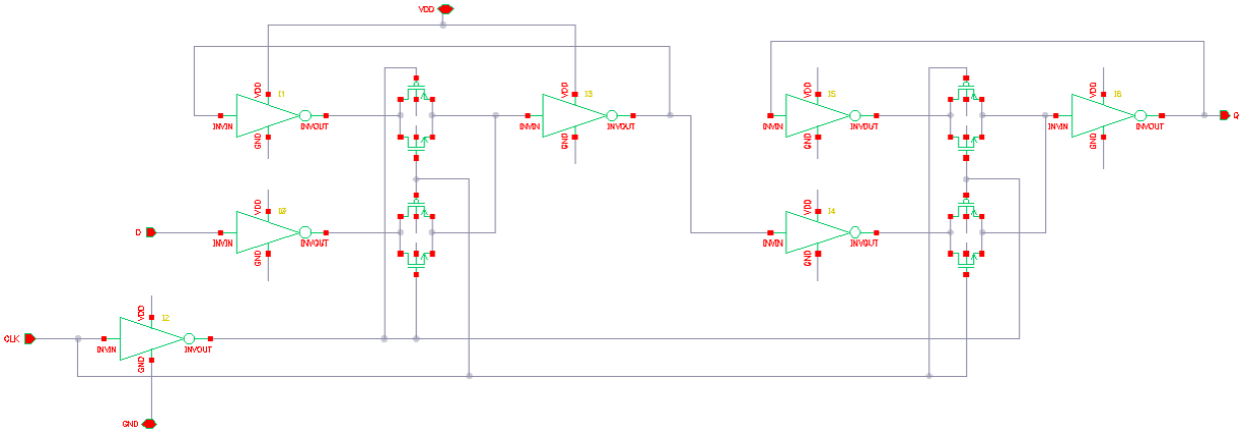


Figure 83 Implementation of Flip Flop using negative and positive latches

The flipflop is simulated and the delay is found to be almost one clock cycle ($1.27\ ns$) as shown in Figure 84. However, the targeted delay is 1.5 clock cycles, so another Negative Latch is added after the flipflop. Adding a negative latch resulted in a $0.62\ ns$ delay. Combining it with the flip flop increased the delay of the system to $1.89\ ns$ which is almost 1.5 cycles ($1.875\ ns$). Delay results are shown in Figure 85.

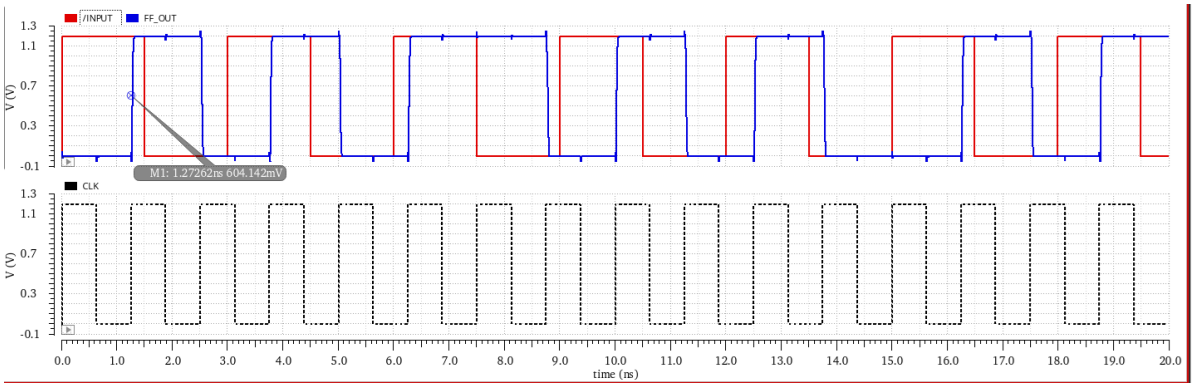
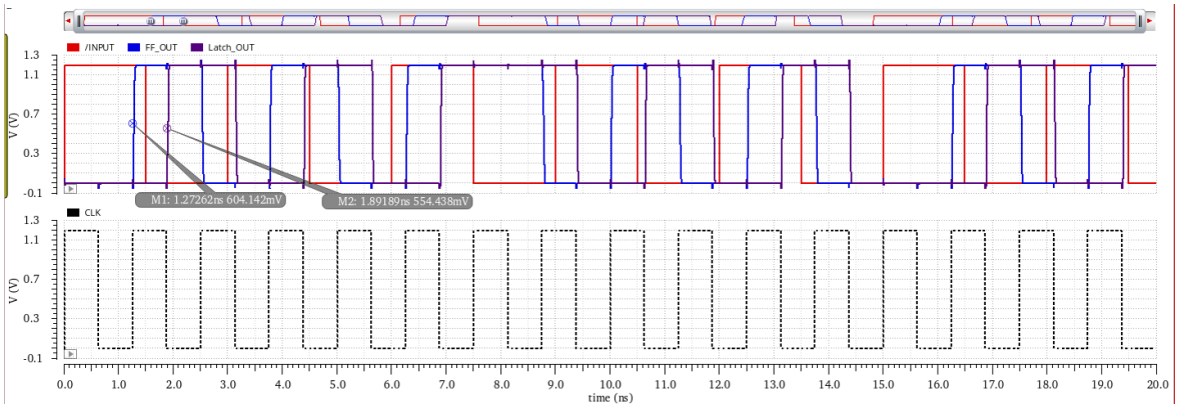


Figure 84 Flipflop Delay test



4.3.3.6 Full Integration of the System transistor-level

The system is fully integrated and all the blocks are transistor-level as shown in Figure 86. From Figure 87, the delay is determined to be 1.9 ns which is almost the required delay (1.875 ns). The power spectral density of the system is shown in Figure 88. The measured SNR of the system's output is 52 dB, operating with a supply of 1.2 V, and with an input amplitude of $0.335 * 0.025456 = 8.5\ mV$. Table 14 summarizes the achieved specs by the system

Table 14 Achieved Specs

Sampling Frequency	800 MHz
Center Frequency	200 MHz
OSR	64
BW	6.25 MHz
Input Amplitude	8.5 mV
SNR	52 dB
ENOB	8 $bits$
SFDR	63.13 dBc
Power Consumption	37.69 mW
DR	60 dB

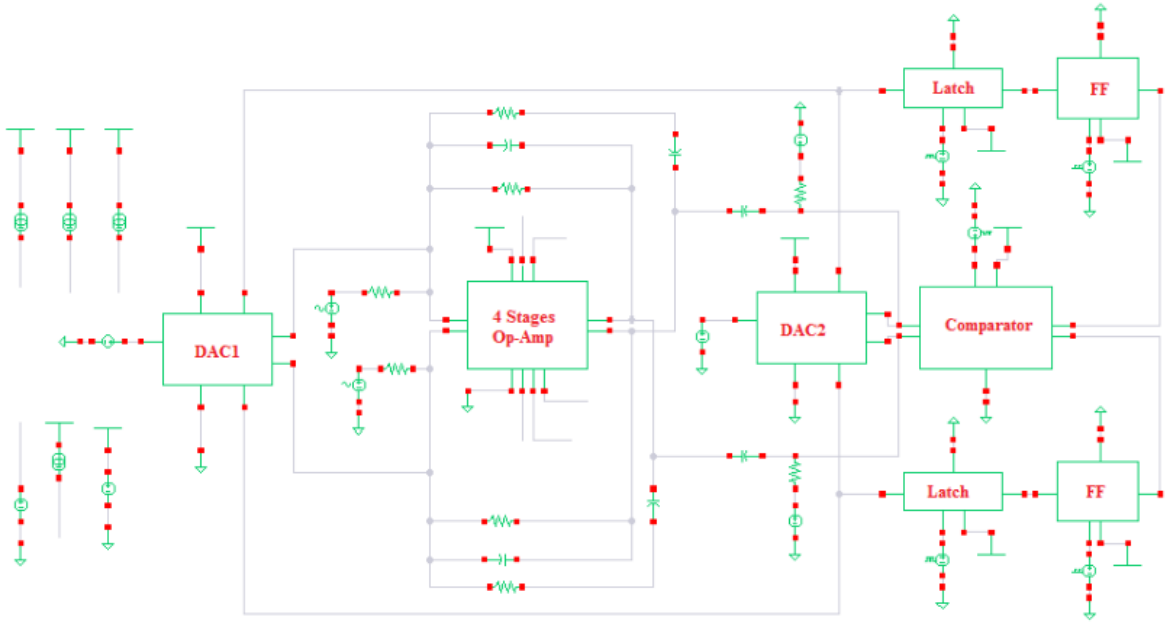


Figure 86 System transistor-level

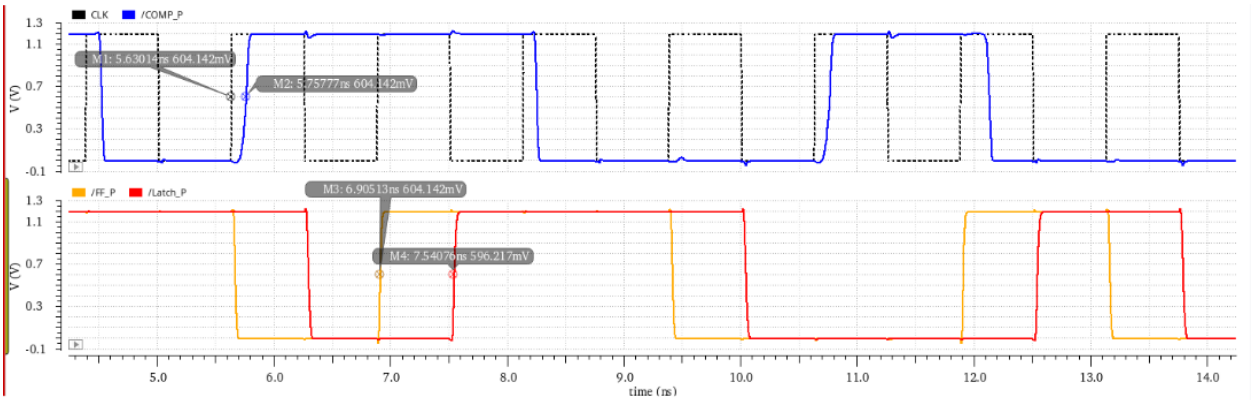


Figure 87 Delay of the system

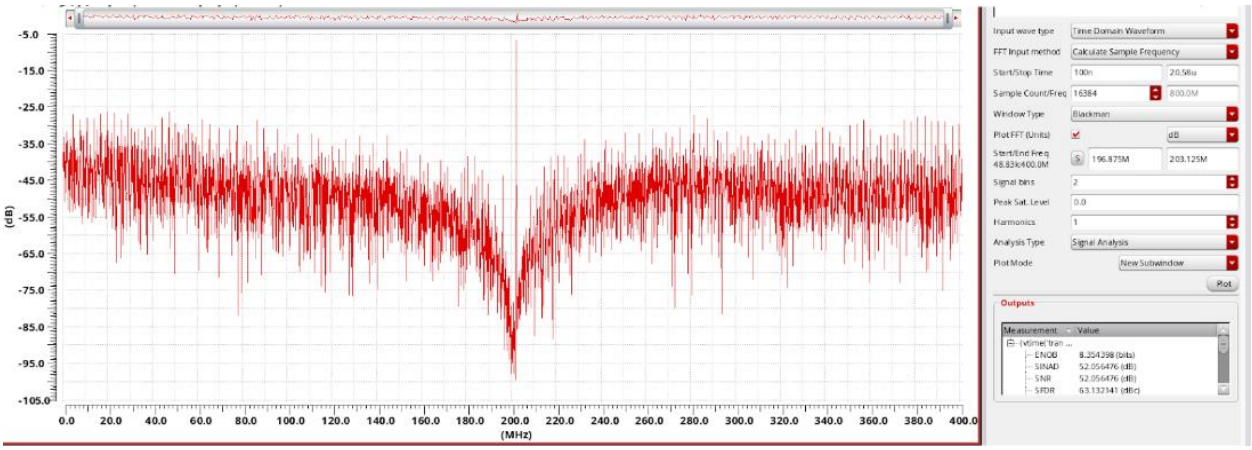


Figure 88 Output power Spectral Density of the system

Since the input amplitude is significantly small (8.5 mV) and comparable to the noise level, Noise analysis is included in the simulation to ensure the stability and operation of the system when noise is included. The power spectral density of the system is shown in Figure 89. The measured SNR of the system's output is 50.06 dB, operating with a supply of 1.2 V, and with an input amplitude of $0.335 * 0.025456 \ = 8.5\ mV$.

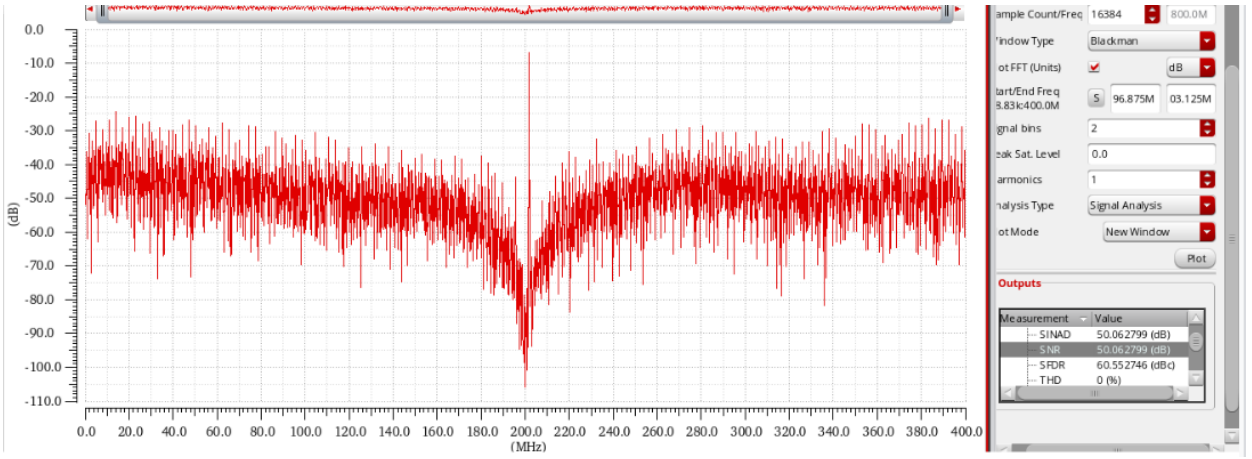


Figure 89 Output power Spectral Density of the system when noise is included

Chapter 5

Cost Analysis

5.1 Cost

The design procedure followed in this thesis aims at decreasing the design time and, hence, the design expenses. The system is first modeled in Simulink using the transfer function of the resonator and ideal blocks for the comparator, DACs, and delay. Then the system is simulated in Cadence using ideal Verilog-a blocks. As a result, the transistor-level design of the block components requires fewer iterations because the relations between the blocks were thoroughly studied in the modeling and simulation stages. The cost of the ADC itself cannot be accurately determined at this stage before the generation of the layout. However, in the design of the resonator, the capacitors used are all less than $1\ pF$ and the resistances used are all less than $10\ k\Omega$ to achieve a small area with a reasonable recurring silicon cost.

5.2 Manufacturability

This design is implemented in $65nm$ CMOS process technology, with a supply of $1.2V$. Due to the small power supply, low-threshold-voltage $NMOS$ and $PMOS$ are used. In future work, this design could be implemented in lower technology nodes.

5.3 Social and Economic Impact

5G wireless technology is expected to deliver higher peak data speeds, lower latency, more reliability, and more capacity when it is fully realized in the next decade. Due to its higher performance and improved efficiency, it is expected to have a huge global social and economical effect. The availability of hardware that supports the 5G technology in a country will allow it to build a stronger network infrastructure that will be beneficial in every social and economic aspect.

5.4 Sustainability

The sustainability of this ADC stems from the sustainability of its main application, SDR receivers. SDR technology is inherently sustainable. Since it performs most of the digital processing in the digital domain, the SDR receiver has wide-range flexibility in its characteristics that can be controlled via the software. This means that the same SDR receiver can be used for multiple different communication standards by programming the digital signal processing block. This makes SDR receivers significantly more sustainable than the traditional RF receivers that only support one communication standard and are thrown away when a new standard is introduced.

5.5 Environmental impact

The fact that mobile devices with SDR receivers can in theory support any new communication standard could decrease the need for new mobile devices. This could decrease the amount of waste resulting from the manufacturing process of new devices or the waste resulting from throwing away old devices. And given that our planet is suffering from a huge waste disposal problem, any means for waste reduction, even if small, should be exhausted. However, further studies are needed to determine the actual possible waste-reduction effect of the SDR technology because the phenomenon of buying a new mobile device does not only depend on the pure need for one but also on changing trends, advertisement campaigns, social norms, and other factors.

Chapter 6

6.1 Conclusion

A second-order CTBPSD ADC is thoroughly analyzed and systematically implemented in Cadence Virtuoso using 65 nm CMOS process technology. The system is designed to have a sampling frequency of 800MS/s with a bandwidth of 6.25 MHz at 200MHz center frequency with a power supply of 1.2 V and a delay of one-half clock cycles. The system incorporates a differential single Op-Amp resonator as a loop filter, a modified StrongArm latched comparator as the quantizer, two current-steering DACs in the feedback loop, and a master-slave positive-edge-triggered register and a negative latch to incorporate the required delay.

The final transistor-level ADC achieves an SNR of 52 dB, an SFDR of 63.13 dBc and an ENOB of 8 $bits$ with a power consumption of 37.7 mW. Furthermore, the transistor-level ADC is simulated while including the noise of the system. The simulation verified the operation and stability of the system and achieved an SNR of 50.06 dB.

Finally, the cost analysis of the system was discussed from the cost, manufacturability, social and economic impact, sustainability, and environmental impact perspectives.

6.2 Future Work

- The layout design of the complete system is required to further include parasitics expected to be added to the system such as routing parasitics, as well, verification of the system post-layout.
- Modifying the resonator design to include a method that provides tunability to the center frequency and quality factor of the resonator, such as using capacitor banks. Incorporating tunability in the system allows the receiver to be suitable for multiple standards.

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