NEURAL STIMULATOR

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Table of Contents

List of Tables

List of Figures

List of Symbols and Abbreviations

FDA	Food and Drug Administration
VNS	Vagus nerve stimulation
TG	Transmission gate
DAC	Digital to analog converter
CMOS	Complementary metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
NMOS	n-type metal oxide semiconductor electron channel
PMOS	p-type metal oxide semiconductor holes channel
OTA	Operational transconductance amplifier
DC	Direct current
DAC	Digital to analog converter
Sat	Saturation region
PVT	Process Voltage Temperature
TT	Typical-typical Process variation
FF	Fast-Fast process variation
SS	Slow-Slow process variation
SNFP	Slow N-type fast P-type
FNSP	Fast N-type slow P-type
SFE	Stimulation front end

DBS	Deep Brain Stimulation
CCS	Current Controlled Stimulation
INS	Implantable neurological stimulators
VCS	Voltage Controlled Stimulation
PE	Power Efficiency

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Abstract

This thesis discusses designing, simulation and implementation of the SoC electrical stimulator. Represented two different implementation techniques for stimulation, to reach our goal.

The first design aims to implement a multiple-waveform current stimulator circuit that integrates the adaptive generation of the three most popular stimulation waveforms (rising exponential, falling exponential and rectangular). Switching technique is used to merge repeated blocks to reduce static power consumption, reject charge accumulation and increase efficiency. The stimulation amplitude range can be varied from 0 to 2mA in a manner that each range can be divided into 16 steps by a 4 bit binary weighted digital to analog converter (DAC). The simulated power consumption of the proposed stimulator for one channel is 12.3 µW and the maximum achieved power efficiency is 96.47 %.

While the second design is a high-voltage-tolerant stimulator with adaptive loading in a standard process, in order to avoid the use of high-voltage transistors. The proposed stimulator consists of a high-voltage generator (charge pump), a pair of high-voltage-tolerant output drivers, and a pair of current controllers, the stimulator has been designed to deliver biphasic stimulus currents with H-bridge topology. The biphasic stimulus pattern a constant 30µA current. With average static power consumption 429.68 µW. And with lower charge pump clock frequency 10 times less than previous work in this field, which will result in a better power efficiency. Finally, smaller silicon area is expected compared to previous circuits due to using less number of charge pump stages and avoiding some area consuming techniques such as Triple well technique.

Motivation

DBS therapies are options for patients with drug resistant epilepsy who are not candidates for respective epilepsy surgery. In 1997, the US Food and Drug Administration (FDA) approved vagus nerve stimulation (VNS) implant as a side therapy for reducing the frequency of seizures in patients. [29]

Neurons of the brain communicate information by means of electricity. A number of invasive and noninvasive approaches in order to hack the nervous system through electromagnetism and thus exerting control over the organs and systems of the organism have been developed in the last 30 years. Stimulation of the nervous system finds application in medical and non-medical areas, e.g. vagus stimulation for managing epilepsy and treatment-resistant depression, or cochlear implants for hearing loss.

Deep Brain Stimulation (DBS) is an established invasive technique based on direct electrical interaction between an electronic devices and the brain (by electrodes). Therapeutic DBS was developed during the eighties and approved by the FDA in the late nineties and early 2000s. Stimulation is delivered via chronically implanted leads, typically one (unilateral) or two (bilateral). Due to its high cost inflicted by the brain surgery, system tuning, and maintenance, DBS is currently only established as a last-resort treatment in neurodegenerative diseases such as Parkinson's Disease, epilepsy, essential tremor. It is a flexible treatment and gives the physician access to several adjustable stimuli parameters that can be manipulated to produce a satisfactory outcome.

A complete closed-loop epileptic seizure monitoring and controlling system in an implantable device circuit as shown in Fig. [1] should have:

1) **Detector**: to get the brain signal
2) **Signal Processor**: convert the brain analog signal to a digital one and analyze it in order to detect the seizure when happened and hence, it sends a control signal to the stimulator.
3) **Stimulator**: the output stage of the device which response back with a seizure anti-response signal in order to suppress the detected seizure.

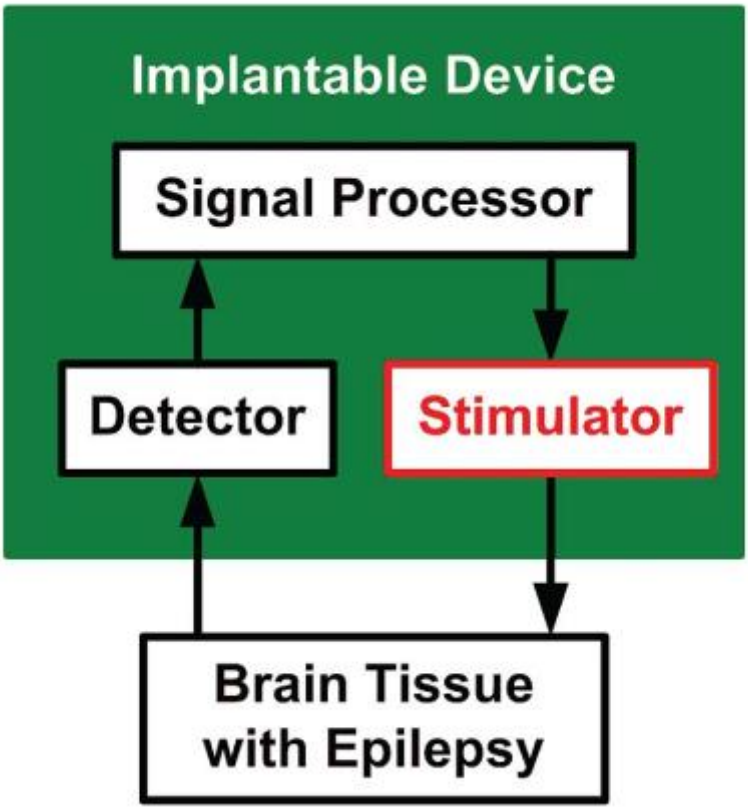

Figure 1: Whole implantable device

Presented thesis is going deep into the last stage of that device which is the Stimulator. Two different designs are discussed deeply later on.

Chapter 1: Introduction

In this thesis we are going to prove electrical stimulation techniques with high power efficiency. The thesis flow will go as following

Chapter 2: survey about different types of neural stimulators and comparison between different specifications

Chapter 3:design 1

Chapter 4: Design II is discussed, this design shown new manner to implement three different waveforms for stimulation current to collect more benefits, technique is used TG switching scheme to reduce static power consumption hence increase efficiency of stimulator. Post layout simulation and layout technique is discussed

Chapter 2: Survey

Many existing and emerging therapies use implantable neurological stimulators (INS) >> DBS to alleviate sensory deficits such as epilepsy, manage chronic pain, control bladder function, and eliminate motion disorders such as paralysis, Parkinson's disease, and essential tremor. Efficacy and safety of these therapies are the key factors that result in their acceptance and popularity among patients and professional caregivers. These factors result from a combination of parameters that are partly clinical and partly engineering [1]. The clinical parameters are related to the mechanisms of neural stimulation, structures within the central and peripheral nervous system that are targeted for stimulation, and the methods undertaken for surgical intervention. The engineering parameters are broad and cross over multiple disciplines. However, those related to electrical engineering are the circuitry inside the INS>>DBS, stimulating electrodes specifications (electrochemistry), and electrical characteristics of the neural tissue. Improving the efficiency of the INS circuits has always been a major goal for electrical engineers involved in design of implantable devices to shrink the implant size by reducing the battery size or extend its lifetime. Smaller implants are safer because they are less invasive and have a lower risk of post-surgical complications. There are two sorts of power consumption in an implantable micro stimulator. A smaller part of the power drained from the battery is consumed in the INS internal circuitry, resulting in heat dissipation. A larger portion of the power is transferred into the tissue through stimulus pulses. The internal power consumption can be reduced by lowering the operating voltages and utilizing low power circuit design techniques. The amount of transferred power to the neural tissue, which is needed to produce the desired neurological effects depends on several factors that can be categorized into the following groups:

1- Stimulation front-end (SFE) circuitry, i.e. part of the INS circuitry that directly drive the electrodes.
2- Stimulus characteristics including waveform, amplitude, pulse width, and stimulation frequency
3- Electrode characteristics including size, geometry, material, impedance, surface roughness, and safe charge injection density.

4- Properties and excitation thresholds of the targeted neural tissue, activation function, strength-duration, and strength-distance relationships.

There have been extensive efforts dedicated to every one of the above categories to model and understand the effects of each parameter in improving the efficiency and efficacy of neural stimulation. However, there are few models that take into account the effects of multiple parameters from two or more groups without over simplification or becoming very complicated. Therefore, it is described types of popular SFE circuits based on voltage control and current control. It is compared them to a new type of SFE circuit based on charge control and described the architecture of an integrated switched capacitor based micro stimulating system. To choose more efficient stimulation a comparison between the voltage, current, and charge controlled SFE circuits is done [2].

Stimulator Types:

A. Voltage Controlled Stimulation The voltage SFE consists of an amplifier which amplifies the input voltage set by the DAC. The gain of this amplifier can be adjustable Fig. 2.

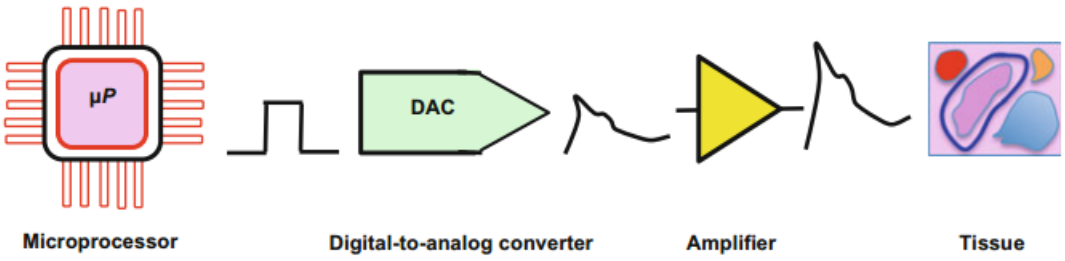

Figure 2: Voltage Controlled Stimulation

B. Current Controlled Stimulation The SFE for current stimulation consists of a voltage to current converter, the input of which is set by the DAC. The CCS-SFE has an output range which is varied by DAC inputs.

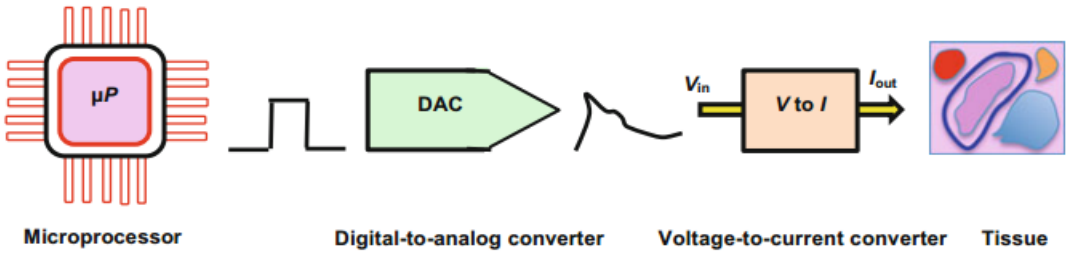

Figure 3: Current Controlled Stimulation

C. Switched-Capacitor Based Stimulation or charge-mode stimulation, the stimulator consists of a bank of capacitors (Fig. 4 This bank of capacitors is charged sequentially from a DC–DC converter. The supply voltage of DC–DC converter is adjustable. So, the total charge on a capacitor is alterable. The capacitors are discharged into the tissue. This discharging action is carried out through several electrodes by digitally controlled switches. Every capacitor can be discharged into the load consecutively. In this way, quantized amounts of charge are impelled into the tissue. The charge injected over each stimulation pulse is measured. For this measurement, the current is integrated over the period of the pulse. But the main issue is that the circuit requires large capacitors. The large capacitors can only be provided in off-chip form. Difficulty in provision of large-value on-chip capacitors is the main disadvantage of this technique. Otherwise, it serves as a unification of advantages of VCS and CCS methods. It combines the improved power efficiency and safety of VCS with the superior charge-controlling ability of CCS method.

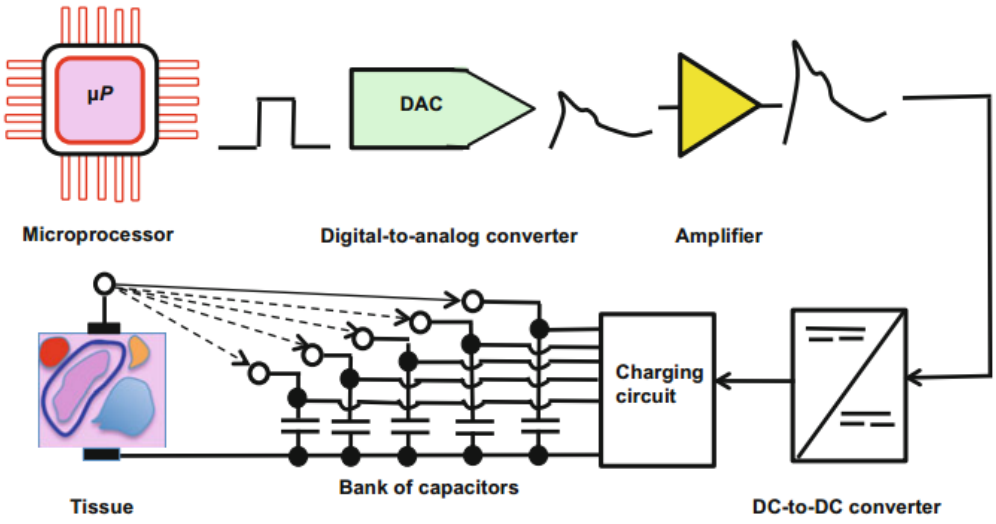

Figure 4: Switched Capacitor Based Stimulation

Stimulation parameters:

- Fail Safe

For safety consideration, a large off-chip DC capacitor in μF range is connected in series with the electrode by connecting this capacitor, DC currents are stopped from reaching the tissue. Protection against any accidental semiconductor chip failure is also assured. This is because any resulting excessively harmful current cannot flow in the body be remembered that DC current integration will cause voltage buildup on the capacitor. Hence, the capacitor must be regularly discharged. Among the disadvantages of this technique, it must be mentioned that the value of blocking capacitor has to be the electrode–electrolyte capacitance. Generally, this large capacitor cannot be integrated. It is externally connected with the chip. In multichannel implants, several such capacitors are required. One capacitor is needed for each electrode. A large amount of space is therefore wasted. Lastly, the discharging step for charge balancing is an uncontrolled process.
Short circuit electrode

Second method is commonly used for a biphasic pulse. It removes any leftover charges present due to mismatching effects. Following each stimulation cycle, short-circuiting of the electrodes helps to discharge them. The reason for the inability to know discharging time accurately is the wide variation in current matching and electrode impedances. Further, changes take place in their behavior over a period of time. Nonetheless, the blocking capacitor issues are steered clear off. is this method is used in second design.

- Avoiding Charge accumulation

The charge accumulation caused by the dc leakage current or by the mismatch during biphasic stimulation will result in undesirable effects to the tissue.

- Small area

It is known that the chip will be embedded in the brain of a human so the area of chip should be compact and suitable.

- High-Voltage Tolerance

low-voltage CMOS technologies have been used to implement the integrated circuits for biomedical applications. The gate-oxide thickness of MOS transistor has been shrunk to improve circuit performance and operating speed in advanced CMOS technologies. In addition, the power supply voltage in CMOS integrated circuits has also been scaled down to follow the constant-field scaling requirement and to reduce power consumption. However, the stimulator with low voltages devices must deliver the stimulus current with high voltage across the load (electrode). The high-voltage tolerant output driver must be designed in low-voltage CMOS technologies to prevent from the reliability issues, such as electrical overstress on gate oxide. The stacked MOS configuration has been reported to allow high voltage across the output driver in chapter 3 design 1. [3]

- Efficiency

Efficiency of each SFE can then be simply calculated using PE equation mentioned below. In traditional current-mode stimulator with constant current usually has the lowest power efficiency to voltage-mode and charge-mode stimulator so, it is designed in design 2 chapter 3 raising and falling exponentially current stimulation. It is proposed to use these currents to eliminate the headroom and improve PE. With an exponentially rising and falling voltage on the stimulation electrode approximately constant and thus minimizes the power shaded area.

$$\text{PE}=\mathcal{E} = \frac{P_{out}}{P_{in}} = \frac{I_{stim} * V_{load}}{P_{static}+(I_{stim}*V_{DDH})}$$

- Monopole & Bipolar

The difference between monopole and bipolar recordings is their placement. Specifically, in bipolar recordings the electrodes are placed both on the scalp, i.e., on the interest area, as it can be seen in Fig. [5][a]. On the other hand, in the monopole

electrode placement method, one of the points of measurement is placed on the scalp, and the other one is located away from the interest area, as shown in Fig. [5][b].

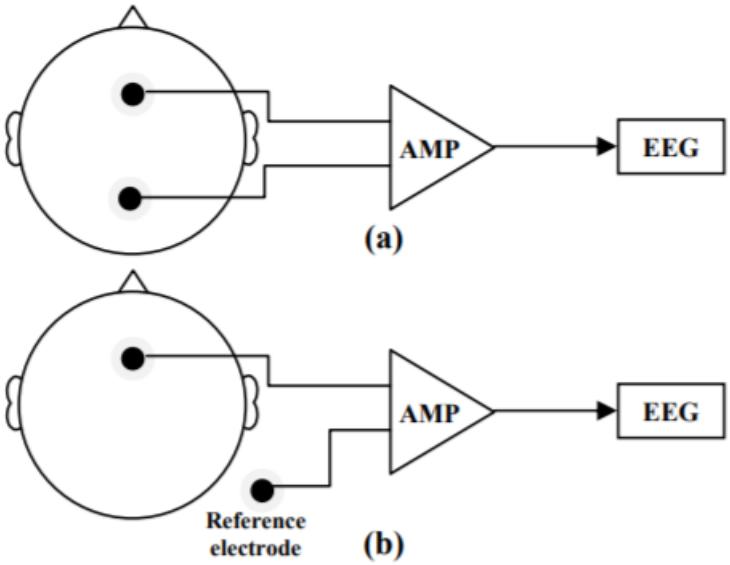

Figure 5: Monopole (b),bipolar (a)

- Monophasic & Biphasic

a “monophasic” wave is a unidirectional wave. It consists of only one type of pulses, either positive pulses or negative pulses. “Biphasic" refers to two phases, or pulses, of two different intensities alternating with each other during treatment. Biphasic current is considered the most versatile of the stimulation therapy waveforms because most devices feature settings that allow control of amplitude (intensity), stimulation (voltage), current, and duration of each pulse. With its versatility and effectiveness, Biphasic current e-stim can be used Fig. [6]

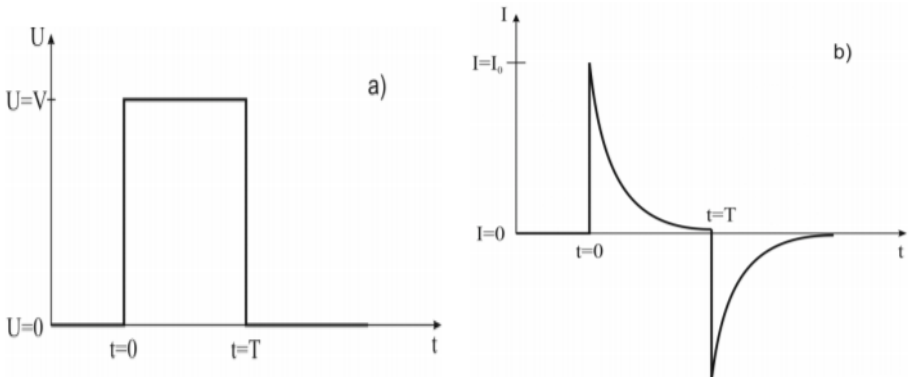

Figure 6: Monophasic & biphasic

Chapter 3: Design I: Adaptable Stimulator

3.1 System overview

Design one have built on the idea of the adaptability of the VDD with change in the electrode impedance. A closed loop stimulator as shown in Fig. [7] uses the Current Controller as a feedback loop which generates the enables signal for the charge pump or the high voltage generator control circuits, when the charge pump is working on the higher frequency the VCC which is the output of the charge pump and the supply voltage of the Anodic and Cathodic High-Voltage Tolerable Output Driver which is connected to the electrode as seen, and as the circuit is adaptable to the change in the electrode impedance, when the impedance of the electrode goes higher hence the output current becomes lower than the wanted value as it's constant current 30uA as a result of that increase in the impedance. Now, is the role of the current controller to change the enable signals in order to run the charge pump on the higher frequency mode which is able to cover the whole range of impedances. And hence the loop repeats this function again and again in order to remain the output current constant.

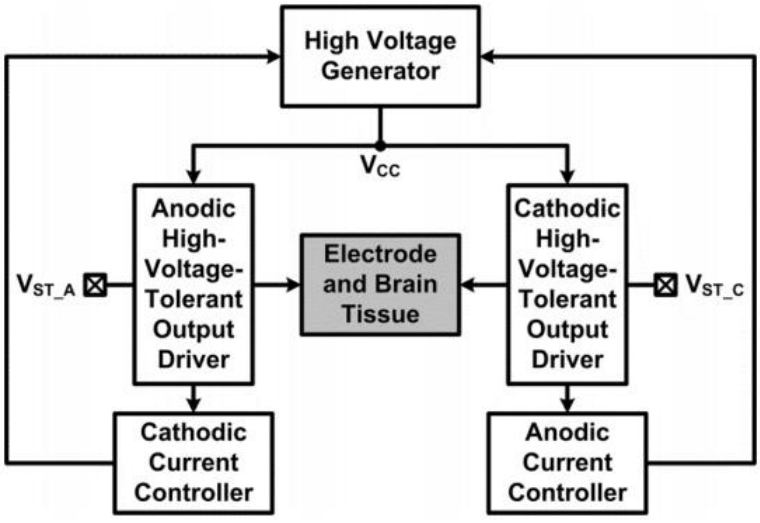

Figure 7: The Whole circuit of design I [31]

3.2 Charge pump (High voltage generator or Step-up DC-DC Converter)

3.2.1 Definition

Charge pump circuits have been often used to generate dc voltages those are higher than the normal power supply voltage (VDD). Some common applications of charge pumps can be found in the nonvolatile memories, such as EEPROM or flash memories, to write or to erase the floating-gate devices [4] – [5]. In addition, charge pump circuits had been used in some low-voltage designs to improve the circuit performance [6] - [7]

3.2.2 Different architectures

Charge Pumps are simply a way to pump up the input voltage to reach higher values with the help of clocks on a charging capacitors.

Main idea of charge pump is cleared in Fig. [8]

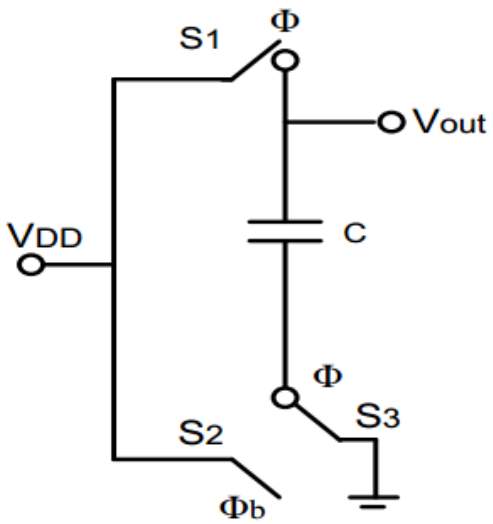

Figure 8: Voltage Doubler

This circuit is called a Voltage Doubler, and it consists of a capacitor and three switches (S1, S2 and S3) when S1 and S3 are closed and S2 is open. The capacitor C charges to VDD and the charge on capacitor is (C*VDD). when S1 and S3 are open

and S2 is closed. And by applying the charge conservation concept, we get

$$Q = CV_{DD} = C(V_{out} - V_{DD})$$

hence the output voltage is:

$$V_{out} = 2V_{DD}$$

But, in practical implementation of charge pumps switches are replaced with N-MOS and P-MOS as switches with two anti-phase clocks [8]. Charge pump differ from one architecture to another, everyone has its advantages and disadvantages.

Starting with Dickson architecture shown in Fig. [9]

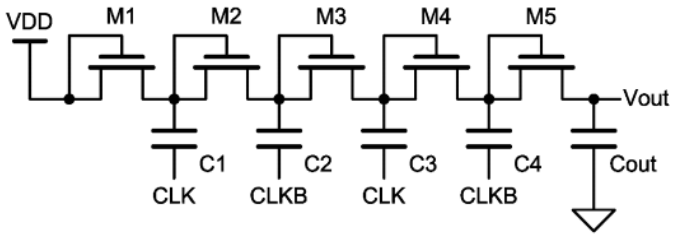

Figure 9 Dickson Charge pump

Vout can be expressed as,

$$V_{\text{out}} = \sum_{i=1}^{5} \left(\text{VDD} - V_{t(M_i)}\right)$$

where, Vt is the threshold voltage which equals to Vds of the drain connected transistor when it's on.[9].

But,

Traditionally, the bulk terminals of the diode-connected N-MOS or P-MOS in the Dickson charge pump circuit are connected to ground. Hence the threshold voltage of the diode-connected N-MOS or P-MOS becomes larger due to the body effect when we have more stages with higher pumping ratio. Therefore, the pumping efficiency of the Dickson charge pump circuit is very bad with higher number of stages.

Several techniques were presented in order to avoid this problem in Dickson architecture.

Using triple-well process, the floating-well technique or the source-bulk connected devices are all different ways in order to eliminate the body effect in Dickson Charge pump.

But, the floating-well technique may generate substrate current in the floating-well devices which may influence other circuits in the same chip while The source-bulk connected technique increases the parasitic capacitance at each pumping node due to the large bulk-to-well PN-junction capacitance, so the pumping capacitors have to be larger which will consume more silicon area, which is bad for fabrication, our aim here.

other modifications were presented by lots of designers as Wu and Chang [10] shown in Fig. [10]

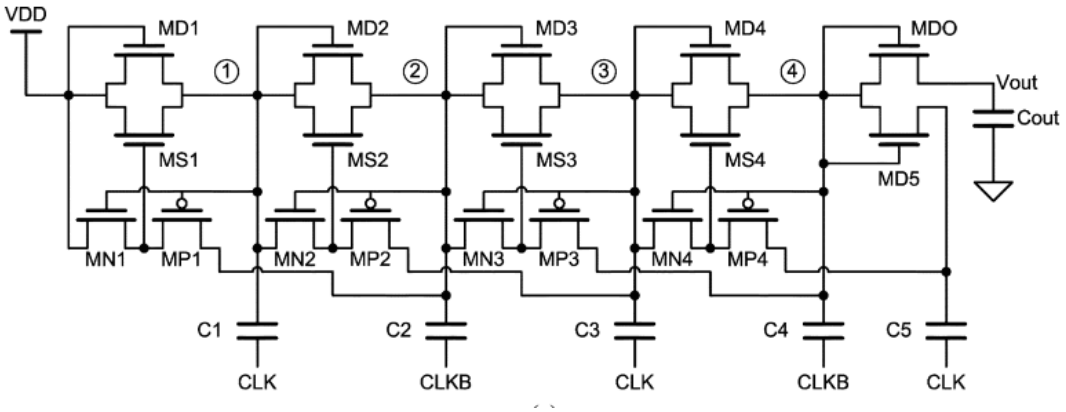

Figure 10: Wu and Chang charge pump circuit

And Pelliconi charge pump [9] shown in Fig. [11]

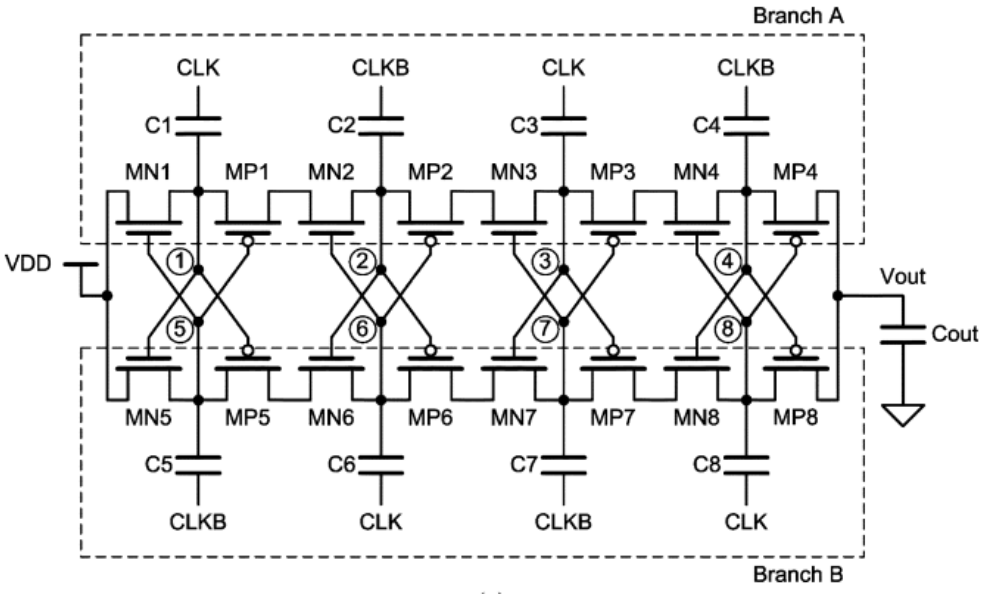

Figure 11: Pelliconi charge pump circuit

Pelliconi charge pump has many advantages. First, its gain is larger than Dickson's one, since no threshold drop is obtained in Pelliconi design. Second, body effect is eliminated by using triple-well NMOS transistors (note that: it consumes more silicon area). Beside that it uses very simple non-overlapping clocking scheme. Finally, it has a completely symmetrical scheme and no specific output stage is needed (as we may need in Wu and Chang design presented before) [8]

3.2.3 Proposed Charge pump

The architecture of the proposed charge pump is based on Pelliconi, one stage Pelliconi charge pump is in Fig. [12], but the PMOS transistors are replaced with diode-connected NMOS transistors, as shown in Fig. [13], due to their low threshold voltage compared to that of the PMOS. The threshold of the NMOS transistors in the UMC 0.13μm CMOS Technology is less than PMOS transistor threshold voltage.

The diode threshold voltage drop will limit the performance of the proposed charge pump.

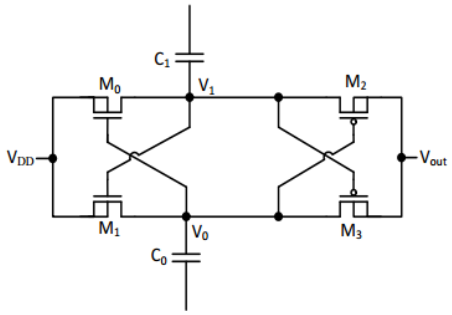

Figure 12: One stage Pelliconi charge pump

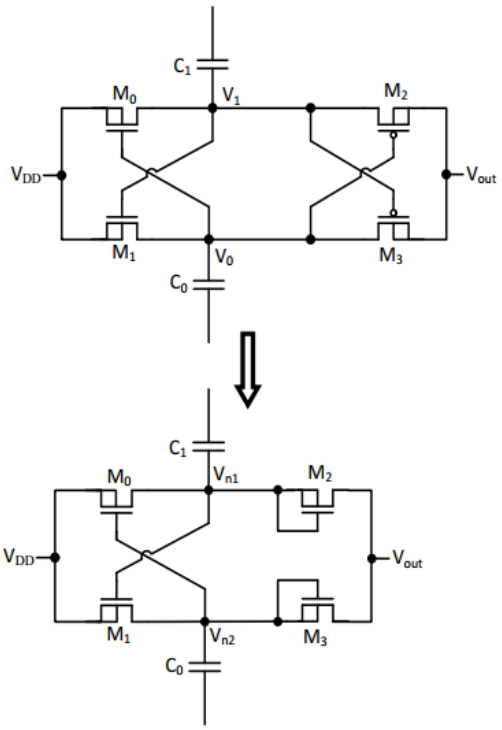

Figure 13: Difference presented from the Pelliconi charge pump

And in order to avoid losing much more silicon area of making such transistors (because the two capacitors in each stage will consume very large area), which will need to be done in a Triple-well Process, Bulk terminals will be connected to ground instead, without affecting the Charge pump behavior as a result of higher threshold voltage due to not using a large number of stages. Which is also good for area due to less number of charging capacitors as shown if Fig. [14].

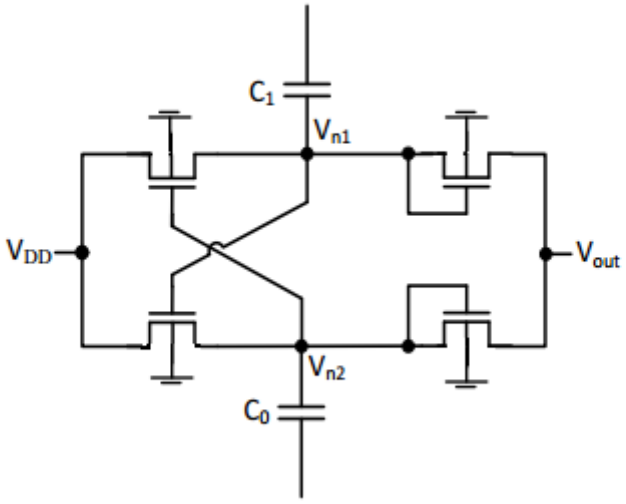

Figure 14: Designed Charge pump

3.2.4 Charge pump parameters

3.2.4.1 Charge Pump Power Efficiency

Charge pump power efficiency is a very important factor in charge pump performance as it defines the ration between the output power and the input power supply from the DC source and the clock sources, of course efficiency can't reach 100% as not all input power delivered to output as charge pump itself consumes some of that power, the efficiency can be expressed as follows

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}}$$

Where:

Pout: is the power delivered to the load

Pin: is the input power from the supply and the clock

Ploss: is the power consumed by the charge pump itself

And simply Pout can be expressed as:

$$P_{out} = I_{out} . V_{out}$$

While Ploss in the charge pump is in two forms:

1) Resistive power consumption Pres

$$P_{res} = I_{out}^2 . R_{out}$$

2) Dynamic power consumption due to charging and discharging capacitors Pdyn

$$P_{dyn} = N. V_{DD}^2 . (C + C_s). f$$

Hence,

$$P_{loss} = I_{out}^2 R_{out} + N. f. V_{DD}^2 . (C + C_s)$$

Where:

N: is the number of charge pump stages

f: is the operating frequency

C: is the charging capacitance

Cs: is the parasitic capacitance

Rout: is output resistance of the pump which depends on the output resistance of one stage which depends on the ON-resistance of the transistor

$$R_{out\ stage} = \frac{1}{(C + Cs). f} + R_{ON}$$

3.2.4.2 Charge Pump Load Line

Charge pump load line shown if Fig. [15] is representing a relationship between Iout and Vout in order to have a constant output power for example (V1*I1 = V2*I2) even if V2>V1 but I2<I1

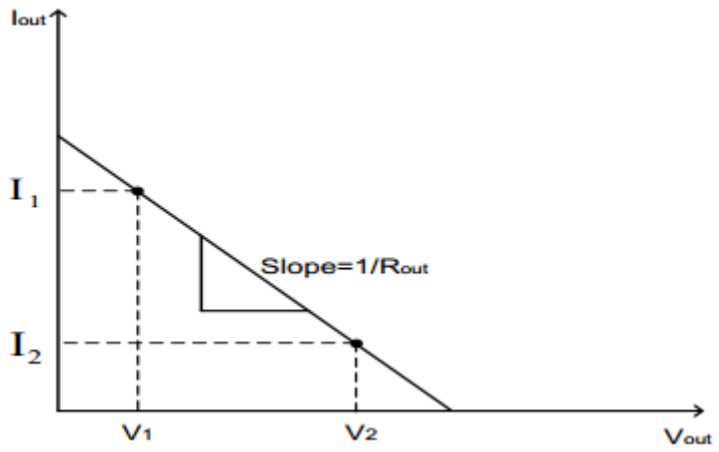

Figure 15: Charge Pump load line

The inverse slope of that curve is indicating Rout of the charge pump

$$Slope = \frac{1}{R_{out}} = \frac{dI_{out}}{dV_{out}}$$

3.2.4.3 Output Voltage Ripple

$$V_R = \frac{I_{out}}{f.C_{load}} = \frac{V_{out}}{R_L.f.C_{load}}$$

The ripple at the output node is due to charging and discharging the output node by the load resistance RL. As noticed increasing the value of the output capacitor or increasing the clock frequency will help to have a small ripple compared to Vout. Where the equivalent circuit may be presented as Fig. [16]

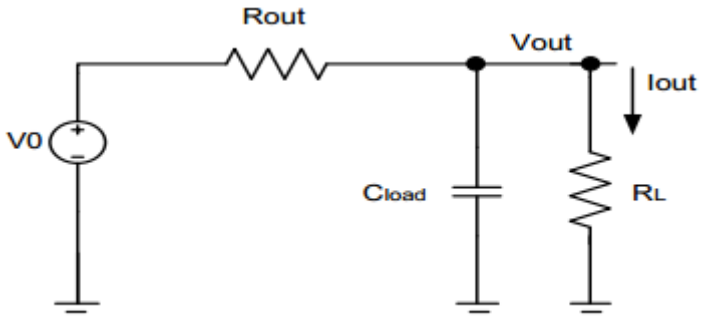

Figure 16: Charge Pump equivalent circuit

3.2.4.3 Layout Area

The area of the charge pump is considered as one of the important parameters in charge pump design. The capacitors consume much area than transistor's size (as mentioned before). So it is required to decrease the charging(boosting) capacitor value to improve the charge pump silicon area. The amount of charge transferred per stage during one clock cycle is proportional to the product (Cboost * Vclk), hence to save area we may reduce (Cboost) and increase Vclk. But generating higher clock amplitude needs extra circuit as an example the circuit shown in Fig. [17], with C1 and C1b area we must do a compromise to choose the best choice in order to have a good charge transfer and not bad silicon area.

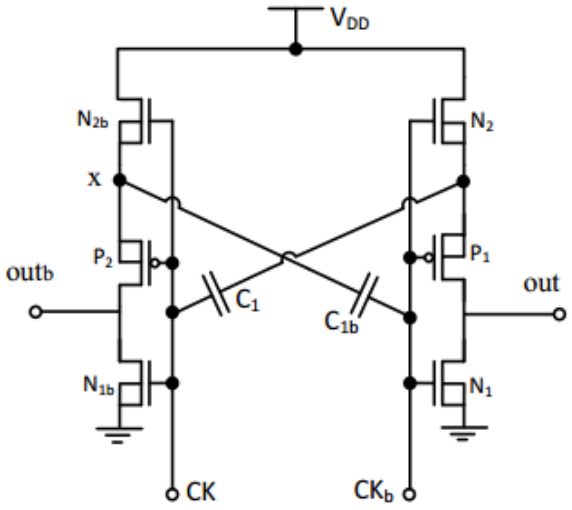

Figure 17: Clock booster circuit

3.2.5 Charge pump controlling circuit

Depending on VCO (voltage controlled oscillator) which changes its output sinusoidal waveform frequency $f(t)$ depending on the following equation.

$$f(t) = f_0 + K_0 * v_{in}(t)$$

Where:

$f(t)$: is the instantaneous frequency of the oscillator at time t (not the waveform amplitude

f_0 : is the quiescent frequency of the oscillator.

K_0 : is called the oscillator sensitivity, or gain. Its units are hertz per volt.

And v_{in} is the Control signal coming from the comparator Vctrl, indicating whether the current is higher or lower than 30uA.

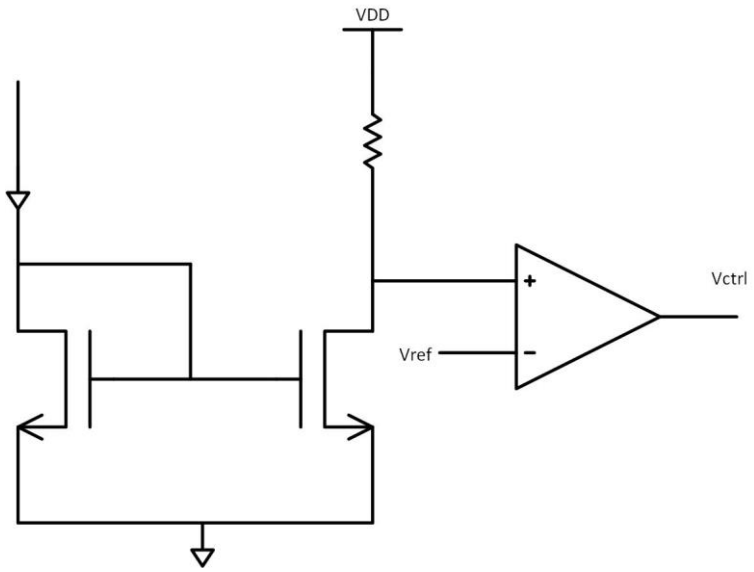

Figure 18: Current Controller circuit

As Known VCO block from "ahdLib" (Cadence Virtuoso Library) output is sinusoidal, so in order to have a square wave (CLK) signal for the Charge pump, a

simple comparator was used here. So, Now the output of that comparator is a square wave signal with the same frequency of the input signal with amplitudes 0 and VDD.

And hence this clock is used to generate two non-overlapped clocks in order to be used with the charge pump.

If Vctrl is high (3.3v as it's the output of the comparator) hence we've a high frequency mode for the VCO.

charge pump circuit starts to pump to high VCC voltage, if the Control signal is high. Hence the charge pump circuit is at the high frequency stat, which makes it keeps pumping to higher voltage. Then, the output voltage of high voltage generator increases, and voltage is delivered from the charge pump. The charge pump circuit keeps pumping until the current stimulating becomes higher than 30uA then V+ is lower than V- With a very simple idea using the current controller as follows. When the current Istim is less than 30uA the comparator input V+ which equals VDD - (Istim * R) becomes higher than V-, hence the comparator output becomes high, hence charge pump pumps more voltage. And When the current Istim is higher than 30uA the comparator input V+ which equals VDD - (Istim * R) becomes lower than V-, hence the comparator output becomes low, hence charge pump pumps less voltage.
That is to say, the Control signal becomes low. Hence, charge pump circuit is working at the low frequency state causes that output voltage of high voltage generator and the stimulated current to decrease. Until the current stimulating becomes lower than 30uA then V+ is higher than V- in the Current Controller.

Here we see one but very important advantage of the output capacitor which is 15 pF, to reduce ripples in the output of the high voltage generator circuit.

3.3 Output driver and pre-driver

3.3.1 Idea

Output driver is the last stage of the stimulator, actually it's the most important part in it. As the output driver is the communicating module with the outer environment, which mainly it's the electrode. Output driver mission is to steadily give the stimulus current or voltage or in some new cases charge (as we mentioned in the survey in Chapter 2).

In the closed loop adaptable designs such as this one, high voltage generators or charge pumps are mostly used, which puts more limitations on the design of the output driver to be able to sustain such a high output voltage without any hazards on the output devices inside the output driver. Not just hazards are to be put into our considerations designing the output driver, but also devices lifetime has become a very important issue on a general consideration and on a specific one, as this simulator is expected to be planted inside a brain on someone using a not easy surgery. So, output driver devices lifetime has to be carefully studied. In Fig. [19] graphs indicating life time of the MOS transistor is illustrated regarding the voltage drop on the transistor and the applied gate voltages.

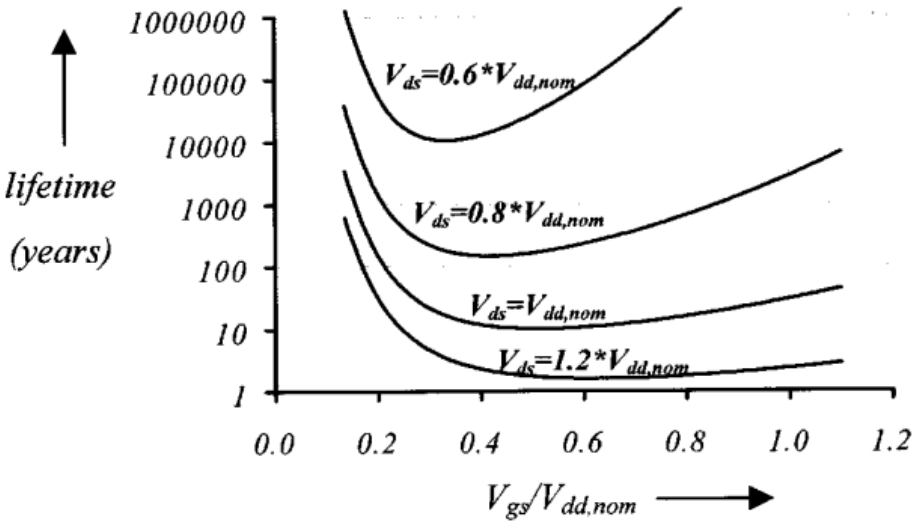

Figure 19: lifetime of the transistor vs. applied voltage [11]

Where, Vdd,nom on the graph is indicating the nominal voltage of the CMOS technology which is here 3.3v.

So, and as a roughly estimated values if we want the circuit to live nearly 100 years (as a good value comparing to man's life and new technologies), Vds across every transistor must be smaller than Vdd (better to be smaller than 0.9Vdd)

3.3.2 Different Architectures

Output drivers may take many forms. Not just with the type of stimulation which was clarified in Chapter 2. But also every type of them may have a variety of architectures and ideas, each one has its advantages and disadvantages. Starting with the first idea in Fig. [20].

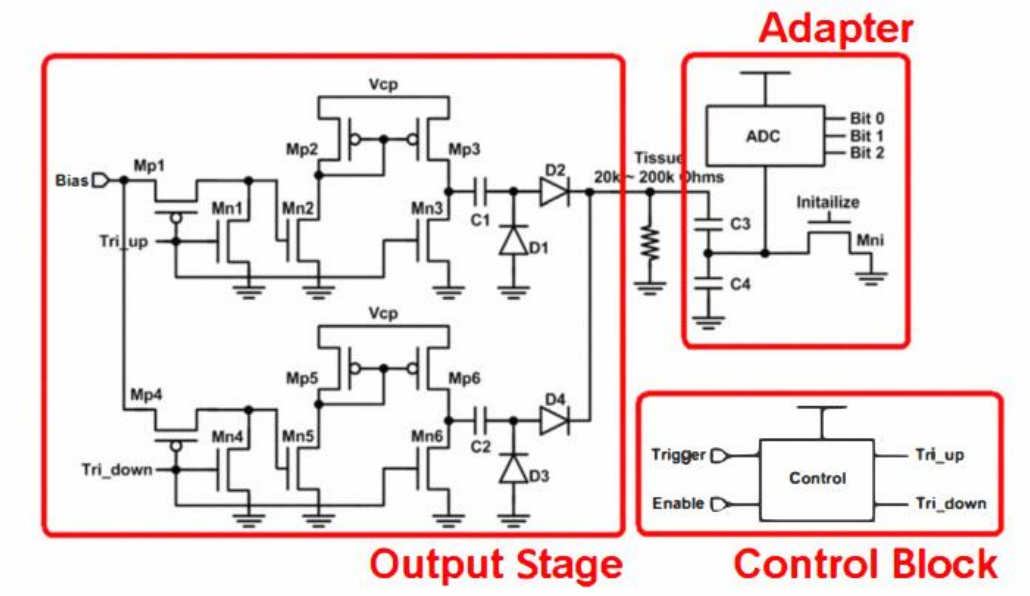

Figure 20: Output driver example 1 [12]

Second idea in Fig. [21].

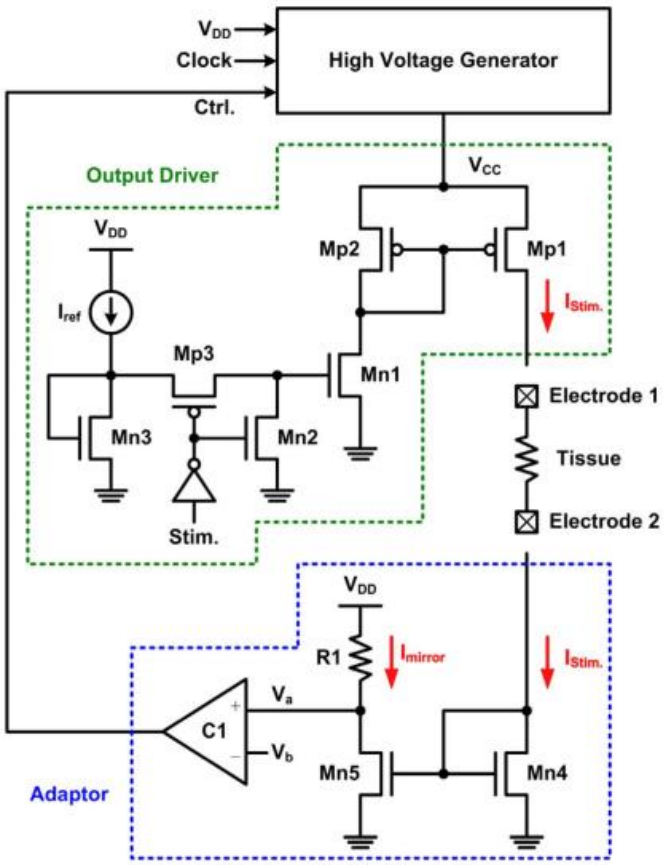

Figure 21: Output driver example 2 [13]

But There is a very important Problem with such circuits, is that it need high voltage devices to sustain such a high output voltage of the charge pump. Which enlarges power consumption and is more expensive. Hence an idea that enables us to use low voltage CMOS devices in order to skip those problems mentioned above, becomes a must.

This idea must make the driver function completely right with the ability of handling high voltages, while ensuring sufficient lifetime, in a CMOS generation with a significantly lower nominal supply voltage. [11]

One example of an idea is about technological solutions which can be presented is multiple gate oxides [11] - [14] - [15] which yield high-voltage-tolerant transistors. But on the other hand, the cost of a more expensive process, masks and processing steps must be added to the baseline process.

But the idea on which this design is based on, is using only ordinary transistors with nominal voltage equals 3.3v. But hence one of the innovative circuit solutions must be used to achieve high-voltage tolerance [16] - [17]. With this type of high voltage tolerance, the voltages across all transistors' terminals are limited to sufficiently low values to ensure sufficient lifetime as shown before.

This circuit which will have the mission of making the output driver able to deliver the wanted current with the ability to sustain the high voltage output form the high voltage generator by controlling the gate voltages is called **pre-driver**

3.3.3 Problems which may be faced without the innovative circuit

Two electric field strengths appear to be the most dominant for the lifetime of MOS transistors. The vertical and lateral electric field in the (intrinsic) transistor. The two lifetime-determining mechanisms corresponding to these fields are denoted as oxide breakdown and hot-carrier degradation.

A. Oxide Breakdown

   Oxide degradation is the process of slow degradation happens to the oxide as a results to currents flowing through this oxide in response to an electric field across the oxide. Which makes oxide breaks down, i.e., is destroyed, if a certain amount of charge-per-area passed through the oxide. The oxide current, and following it the transistor's lifetime, are strong functions of the applied electric field across the oxide. It was found that oxide lifetime is sufficient if this electric field is limited to a value typically corresponds to a tolerable oxide voltage 20% higher than the process's nominal supply voltage.[18]

B. Hot-Carrier Degradation

With large drain–source voltages and transistors operating in saturation, carriers flowing from source to drain may gain high energies, i.e., become hot, close to the drain region. Upon collisions with the silicon lattice, a small fraction of these hot carriers shoot into the gate oxide near the drain area, thereby slowly degrading the gate oxide and the transistor's performance [19], [20].

3.3.4 Proposed Design

Is based on the H-Bridge topology. The H-bridge is a configuration of four switches that offers the possibility to reverse the stimulation current direction using the same current source. [31]

In order to benefit from the highest possible dynamic range, the switches on-resistance must be minimized.

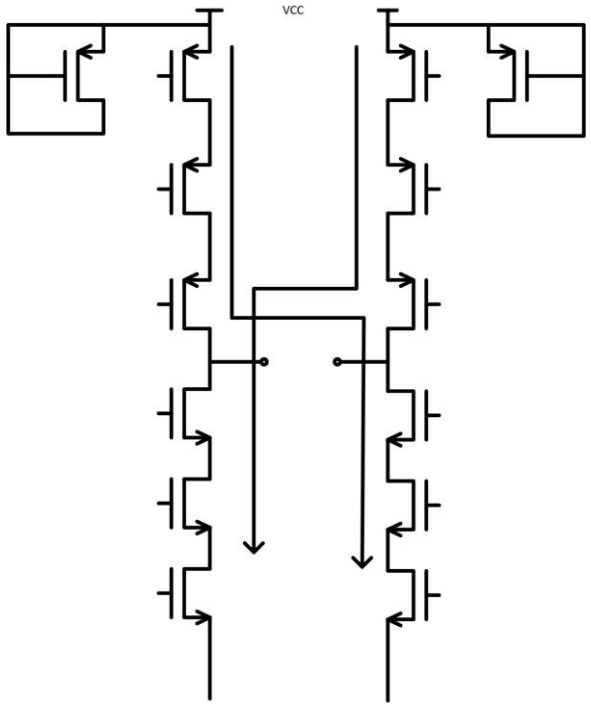

Figure 22: Presented the output driver two phases Anodic and Cathodic

As shown in Fig. [22] the H-Bridge topology idea is dealing with one PMOS block and one NMOS block, with the ability of working on two phases Anodic current stimulation phase and Cathodic current stimulation phase. Between the two output pins Electrode is placed, so this output driver enables using Bipolar electrode. as illustrated in Chapter 2 the difference between bipolar and unipolar electrodes.

3.3.4.1 Steps of designing

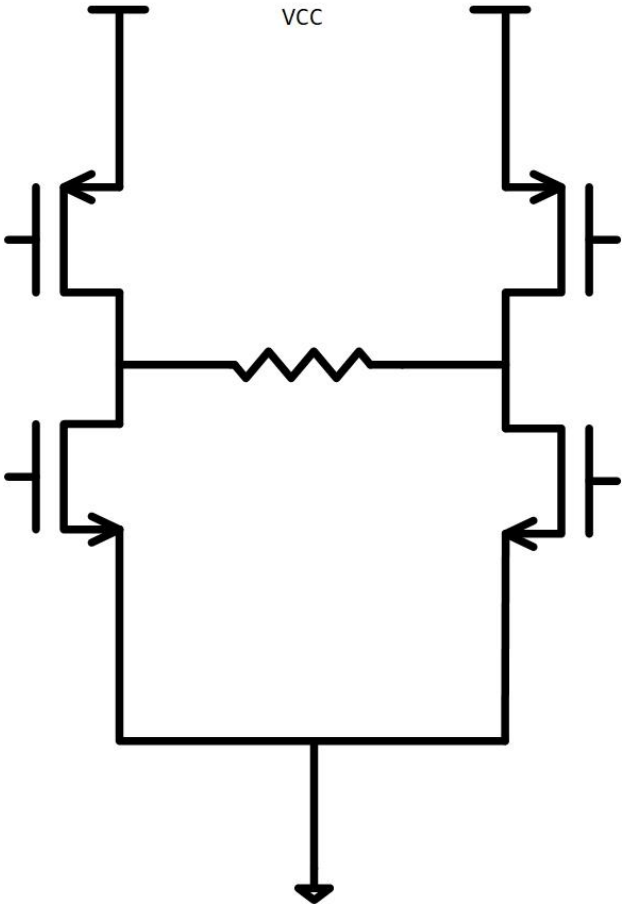

Figure 23: step1 of designing the output driver

As shown in Fig. [23], designing was started by trying a one transistor in every branch in order to verify the concept of working. With dc gate voltages, which will take a totally different part in the coming sections, in order to compare between the two ideas of the digitized output driver and the use of pre-driver.

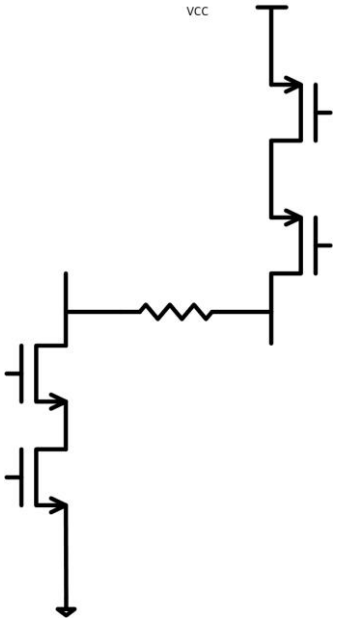

Figure 24: Step2 of designing the output driver

As shown if Fig. [24] and Fig. [25] steps of designing was to reach optimum number of stacked transistors in order to sustain the high voltage output from the charge pump or the high voltage generator.

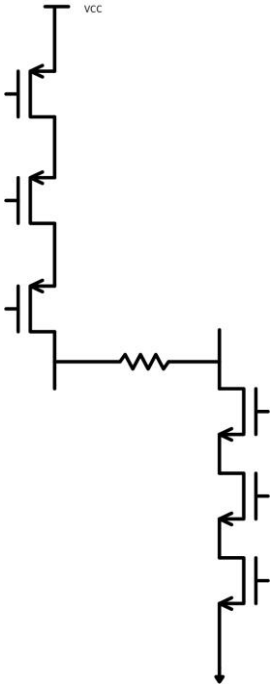

Figure 25: Step3 of designing the output driver

Three stacked MOS are shown a good response in order to avoid reliability problems which decreases the lifetime of the transistor mentioned before, which are Oxide Breakdown, Junction Breakdown and Hot-Carrier Degradation.

Final testing model (before pre-driver circuit was developed) is shown in Fig. [26]

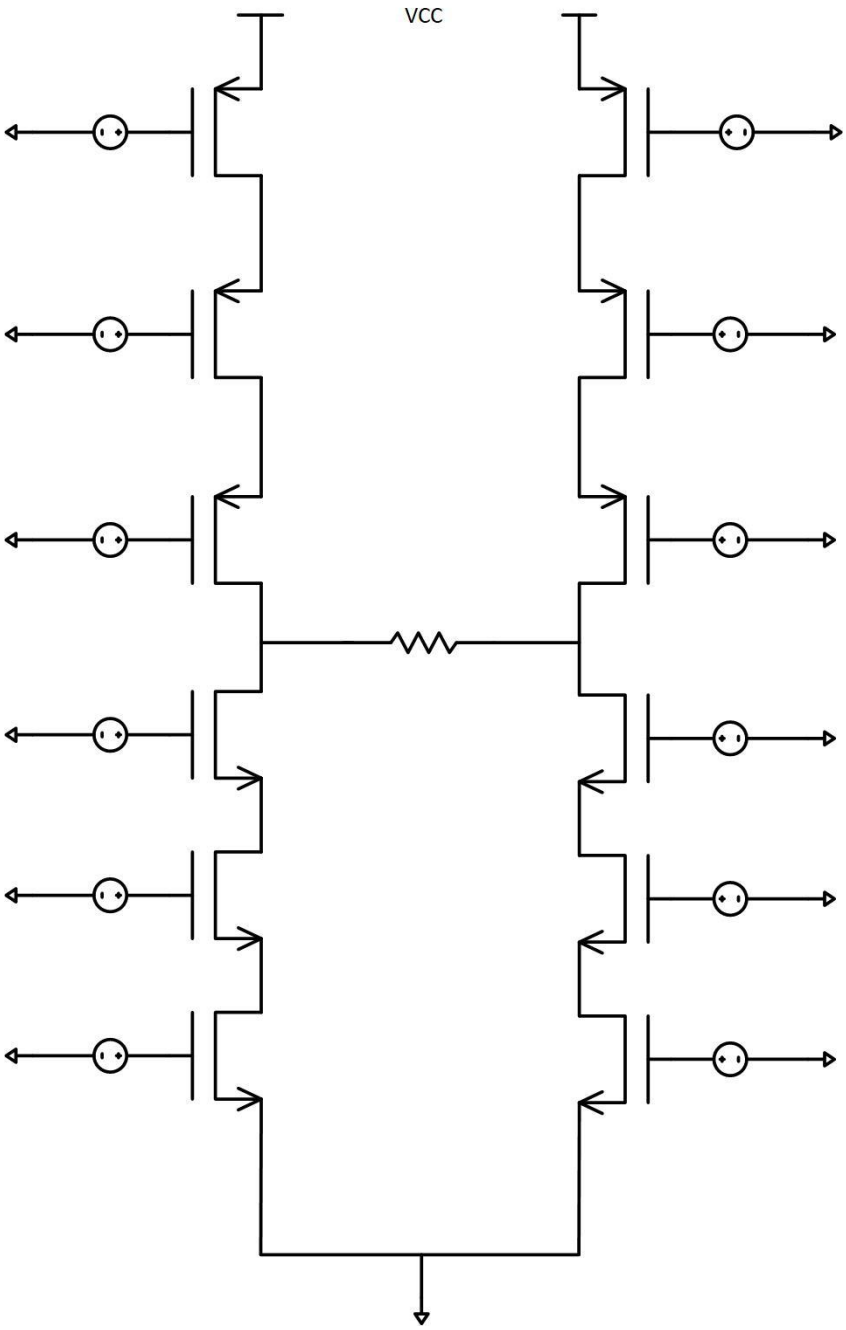

Figure 26: final design before pre-driver

3.3.5 Pre-driver

The proposed design strategy is to employ the stacked transistors to withstand the higher voltage generator output voltage. An example of two stacked transistors is shown in Fig. [27], where the source of the first transistor is connected to the drain of the second transistor.
By this way, the voltage across from the drain of the upper device to the source of the lower device can rise up to two times of the nominal supply (nVDD).
In this topology, the gate bias of the transistors and should be carefully set, and the maximum voltage across the terminals of all transistors should be limited by the nominal supply voltage.
If n transistors are stacked, it can withstand n times the nominal supply voltage without decreasing the transistors reliability [11]

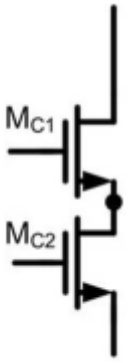

Figure 27: Two stacked NMOS transistors

Here, Using Triple well technology was avoided due to the bigger layout silicon area and the complexity of the layout itself.

Triple well technology is used mainly in order to raise the breakdown voltage of the parasitic well diode, as for the triple-well technologies the breakdown voltages of NMOS transistor with deep n-well layer, NMOS transistor without deep n-well layer, and PMOS transistor are limited by the n-well/p-substrate diode, n + /p -well diode, and n-well/p-substrate diode, respectively. The prior work reported that the

breakdown voltage of the n-well/p-substrate diode is higher than that of the n + /p - well diode [21]

3.3.6 Pre-driver two stages

3.3.6.1 Stage 1: nth VDD generator

As shown in Fig. [28]

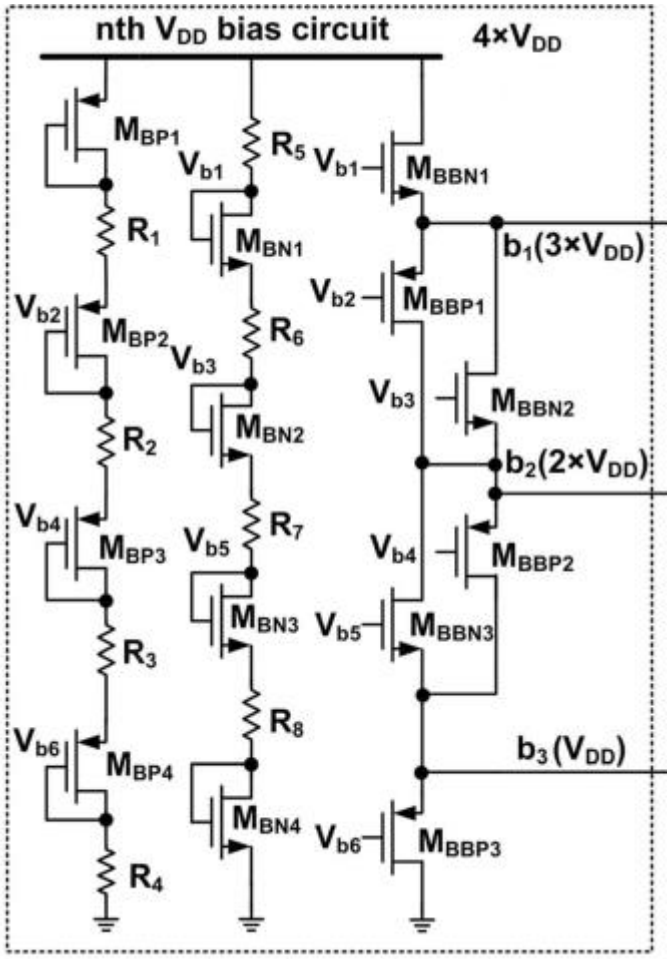

Figure 28: Pre-driver circuit first stage

This circuit mission is to do a voltage dividing between the three output branches b1, b2 and b3. In order to work as a biasing circuit for the second stage of the pre-driver circuit and the first and the last two transistors in the MOS stacked transistors. [22]

Where the first two columns work to get the gate voltages of the outer three stages in order to bias them correctly in the saturation region, which will reflect on their behavior as will be shown.

For the first pair MBBN1 and MBBP1 with the function of the push-pull output stage which has low power dissipation in the standby condition, the NMOS lower the drain source with Vdsat which is nearly VDD, that makes the output b1 is 3VDD and with the same idea b1 is considered as an input to the second pair MBBN2 and MBBP2 hence we get b2 which is 2VDD and use it again with the third pair MBBN3 and MBBP3 to get b1 equals VDD

In Fig. [29] an example of the nth bias circuit with 4*VDD = 12v, hence we can see outputs b1 to b3 with b1= 9v, b2= 6v and b3=3v

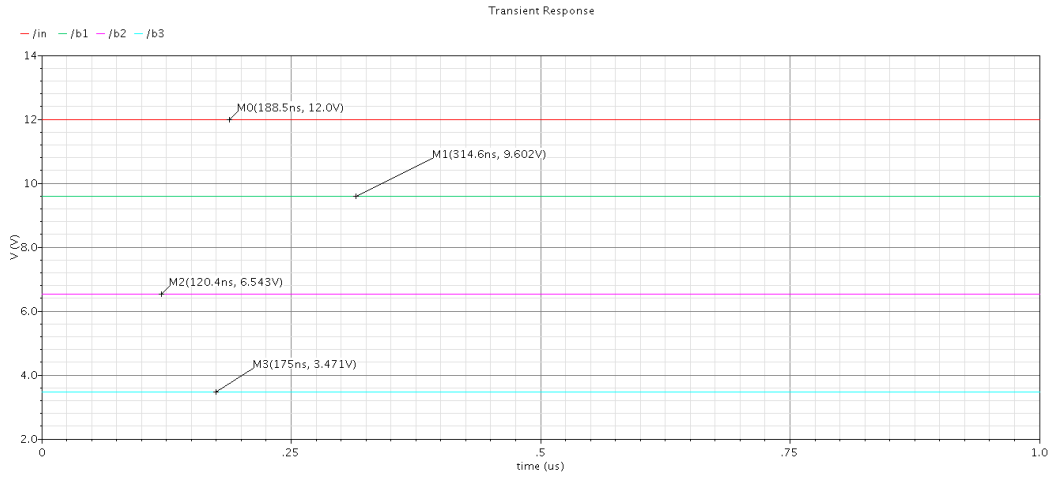

Figure 29: Pre-driver first stage test

3.3.6.2 Stage 2: The pre-driver output stage (Self-adaptation bias circuit)

As shown in Fig. [30]

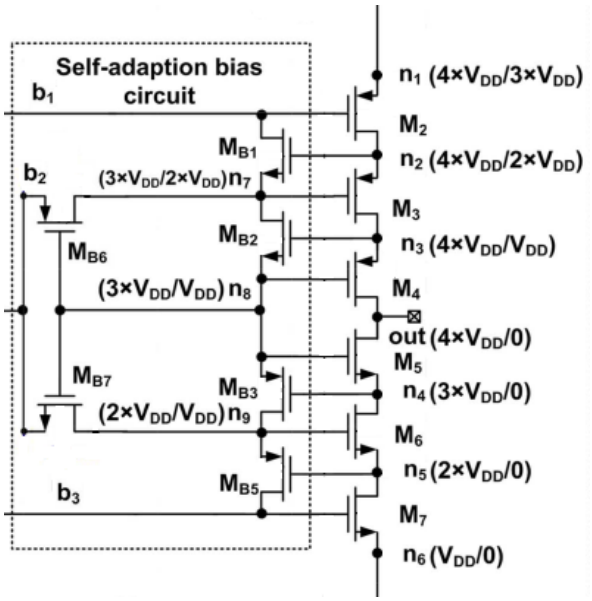

Figure 30: pre-driver output stage

Idea of the previous circuit is very simple.

Assuming working in the Anodic phase hence, the upper PMOS block is working and the lower NMOS block is not, which means that the upper three stacked transistors are on and operating in the triode region as a resistance, in order to tolerate with the changeable current floating among them. While the lower three stacked transistors are in the off region.

For the higher PMOS block and starting from M2 and because b1 is 3VDD, so in order to have M2 in triode, M2 drain is higher than 3VDD+Vth which is very close to 4VDD. And hence for MB1 it will be forced to enter the triode region as Vgd < Vth, which will make the voltage of the node b1 moving to node n7 and hence the same thing is repeated between M3 and MB2. Then n8 is also 3VDD when MB2 pass the voltage of n7, and again the same idea happens with M4.

Checking that MB6 is off at this stage is positive as Vsg = 2VDD – 3VDD which is < that |Vthp|

For the lower NMOS block starting from the previous conditions and for MB7 Vgs>vth and it's design to work in the triode region, hence n9 is equal to b2 equals 2VDD. And for transistors M5, M6 and M7 in order to be off we expect Vgs to be less than Vth, which will force those points n4, n5 and n6 to take those values

Checking that MB3 and MB5 are off too, can be easily done when its Vsg found to be less that |Vthp| as illustrated.

For the Cathodic phase the same thing happens but with the flipped circuit, because the design is symmetrical as shown in the overview on design I section.

3.4 Results

3.4.1 Simulation results

3.4.1.1 Charge pump

Charge pump presented was a three stages charge pump based on Pelliconi design with some changes as mentioned before with its control circuit which received the Vctrl from the Current Controller.

1- Ideal charge pump at the higher frequency (Iout = 0)

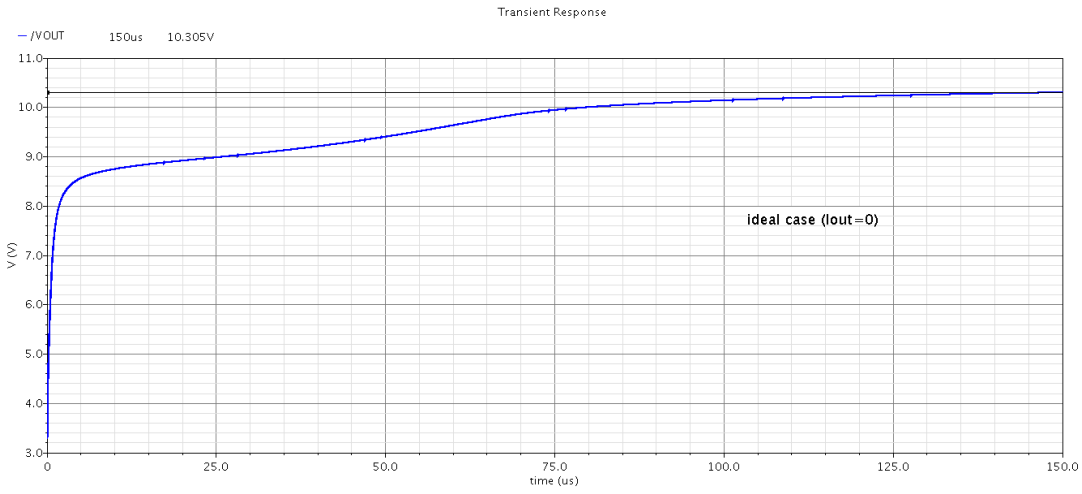

Figure 31: Charge pump ideal output at f1

2- Ideal charge pump at the lower frequency (Iout = 0)

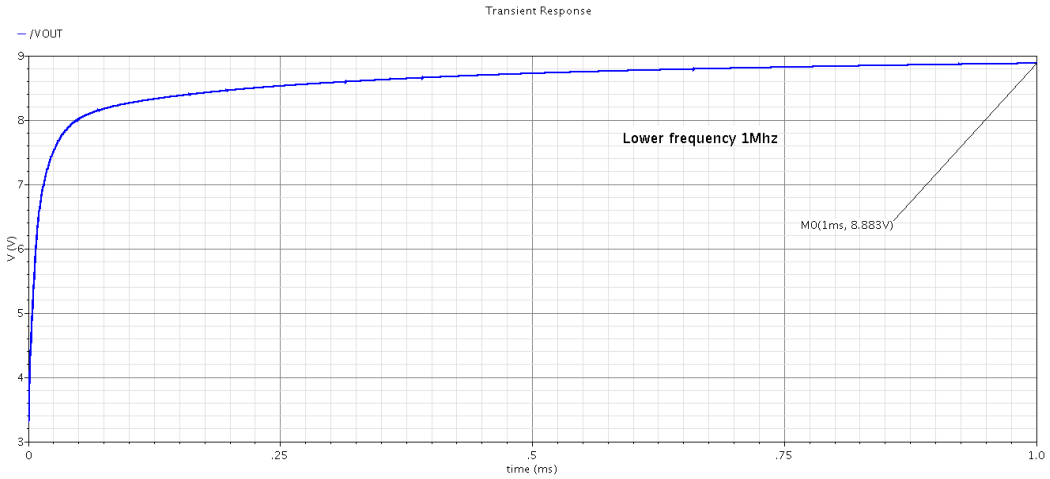

Figure 32: Charge pump ideal output at f2

3- Charge pump output variation with (Iout doesn't equal zero)

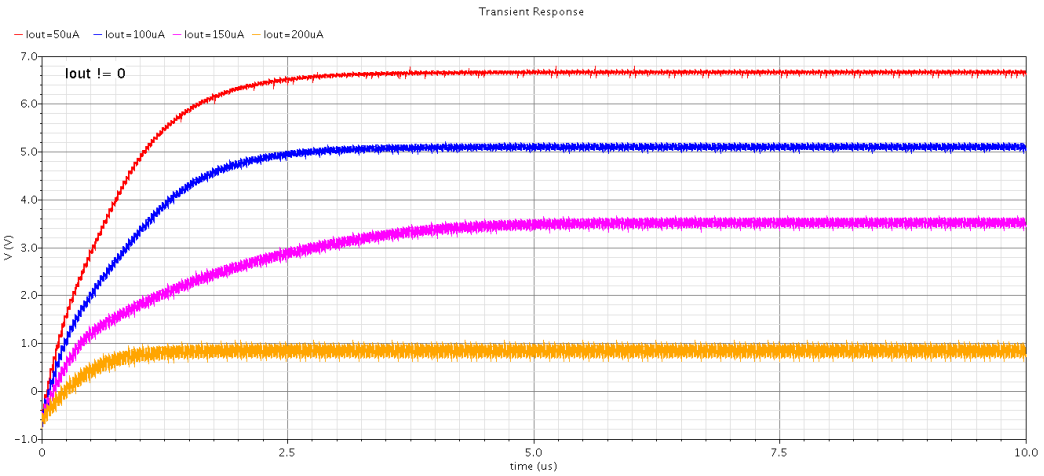

Figure 33: Charge pump Vout with Iout change

4- Charge pump efficiency with change of load impedance

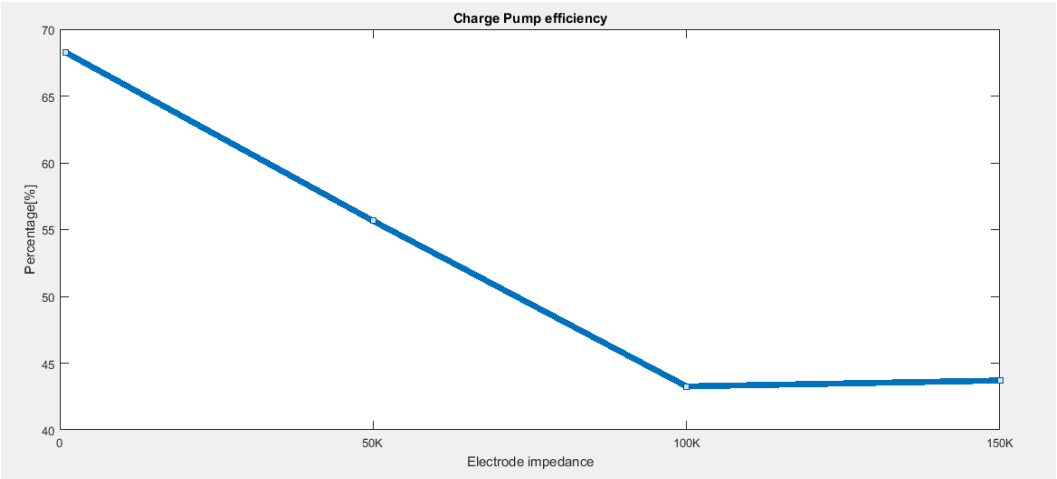

Figure 34: Charge pump efficiency

5- Comparator output with 4 different values of electrode impedance as follow

From 0 to 5u R= 1k

From 5u to 10u R= 50k

From 10u to 15u R= 100k

From 15u to 20u R= 150k

We can notice from the previous figure the change in the frequency of the high output and the low output which the two non-overlapping clocks follows.

3.4.1.2 Output Stage

Output Stage is consisting from two main parts:

A. Pre-driver

B. High voltage output driver

1- Output current with change in electrode impedance.

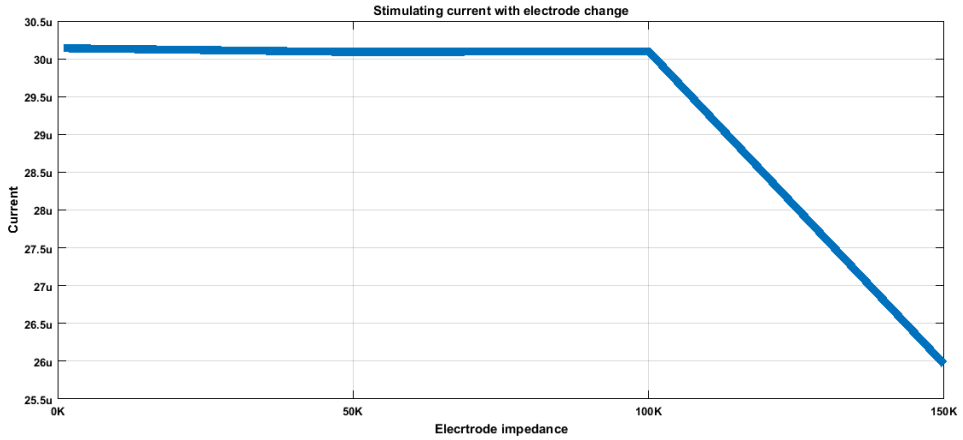

Figure 35: Output current with change in electrode impedance

Note that: change happens after 100k is not so sharp as it may appear to be, but it's very slight change in current after 100k, the wanted idea from that curve to illustrate the allowed of working region of the impedance.

2- Checking that in the high voltage output driver that no Vds has exceeded the nominal voltage of the technology which is 3.3v

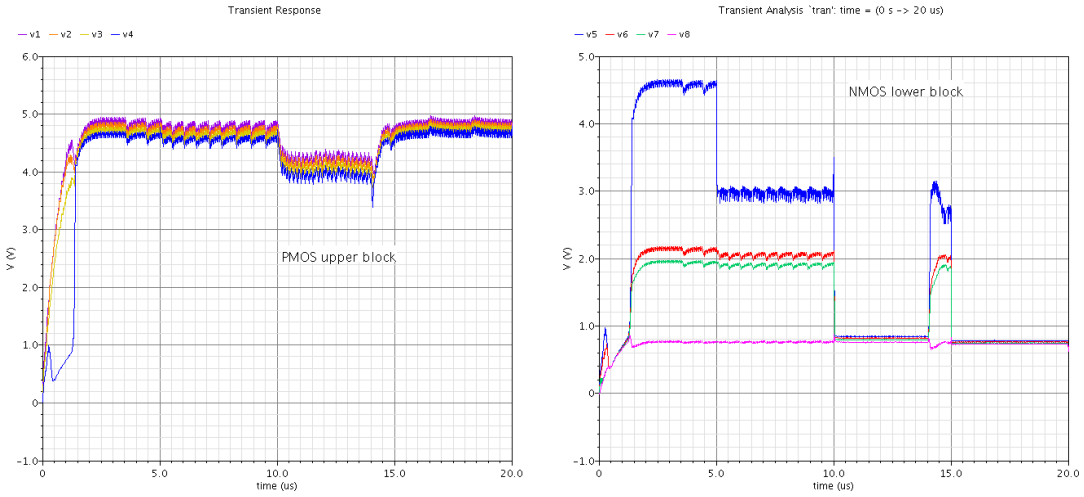

Figure 36: Vds across transistor check

It's clear form the figure that there is no drop voltage across any transistor has exceeded the nominal supply voltage. Where (v2 - v1) is the voltage drop across first one and so on.

3- Power consumption with change in electrode impedance.

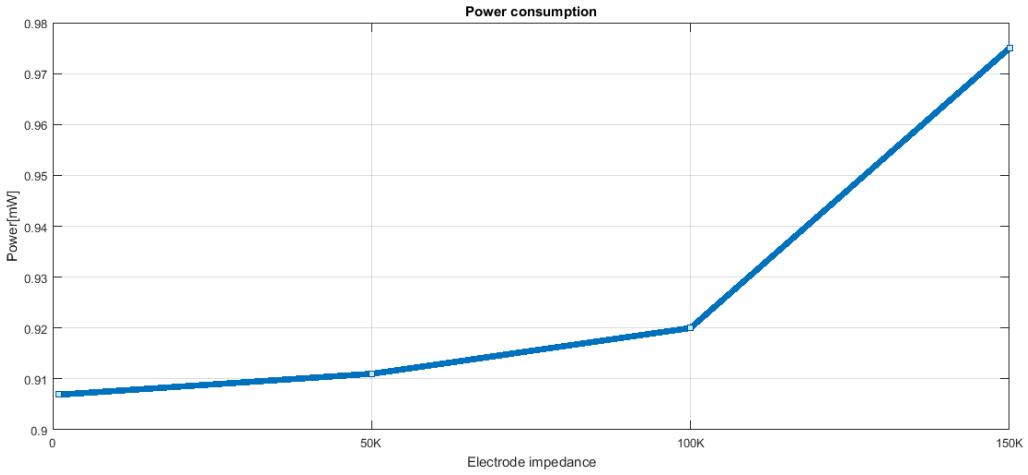

Figure 37: Power consumption

As clear power increases with higher electrodes, as the charge pump operates with f2 the higher frequency more time than the lower one.

4- Total Anodic Cathodic current

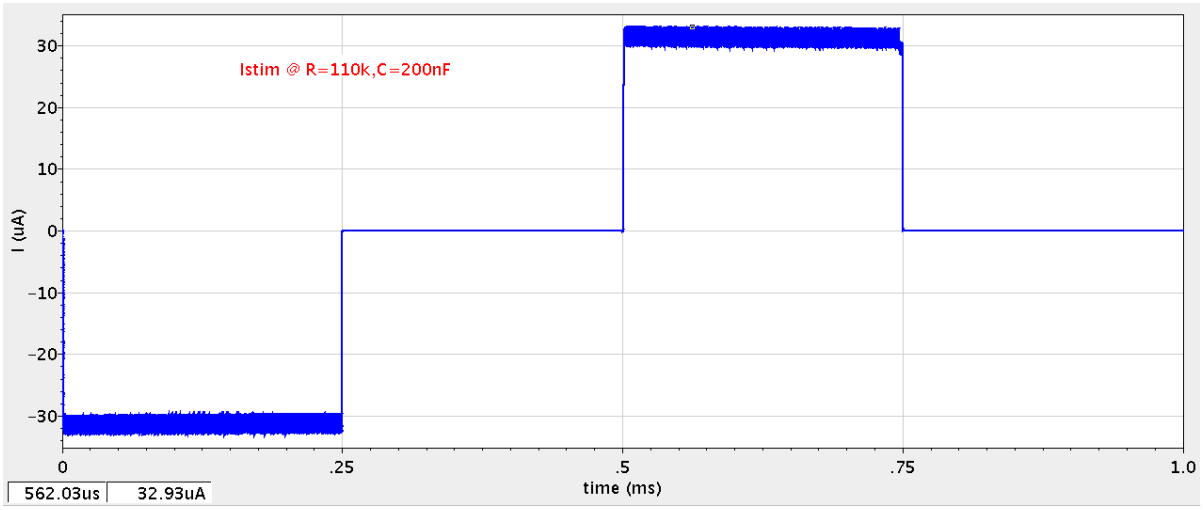

Figure 38: Anodic Cathodic current

3.4.2 Process VDD Temperature (PVT or corners)

1- VDD change with TT, FF, SS, SF and FS

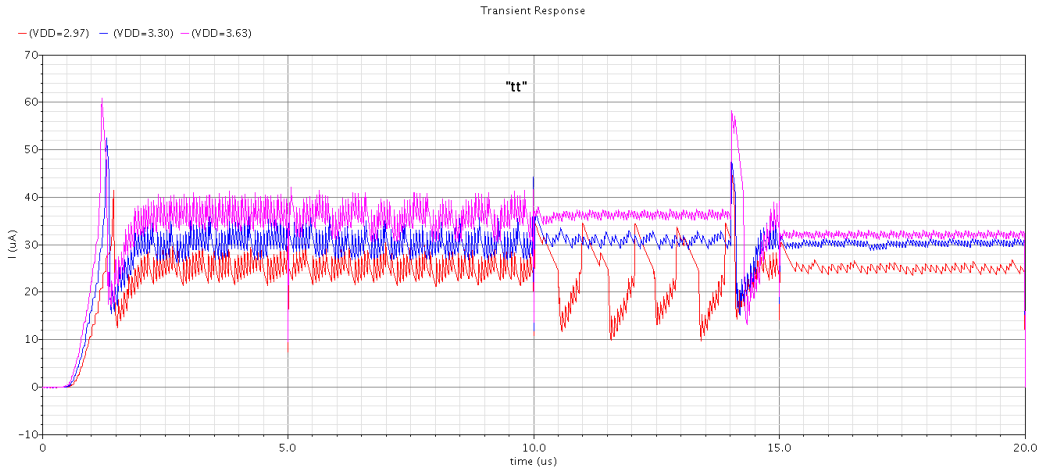

Figure 39: typical NMOS typical PMOS

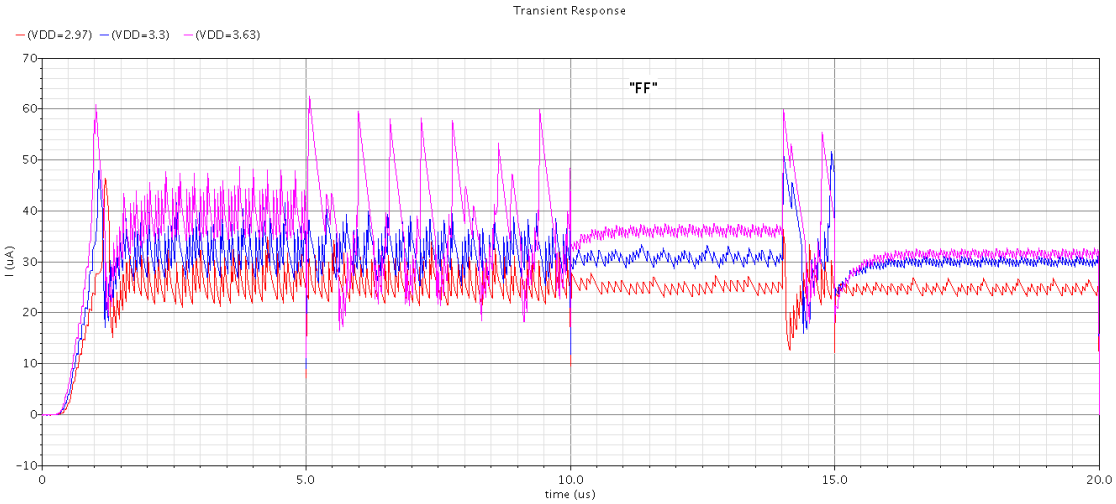

Figure 40: fast NMOS fast PMOS

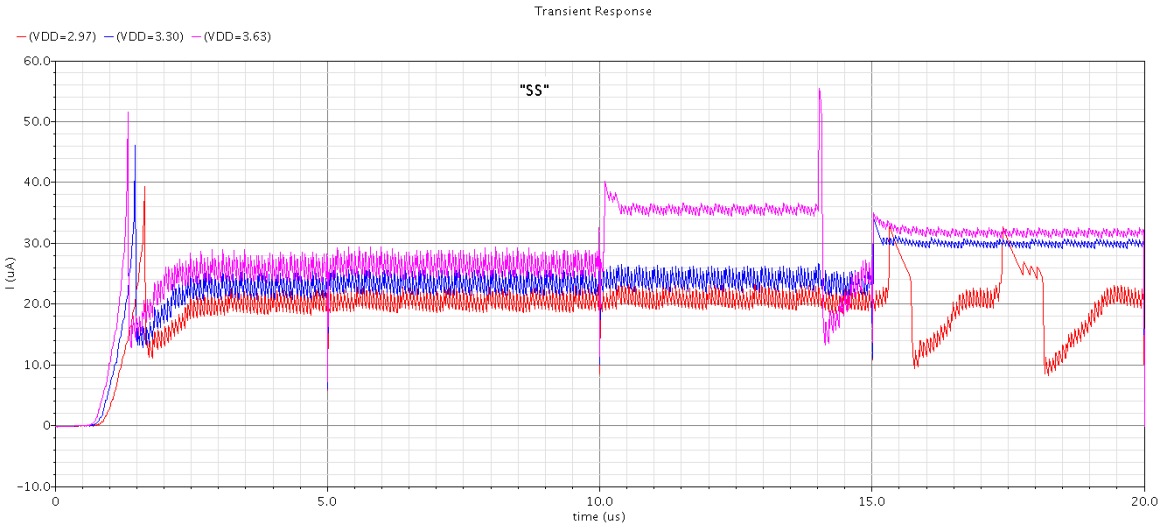

Figure 41: slow NMOS slow PMOS

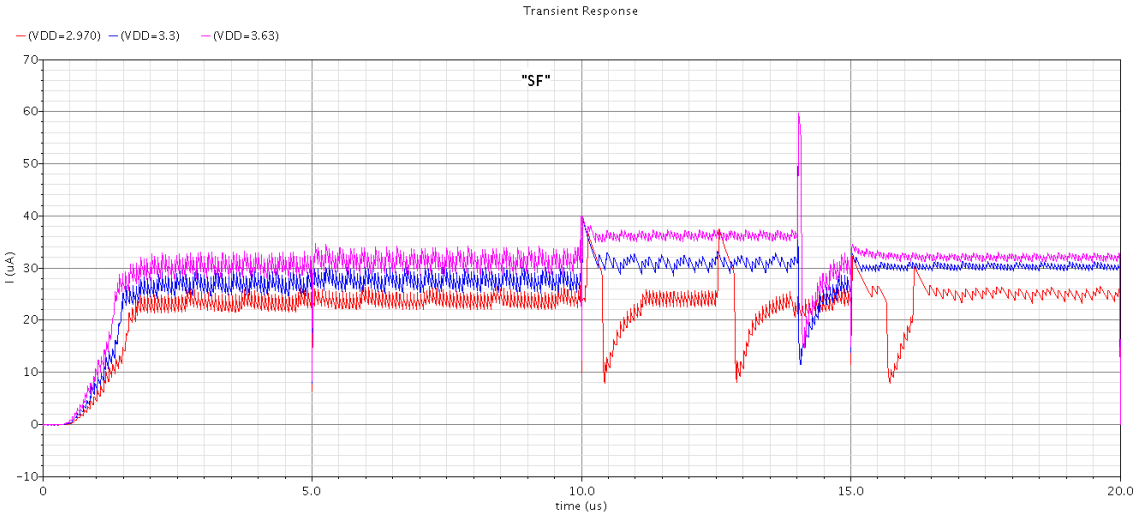

Figure 42: slow NMOS fast PMOS

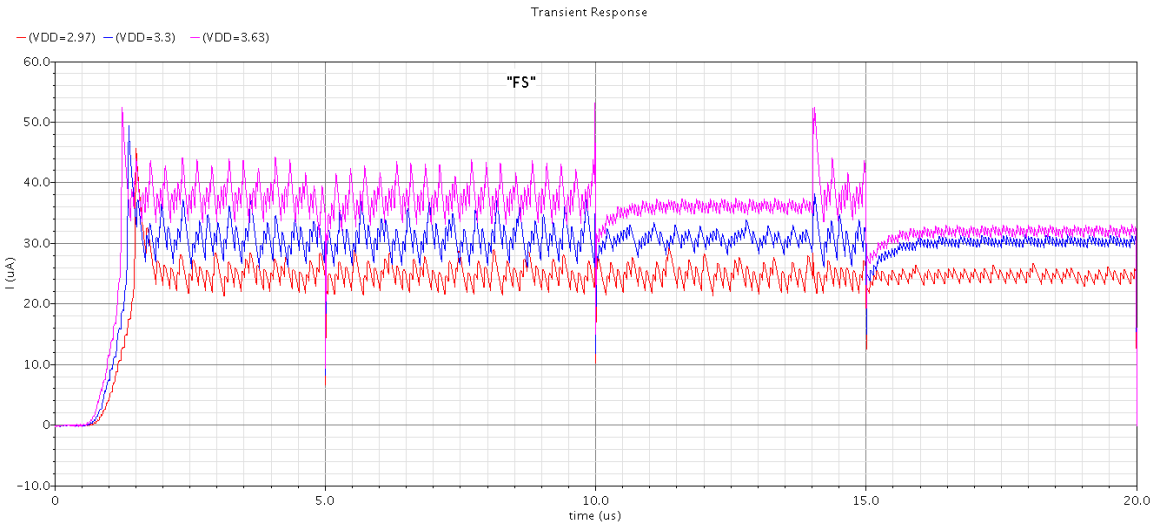

Figure 43: fast NMOS slow PMOS

2- Temperature change (from -40’c to 85’c)

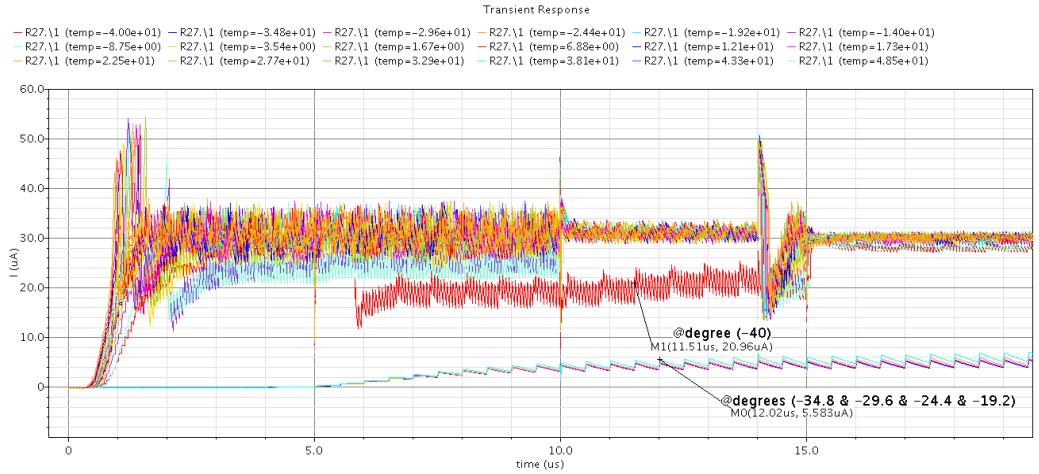

Figure 44: Most accurate temperature variations

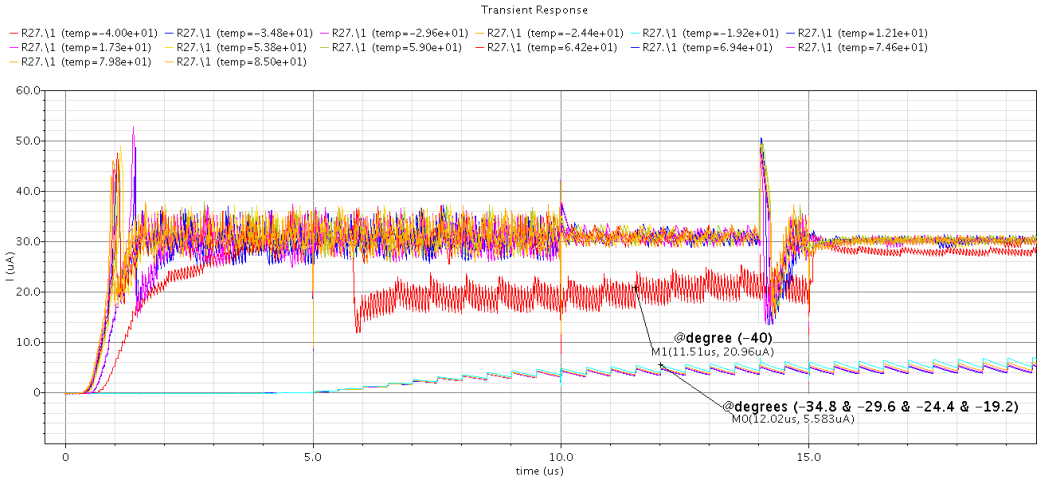

Figure 45: less accurate temperature variations

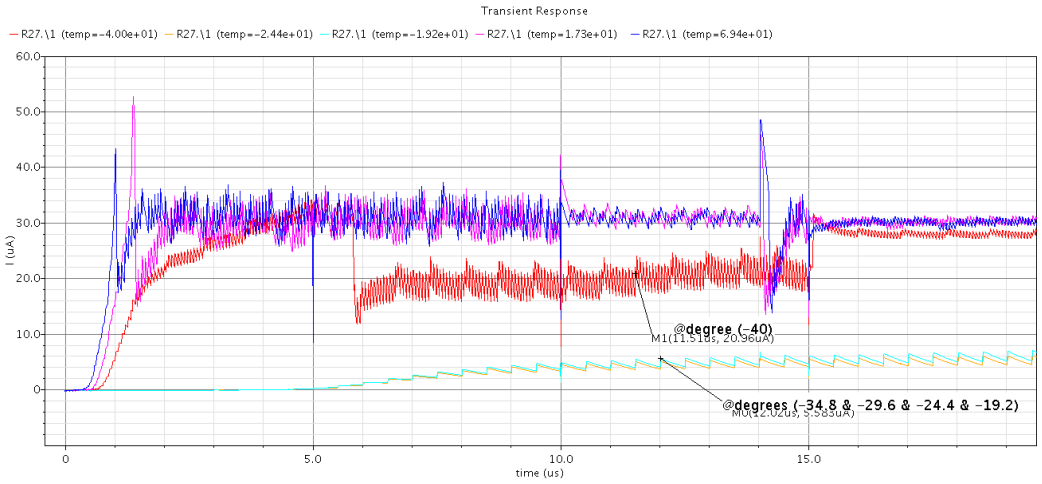

Figure 46: Least accurate temperature variations

3.4.3 Layout

1- Total Area

Total area of the stimulator is **278um X 273um** (output capacitor may be done off chip as it takes a huge area compared to other blocks as will be shown)

2- Common centroid technique with the same boundaries

- Current mirror in the current controller shown before.

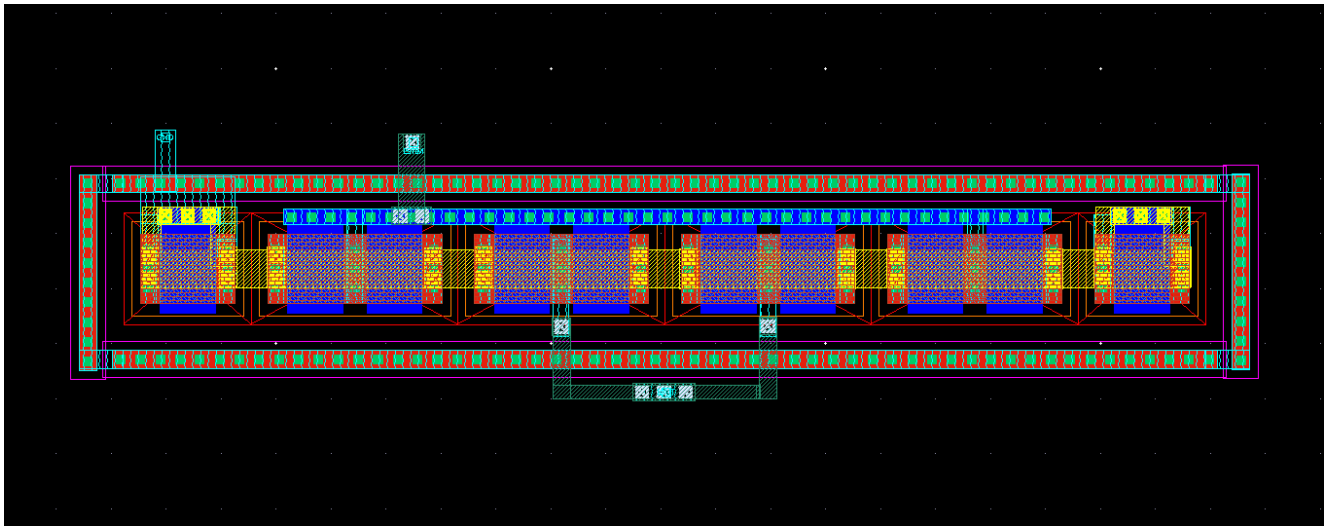

Figure 47: Current Controller layout

As seen in the layout every transistor is divided into two multipliers and two fingers for less parasitics and to be able to apply the common centroid technique as follow from left to right **DUMMY M1 M2 M2 M1 DUMMY** and the outer via (M1 to P-substrate) is for better isolation for NMOS devices.

- First two paired transistors in the stacked output driver

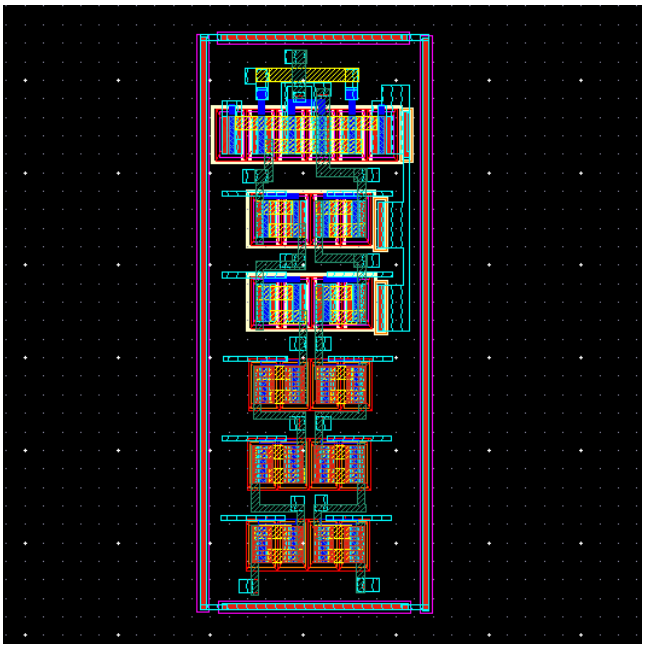

Figure 48: Total layout of the high voltage output driver

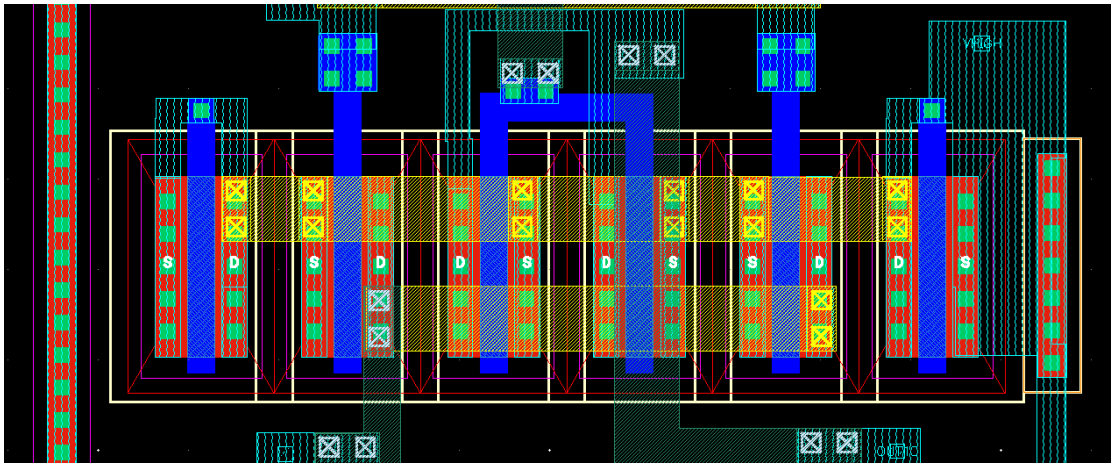

Figure 49: output driver first two stacked transistors

As seen Common Centroid is applied here two with the same boundaries using dummies.

3- Total circuit

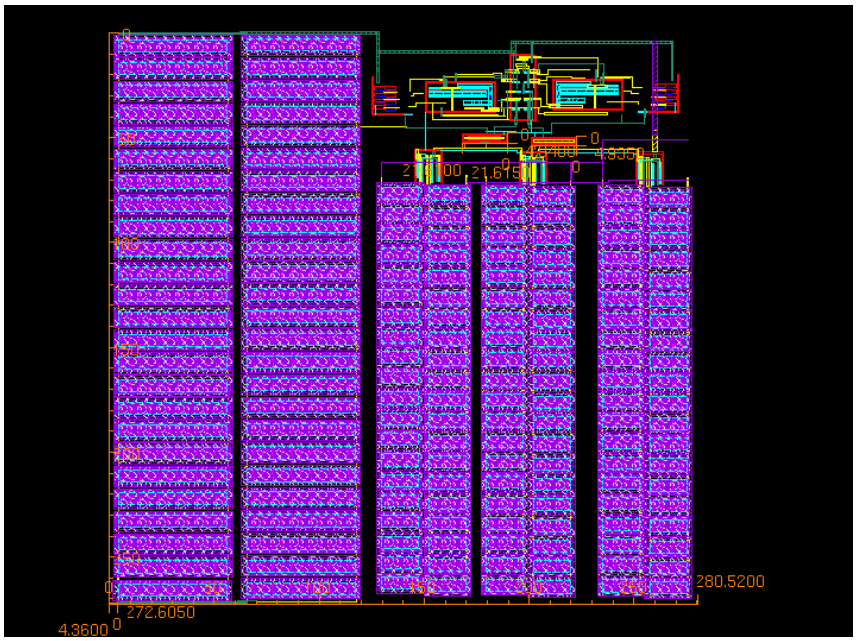

Figure 50: Total circuit layout

4- Circuit Floor plan

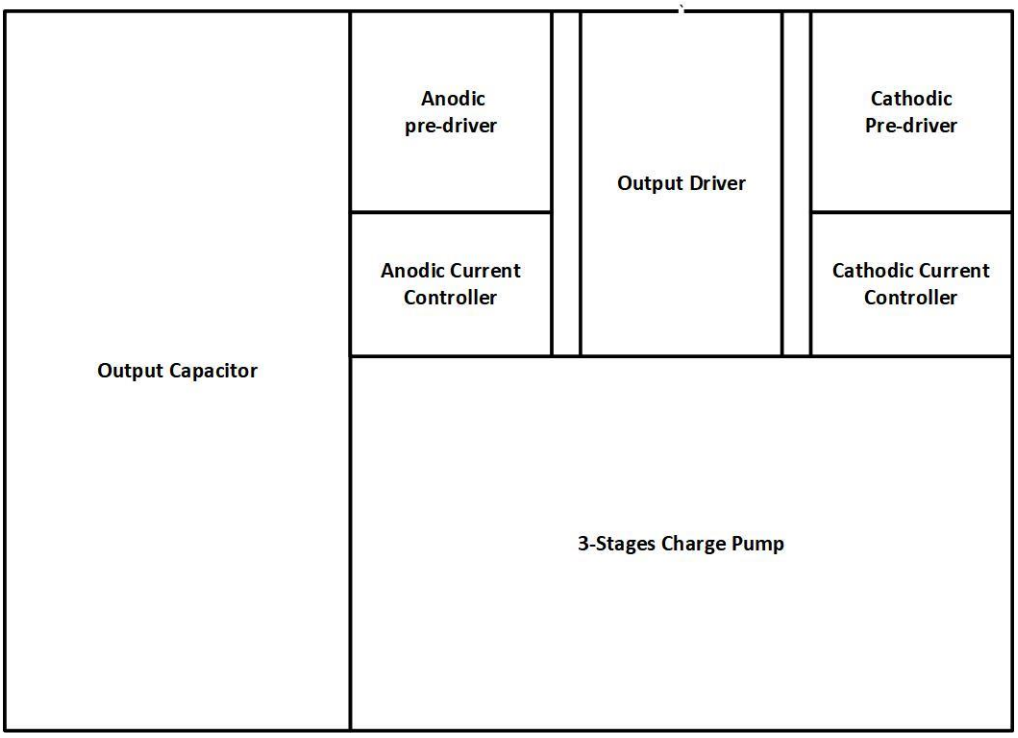

Figure 51: Floor plan of the proposed design I

3.4.4 Post Layout simulation

1- Output current

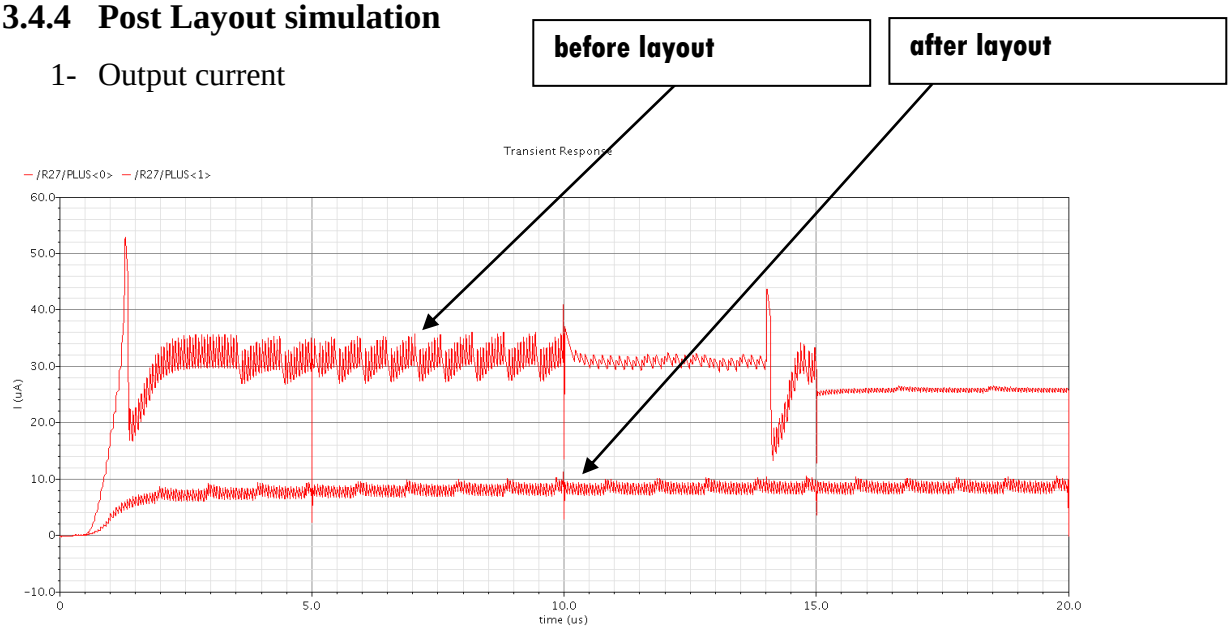

Figure 52: Output current post layout

As seen it's constant but the amplitude is smaller than previous, with more frequency it goes higher. But it's not a permanent solution, as with higher frequency the power will go higher so another layout technique (such as seeing the parasitics on the circuit, trying every parasitic alone R, C or CC) can be used and hence some layout modifications would be suitable more than making the frequency higher.

3.4.5 Summary and comparisons between different designs

Table 3-1: Summary of proposed stimulator with comparisons

	This work	[13]	[19]	[12]
Technology	UMC-0.13µm CMOS Process	0.35µm 3.3-V/24-V CMOS Process	0.18µm LV	0.35µm 3.3-V/24-V CMOS Process
Layout Area	278 X 273 µm²	1000 X 700 µm²	1.2 X 0.9 mm²	600 X 500 µm²

Operating voltage	3.3v	3.3v	0~12v	3.3v, 6v-24v
Current range	Constant 30μA	~40μA	0~3000μA	30μA
Stimulation type	Biphasic	NA		
Electrode configuration	Bipolar	Two Leads Per Site	Bipolar	One Interface Lead Per Site
Loading impedance	1k ~ 150k and 4n ~200n	10k ~ 300k and 1μF	NA	24k ~ 200k
Static power consumption	≤ 429 μW	1.1 ~ 1.4 mW	≤ 150 μW	0.24 - 0.56 mW

Chapter 4: Design II Ultra Low Power multi-waveform current neural stimulator

4.1 Overview

Electrical stimulation has been widely used for treatments of the neurological disorders in various devices such as retinal, cochlear, deep brain tissue and epileptic seizure stimulation implants. The approach is to deliver implementable electrical stimuli through the electrode(s) to the specific tissue areas where relate to the diseases. Current Mode Stimulation (CMS) has been dominated over the voltage mode because of having well manipulation on the injected charge. Regardless of the load (electrode tissue) impedance and its variations, the CMS delivers the amount of charge needed for a desired neural excitation. [1]

4.2 subthreshold (weak inversion)

In analog circuits MOSFET devices are employed as active devices generally, biased in strong inversion (Vgs > Vth, Vds > Vgs- Vth) to be able to operate at high frequencies and at the same time keep the noise level very low. On the other hand, in deep submicron CMOS technology, the negligibility of leakage current when Vgs<Vth is not acceptable manner in those technology. Using CMOS in very low current density applications such as biomedical applications are a very efficient and can achieve the required purpose with low power consumption and acceptable reliability. Subthreshold or weak inversion region is shown in Fig. [53], is used in Ultra Low Power CMOS circuits, as it is high efficiency ratio and minimum power consumption. The main issues associated with weak inversion circuits such as variation due to the PVT, mismatch effects and device noise [21].

4.2.1 Model of MOSFET in weak inversion

$$I_{DS} = 2n\mu_e C_{ox} V_T^2 \frac{W}{L_e}\left(ln^2\left(1 + e^{\frac{(V_p - V_s)}{2V_T}}\right) - ln^2\left(1 + e^{\frac{(V_p - V_D)}{2V_T}}\right)\right)$$

$$I_{DS} = I_S * \left(I_f - I_r\right)$$

Eq. (4.1), (4.2): The first term is called forward channel current, IF, and the second part is called reverse channel current, IR. Also, specific current of the device is

defined as: IS = 2nμeCoxV_T^2.n is the subthreshold slope factor and is usually between 1 and 1.5, μe in [m2/(V · s)], is the effective carrier mobility in the channel and is different for electrons and holes, Nch represents the channel doping density, Cox is the gate oxide capacitance per unit area,V_T = kT /q is the thermodynamic voltage, k is Boltzmann's constant is absolute junction temperature, and q is the elementary electron charge, W and Le are the effective channel width and length of the device,VP is the device pinch off voltage. Model is discussed in details in [20].

$$V_p = V_G - V_{To} - \boldsymbol{\gamma} * \left(\sqrt{V_G - V_{To} + \left(\sqrt{\Psi_o} + \frac{\boldsymbol{\gamma}}{2}\right)^2} - \left(\sqrt{\Psi_o} + \frac{\boldsymbol{\gamma}}{2}\right) \right)$$

where, V_{To}stands for the device threshold voltage and is equal to the gate voltage when the inversion charge density in the channel is zero

$$V_{To} = V_{FB} + \Psi_o + \boldsymbol{\gamma}\sqrt{\Psi_o}$$

where V_{FB} is the flat band voltage.

$$\boldsymbol{\gamma} = \frac{\sqrt{2q\varepsilon_s N_{ch}}}{C_{ox}}$$

$\boldsymbol{\gamma}$ is the substrate factor or body effect ε_s=k*ε_o is the Si dielectric constant (KSi=11.7), $\boldsymbol{N_{ch}}$ is the doping concentration in the substrate, $\Psi_o = 2 * \Psi_f + mV_T$ is the surface potential, $\Psi_f = V_T \ln(\frac{N_{ch}}{n_i})$ is the substrate Fermi potential, and ni stands for the intrinsic carrier concentration of Si.

Derivative of the gate voltage with respect to the pinch off voltage is defined as the device subthreshold slope factor given by:

$$n = \frac{dV_G}{dV_p} = 1 + \frac{\boldsymbol{\gamma}}{2\sqrt{\Psi_o + V_p}}$$

$$V_p \cong \frac{V_G - V_{To}}{n}$$

so, the current in saturation (strong inversion):

$$I_{DS} = \frac{n\mu_e C_{ox}}{2}\frac{W}{L_e}\left(\left(V_p - V_s\right)^2 - \left(V_p - V_D\right)^2\right)$$

$$I_{DS} \cong \frac{\mu_e C_{ox}}{2n}\frac{W}{L_e}(V_G - nV_s - V_{To})^2$$

It is noticeable that the current sensitivity to the source voltage is n times more than gate voltage. In other words: gm,s = n × gm. Assuming that n is equal to one, then above equation simplified to the conventional equation:

$$I_{DS} \cong 2n\mu_e C_{ox}\frac{W}{L_e}V_T^2\left(e^{\frac{V_p - V_s}{V_T}} - e^{\frac{V_p - V_D}{V_T}}\right)$$

$$\cong 2n\mu_e C_{ox}\frac{W}{L_e}V_T^2 e^{\frac{V_G - V_{To}}{nV_T}}\left(e^{\frac{-V_s}{V_T}} - e^{\frac{-V_D}{V_T}}\right)$$

$$I_{DS} \cong I_{Do}\frac{W}{L_e}e^{\frac{V_G - V_{To}}{nV_T}}\left(e^{\frac{-V_s}{V_T}} - e^{\frac{-V_D}{V_T}}\right)$$

$$I_{DS} \cong I_{Do}\frac{W}{L_e}e^{\frac{V_G - V_{To}}{nV_T}}\left(e^{\frac{-V_s}{V_T}} - e^{\frac{-V_D}{V_T}}\right)$$

Considering V_s = 0 and V_D >>V_T in our design current equation can be simplified to:

$$I_{DS} \cong I_{D1}\frac{W}{L_e}e^{\frac{V_G}{nV_T}}$$

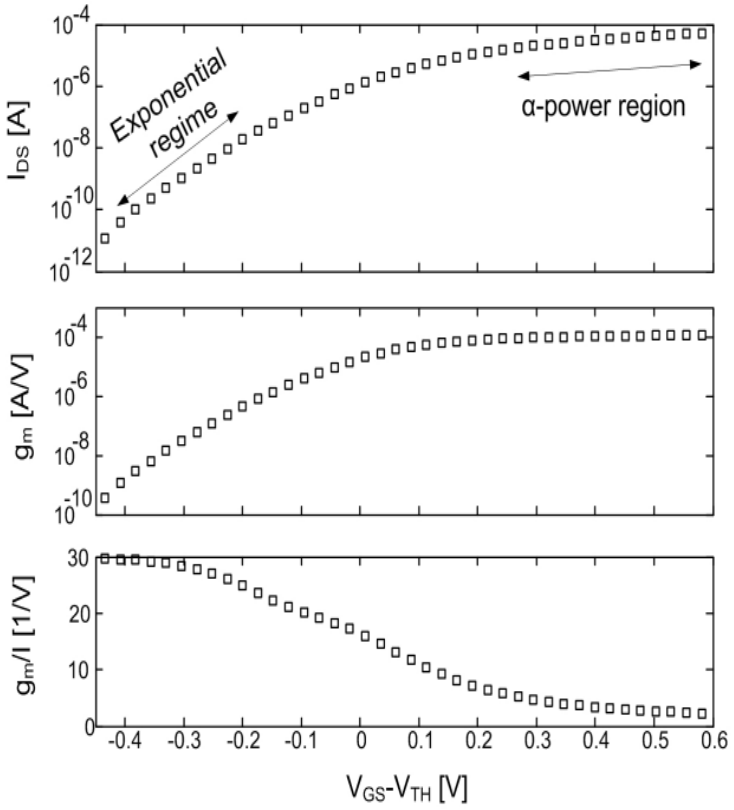

Figure 53: I-V characteristic in subthreshold region

4.2.2 Design consideration in weak inversion

the extreme issue in subthreshold design is exponential effects which appear in current equation:

$$I_{DS} \cong I_{Do} \frac{W}{L_e} e^{\frac{V_G - V_{To}}{nV_T}} \left(e^{\frac{-V_S}{V_T}} - e^{\frac{-V_D}{V_T}} \right)$$

it clearly illustrates the exponential I-V characteristics of a MOS device biased in (subthreshold). This characteristic is on one hand useful for implementing widely tunable circuits, while on the other hand, it represents the high sensitivity of the circuit to PVT variations. For example, any small variation on device threshold voltage (V_{To}) will be translated to exponential variation on the bias current. In addition to Device mismatch is one of the most important design issues especially in design of high performance analog systems in modern deep-submicron (DSM) technologies. Experiments show that the two main sources of introducing mismatch among devices are difference in threshold voltage (ΔV_T) and current factor,

($\Delta\beta$, where $\beta = \mu CoxW/Le$). The difference among devices raised from difference in V_T and β have random nature with a normal distribution where their mean values are $V_{To} and\ \beta o$. The variance of these parameters can be presented by:

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{w.L}$$

$$\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 = \frac{A_\beta^2}{w.L}$$

where proportionality constants A_{VT} and A_β are technology dependent parameters.

Let us (for simplicity) assume simple current mirror and differential pair, it can be shown that the mismatch between current values and input referred voltage offset are, respectively:

$$\left(\frac{\sigma(\Delta I_{DS})}{I_{DS}}\right)^2 = \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \left(\frac{gm}{I}\right)^2 \sigma^2(\Delta V_T)$$

$$\sigma^2(\Delta V_{GS}) = \sigma^2(\Delta V_T) + \left(\frac{gm}{I}\right)^2 \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2$$

Since the value of gm/I has its maximum value in subthreshold, and regarding to previous equation.it is expected that the voltage matching improves slightly by moving towards weak inversion, while the current matching degrades. This implies that implementing current mirrors with acceptable level of matching will be much more difficult in weak inversion region compared to the current mirrors implemented in strong inversion region.

4.3 Transmission Gates

Transmission gates (TG) represent an analog switch, a transmission gate consists of a PMOS and NMOS connected in parallel [1]. Gate voltage applied to these gates is complementary of each other ($V_{control}$ and $\bar{V}_{control}$)shown in Fig. [54] . Transmission gates act as bidirectional switch between two nodes A and B controlled. by signal $\mathrm{V_{control}}$. Gate of NMOS is connected to $\mathrm{V_{control}}$ and gate of PMOS is connected $\bar{V}_{control}$ to (invert of $V_{control}$). When control signal $V_{control}$ is high i.e. V_{DD} both transistor is on and provides a low resistance path between A and B. On the other hand, when $V_{control}$ is low, both transistors are turned off and provide high impedance path between A and B.

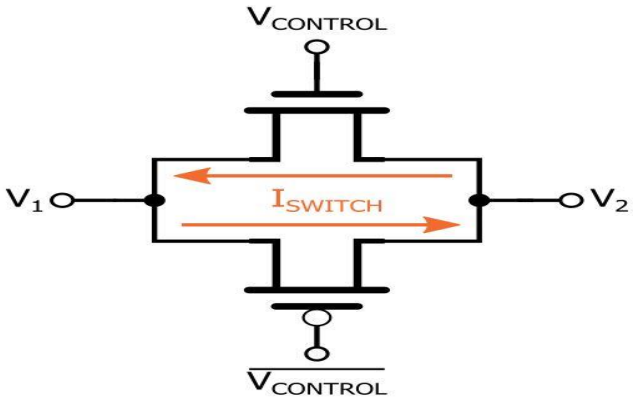

Figure 54: Transmission Gate

A detailed analysis of working of transmission gates follows:

When input node V_1 is connected to V_{DD} and control logic is also high ,

$V_{control}$ =V_{DD} :

The output V_2 node may be connected to capacitor. Voltage at output node is V_{out}.

For PMOS, Source of is at higher voltage than drain.

For NMOS, drain is at higher voltage than Source terminal.

Hence, node V_1 will act as source terminal for PMOS and as drain terminal for NMOS.

Drain to Source and gate to source voltages for NMOS are as:

$$V_{DS,n} = V_{DD} - V_{out}$$

$$V_{GS,n} = V_{DD} - V_{out}$$

For NMOS to be turned off, $V_{GS,n} < V_{th,n}$

$$V_{DD} - V_{out} < V_{th,n}$$

$$V_{out} > V_{DD} - V_{th,n}$$ (Cut off region)

For $V_{out} < V_{DD} - V_{th,n}$

$V_{DS,n} > V_{GS,n} - V_{th,n}$

i.e. will operate in saturation mode

Similarly, for PMOS,

$$V_{DS,p} = V_{out} - V_{DD}$$

$$V_{GS,p} = -V_{DD}$$

For PMOS to be turned off $V_{GS,p} > v_{th,p}$ threshold voltage for PMOS is -ve so PMOS will always be turned on.

For PMOS to operate in linear region, $V_{DS} > V_{GS} - v_{th,p}$

$$V_{out} - V_{DD} > -V_{DD} - V_{th,p}$$

$$V_{out} > -V_{th,p}$$

$$V_{out} > |V_{th,p}|$$

For $V_{out} \leq |V_{thp}|$, PMOS will be in saturation mode.

Unlike NMOS, PMOS remain turned on regardless of output voltage V_{out} as shown in Fig. [55].

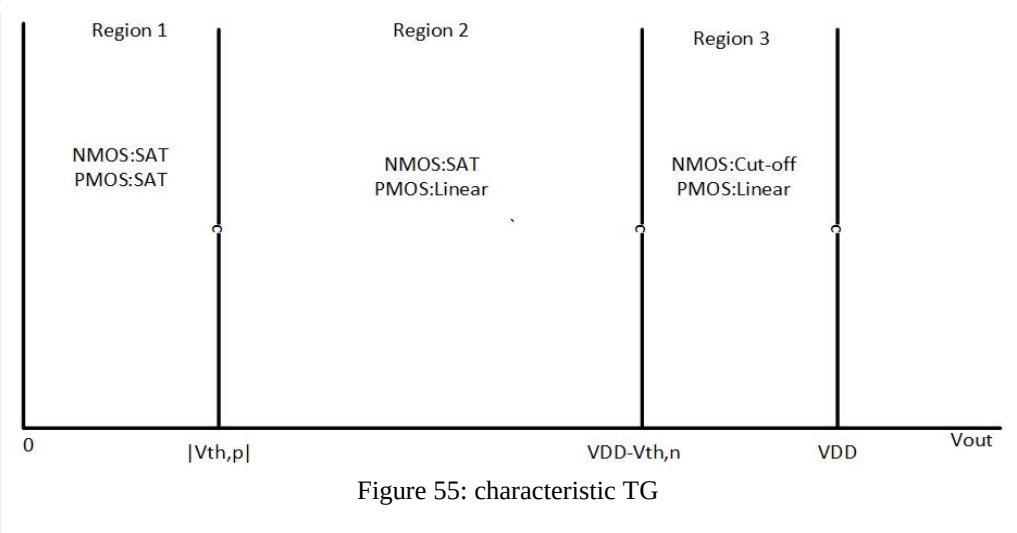

Figure 55: characteristic TG

Thus PMOS will always be turned on, and as it is known that PMOS Passes a strong 1 so voltage level high will be transmitted unattenuated. Similarly,

When voltage V_1 at node , V_1 = 0 and $V_{control}$ =V_{DD} , node V_1 will act as source terminal for NMOS and will act as drain for PMOS. NMOS will always be turned on hence level 0 will also be transmitted unattenuated.

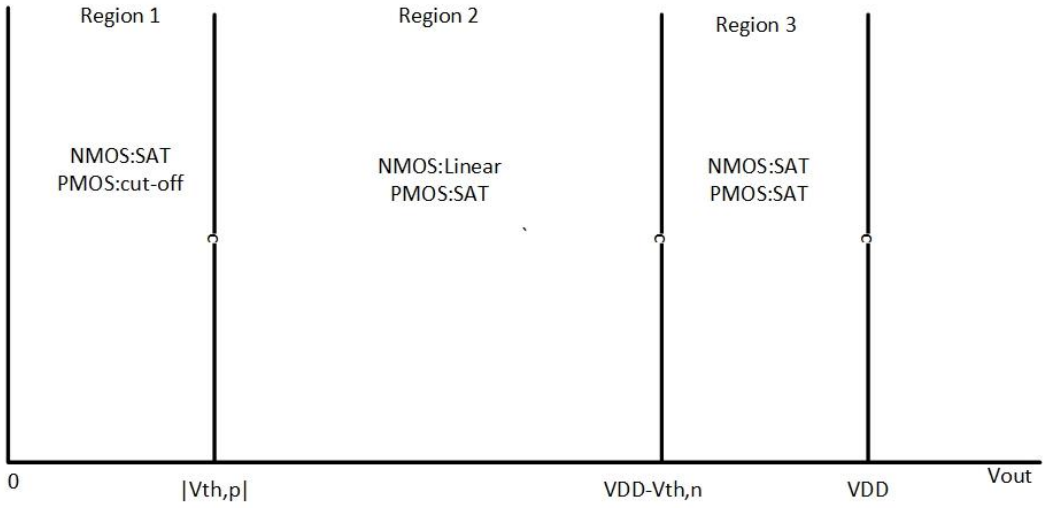

Figure 56: characteristic TG (b)

when voltage V_1 at node, V_1 =V_{DD} and $V_{control}$= 0: node V_1 will act as drain terminal for NMOS and source terminal for PMOS

$V_{GS,n} = 0 - \boldsymbol{V_{DD}} < V_{th,n}$ (cut off region)

Hence NMOS will be turned off

$V_{GS,p} = \boldsymbol{V_{DD}}\text{-}\boldsymbol{V_{DD}} = 0 > V_{th,p}$ (Cut off region)

Thus both transistor will remain off. Path between A and B will be an open circuit.

when voltage at node V_1, V_1 = 0 and $\boldsymbol{V_{control}}$= 0 : node V_1 will act as source terminal for NMOS and will act as drain for PMOS.

$V_{GS,n} = 0 - 0 = 0 < V_{th,n}$ (Cut off region)

$$V_{GS,p} = \boldsymbol{V_{DD}} - \boldsymbol{V_{out}}$$

$V_{GS,p}$ will be some positive voltage and threshold voltage of PMOS ,Vth,p is negative.

$V_{GS,p} > V_{th,p}$ (Cut off region)

Hence both transistor will remain off and high impedance path exists between A and B.

The equivalent resistance of TG can enhance the switching between two states, on the other hand This nonlinear resistance in case of NMOS or PMOS only can causes errors in dc accuracy as well as ac distortion.TG solves this problem.

On-resistance is minimized, linearity is also improved, and the low impedance node or high impedance node improved also; as equivalent resistance is a parallel combination as shown in Fig. [57].

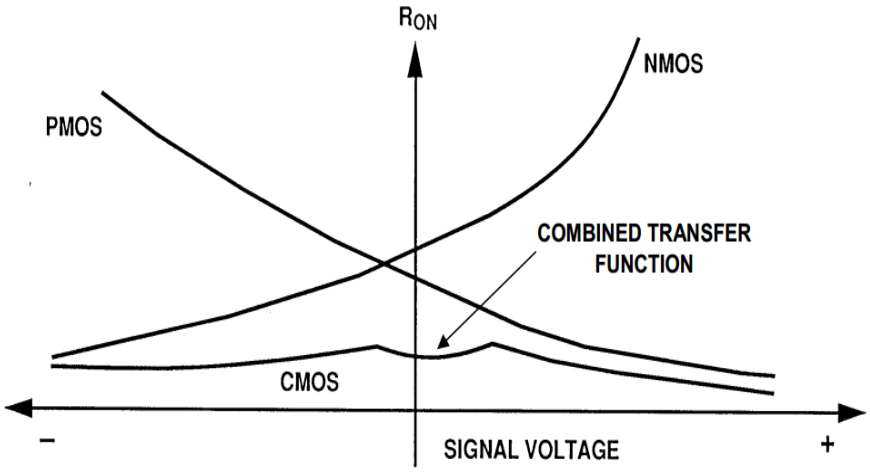

Figure 57: resistance of NMOS, PMOS and equivalent TG

4.3.1 Consideration in design analog switch TG:

Clock feedthrough [22]:

An analog switch is a basic component in integrated circuits (ICs). The on/off behavior of an analog switch is controlled by the gate voltages that govern the presence of charge in the inversion channel underneath the gates. A CMOS transmission gate switch which is used with process scaling and the increasing demand for portable systems, a lower power supply voltage has become common. In order to pass a large analog signal. A TG switch has an approximately uniform on-resistance as shown before, and can pass wide analog signal swings. Clock feedthrough Fig. [58] is a fundamental problem in analog switch ICs. The most commonly accepted clock feedthrough mechanism (in the charge domain) occurs when the switch is turned off, dispersing the charge in the inversion channel, forcing current to flow either into the substrate or the load capacitor at the MOSFET drain or source. This mechanism produces an error voltage on the load capacitor. This flow of electrons was called charge feedthrough.

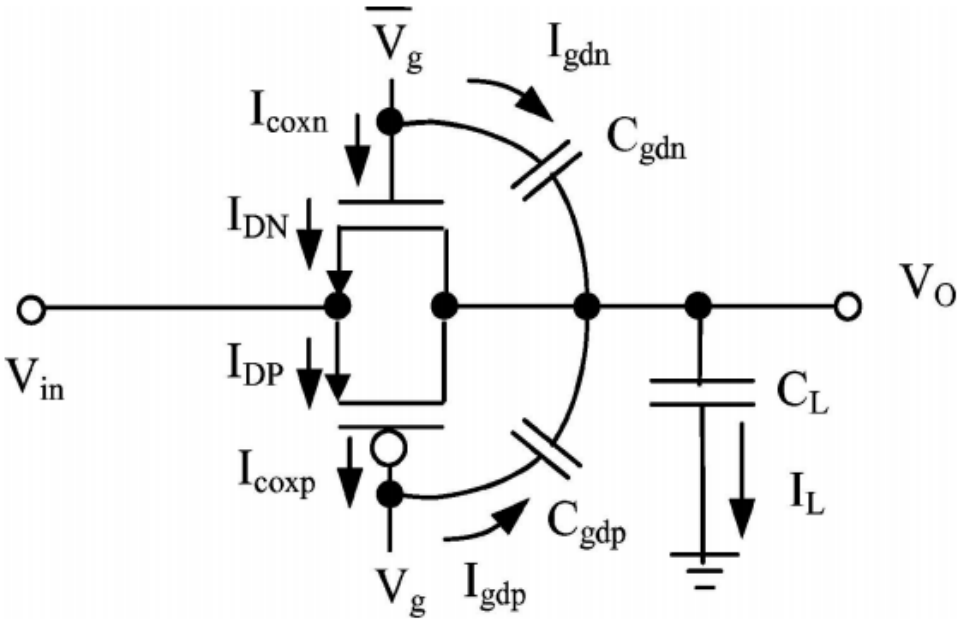

Figure 58: feedthrough issue in TG at off state

4.4 Rising ramp generator

For the exponential waveforms, rising and falling ramp generator are needed,that is shown in Fig. [59]. For the rising ramp voltage, the topology is a simple current integrator as depicted in Fig.3. The rising ramp voltage would be generated by offset voltage when applied clock to TG is high thus capacitor will have certain voltage in certain time till, on other state of cycle the other TG will be closed and capacitor will charge by biasing current. The slope of ramp can be changed by applied Current and capacitance the operation of rising ramp is shown in Fig. [60].

$$V_{Rise\_Ramp} = V_{offset} + \frac{I_c}{C} * t$$

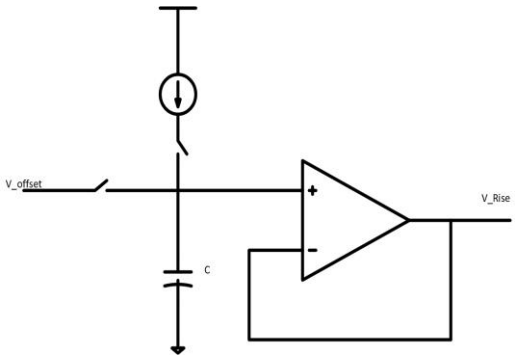

Figure 59: Rising Ramp Generator

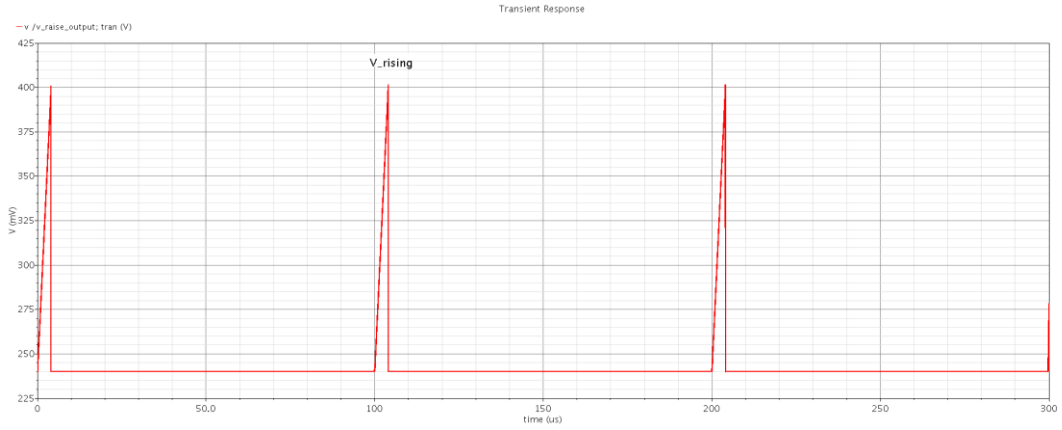

Figure 60: rising ramp at 10 KHz

4.5 Falling ramp generator

Similarly, to raising ramp falling ramp generated by capacitor will precharge to arbitrary offset voltage during open circuit of sink biasing current Fig. [61], at the other state of applied clock capacitor will discharge in certain time.

$$V_{Fall\_Ramp} = V_{offset} - \frac{I_c}{C} * t$$

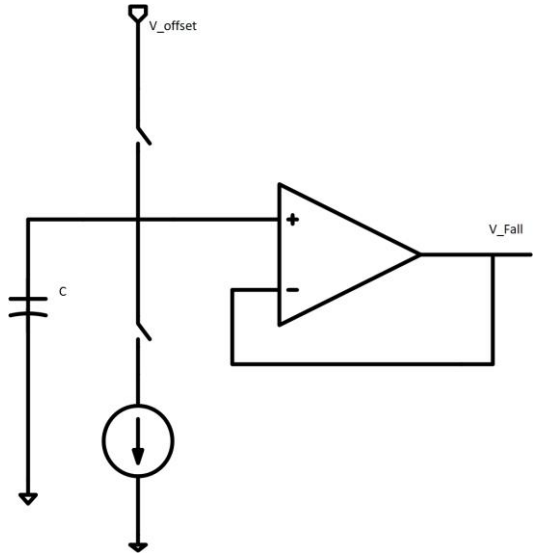

Figure 61: Falling Ramp Generator

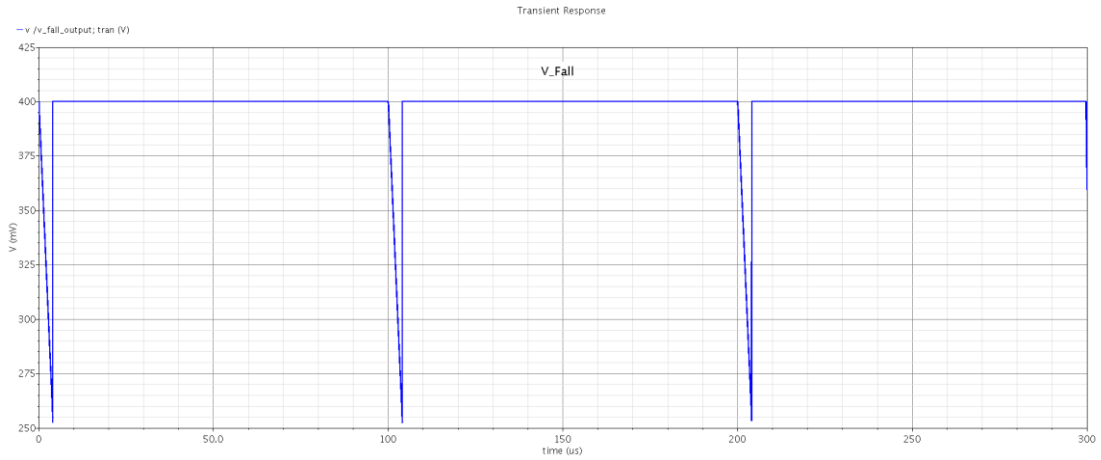

Figure 62: falling ramp waveform at 10 KHz

he applied control waveforms voltage to transmission gate is shown in Fig. [63].

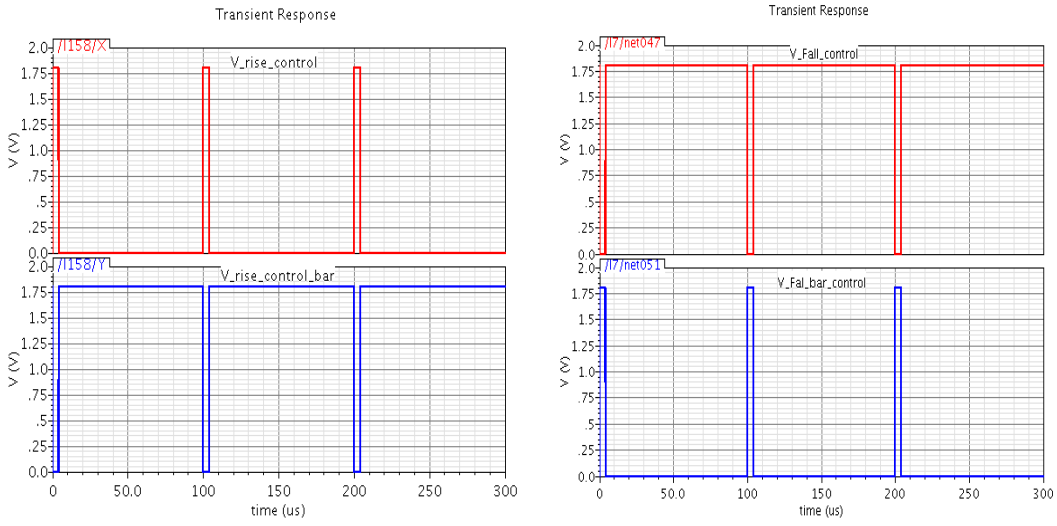

Figure 63: control input waveform rising and falling at frequency =10 KHz

4.6 Operational Trans-Conductance Amplifier (OTA)

The operational amplifier is an extremely versatile general purpose linear circuit which is used widely in analog design circuits [23]. A firm understanding of some of the specifications used to identify operational amplifiers is necessary to determine if an amplifier will be satisfactory in an intended application specially in low power applications, typically the vital issue in design is conflicting between different parameters. Operational amplifiers had their origins in analog computers, where they were used to perform mathematical operations in many linear, non-linear and frequency-dependent circuits. The popularity of the op-amp as a building block in analog circuits is due to its versatility. Due to negative feedback, the characteristics of an op-amp circuit, its gain, input and output impedance, bandwidth etc. are determined by external components and have little dependence on temperature coefficients or manufacturing variations in the op-amp itself . OTA's applications comprise amplifiers, summers, multipliers, differentiators, integrators, continuous-time OTA-C filters, voltage controlled oscillators, and continuous-time sigma-delta modulators.

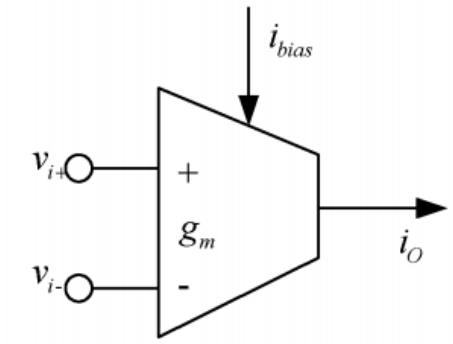

Figure 64: single ended OTA symbol

4.6.1 specifications of OTA

- Open Loop Gain:

The open-loop gain Fig. [65] is the gain of the amplifier without the feedback loop being closed, hence the name “open-loop.” For a precision op amp this gain can be very high. This gain is flat from dc to what is referred to as the dominant pole. This is referred to as a single-pole response. It will continue to fall at this rate until it hits another pole in the response. This 2nd pole will double the rate at which the open-loop gain falls. If the open-loop gain has dropped below 0 dB (unity gain) before it

hits the 2nd pole, the op amp will be unconditional stable at any gain. This will be typically referred to as unity gain stable. If the 2nd pole is reached while the loop gain is greater than 1 (0 dB), then the amplifier may not be stable under some conditions.

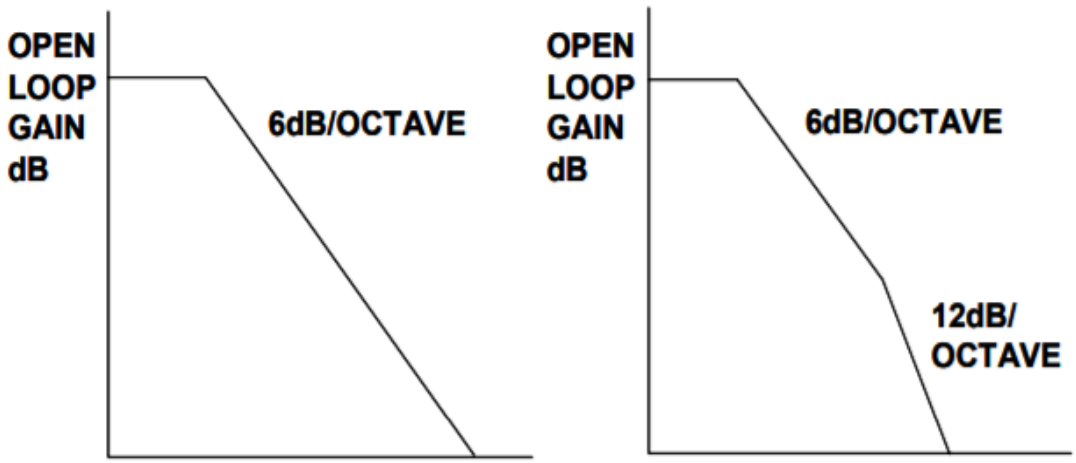

Figure 65: Open-Loop Gain

- Closed Loop Gain:

This is the gain of the amplifier with the feedback loop closed, as opposed the open-loop gain, which is the gain with the feedback loop opened. It has two forms, signal gain and noise gain. These are described and differentiated below.

- Gain Bandwidth Product:

If we multiply the open-loop gain by the frequency the product is always a constant. The caveat for this is that we have to be in the part of the curve that is falling at 6 dB/octave. This gives us a convenient figure of merit with which to determine if a particular op amp is useable in a particular application due to certain application.

- Stability Criteria:

Feedback theory states that the closed-loop gain must intersect the open-loop gain at a rate of 6 dB/octave (single-pole response) for the system to be stable. If the response is 12 dB/octave (2 pole response) the op amp will oscillate. The easiest way to think of this is that each pole adds 90° of phase shift. Two poles then mean 180°, and 180°

of phase shift turns negative feedback into positive feedback, which means oscillations.

- Slew Rate:

The maximum time rate of change of output voltage. This quantity depends on compensation for an externally compensated amplifier and maximum biasing current Fig [66].

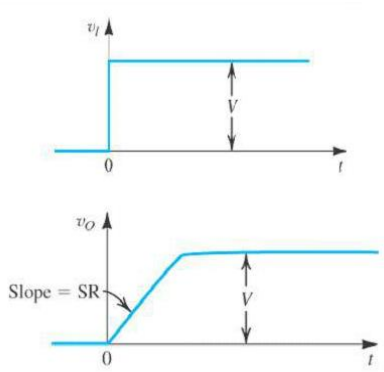

Figure 66: Slew Rate

- Input bias current:

  All op-amps must have some input bias current however small. This value is typically in the Nano ampere region but is can be in the Pico ampere region for premium parts and even the femtoampere region for op-amps made for what is known as electrometer applications. Positive bias current is current into the part. Bias current can be either positive or negative and we are usually only concerned with the magnitude.

  OTA Types:

  1- Fully differential OTA.

  2- cross-coupled differential pairs input with floating voltage adjustment.

  3- fully differential complementary OTA with high linearity.

  4- Single ended OTA.

5- Single ended current based OTA.

4.6.2 Designed OTA

In proposed OTA Fig. [67] is used in unity negative feedback topology with high gain to reduce offset between input voltage and with low biasing current 100 nA to achieve low power consumption and single ended to fit area constrain. the ramp generators which will be input voltage to desired OTA was built simply with charging or discharging capacitor and with low basing current and low input offset to maintain it in subthreshold region.

The specification of our design proved that gain OTA is equal to 46 dB which is very enough to buffer rising and falling signals and slew rate equal to 100 A/µS at load capacitance 100 fF.and phase margin 50 deg to ensure stability and proper operation.

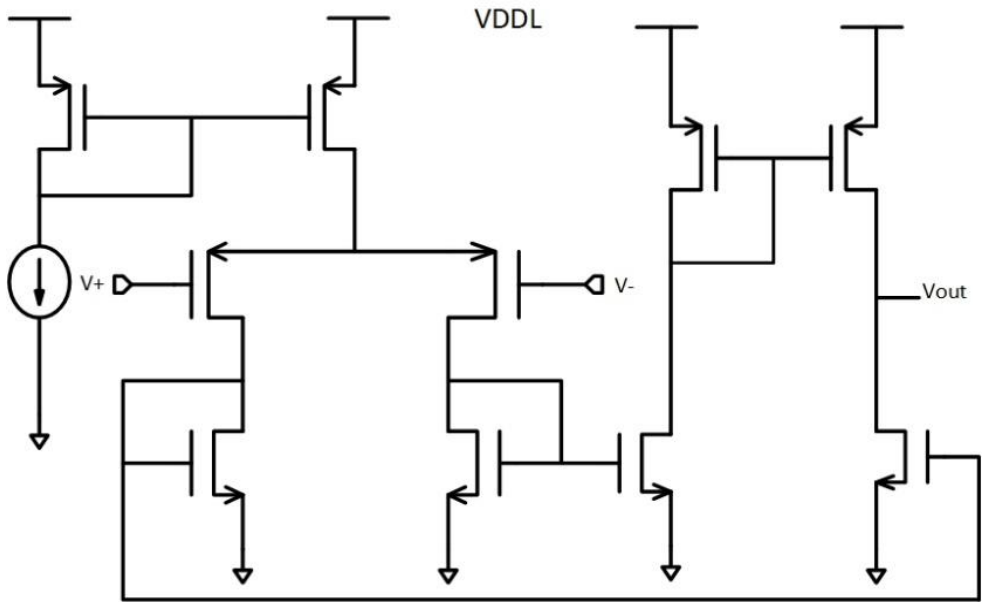

Figure 67: Desired OTA current based

4.7 Biasing Current

Low voltage current source is designed Fig. [68] with low process variation and low power consumption to achieve the stimulation parameters, the input biasing voltage Vin=400 mV is lower than threshold voltage of M1 transistor to force it in subthreshold region, M3-M4 is designed to be in saturation with suitable aspect ratio to mirror current accurately and due to long channel length there is no large mismatch between pairs and layout technique like dummies and centroid is used to reduce

mismatching. The current will flow through M2 with same size of M1then the gate to source voltage of M2 will be approximately 400 mV.the M5-M6 and M7-M8 will produce current in resistance I_{in}.

$$I_{in} = \frac{V_{in}}{R}$$

The source follower topology which is used with M6 and negative feedback enables us to equally input diff-pair. The output current branches for PMOS-NMOS is mirrored to fit for steering or sinking currents for proposed ramp generators.

It is possible to use mirrored current with suitable ratio between M8-M9 for raising ramp generator, on the other hand M10-M11 as a sink current for falling ramp.

The value of resistance is 160 KΩ we can implement it off-chip to avoid process variation. Also to force low current passing in branches.

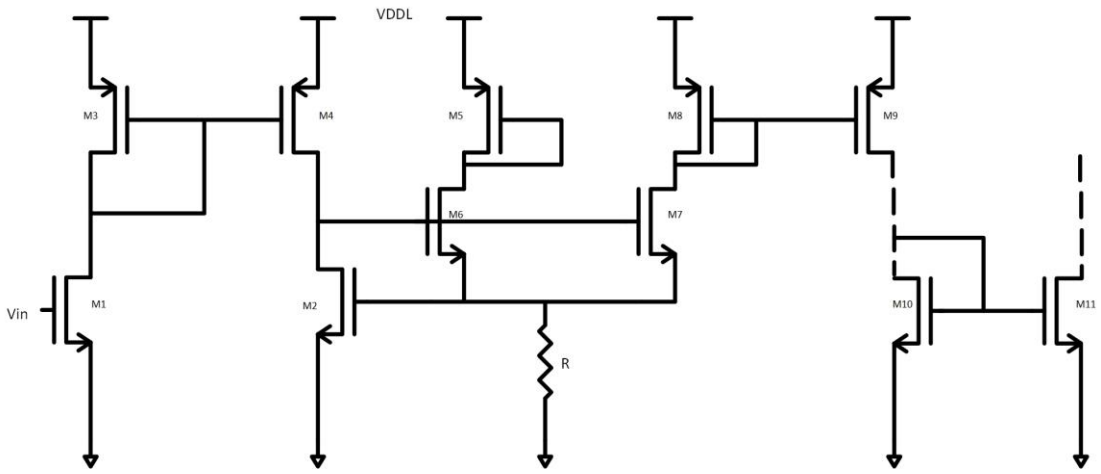

Figure 68: proposed low voltage current source

I_{in} is then attenuated about 500 times to become around 5 nA reference current flowing through M8 and M7, I_{in} is defined independent of the threshold voltage which helps to minimize process variation effects on the output current. The above mentioned value for Vin in the proposed current source, originates from two considerations. First, in should be large enough with respect to the variations of VGS M2 that is caused by the mismatches. On the other hand, the value of R may not be

too large since it occupies great portions of the chip area and produces substantial amount of thermal noise. Therefore, for large values of the Vin, there is a constraint on the resistor size to generate the predefined magnitude of I_{in}.In order to compromise between these two criteria, the Vin has been chosen to be equal to 400 mV as it was said before. The following Table shown process variation on biasing circuit.

Table 4-1: Process and voltage variation

VDDL / corner	1.7 V	1.8 V	1.9 V
TT	474.23 nA	479 nA	483.11 nA
FF	474.23 nA	479 nA	483.11 nA
SS	474.23 nA	479 nA	483.11 nA

4.8 Shared OTA to reduce power consumption:

The generators are needing two different OTAs as shown in above sections to get required output ramps (falling, rising), so to reduce the area and power consumption as well, we have been designed switching scheme with special input waveforms to have shared OTA with 3 different output waveforms (rising, falling, rectangle) as shown in Fig. [69].

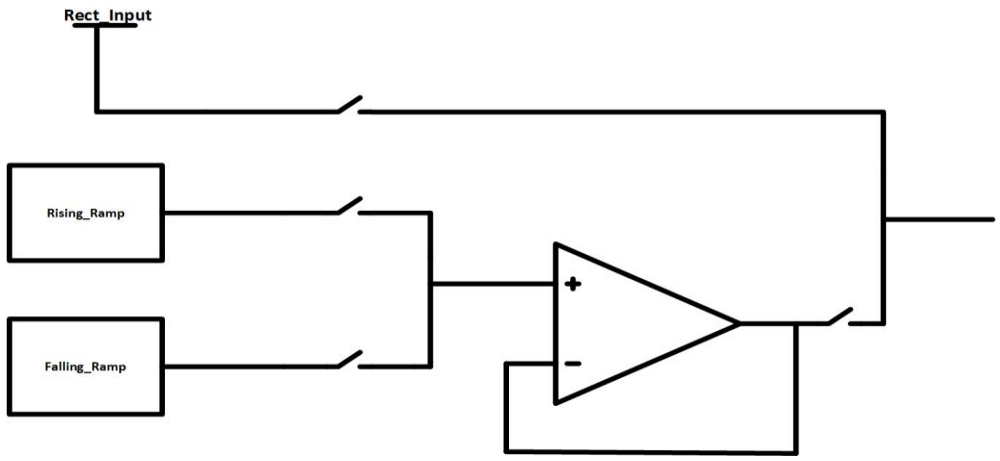

Figure 69: the desired block diagram to minimize area and power

The following input waveforms Fig [70] enable us to maintain 3 different output of neural current stimulation rising expediential, falling expediential and rectangle which will be discussed in the following sections.

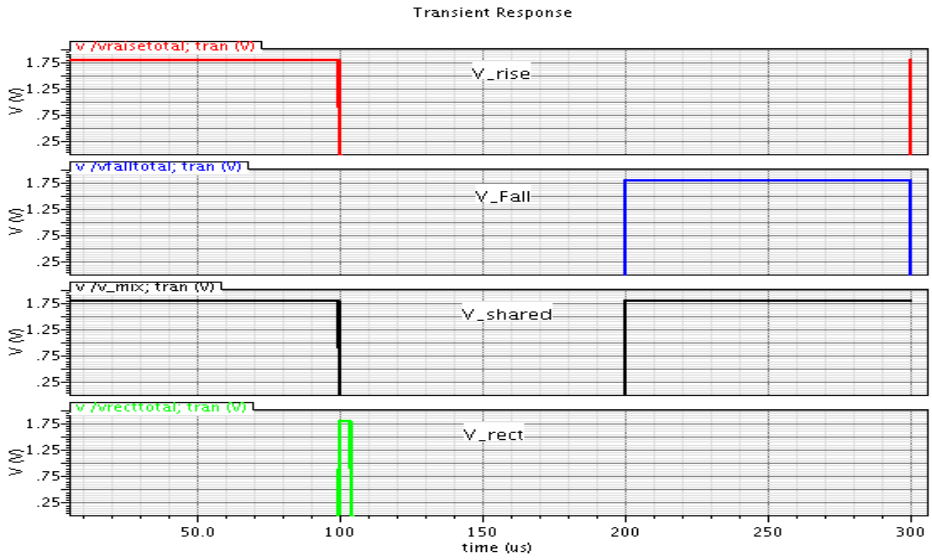

Figure 70: different waveforms are applied to TG switching scheme

If we assume the cycle will be 300 usec to generate required output at frequency 10 KHz, first the rising ramp will be produced as illustrated before, then the first TG which connected to its output will pass the ramp and buffered through OTA, during this period -100 usec-the another TG is off and doesn't pass falling ramp to OTA.the TG which is controlling the rectangle output which is generated by constant DC value will be on and pass DC value, finally falling ramp will be generated during its TG is on in last 100 usec and buffered through OTA.The shared waveform which is applied to forth TG have an important role to mix 3 waveforms at output node as it is illustrated in Fig. [71], the output node will be connected to 4 bit binary weighted current digital to analog converter (DAC) which will produce the stimulation current .So the output signals which will be applied to 4-bit DAC is a combination between rising ramp, falling ramp and rectangular pulse, the following waveforms will explain the changes before and after each TG and OTA till applied signal to DAC.The reduction in number of designed OTA save area and power consumption. The frequency of operation is not necessary to be 10kHz and this is not effective parameter in our design.

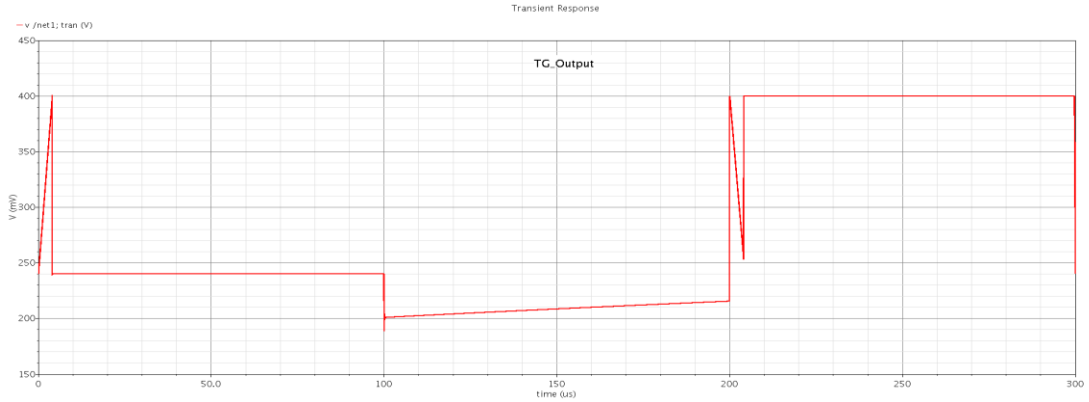

Figure 71: first 2 TG output shown mixed rising and falling (a)

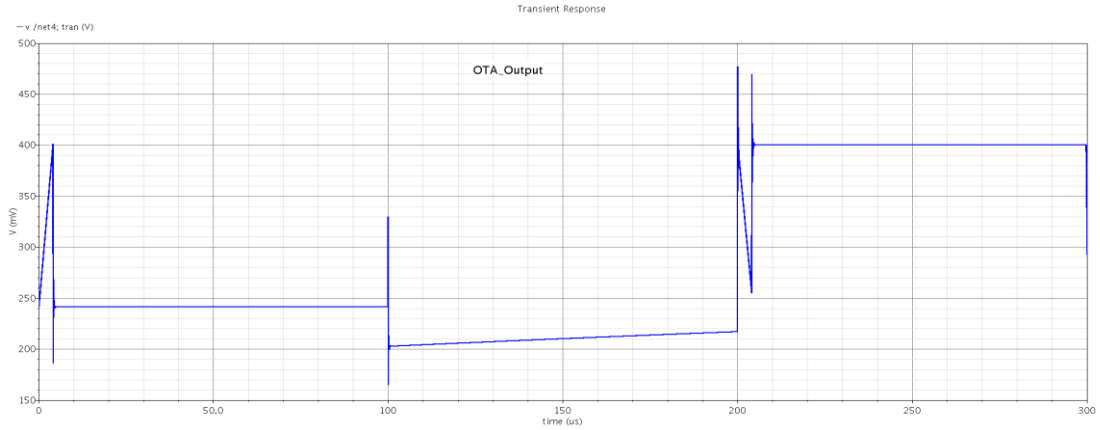

Figure 72: OTA output after mixing ramps (b)

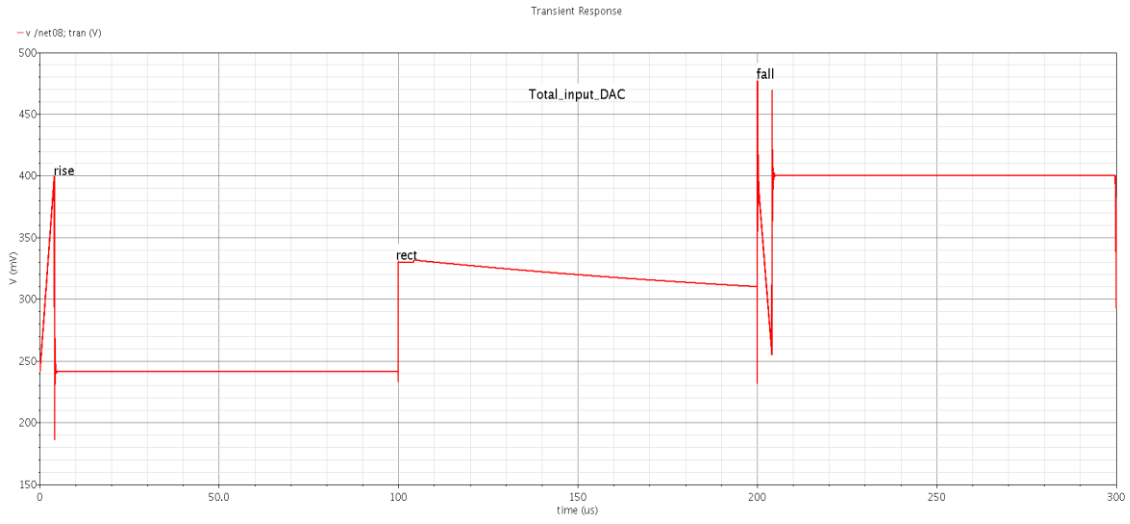

Figure 73: finally output which will be applied to DAC

The generation of rising and falling ramps are depending on biasing current as shown in above sections the following section will discuss very low power biasing current which is working in subthreshold region to satisfy design specifications.

4.9 DACs Digital to analog Converters

D/A converters Fig. [74] are type of data converters which convert digital code to finite analog signal [27]. After recording the behavior of Brain the digital code is produced then we need to convert it to an analog signal to make necessary stimulation step. DACs are available with wide range of specifications specified by application requirements. Some of the important specifications are Resolution, Accuracy, linearity, monotonicity, conversion time, settling time and stability on the other hand, DACs have some Dynamic specifications will be discussed briefly.

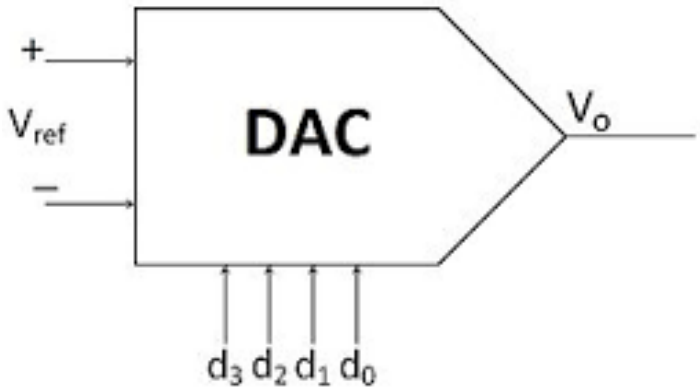

Figure 74: Digital to analog converter

4.9.1 Specifications

A) static specifications

- Resolution: is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB (least significant bit) at the digital input. Simply, resolution is the value of LSB.
- Accuracy (full scale range):Absolute accuracy is the maximum deviation between the actual converter output and the ideal
  converter output. The ideal converter is the one which does not suffer from any problem. Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors. The relative accuracy is the maximum deviation after the gain and offset errors have been removed. Accuracy is also given in terms of LSB increments or percentage of full-scale voltage shown in Fig. [75].

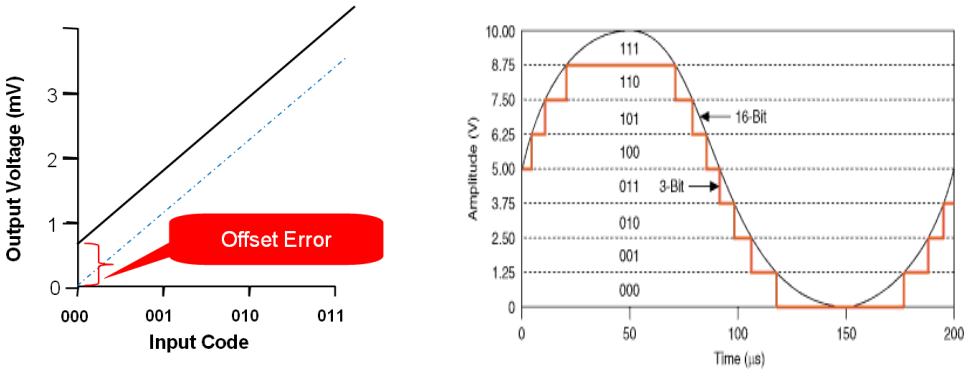

Figure 75: static specifications shown accuracy and resolution

Monotonically: A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristic is essential in control applications is shown in Fig. [76]. Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition. When a D/A Converter doesn't satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input.

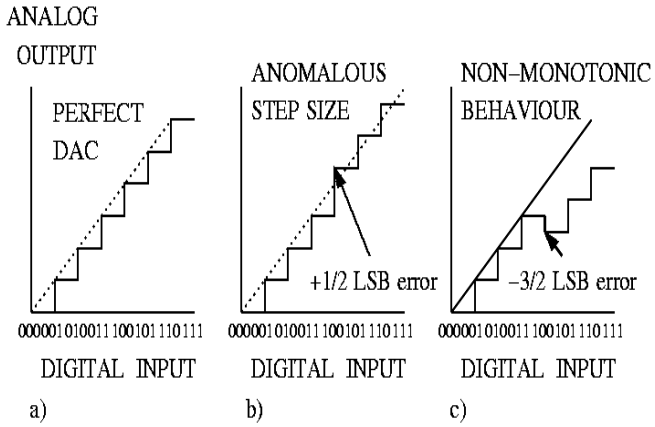

Figure 76: static specifications shown different errors can occur in output of DAC

B) Dynamic specifications:

- Conversion time: It is the time taken for the D/A converter to produce the analog output for the given binary input signal. It depends on the response time of

switches and the output of the Amplifier. D/A converters speed can be defined by this parameter. It is also called as setting time.

- Glitch energy: A glitch is the transient that occurs on an analog output as the DAC changes from one value to another Fig. [77]. A common cause of glitches are some analog output switches on the DAC operate faster than others, which produces temporary, spurious effects on the output until all switches have settled. Another common cause of glitches are the capacitive coupling between digital and analog outputs.

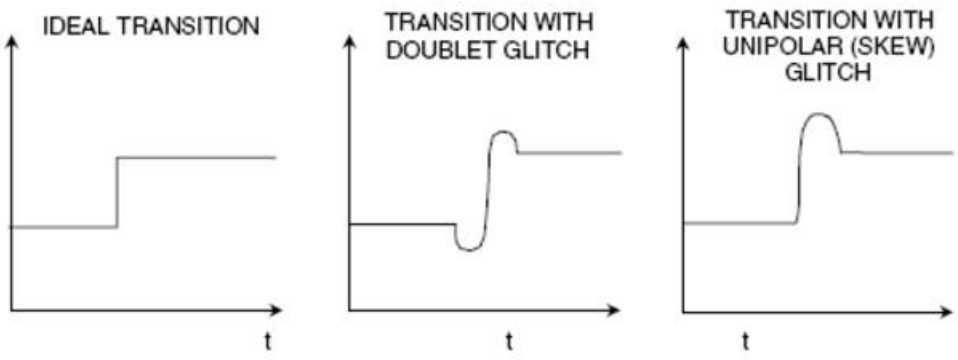

Figure 77: Glitch energy occurrence

4.9.2 DAC Types:

1- Pulse-width modulator DAC:

This is the most straight forward DAC kind. This sort of DACs work by continuously switching a constant current or voltage by a duration into low pass filter. The duration of the switching is determined by the binary input code to the DAC. Major application of them is speed and torque control of motors. Other than that they are used in many different applications as well [24].

2- Over-sampling DAC:

The over-sampling DAC are interpolation based DACs. These DACs utilize pulse density conversion strategy to convert digital bit stream into an analog signal. This technique enables low internal resolution.as the output is genuinely linear. A 1-bit DAC is seldom employed. The DAC operates on Delta-Sigma technology.in this method a pulse density modulated signal is used as input. Oversampling DACs are used where very high resolution is required, for instance greater than 16 bits because of its high linearity and low cost. furthermore, over sampling rate performance requirement of low pass filter at the output and consequently entails

further mitigation of noise due to quantization. With delta-sigma method sampling rate up-to 100,000 sample/s and resolution of 24 bit can be obtained.

3- Thermometer-coded DAC

The thermometer-coded DAC consists of equal number of current source part as the number of possible output values of the designed DACs, one for each one. For instance, a thermometer-coded DAC will have 255 segments and 65,535 segments if it had been designed for 8 and 16-bit input respectively although such DACs have the highest speed and accuracy, they are highly expensive and complex compared to other kinds of DACs. Such DACs can process greater than 1 billion samples per second which is greater than any other type of DAC.

4- Hybrid DAC:

Hybrid DAC as the name suggests is a kind of DAC that combines two or more of the techniques described above. In most integrated devices where DACs are used, hybrid DAC is more preferred as using it is difficult to provide a balance among cost, speed and precision using any one of the techniques mentioned above is very challenging. A case in point, the segmented DACs is special kind of hybrid DAC which combines tow principles. While for the most significant bits it employs the thermometer-coded principle, and for the least significant bits,it utilizes the binary-weighted principle. Via this hybrid methodology, a tradeoff is achieved in between the precision of the DAC and the number of current source required by the DAC

5- R-2R LADDER DAC:

Fig. [78] An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin’s theorem in arriving at the desired output voltages. The R-2R network consists of resistors with only two values - R and 2xR. If each input is supplied either 0 volts or reference voltage, the output voltage will be an analog equivalent of the binary value of the three bits. VS2 corresponds to the most significant bit (MSB) while VS0 corresponds to the least significant bit (LSB).

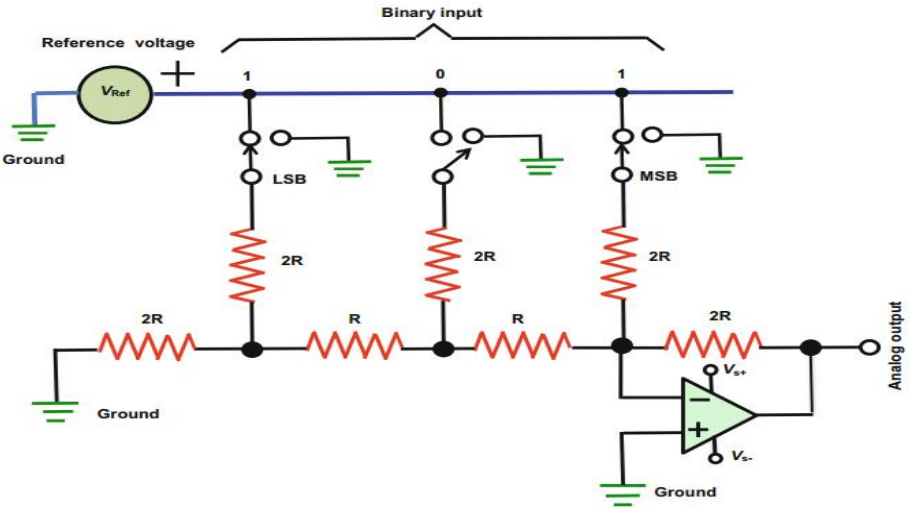

Figure 78: R-2R Ladder DAC

6- The Binary Weighted DAC:

Fig. [79] An alternative to Ladder DAC, which uses multiple resistor values. A disadvantage of the former DAC design was its requirement of several different precise input resistor values: one unique value per binary input bit. Manufacture may be simplified if there are fewer different resistor values to purchase, stock, and sort prior to assembly. The above types can't be used in low power application especially biomedical applications.

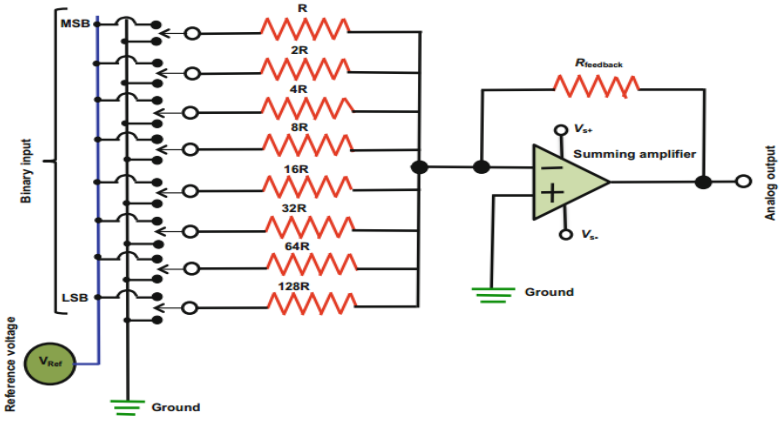

Figure 79: binary weighted resistor DAC

7- Switched capacitor DACs:

Fig. [80] is a charge-mode. Switched-capacitor DACs are the most popular DAC for ADC architectures. They can be switched into configurations to realize many different functions, making them good for implementing various types of mathematical algorithms in addition to the DAC operation.

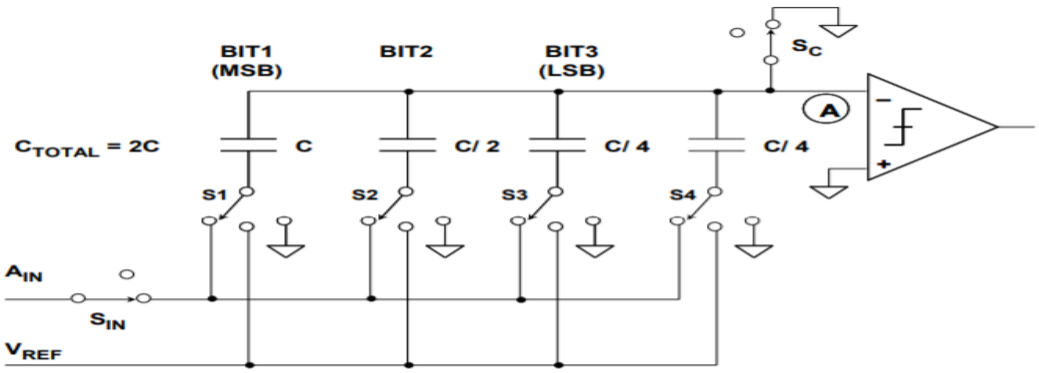

Figure 80: switched Capacitor DAC

8- Current mode DACs:

Fig. [81] Current-steering DACs are a more common integrated DAC compared to resistor DACs. They are probably the most common bias DAC architecture due to their small size and simplicity. The current-steering DAC replaces the resistor element in the resistor DAC architectures with a MOSFET current element and uses some form of summation of the current elements to produce the result. Sometimes the result needs to be a current such as in integrated bias circuits. This current is then passed to the next stage of a current mirror bias or passes through a MOSFET stack to produce a set of current mirror bias voltages. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler and in Current mode or inverted ladder type DACs, the stray capacitance does not affect the speed of response of the circuit due to constant ladder node voltages. So improved speed performance.

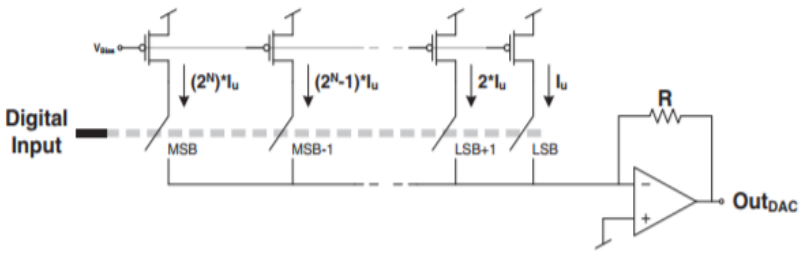

Figure 81: current steering DAC

Many of the DACs in literatures are based on device scaling techniques, namely current scaling, voltage scaling and charge scaling. Current-mode D/A converters are intended for high speed applications, though it has also the potential of being utilized in low power application where speed is not the major concern. Many techniques have been developed to tackle various error sources in DAC [32]. These errors can be divided into several major groups, these are: amplitude errors, output impedance, DC errors by thermal noise, output interconnect network, clock skew, mismatch based time skew, clock reflections, nonlinear settling, clock jitter, power supply bounce, substrate noise, etc.to resolve these problems the design method can be categorized into several levels these are: functional level, device level, circuit level and signal level. The key factors in these design strategies are the model, switch, current source calibration, glitch, mismatch shaping.

Designed DAC:

It is designed 4-bit current steering DAC Fig. [82] for proposed stimulation, as the main advantage to eliminate charge accumulation at output stage on stimulator or on electrode and the parasitic capacitance which is produced at output node. The switching scheme which is used to generate different input steps (0000-1111) is TG.the input waveforms are generated as mentioned before will be applied to gates of DAC transistor with level lower than threshold voltage to ensure operating in subthreshold region and to be allowable to generate raising and falling exponential stimulation current.

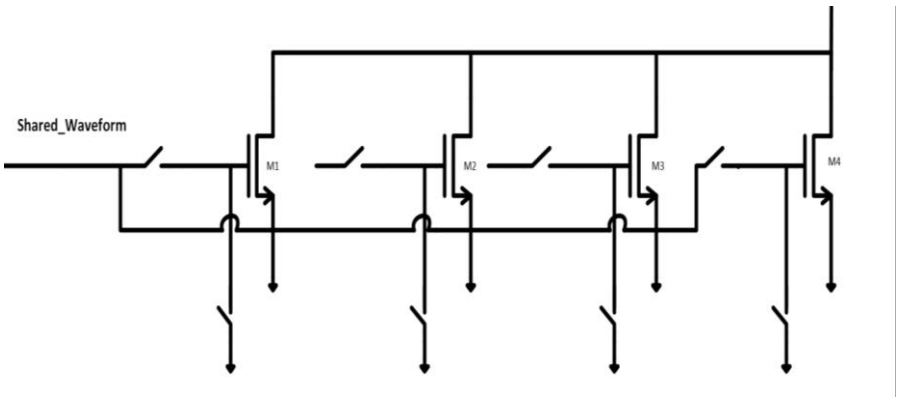

Figure 82: 4-bit current stimulation DAC

4.10 Output Stage (Stimulation stage)

4.10.1 Rising exponential current stimulation:

In CMOS technology, the rising exponential law is available only for the weak inversion operation of the MOS transistor. Note that, multiple circuits have been developed to perform rising exponential, but these circuits are just appropriate to be used in automatic gain controllers. The introduced stimulator circuit also includes a rising exponential current pulse generator designed based on the idea will be discussed. The adopted strategy is to use MOS transistor in weak inversion. By simply linearly varying Vgs and keeping it below the threshold voltage, a rising exponential current pulse is obtained. So, a voltage ramp generator is needed. A very simple approach to generate a ramp voltage is charging a capacitor by a constant current [27]. This will result of generating rising exponential pulses. The main transistor which is biased in weak inversion region has a Vth of almost 520mV. The dimensions of MOS are used in DAC and output stage are chosen to be large enough in order to decrease the process variation effects. Setting the amplitude of current pulses is done through the 4- bit current-steering DAC. the input current is amplified.to overcome this issue, a circuit is proposed in Fig. 10 in which the path of the stimulation current is placed in series with the load and no extra mirroring current is wasted. the gates of the binary weighted transistors (M1...M4) are connected or disconnected to the Ramp generator by the 4-bit gain control TG (TG1.TG4). For keeping (M1...M4) in the subthreshold region, VR Ramp must not exceed the threshold voltage which is about 520 mV for these transistors.

$$I_{stim} = A\, e^{\tau t}(u(t) - u(t - PW))$$

where A is the exponentials amplitude scaling parameter, the rising time constant, u(t) the step function and PW the pulse width.

so, the proposed rising current stimulation is given by the following equation:

$$I_{stim} = I_D[TG1 + 2TG2 + 4TG3 + 8TG4] * \frac{W}{L} * e^{\frac{V_{Ramp}}{nV_T}} * e^{\frac{I_c}{nV_T C}}[u(t) - u(t - PW)]$$

4.10.2 Falling exponential current stimulation

falling exponential stimuli generator is proposed to potentially optimize the energy efficiency while stimulating excitable cells in [ref]. The circuit is based on charging a capacitor with a transistor in series, which is biased in triode region The current is amplified by the current steering DAC. Although this approach results in a very good output impedance, it adds complexity, and power consumption to the circuit. The falling exponential waveform is produced by exploiting the transistors biased in the subthreshold region. For the falling exponential output current, V_{fall} becomes active, the gates of (M1..M4) are connected or disconnected to the V_{fall} which is expressed and shown in Fig.[83]. The initial value of V_{fall} must be set below the threshold voltage to ensure the (M1..M4) work in the subthreshold region. Hence, the falling exponential stimulation current can be given by the following equation:

$$I_{stim} = A\, e^{-\tau t}(u(t) - u(t - PW))$$

$$I_{stim} = I_D[TG1 + 2TG2 + 4TG3 + 8TG4] * \frac{W}{L} * e^{\frac{V_{fall}}{nV_T}} * e^{-(\frac{I_c}{nV_T C})}[u(t) - u(t - PW)]$$

4.10.3 Rectangle current stimulation

The output current waveform can be programmed into rectangular mode. The gate of transistors are V_{rect} switched to the or ground. If $V_{rect} < V_{th}$, then the stimulation current can be written as:

$$I_{stim} = I_D[TG1 + 2TG2 + 4TG3 + 8TG4] * \frac{W}{L} * e^{\frac{V_{rect}}{nV_T}}[u(t) - u(t - PW)]$$

4.10.4 Voltage to current Converter:

The gain booster part includes OTA and M5 which holds the negative feedback during the stimulation time. It performs two actions simultaneously; first, it sets the VD = 100 mV at the drain of (M1..M4) transistors to bias them in the subthreshold region in a way that the second term for in Eq.*** is negligible. Second, it boosts the output impedance of the stimulator by

$$R_{out} = A_{OTA} * g_{m5} * r_{05} * \frac{r_{o1}}{TG1} /\!/ \frac{r_{o2}}{TG2} /\!/ \frac{r_{o3}}{TG3} /\!/ \frac{r_{o4}}{TG4}$$

where A is the gain of OTA, gm5 is the trans-conductance of M5,ro5,M5 and (M1::M4) are the drain to source channel resistance of their corresponding transistors. OTA has the same topology as depicted in Fig. [67]. The stimulation current is applied to the tissue when electrode is active as shown in Fig. [83]. For the charge balancing, many charge balancing methods can be used here, however, for simplicity just short circuit technique is employed. During the non-stimulus phase, the load is shortened when reset is high, to deplete the charge that was remained in the previous stimulation phase [26].

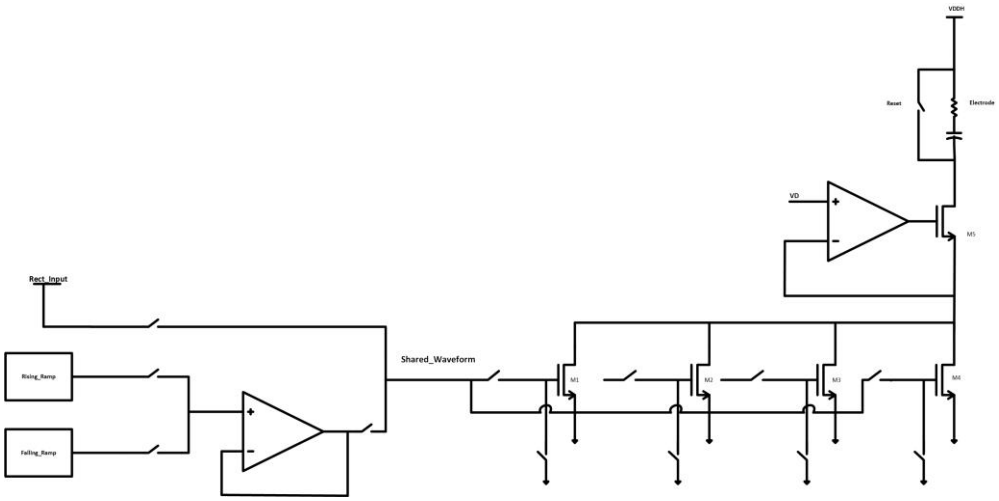

Figure 83: the proposed current stimulator output stage

The analog HV-switches in the output and the entire low voltage switches in the body of the proposed stimulator have transmission gate structure as discussed. Finally, the stimulation should be emphasized that the stimulation parameters such as amplitude, duration, and time constant (for exponential waveforms) are variable and can be altered as needed. In all modes of operation, the binary weighted transistors DAC assigns the 4-bit programmable amplitude of the output current. Also, the amplitude can be controlled by the Ramp in rising exponential, Vfall Ramp in falling exponential and Vrect in rectangular mode. Although primitive circuits were employed to provide the bias voltages needed in this Design.

4.11 Results

4.11.1 Simulation Results

Power calculation at VDDL=1.8 V

Table 4-2: measured power VDD=1.8

OTA	82.53 * 2 nW
Input OTA	9.918 *10^-13 W
Rising Ramp	2.8304 nW
Falling Ramp	5.9763 nW
Rect	7.69675 nW
Biasing	1.5356 * 10^-21 W
Total DC Power Consumption	181.564 nW

-Simulations:

DC power =12.37 µW for single input waveform

DC power=35.392 µW for multi-waveform

Dynamic power=75.16 µW @ 10KHz

Power calculation VDDL=1.2V

Table 4-3: measured Power VDD=1.2V

OTA	22.53 * 2 nW
Input OTA	7.216 *10^-13 W
Rising Ramp	2.75 nW
Falling Ramp	4.47 nW
Rect	4.4325 nW
Total DC Power Consumption	56.459 nW

- Simulations:

DC power =13.5 µW multi input waveform

DC power= 7.35 µW single input waveform

Dynamic power= 49.47 µW @ 10KHz

Table 4-3: Comparison Study

Specifications	Reference ***	This work
Static Power	23.3 µW	12.37 µW(static) 75.16 µW(Dynamic)
Area	NA	140.35 µm *112.025 µm
Efficiency	94.7 %	96.47 %
Capacitance	Ones of pF	1 pF
Rising offset	100 mV>>>400 mV	160 mV @ 1 mA
Falling offset	525 mV>>>350 mV	425 mV @ 1 mA
Rectangle	200 mV>>>525 mV	330 mV @ 1 mA

VDD	1.8V - 3.3V	1.2V - 1.8V - 3.3V
Technology	180n CMOS	Umc 130um CMOS
Frequency of Operation	7.936KHz>>>76.92 KHz	10KHz

The reduction in static power Consumption affected by reduction in number of OTAs, the dynamic power affected by capacitance and operated frequency as if we increase the frequency the dynamic power will increase and it is not necessary to increase frequency in our design.

Dynamic Power parametric study:

Table 4-4:Dynamic Power parametric study

Frequency	Power
20KHz	94.49 µW
15KHz	76.81 µW
12.5KHz	70.78 µW
10KHz	75.16 µW
9KHz	54.76 µW
7.93KHz	52.77 µW

Stimulation Current:

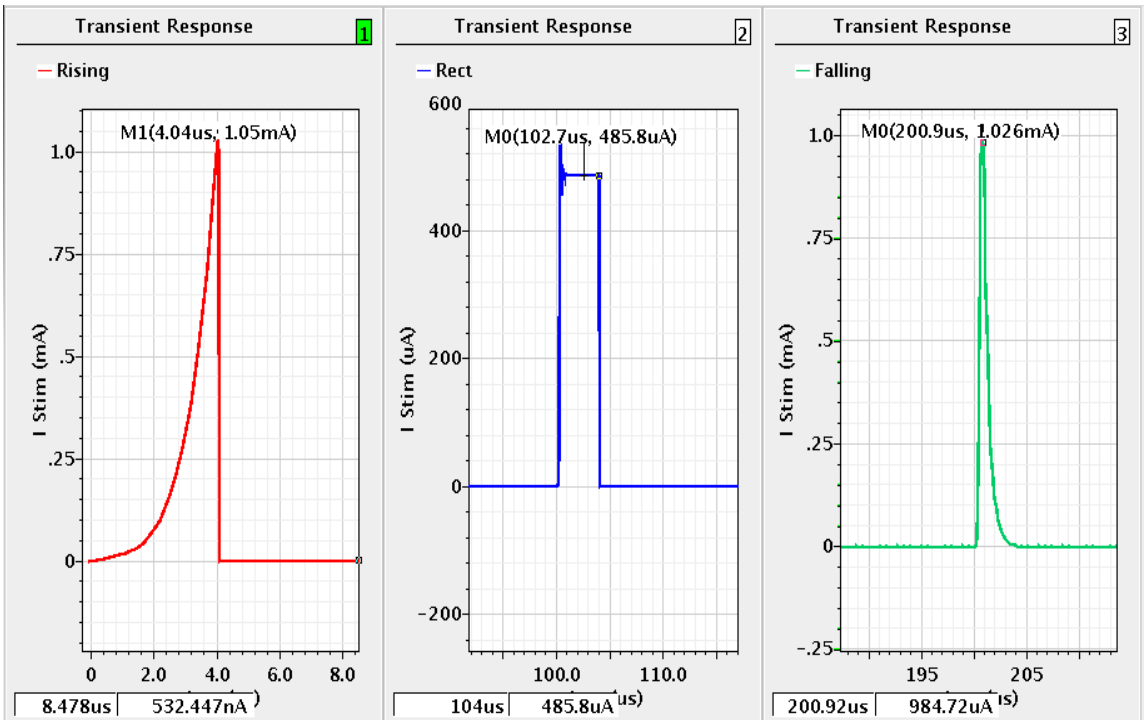

Figure 84: Output Stimulation Current

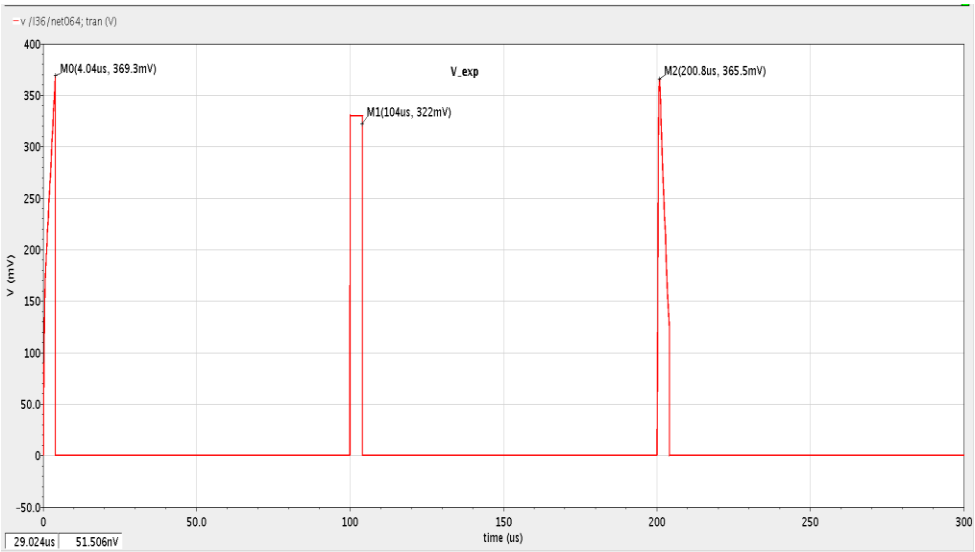

Figure 85: Switching signal

The above figure showing the reverse signal from DAC during the off phase, the stimulation will save current till electrode reset as the charge accumulation can't occur, the reset signal is simple method to prevent charge accumulation.

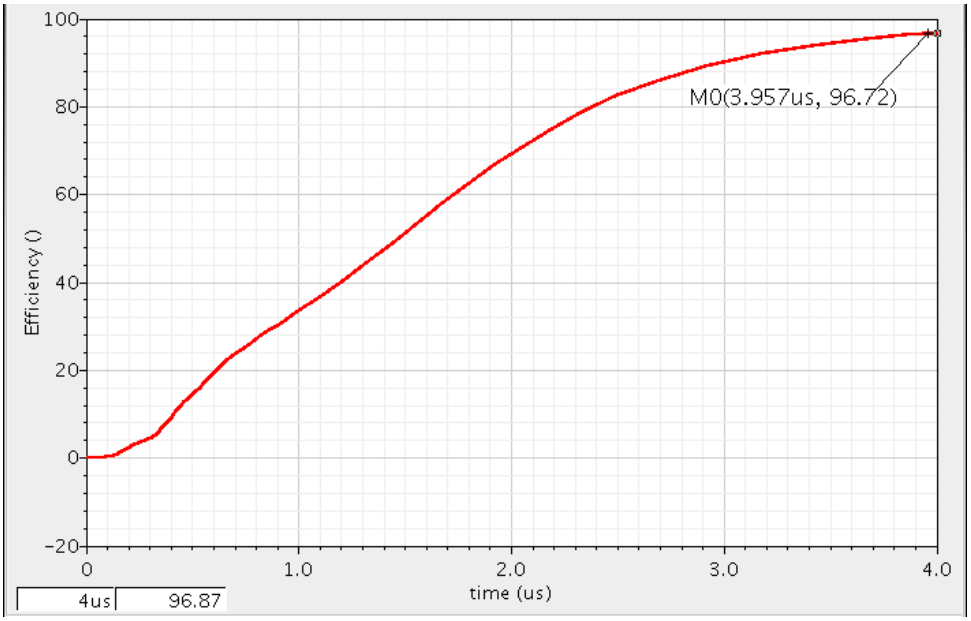

Figure 86: Efficiency

The model of calculation efficiency Fig. [86] is assuming single waveform applied and the highest efficiency occur at high stimulation current due to reduction in static power the efficiency increase, the pulse width of stimulation duration enables us to get high compliance voltage at electrode as gain boosting topology of current stimulation was used as high compliance voltage is main specs in current stimulation.

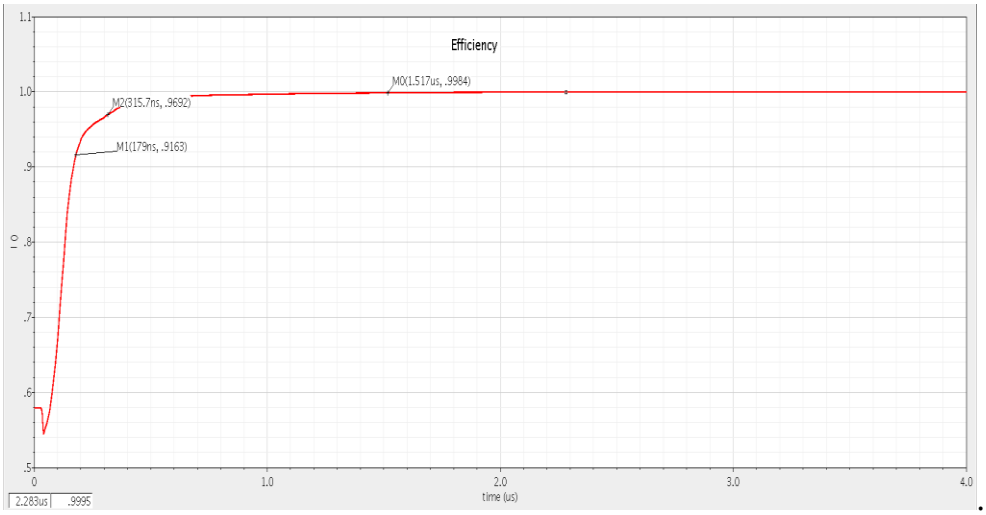

Figure 87: efficiency measurement

Variation in applied offset voltage can change amplitude of current stimulation but the main constrain is offset voltage can't exceed threshold voltage of Transistors to maintain them in subthreshold.

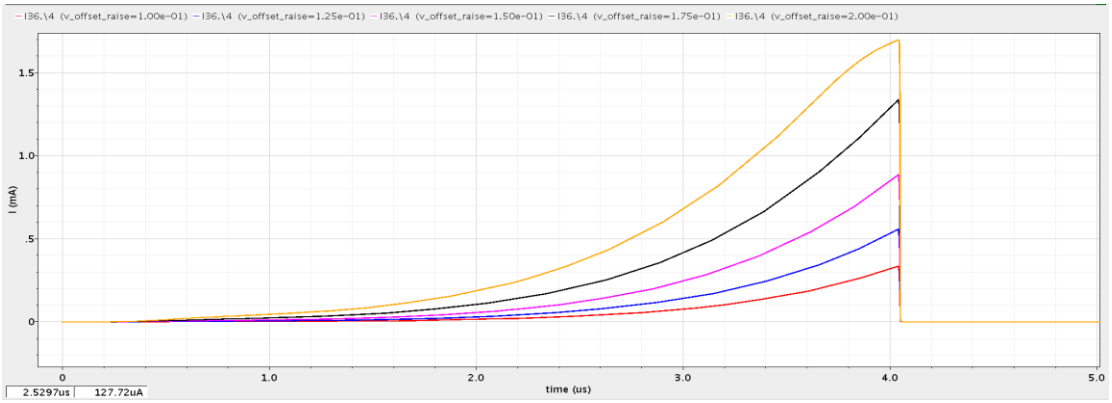

Figure 88: Varying offset voltage Rising

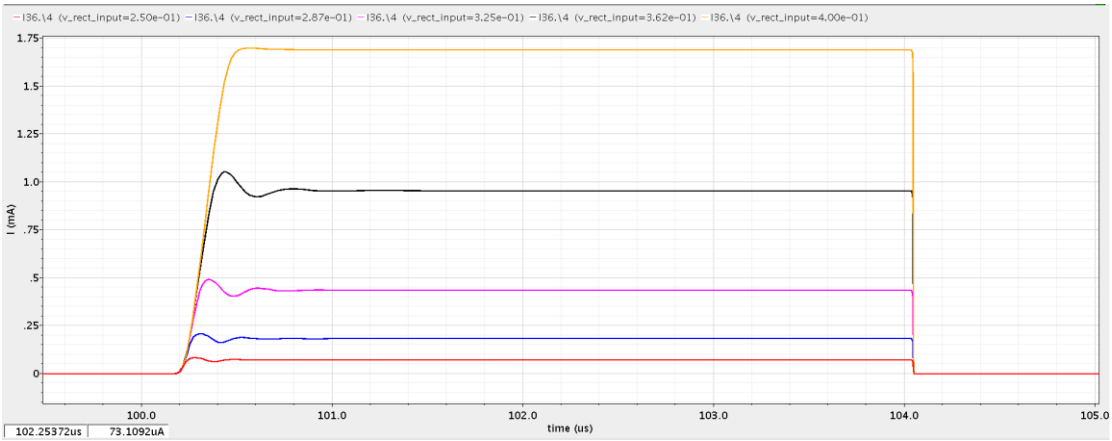

Figure 89: Varying offset voltage Rect

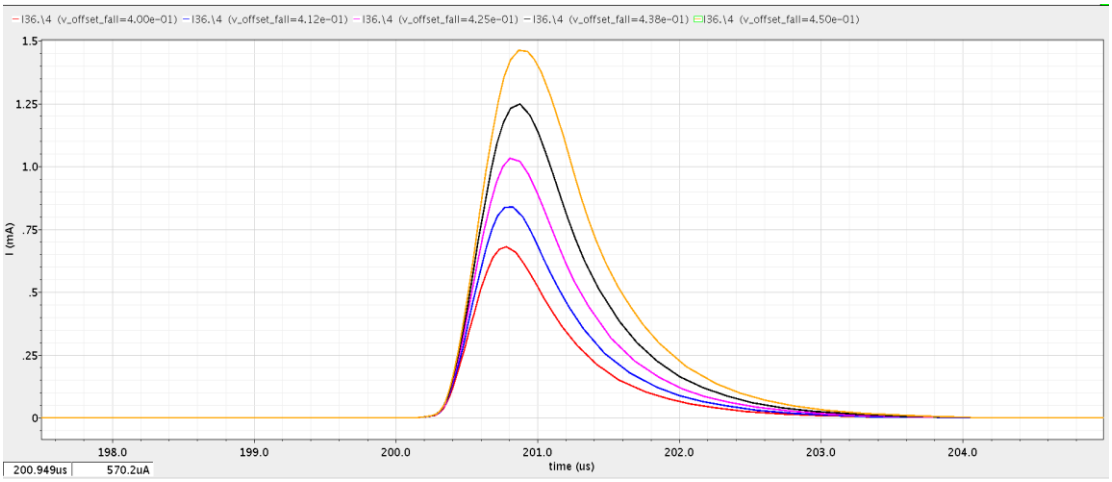

Figure 90: Varying offset voltage falling

Simulation results VDD=1.2V: we tried to make our design multi supply voltage the parametric study was done to ensure ability of design to maintain safe and efficient in different supply voltage.

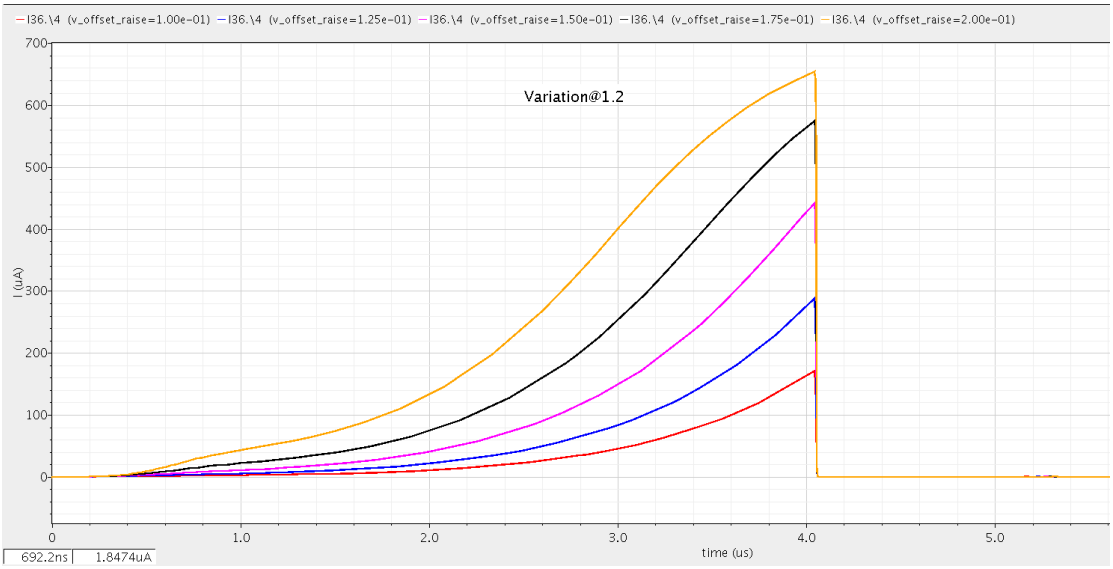

Figure 91: Output Current Stimulation VDDL= 1.2 V

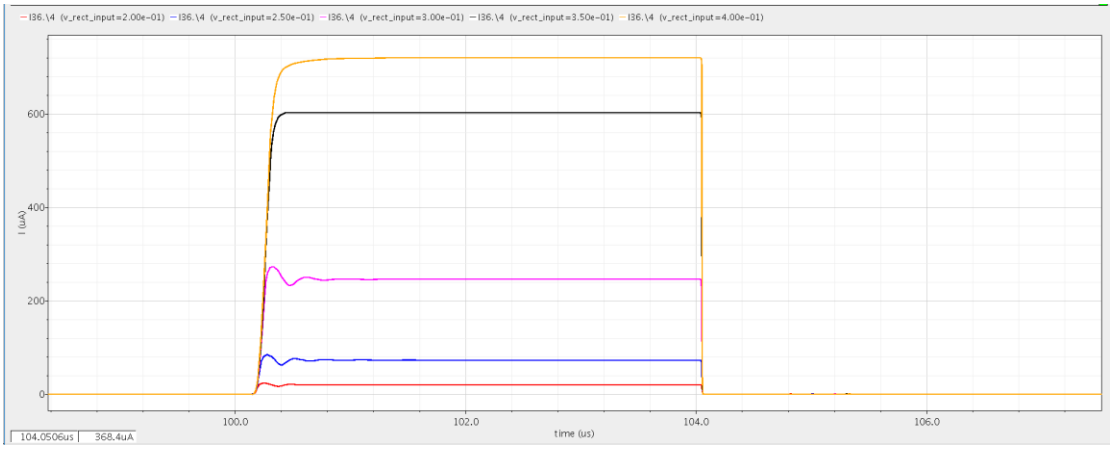

Figure 92:Output Current Stimulation VDDL=1.2V

4.11.2 Process Variation

The subthreshold region is highly sensitive to variation and mismatch as mentioned before, the following Parametric analysis shown the different corner technology design for different transistors types, supply voltage variation and temperature.

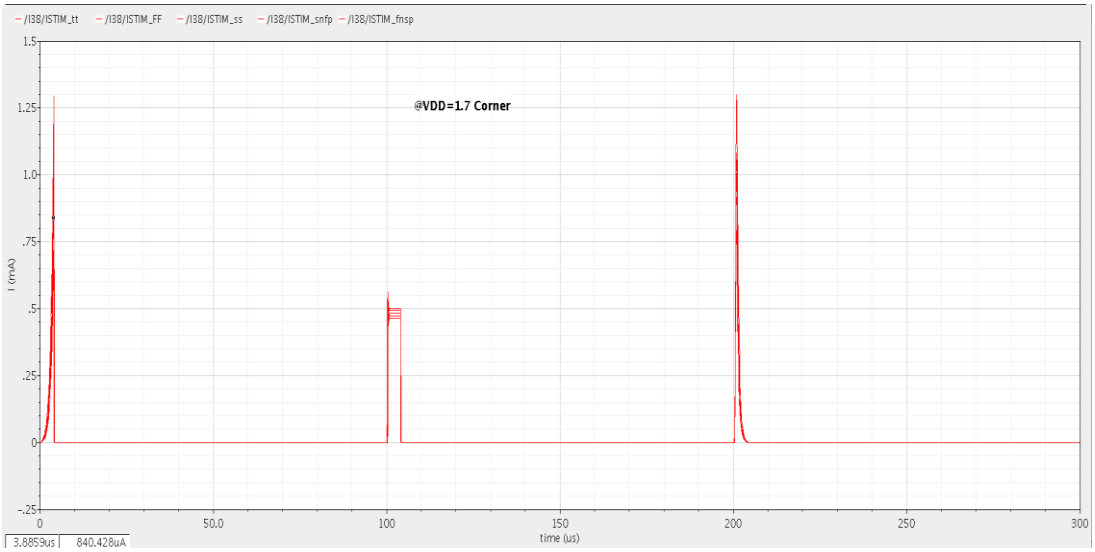

Figure 93: HG-Transistor Different Corners VDD=1.7 V (Total)

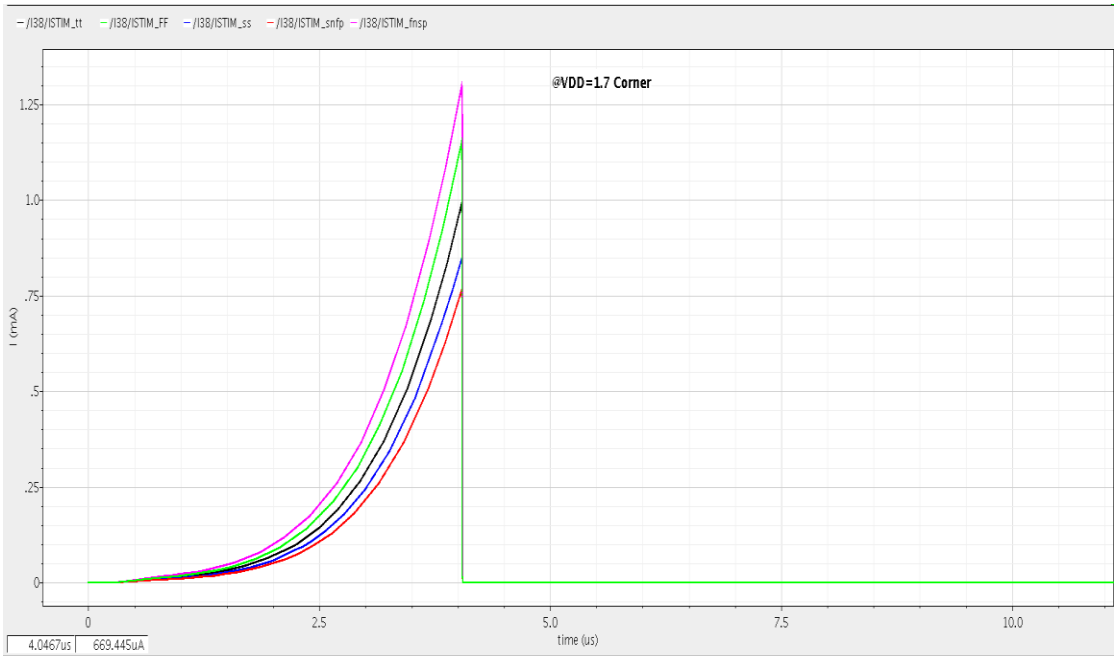

Figure 94: HG-Transistor Different Corners VDD=1.7 V (Rise)

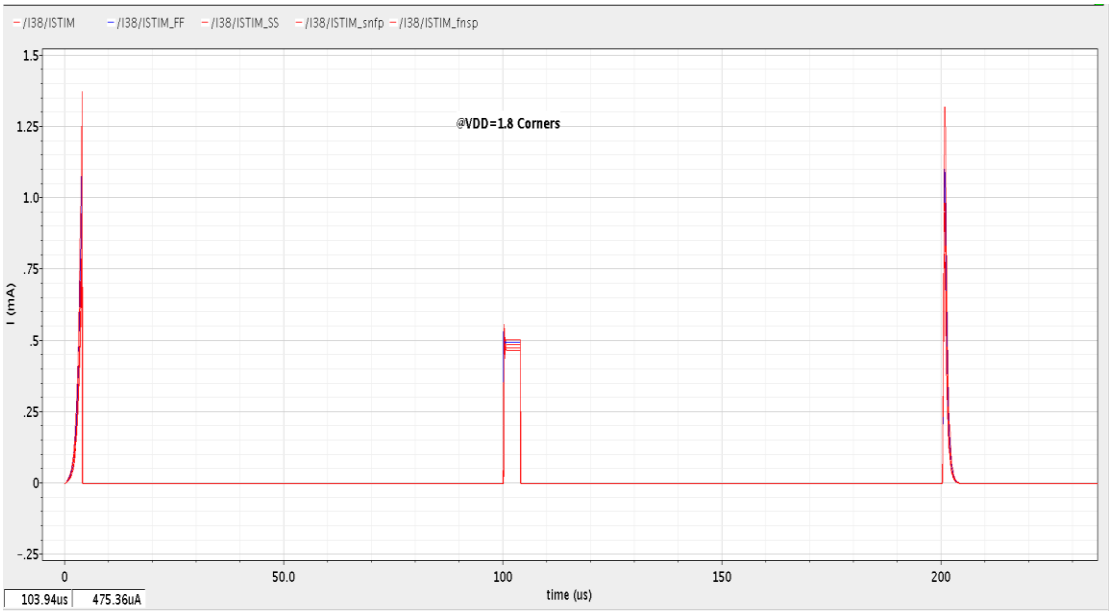

Figure 95: HG-Transistor Different Corners VDD=1.8 V (Total)

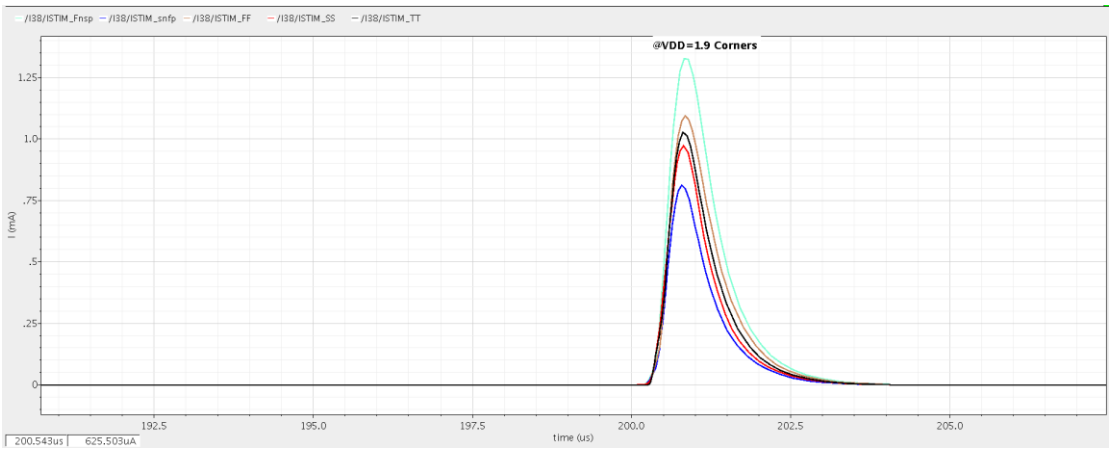

Figure 96: HG-Transistor Different Corners VDD=1.9 V (falling)

Figure 97: HG-Transistor Different Corners VDD=1.9 V (Rect)

Temperature Variation:

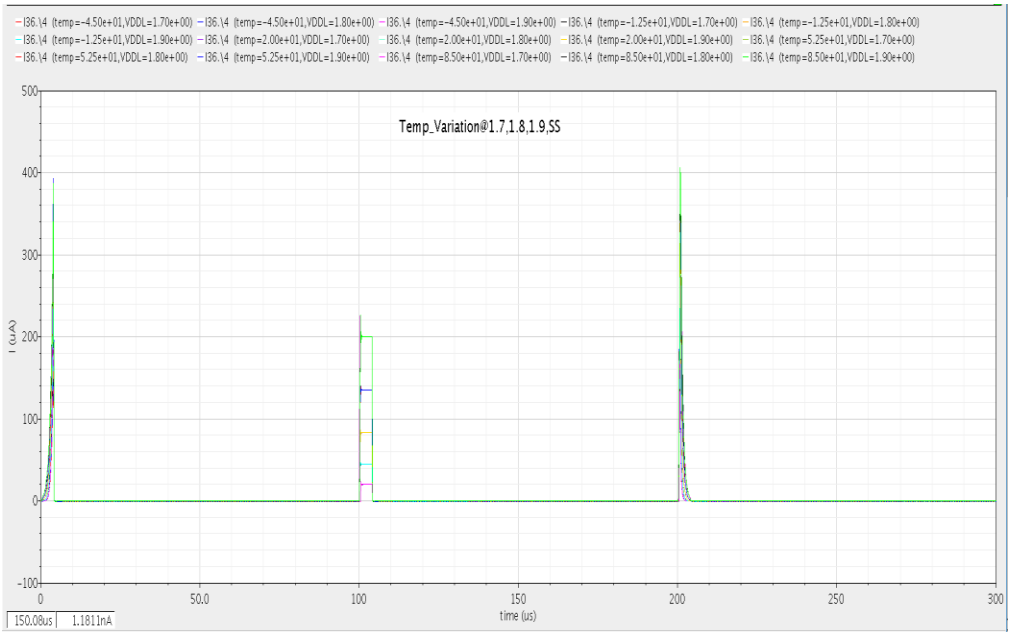

Figure 98: HS-Transistor Temperature & SS VDD=1.9,1.8,1.7 V (Total)

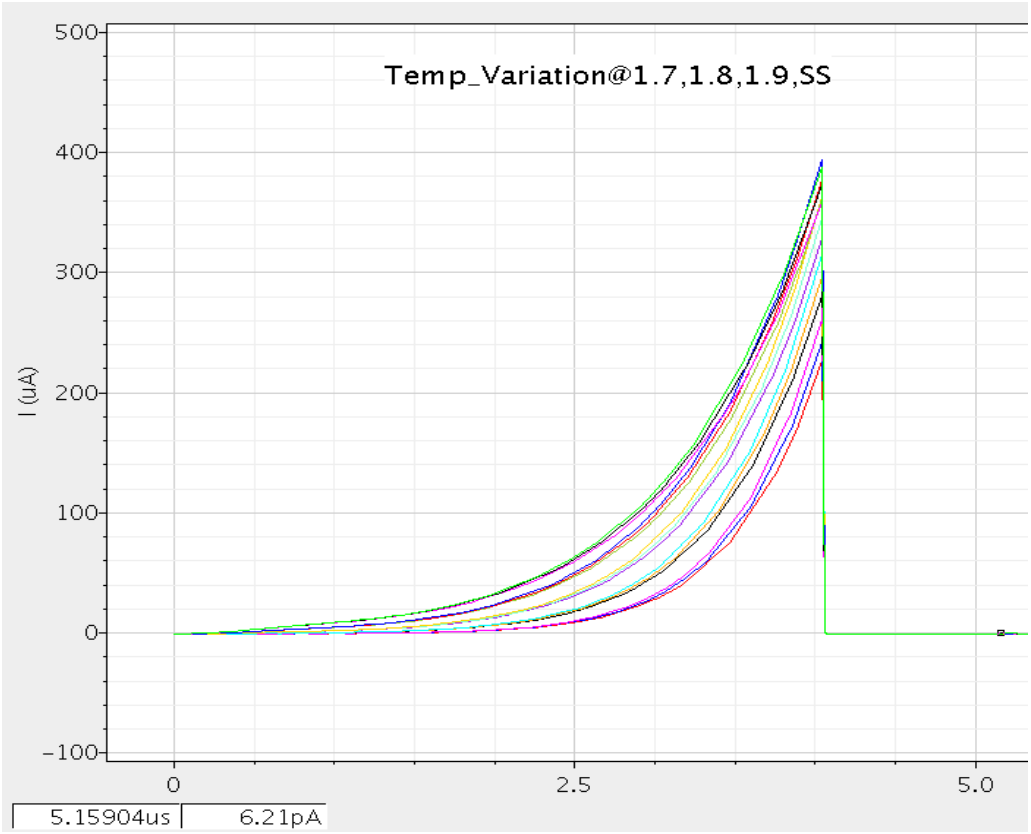

Figure 99: HS-Transistor Temperature & SS VDD=1.9,1.8,1.7 V (Rise)

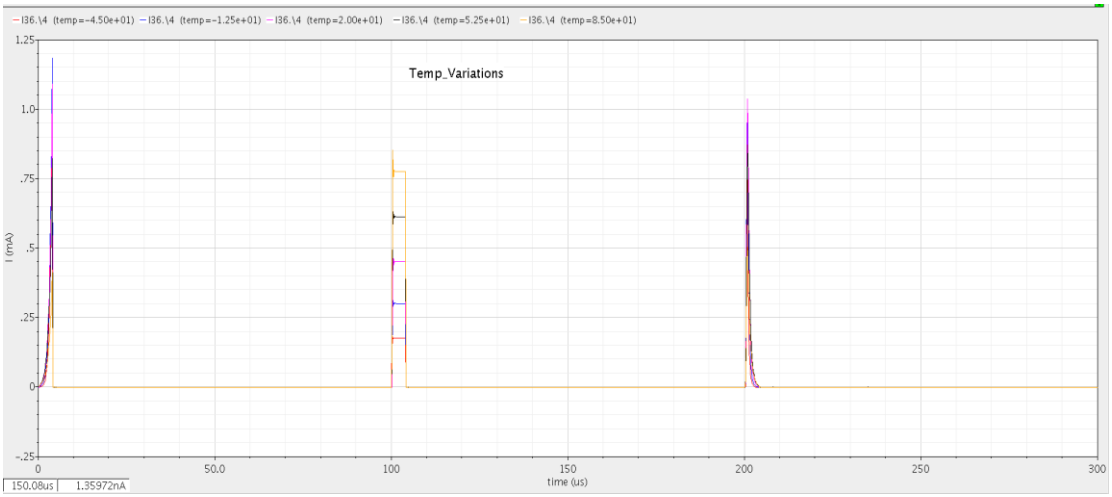

Figure 100: HS-Transistor Temperature & TT VDD=1.8V (Total)

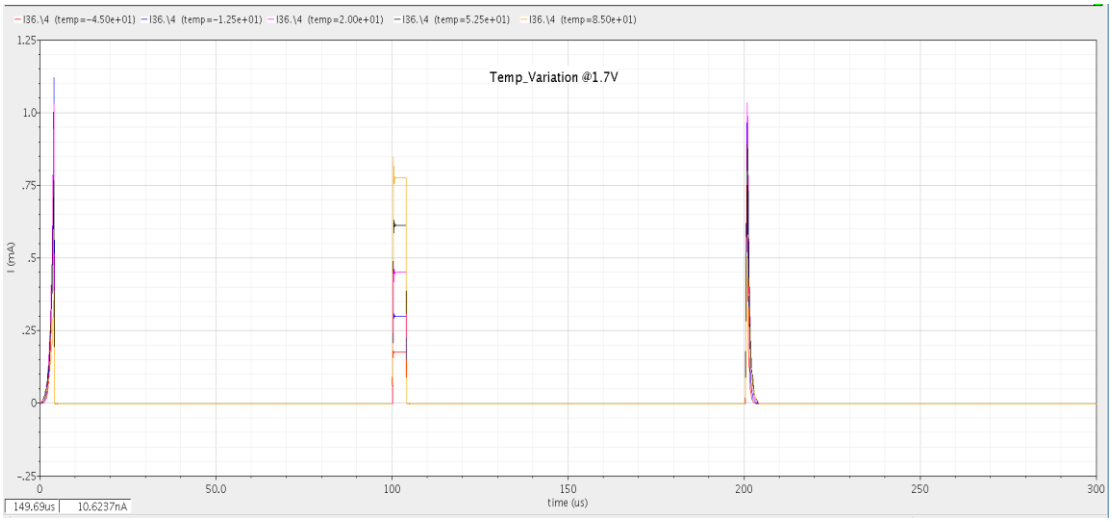

Figure 101: HS-Transistor Temperature & FF VDD=1.7V (Total)

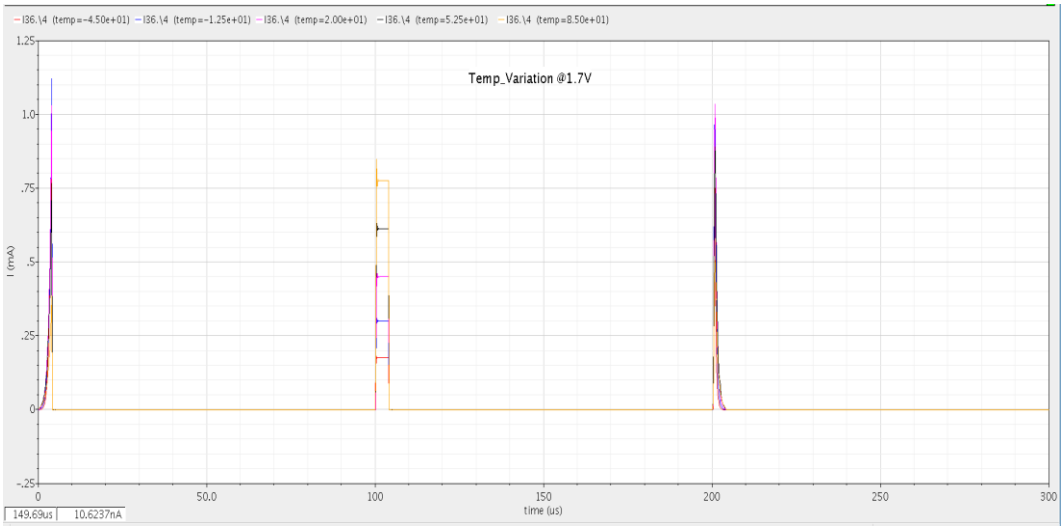

Figure 102:HS-Transistor Temperature & TT VDD=1.7V (Total)

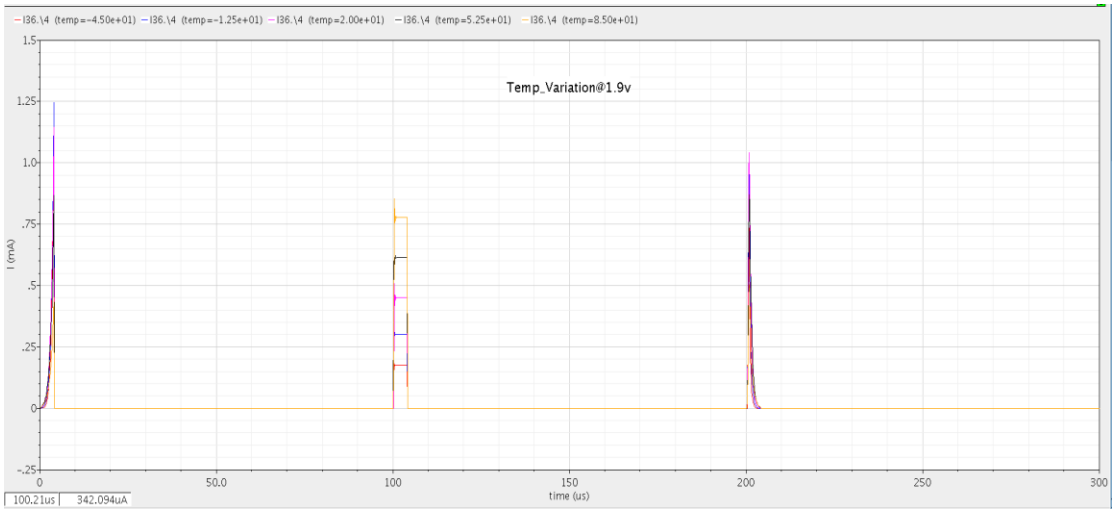

Figure 103: HS-Transistor Temperature & TT VDD=1.9V (Total)

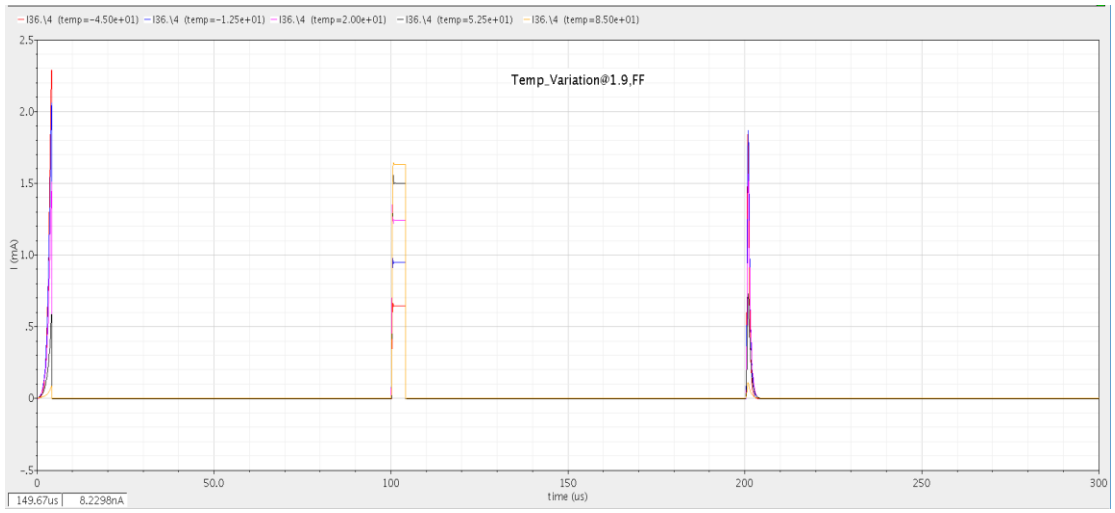

Figure 104: HS-Transistor Temperature & FF VDD=1.9V (Total)

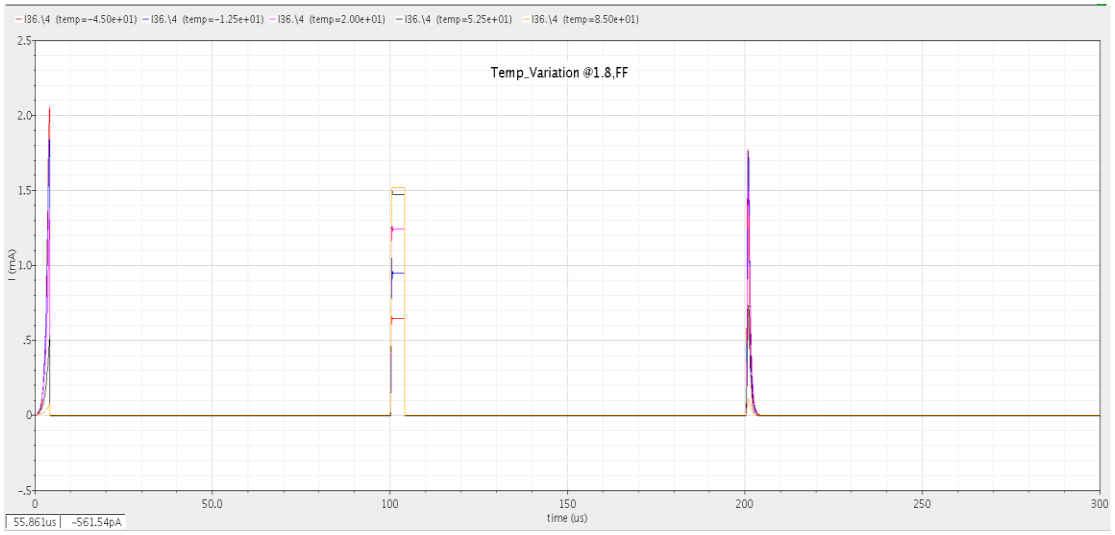

Figure 105: HS-Transistor Temperature & FF VDD=1.8V (Total)

Electrode Parametric analysis:

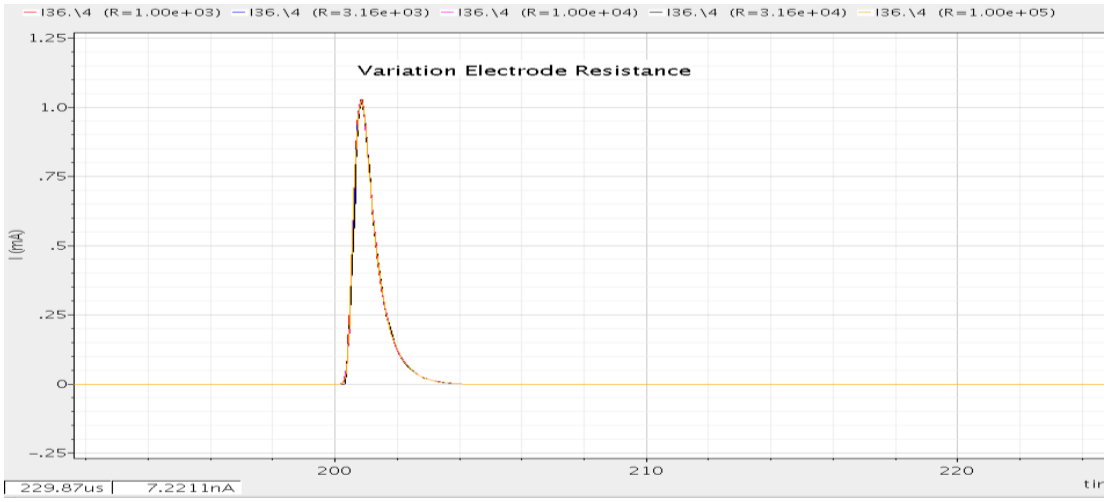

Figure 106: Electrode Resistance Variation 1K>>100K

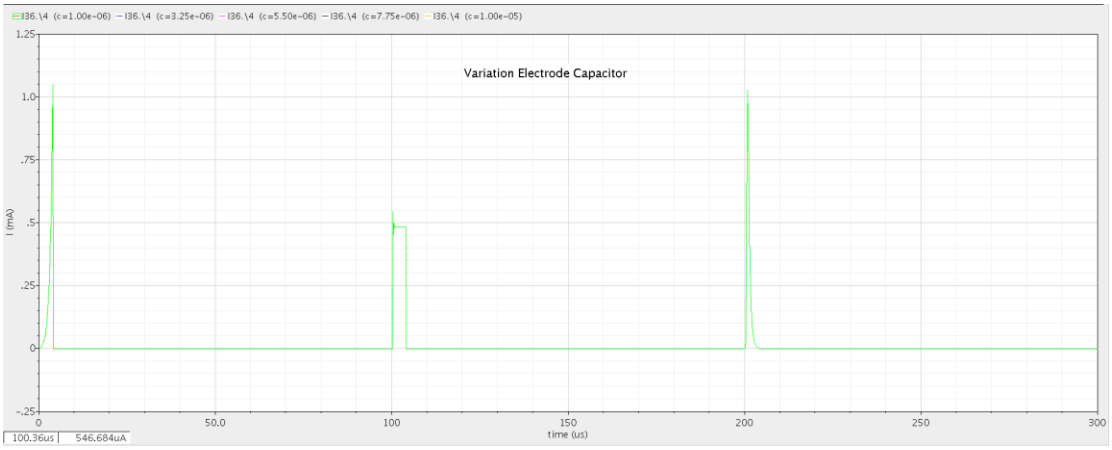

Figure 107: Electrode Capacitor Variation 1uF>>10uF

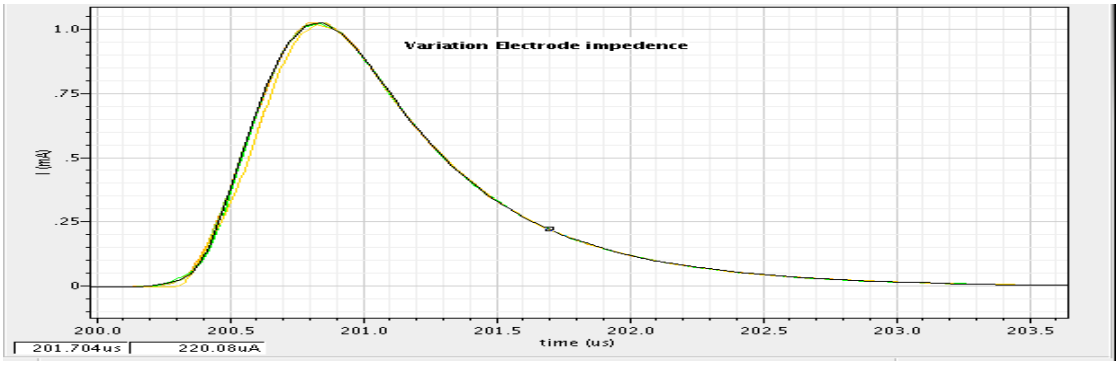

Figure 108: Electrode Capacitor Variation 1uF>>10uF

4.12 Layout

The post layout simulation was illustrated in this section shown basic technique used such as common centroid and interdigitated, the Area of layout for Design II is measured to be 140.35 µm *112.025 µm the next figure Fig [109] shown floorplan.

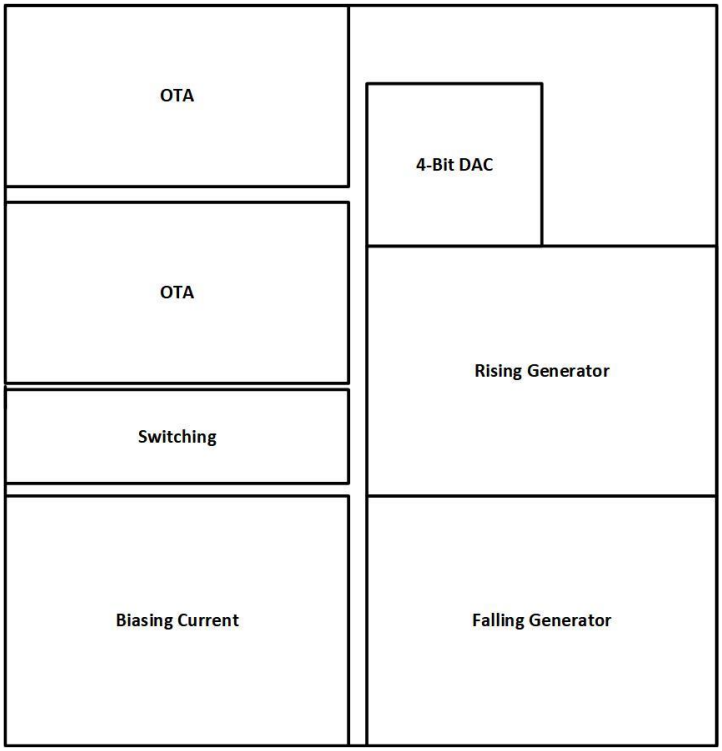

Figure 109: proposed floorplan Design II

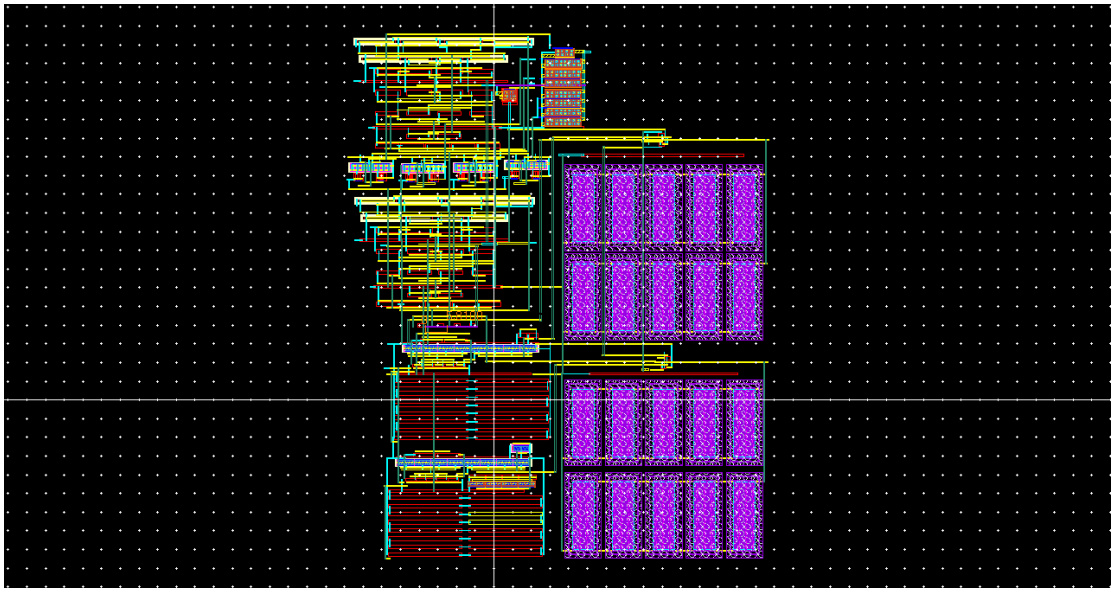

Figure 110: Layout schematic Design II

The amplitude of current stimulation was reduced after post layout simulation and we need to pay more offset voltage and biasing to get the same current which we got in first simulations.it is noticeable that time constant of rising ramp became more sluggish due to parasitic capacitance the following figures shown us variation at supply voltage 1.8.

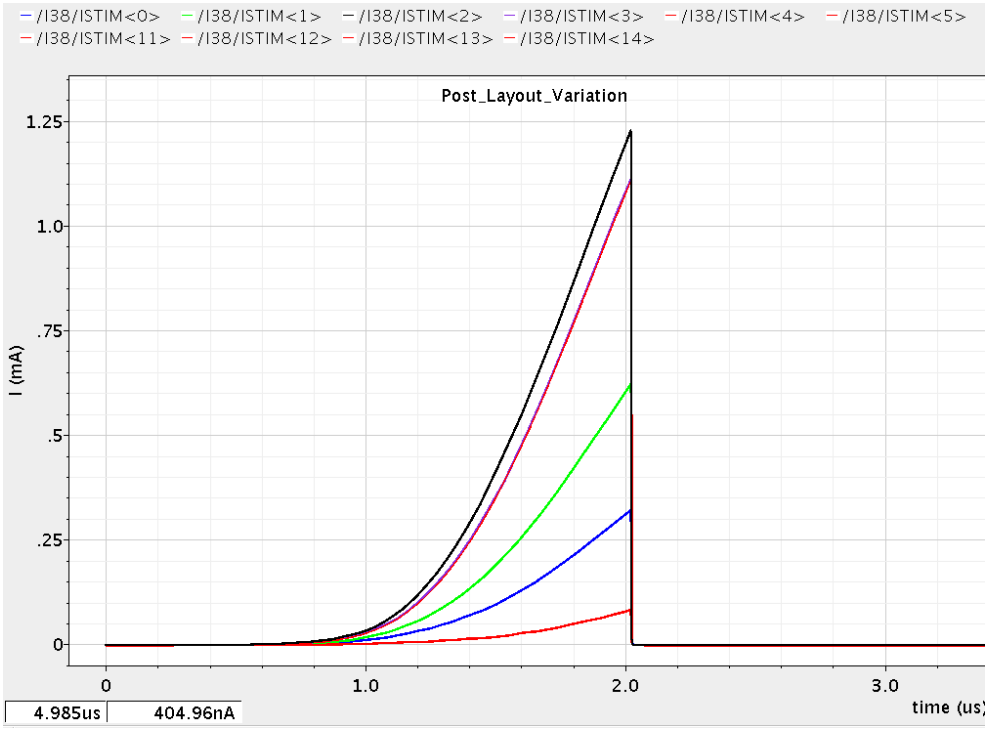

Figure 111: Post Layout Simulation rising Ramp

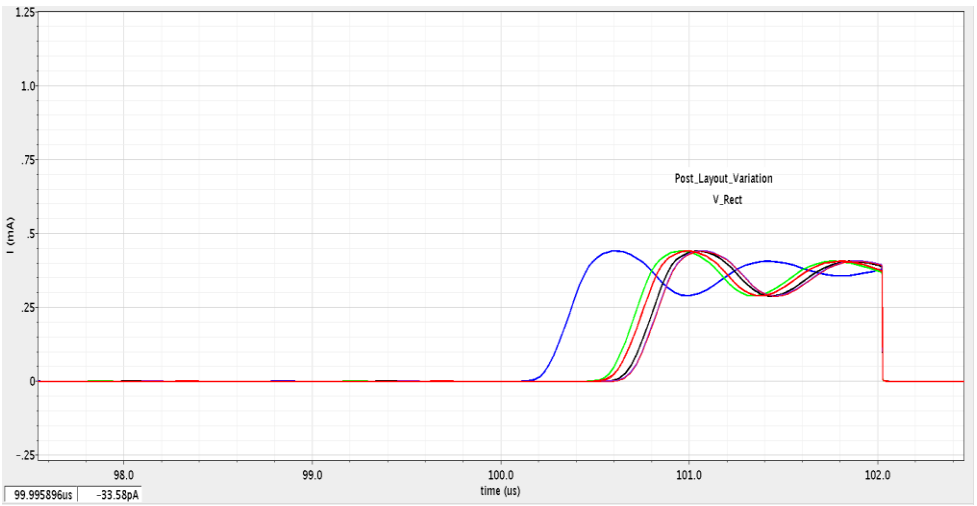

Figure 112:Post Layout Simulation Rect

Figure 67 is showing that increasing the ripples in rectangle current stimulation we can estimate this due to reduction occurrence of phase margin at OTA. Using of MOM capacitor reduced area and parasitic capacitance.

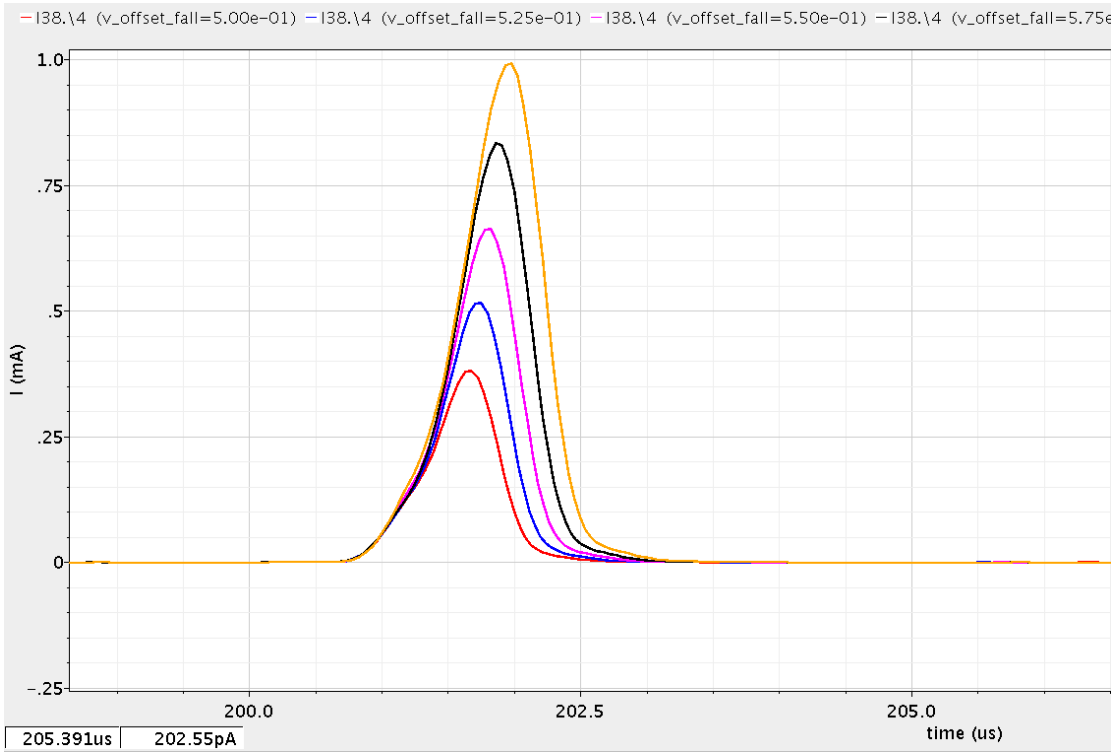

Figure 113: Post Layout Simulation Falling Ramp

Parametric study supply voltage 1.2 V the amplitudes of current became smaller after running PEX simulations with changing supply voltage to 1.2 V the main issue is the parasitic and highly appearance of mismatching.

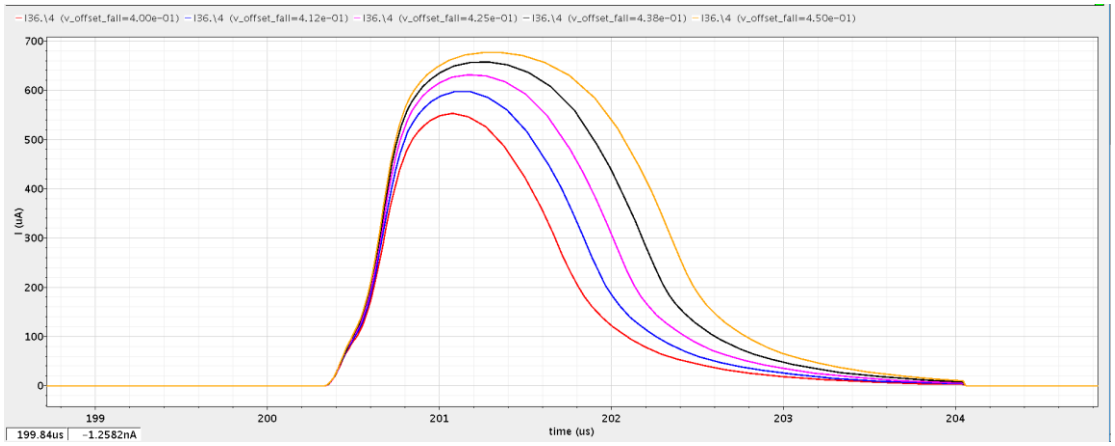

Figure 114: Post Layout simulation at 1.2V

Chapter 5: Conclusion and future recommendations

After going through Designing, simulations and post-layout simulations of two different implementations of a neural stimulation. We can say that it is very useful to implement the stimulators after merging the charge pump control circuit without any ideal component in Design I and doing the tape out preparations and simulations.

Some future recommendations regarding design I:

- Using of triple well technology was avoided twice and another technique were used instead, once in the charge pump and the second time was in the output driver. So if it'll be possible for someone to do the transistors using triple well technology it may give him better results, but it will consume more area and effort form him.
- Charge pump design is very efficient especially with low voltage applications such as MEMS devices if we are able to use low threshold MOSFETS
- Pre-driver design is changeable as long as it does its job in making the output driver able to sustain high voltage from the charge pump. So, you may find another one which is more power efficient and self-switching between anodic and Cathodic modes without the need of outside switches

References

Below are some examples of citations following the IEEE standard:

[1] J. Simpson and M. Ghovanloo, "An Experimental Study of Voltage, Current, and Charge Controlled Stimulation Front-End Circuitry," 2007 IEEE International Symposium on Circuits and Systems, New Orleans, LA, 2007, pp. 325-328.R. G. Arns, ”The other transistors: early history of the metal-oxide semiconductor field-effect

[2] V.K.Khanna1,“NeuralStimulationandChargeBalancingApproaches,”Implantable Medical Electronics pp 81-107.

[3] C. Lin and M. Ker, “Overview of on-Chip Stimulator Designs for Biomedical Applications,”Journal of Neuroscience and Neuroengineering (JNSNE),Aug. 2012

[4] M. Kuriyama, S. Atsumi, A. Umezawa, H. Banba, K.-I. Imamiyu, K.Naruke, S. Yamada, E. Obi, M. Oshikiri, T. Suzuki, M. Wada, and S.Tanaka, “A 5 V-only 0.6 m flash EEPROM with row decoder schemein triple-well structure,” in IEEE Int. Solid-State Circuit Conf. Dig.Tech. Papers, 1992, pp. 152–153

[5] T. Kawahara, T. Kobayashi, Y. Jyouno, S.-I. Saeki, N. Miyamoto, T. Adachi, M. Kato, A. Sato, J. Yugami, H. Kume, and K. Kimura, “Bitline clamped sensing multiplex and accurate high voltage generator for quarter-micron flash memories,” IEEE J. Solid-State Circuits, vol. 31, pp. 1590–1600, Nov. 1996.

[6] T. B. Cho and P. R. Gray, “A 10 b, 20 M sample/s, 35 mW pipeline A/D converter,” IEEE J. Solid-State Circuits, vol. 30, pp. 166–172, Mar. 1995

[7] R. S. Pierre, “Low-power BiCMOS op-amp with integrated current-mode charge pump,” IEEE J. Solid-State Circuits, vol. 35, pp. 1046–1050, Jul. 2000.

[8] S. Abdelaziz, A Low Voltage Start-Up Charge Pump for Energy Harvesting Applications. MSc thesis, Cairo University, 2012.

[9] M.-D. Ker et. al., “Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage CMOS processes,” IEEE J. Solid-State Circuits, vol. 41, no. 5, pp. 1100-1107, May 2006

[10] J.-T. Wu and K.-L. Chang, “MOS charge pump for low-voltage operation,” IEEE J. Solid-State Circuits, vol. 33, pp. 592–597, Apr. 1998.32

[11] W. L. Chen, C. Y. Lin and M. D. Ker, "Design of stimulus driver to suppress epileptic seizure with adaptive loading consideration," 2010 International Symposium on Next Generation Electronics, Kaohsiung, 2010, pp. 9-12.

[12] C. Y. Lin, W. L. Chen and M. D. Ker, "Implantable Stimulator for Epileptic Seizure Suppression With Loading Impedance Adaptability," in IEEE Transactions on Biomedical Circuits and Systems, vol. 7, no. 2, pp. 196-203, April 2013.

[13] K. Bult, “Analog broadband communication circuits in pure digital deep sub-micron CMOS,” in *Dig. Tech. Papers Int. Solid-State Circuits Conf.*, 1999, pp. 76–77 7 in 32

[14] M. Takahashi, T. Sakurai, K. Sawada, K. Nogami, M. Ichnida, and K. Matsuda, “3.3 V–5 V compatible I/O circuit without thick gate oxide,” in *Proc. Custom Integrated Circuits Conf.*, 1992, pp. 23.3.1–23.3.4

[15] M. Hargrove, S. Crowder, E. Nowak, R. Logan, L. K. Han, H. Ng, A. Ray, D. Sinitsky, P. Smeys, F. Guarin, J. Oberschmidt, E. Crabbé, D. Yee, and L. Su, “High-performance sub-0.08 m CMOS with dual gate oxide and 9.7 ps inverter delay,” in Proc. Int. Electron Devices Meeting, 1998, pp. 22.4.1–22.4.4.

[16] C. Hu, “Gate oxide scaling limits and projection,” in Proc. Int. Electron Devices Meeting, 1996, pp. 319–322.3 in 32

[17] R. Woltjer and G. Paulzen, “Universal description of hot-carrier-induced interface states in nMOSFETs,” in *Proc. Int. Electon Devices Meeting*, 1992, pp. 535–538.

[18] B. Serneels, M. Steyaert, and W. Dehaene, “A 237 mW aDSL2 CO line driver in standard 1.2 V 0.13 m CMOS,” in Proc. IEEE Int. SolidState Circuits Conf. Dig. Tech. Papers, Feb. 2007, pp. 524–526

[19] Z. Luo and M. D. Ker, "A High-Voltage-Tolerant and Precise Charge-Balanced Neuro-Stimulator in Low Voltage CMOS Process," in IEEE Transactions on Biomedical Circuits and Systems, vol. 10, no. 6, pp. 1087-1099, Dec. 2016.

[20] Y. Tsividis, Operation and Modeling of the MOS Transistors, McGraw-Hill, 1999.

[21] R. G. Arns," The other transistors: early history of the metal-oxide semiconductor field-effect transistor," in IEEE Engineering Science and Education J., vol. 7, no. 5, pp. 233-240, Oct. 1998.

[22] B. Sheu and C. Hu, "Switch-induced error voltage on a switched capacitor." IEEE Journal of Solid-State Circuits, vol. SC-19, no. 4, pp. 519–525, 1984.

[23] H. S. Raghav, B. P. Singh and S. Maheshwari, "Design of low voltage OTA for bio-medical application," 2013 Annual International Conference on Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy, Kanjirapally, 2013, pp. 1-5.

[24] L. F. Rahman, F. A. Rudham, M. B. I. Reaz and M. Marufuzzaman, "The evolution of digital to analog converter," 2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES), Putrajaya, 2016, pp. 151-154.

[25] X. Liu et al., "A 16-channel 24-V 1.8-mA power efficiency enhanced neural/muscular stimulator with exponentially decaying stimulation current," 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, 2015, pp. 2992-2995.

[26] F. Mooziraji,O. Shoaei, "A high power efficient multi-waveform current stimulator used in implantable neural stimulation," Analog Integrated Circuits and Signal Processing, pp.459–469, Jan. 2016.

[27] A. Wongsarnpigoon, W. M Grill, "Energy-Efficient Waveform Shapes for Neural Stimulation Revealed with a Genetic Algorithm," J. of Neural Eng., Vol. 7 No. 4, 2010.

[28] J. Simpson, M. Ghovanloo, "An Experimental Study of Voltage, Current, and Charge Controlled Stimulation Front-End Circuitry," IEEE ISCAS, pp.325–328, May 2007.

[29] R. Cubo, A. Medvedev and H. Andersson, "Deep Brain Stimulation therapies: A control-engineering perspective," 2017 American Control Conference (ACC), Seattle, WA, USA, 2017, pp. 104-109.

[30] P. F. Diez, V. Mut, E. Laciar and E. Avila, "A comparison of monopolar and bipolar EEG recordings for SSVEP detection," 2010 Annual International Conference of the IEEE Engineering in Medicine and Biology, Buenos Aires, 2010, pp. 5803-5806.

[31] W. M. Chen et al., "A Fully Integrated 8-Channel Closed-Loop Neural-Prosthetic CMOS SoC for Real-Time Epileptic Seizure Control," in IEEE Journal of Solid-State Circuits, vol. 49, no. 1, pp. 232-247, Jan. 2014.

[32] James J. Pastoriza, "Solid State Digital-to-Analog Converter," U.S. Patent 3,747,088, filed December 30, 1970, issued July 17, 1973. (the first patent on the quad switch approach to building high resolution DACs).