CAIRO UNIVERSITY

GRADUATION PROJECT THESIS

Layout Design Automation

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Abstract

Analog layout automation is the pivot of modern Integrated Circuit (IC) industry to decrease time-to-market that helps to enhance the investment specially in advanced node technology. One of the most critical points that threatens the high node technology is the interconnect delay that becomes dominant of the gate delay.

Another problem that threatens the high node technology is that due to reduction of minimum spacing between the routes, crosstalk is more likely to occur on critical signals which results in distortion for the critical signals and may cause malfunction for the whole IC.

In this thesis we could control the parameters of the routes for critical signal (width, Metal layer (MX)) to get better delay to get the optimum available parameters to decrease the interconnect delay replacing the old interconnect with the proposed interconnect.

To improve the circuit performance, we should avoid any coupling capacitance from aggressive neighbors (High speed and High switching power circuits) that can cause crosstalk and malfunction for the circuit.

In this thesis we could add shielding with suitable type to protect the interconnect from any crosstalk.

To achieve high yield, the fab puts some rules to guarantee well fabricated chips that called design rule checks (DRCs). One of them is density rule to protect metals through chemical mechanical polishing (CMP), etching and chemical vapor deposition (CVD). So, we need generic runsets to fill in the layout to achieve the required density, but they have some problems when dealing with critical nets, highly symmetric blocks or filling with decoupling caps.
In this thesis we could consider all these issues automatically that saves time and cost with easy interface

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List of Abbreviations

BE	**B**ack **E**nd
BJT	**B**ipolar **J**unction **T**ransistor
CMP	**C**hemical **M**echanical **P**olishing
CVD	**C**hemical **V**apor **D**eposition
DRC	**D**esign **R**ule **C**heck
EDA	**E**lectronic **D**esign **A**utomation
ESD	**E**lectro-**S**tatic **D**ischarcge
FE	**F**ront **E**nd
GUI	**G**raphical **U**ser **I**nterface
GND	**G**round
IC	**I**ntegrated **C**ircuit
LOD	**L**ength Of **D**iffusion
LPE	**L**ayout **P**arasitic **E**xtraction
LVS	**L**ayout **V**ersus **S**chematic
MIM	**M**etal-**I**nsulator-**M**etal
MOM	**M**etal-**O**xide-**M**etal
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect-**T**ransistor
PCB	**P**rinted **C**ircuit **B**oard
PIP	**P**oly-**I**nsulator-**P**oly
QoR	**Q**uality **o**f **R**esults
R&D	**R**esearch **& D**evelopment
SADP	**S**elf-**A**ligned **D**ouble **P**atterning
SCR	**S**ilicon-**C**ontrolled **R**ectifier
STI	**S**hallow **T**rench **I**solation
TCL	**T**ool **C**ommand **L**anguage
TNS	**T**otal **Ne**gative **S**lack
Vac	**V**oltage of **A**lternative **C**urrent
Vdc	**V**oltage of **D**irect **C**urrent
VDD	**V**oltage **D**rain **D**rain
VLSI	**V**ery **L**arge-**S**cale **I**ntegration
WNS	**W**orst **N**egative **S**lack
WPE	**W**ell **P**roximity **E**ffect

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Chapter 1

Introduction

1.1 Motivation

Over the past decades, the automation of the physical design of digital circuits has seen an incredible progress, while the automation of the physical design of analog circuits falls behind considerably and it is the main reason for long time-to-market of any Analog/Mixed-Signal Integrated Circuit (IC) chip. The main problem is that a good physical design of analog circuits depends mainly on the physical design engineer's experience and the main concern is the quality of the physical design which requires repetitive iterations between the circuit design and physical design teams to implement a good physical design that satisfies all the circuit specifications, while in physical design of digital circuits the main complexity comes from the quantity of the devices implemented ("More Moore"). The effort done by the engineering team to finish the physical design of the analog circuit is much more than its' digital counterpart. The figure below Figure 1.1 (a) illustrates the difference between the analog design and digital design for an IC in terms of the area and effort exerted by the engineers.

Figure 1.1 (a): Area vs. Effort of an IC chip

The Research and Development (R&D) teams working in Electronic Design Automation (EDA) tools in the industry have made considerable progress in the physical design automation of the analog circuits. The tools made so far are made on some basis and they lack the experience of a layout design engineer, there are some points in modern technology nodes that helped the R&D teams to develop such tools and made the automation of the analog layout approachable: -

- Manhattan routing approach and fixed-pitch design rules in modern technology nodes have opened a gate for a rule-based automation approach.
- The ICs nowadays require many analog blocks that follow the same considerations and reliability issues mitigation techniques which made the layout task of the analog blocks more repetitive.
- The massive progress in the algorithms field and the availability of more computation power to solve such problems in the automation of analog layout.

All these points pushed the R&D teams to try closing the gap between the analog and digital physical design which in result can improve the time-to-market considerably and improve the amount of mass production all over the world.

1.2 Sources of analog layout complexity

Although layout automation in analog IC design has been improved over the past decade, this improvement isn't like the rate of improvement of its digital counterpart. This lateness in analog layout automation comes from the analog design problem itself, which is very much more complicated even for small problem sizes, it deals with many specific circuit classes; it requires a customized design approach for each circuit class, and analog circuits are very susceptible to noise and process variations.

So analog layout has been hard to automate as in analog design the major design goals are gain, bandwidth, stability, noise reduction, linearity, and power minimization, the analog layout will affect these goals due to the manufacturing process.

The analog layout is complex and time-consuming as analog design steps typically overlap and several steps are performed simultaneously. For example, device generation, module placement, and routing are usually executed simultaneously, and the layout designer must communicate with the circuit designer and can't without understanding the functionality of each block, after parasitic extraction, the circuit designer should simulate the circuit with parasitic and check it meet the specification so as we said there is overlap between design steps and layout steps and this complicates the process of analog layout automation.

In contrast to the digital domain, the design steps for digital circuits are mostly separated from each other and are performed sequentially where layout designers can go off and hide in a closet and do the layout which means the digital layout is completely isolated from the design steps and all the information that the layout designer need is where the inputs are, where the outputs are, and where the power rails are.

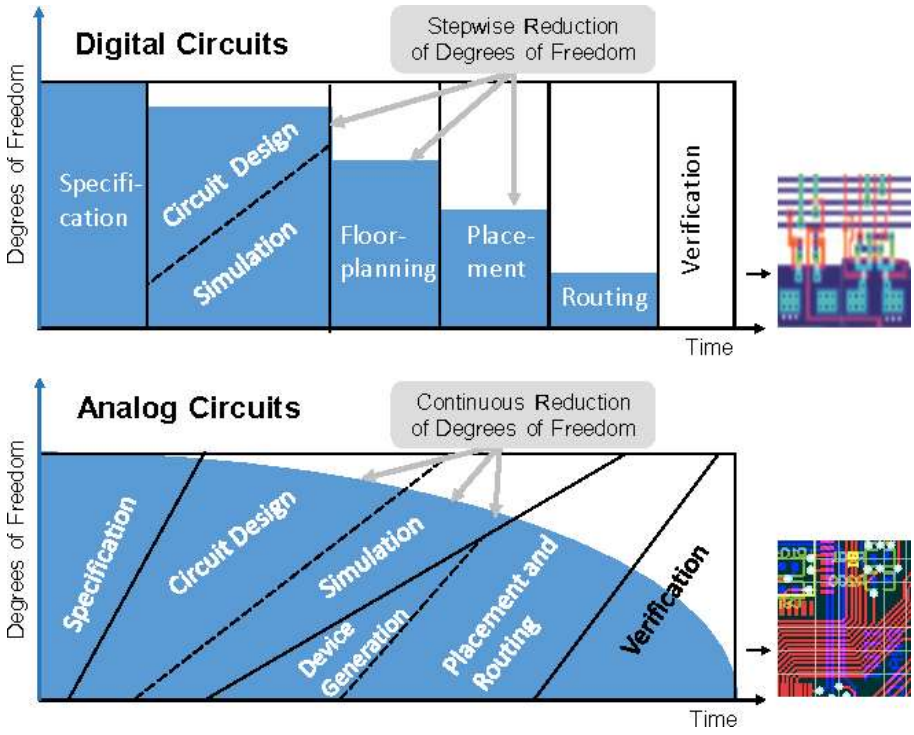


Figure 1.2 (a) difference between Analog and Digital design steps

1.3 Scripting

Nowadays, every complicated design project will place high importance on high quality as well as time to market [17]. Scripting can be a good solution to boost the design process. it can used to automate the repetitive operations that take long time in design journey.

1.3.1 What is the scripting language

A scripting language is a programming language that is interpreted. It is a series of commands that can be executed without compiling. unlike the programming language scripting languages do not require the compilation step as they translate the commands and directly interpreted from source code [18]. Examples of scripting languages:

- Python
- TCL
- Perl

1.3.2 Custom compiler Tcl

Tools in this thesis are designed with custom compiler tcl . Custom compiler tcl has some benefits that help us to design our tools as following [19]:

- As a scripting language, custom compiler tcl provides enough programmability (variables, control flow, and procedures) which lets you build complex scripts that assemble existing commands into a new flow tailored for your needs
- Custom Compiler TCL is built for user convenience. Users knowing TCL and basic Custom Compiler TCL methods can easily write scripts for any application in the Custom Compiler platform
- Traditional TCL has its graphical extension (TK). Similarly, Custom Compiler has built-in OPAL framework, which provides standard components for building user interface

Chapter 2

Learning phase and literature Review

2.1 Learning phase

We started by learning the basics of VLSI, moving on devices fabrication, fabrication problems and analog layout issues. We'll talk about this learning phase by three sections:

- Illustration these basics before starting on the main topic to be on common ground.
- Discussing the Layout or the standard cells we have done in the learning phase
- Talking about TCL language and the projects we have done with it

2.1.1 Passive elements

Resistors

As we know resistors are one of the main passive's components, we need either in analog or digital so we'll talk briefly about its types and its definitions.
In semiconductor field we define the resistance by the product of the resistance sheet and the number of squares of this resistance.

Rs has units of "ohms/square", and you are probably tempted to ask "per square what?". Well, it can be any square at all, cm, μm, km, since all we really need to know is Rs and the length to width ratio of the resistor structure to find the resistance of a resistor. We do not need to know what units are used to measure the length and the width, so long as they are the same for both. For instance, if the resistor has a sheet resistivity of 50 Ω/square, then by blocking the resistor off into squares WxW in dimension, we see that the resistor is 7 squares so R=50(Ωsquare)7(squares)=350(Ω).

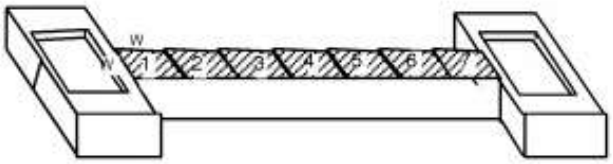


Figure 2.1.1 (a) showing the squares of a resistor

- **Diffusion resistor**

The cross-section of a diffusion resistor is shown in Figure 2.1.1(b) . It is a structure very similar to a MOSFET with the gate removed. Thus, rather than a 4-terminal device, it is a three-terminal device. The third terminal is the substrate (t0), which acts to modulate the channel resistance in the same way that substrate acts as a back-gate in a MOSFET. It can be modeled as a JFET where the substrate acts as the gate. In this paper a very simple empirical model is developed that can be easily extracted. This model is not meant to compete against the more sophisticated physics-based models [3, 4], rather this three-terminal model is provided as an alternative to the simple two-terminal model that are commonly used. Trying to model a three-terminal component with a two-terminal model results in several problems that are neatly resolved by this model.

Neglecting any high frequency effects, and assuming normal operation, the current through the resistor in the normal mode of operation flows between terminals t1 and t2. However, it is a three-

terminal element in that the characteristics are dependent on the voltage at the substrate terminal t0. The voltage of the substrate acts to modulate the resistance between t1 and t2.

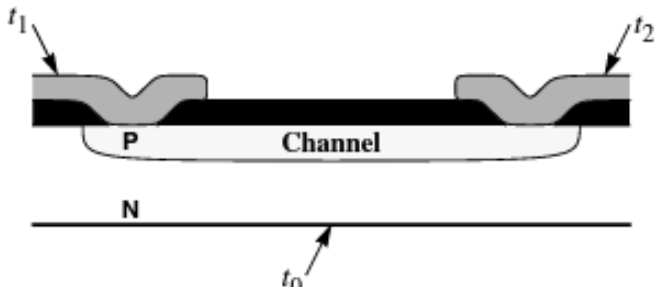


Figure 2.1.1 (b) Cross-section of a p-type diffusion resistor

- **Poly resistor**

A resistor has a resistor body of polycrystalline silicon and electric contact regions arranged on and/or in the resistor body, so that a resistor part is formed between the contact regions, which gives the resistor its resistance. The material in the resistor body is doped with for example boron to define its resistance. To give the resistor a good long-term stability the resistor part is protected by one or more oxide-based blocking layers produced from transition metals. These blocking layers can prevent movable kinds of atoms such as hydrogen from reaching the unsaturated bonds in the polysilicon. Such movable kinds of atoms can for example exist in passivation layers located outermost in an integrated electronic circuit in which the resistor is included. The blocking layers can be produced from layers having 30% titanium and 70% tungsten, which are oxidized using hydrogen peroxide. As shown in figure 2.1.1(c) we can see a cross section of poly resistor above p-substrate.

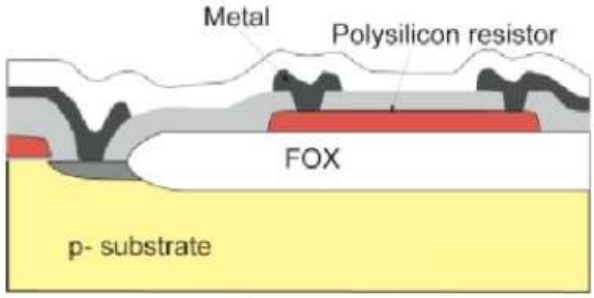


Figure 2.1.1 (c) Cross-section of a Poly resistor

- **Nwell resistor**

N-well resistors are sometimes used to add series resistance to a grounded-gate NMOST protection device in order to ensure simultaneous triggering of multiple fingers. It turns out that such protections may fail far below their nominal electrostatic discharge (ESD) threshold depending on the particular layout. It is shown that n-well snapback plays a major role in the failure mechanism. Maximum ESD performance can be obtained by applying a simple design rule for the n-well geometry. As shown in figure 2.1.1(d) we can see a cross section of Nwell resistor above p-substrate.

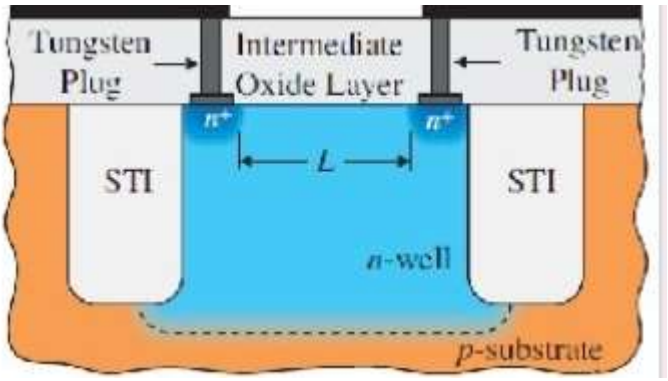


Figure 2.1.1 (d) Cross-section of a Nwell diffusion resistor

Diffusion into Nwell resistor

In this type we combine diffusion resistor immersed into Nwell.This gives us higher resistance compared to each type alone.

- **p-Base and Pinched-Base Resistors**

With the additional p-base diffusion in the BiCMOS process, two additional resistor structures are available. The p-base diffusion can be used to form a straightforward p-base resistor as shown in Figure 2.1.1(e) Since the base region is usually of a relatively low doping level and has a moderate junction depth, it is suitable for medium-value resistors (a few kilohms). If a large resistor value is required, the pinched-base resistor can be used. In this structure, the p-base region is encroached by the n+ diffusion, restricting the conduction path.

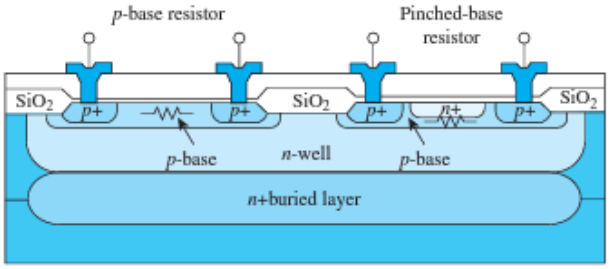


Figure 2.1.1 (e) Cross-section of a p-Base and Pinched-Base resistor.

- **Metal resistor**

Here we are using the metal resistivity whether we use cupper of aluminum, also we calculate the resistivity by the product of the resistance sheet and the number of squares of this resistance as illustrated in figure (2.1.1 (a)).

Capacitors

The primary purpose of capacitors is to store electrostatic energy in an electric field and where possible, to supply this energy to the circuit. To prevent a dangerous failure of the circuit, they allow the AC to move but block the flow of DC.

- **MOM capacitor**

MOM (Metal-Oxide-Metal) capacitors are today the workhorses for providing a large number of stored charges in sub-100 nm CMOS nodes. In these nodes the BEOL (Back-End-to-Line) distances are in the range of tens of nanometers. Even with increasing BEOL distances in broadly exploited and less expensive CMOS nodes with critical dimensions=130 nm or greater these structures are approaching into the focus as they allow the further shrink of analogue circuits. Furthermore, these structures can be implemented without any additional mask adder to the conventional flow.

We present results of capacitance measurements of various structures mainly to be distinguished by the distance of the metal. A simple empirical model consisting of an area and a fringing part is derived out of structures with same area but different perimeter.

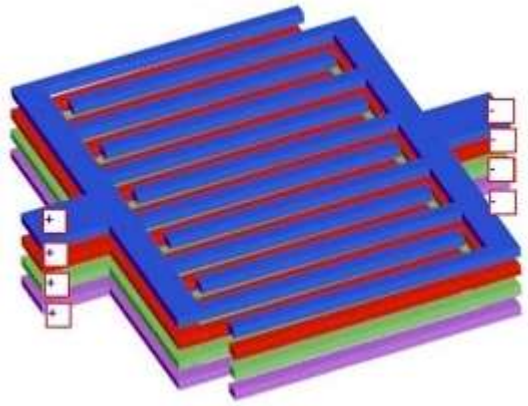


Figure 2.1.1 (f) Cross-section of a MOM capacitor.

- **MIM capacitor**

A MIM capacitor consists of parallel plates formed by two metal planes separated by a thin dielectric. MIM capacitors are used in RF circuits for oscillators, phase-shift networks, coupling, and bypass capacitance. They are also useful for analog design, due to their highly linear nature and dynamic range.

Special processes exist to create MIM capacitors, and these devices are usually formed in additional top layers of the stack. For example, in the IBM CMOS10LP/RFe process technology, a MIM capacitor is formed by adding two masks between the last metal and terminal aluminum layers.

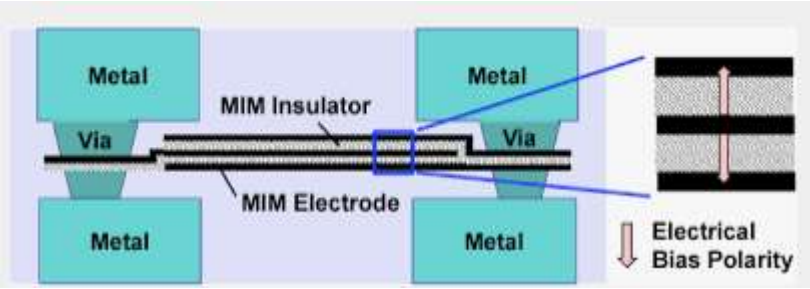


Figure 2.1.1 (g) Cross-section of a MIM capacitor

- **PIP capacitor**

A PIP capacitor and methods thereof. A method of fabricating a PIP capacitor may include forming a field oxide film over a silicon substrate to define a device isolating region and/or an active region. A method of fabricating a PIP capacitor may include forming a lower polysilicon electrode having doped impurities on and/or over a field oxide film. A method of fabricating a PIP capacitor may include performing an oxidizing step to form a first oxide film over a polysilicon and/or a second oxide film on and/or over an active region. A method of fabricating a PIP capacitor may include forming an upper polysilicon electrode on and/or over a region of a first oxide film and forming a gate electrode on and/or over a second oxide film at substantially the same time. A method of fabricating a PIP capacitor may include forming a polysilicon resistor. A PIP capacitor is disclosed.

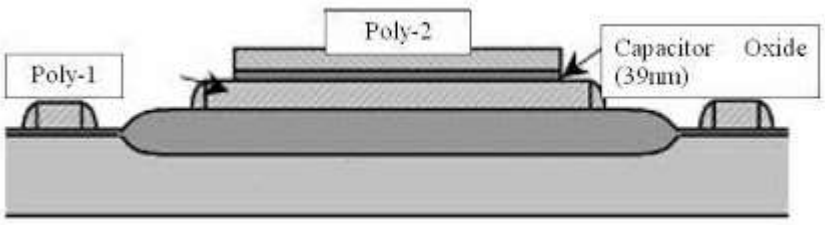


Figure 2.1.1 (g) Cross-section of a PIP capacitor

- **MOS capacitor**

The MOS capacitor or metal-oxide-semiconductor capacitor is a two terminal device consisting of three layers: a metal gate electrode, a separating insulator (often an oxide layer), and a semiconducting layer called the body. The device operates using the field effect, that is, the modulation of the surface conductivity of the semiconductor body by means of an applied voltage between the gate and the body.

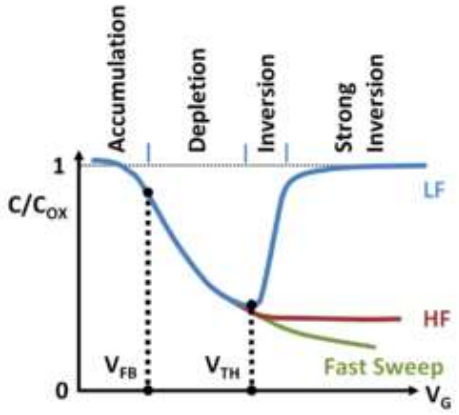


Figure 2.1.1 (h) three different types of MOS capacitor

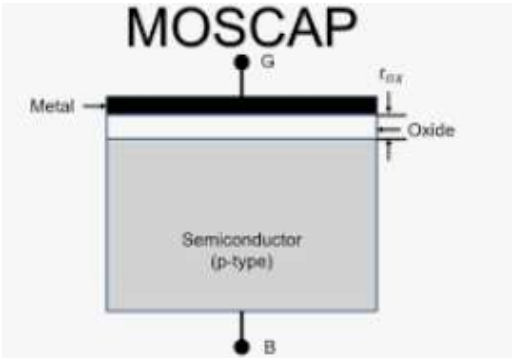


Figure 2.1.1 (I) Cross-section of a MOS

Figure 2.1.1 (I) shows three different types of small-signal capacitance vs. voltage curves observed in the MOS capacitor, in this case on a p-type substrate. A small-signal gate bias variation is superposed upon the steady bias V_G. For steady voltages V_G above the threshold voltage V_{TH} an inversion layer can form. The inversion regime of biases is divided in the figure into the strong inversion regime, where the inversion layer capacitance is so large at low frequencies that the overall capacitance is close to the insulator capacitance C_{OX} and the regime labeled simply "inversion", which is the regime where the inversion layer is gaining dominance over the depletion layer capacitance.

2.1.2 PN Junction

Whenever n-type and p-type diffusion regions are placed next to each other, a pn junction diode results. A useful structure is the n-well diode shown in Fig. 2.1.2 (a). The diode fabricated in an n well can provide a high breakdown voltage. This diode is essential for the input clamping circuits for protection against electrostatic discharge. The diode is also very useful as an on-chip temperature sensor by monitoring the variation of its forward voltage drop.

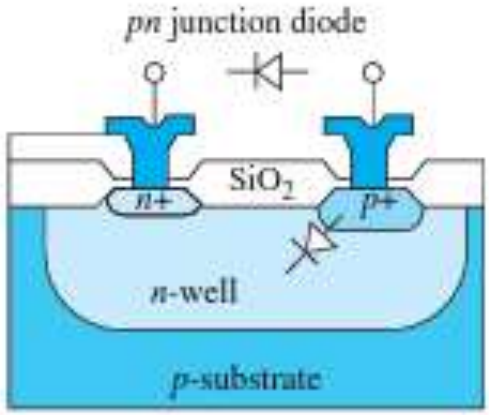


Figure 2.1.2 (a) Cross section of PN Junction

2.1.3 BJT

In CMOS technology we can fabricate the PNP and NPN transistors as in BJT technology. We will take an example for NPN and PNP is the compliment of this design. An NPN vertical bipolar transistor can be integrated into the n-well CMOS process with the addition of a p-base diffusion region Figure 2.1.3 (a). The characteristics of this device depend on the base width and the emitter area. The base width is determined by the difference in junction depth between the n+ and the p-base diffusions. The emitter area is determined by the junction area of the n+ diffusion at the emitter. The n-well serves as the collector for the npn transistor. Normally, an n+ buried layer is used to reduce the series resistance of the collector, since the n well has a very high resistivity. However, this would further complicate the process by introducing p-type epitaxy and one more masking step. Other variations on the bipolar transistor includes poly-emitter and self-aligned base contact to minimize parasitic effects.

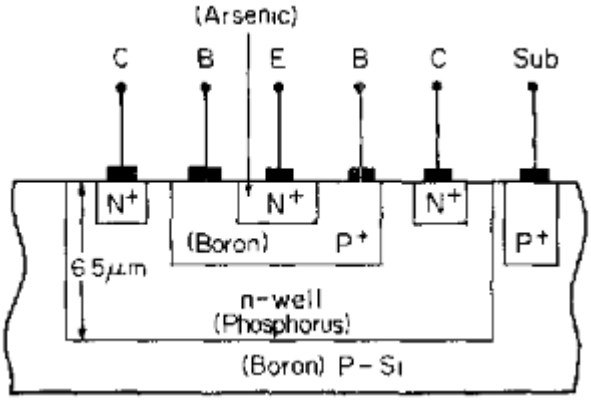


Figure 2.1.3 (a) Schematic cross-sectional view of the isolated vertical n-p-n transistor.

2.1.4 Antenna effect

During the Fabrication Process the large amount of charge is induced in plasma etching, ion implantation and in other processes. If a large interconnect (Poly or other Conducting material) is connected to the Gate of a MOSFET, then this larger conducting material will act as Antenna and will receive the induced charge of the Fabrication Process. The charge due to these extra carriers might be too much for the thin gate to handle it, and it may also damage the thin oxide layer. So, Antenna effect may result in breakdown of Gate Oxide or degrade the I-V Characteristics.

Antenna rules: Foundry provides the antenna rule file, which must be followed during the layout design. In the antenna rules most, common rule is Antenna Ratio same as shown in fig2. Antenna ratio is the ratio of metal area connected to the gate to the total area of gate.

Antenna area/gate area < Maximum Antenna Ratio

Antenna Preventions: Techniques to fix the antenna violations as follows:

Routing on Higher Metal Layer: Long metal can be taken to higher metal routing layer. This is known as metal jumping. This metal jumping is usually done near to the load. This metal jumping will break the long interconnect and hence the charge collected on the long interconnect will not discharge through gate oxide because the higher metal layer is not yet fabricated. This solution may increase the routing congestion on higher metal layer (See **figure 2.1.4 (a))**

Reduce the via-area: Large via area also results in process antenna violation. Converting multi-cut vias to double-cut via or double-cut vias to single-cut via reducing the cut area. This may impose serious reliability issues such as electro migration.

Diode Insertion: Diode helps dissipate charges accumulated on metal. Diode should be placed as near as possible to the gate of device on low level of metal. Connecting a diode to the gate electrode which provides a discharging path for the static charge present on the metal layer. Diode should always be connected in reverse bias, with cathode connected to gate electrode and anode connected to ground potential. (See **figure 2.1.4 (b))**

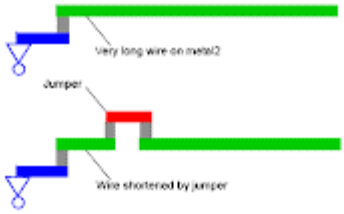


Figure 2.1.4 (a) Routing on Higher Metal Layer

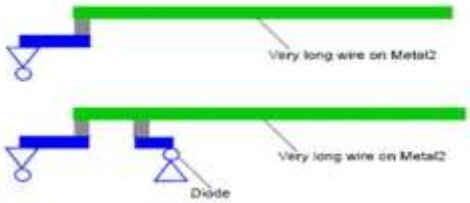


Figure 2.1.4 (b) Diode insertion

2.1.5 Latch Up

Latch up is the creation of a low impedance path between the power supply rails and is caused by the triggering of parasitic bipolar structures within an integrated circuit when applying a current or voltage stimulus on an input, output, or I/O pin or by an over on the power supply pin. Inside a CMOS circuit, two parasitic BJT (Bipolar Junction Transistors) get formed and connected in such a way that these BJT form a PNPN device or SCR (Silicon-Controlled Rectifier) or Thyristor as shown in the figures.

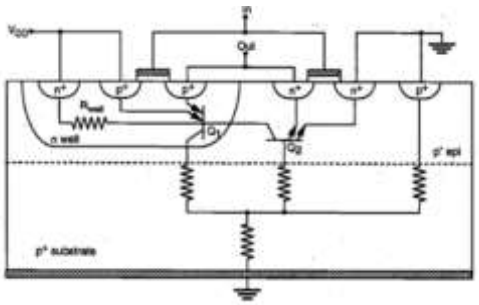


Figure 2.1.5 (a) CMOS inverter has latch up problem

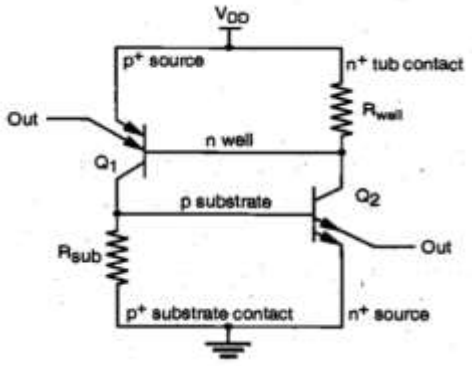


Figure 2.1.5 (b) equivalent circuit of latch up

Solutions for latch up

- Use FOX between tranistors
- Increase the number of blugs to connect noise to substrate
- Increase the dopping of Nwell

2.1.6 Substrate Isolation

Silicon integrated circuits utilize various forms of isolation to electrically isolate devices, such as reverse-biased PN junctions or trench isolation. With the exception of exotic materials such as silicon-on-sapphire, they all utilize a silicon substrate which is a potential path for noise coupling. Such coupling can decrease performance or even cause functional failures. So, designers need to use various techniques to reduce noise coupling.

Various substrate types are typical:

- High resistivity; used for RF where low loss for devices like on-chip inductors and capacitors is desirable.
- P type epi grown on a P+ substrate typically used for digital logic. The combination of low resistivity substrate, giving latch up protection, and higher resistivity epi for device performance is possible.
- Low resistivity buried layers and high resistivity epi for bipolar processes.

As shown in figure (16) an example of the importance of the substrate isolation

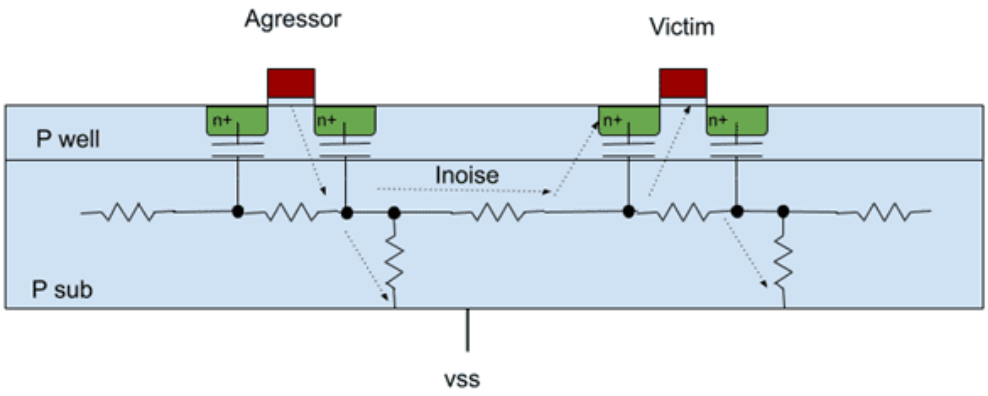


Figure 2.1.6 (a) Substrate noise coupling between two NMOS devices

figure 16 Substrate noise coupling between two NMOS devices

- Ways to reduce the substrate noise and to isolate the substrates:
  - Guard ring to isolate different blocks from each other's
  - Time scheduling between analog and digital circuits
  - Relocation of the sensitive blocks
  - Isolate the substrate using Deep Nwell
  - Increate the substrate resistance by native devices

2.1.7 Multiplier and Fingers

Multiplier

Multipliers refer to multiple copies of transistors with individual drains and source. Multiplier doesn't depend on how many fingers in the one multiplier so figure 2.1.7 (a) and 2.1.7 (b) is one multiplier although figure 2.1.7 (b) has two fingers.

Finger

Multiple fingers use shared diffusions. figure 2.1.7 (a) is one finger and figure 2.1.7 (b) is two fingers.

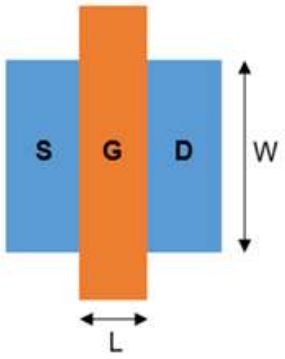


Figure 2.1.7 (a) One finger and One multiplier

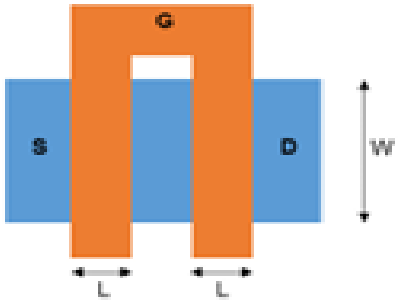


Figure 2.1.7 (b) Two finger and One multiplier

When laying out a MOSFET with a particular width and length, in an EDA tool, one has two options with regards to the shape of the gate:

1) Single stripe (classical case) (one finger);
2) Several stripes (several fingers).

Advantages for using multi fingers:

1) MF provide more flexibility in layout planning for transistor with high W/L or L/W. In other words, allows making a layout more square-like.

2) MF allow better matching of transistors, when needed. For example, if using common-centroid techniques.

3) MF layout reduces gate resistance (for AC).

4) MF reduce current density in the gate if there are technology limitations on this.

Important to match orientation if overall device matching is required

Total width = finger width *num.fingers*num.multuplier

2.1.8 Matching

Analog circuits often use structures like differential pairs and current mirrors, where the matching of device characteristics such as the threshold voltage V_t is important. Circuits using these structures with device threshold differences of a few millivolts or less can determine the performance and yield of a design. The threshold difference between a pair of (otherwise identical) MOS devices is due to the variations in number of doping atoms in the channel. This difference has been shown to be proportional to the inverse square root of the channel area,[1] and it reduces with decreasing gate oxide thickness. However, matching also requires careful layout techniques to minimize the differences in device parameters due to distance, lithography variations, rotation, process variations, biasing, and temperature gradients on the chip.

Mismatch in integrated circuits is generally of two types:

Random mismatches

Random mismatches due to microscopic fluctuations in dimensions, doping, oxide thickness, and other parameters that influence component values

Systematic mismatches

Systematic mismatches are caused by: Process biases, Mechanical stress, Temperature gradients, and Polysilicon etch rates, etc.

Before talking about matching techniques let's see **the Rules for MOS transistor matching:**

- Place transistors segments in the areas of low-stress gradients.
- Place transistors in close proximity.
- Orient transistors in the same direction.
- Keep the layout of the transistors as compact as possible
- Whenever possible use Common centroid layouts as will be illustrated.
- Place transistors well away from the power devices.
- For current matching keep overdrive voltage large.
- For voltage, matching keeps overdrive voltage smaller.

We have two matching techniques:

1. **Common centroid**

Common centroid layout is generally used with Diff pairs or current mirrors. It is a matching method in which the two transistors of the Diff pair are symmetrically laid out about a certain axis. This guarantees that both transistors see the same process variations so they'd be matched under all conditions. This method depends on having a symmetry axis for the drawn pattern as figure (2.1.8 (a)).

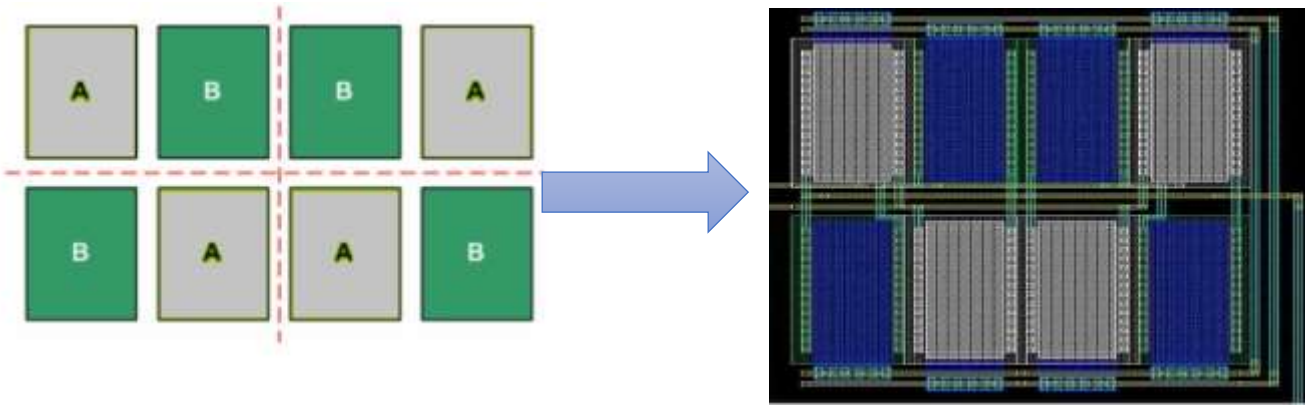


Figure 2.1.8 (a) example for common centroid pattern

2. Inter digitalization

In an interdigitated pattern, all the transistors are in an interleaved pattern like suppose there are two transistors A & B with 2 fingers each. then ABAB or ABBA or AABB called interdigitation. Here in figure (2.1.8 (b)) the first half is exactly mirrored and the variations for A and B are the same. While in a

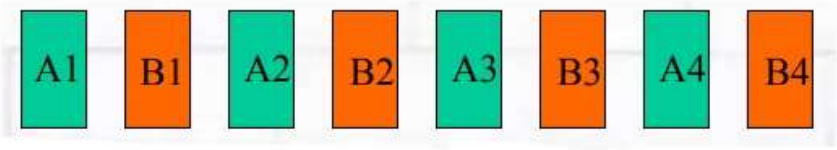


Figure 2.1.8 (b) example for interdigitated pattern

common centroid pattern we care for X and Y variations unlike interdigitated we care only X variations while in common centroid we can match in both axis (X & Y-axis).

2.1.9 Layout Second Effects

Length of Diffusion (LOD)

This is known as "**length of diffusion**" or LOD effect, where the characteristics of a device vary according to the distance of its gate from the diffusion edge. To design with LDE effects, various layout techniques can be used: Use similar diffusion size, shape, orientation. As shown in figure (2.1.9 (a)) Transistor A the distance from gate to the end of the right diffusion is bigger than the distance from gate to source of A so this transistor well suffers from LOD. We can use dummy to reduce this problem.

Reasons for LOD: -

- Drain or source sharing between transistors
- Silicon shallow trench isolation

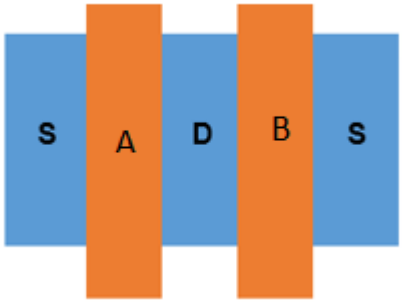


Figure 2.1.9 (a) shows the effect of LDO

Shallow trench isolation (STI)

STI "shallow trench isolation" stress is **the stress that is exerted by STI wells on device active regions and is generally compressive in nature**. Irrespective of the use of stress modulation techniques in the process, STI stress is not negligible and its magnitude depends on the sizes of the STI wells and the active regions for a given process.

STI

STI also known as box isolation technique, is an integrated circuit feature which prevents electric current leakage between adjacent semiconductor device components. STI is generally used on CMOS process technology nodes of 250 nanometers and smaller. Older CMOS technologies and non-MOS technologies commonly use isolation based on LOCOS. The Shallow Trench Isolation (STI) is the preferred isolation technique for the sub-0.5 μm technology, because it completely avoids the bird's beak shape characteristic. With its zero-oxide field encroachment STI is more suitable for the increased density requirements, because it allows forming of smaller isolation regions. The STI process starts in the same way as the LOCOS process. The first difference compared to LOCOS is that a shallow trench is etched into the silicon substrate, as shown in Figure 2.2.9 (b). After under etching of the oxide pad, also a thermal oxide in the trench is grown, the so-called liner oxide.But unlike with LOCOS, the thermal oxidation process is stopped after the formation of a thin oxide layer, and the rest of the trench is filled with a deposited oxide .Next, the excessive (deposited) oxide is removed with chemical mechanical planarization. At last, the nitride mask is also removed. The price for saving space with STI is the larger number of different process steps.

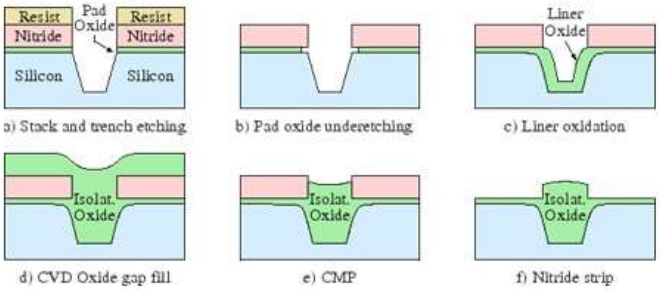


Figure 2.1.9 (b) LOCOS Process

Deep trench isolation

It uses the trenches of fixed width, typically 0.18 to 1 μm in width and 2 to 5 m in width and 2 to 5 μm in depth. Smaller trench widths are particularly attractive for memory application. It finds application in CMOS image sensors (used in camera). The process is fabricated by starting from a standard LOCOS structure. After nitride patterning, the trenches are etched. Trench is typically done by simultaneously depositing SiO2SiO2 while etching silicon anisotropically.

This creates small cusp of SiO2SiO2 at the top of the trench. The thickness of this cusp increases with time and create desired taper. The walls cannot undercut the mask and must result in rounded bottom. Then a field implant is done. The implant is followed by a thin local oxidation.

Finally, a layer of polysilicon is deposited and etched back. If polysilicon is thick enough it will fill the groove. Second thermal oxidation can be used to complete the process by oxidizing the upper part of polysilicon in groove.

Well Proximity Effect (WPE)

This lateral non-uniformity in well doping causes the MOSFET threshold voltages and other electrical characteristics to vary with the distance of the transistor to the well-edge. This phenomenon is commonly known as the well proximity effect (WPE).

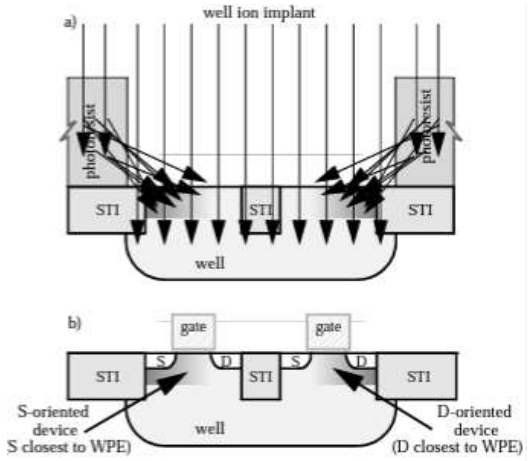


Figure 2.1.9 (c) shows the distribution of the doping due to WPE

2.2 Training Projects

This phase will be divides two sections Layout section and Scripting section. Let's talk now about **Layout section**:

After learning the basics of VLSI and analog layout concepts we started to build basic digital blocks to understand how to use the tool and how to pass DRC and LVS verifications. The standard cells we have done are XOR, AND, OR, NOT taking in account the following conditions:

- All the blocks have to be the same height.
- The supply metal stack must be the same level.
- Use the minimum dimensions as these are digital blocks, the most important factors Area, Power and speed
- Passing the DRC and LVS verifications

As shown in figure 2.2 (a) shows examples for a block we have done which is 3Input NOR.

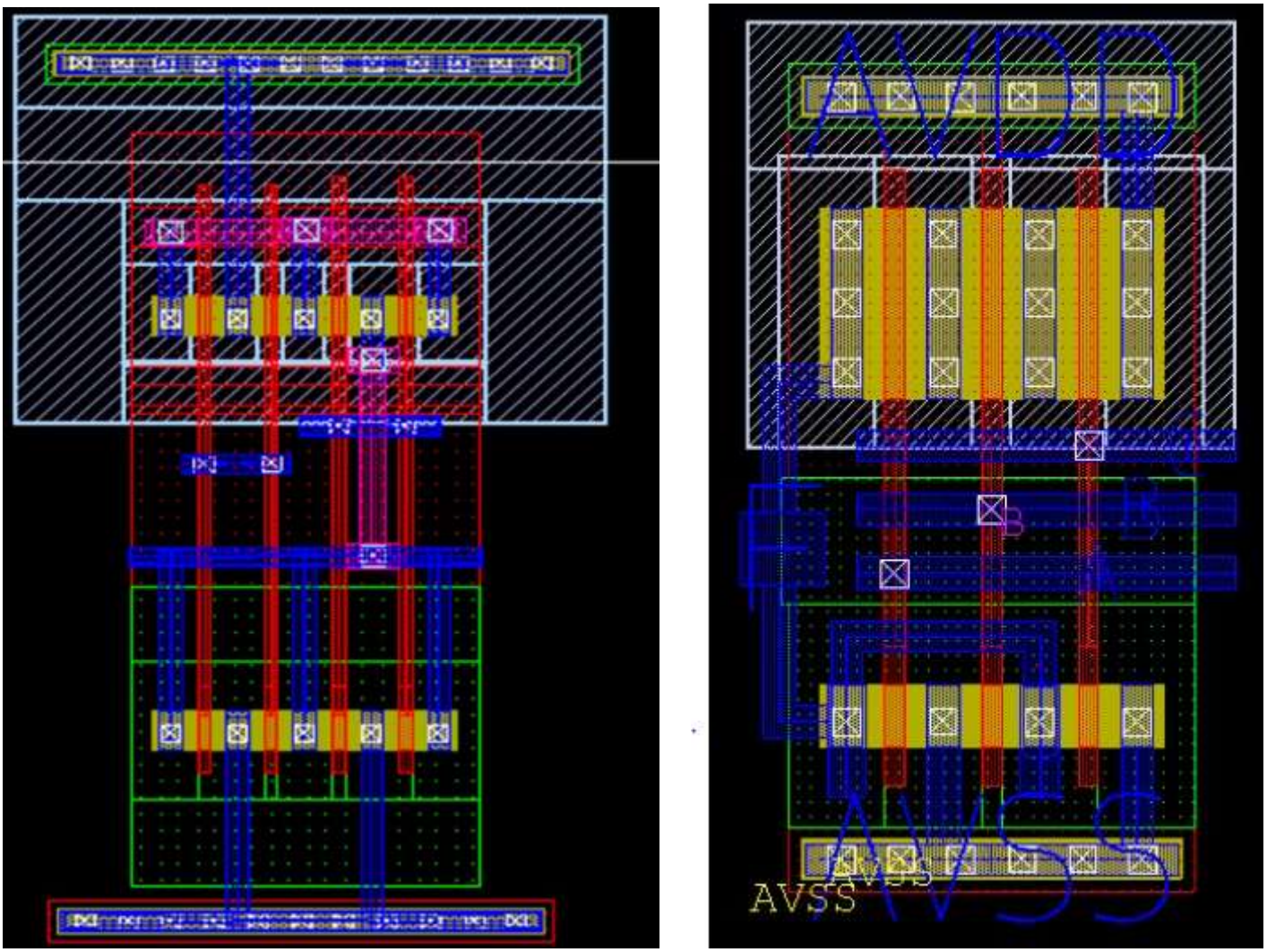


Figure 2.2 (a) Layout of 3 Input NOR

After making Digital blocks, we have made a fully Analog block which was a practice for most of analog concept. This block is **voltage gain amplifier**, this block consists of Current Mirror, Differential Pair, CMFB stage, resistors and capacitors as shown in figure 2.2 (b)

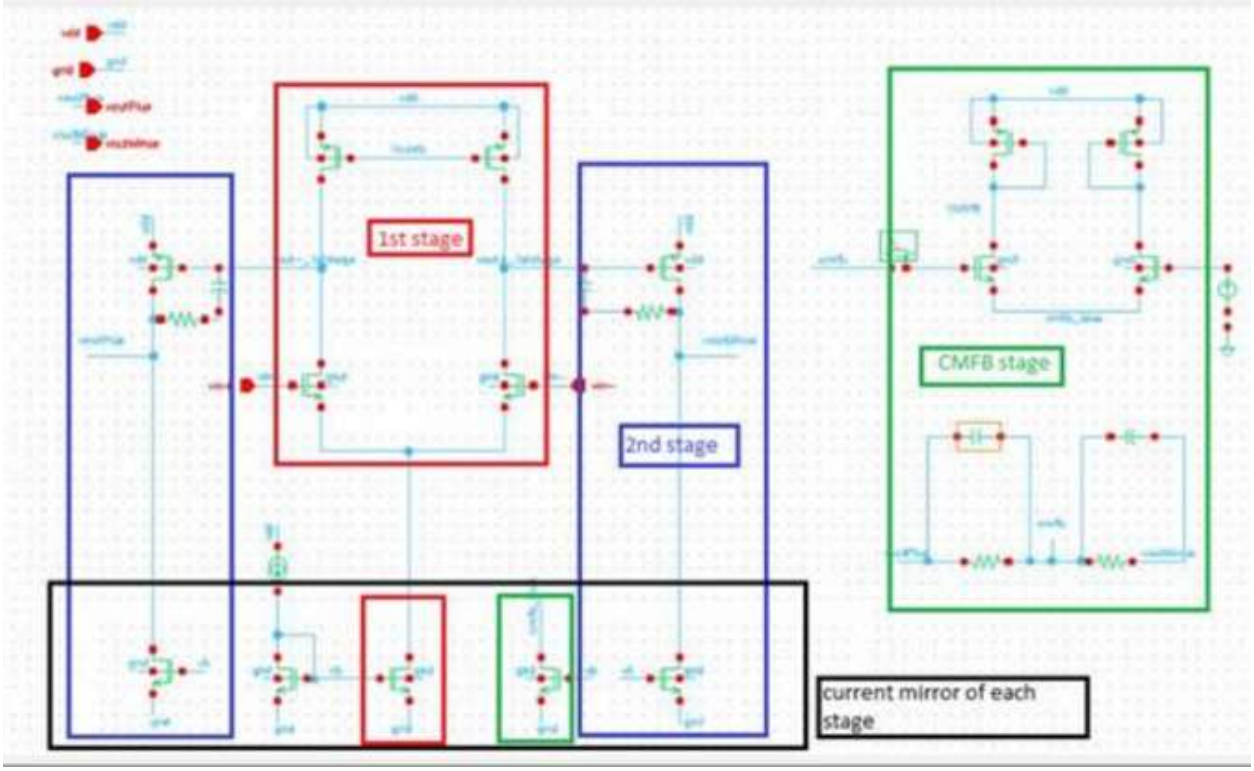


Figure 2.2 (b): Analog block -VGA- Components

Let's see the actual layout for some blocks like current mirror, differential pair, resistor and capacitor.

- Current mirror which shown in figure 2.2 (c) is matched by common centroid technique

E	E	D	C	C	B_Dummy	D	D	D	Dummy
E	E	D	C	C	B	D	D	E	E
E	E	D	C	A	B	D	D	E	E
E	E	D	D	B	A_Dummy	C	D	E	E
E	E	D	D	B	C	C	D	E	E
Dummy	D	D	D	B	C	C	D	E	E

Table 2.2a: Common centroid matching pattern for current mirror

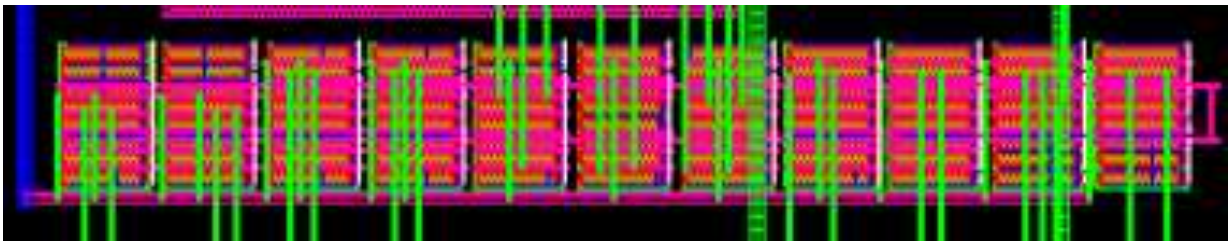


Figure 2.2 (c): Actual layout for current mirror

- Differential pair which shown in figure 2.2 (e) is matched by inter digitization

Figure 2.2 (d) Inter digitization matched technique for differntail pair

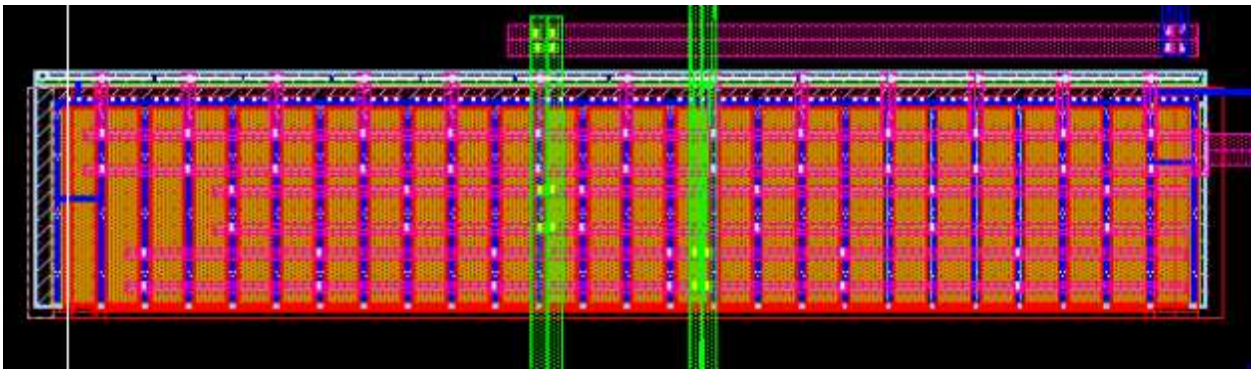


Figure 2.2 (e) Actual layout for differential pair

- Figure 2.2 (f) shows resistor layout and Figure 2.2 (g) shows capacitor layout using MOM over MOS cap

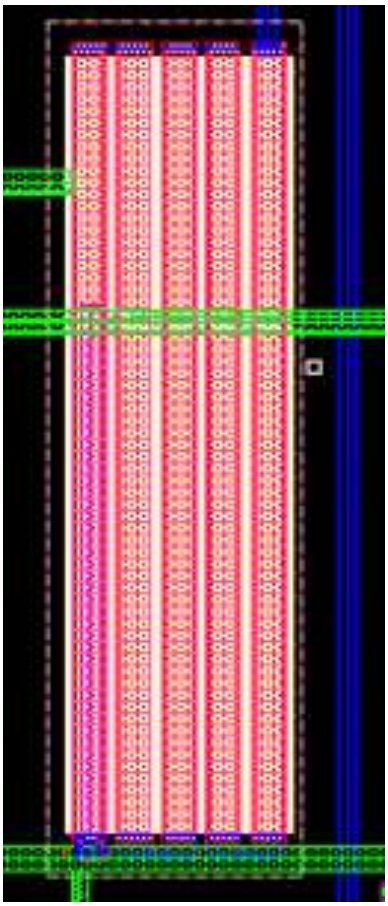


Figure 2.2 (f) Resistor layout

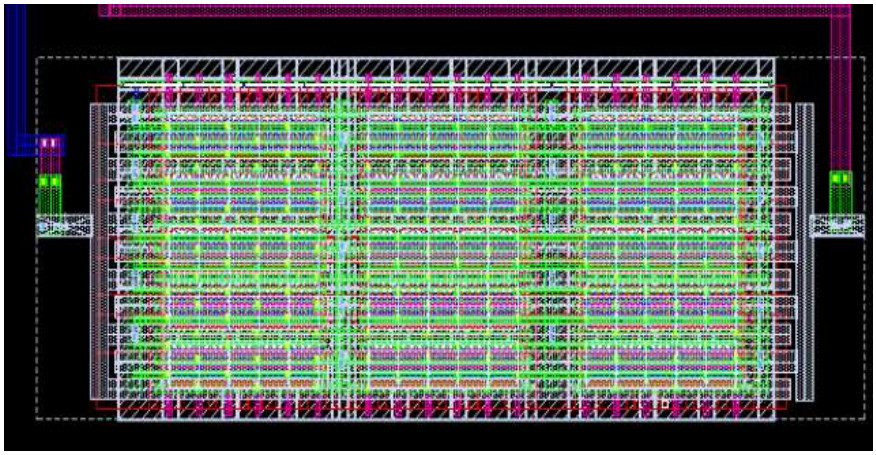


Figure 2.2 (g) capacitor layout

Now we'll talk about **Scripting section**:

We have made two projects:

1. **Binding keys** which is a script make the user hide and show the metal stack by just clicking a number using the keyboard also he can use alt +key to show this metal without kidding others and ctrl + key to show all except this metal number.

2. **Object analyzer** which makes the user discover all the attributes which concern on certain object. In figure 2.2 (I) has many options have to be discussed
   - User can select many objects from layout then press the SelectedObject -Red square- and looping on them one by one and discover each one using Previous and Next Buttons-Green square-.
   - Also, user can enter a certain command then press Command -Blue button- and discover the object which will be returned.
   - If the user needs to enter another command or select another object, he has to press the fresh button -Brown button -

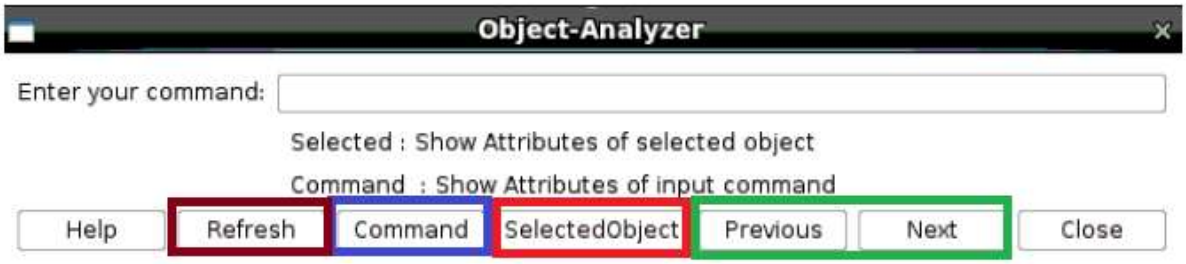


Figure 2.2 (h) Object Analyzer GUI

The figure 2.2 (K) shows an example and extra features:

- The red square shows the user the number of selected items from layout.
- The green words means that this object has internal objects. If the user needs to discover, he just has to double click on it and will be appear as figure 2.2 (J).
- GUI has guide lines for users to make it easier to read the GUI.

Figure 2.2 (i) This figure shows if the Object has internal Objects

Figure 2.2 (j) Example shows the Object Analyzer features

2.3 Literature Review

The interconnect delay has become the dominant factor affecting system performance. Today's electronic systems such as computers and digital communication systems, have necessitated a rapid increase in operating frequency. Because of this, VLSI interconnects have become one of the critical issues in an overall system design. Improperly designed interconnects lead to signal integrity degradations such as signal delay, cross talk and ground noise, limiting the overall system performance. In recent years, research into the interconnect optimization problem has been very active, and much important progress has been made. so, we had to do heavy searching to select the best, accurate and general solution. Here we'll discuss the latest published papers, each paper will be discussed as follow: abstract, the technique they used and why we selected it or not.

2.3.1 Studies papers and Research

Paper 1: AN OPTIMIZATION ALGORITHM BASED ON GRID-GRAPHS FOR MINIMIZING INTERCONNECT DELAY IN VLSI LAYOUT DESIGN

Abstract

In this paper, they described a routing optimization algorithm based on grid-graphs for application in a deep-submicron VLSI layout design. The algorithm is named S-RABILA (for Simultaneous Routing and Buffer Insertion with Look-Ahead), constructs a maze routing path, with buffer insertion and wire sizing, taking into account wire and buffer obstacles, such that the interconnect delay from source to sink

is minimized. A key contribution of this work is a novel look-ahead scheme applied to speed up the runtime of the algorithm, and aids in finding the exact solution. Hence, the algorithm is accurate, fast, scalable with problem size, and can handle large routing graphs. Experimental results show the effectiveness of the look-ahead scheme and indicate that S-RABILA provides significant performance improvements over similar existing VLSI routing algorithms.

Their technique
A routing optimization algorithm based on grid-graphs.

Why not selected
This paper mainly focusses on digital issues as they used buffer insertion but our issues focus on analog layout so this solution won't be efficient for our situation. Also, this paper used Interconnect approximate Delay Model and we wanted to do an accurate model without any approximation.

Paper 2: GLOBAL INTERCONNECT WIDTH AND SPACING OPTIMIZATION FOR LATENCY, BANDWIDTH AND POWER DISSIPATION

Abstract
In this paper addresses a novel methodology optimizing global interconnect width and spacing for International Technology Roadmap for Semiconductors technology nodes. Global interconnects with and without buffer insertion are considered. The effects of the width and spacing of global interconnects on performance, such as delay, bandwidth, total repeater area and energy dissipation, are analyzed. The product of delay and bandwidth is used as the figure of merit for simultaneous short latency and large bandwidth and the proposed methodology can optimize global interconnects for the maximal figure of merit. It is demonstrated that buffers should not be inserted in global interconnects if interconnect length is shorter than a critical length, which is a constant for a given technology. For global interconnects with buffer insertion, the optimal width and spacing have analytical expressions and are constants for a given technology. For global interconnects without buffer insertion, the optimal width and spacing are dependent on both the technology parameters and interconnect length and can be computed numerically.

Their technique
A novel methodology optimizing global interconnect width and spacing for International Technology Roadmap for Semiconductors technology nodes.

Why not selected
This technique also had been forced to insert buffers on long wires which focuses on digital not analog issues also depends on charts which takes a lot of time to build and the cases reached to be infinite so to overcome this issue they will use approximations because it is impossible to cover all the cases which the engineer will face also, they have more than 2 parameters to set which made the charts are 3D, this made the matter harder and complex.
Figure 2.3.1 (a) shows the complexity of the figures

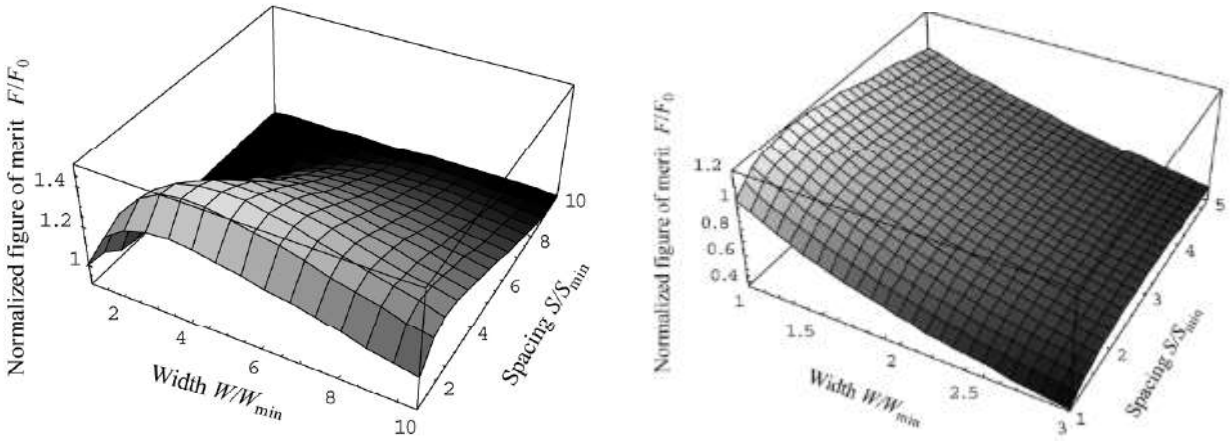


Figure 2.3.1 (a) Samples of Used figures in this paper

Paper 3: INTEGRATED CIRCUIT CONCEPTION: A WIRE OPTIMIZATION TECHNIC REDUCING INTERCONNECTION DELAY IN ADVANCED TECHNOLOGY NODES

Abstract

In this paper, we will introduce a new routing technique, with the objective to optimize timing, by only acting on routing topology, and without impacting the IC Area. In fact, the self-aligned double patterning (SADP) technology offers an important difference on layer resistance between SADP and No-SADP layers; this property will be taken as an advantage to drive the global router to use No-SADP less resistive layers for critical nets. To prove the benefit on real test cases. Their experiments show that worst negative slack (WNS) and total negative slack (TNS) improved up to 13% and 56%, respectively, compared to the baseline flow.

They have special features which are adding automation to their solution based on Mentor Graphics' physical design EDA tool Nitro-SoC™ and focused on some issues like honoring all physical constraints coming with cutting-edge technologies and achieving expected quality of results (QoR).

Their technique

A new routing technique.

Why not selected

After examining on the paper, we didn't find the automation part as they mentioned! also there isn't a direct solution it depends on the engineer experience as using higher metal stack as this already the engineers do. Also, their technique has 8 steps which is consuming time for engineers.

Paper 4: OPTIMIZATION OF INTERCONNECT ARCHITECTURES THROUGH CODING
Abstract

In this paper, provides a thorough review and analysis of the advantages and possibilities of coding for addressing the aforementioned challenges during the optimization of the communication architecture of a System-on-Chip. An outlook into future research directions is also presented. As technology improves and the system bottlenecks shift from the processing to the communication plane, some concepts from the (off-chip) communication system engineering are getting introduced and adapted for on-chip communication architecture. This work focuses on the use of coding strategies to improve the on-chip interconnect architecture. As depicted in Figure (2.3.1 (b)), the main idea is to include an encoder and a decoder in the communication path, so that the characteristics of the signal can be adapted to the properties of the physical medium.

Figure 2.3.1 (b) Optimization of the interconnect architecture through coding and related trade-offs.

Their technique
Using coding techniques to optimize the interconnect delay

Why not selected

This paper combined between communication concepts and layout which made the matter more and more complex. Also based on very complex analysis, equations and results. Also, their solution can't be done using Synopsis Custom Compiler EDA tool. If need to use their solution we will make a lot of approximations to make the job understandable and easy to compatible with the tool and we will back to the main problem which is approximation

2.3.2 Our Selection Technique

We build our tool based on simulation results to use the simulation advantages without any approximations. Our tools suit any field: analog or digital or AMS, not specified field as all papers focus only one field so we need general purpose tool which is our choice. To know how powerful is our choice let's know the simulation benefits for analog, digital and AMS.

- **Digital** simulation tools use simple models of electronic circuits to test circuit designs. However, instead of populating continuously varied signals like analog circuit simulation, it only uses a few small voltage levels (logic 0 and logic 1)
- **Analog** simulation tools use accurate models of electronic circuits to test design functionality. It can employ different modes: AC, DC, and transient. All analog simulators use mathematical algorithms to test the performance of the electronic circuit. There are two types of analog circuit simulators: SPICE and FastSPICE. SPICE simulators are used to measure the functionality of the circuit by comparing it to extremely accurate, non-linear, and linear models. FastSPICE simulators, on the other hand, use less complex model representations to test the functionality of a circuit design.
- **Analog-Mixed-Signal** simulation tools naturally combine both analog and digital simulation elements. The analog simulator is used for analog analysis while the digital simulator is used for digital analysis.

Chapter 3

RC Parasitic Improvement and Isolation tool

3.1 Introduction

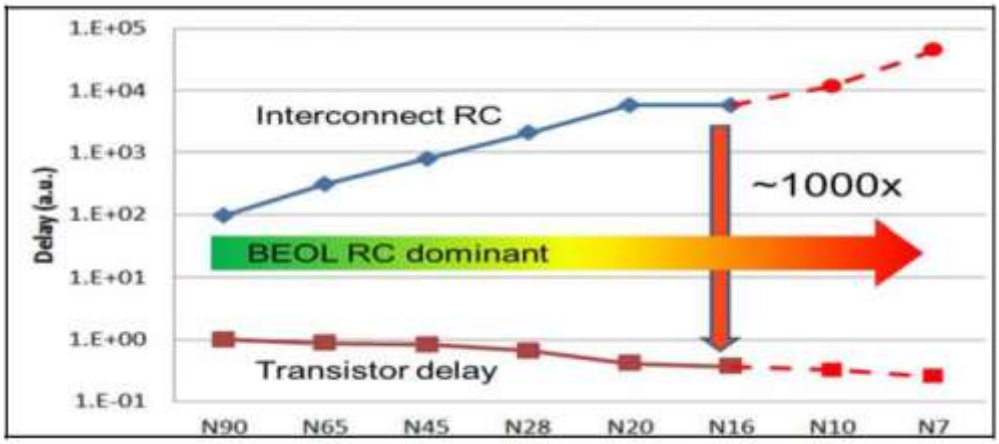


Figure 3.3 (a): Gap between Interconnect delay and Transistor gate delay from [1], IEEE, 2013

In the beginning of the Very Large-Scale Integration (VLSI) industry, the parasitic RC delay of the interconnects was not an important matter. As the technology advances, the gate delay of the transistors decreases significantly while the delay of the interconnects increases and that is because the following reasons: -

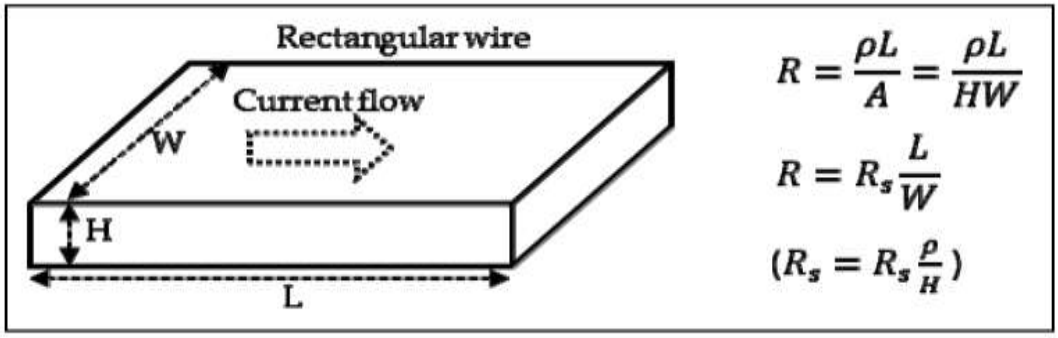


Figure 3.1 (b): Interconnect Resistance R and sheet resistance Rs from [2]

1. The interconnect dimensions cannot be scaled with the same scaling ratio used for scaling down transistor dimensions as the resistance increases and the wire chokes the current quadratically.
2. As the chip becomes faster, the skin effect appears, and the resistance increases, and the delay becomes even worse.
3. The chip size increases with technology advancing and which increase the resistance for the global routing interconnects.
4. The interwire capacitance between the interconnects increases.

3.1.1 Scaling down impact on resistance

We can examine the following equation

$$R = \frac{\rho L}{HW} \qquad (3.1.1a)$$

Assume dimensions of the wire H and W are scaling down with ration K

$$H = \frac{H}{K} \quad (3.1.1b) \qquad W = \frac{W}{K} \quad (3.1.1c)$$

Substitute by 3.1.1(b, c) in 3.1.1a

$$R_{New} = \frac{\rho L}{\left(\frac{HW}{K^2}\right)}$$

$$R_{New} = R \times K^2$$

The resistance increases quadratically and that's the reason why the interconnect dimensions cannot be scaled down with the same ratio as the transistor dimensions. Also, the length of the interconnect is not assumed to be scaled down with ratio K because the chip size actually increases, so it should be assumed that L also increases which will increase the resistance even more and that is an illustration why the interconnect resistance is a very important factor in the new technology nodes because it is the main factor that worsens the delay of the interconnect.

3.1.2 Skin effect

The skin effect is and AC effect that is highly dependent on frequency, it is a phenomenon where current flows through the entire cross-section of the interconnect and instead it flows through the outer shell of the interconnect. The current density in the interconnect can be characterized with the following equation

$$J = J_o e^{-(1+j)\left(\frac{d}{\delta}\right)} \quad (3.1.2a)$$

Where J_o is the maximum current flows at the surface, d is the depth below the surface and δ is a parameter that indicates the depth where the current drops to 1/e from its maximum value J_o

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}} \quad (3.1.2b)$$

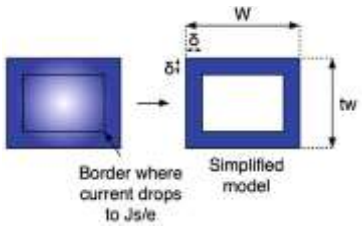


Figure 3.1.2 (a): Skin effect. Current flows more in the outer shell of the interconnect, from [3]

3.1.3 Chip size and technology advancing relation

As the technology advances, the minimum feature size decreases, however the chip size keeps increasing. This is due to the very high demand for functionality and performance which increases the complexity of the integrated circuits (ICs) requiring a greater number of transistors on the same chip to satisfy the performance and functionality needs of the IC which require more area.

The continuous feature size reduction in transistors improved the gate delay of the transistors dramatically, however the effect of this reduction on the delay of the interconnects is less positive as the chip increases so the length L of the interconnects increases to traverse the chip.
also the other dimensions scaling down is making the delay even worse as illustrated in section 3.1.1.

3.1.4 Interconnect capacitance

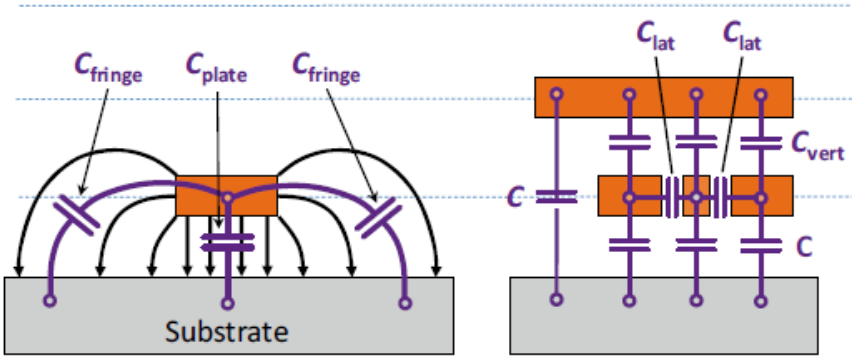


Figure 3.1.4 (a): Interconnect different capacitances, from [4]

The other important parameter that affects the interconnect performance is the capacitance of the interconnect, as shown in Figure 3.1.3 (a) there are different types of capacitances for each interconnect

1. Lateral Capacitance (Interwire Capacitance): The capacitance between the interconnects on the same metal layer.
2. Parallel Plate Capacitance (Vertical Capacitance): Vertical coupling capacitance between interconnects on different metal layers or between an interconnect and the substrate.
3. Fringe Capacitance: Capacitance between the interconnect sidewalls and the substrate/another wide interconnect.

The different types of capacitances of the interconnect affects its performance dramatically, the delay increases for the interconnect if the capacitance is happened only due to substrate and quiet signals surrounding the interconnect acts as an AC ground, for a noisy signals (High frequency and High switching power) the problem becomes much bigger as that introduces a cross-talk between the two signals which can distort the victim signal and the information that is carried on this signal might not be correct.

As the technology advances the interwire capacitance increases as shown in the following figure

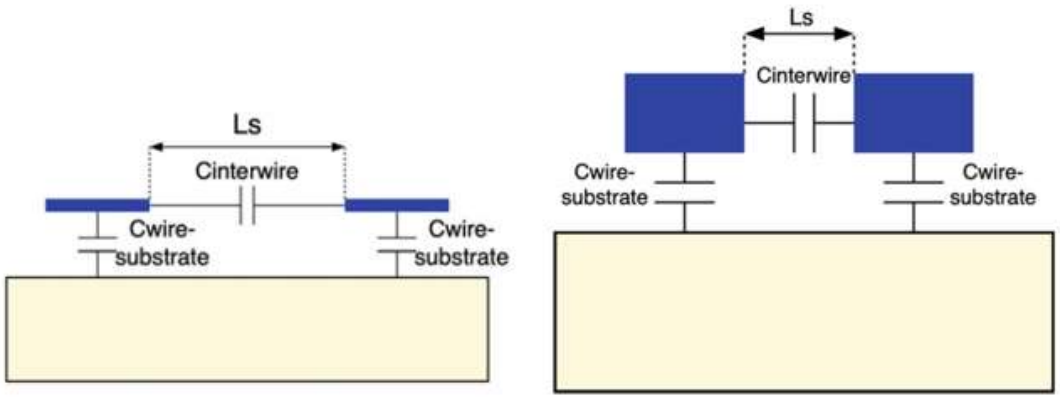


Figure 3.1.4 (b): Interwire Capacitance in old technologies (Left), Interwire Capacitance in new technologies (Right), from [3]

The capacitance between two conductors can be calculated with the following formula

$$C = \frac{\epsilon A}{d} \qquad (3.1.4a)$$

As shown in Figure 3.1.4 (b), The common area between the two sidewalls of the conductors becomes much larger as the technology advances while the minimum distance between two conductors becomes smaller. The factor $\frac{A}{d}$ increases dramatically which increases the capacitance between interconnects and degrades the performance.

3.2 Delay Estimation

3.2.1 Wire Delay model – Elmore delay formula

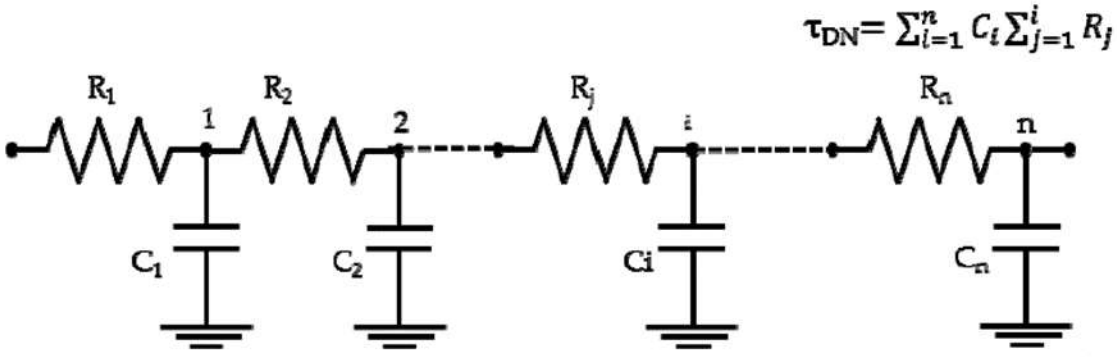


Figure 3.2.1 (a): Wire Delay Model - Elmore Delay formula, from [2]

The interconnect can be modeled by the RC sections shown in Figure 3.2.1 (a), Delay can also be calculated using the formula in Figure 3.2.1 (a).

For more accurate results we need to model the interconnect with an infinite number of RC sections.

$$\tau_{DN} = \lim_{n\to\infty} \sum_{i=1}^{n} C_i \sum_{j=1}^{i} R_j$$

That would be an approximate result and it is not practical as the capacitance calculation is very complex due to its calculated due to multiple resources.

3.2.2 Proposed method (Simulation-based delay estimation)

In this method we can create the following test case for any interconnect that has a single source, single destination.

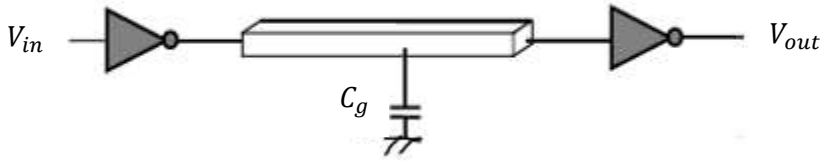


Figure 3.2.2 (a): Delay estimation test case

We can get accurate results for the delay by creating the test case in Figure 3.2.2 (a).

1. Estimate the delay of each inverter.
2. Place the interconnect between the two inverters.
3. Apply a step at the input of first inverter (V_{in}).
4. Receive the step at the output of the second inverter (V_{out}).
5. Measure the delay of the whole circuit.
6. Subtract the delay of the two inverters and get an estimate for the delay of the interconnect.

The previous method has a very high potential in future work. We can create another test case for a generic interconnect that has multiple sources and multiple destinations and get the worst-case delay, then try to improve it. But for now, we are considering the case of a single source, single destination interconnect.

The advantage of this method is the RC values are calculated accurately with the simulation.

The disadvantage of this method is mainly because it is time consuming.

3.3 RC Parasitic Improvement techniques

3.3.1 Metal layers

The figure on the right (Figure 3.3.1 (a)) shows the spacing between metal layers and each other as well as the spacing between each metal layer and the substrate.

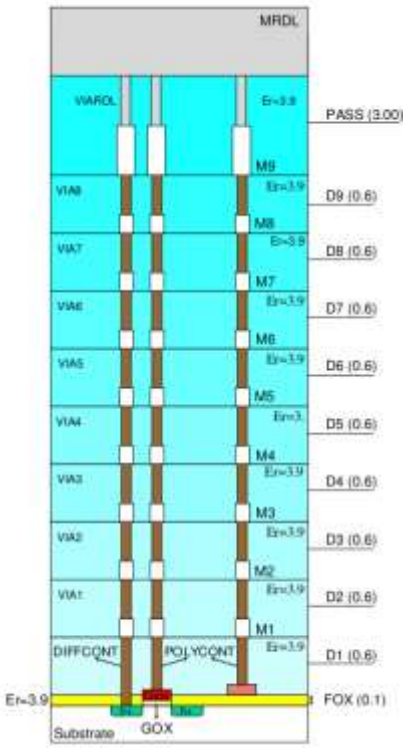


Figure 3.3.1 (a): Cross-sectional view showing all the metal layers, from [6]

Let's focus on the main reason for the interconnect delay and it is the coupling capacitance to the substrate.

Recall equation 3.1.4a

$$C = \frac{\epsilon A}{d}$$

Where d is the vertical distance between the metal and the substrate, A is the common parallel plate area of the interconnect and the substrate and ϵ is the dielectric permittivity and it is constant for the technology.

Using higher metal layers results in d increasing significantly. Assume no surroundings, then the coupling capacitance to substrate

$$C_{new} = \frac{\epsilon A}{d_{new}}$$

Where $d_{new} \gg d$ And that results in a dramatic reduction for the capacitance to substrate while keeping the same resi technology the sheet resistance R_s is constant for M1-M8 as shown in the following table. And so the value RC would decrease dramatically which means the delay is reduced.

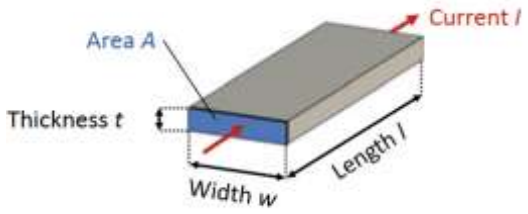


Figure 3.3.2 (a): Cross-sectional view for an interconnect, from [4]

Name	Sheet Resistance	Thickness (nm)
DIFF	0.001	50
PO	15	50
M1	0.1	95
M2	0.1	95
M3	0.1	95
M4	0.1	95
M5	0.1	95
M6	0.1	95
M7	0.1	95
M8	0.1	95
M9	0.28	190
MRDL	0.35	280

Table 3.3.1a: Sheet resistance table for SAED 32/28nm PDK, from [6]

3.3.2 Wire Sizing

As shown in Figure 3.3.2 (a) on the right, the current flows in the cross-sectional area (A=wt).

Where w is the width of the interconnect and t is the thickness of the interconnect.

The designer has control only on the width and length of the interconnect. While the thickness t is a constant for the technology.

The resistance of the interconnect can be calculated using the following formula

$$R = \frac{L}{\sigma w t} \qquad (3.3.2a)$$

Increasing the width of the interconnect should decrease the resistance R, however the designer has almost no control over the length of the interconnect after the Placing phase. So, let's investigate the effect of increasing the width on the value of RC.

Let $w_{new} > w_{old} \rightarrow R_{new} = \frac{L}{\sigma w_{new} t} > R$. The relation between the width and resistance is inversely proportional $R\ \alpha \frac{1}{w}$. But increasing the width increases the are A which in result increases the parallel plate capacitance to the substrate. Recall equation 3.1.4a

$$C = \frac{\epsilon w L}{d}$$

We can see that from the previous equation, the dominant parameter that controls the capacitance is the length L of the interconnect. So, increasing the width of the interconnect should have a bigger effect on the resistance and a slight increase in the capacitance to the substrate.

Overall, the value RC should be decreasing by increasing w and so the delay of the interconnect.

3.3.3 Metal stacking

This is another technique for decreasing the resistance of the interconnect. The idea is to keep the width of the interconnect constant while using another metal layers in parallel with the interconnect and connecting all of them with vias. Lets say we have an interconnect on M2, We will use M3, M4 in parallel with M1 with the same length and width.

The signal now can propagate in higher width and the resistance of the new interconnect R would decrease to $R_{new} \approx \frac{R}{3}$ (M2:M4 has the same sheet resistance R_s). Assuming ideal case with no surroundings. The capacitance should remain constant and RC value should decrease to $\frac{RC}{3}$ and the delay should decrease to 1/3 of its old value.

3.4 Test Case Results

In this section we will investigate each technique mentioned in section 3.3 and see the improvement results and that should serve as the basis for the delay improvement tool we will talk about the tool in detail in section 3.5.

3.4.1 Calculating the delay of a single inverter

Inverter design on the transistor level

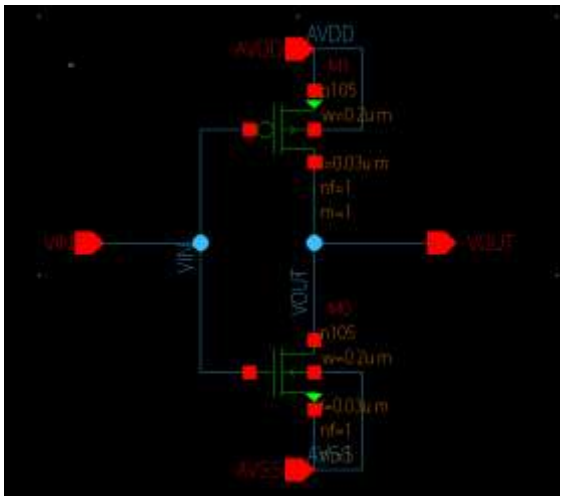


Figure 3.4.1 (a): Inverter design on the transistor level

Test Bench to calculate the delay of the inverter

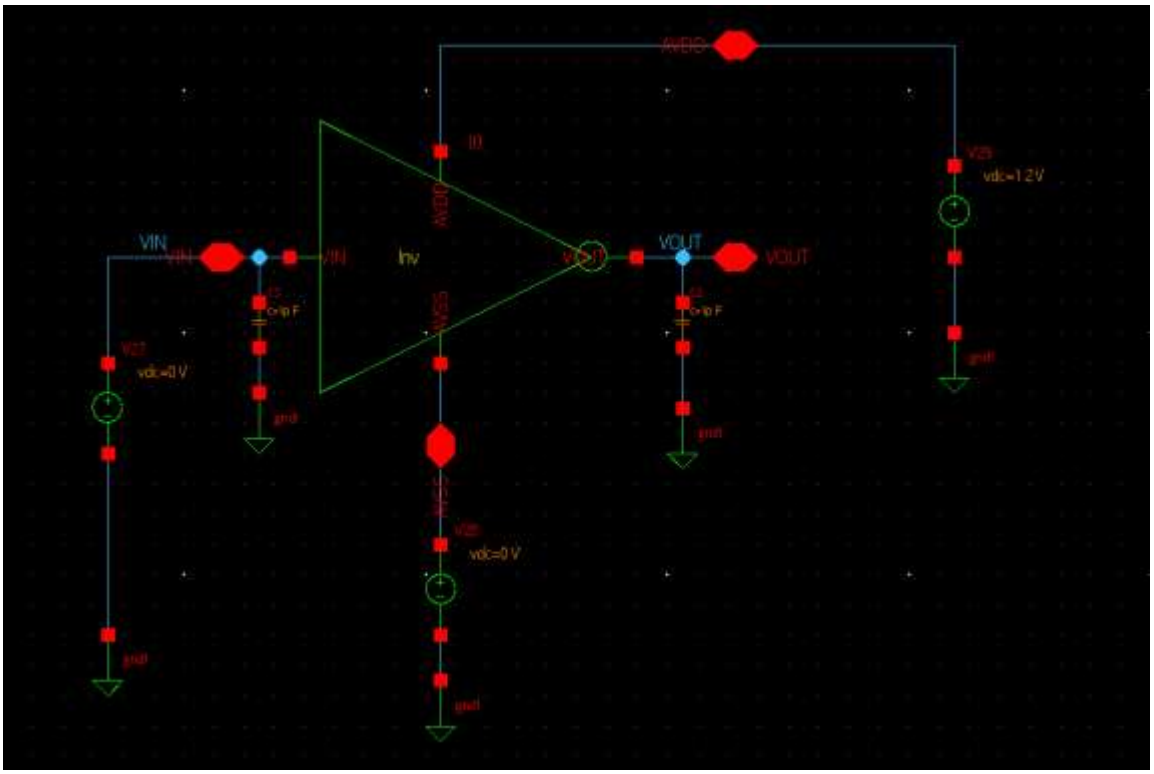


Figure 3.4.1 (b): Test bench to calculate the delay of the inverter

We are now ready to calculate the delay of the inverter in order to distinguish between it and the delay of the interconnect which is our main concern.

Steps to calculate the delay

1. Run Layout Vs. Schematic (LVS) Check
2. Run Layout Parasitic Extraction (LPE) to extract the parasitic
3. Get the output file of the LPE in ".SPF" format
4. Back annotate the output file to the schematic.
5. Calculate the delay

The previous steps should be done again if anything changes in the layout.

Now let's see the results

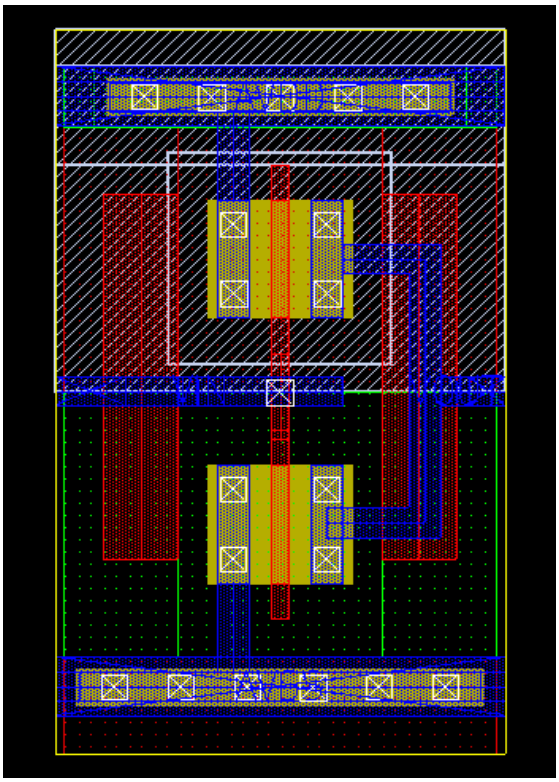


Figure 3.4.1 (c): Layout design of the inverter

Verification checks results (LVS, LPE)

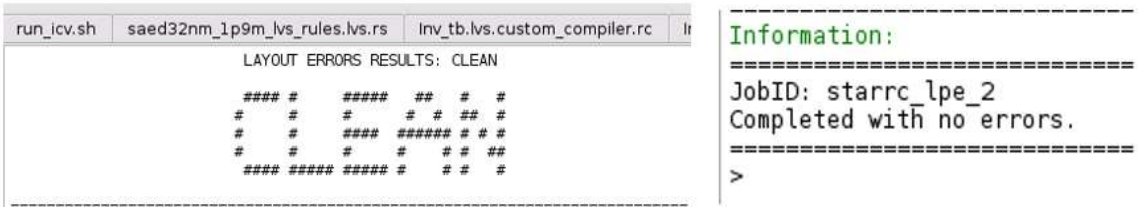


Figure 3.4.1 (d): LVS result (Left), LPE result (Right)

Results

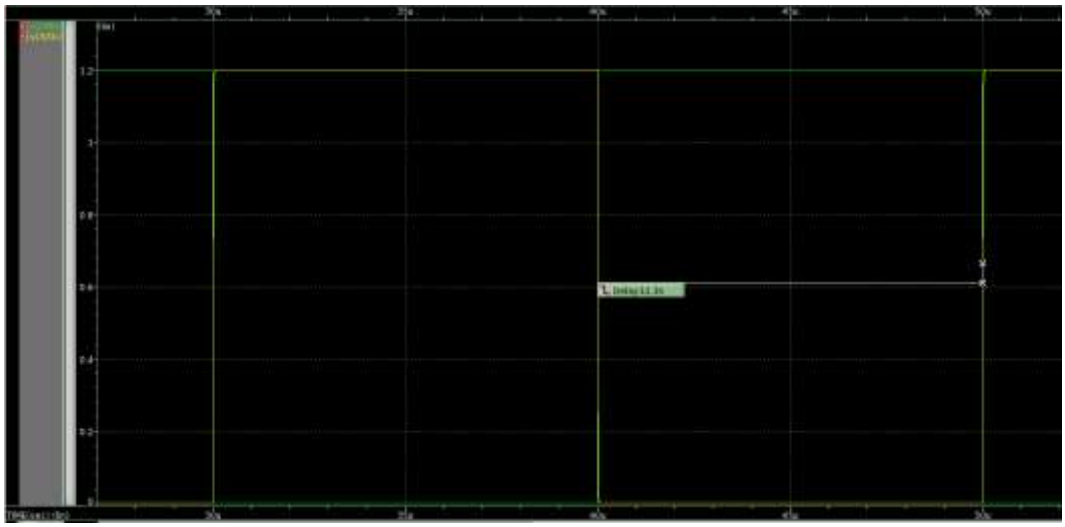


Figure 3.4.1 (e): Inverter Delay

The delay result is shown in Figure 3.4.1 (e)

$$Delay = 11.3\ ns$$

3.4.2 Two inverters (Buffer)

Layout of two inverter connected as a buffer

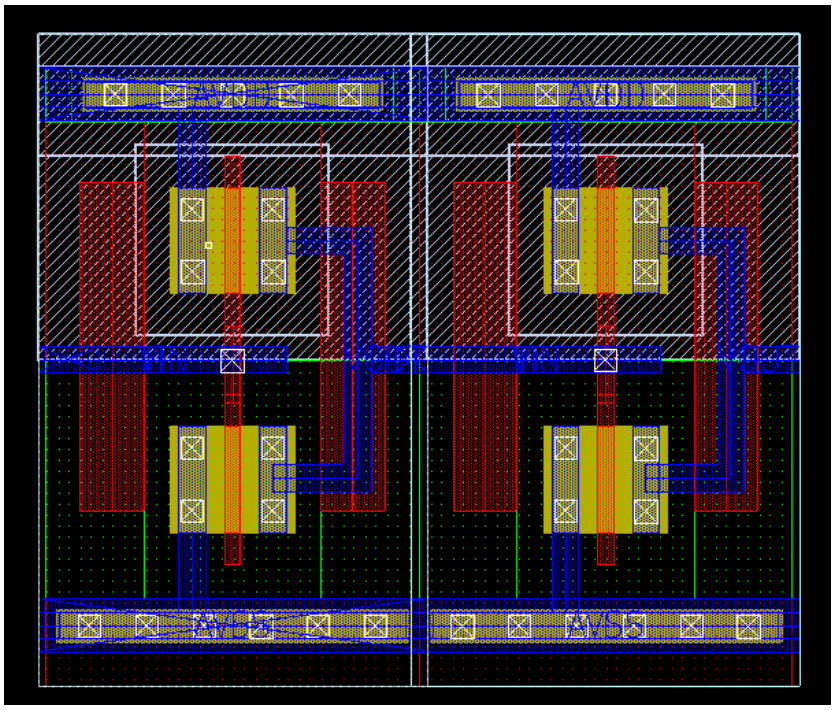


Figure 3.4.2 (a): Layout of two inverters (Buffer).

Now let's repeat the steps we mentioned in section 3.4.1 to calculate the delay.

Test bench to calculate the delay

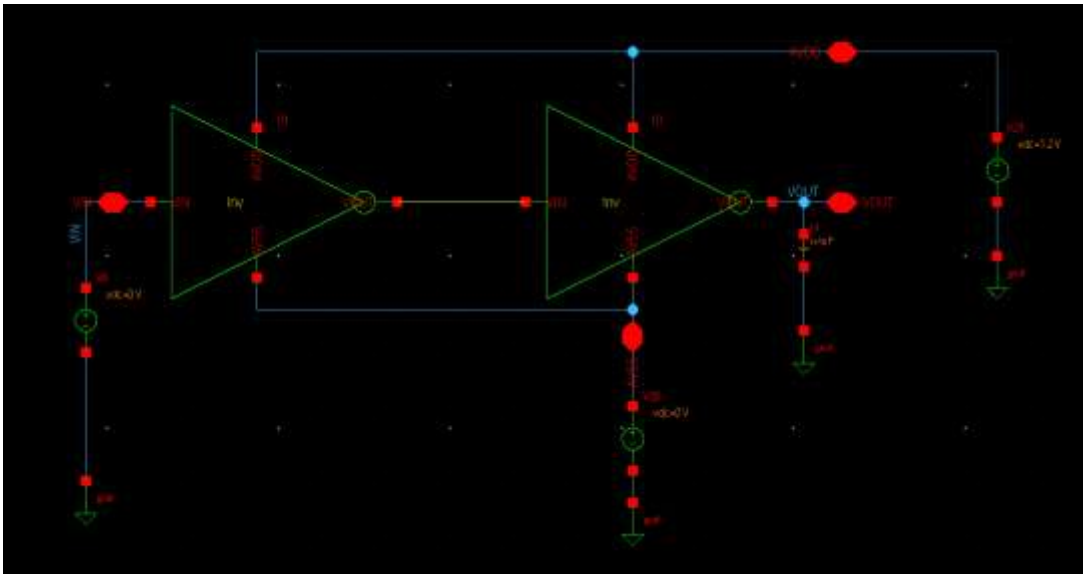


Figure 3.4.2 (b): Test bench to calculate the delay

Verification checks results (LVS, LPE)

Figure 3.4.2 (c): LVS result (Left), LPE result (Right)

Results

Figure 3.4.2 (d): Buffer Delay

As shown in Figure 3.4.2 (d)

$$Delay = 10.8\,ns$$

For clarification: The delay is smaller than the single inverter delay and that is because in the first case of a single inverter we modeled the load at the output with a capacitor C=1pf and that is much bigger than the capacitance of the inverter, we must assume a load at the output because that is the normal case, the interconnect should be connected to another device from the output end of the inverter which would introduce a load capacitance. And because the value assumed was a large value for a single inverter to load. after adding another inverter, the delay improved as expected: If we need to load a large capacitance, we should use an inverter chain. But we are not concerned about all of that, our main concern is the delay of the interconnect between the two inverters and that would be clear in the next test case.

3.4.3 Two inverters connected with a very long interconnect

Layout of two inverters connected with a very long interconnect

Figure 3.4.3 (a): Two inverters connected with a very long interconnect

Verification checks results (LVS, LPE)

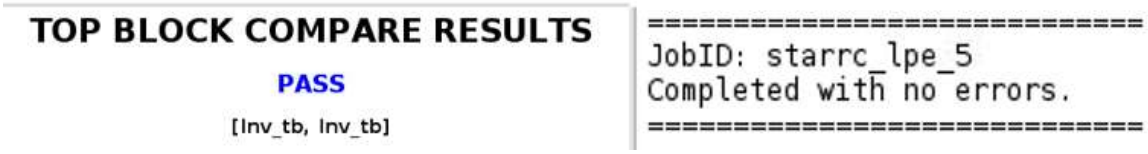


Figure 3.4.3 (b): LVS result (Left), LPE result (Right)

Results

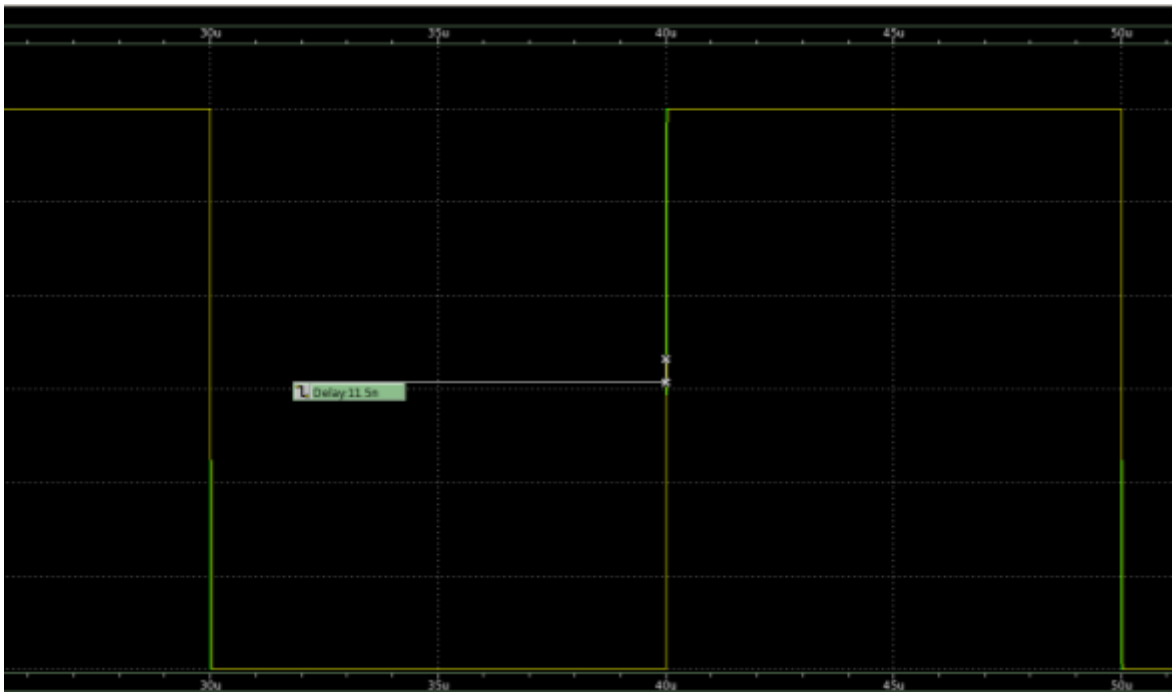


Figure 3.4.3 (c): Delay of two inverters connected with a very long interconnect

As shown in Figure 3.4.3 (c)

$$Delay = 11.5\ ns$$

Now the interconnect itself acts as a large capacitance load so the delay for the output load comes closer to the case of a single inverter loading a large capacitor. In the next 3 test cases we will see how the

techniques mentioned in section 3.3 impact the delay of the interconnect we will keep the distance between the two inverters constant and apply one technique only and measure the delay.

3.4.4 Using higher metal layers to improve the delay

In this case we will connect the inverters with a wire of the same dimensions as in section 3.4.3 but we will change the metal layer from M1 to M3

Layout of two inverters after connecting them with M3 instead of M1

Figure 3.4.4 (a): Layout of two inverters after connecting them with M3

Note: we used an array of vias to see the effect on the interconnect delay only and to avoid the bottleneck that could be introduced by the vias.

Verification checks results (LVS, LPE)

Figure 3.4.4 (b): LVS result (Left), LPE result (Right)

Results

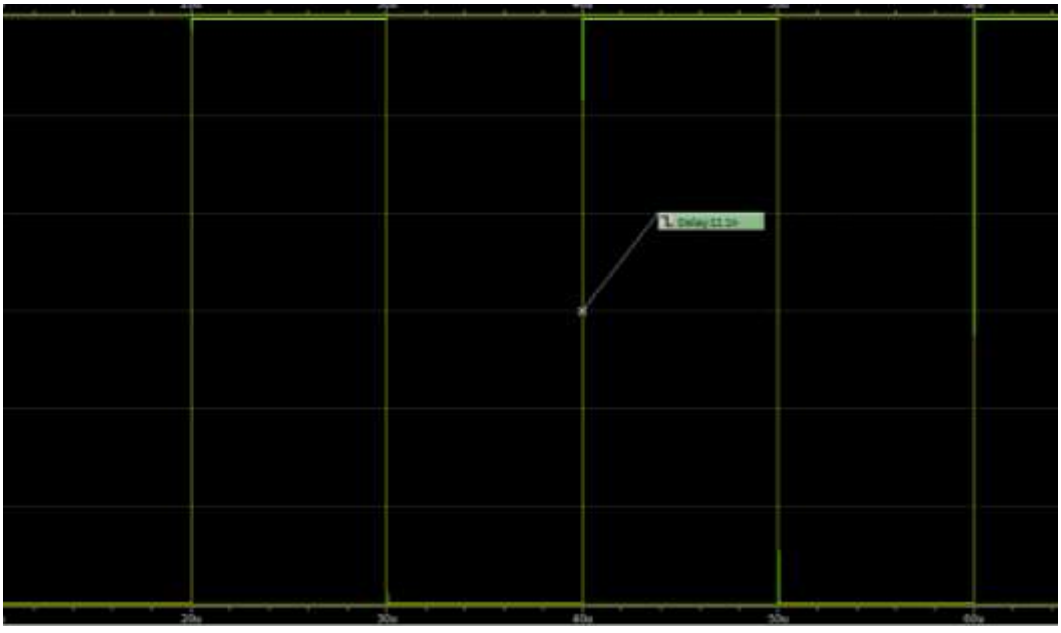


Figure 3.4.4 (c): Delay of two inverters connected with a very long interconnect

As shown in Figure 3.4.4 (c)

$$Delay = 11.1\ ns$$

3.4.5 Increasing the width of the interconnect to reduce the delay

Layout of two inverters after connecting them with wider M1 interconnect

Figure 3.4.5 (a): Layout of two inverters after increasing the width from $w = 0.05\mu m$ to $0.2\mu m$

Width increased from $W = 0.05\mu m \rightarrow 0.2\mu m$

Verification checks results (LVS, LPE)

Figure 3.4.5 (b): LVS result (Left), LPE result (Right)

Results

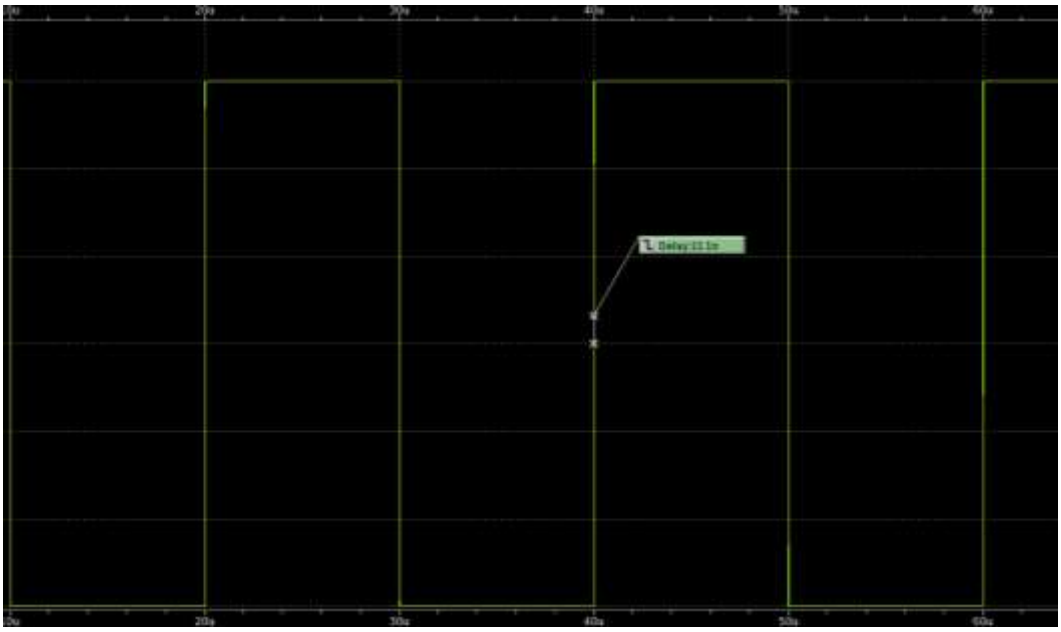


Figure 3.4.5 (c): Delay of two inverters after increasing the width $W = 0.05\mu m \rightarrow 0.2\mu m$

Exact Delay

delay(v(/VIN),v(/VOUT),0.6,0.6,3,3)	11.0780n

Figure 3.4.5 (d): Exact Delay of two inverters after increasing the width W=0.05μm→0.2μm

As shown in Figure 3.4.4 (c)

$$Delay \approx 11.1\ ns$$

3.4.6 Stacking metal layers to reduce the overall resistance and the delay

Layout of two inverters after connecting them with stack of metals from $M1 \rightarrow M3$

Figure 3.4.6 (a): Layout after using stack of metals from $M1 \rightarrow M3$ for connectiong

Verification checks results (LVS, LPE)

Figure 3.4.6 (b): LVS result (Left), LPE result (Right)

Results

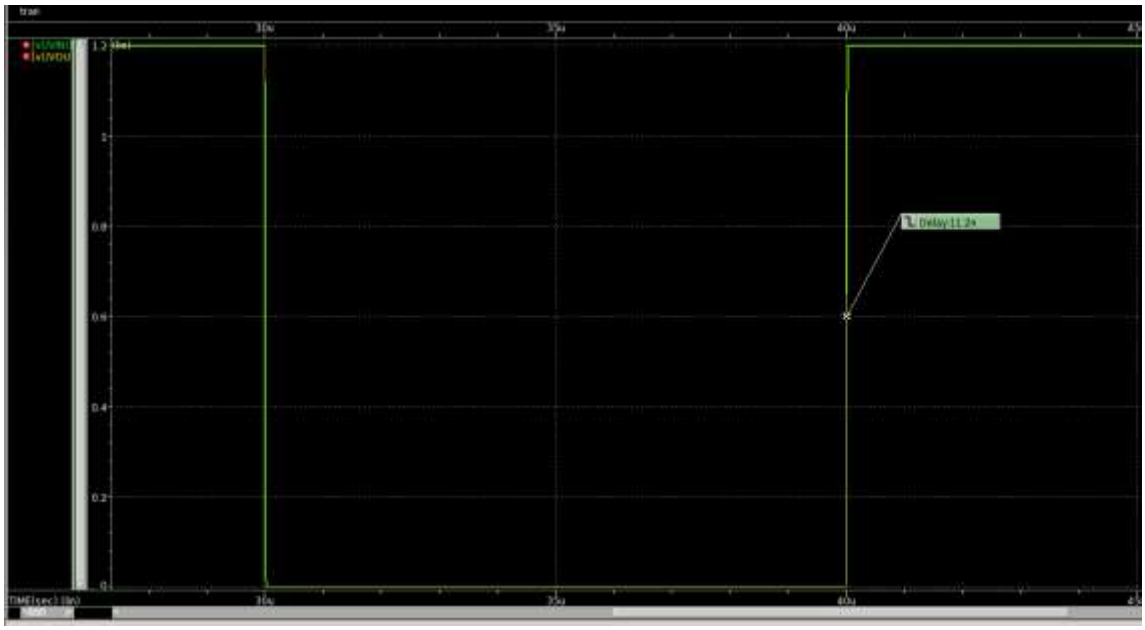


Figure 3.4.6 (c): Delay of two inverters after connecting them with stack of metals from $M1 \rightarrow M3$

Exact Delay

Figure 3.4.6 (d): Exact Delay of two inverters after connecting them with stack of metals from $M1 \rightarrow M3$

As shown in Figure 3.4.6 (c)

$$Delay \approx 11.2\ ns$$

$$Delay_{interconnect} \approx 11.2$$

3.4.7 Test cases results summary

$$Delay_{inverters} \approx 11\ ns$$

Metal layer used	Width (μm)	Measured Delay	Interconnect Delay
M1	0.05	11.5 ns	0.5 ns
M1	0.2	11.078 ns	0.078 ns
M3	0.05	11.1 ns	0.1 ns
M1, M2, M3	0.2	11.2 ns	0.2 ns

Table 3.4.7 (a): Test cases results

From Table 3.4.7a one can say that wire sizing is the best method for improving the delay because it has reduced the delay from 11.5 ns to 11.078 ns which is lowest delay achieved. However, this is valid only for this test case, if the original interconnect had different parameters (e.g., layer, width), we might find another technique can achieve better delay than wire sizing. But we have proved that all the techniques can improve the delay as expected and that was the main goal of the test cases. We have developed a tool that can find the best solution of these techniques based on the three techniques mentioned in section 3.3.

Note: The two inverters contribute with a delay of 11 ns approximately as calculated in 3.4.2.

3.5 RC Delay Improvement Tool

In this section we will talk about the tool in detail and how it applies the techniques mentioned in section 3.3, the delay is measured by placing the interconnect between the two inverters, and then calculate the total delay of the circuit.

The tool is a simulation-based tool that calculates the delay from simulation and then applies one of the techniques and save its delay and after several iterations that can be controlled by the user, the tool gets the minimum delay from the saved delay data and shows the best solution to the user.

The following is the basic flow diagram for the tool iterations.

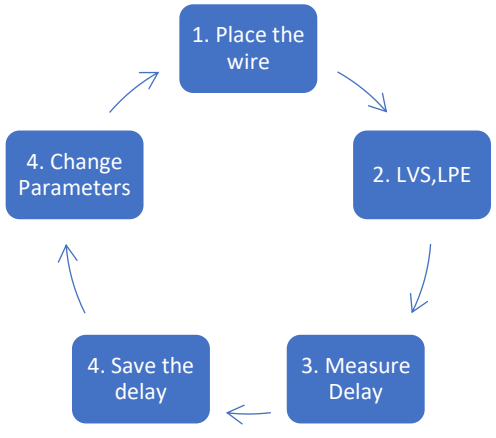


Figure 3.5 (a): Flow diagram of the RC Delay improvement tool

3.5.1 Tool rules for the inverter cell

We have talked about the basic flow diagram that the tool follows to find the best delay possible, we also mentioned that for the tool to calculate the delay, the interconnect is placed between two inverters and then the tool calculates the total delay of the circuit. But there are some rules the user must follow if he intends to use his own inverter cells instead of the ones integrated with the tool.

Rules

1. VIN, VOUT must be at $h/2$ from the bottom/top of the bounding box of height h.
2. The distance between the supply rails and the bounding box$Distance = h/2 - x$. Must bet entered by the user for the tool.
3. All pins (VIN, VOUT, VDD and VSS) must be created with M1.

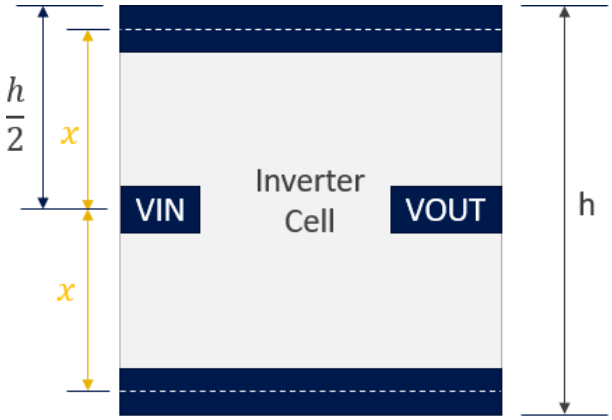


Figure 3.5.1 (a): Inverter cell dimensions rules

3.5.2 How the tool works.

Tool Graphical User interface (GUI)

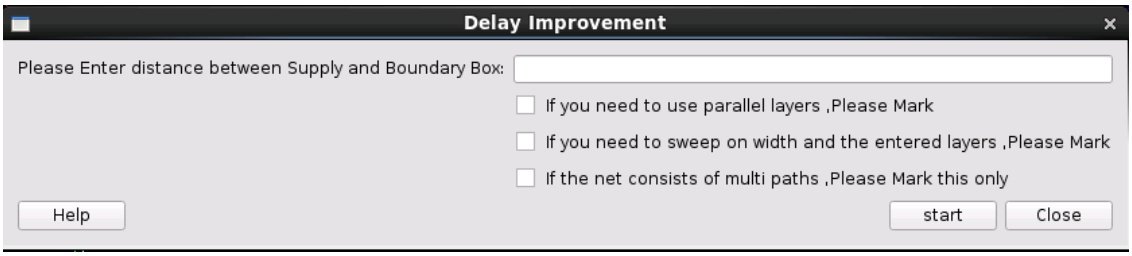


Figure 3.5.2 (a): RC Delay Improvement tool GUI

The tool has three main options: -

- **Changing metal layer and wire sizing**

1. Getting inputs from user (Critical net, Available layers, Maximum width, number of iterations, distance between the boundary box and the center of the supply rails)
2. The tool then gets the surroundings of the critical net to get an accurate value for the total capacitance on the net.
3. Place the interconnect between two inverters and apply a step at the input and measure the delay at the output of the whole circuit.
4. Save the delay of the original net that was measured in step 3
5. Change the width and measure the delay again.
6. Save the measured delay

7. If the number of iterations ended on this width, then the tool checks the available layers entered by the user and check if it is available and does not cause any type of conflict (e.g. short circuit) with any other net of the surroundings.
8. The tool repeats the iterations on the width for the new metal layer and saves the delay in each iteration.
9. After finishing all the iterations, the tool prints the best solution found from the saved data.

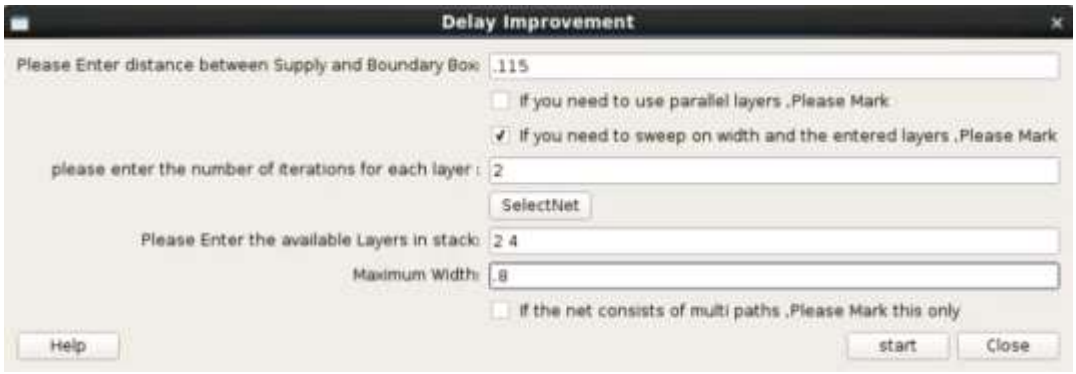


Figure 3.5.2 (b): Changing Metal Layer and Wire Sizing GUI

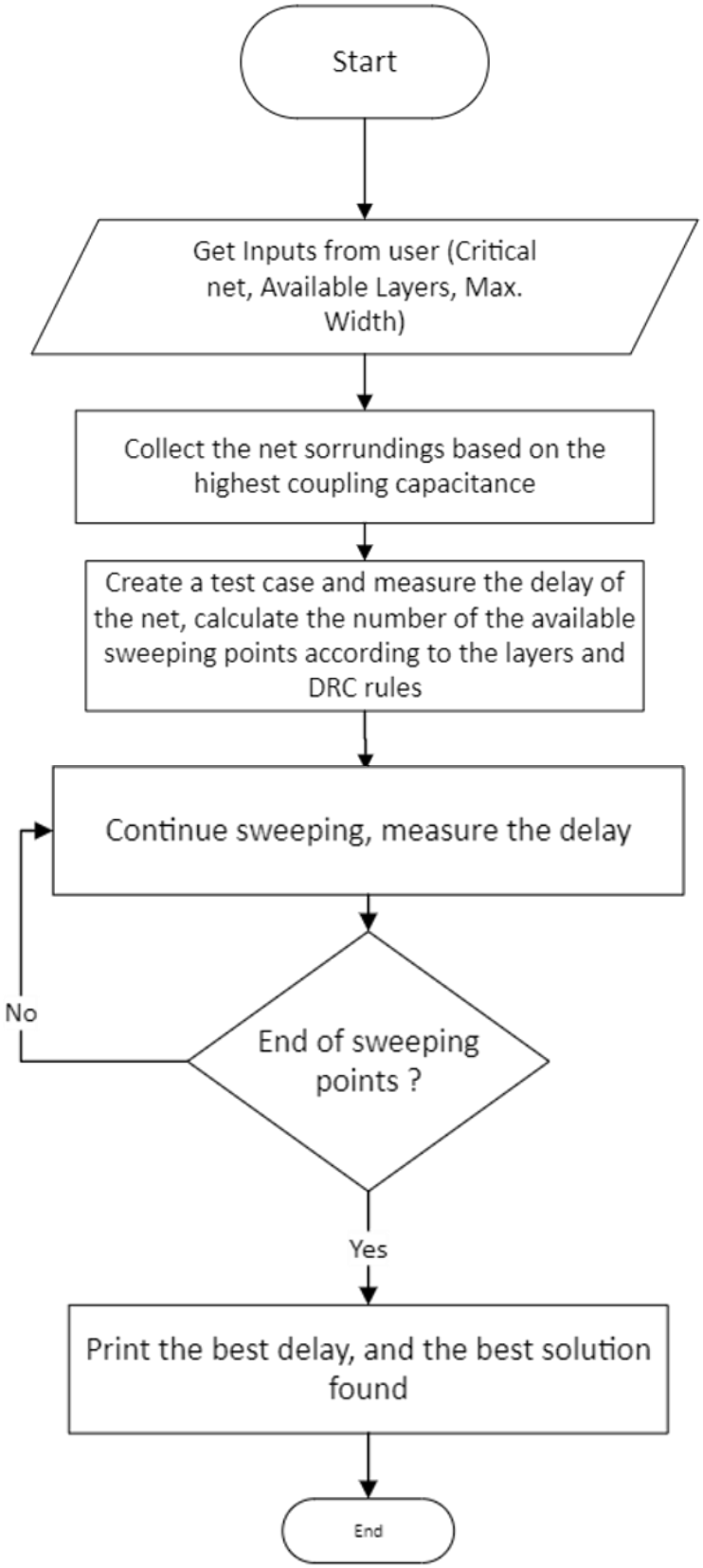


Figure 3.5.2 (c): Wire sizing and changing metal layers flowchart

Example

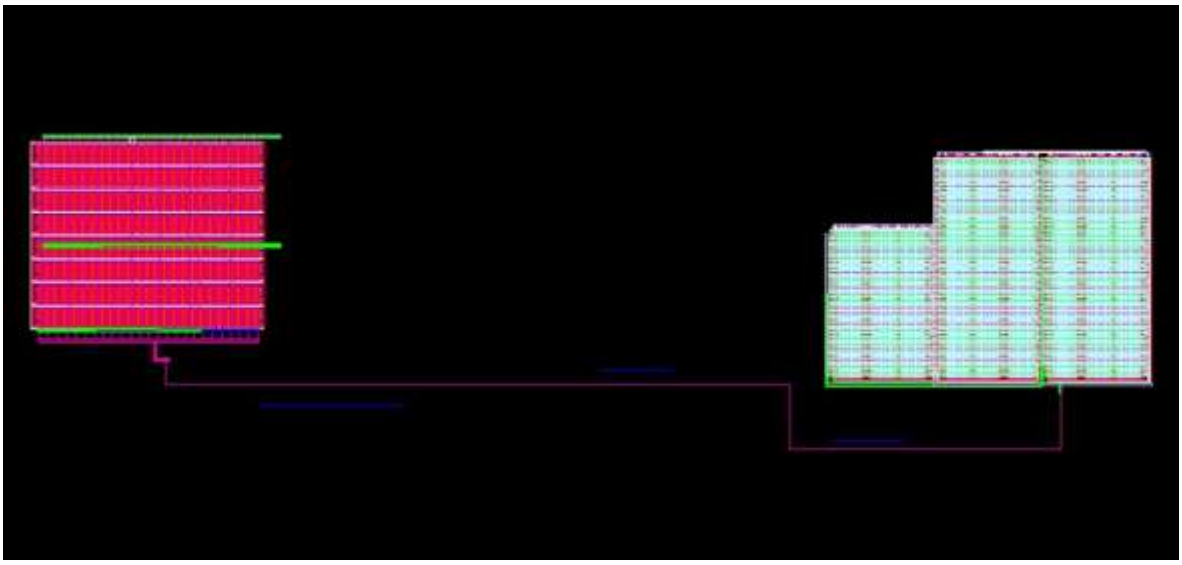


Figure 3.5.2 (d): Long interconnect between two blocks with dummy M1 surroundings

Example Results using Wire sizing and changing metal layers techniques.

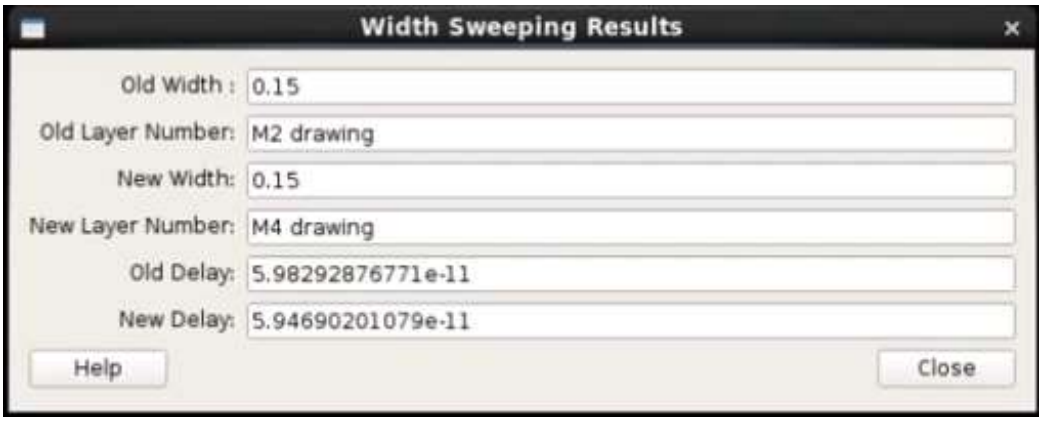


Figure 3.5.2 (e): Wire sizing and changing metal layers results

- **Stacking Metal Layers**

1. Getting inputs from user (Critical net, Available layers, Stacking width, number of iterations, distance between the boundary box and the center of the supply rails).
2. The tool then gets the surroundings of the critical net to get an accurate value for the total capacitance on the net.
3. Place the interconnect between two inverters and apply a step at the input and measure the delay at the output of the whole circuit.
4. Save the delay of the original net that was measured in step 3.
5. The tool then tries stacking different metal layers with the same width together to reduce the resistance.
6. Save the measured delay for each combination of metal layers.
7. After finishing all the combinations, the tool prints the best solution found from the saved data.

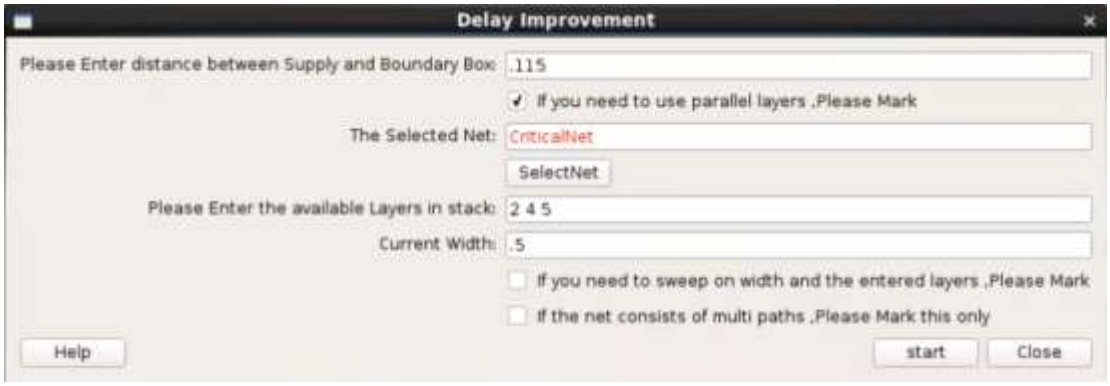


Figure 3.5.2 (f): Stacking metal layers option GUI

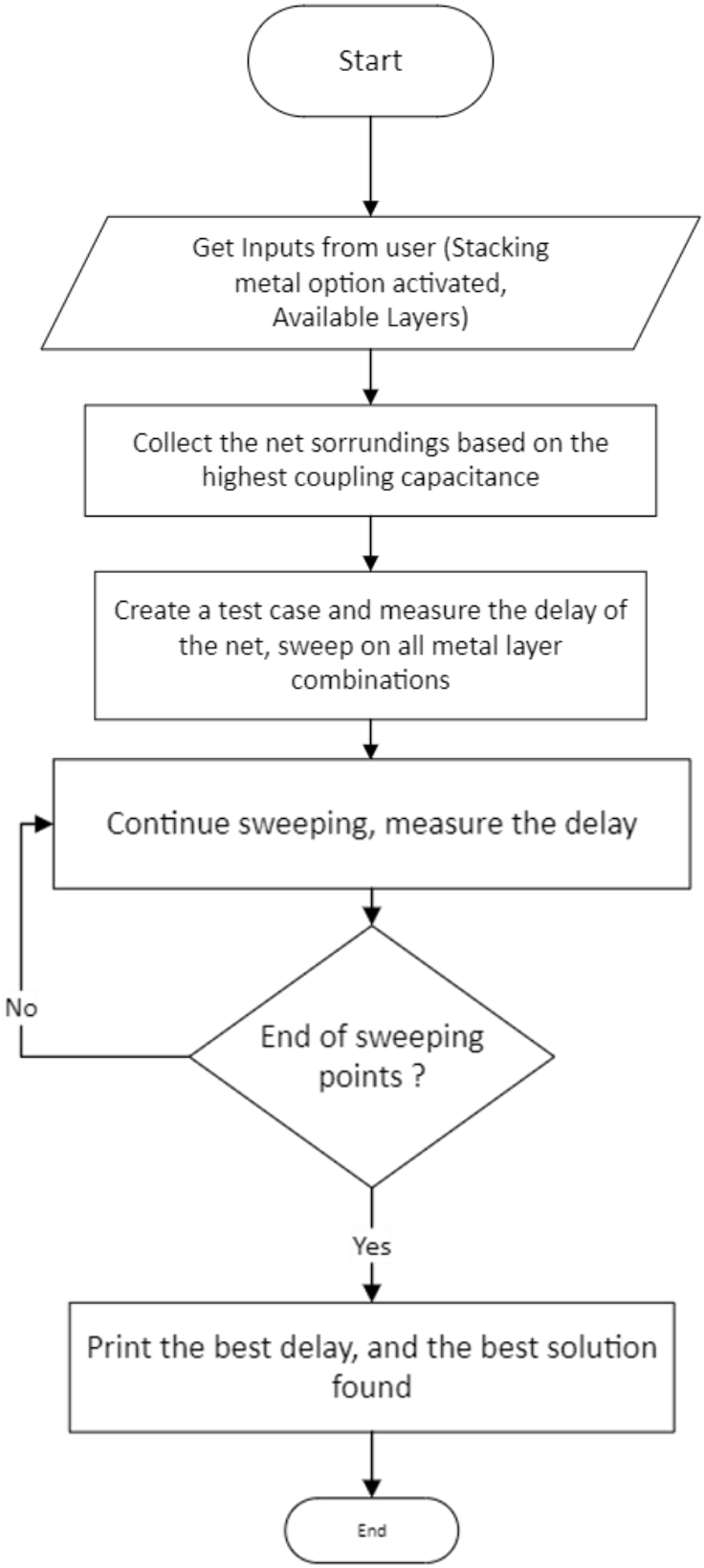


Figure 3.5.2 (g): Stacking Metal layers flowchart

Example Results using Stacking metal layers technique.

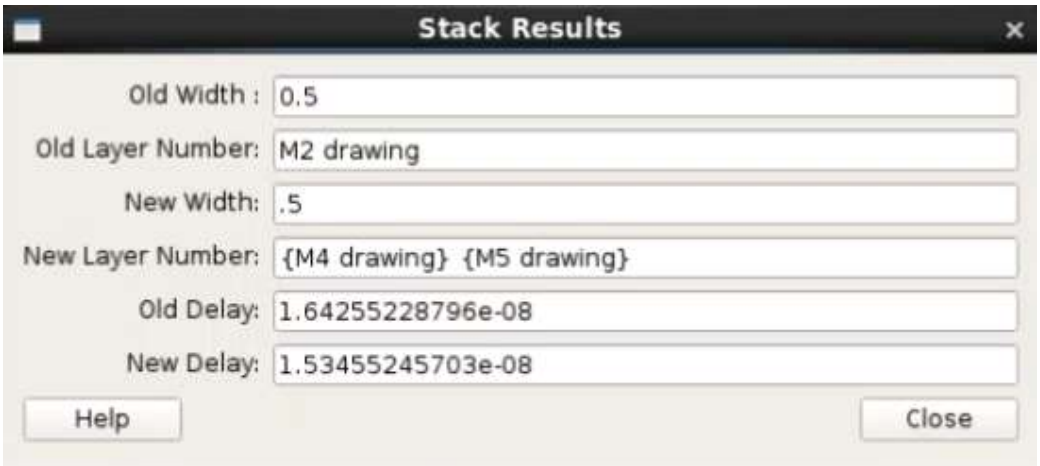


Figure 3.5.2 (h): Stacking metal layers results

- **Interconnect with bridges (multi paths interconnect)**

Example of an interconnect with bridges

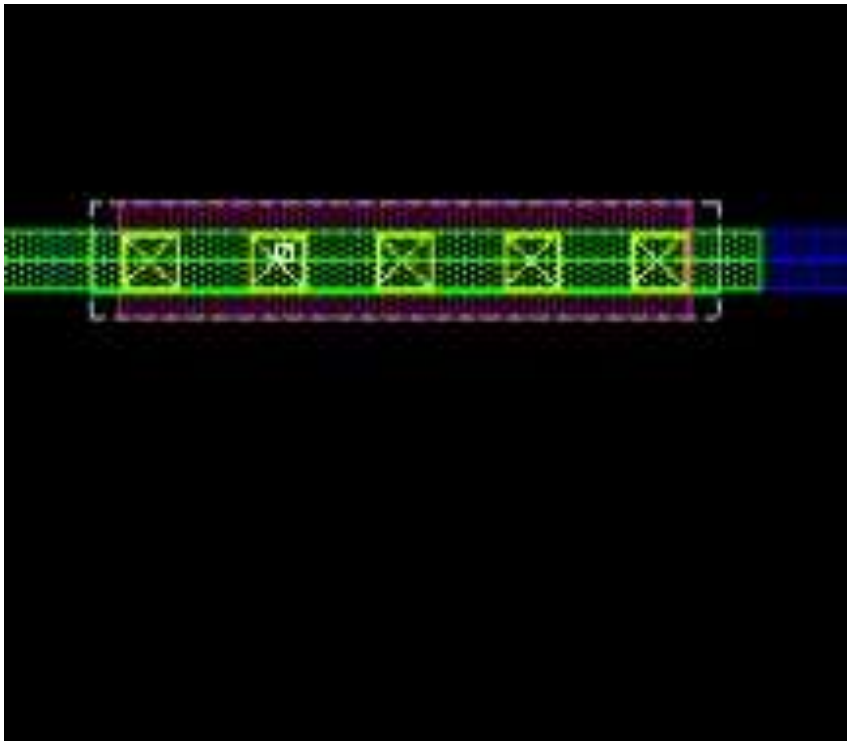


Figure 3.5.2 (i): Interconnect with bridges

1. Getting inputs from user (Critical net, Maximum width, number of iterations, distance between the boundary box and the center of the supply rails).
2. The tool then gets the surroundings of the critical net to get an accurate value for the total capacitance on the net.

3. Place the interconnect between two inverters and apply a step at the input and measure the delay at the output of the whole circuit.
4. Save the delay of the original net that was measured in step 3.
5. The tool then iterating on one path only and setting the other paths width to w= Maximum Width.
6. Save the measured delay for each combination of metal layers.
7. After finishing all the combinations, the tool prints the best solution found from the saved data.

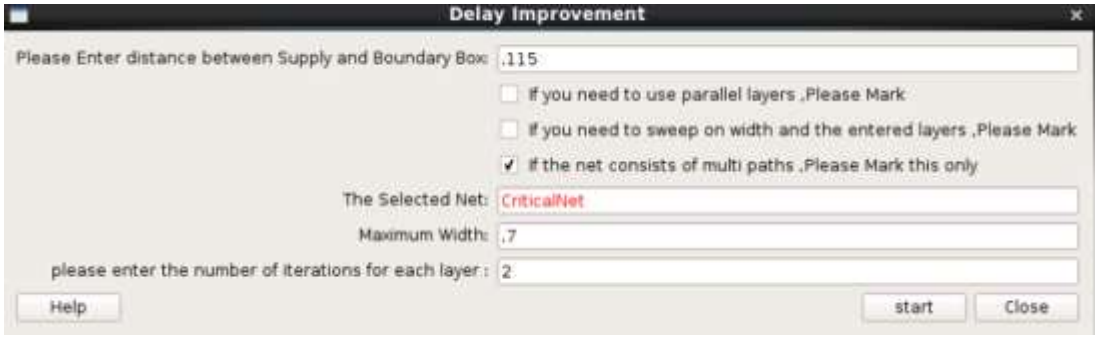


Figure 3.5.2 (j): Multipaths interconnect option GUI

The tool follows the flowchart in Figure 3.5.2c to find the best width for each path and then after finishing iterations assign the best width to its path and then iterate on the next path until it covers all the paths in the interconnect, however this solution was not improving the delay so in future work we can change the metal layers while iterating on the width at the same time in order to improve the delay of the interconnect.

3.6 Shielding Tool

3.6.1 Introduction

Technology scaling results in reduction of dimensions of transistors and interconnects. Crosstalk reduction in VLSI interconnect has become more important for high speed circuit design.one of the most important solutions to reduce crosstalk is Shielding as it is an effective and common technique to deal with signal integrity issues such as crosstalk noise and delay uncertainty. The basic idea of shielding is to reduce capacitive and inductive coupling effects [8].

3.6.2 Capacitive coupling

Capacitive coupling effect between two interconnects has become the major concern in Deep Sub-Micron technology as the thickness of the interconnect is greater than interconnect width, and the spacing between wires is very small as shown in Figure 3.6.2(a). So, the aggressive technology scaling is leading to an increase in coupling capacitance between interconnects.

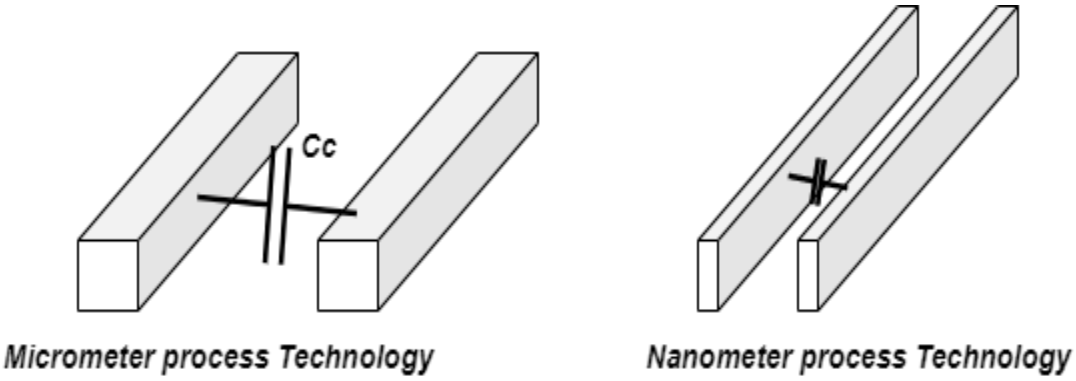


Figure 3.6.2(a) Decreasing in wire geometries in the nanometer process technology leads to an increase in coupling capacitance.

Due to coupling capacitance if there is a switching in a net in the design, this switching may affect the other nets that are in close physical proximity. The net under this effect is called a victim, and the switching net is called an aggressor. In Figure 3.6.2(b) when the aggressor transition occurs as the signal value changed from 1 to 0 as a step, there is a bounce in the voltage of the victim signal “pull down” due to the leakage current flowing through the coupling capacitance (Cc). This glitch in the victim signal due the aggressive transition is called coupling noise pulse.

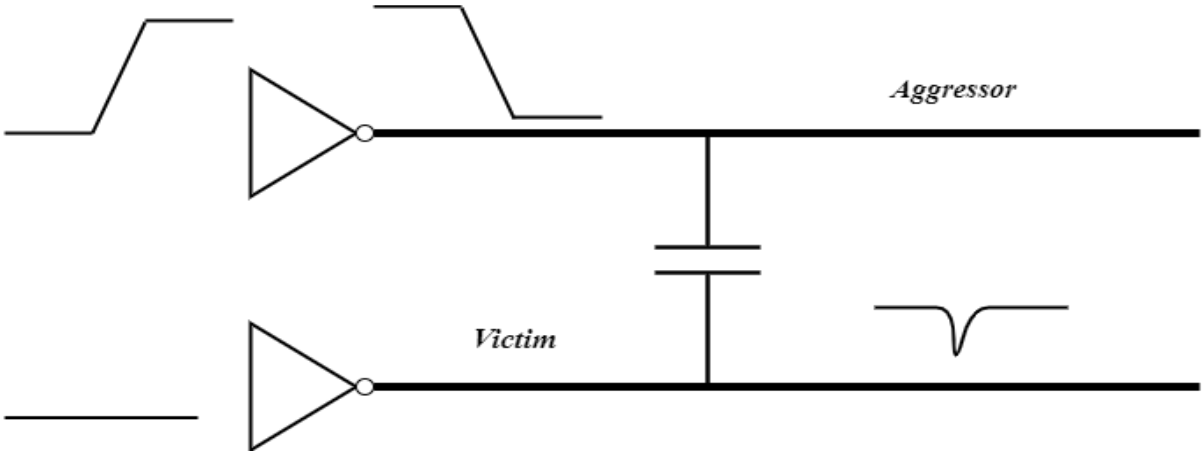


Figure 3.6.2(b) Victim glitch due to aggressor transition

Usually the coupling noise pulse occurs when the aggressor transition is completed and there is no leakage current flowing through the coupling capacitance. Finally, this noise dies down after the aggressor transition is vanished and the victim discharges the accumulated charge [16].

This change in the victim signal can affect the performance of the design. if the height of the glitch is in the range of noise margin, this glitch can be considered a safe glitch. if the height of the glitch is out of the range of noise margin this can affect the performance of the design

There is another scenario, when both victim and aggressor are switching at the same time. This scenario is leading to a change in the timing of signal transition, called delay uncertainty, occurs in the victim lines [9]. If the victim and the aggressor are switching in opposite directions. The aggressor is switching from high to low and the victim is switching from low to high as shown in Figure 3.6.2(c), the coupling noise can slow the victim's direction. on the other hand, if they are switching in the same direction then the coupling noise can speed up the victim transition [16].

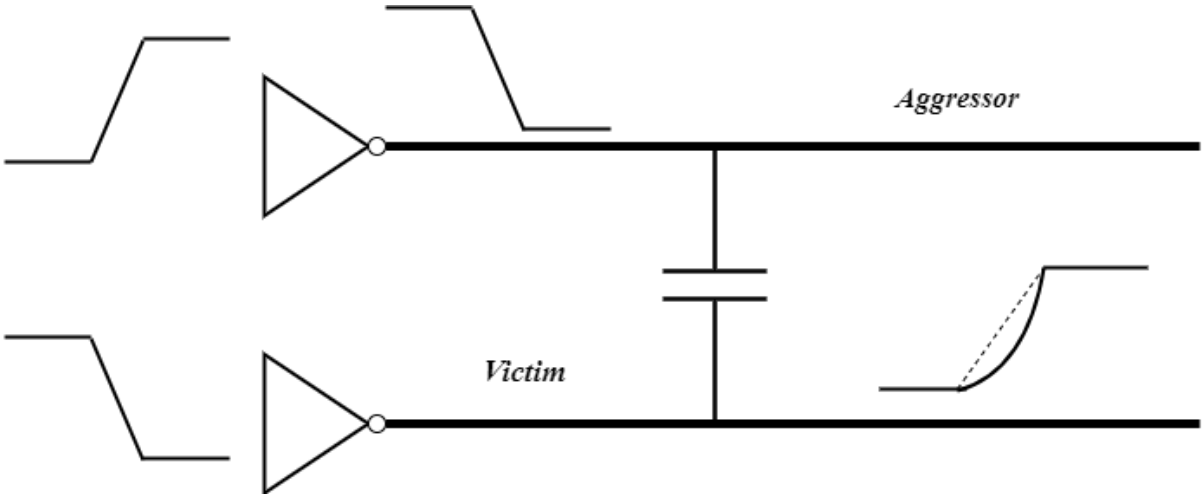


Figure 3.6.2(c) Both victim and aggressor are switching in opposite direction

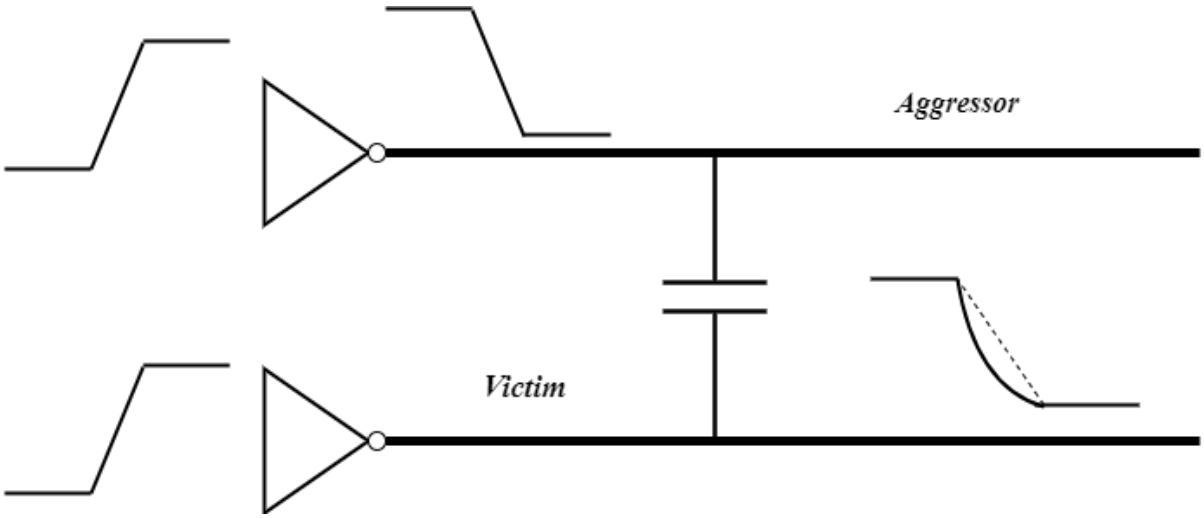


Figure 3.6.2(d) Both victim and aggressor are switching in the same direction

3.6.3 Solutions to reduce crosstalk effects

To reduce the effects of crosstalk there are some solutions that the designer can use. As mentioned to reduce the crosstalk effects. It is required to reduce the coupling capacitance. There are two commonly used techniques to reduce the coupling effect:

1. Increase the spacing between the two interconnects (Spacing) as shown in Figure 3.6.3(a)
2. inserting a shield line (shielding)

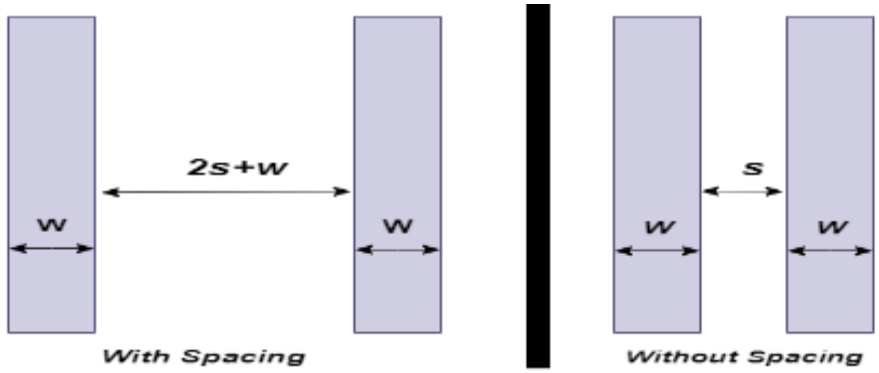


Figure 3.6.3(a) Increasing in spacing reduce the coupling capacitance

There are also alternative methods to reduce crosstalk effects:

1. If the victim's length is too long. it is required to insert a buffer
2. If the aggressor and the victim are in the same metal layer. it is better to use a different metal layer.
3. Use Manhattan routing rule to reduce the common area between metal layers. For example, if Metal 1 is routed in horizontal direction. Is required to route M2 in vertical direction as shown in Figure 3.6.3(b)

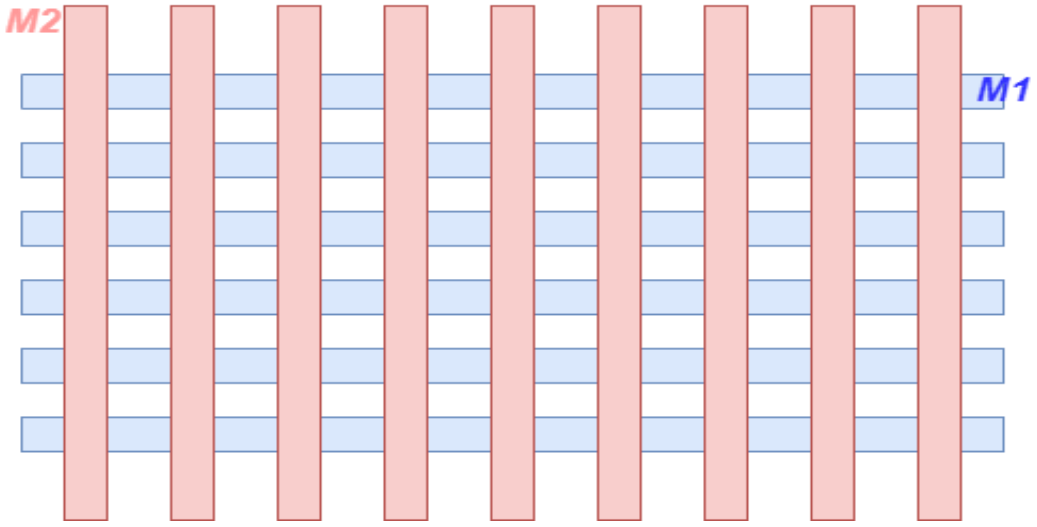


Figure 3.6.3(b) Manhattan routing rule

In this thesis, we will discuss Shielding and its types and how shielding can be a good solution to avoid crosstalk by reducing the capacitive coupling noise and one of the important benefits of shielding is to reduce inductive coupling noise.

3.6.4 Basic idea of Shielding

The basic idea of the Shielding is to reduce the coupling capacitance and inductance between two wires one of them is an aggressor and the other is a victim. Shielding is done by inserting a wire connected to the power signal VDD/Ground.

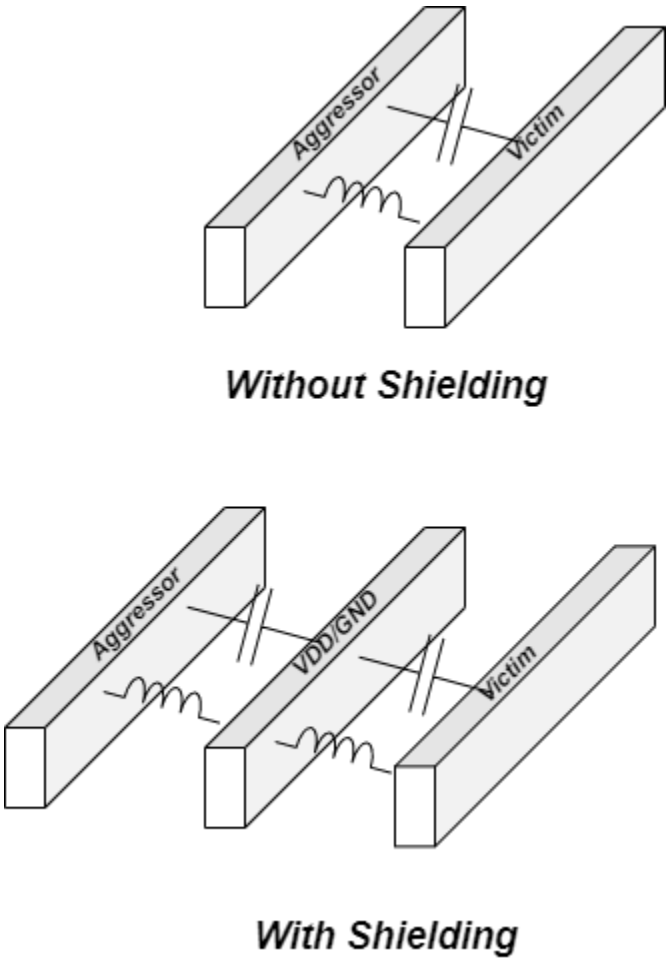


Figure 3.6.4(a) Shielding reduce the coupling capacitance and inductance

As shown in Figure 3.6.4(a) there is a shielding interconnect that is inserted between the aggressor and the victim. Coupling capacitance between the victim and the aggressor disappeared and was replaced by a coupling capacitance between the signal and shield line. Shield line prevents the switching effect of the close nets to affect the sensitive net. Shield insertion can also reduce the inductive coupling between the signal lines by providing a closer current return loss path for both the aggressor and the victim lines [7]. The mutual inductive effect is reduced with shield insertion compared to spacing technique. We can say that with shield insertion the inductive coupling is reduced and is not eliminated because the mutual inductive still exists between the aggressor and the victim.

3.6.5 Shielding Parameters

In high speed circuits it is required to get the best effectiveness of shielding to reduce the crosstalk between the close nets that can affect the performance of the design. In this section we will discuss what factor and parameter and how large these factors and parameters have impacts on the shielding effectiveness of the victim lines need to be figured out. According to [7] [8][9] there are some parameters that can affect the effectiveness of the shielding such as:

- Geometric characteristics of the shield lines and signal lines (aggressor and victim)
- Spacing between the shield lines and signal lines
- The number of connections that tied the shield line with power signal VDD/GND
- Shield material

A. Geometric characteristics of the shield lines and signal lines

The coupling noise for shielded lines is increased when the signal length increases and decreases when the signal width increases as shown in Figure 3.6.5(a) and Figure 3.6.5(b) .

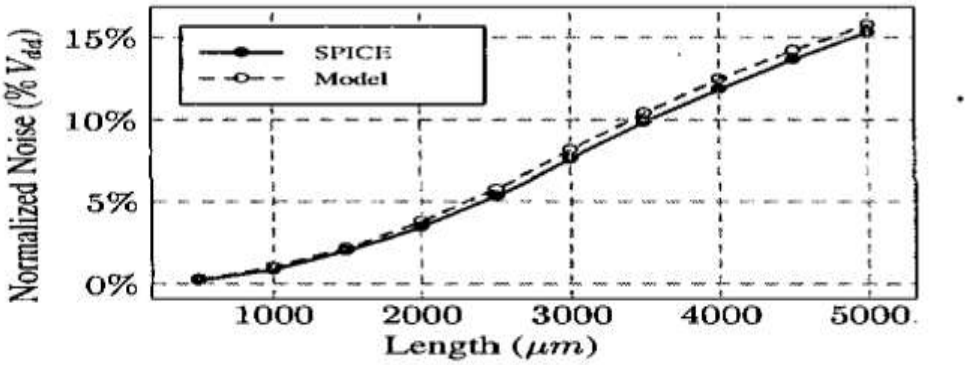


Figure 3.6.5(a) Crosstalk noise characteristics in term of length of signal line

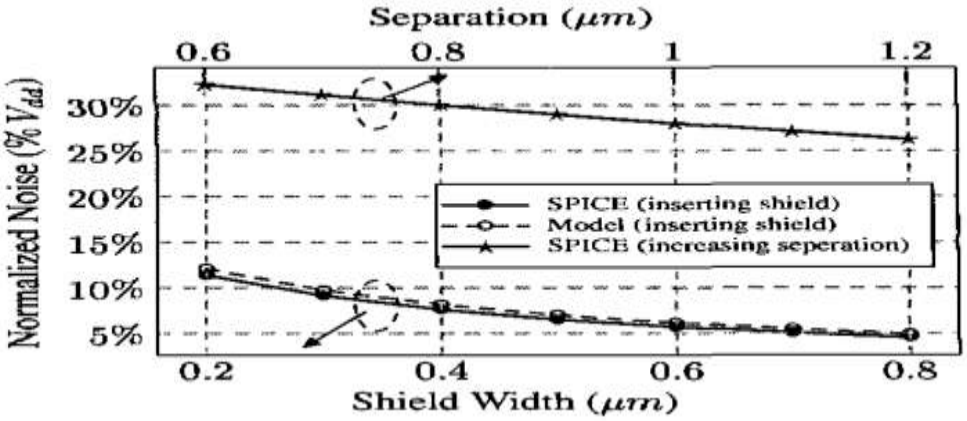


Figure 3.6.5(b) Crosstalk noise characteristics in term of width of signal line

B. Spacing between the shield lines and signal lines

Spacing is one of the most important parameters that affect crosstalk noise. When Spacing increases between the shield line and signal lines, crosstalk noise decreases. increasing the spacing between aggressor and the victim has the same effect on the coupling noise as shown in Figure 3.6.5(b).

C. Number of Ground Connections

When connecting the shield line with ground, it is not considered as an ideal ground as there is a parasitic resistance of the shield line. This resistance causes noise to couple to the victim line, so we need to connect many ground connections to reduce parasitic resistance and therefore, reduce the coupling noise as shown in Figure 3.6.5(c) .

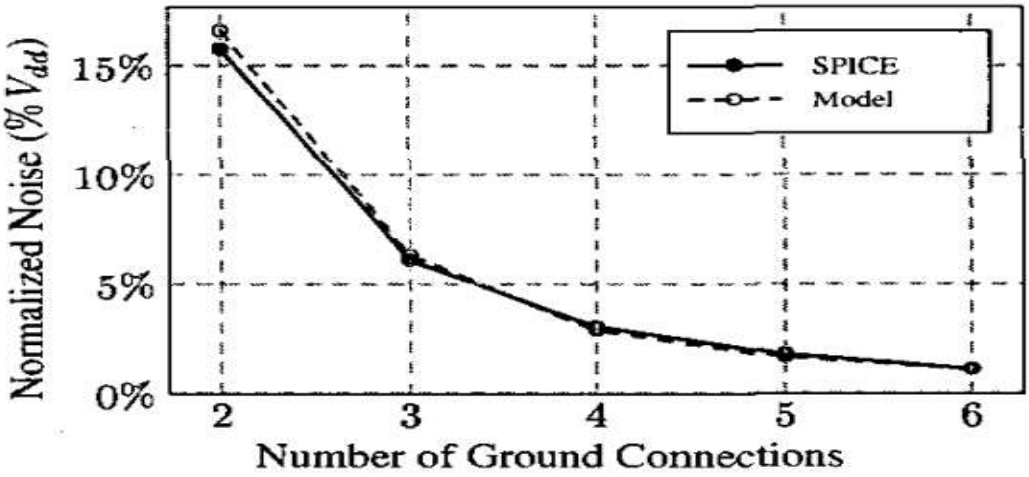


Figure 3.6.5(c) Crosstalk noise characteristics in term of number of ground/power line connections

D. Shield material

Crosstalk noise is affected by shield material. Different shield materials have different resistances therefore when the resistance of the shield line decreases the crosstalk noise decreases. There is a comparison between copper and aluminum. As we know the resistivity of the copper is lower than the resistivity of the aluminum so crosstalk noise with a shield line of copper is lower than aluminum one Figure 3.6.5(d) .

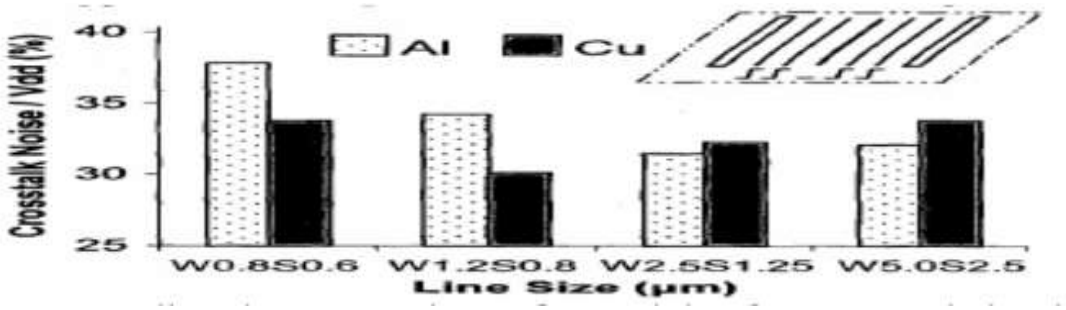


Figure 3.6.5(d) Crosstalk noise comparison of materials of copper and aluminum

3.6.6 Shielding Styles

According to the position of the victim and the aggressor. We can select the best shield style to reduce the coupling noise as much as possible. There are three basic styles of shielding as following:

- Parallel (Horizontal)
- Tandem (Vertical)
- Coaxial (All-Around)

A. Parallel

We can use this style when the aggressor and the victim are routed with the same layer. the designer can choose the best value for the shield line width and the spacing between the shield line and the signal lines as shown in Figure 3.6.6(a) . Shielding can be on the right , left or both sides.

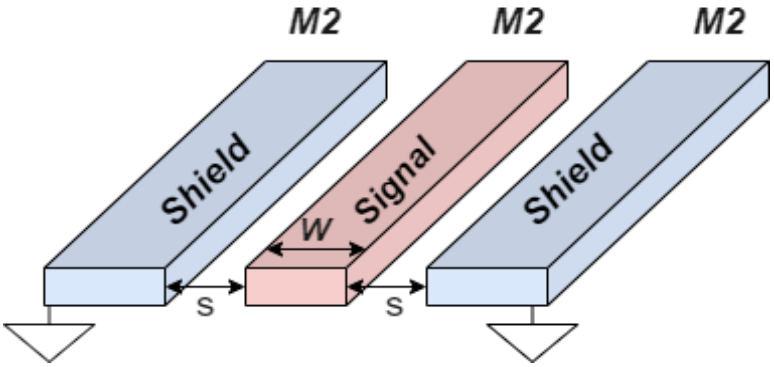


Figure 3.6.6(a) parallel style of shielding

B. Tandem

Tandem style is used when the aggressor is routed in a different layer from the victim layer. The aggressor can be above or below the victim. The shield layer can be Top, Bottom or both sides as shown in Figure 3.6.6(b).

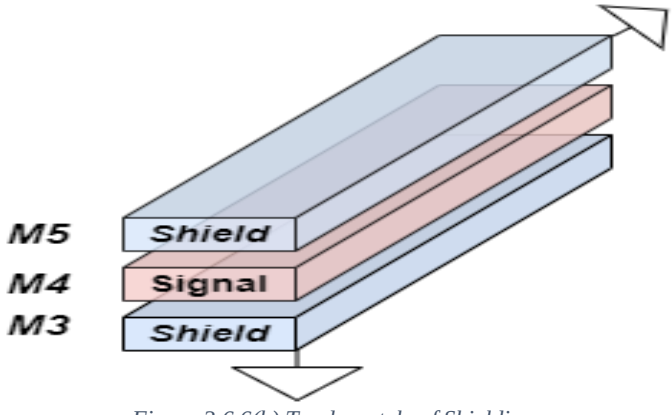


Figure 3.6.6(b) Tandem style of Shielding

C. Coaxial

Coaxial style is a combination of parallel and tandem. It wraps around the signal on all four layers. Coaxial style has Three Types:

- Solid in Figure 3.6.6(c)
- Split in Figure 3.6.6(d)
- Center-Only in Figure 3.6.6(e)

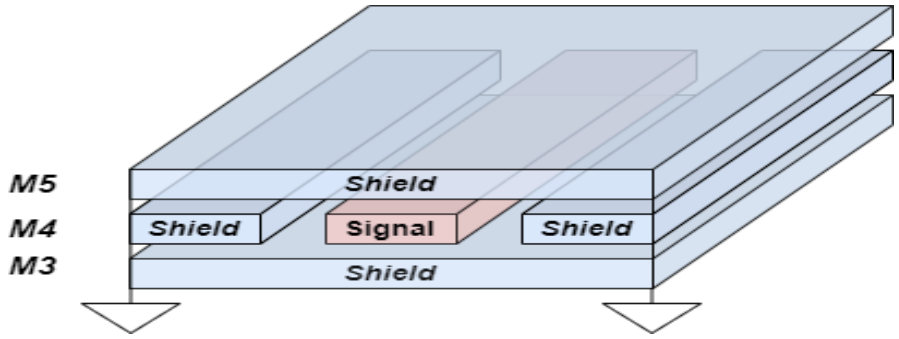


Figure 3.6.6(c) Solid type of Coaxial style Shielding

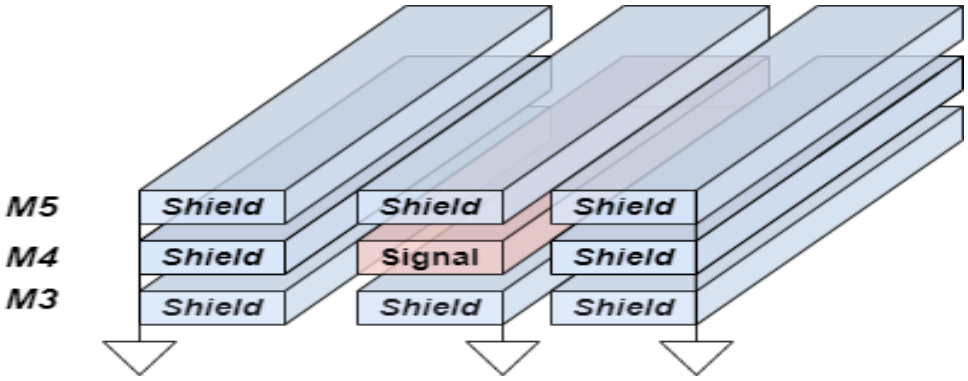


Figure 3.6.6(d) Split type of Coaxial style Shielding

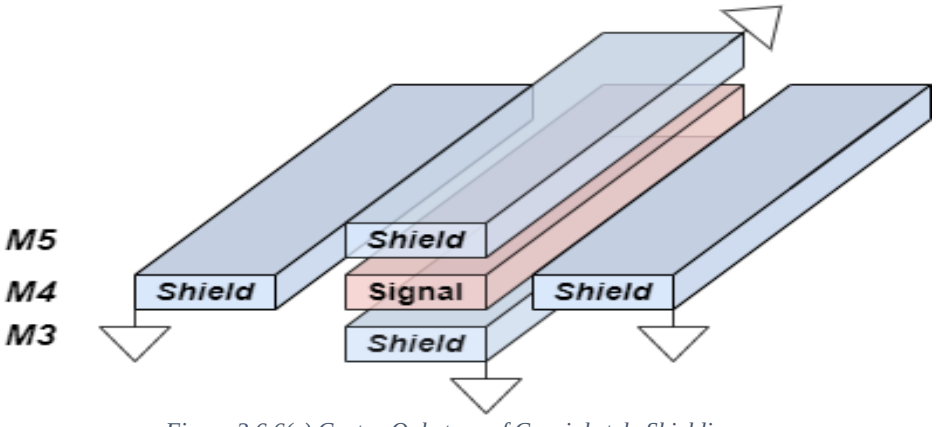


Figure 3.6.6(e) Center-Only type of Coaxial style Shielding

3.6.7 Shielding Tool Overview

Shielding tool is designed with simple GUI that helps the user to shield the sensitive signals with easy way

Figure 3.6.7(a) Shielding tool GUI

3.6.8 Flow Chart

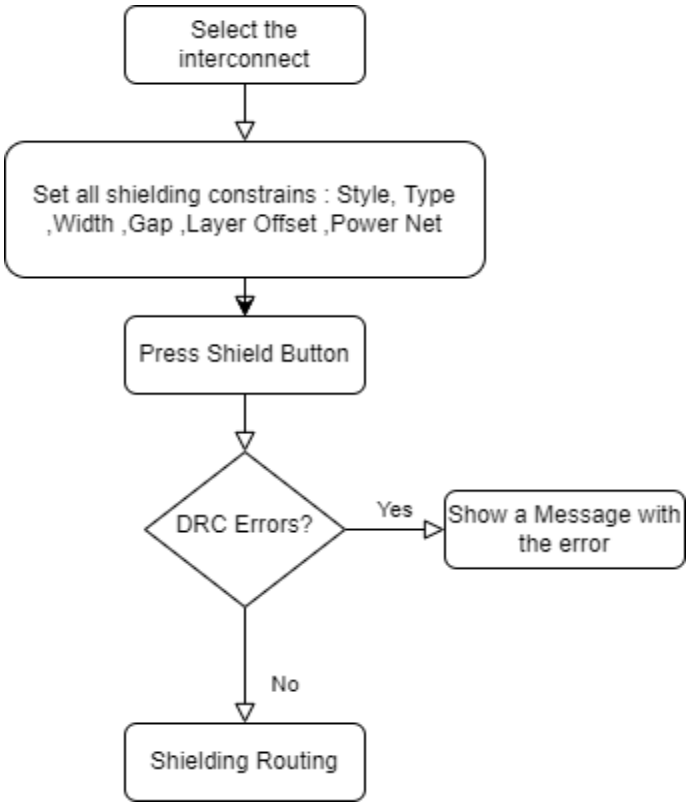


Figure 3.6.8(a) Shielding tool flow chart

3.6.9 How the tool Works

The designer can use the Shielding tool in an easy way. there are some steps to use Shielding tool without errors or warnings:

- The tool starts with the GUI in Figure 3.6.9(a) with default constraints.
- The designer can select the sensitive signal that will be shielded by pressing on the arrow button. GUI will disappear and the current design will be opened. then select the signal line, instantaneously the GUI will appear again with the name of the signal net.
- Select the shield style from the style group {Parallel, Tandem, Coaxial}. then select the Style type
- In case of Parallel or coaxial style, Choose a convenient width for shield line and a suitable distance between the shield line and signal line
- In the case of Tandem or coaxial style, Choose the layer index that selects which metal layer will be above or below the signal line. For example, if the signal line is routed with M3 if the user selects the top offset = 1 and bottom offset = 1 the shielding tool will route with M4 above the signal line and M2 below the signal line.
- Select the signal that the shield line will be tied with Power/Ground
- Press the Shield button if there are no errors the shielding will be done. But if there are DRC error warning message will appear

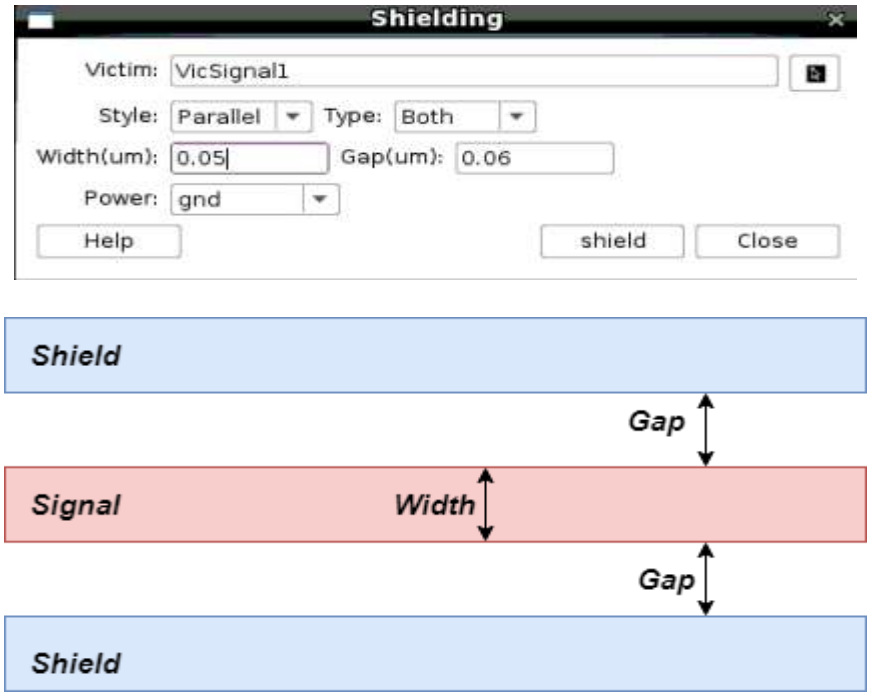


Figure 3.6.9(a) Shielding dimensions.

3.6.10 Test cases with Shielding tool

A. Test case 1

This is a simple case: both victim and aggressor are in parallel in the same metal layer Figure 3.6.10(a). It is required to shield the victim signal with parallel style

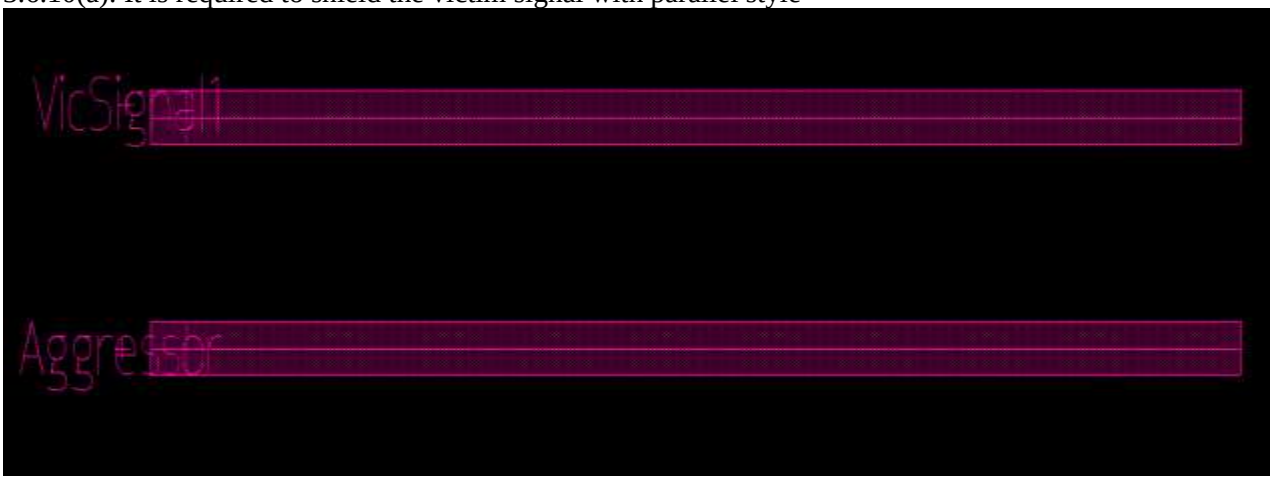


Figure 3.6.10(a) Both victim and aggressor are in parallel in the same metal layer

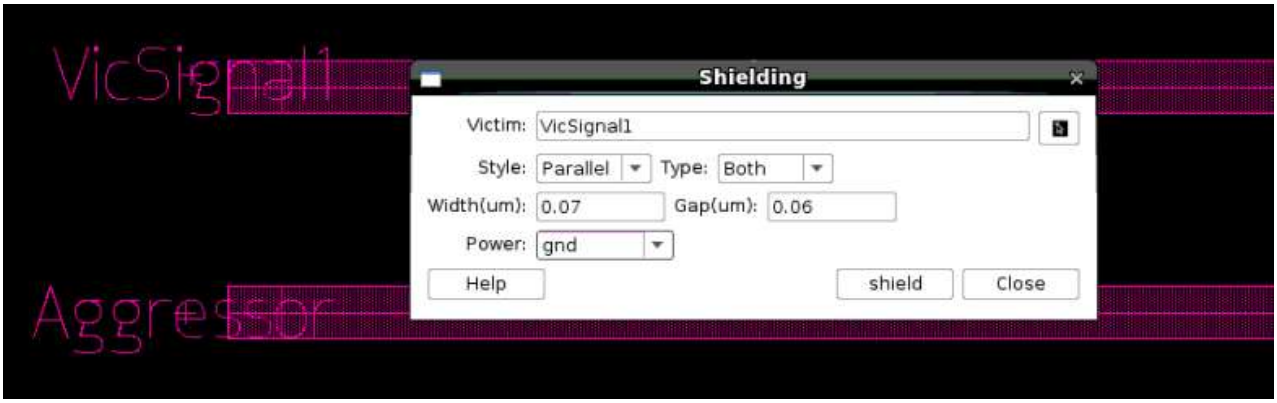


Figure 3.6.10(b) Shielding constraints for test case 1

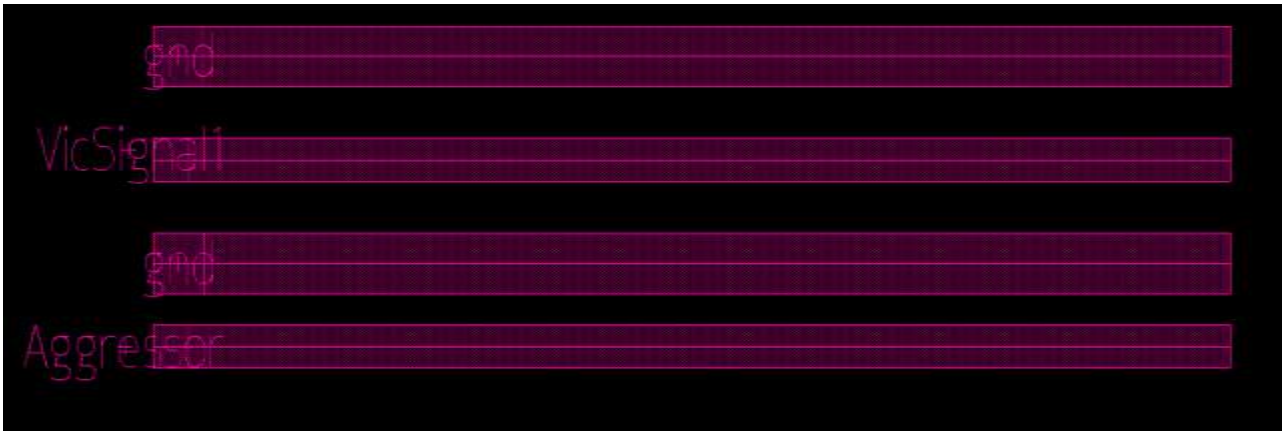


Figure 3.6.10(c) Test case1 results

B. Test case 2

In this case: victim signal is a line with multi corners Figure 3.6.10(c). It's required to be shielded with Coaxial shielding with Solid type. this case is a combination between parallel and tandem styles

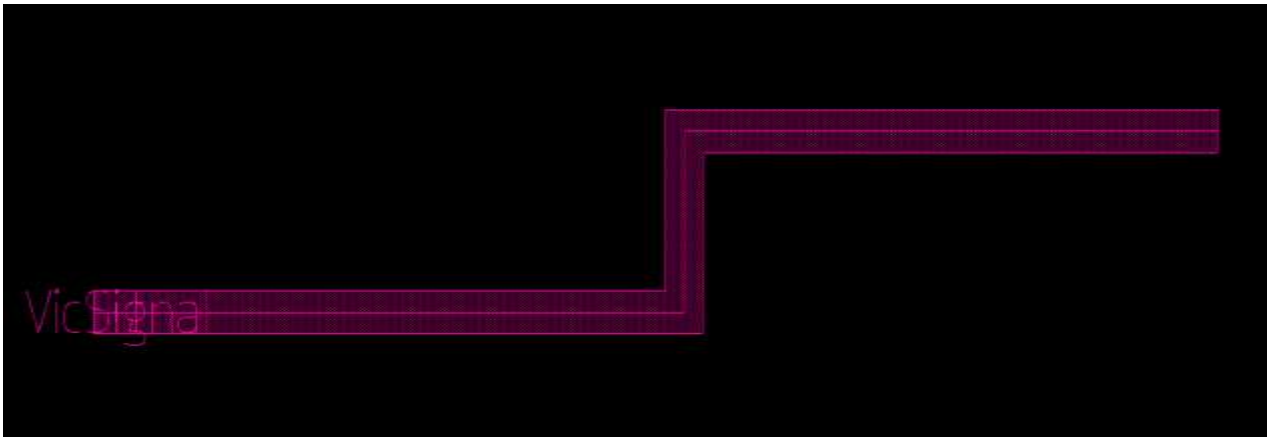


Figure 3.6.10(d) Victim signal with multi corners

Figure 3.6.10(e) Shielding constraints for test case 2

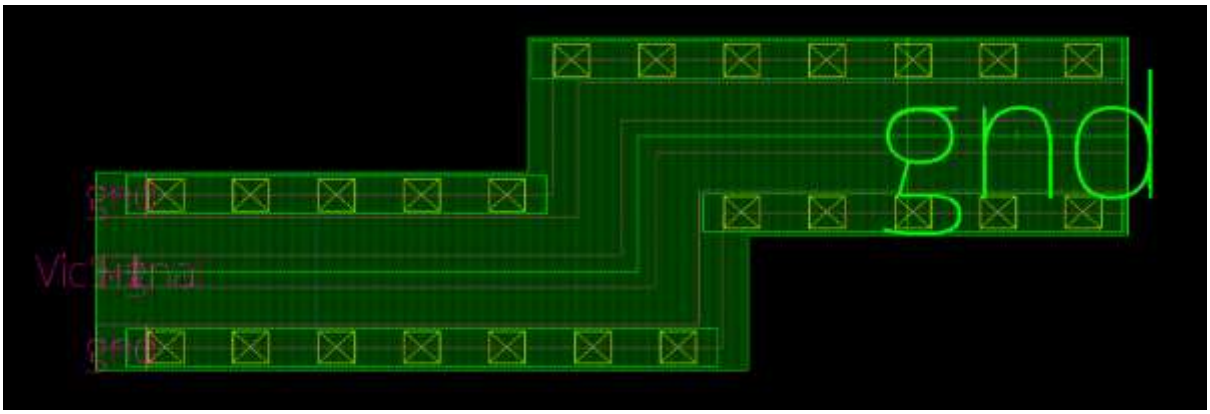


Figure 3.6.10(f) Test case2 results

There are two solid plates, one below the signal with M1 Figure 3.6.10(f). The other one is above the signal with M3. To complete the shielding all-around the signal, there are two shield lines parallel to the signal line. All shield lines are tied to ground signal and connected with each other with vias .

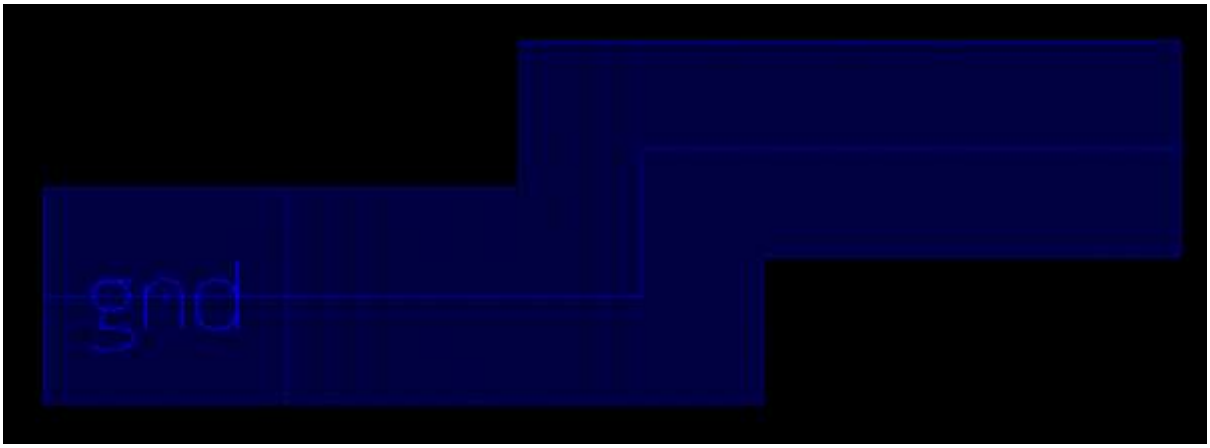


Figure 3.6.10(g) Below solid plate routed with M1

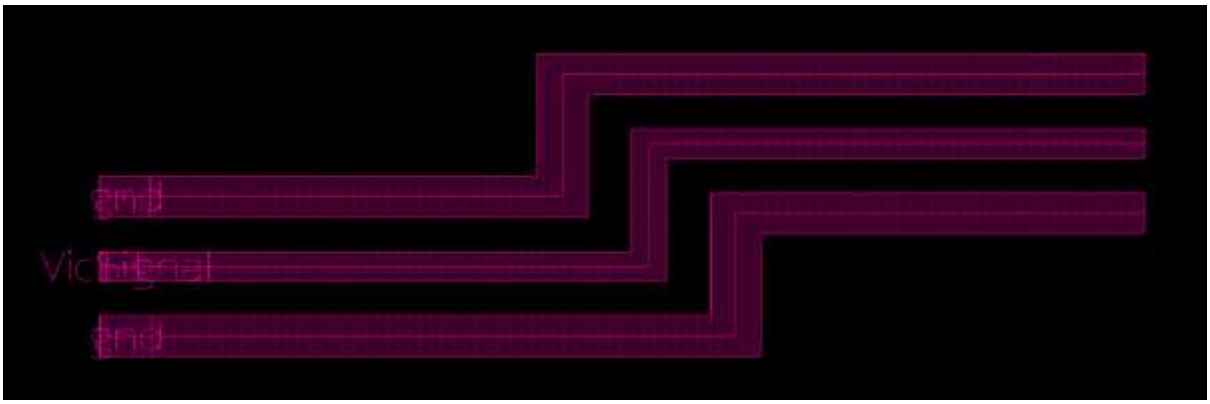


Figure 3.6.10(h) Two shield lines parallel to signal line

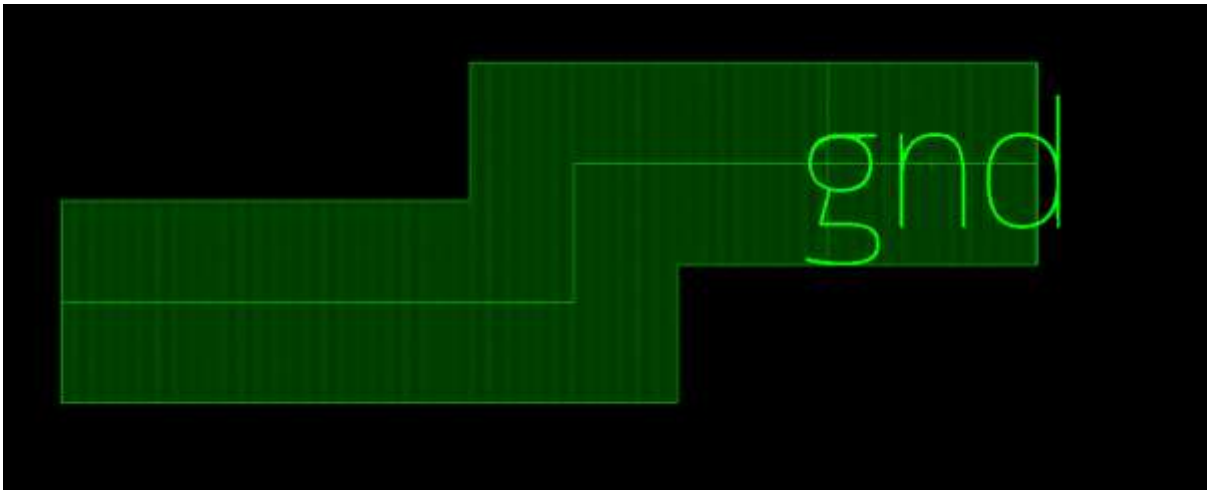


Figure 3.6.10(i) Below solid plate routed with M3

3.6.11 Errors and Warnings

Tool can support Warnings alerts if there are any errors. If the user forgets to select an interconnect and press on the shield button, a warning alert will appear Figure 3.6.11(a). To avoid DRC errors: if the user sets the width or the gap lower than minimum values, the tool will alert the user Figure 3.6.11(b), Figure 3.6.11(c) .

Figure 3.6.11(a) Missing to select an interconnect

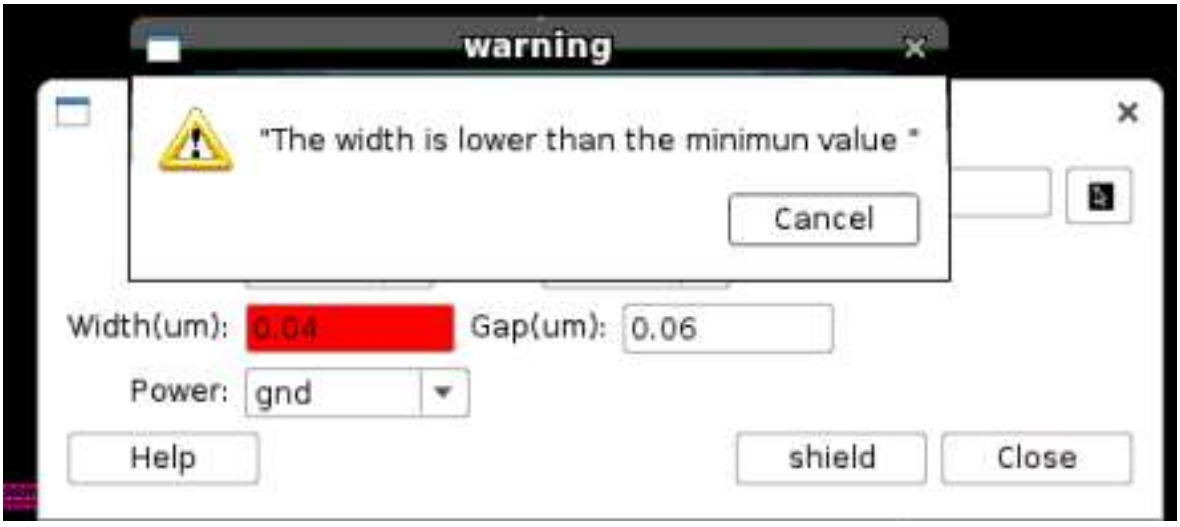


Figure 3.6.11(b) Width is lower than the minimum value

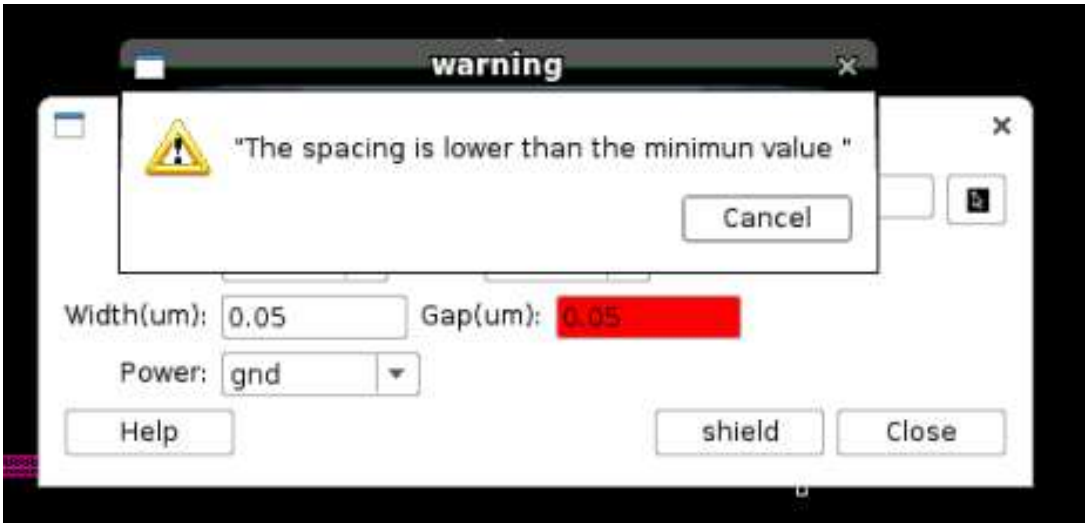


Figure 3.6.11(c) Gap is lower than the minimum value

While using tandem or coaxial style user can set layer offset with metal layer that is not in metals range. So, tool can alert him as shown in Figure 3.6.11(d)

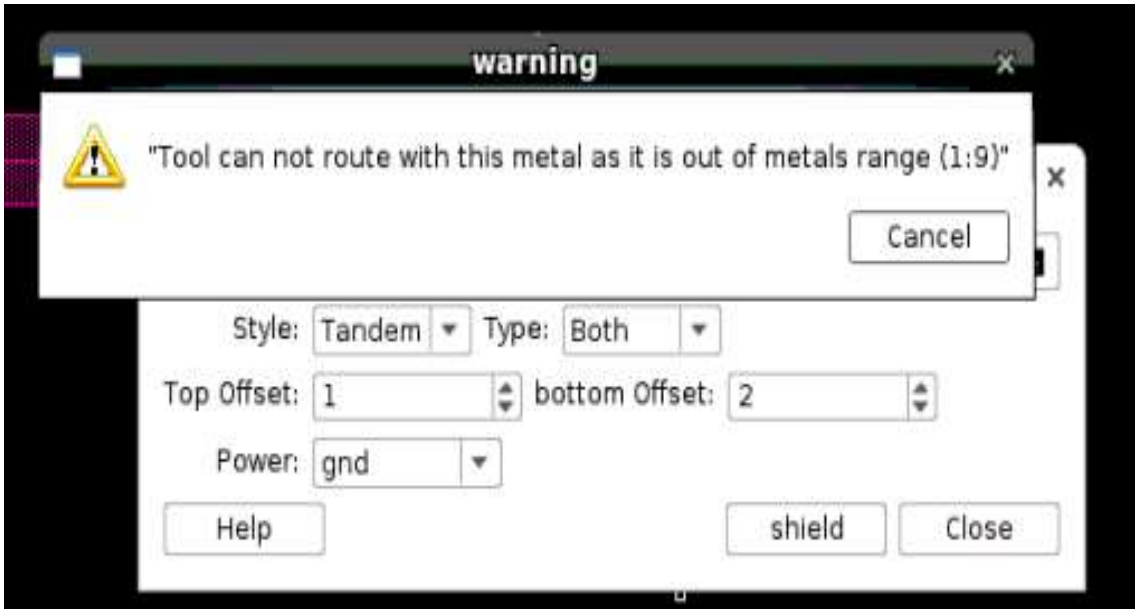


Figure 3.6.11(d) Warning alert due to layer offset

Chapter 4

Automated Decoupling Caps and Back-End Filling Tool

4.1 Introduction

Filling is one of the most important features that is required in modern IC industry. It can be used whether in place and route tools in digital design or in analog design to achieve high yield and guarantee some DRCs. Filling is done by generic runsets but they have some issues that aren't considered, in this section we will show these issues and how to solve them through proposed scripts. Filling done by Place and Route tools adds complete cells that are called filler cell insertion, these cells have no logical connectivity or specific function they are left floating or connected to VDD or GND.

4.1.1 Filler cell insertion

Filler cell insertion is used to fill empty areas in the boundary to have uniform layout because the more uniform the layout is, the higher yield we have. It's also used to have continuous VDD and GND rails and to have continuous Nwells and Psubs.

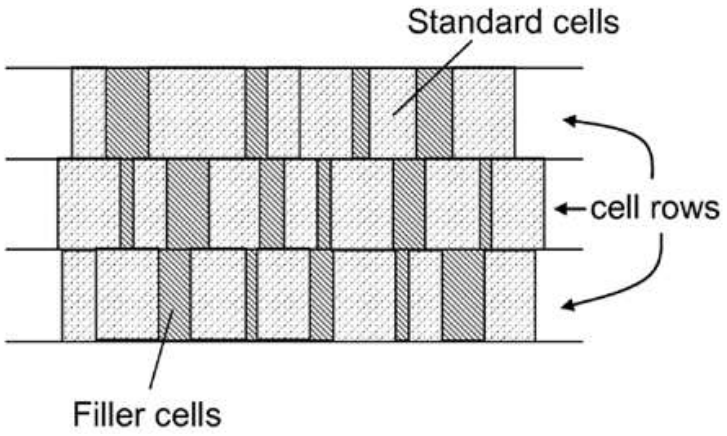


Figure 4.1.1 Filler cell insertion, from [10]

Here, some questions need to be answered:
Why do we need to have continuous VDD and GND?
Why do we need to have continuous Nwells and Psubs?
When can we put these filler cells?

We should have continuous power rails because if we design our cells uniformly, watching grid alignment and rules, we can allow an automated tool free reign over placement and wiring. We will know that our circuit will be built correctly regardless of the software decisions.

If there is continuity Nwell and implant layer it is easier for foundry people to generate them and the creation of a mask is a very costly process so it is better to use only a single mask.
If Nwell is discontinuous the DRC rule will tell that place cells further apart i.e., maintain the minimum spacing because there is a well proximity effect.
we know Nwell is tap to VDD and P substrate is tap to VSS to prevent latch up problem. now if

there is a discontinuity in Nwell it will not find well tap cells, so we have placed well tap cells explicitly, therefore it will increase the area explicitly, hence we have filler cells so no need to place well tap cells.

when optimization of clock tree synthesis is completed i.e., after timing has been met because let's say if we want to place buffer/inv for optimization purpose we can't place these cells because there is already placed filler cells, and enough area is not there to present buffer/inv, so after timing has been met and routing optimization is done then only placed the filler cells to fill the empty space.

4.1.2 Metal Dummies

Filling can be with metal dummies as well. But this filling is more common in analog or analog and mixed signals to solve some problems related to density due to some different issues:

- **Due to etching**
  A narrow metal wire separated from other metal receives a higher density of etchant than closely spaced wires, such that the narrow metal can get over etched

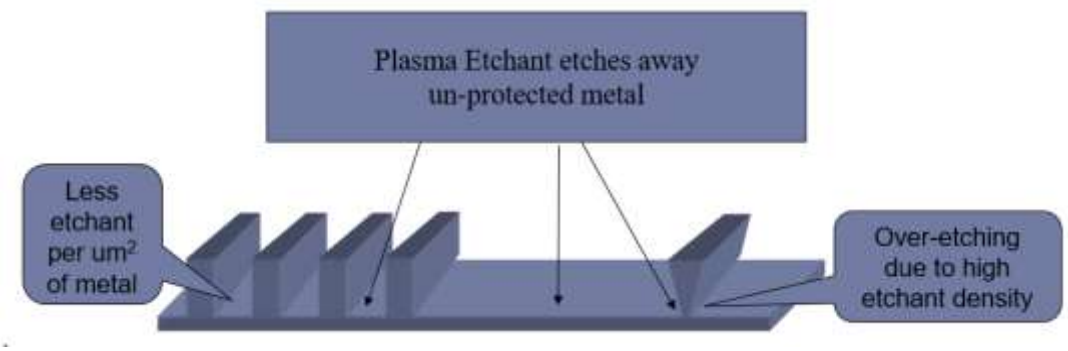


Figure 4.1.2 (a) Etching related to density, from [11]

So, the etching won't be symmetric that leads to difficulty in matching and deform the distribution of the current. To solve this problem, the fab puts a condition of minimum density for example: min density is 30% in specific window size with specific step.
So, the layout designer should add metal dummies in the space areas to achieve density higher than the minimum, but he should be care about that if it's critical signal that passes through that metal layer, we must put the minimum only not to couple over this net.

- **Due to CMP**
  To know how the problem came, we should know how the CMP is done:

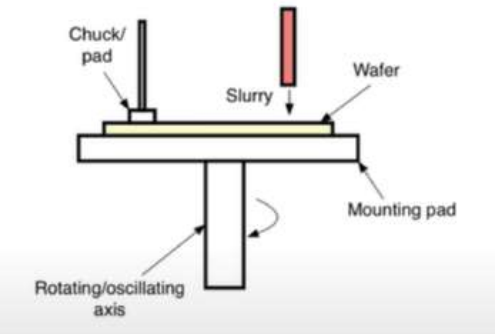


Figure 4.1.2 (b) CMP process, from [3]

We put the wafer over mounting pad and add to it some particles through material called Slurry this material helps to polish the wafer chemically when we erosion the wafer by the chunk/pad. The polishing will be effective when we rotate the oscillating axis (mechanically).
to have symmetric way in polishing we should have uniform distribution of metals over the silicon dioxide (SiO2) because the metals are softer than the silicon dioxide mechanically so there are some problems arise when there is large difference in metal densities. We can highlight two of them:

- Dishing
  It's the difference between the height of the oxide in the spaces and that of the metal in the trenches.
- Oxide Erosion
  It's the difference between the oxide thickness before and after CMP.

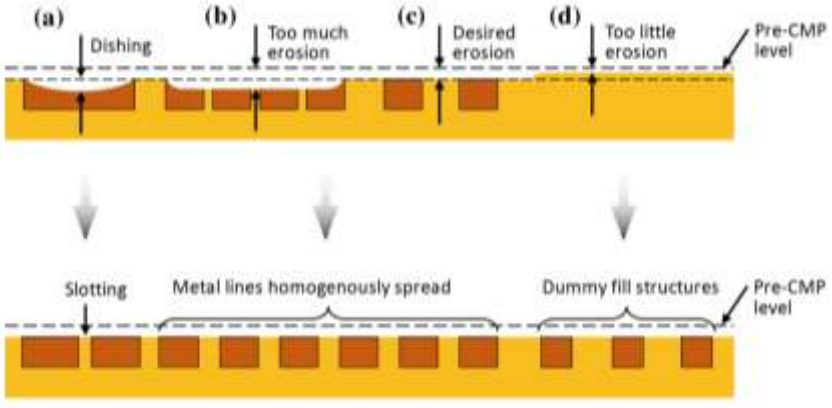


Figure 4.1.2 (c) CMP problems, from [4]

We notice in the above figure that when the density is low as in case (d) so we will have too little erosion. And if we have high metal density. There will be too much erosion with dishing as in case (b). high density can be verified when the metal is very wide as in case (a) so Slotting is the perfect solution to decrease the density. We aim to have all metals like case (c). To solve these problems, the fab put some rules on the minimum and maximum density to have the metal lines homogenously spread over the wafer.

- **Due to oxide CVD**
  To identify this issue clearly let's have an example: we want to deposit two tracks of the same metal layer M1 but there is a large distance between them.

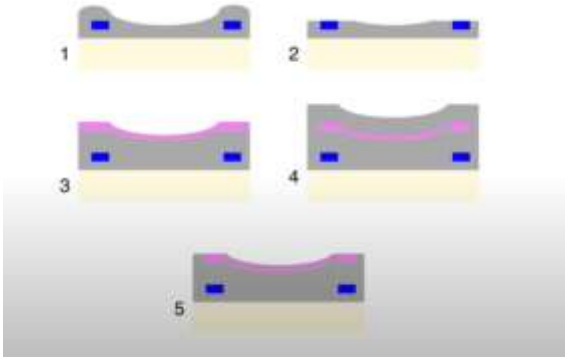


Figure 4.1.2 (d) CVD before Dummies filling, from [3]

1. We deposit M1 and SiO2 over them creating a valley of SiO2 between them.
2. CMP is done but still there is a valley between them.
3. We deposit M2 so the valley will be filled with M2.
4. We put SiO2 with normal thickness.
5. CMP is done but there is a shortage between two metals tracks on M2.

So, the fab put a rule on the minimum density to guarantee that there is no deep valley of SiO2 so we can avoid shortage between two metal tracks

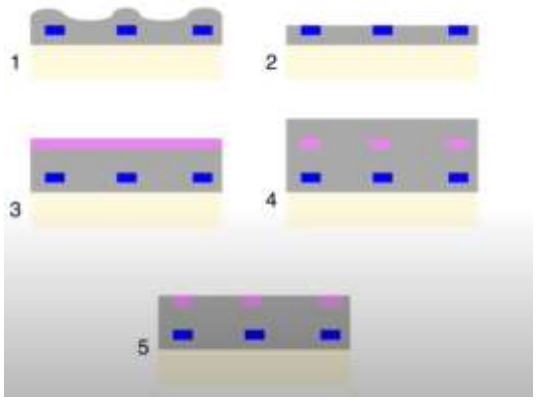


Figure 4.1.2 (e) CVD after dummies filling, from [3]

As we saw the dummies filling is very important to deal with some issues during the fabrication process. Layout engineer can leave these dummies floating or connect it to VDD or GND to protect the surrounding signals from any coupling or noise.

The layout engineer uses some generic runsets to fill in the layout in no time approximately. But the tax appears in analog design when we are interested in symmetry between specific blocks and need to avoid any coupling.

4.2 Motivations

4.2.1 Empty area on the FE is better to be filled with decaps

when we use the generic runsets, filling will be with floating metal dummies that adds around 20% extra capacitance in the filled area. We can control these extra capacitances by changing the number of the dummies:

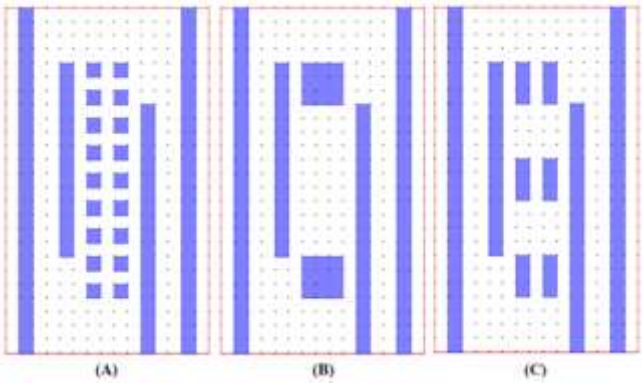


Figure 4.2.1(a) (A) Regular dummy fill
(B) Two large dummies
(C) Six dummies, from [14]

We can control the capacitance value by replace sharp corners with round corners

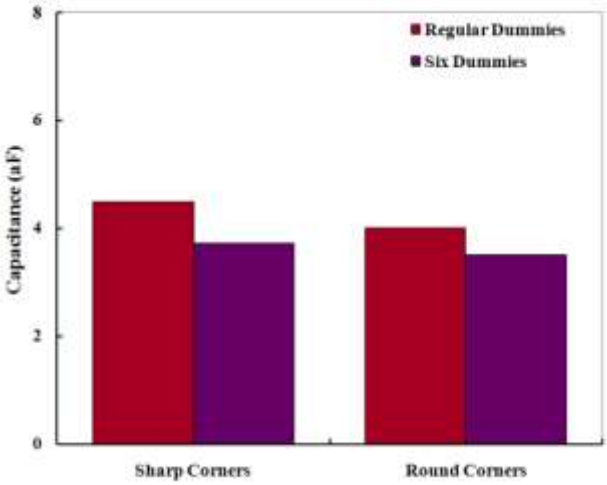


Figure 4.2.1 (b) Comparison between two different patterns with and without sharp corners, from [14]

Dummies lead to a significant increase in the parasitic losses. Therefore, the dummy metal pattern must be designed such that the parasitic losses are minimized. The pattern controls also the dishing problem as we see in the below figure, we have some different patterns:

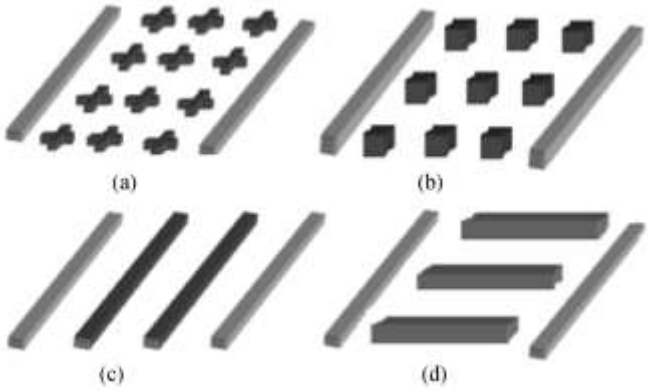


Figure 4.2.1 (c) Possible dummy shapes. (a) Cross. (b) Square. (c) Parallel line (d) Orthogonal, from [15]

A cross dummy fill can have a better effect on metal dishing, compared to the other three dummy fill shapes. The orthogonal dummy structure has the worst impact on copper dishing. The best performance of the cross-dummy fill can be explained in two ways. One reason is because the smaller area of the cross dummy brings a smaller area of trench, which makes the pad surface less distorted and causes less copper loss during the polishing process. The other reason is because it can achieve more uniform distribution compared to the other three shapes at the same density, which makes the wafer endure mechanical force more evenly. Therefore, in order to reduce dishing in real design, the cross-shape dummy fill is preferred over the other three shapes.

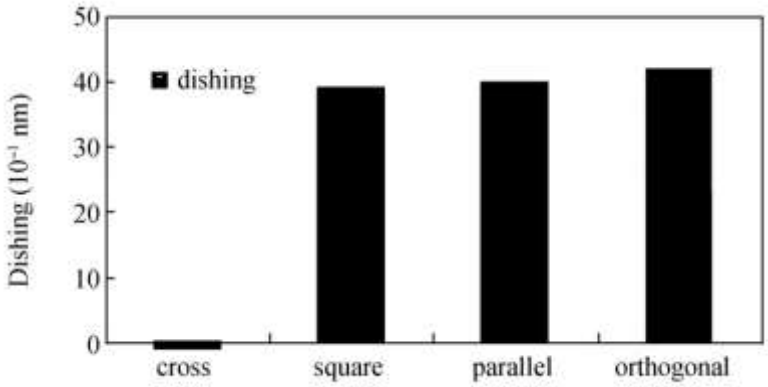


Figure 4.2.1 (d) Copper dishing with different dummy shapes, from [15]

From the previous studies we can tell that the cross-dummy filling with round corners is the best pattern for dishing and parasitic capacitances. But this pattern is very difficult in fabricating and requires very slow processes to create them in symmetric way, the improvement in capacitance load sometimes doesn't satisfy the designer.

One of the magical solutions is to fill with Decoupling capacitors, we can benefit from them to fill in empty areas instead of filling with dummies:

- Solving IR drop voltage:
  VDD and GND are special signals because they are DC signals and there is high sinking and driving current at them so even the path was low resistive it will cause high voltage drop. This high current is due to all circuits use VDD and GND rails except for transimition gates but we can't use them alone.

  So, we can consider that all circuits use VDD and GND.
  To solve this problem we can use power grid with high metal layers and very wider metals to have minimum resistance.

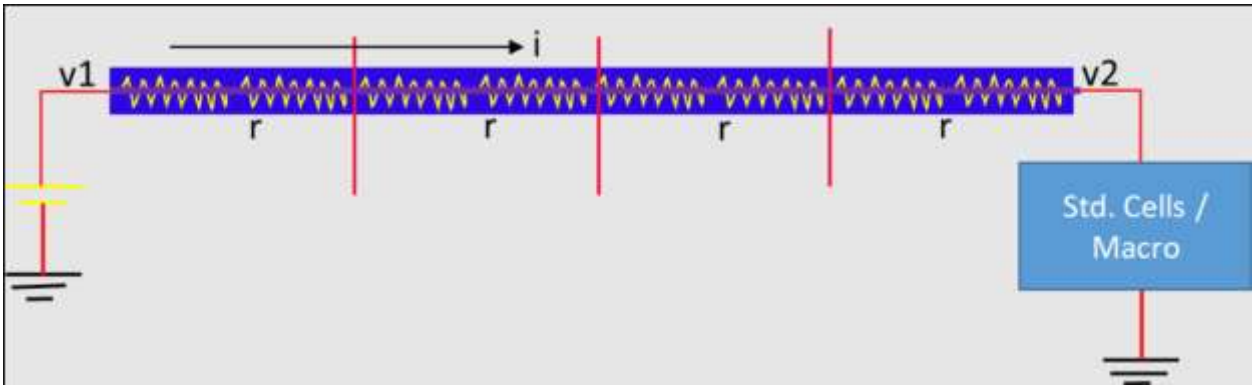


Figure 4.2.1 (e) IR drop in supplies, from [16]

Using the decoupling cap as a bank of charges that can compensate that drop by charging from VDD then discharges it into the circuit so we can have strong VDD and GND.

- Solve Ground & supply bounce problem:
  As we mentioned before, VDD and GND drives and sinks high current to and from all circuits.in this point we must mention that these circuits work non-correlatedly so there is variation in the current value all the time.

  According to Ohm's Law for inductors:

$$V = L\frac{di}{dt}$$

  So, this variation leads to voltage drop. But the question is:
  why do we have inductance on VDD and ground nets?
  The inductance is due to off chip reasons as PCB tracks and from pad pins, due to on chip reasons as bonding pads or due to packaging in bonding wires.

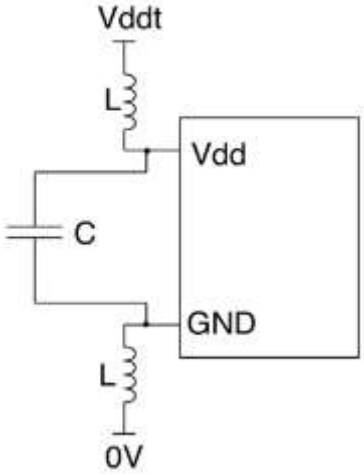


Figure 4.2.1 (g) Bouncing solution, from [3]

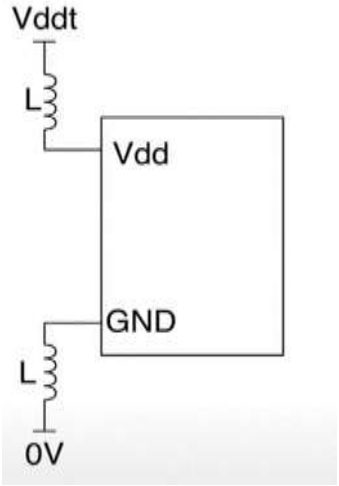


Figure 4.2.1 (f) Bouncing circuit, from [3]

To solve this problem, decoupling caps are used to vary the value smoothly.
This is clear in the Ohm's Law for capacitor:

$$V = \frac{1}{C}\int i\,dt$$

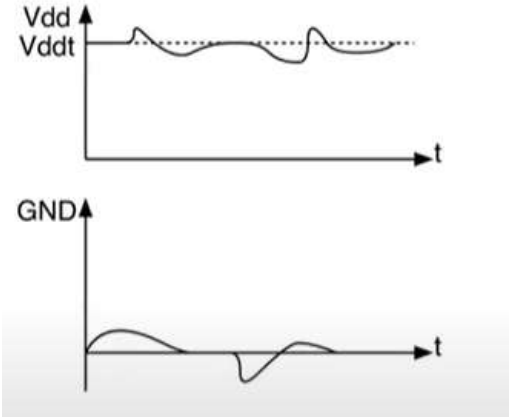


Figure 4.2.1 (i) Bouncing diagram, from [3]

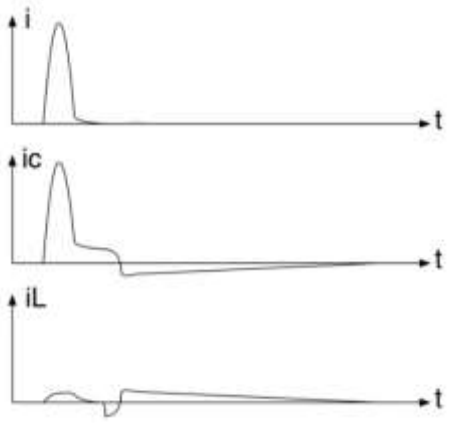


Figure 4.2.1 (h) Bouncing solution diagram, from [3]

We are interested in VDD and GND although the other pins have also inductance but they don't have this large swing in the current. This bouncing is solved by on chip cap or off chip. On chip decaps solves inductance issues due to on chip and off chip, but off chip solves off chip inductance only.

- Predefined capacitance:
  when we add metal dummies, they add to know later capacitance that we know its value after simulation but decoupling caps add predefined capacitance.

- Avoid noise from unknown resources:
  Dummies can collect noise from everywhere that can affect the signals and we can't define each capacitance from its resource.

Using decoupling ca more useful than dummy metals but it's timing consuming. If it's automated it will be really a bargain.
Our proposed script aims to fill with decoupling caps with many option that will be discussed later.

4.2.2 BE filling on highly symmetric blocks

Today large analog circuits require symmetric layouts not only for matched transistors but also for entire blocks that need to be identical to each other. Symmetric blocks may be split into halves and laid apart in one- or two-dimensionally symmetric styles so as to ensure similar effects of process and temperature gradients for all subcircuits that are identical by design.

So if the metal dummies added in the symmetric block are different this means different parasitic which will lead to systematic mismatch and decrease the performance of the circuit, for example, CD player the CD player has two-channel the left one and the right one if the two amplifiers that drive the left and right channels seem to be reacting very differently due to systematic mismatch so the volume of the voice in the two-channel will not be the same, may the left channel is slightly louder than the right channel or the opposite and this will translate to a bad design of the circuit.

Another example is, Large analog blocks like variable gain amplifier containing on-chip resistor and capacitor in the output stage Such passive devices significantly affect circuit performance and need to be laid out carefully to minimize the parasitic effects. Furthermore, passive devices identical by design are also laid out symmetrically.

So, symmetry is an important aspect of analog layout but generic runset filling does not take this requirement into consideration as generic runset start from a fixed point and takes a window from this point and checks density on it then takes a step so generic interested in density on the window and doesn't look at the other requirements.

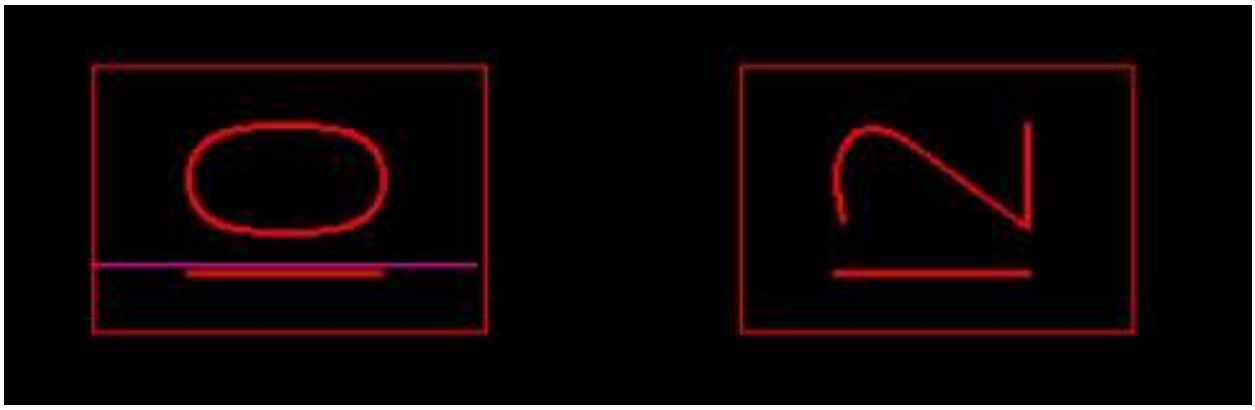


Figure 4.2.2 (a) layout of two block before run generic runset

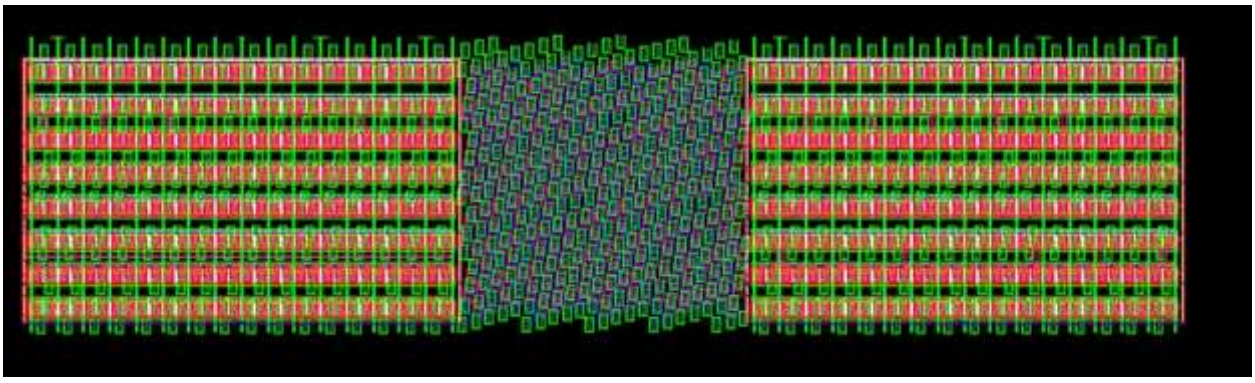


Figure 4.2.2 (b) layout after run generic runset

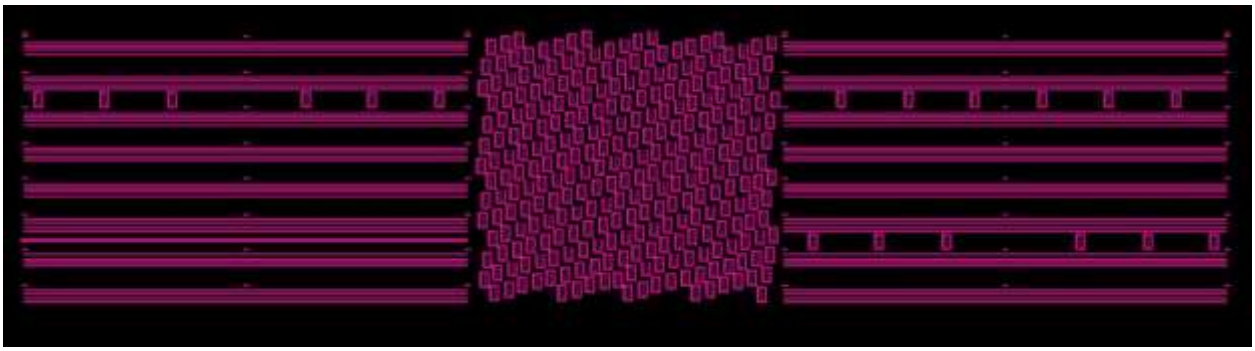


Figure 4.2.2 (c) metal 2 dummies

Figure 4.2.2 (c) shows that metal two dummies on the left on block are not the same as the dummies on the right block right and this which will lead to the systematic mismatch between the two blocks.

4.2.3 BE filling around highly critical nets

As we discussed before density issues due to CMP and etching so to avoid these issues dummy metal fill is needed in empty areas to achieve close-to-uniform metal density across the chip area, so if there is no filling around the critical nets this means density violation which means leaving the area around the critical without filling is forbidden.

Using a generic runset isn't a good solution as traditional blind metal fill will add excessive parasitic coupling and this will add delay on the critical nets, in addition to the losses in the passive structure at higher frequencies due to induced eddy currents, and this parasitic will decrease the chip performance for example clock skew which will force the designer to reduce chip frequency to accommodate the impact to avoid setup time violation, another example in analog circuit metal fill degrades the quality factor of spiral inductors used in an oscillator circuit

We can see the output of generic runsets around the critical net specifically the yellow frame refers to the critical region we want to fill in:

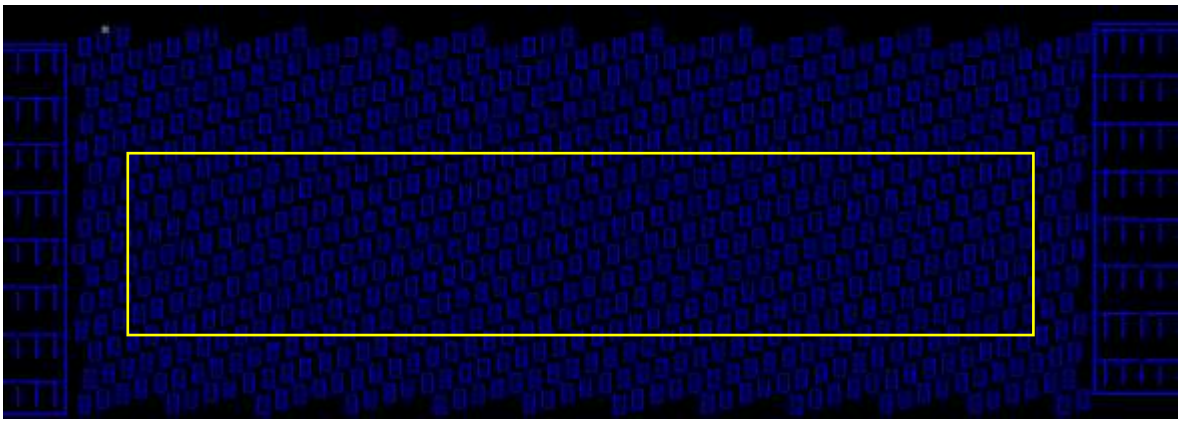


Figure 4.2.3 (a) metal 1 dummies using generic runset

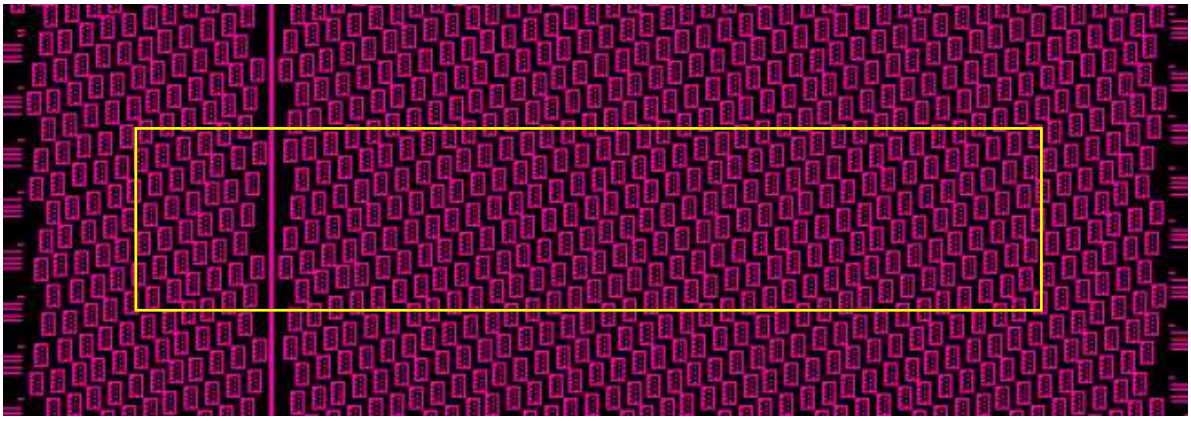


Figure 4.2.3 (b) metal 2 dummies using generic runset

Figure 4.2.3 (c) metal 3 dummies using generic runset

the figures show the generic runset adds a huge number of metal dummies around the critical net excess the minimum density and less than the maximum density this is the aim of the generic filling and it adds dummies close to critical net.

To analyze the impact of metal fill, we refer to the parasitic capacitance model in figure 4.2.3 (d), we have three parasitic capacitances C(lateral) is the coupling capacitance between metal wires on the same layer, C(parallel) is the coupling capacitance between metal wires on adjacent layers, and C(fringing) is the coupling capacitance between the side wall of a metal wire and the top/bottom surface of another metal wire on the adjacent layer and the total coupling capacitance is the summation of all types of parasitic capacitances.

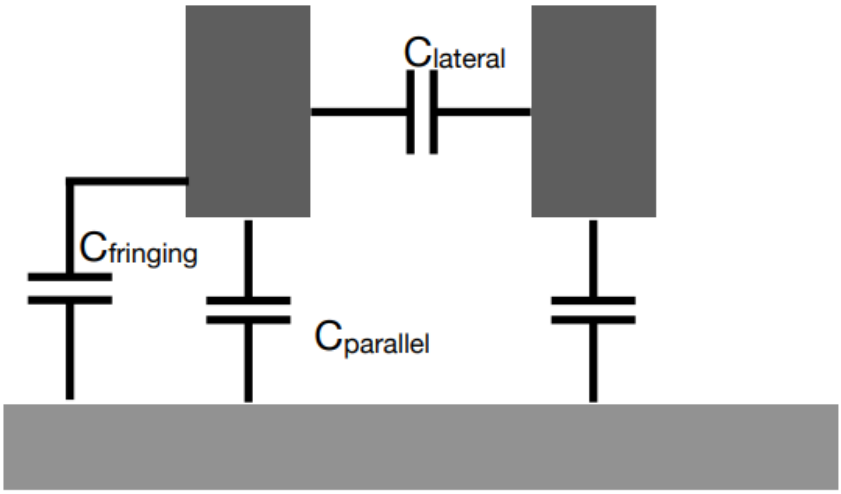


Figure 4.2.3 (d) Parasitic coupling capacitance from [17]

The general equation of the capacitance between two plates that can model the three capacitances can be found with this formula:

$$C = \frac{\varepsilon A}{t} \qquad (1)$$

Where:

ε = permittivity of the dielectric

A=area of plate overlap

t= distance between the plates

To overcome the excessive parasitic capacitance, we should:

1. Fill with a minimum density around the critical net
2. Increase space between critical nets and dummy fill

Approach (1) is straightforward to understand as decreasing the number of dummies around the critical net will decrease the parasitic capacitance but we have to achieve a minimum density.

Approach (2), from equation (1), It can be observed that the value of coupling capacitance is reversely proportional to the spacing between the plates so increasing spacing between critical nets and dummy fill will decrease the parasitic capacitance, However, leaving space between metal fill and critical routing nets can reduce the metal density, and potentially cause metal density violation so be aware of this point and don't leave large space.

One of the most pivotal questions is why we fill with metal dummies instead of filling with decoupling caps as mentioned before, sometimes we have signals we want to deal

with them symmetrically but their surroundings are different from each other so we can't guarantee that filling with decoupling will be symmetric or the remain area to fill without any DRCs is smaller than the smallest unit cap so filling with metal dummies is better than decoupling in this case.

4.3 Proposed solution:

we have built a tool to automatically perform parameterized decap filling and BE filling that conform with above mentioned AMS motivations. The decaps parameters can include the device type, MOM options over the MOS, and max layer of MOM, etc.
running the proposed script, the below GUI will appear:

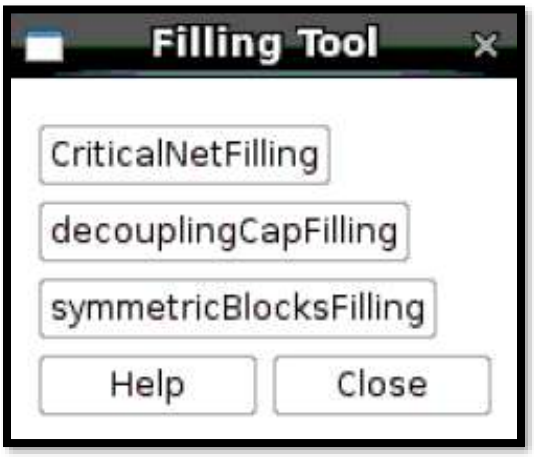


Figure 4.3 General GUI

We can choose the suitable choice to deal with our required motivation. But, to deal with all cases without affecting each other we can start "CriticalNetFilling" to fill on all critical nets we want, then we run "symmetricBlocksFilling" to fill on all highly symmetric blocks in symmetric way, then we run "decouplingCapFilling" to add decoupling caps in the remain spaces, finally we run the generic runset to fill in the spaces that are smaller than the smallest unit cap to achieve the required density.

4.3.1 Decoupling Caps Filling Script

Main features:

* Get the empty areas in the layout.

* Can fill with MOS or MOM over MOS.

* Can fill up to max available layer or desired layer.

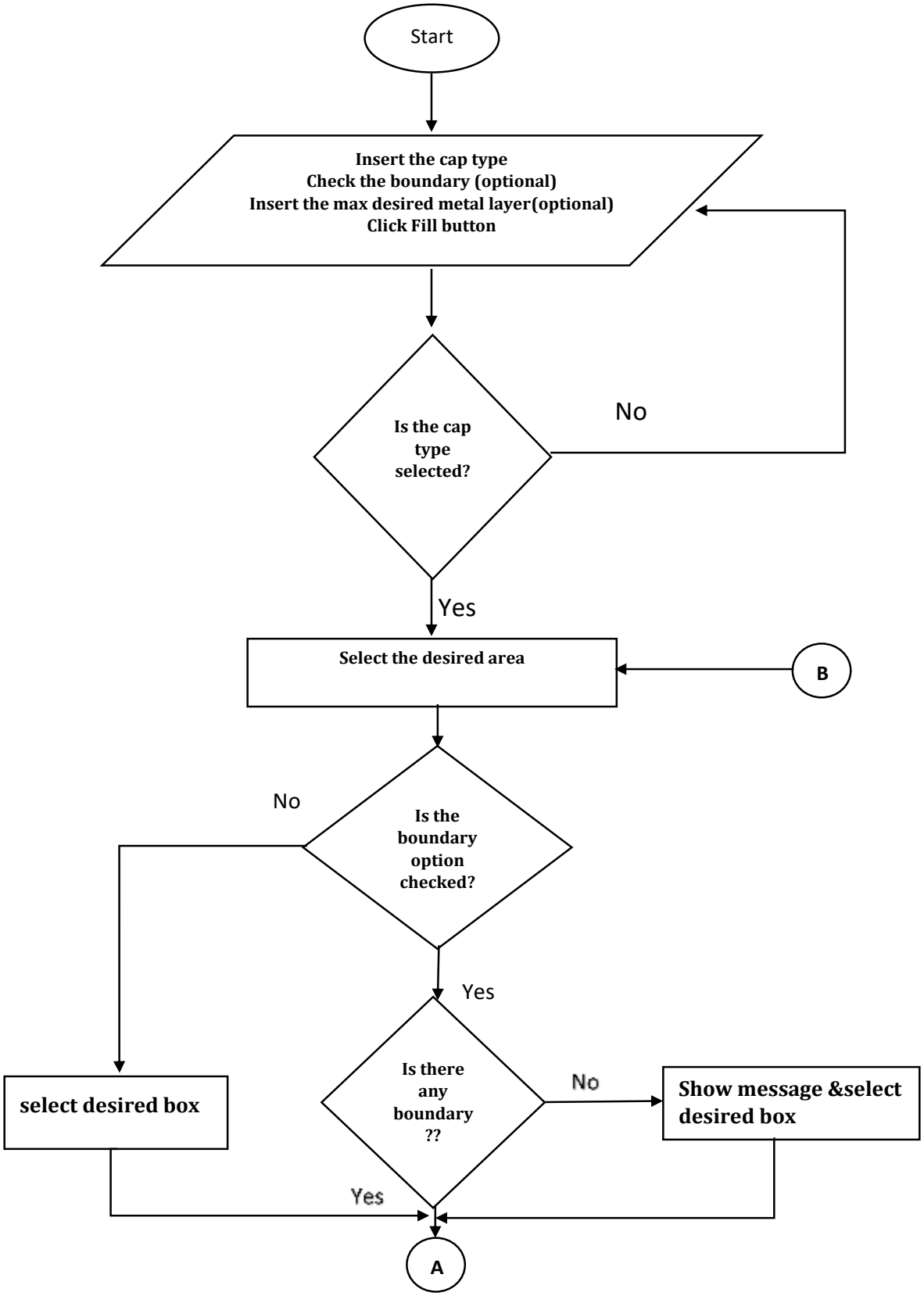
* Can fill inside the boundary or in the desired selected area.

* Insert attribute (capValue) to know the cap value at any time.

* Show all details of the filling in table in GUI including the efficiency of filling.

* Testbench script helps know the created unit cap value that allow to create your own library of filling.

Flow chart


Start
Insert the cap type
Check the boundary (optional)
Insert the max desired metal layer(optional)
Click Fill button
Is the cap type selected?
No
Yes
Select the desired area
B
Is the boundary option checked?
No
Yes
Is there any boundary ??
No
Show message &select desired box
select desired box
Yes
A

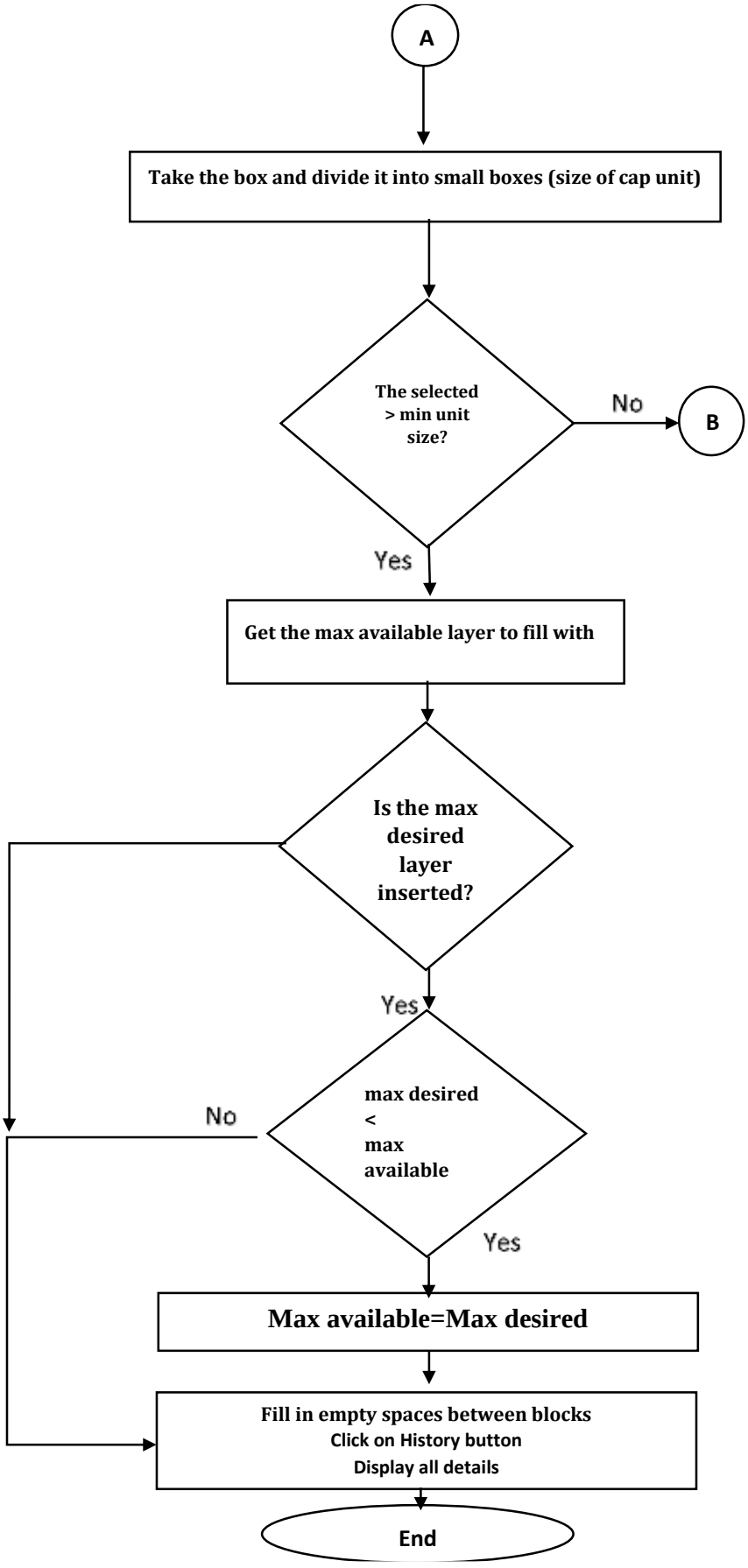


Figure 4.3.1 (a): Flow Chart

How to use:

* Run the script, this window will appear:

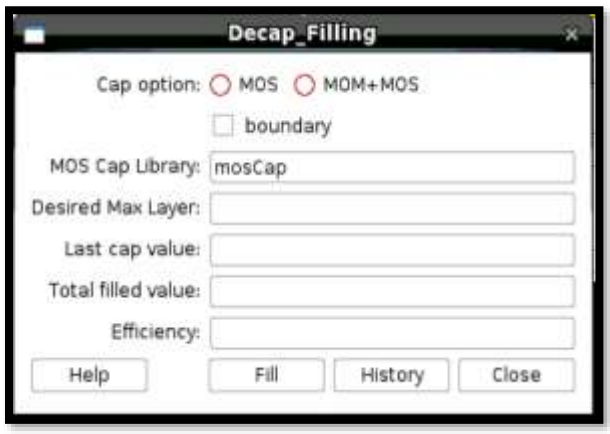


Figure 4.3.1 (b) Decap filling GUI

* If you clicked on Fill button, this message will appear

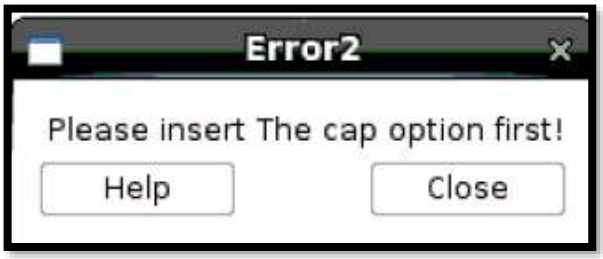


Figure 4.3.1 (c) Error cap option insertion

So, you must specify the cap option (MOS or MOM over MOS)

* When you enter the inputs as:

Figure 4.3.1 (d) Example for inputs in Decap GUI

The script considers free selection because the boundary is unchecked and considers the desired max layer as the max available layer we can insert because there are no conditions on max layer.

* Now you can start filling with **Fill button**, Select your region.

* We could fill outside the boundary because the boundary option was unchecked (case A).

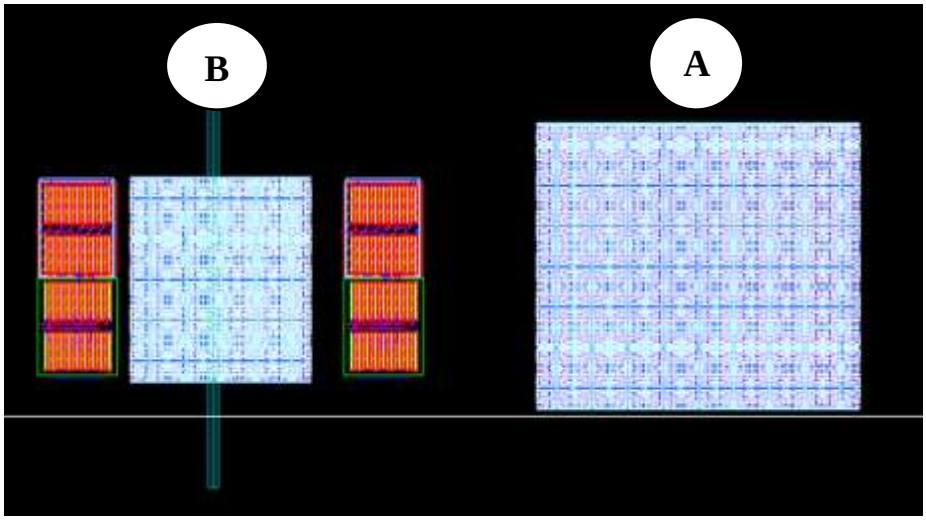


Figure 4.3.1 (e) Free selection example

* The script fills with max available layer in case A because there are no metals in this region.

* The script fills with suitable layer in case B (metal 4) because there is metal 5 in this region.

* When you click on History button:

Figure 4.3.1 (f) History table

Here we can get all details about what happened from start to end

* If the selected area was smaller than the available unit so this message will appear:

Figure 4.3.1 (g) small area warning

Let's try with another case:

* When you enter the inputs as:

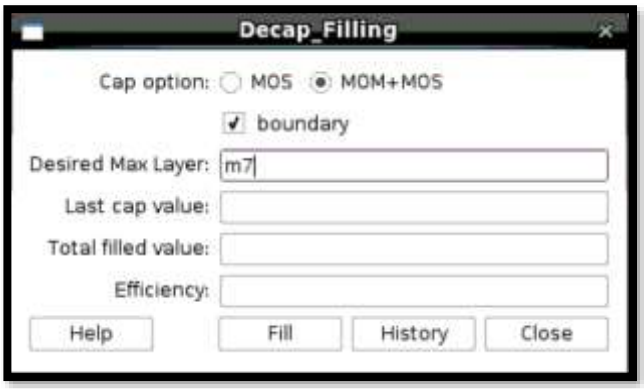


Figure 4.3.1 (h) GUI input example

This message will appear when you click Fill button:

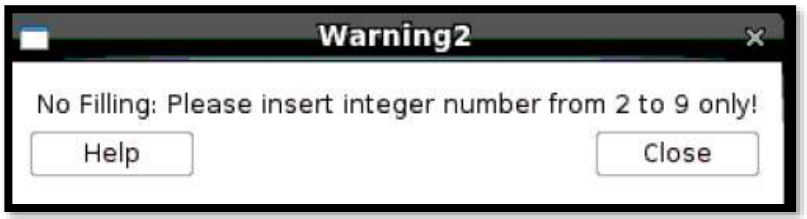


Figure 4.3.1 (i) integer number warning

So, you should insert this option as integer numbers only from 2 to 9

* When we modify the inputs:

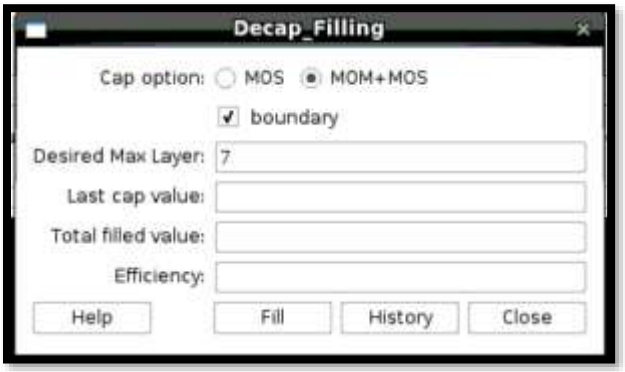


Figure 4.3.1 (j) Modified input in GUI

Now,

* The script will fill inside the boundary of the layout because boundary option is checked and the max layer

* We can put over the MOS is 7 even if it's available more than this.
* When you click fill but there is no boundary layer in layout like this:

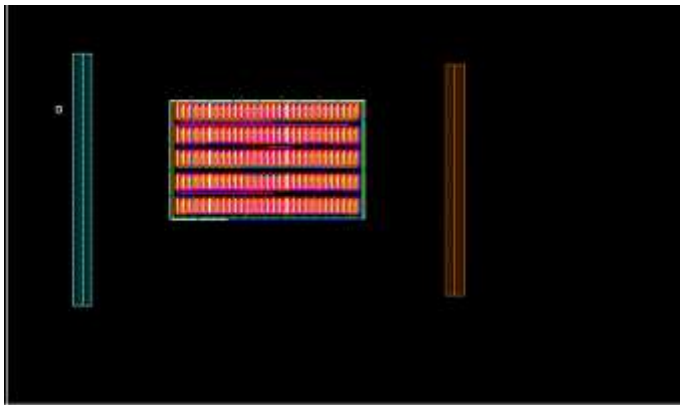


Figure 4.3.1 (k) No boundary layout

This message will appear:

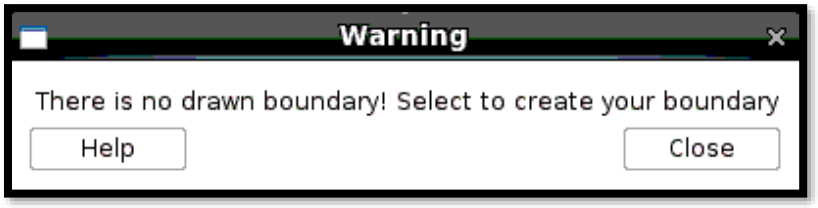


Figure 4.3.1 (l) Unmatchted inputs warning

So, you can verify your boundary before filling.

Now we know how to fill well.
You can select inside the boundary with minimum selection as minimum available cap unit.

Before:

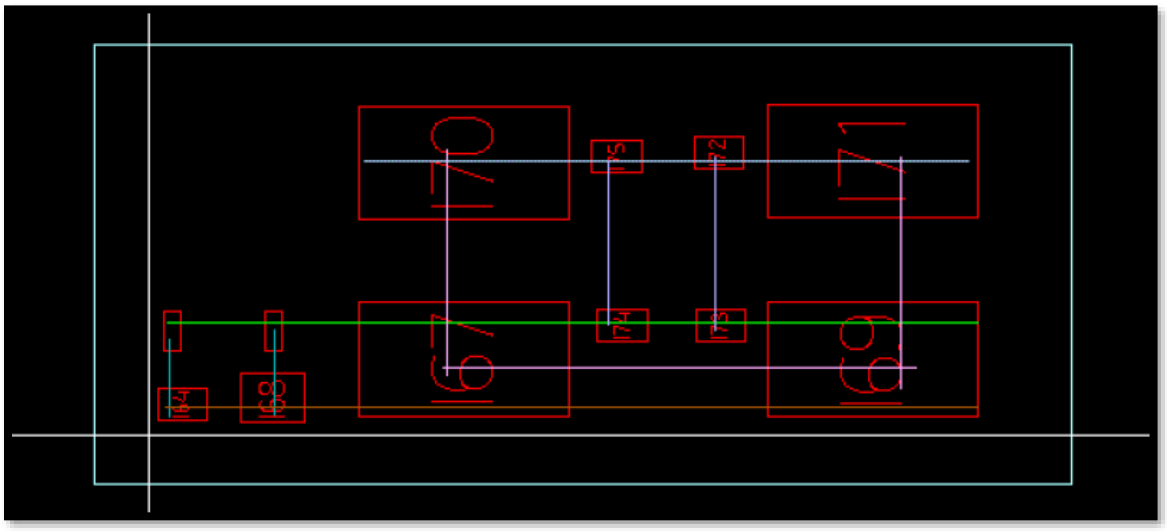


Figure 4.3.1 (m) Layout before filling

After:

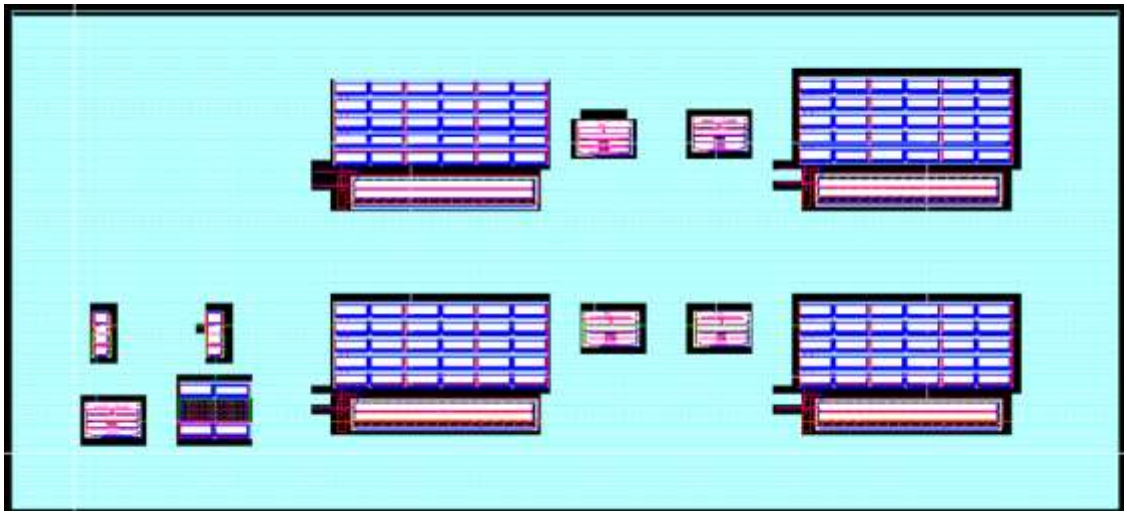


Figure 4.3.1 (n) Layout after filling

Let’s have detailed look:

1- There is no filling here because there is metal 3 passing through it

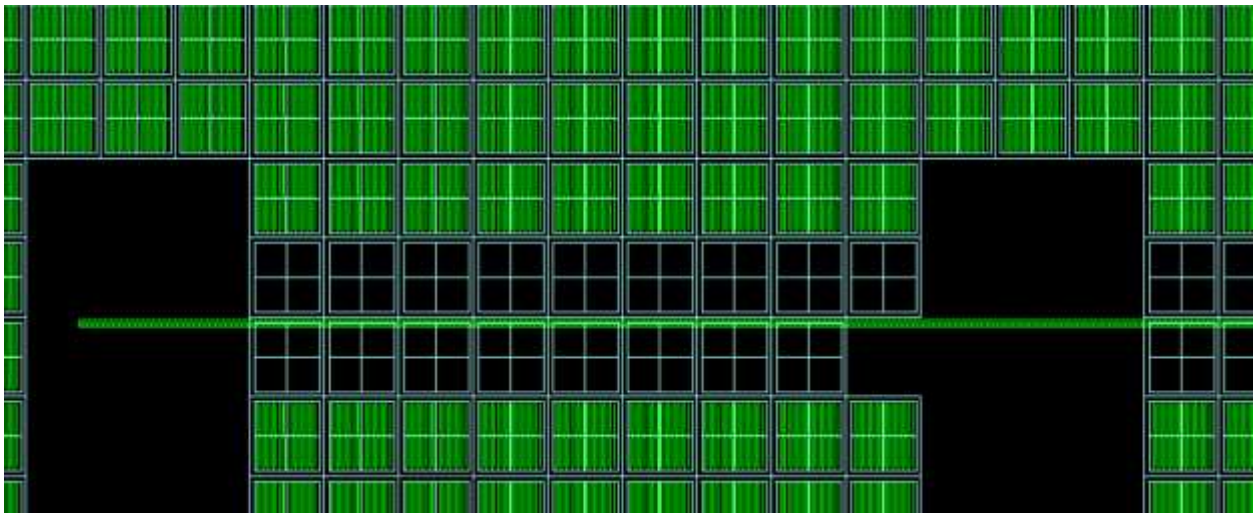


Figure 4.3.1 (o) M3 in filling

2- There is up to metal 7 only because there is metal 8 passing

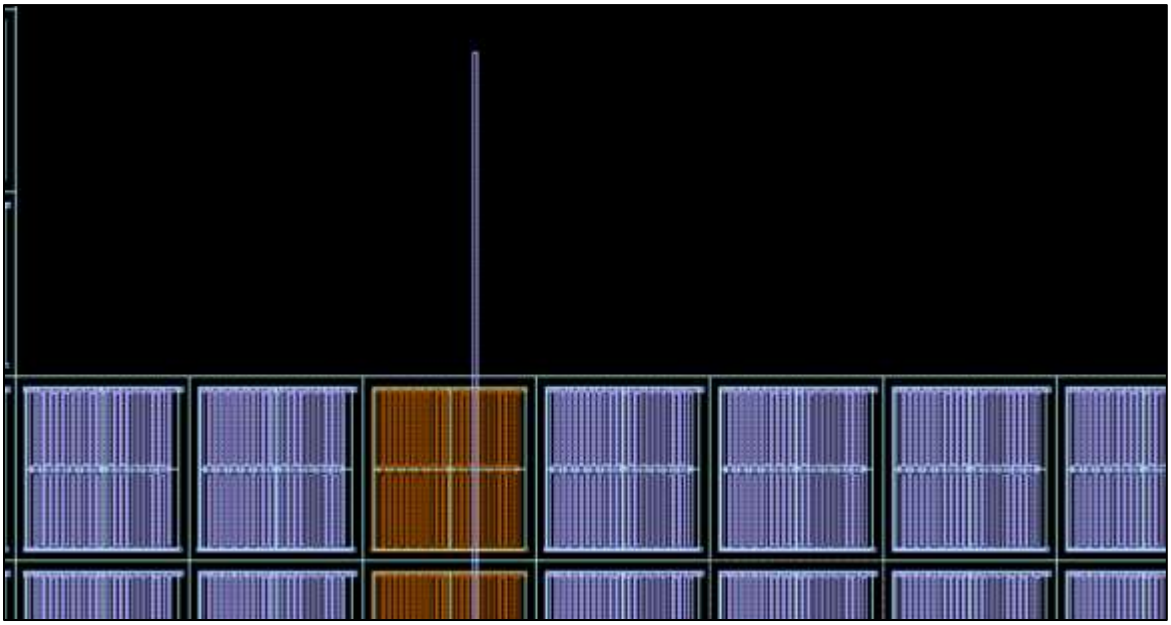


Figure 4.3.1 (p) M7 in filling

3- we can get the conclusion of what happened through the GUI:

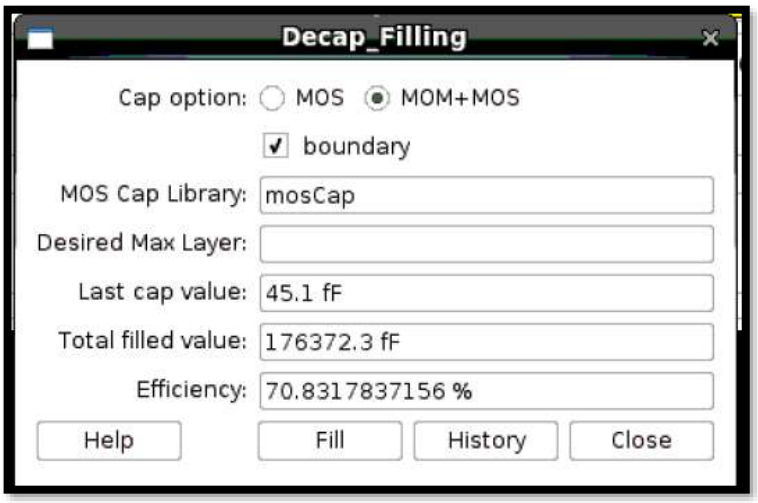


Figure 4.3.1 (q) Conclusion of filling

For more details about the cap filling, **Click on History button**:

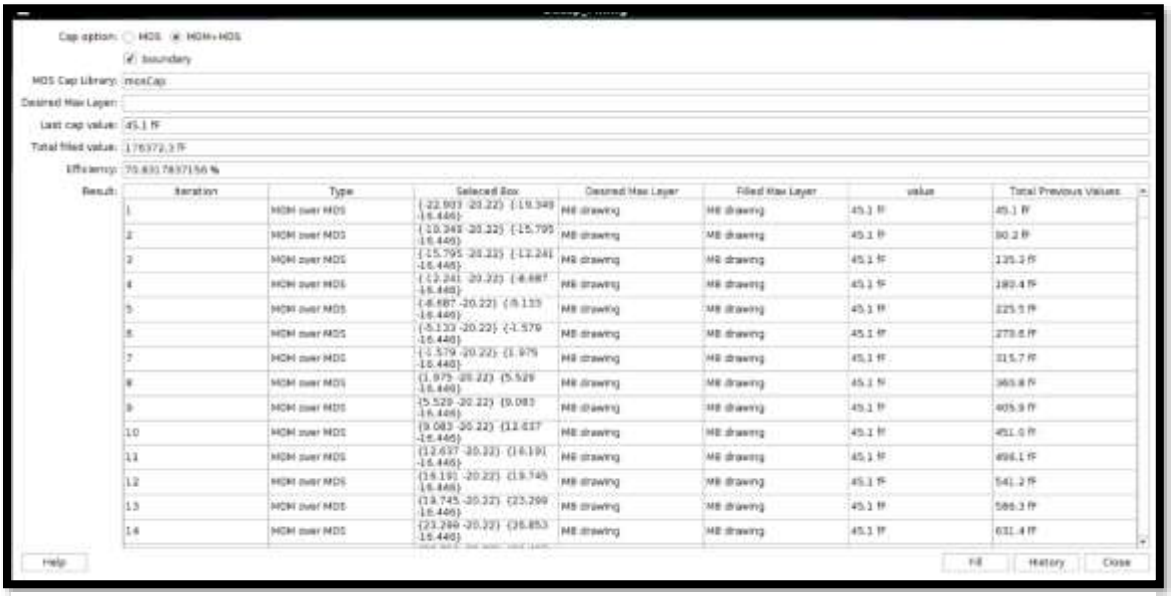


Figure 4.3.1 (r) Detailed history table

We can know the value of specific cap through its attribute (capValue):

We can get it through object Analyzer script

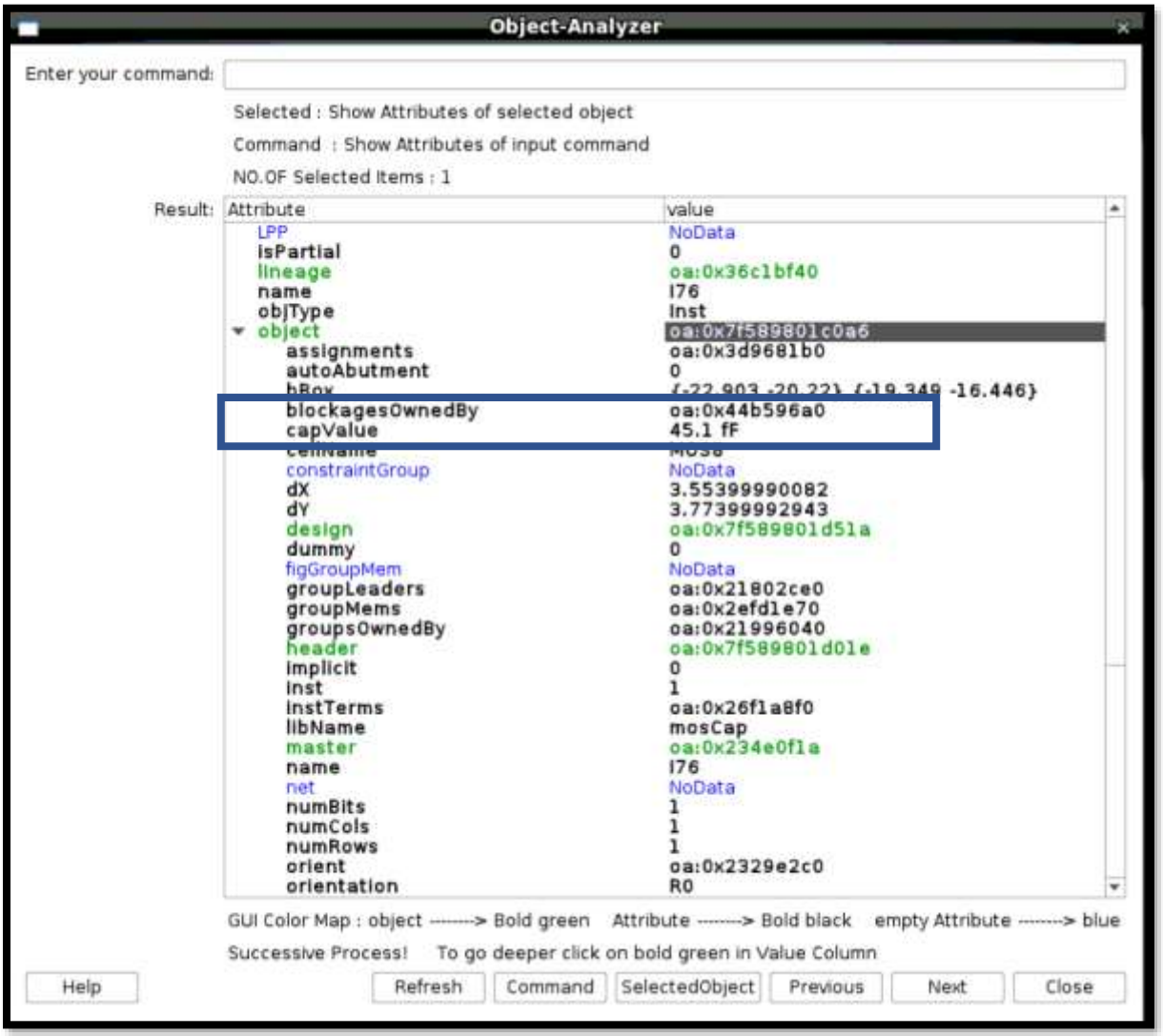


Figure 4.3.1 (s) cap Value in object analyzer GUI

Or, through command:

```
> db::getAttr object.capValue -of [de::getSelected -design [ed]]
45.1 fF
>
```

Figure 4.3.1 (t) cap Value through command

Some notes for illustration

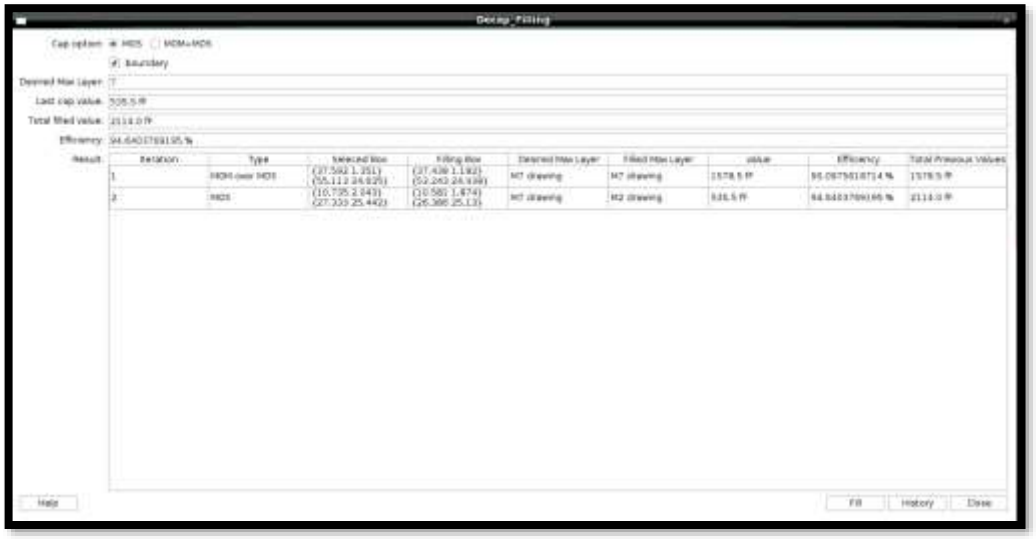


Figure 4.3.1 (u) some cases in history table

* We note that, although we can fill with metal 8 in first iteration but the max desired is M7 so the filling was with M7

* Although the max desired was M7 but in second iteration was with M2 because it was only MOS

* If the second iteration was with MOM over MOS but there is metal 5 in this area the filling will be with M4 to avoid the DRC violations

*** Important Notes**

- If there is metal 1 or 2 in the area, we can't fill with these units we can fill with separate MOS with M1 and the user will route between them. But we prefer not to fill because we think putting dummies won't be much worse than separated caps with routes between them.
- We can create a "mosCap" library at any technology and with the help of "Testbench Script" we can calculate the cap units easily

Testbench script

- Open the layout of your cap
- Make sure there is a schematic with symbol of your schematic with VSource (Vdc=1, Vac=1) and gnd.
- Make sure your design pass LVS
- Run the script:

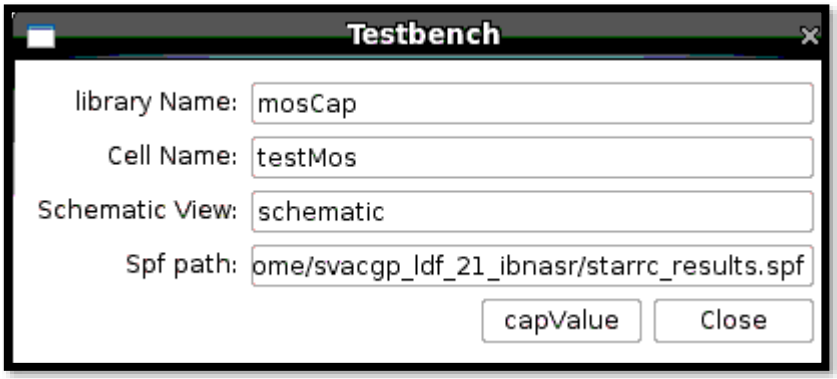


Figure 4.3.1 (v) Testbench GUI

- Insert this required data, the Schematic view is the one includes the symbol like this:

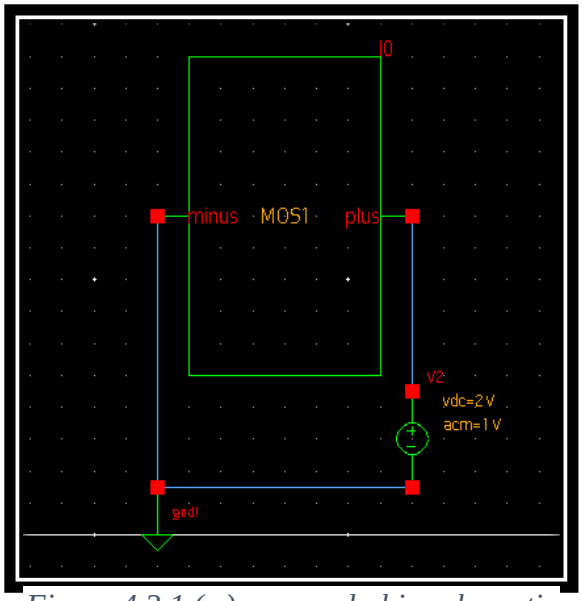


Figure 4.3.1 (w) cap symbol in schematic

- Wait until the graph with the cap value appears

4.3.2 Highly Symmetric Blocks Script

HOW the tool operates:

When the user runs the script on the console this GUI will appear:

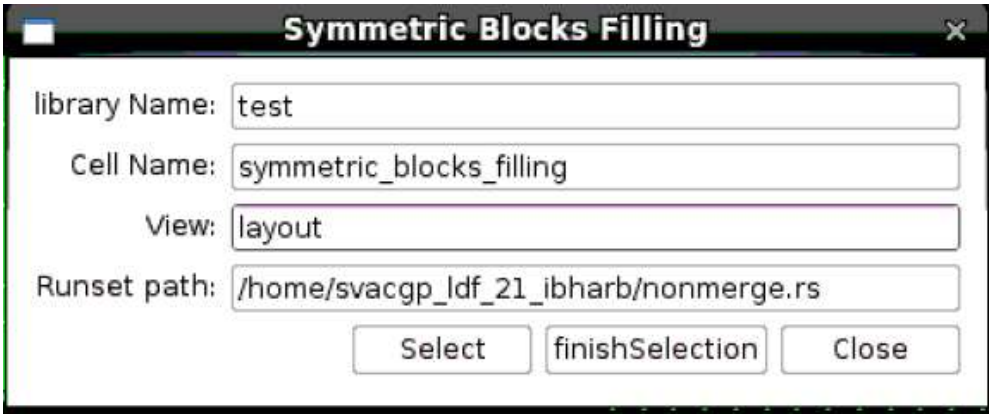


Figure 4.3.2 (a) tool GUI

Inputs of the tool:

-library Name: the name of the library that is currently opened.

-cell Name: the name of the cell that is currently opened.

-layout Name: the name of the layout that is currently opened.

- Runset path: the path of the generic runset.

First, the user should press select button after that GUI window will be deactivated and interactive command will start to wait for the user to select the first block from the lower left point to the upper right point.

After the selection of the first block, a function will check the metals that pass over the block and create another of the same metal layer in the same position but limited by the selection box.

After that, the tool will create a temporary cell and copy the first block with the created metals on it then move this block to the origin point and delete the created metals over the block on the original layout.

After that, the user should repeat the selection for each symmetric block and the tool will repeat the same steps with each block and put the block on top of each other till finish all blocks.

After finishing the selection of all blocks, the user should press finishSelection button the tool will run the generic runset on the temporary cell and import the filling in a new library then add this filling as an instance over the symmetric blocks.

The output of the tool:

Filling over symmetric blocks in a symmetric way.

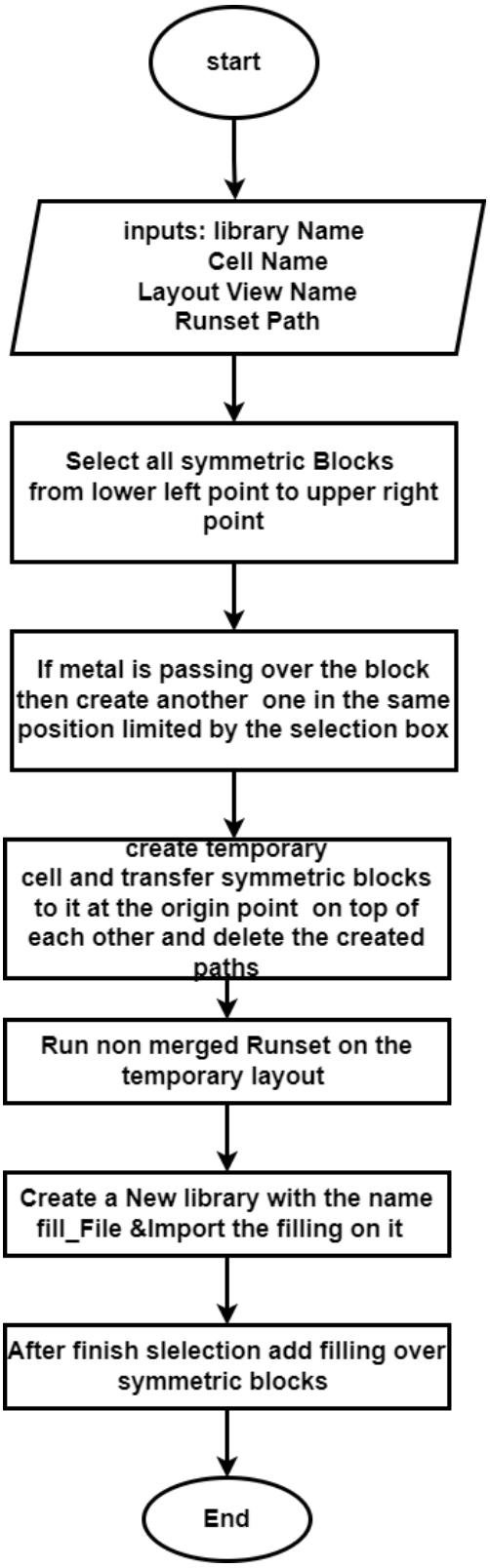


Figure 4.3.2 (b) flow chart

The strength points of this tool:

- Easy to use:
  As we collected many steps on only one button press as in finishSelection button after pressing this button the tool run filling runset and close the window that appears after finishing running runset and creates a new library and import filling on it then add the filling over each block automatic.

- Delete the temporary cell automatic:
  as this cell will not be needed anymore so the tool will delete this cell after closing the GUI.

- symmetric blocks are not fully symmetric:
  if symmetric blocks are not fully symmetric due to using shielding on a net on a block and don't use shielding in another block or may the user be forced to pass a path over a block and didn't add another one on the other block, in this case, the tool will add symmetric dummies on the common part of the blocks.

Results:

Example 1:

in this example, the symmetric are highly symmetric

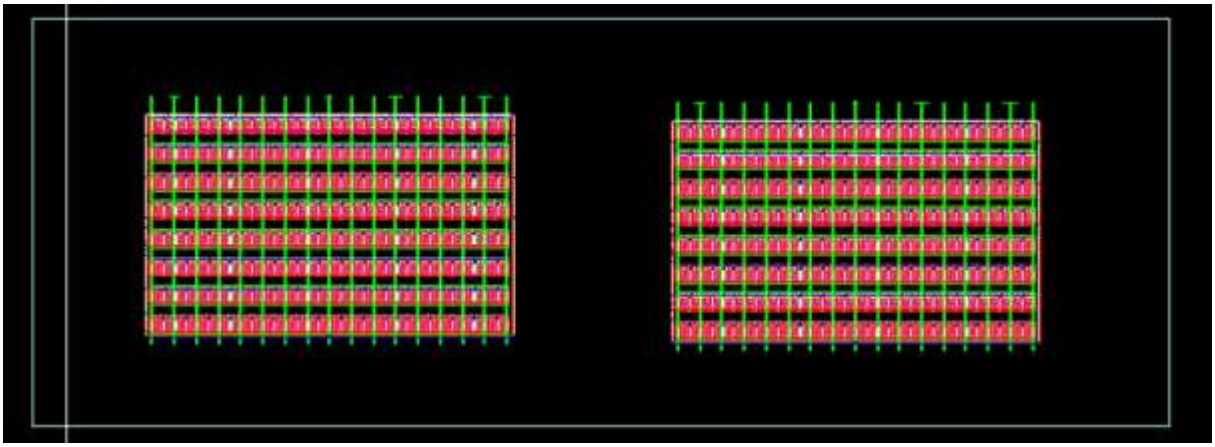


Figure 4.3.2 (c) layout before filling

Suppose that these are two blocks and we want to fill over them and these blocks are highly symmetric the doesn't have a mismatch between them.

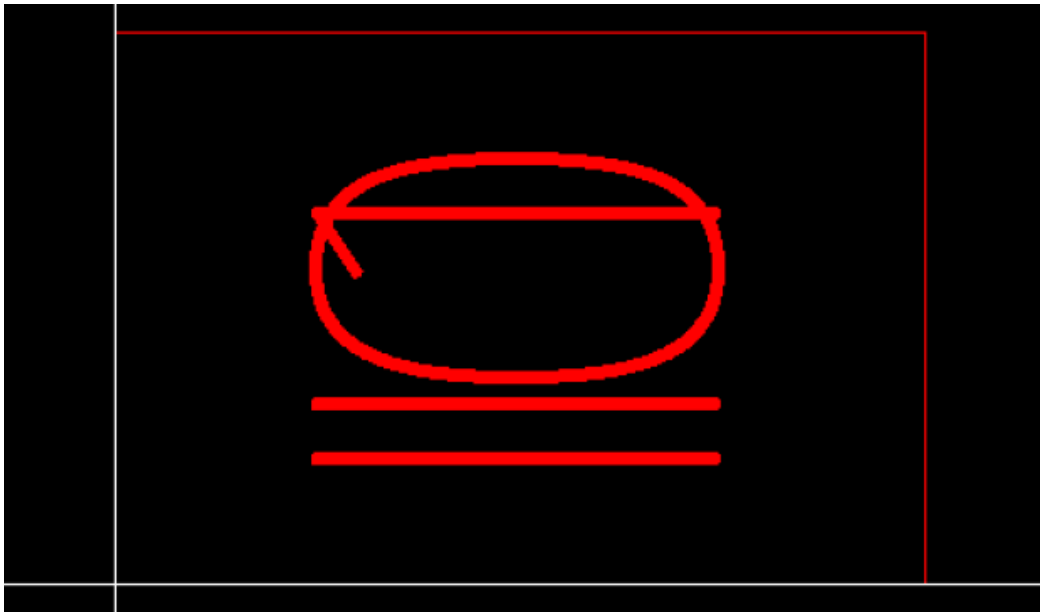


Figure 4.3.2 (d) temporary cell

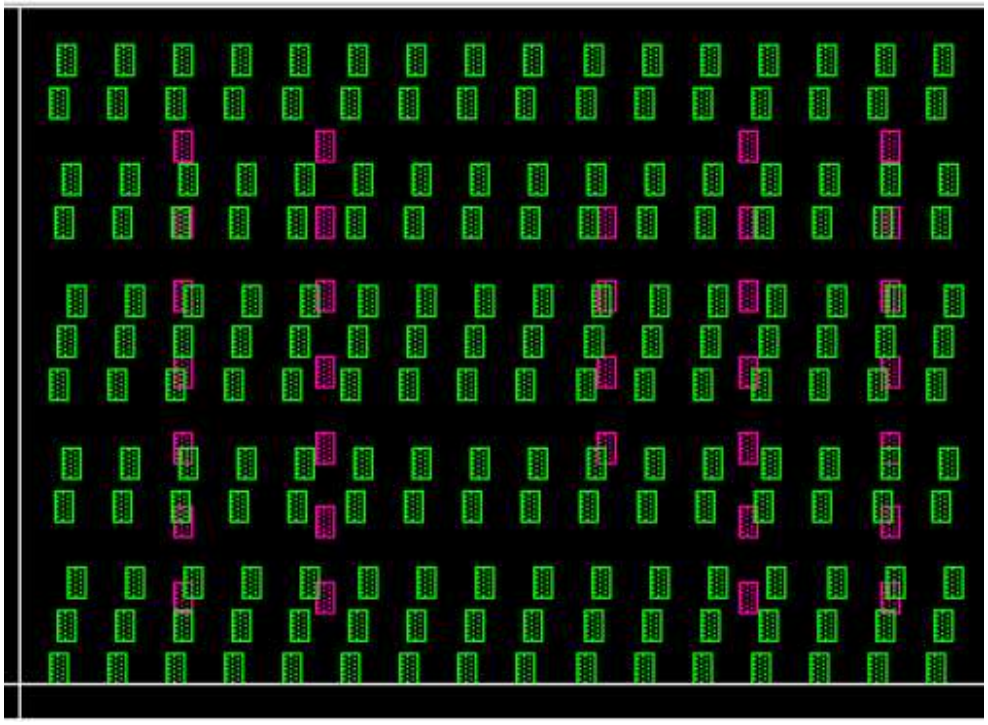


Figure 4.3.2 (e) filling dummies

These are the metals dummies that will be added over the two symmetric blocks and this cell will be added in the original layout as an instance but this cell its origin is at (0,0) point so before adding this cell in the original layout the origin point of the cell should be changed to the lower-left point of each block that the filling cell will be over it.

After running the generic runset on the temporary cell the filling will be as shown in figure 4.3.2 (f):

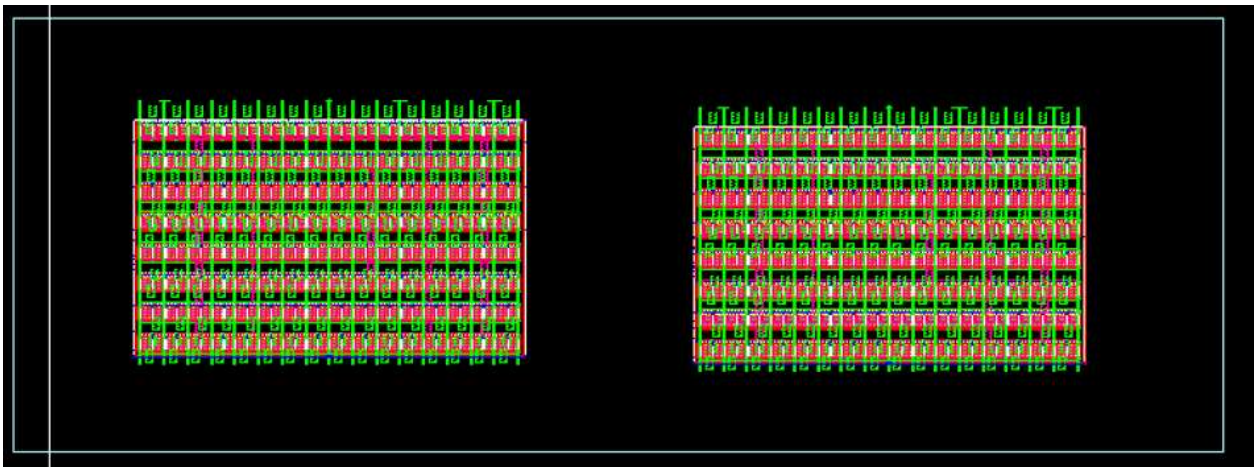


Figure 4.3.2 (f) layout after filling

The following figures show different metal dummies:

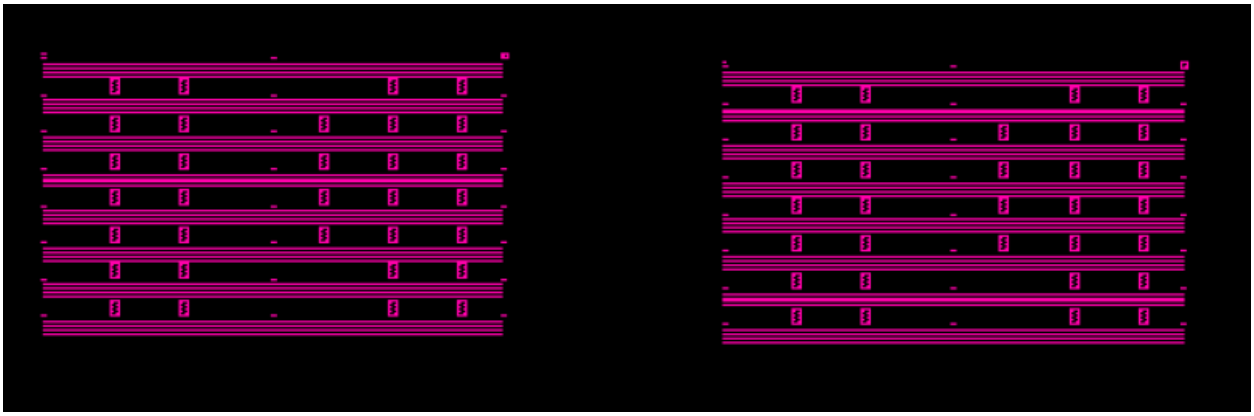


Figure 4.3.2 (g) metal 2 l dummies

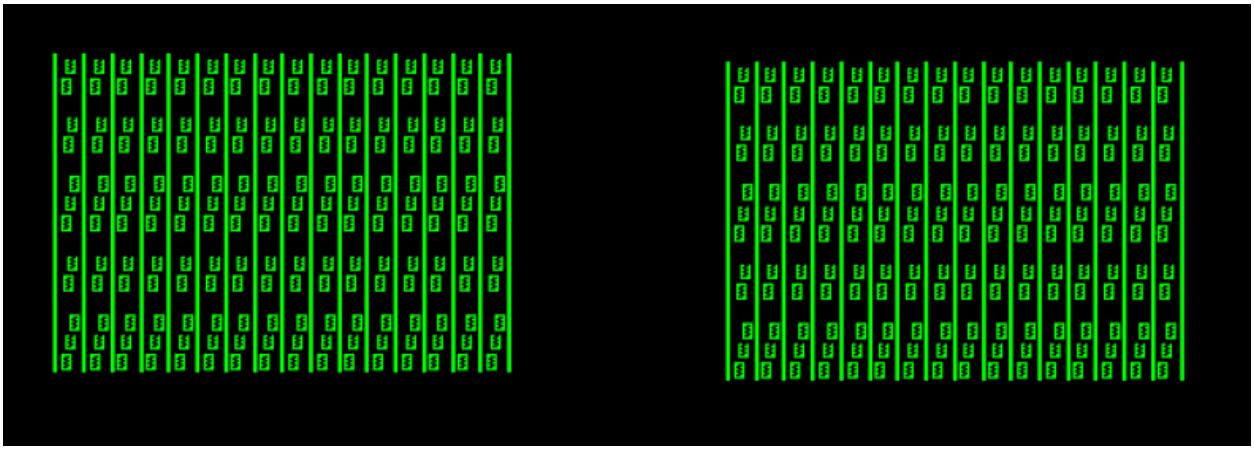


Figure 4.3.2 (h) metal 3 dummies

Example2:

in this example, the symmetric are not highly symmetric

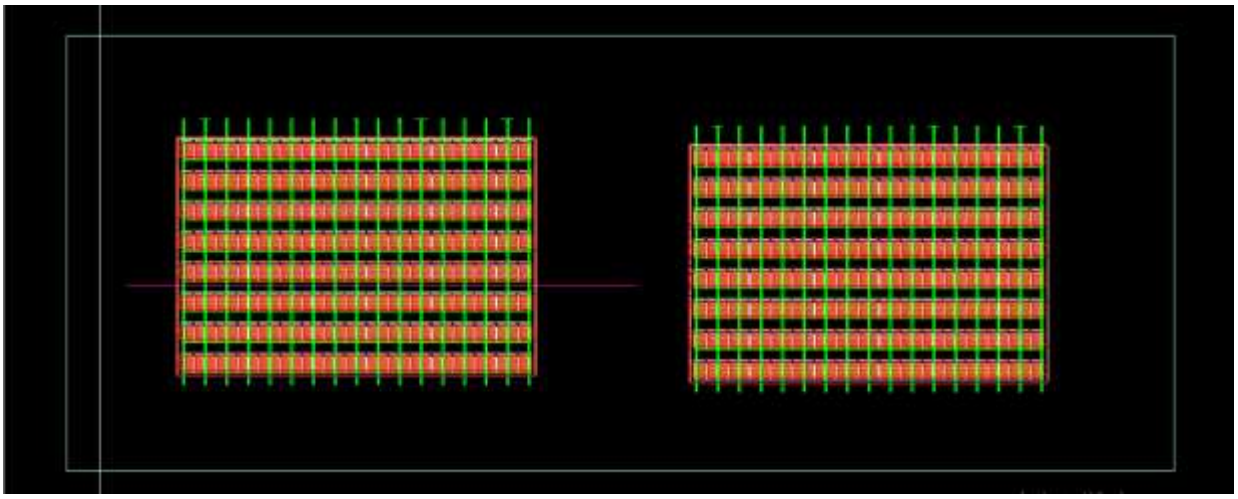


Figure 4.3.2 (i) layout before filling

Suppose that these are two blocks and we want to fill over them and these are not highly symmetric as the left block has a path of metal two and the right block doesn't have an analogous path.

Temporary cell:

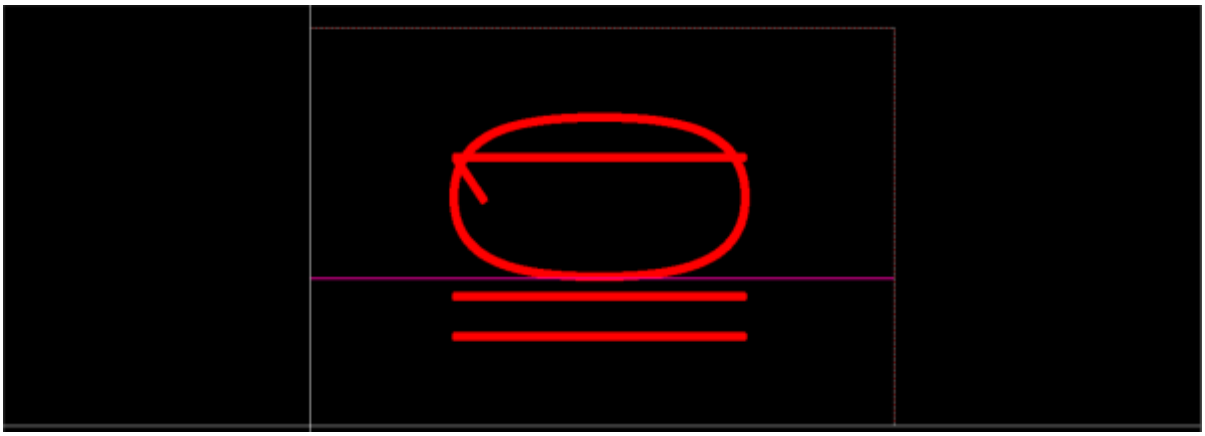


Figure 4.3.2 (j) temporary cell layout

Figure 4.3.2 (j) shows the created temporary and this figure shows that the two are at the origin point on top of each other and the mismatch path is over the two blocks.

After running the generic runset on the temporar cell the filling will be as shown in figure 4.3.2 (k):

Figure 4.3.2 (k) the filling cell layout

These are the metals dummies that will be added over the two symmetric blocks and this cell will be added in the original layout as an instance but this cell its origin is at (0,0) point so before adding this cell in the original layout the origin point of the cell should be changed to the lower-left point of each block that the filling cell will be over it.

After finishing the script, the layout will be as shown in figure 4.3.2 (l):

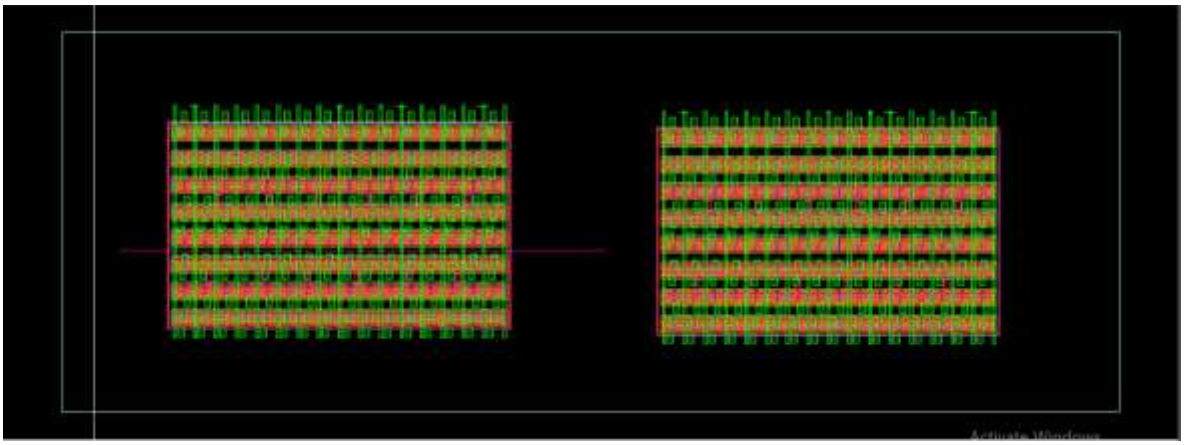


Figure 4.3.2 (l) layout after filling

The following figures show different metal dummies:

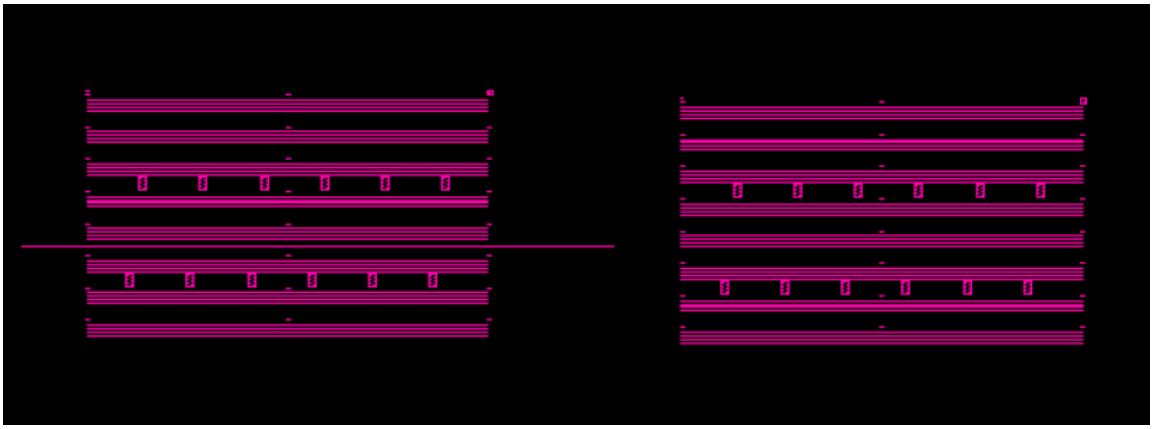


Figure 4.3.2 (m) metal 2 dummies

As shown in the figure the excess path in the left block doesn't have metal dummies over it.

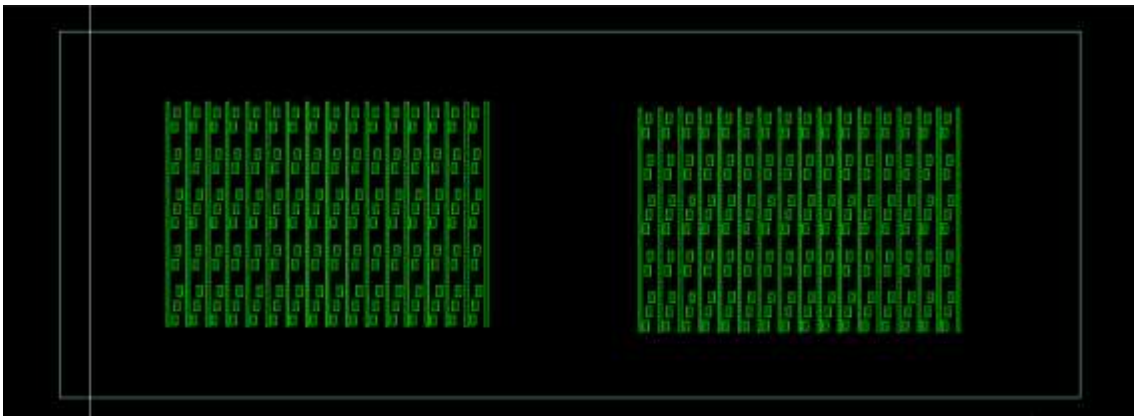


Figure 4.3.2 (n) metal 3 dummies

This figure shows the symmetry of the metal dummies over the two blocks

4.3.3 Critical Net Filling Script

How the tool operates:

When the user runs the script on the console this GUI will appear:

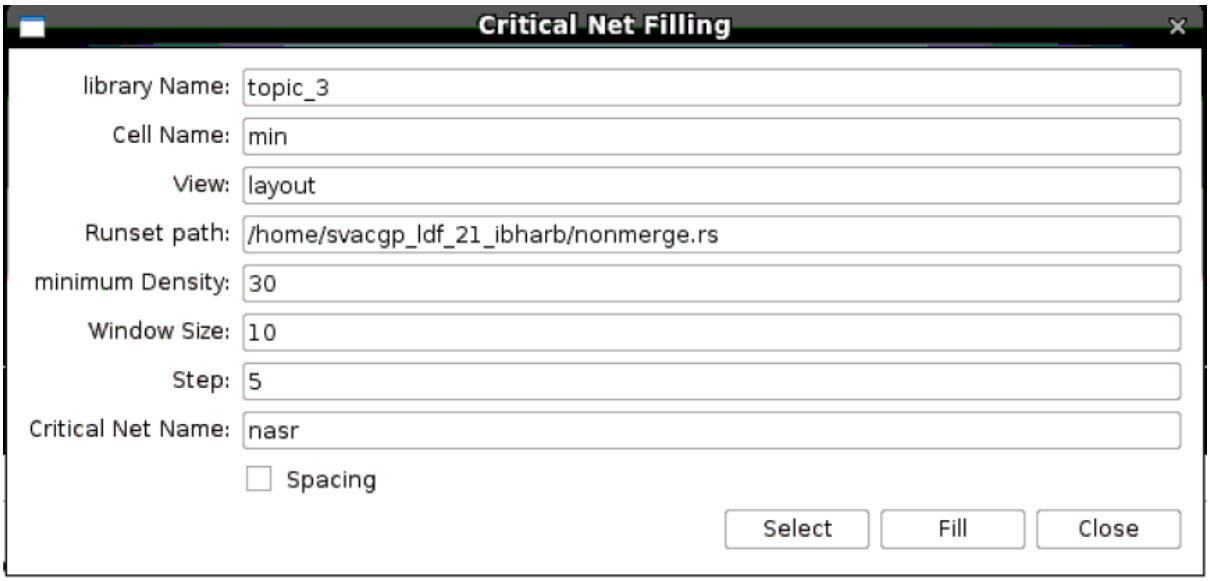


Figure 4.3.3 (a) Critical Net Tool GUI

Inputs of the tool:

-library Name: the name of the library that is currently opened.

-cell Name: the name of the cell that is currently opened.

-layout Name: the name of the layout that is currently opened.

- Runset path: the path of the generic runset.

-minimum Density: desired minimum density.

-Window Size: the size of the window that the tool will achieve minimum density on its.

-step size: the size of the step that the tool will take after finishing to achieve minimum density on the window.

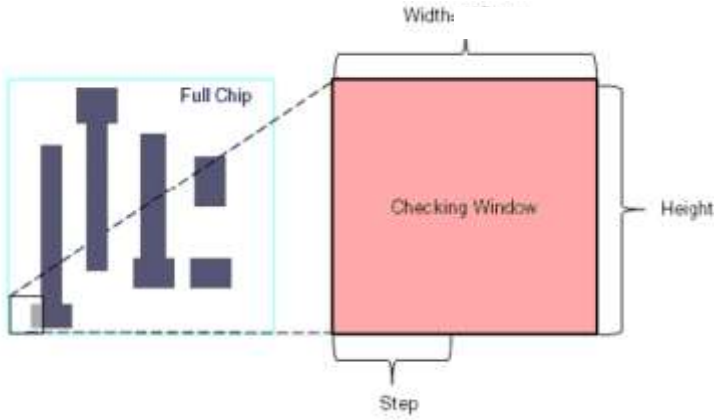


Figure 4.3.3 (b) checking window

First, the user should press select button after that GUI window will be deactivated and interactive command will start to wait for the user to select an area around the critical net

After the user select the area GUI window will be activated and a boundary box will be created to show the user the select area because if the user wants to change the selection area he could press select button again and change the selection area

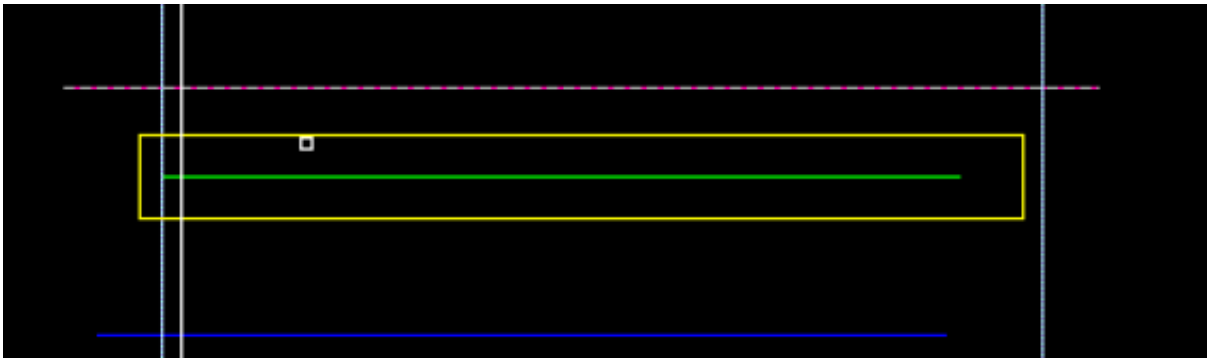


Figure 4.3.3 (c) the figure shows the selection area

After finishing the selection, the user should press fill button then the script will run the generic runset that the custom compiler uses to generate metal dummy fill and then import this dummy into a library.

After that, the script will divide the select area into small squares with sizes equal to the window size and sweep on these squares for each square the script will open the filling cell and identify which metal that will be used in this box then take a box with size equal to the size of the dummy then sweep into the square box before add dummy find the metal pass through the box if the metal type pass through the box matches the dummy metal type then the script will not add dummy in this box and take a step continue adding dummy till achieving minimum density then take a step with size equal to the input step and continue sweeping till finish all the squares.

If the space option is checked the tool will need more inputs:

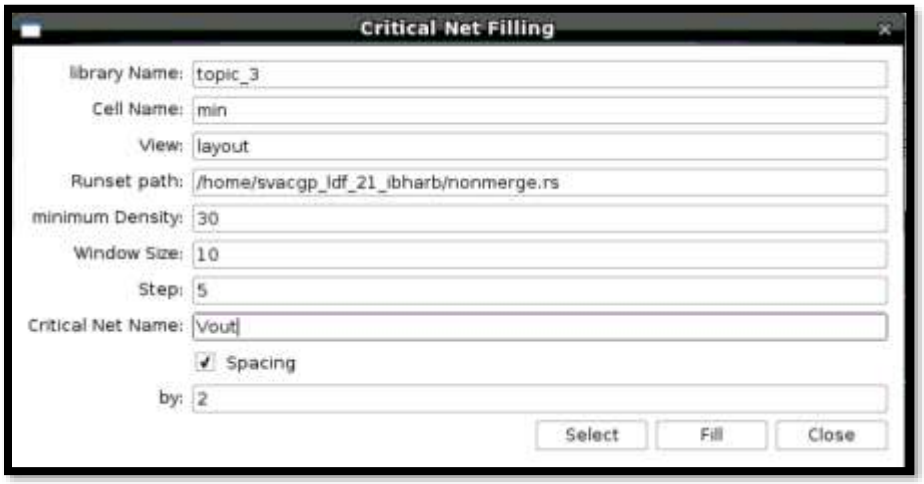


Figure 4.3.3 (d) critical net Tool GUI with space option

Excess inputs: critical net name, space distance.

And the modification the script will do is that it will check before adding a dummy that the name of the metal passing through the box doesn't match the critical net name and if that occurred for any metal type the script will not add a dummy in this box.

Outputs of the tool:

- Filling around the critical net with a minimum density in each window.
- Add blockage for each layer in the selected area to prevent an increase in the density of the selected area after running the generic runset on the entire layout.
- Generate a Table showing the density of each window for the user to make sure the minimum density is achieved in each window.

The strength points of this tool:

If the selected area is small and isn't enough to add a dummy an error message will appear the inform the user to reselect.

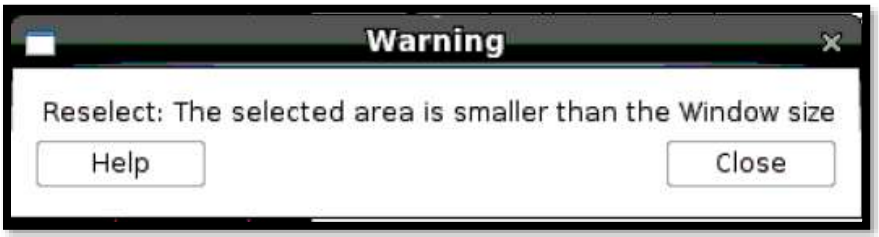


Figure 4.3.3 (e) warning message

If the user selects outside the boundary where there is no layout an error message will appear the inform the user to reselect inside the boundary.

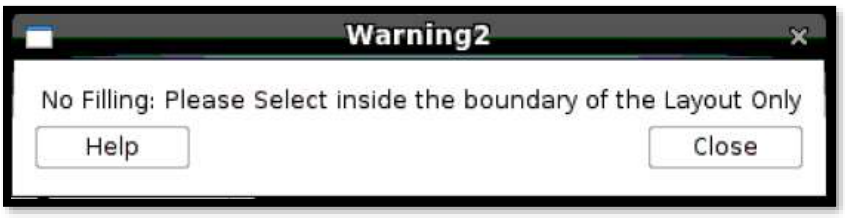


Figure 4.3.3 (f) warning message

If the selection area has part inside the boundary and part outside the boundary the tool will limit the selection area to the boundary limit and this will save time as the tool will not need to open the filling cell to check metal dummies in the area outside the boundary as this area is empty.

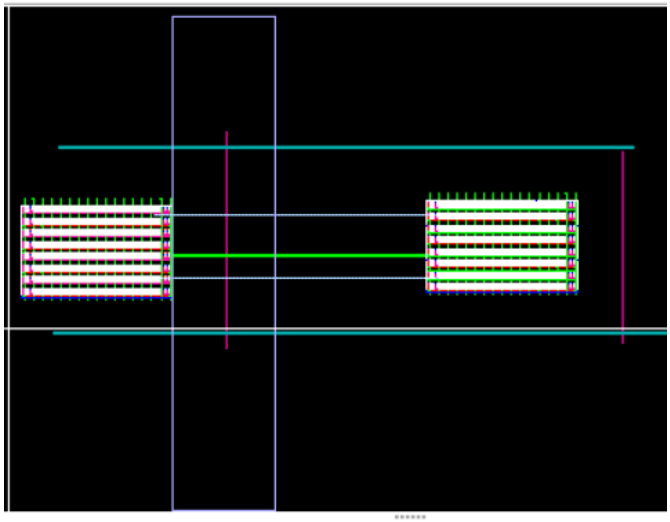


Figure 4.3.3 (g) selection area by the user

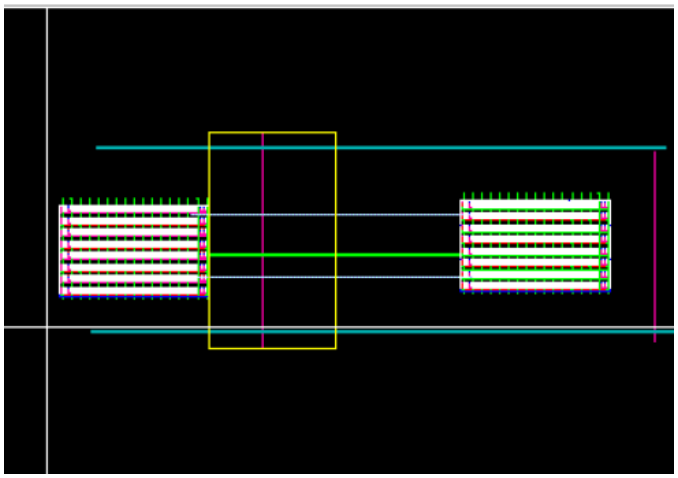


Figure 4.3.3 (h) the actually selected area that the tool will consider

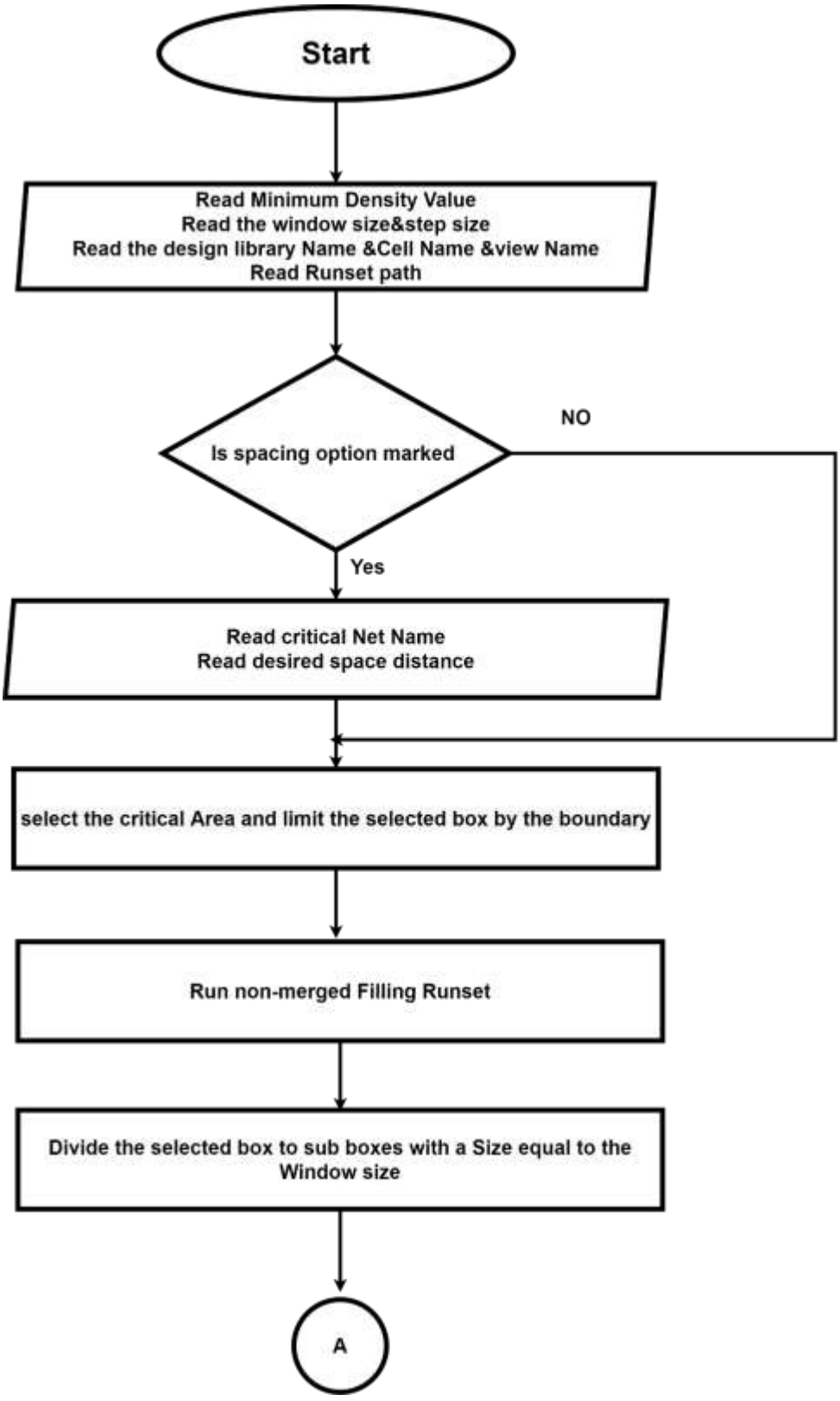


Figure 4.3.3 (i) Flow Chart

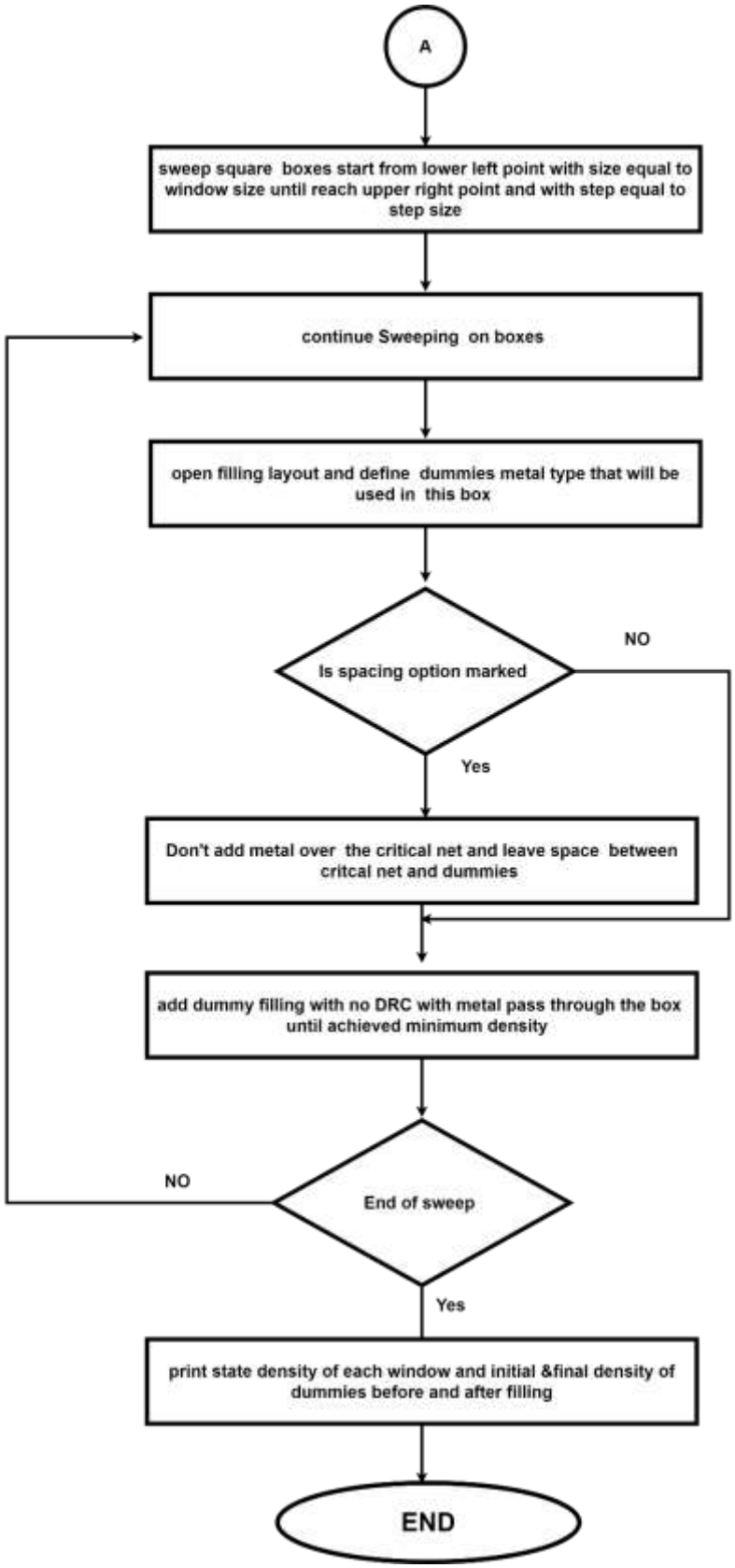


Figure 4.3.3 (j) Flow Chart

Results:

Example1:

In this example, the space option isn't checked.

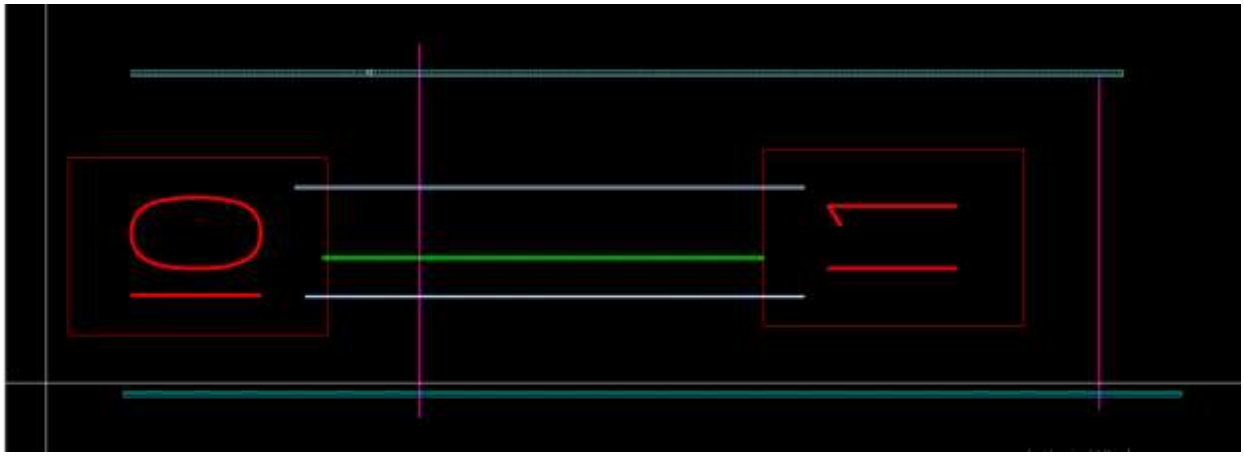


Figure 4.3.3 (k) layout before filling

Suppose the critical net is metal three and the selection area as shown in the figure:

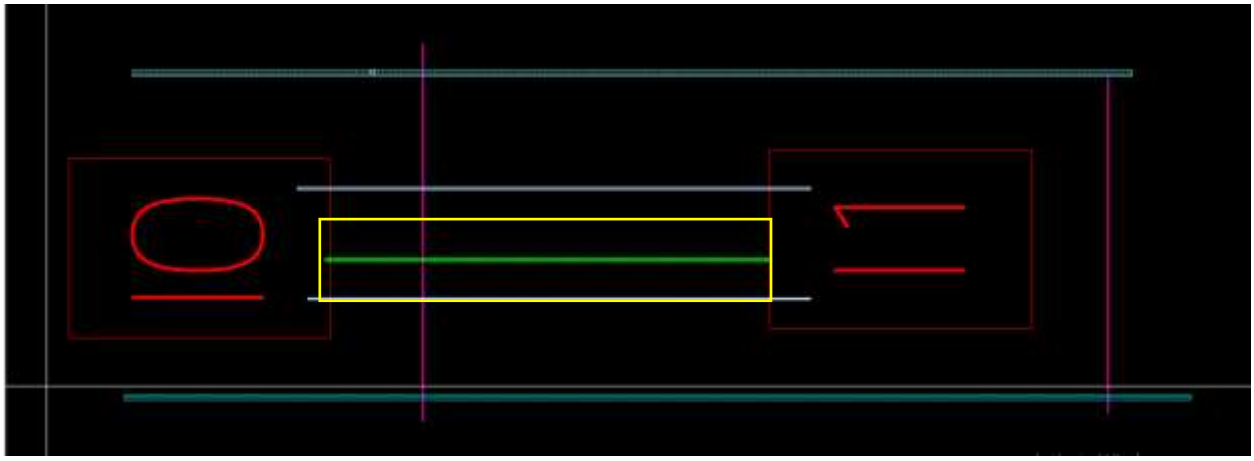


Figure 4.3.3 (l) layout after selection of critical area

After running the script on the layout:

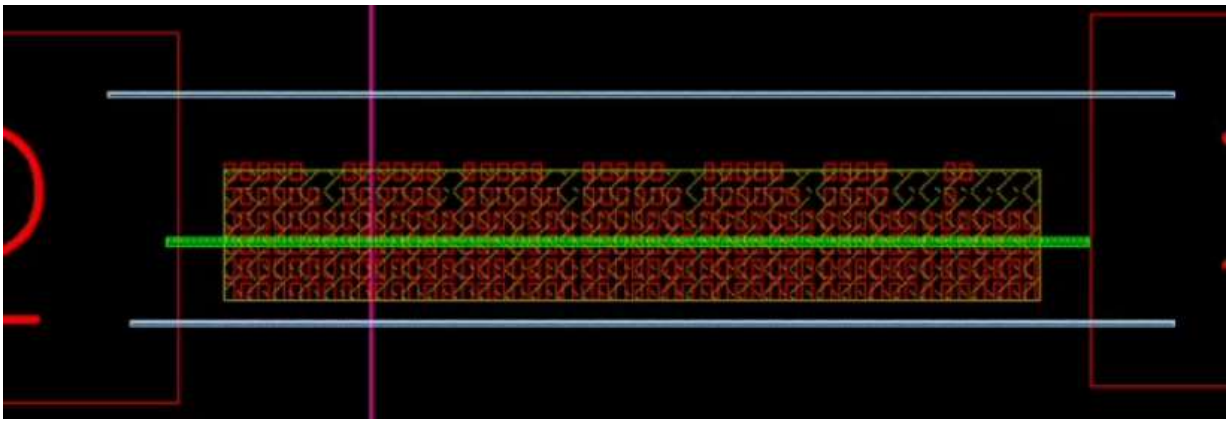


Figure 4.3.3 (m) layout after filling

The following images show different metal dummies:

Figure 4.3.3 (n) metal 1 dummies

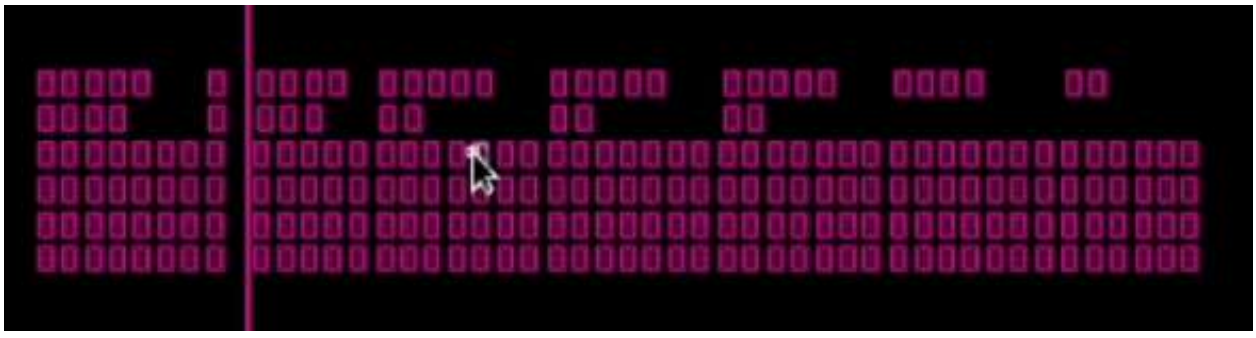


Figure 4.3.3 (o) metal 2 dummies

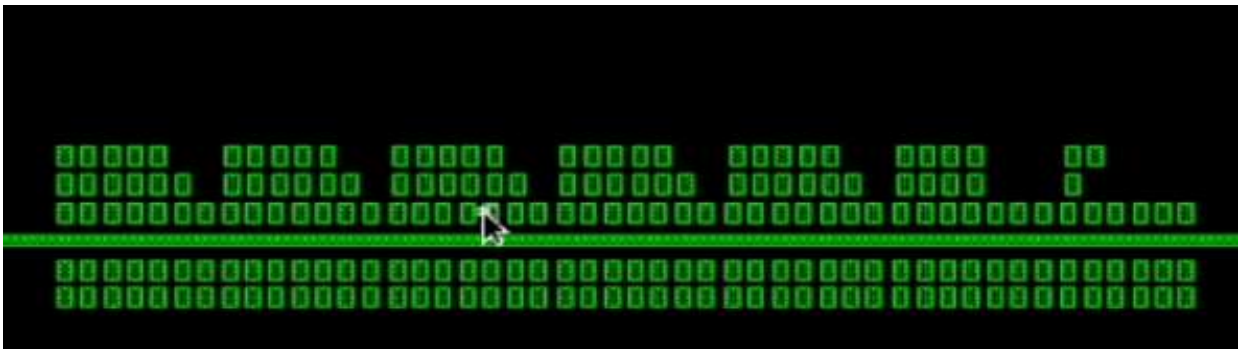


Figure 4.3.3 (p) metal 3 dummies

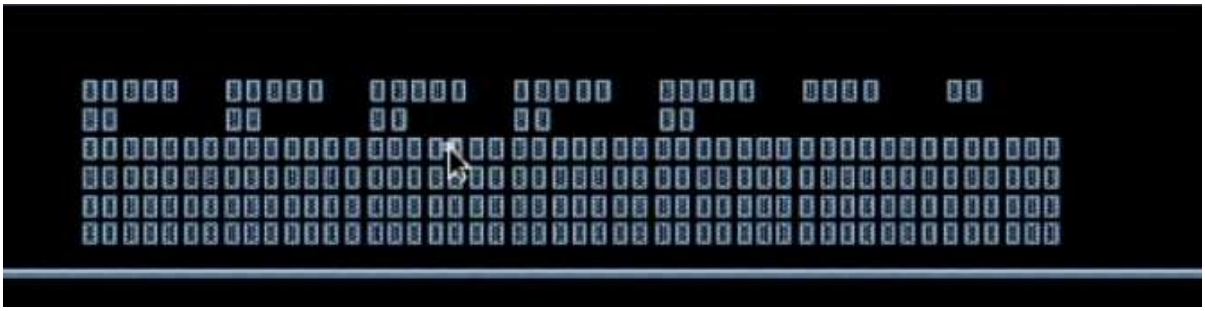


Figure 4.3.3 (q) metal 4 dummies

Table of density results:

As we discussed before the script will generate in the GUI table to show the density of each window and the initial and final density for each metal in the selected area.

Density:

Box	Metal Layer	State Density	inital Density	final Density
{41.556 8.4...	M1 drawing	30.1075268...		
{41.556 8.4...	M2 drawing	30.1075268...		
{41.556 8.4...	M3 drawing	30.4783092...		
{41.556 8.4...	M4 drawing	30.1075268...		
{41.556 8.4...	M5 drawing	30.1075268...		
{46.556 8.4...	M1 drawing	30.1075268...		
{46.556 8.4...	M2 drawing	30.1075268...		
{46.556 8.4...	M3 drawing	30.4783092...		
{46.556 8.4...	M4 drawing	30.1075268...		
{46.556 8.4...	M5 drawing	30.1075268...		
{51.556 8.4...	M1 drawing	30.0589700...		
{51.556 8.4...	M2 drawing	30.0589700...		

Figure 4.3.3 (r) Table of result

Example 2:

In the example the space option is checked:

The input space in the case is 0.5um

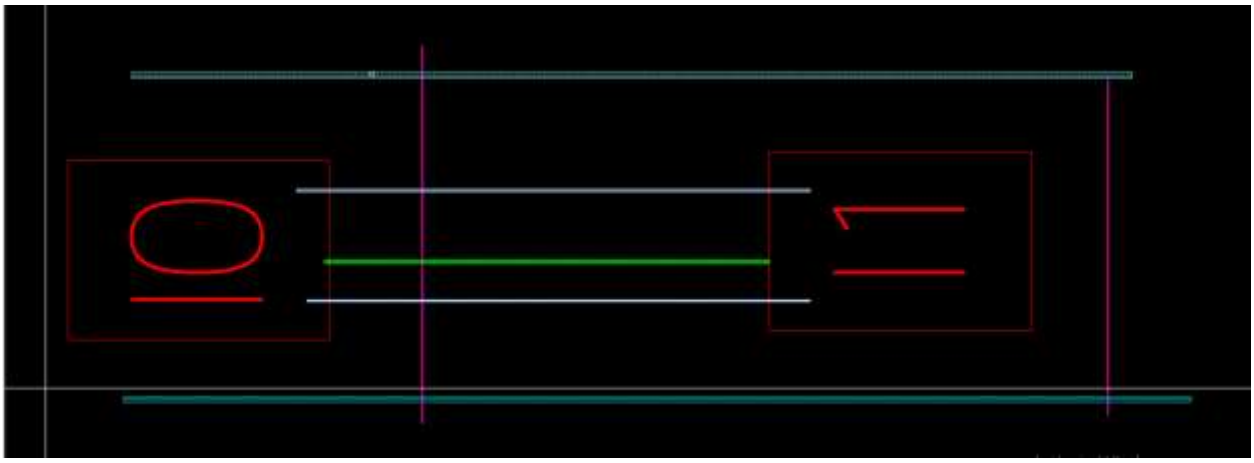


Figure 4.3.3 (s) layout before filling

Suppose the critical net is metal three and the selection area as shown in the figure:

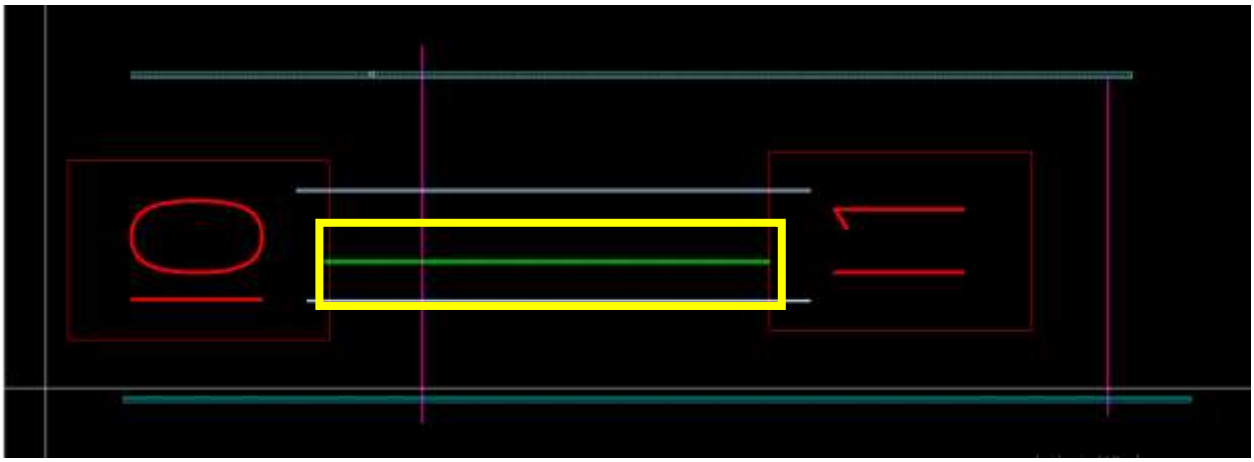


Figure 4.3.3 (t) layout after selection of critical area

After running the script on the layout:

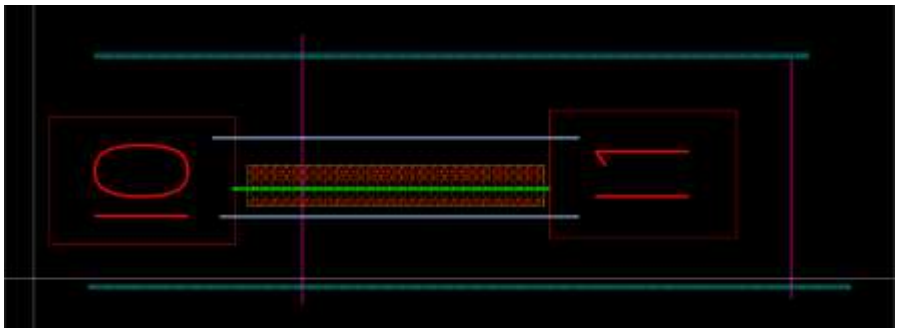


Figure 4.3.3 (u) layout after filling with space option

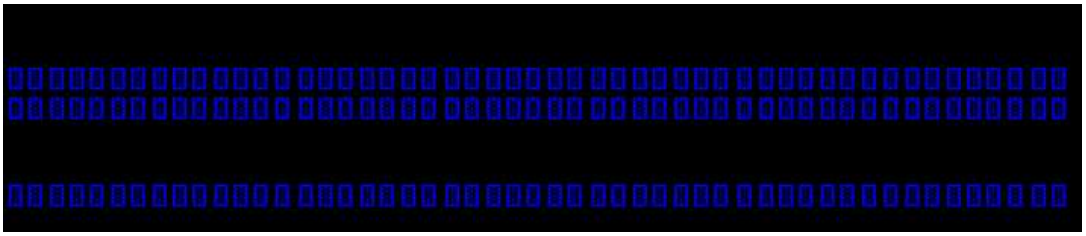


Figure 4.3.3 (v) metal 1 dummies

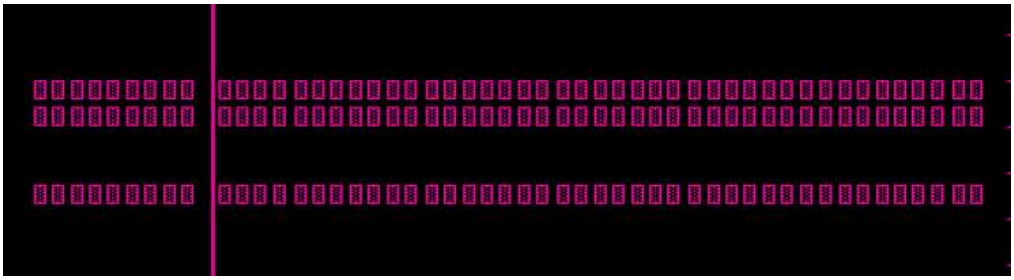


Figure 4.3.3 (w) metal 2 dummies

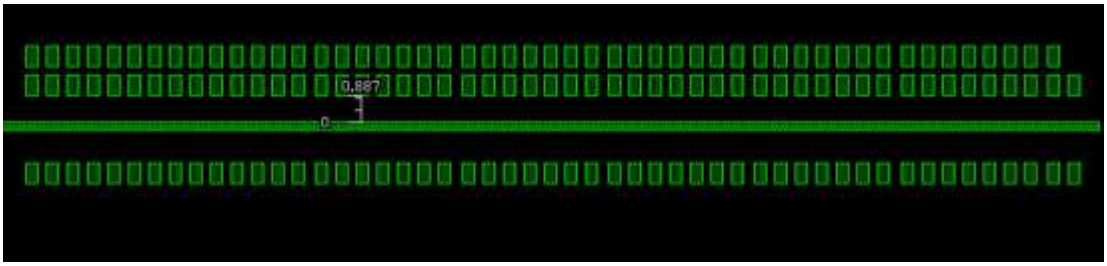


Figure 4.3.3 (x) metal 3 dummies

These figures show that the space between the critical net and dummies is greater than the input space 0.5um and there are no dummies of any metal type in that space.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

According to Filling Tool:

Filling is very important issue that the layout designer should consider in totally digital circuits, totally analog circuits and digital and analog mixed signal circuits. We should be aware of some critical issues related to the filling done by the generic runsets like filling around critical nets with min density, filling over the highly symmetric blocks with symmetric filling and filling with decoupling caps in empty areas instead of floating metal dummies that are parasitic capacitance to know later.

According to RC Delay Improvement tool:

In recent technology nodes, the delay of the interconnects became the most dominant delay that could limit the whole application speed and the layout designer must work very hard to reduce it especially for high-speed applications, The complexity comes from the multiple options that can improve the delay and the effect of each technique can not be seen until the post-layout simulation phase. Our tool works specially to reduce this gap between the pre-layout simulation and post-layout simulation by performing post-layout simulation for the critical interconnect to get the best delay possible and tells the layout how to draw this critical net to get the best delay.

According to Shielding tool:

Shielding is one of the most important solutions to reduce crosstalk. crosstalk is a big problem in deep sub -micron technology due to shrinking in Wire geometries in the nanometer process technology leads to an increase in coupling capacitance. Shielding helps in reducing both coupling capacitance and inductive coupling. So, we decided to make a shielding tool with a simple GUI to be fast and effective. Shielding tool can shield with three different styles {Parallel, Tandem, Coaxial}. Each style has its types. Shielding tool can alert with warning massages if there is any error from the user.

5.2 Future Work

According to Filling Tool:

- Filling around critical net should consider the density gradient:
  in our tool we are interested in the selected region only, as an enhancement we should consider the density gradient outside the selected area
- Filling around critical net should consider symmetry above & below the critical signal:
  in our tool we start filling from lowerleft point of the selected area, as an enhancement we start from the lowerleft point of the critical signal.

- Filling around critical net should consider differential signals case:
  in our tool we deal with single signal as an enhancement we can deal with differential signals.

- Filling over highly symmetric blocks should put suitable dummies to make the blocks completely symmetric not only the filling:
  in our tool we are interested in making the filling symmetric as an enhancement we can create extra dummies to make the blocks themselves symmetric
- Filling over highly symmetric blocks should take surroundings into consideration and block these areas not to be deformed by generic runsets later:
  in our tool we are interested in filling coming from the blocks themselves as an enhancement we should take the surroundings and block these areas.
- Filling with decoupling caps should consider the max density before filling:
  in our tool we are interested in filling with decaps in every available area but as enhancement we should consider the max density before filling
- Filling with decoupling caps should be automatically created without predefined library:
  in our tool we create decoupling caps library to fill with as an enhancement the tool is smart enough to automatically created the suitable decap.

According to RC Parasitic improvement tool:

- Multiple inverter cells can be created, and the tool should select the most appropriate ones according to the driver and load devices.
- Interconnects with bridges (Multi Paths interconnects) delay can be improved by iterating on metal layers and width at the same time instead of the width only.
- The tool can save the data of the interconnects each time it runs to reduce the time in future runs.
- A look-up table can be constructed for basic types of interconnects to reduce the time consumed by each iteration.
- The tool should extract the DRC rules from the Design Rule Manual.
- Provide techniques for the differential signals.

According to Shielding tool:

- Develop a DRC checker in Shielding tool that can detect if there are any DRC errors before routing and can solve them.
- The Tool can detect the best case for shielding if the user selects the aggressive signals. So, the shielding tool can detect the shield style and its type. it can also detect the shield line geometries width and spacing.

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