Integrated Piezo-electric energy harvester module

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Nomenclature

NTRA: National Telecom Regulatory Authority

RF: Radio Frequency waves

AC: Alternating current

DC: Direct current

MPPT: maximum point power tracking

IOT: Internet of things

DRC: design rule checking

LVS: layout versus schematic

PZT: piezoelectric transducer

CTS: charge transfer switch

Acknowledgments

First, we would like to thank Dr. Hassan for his guidance during the course of the project. Without his level of commitment and desire to watch his students succeed we wouldn't be where we are today. Additionally, we would like to thank our families for their support through this project. We would also like to mention the name of Si-Ware for their support. and last but not least we would like to thank Eng. Mahmoud Hassan Kamel from Minia University and Abdelrahim Mohamed Elnabway for helping us with the layout and the Verilog A. Finally, all the thanks goes to National Telecom Regulatory Authority (NTRA) for providing technical and financial support for our project.

Abstract

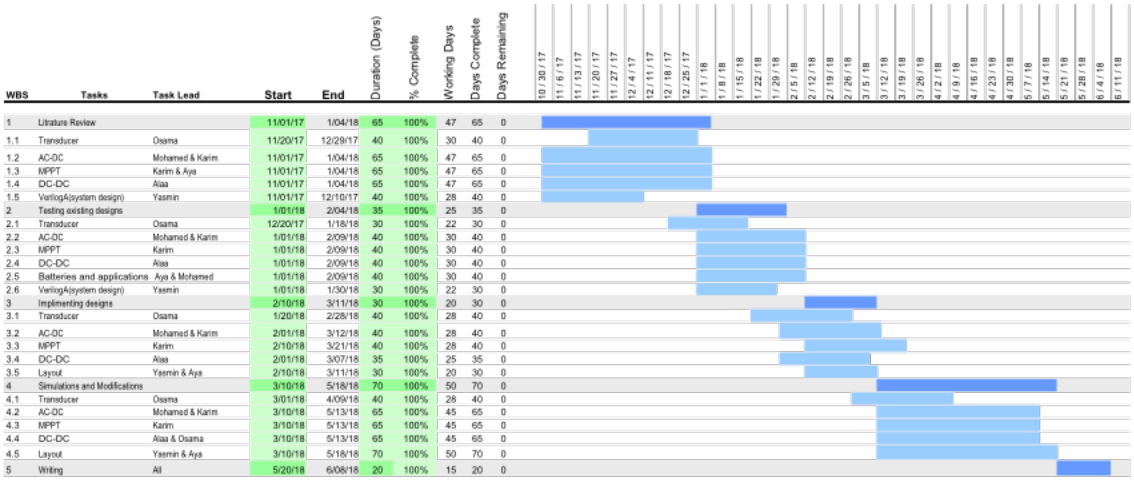
Energy harvesting is used for capturing different sources of energy from the environment such as solar power, heat, mechanical power and RF. Harvesting is highlighted to be an alternative for conventional batteries which has an end and not friendly to the environment. Some applications such as implanted devices in the body and satellites systems work on energy harvesting as conventional batteries are large and we cannot change them continuously. Because of that, Energy harvesting have become one of the hottest topics in industry and research. The need for long life battery becomes demanded and there is a lot of effort has been made in this area. So, the main core of our project is to provide a whole system that brings its energy from harvesting a piezoelectric energy and controlling it to give a fixed DC level to any application. The main problems that faced us were creating an appropriate model for generating piezoelectric energy, getting the maximum power from this harvester, converting the resulted AC voltage to DC voltage and controlling this DC voltage to providing the voltage needed for the application. Converting piezoelectric energy into electric energy is done by the energy transducer. COMSOL simulation has been used in this project to simulate the transducer model and produce results that can be used to provide voltage for the entire system. Based on this model, Verilog-A is used to produce a block with the same results so it can be used with the other blocks in Cadence virtuoso environment. To extract maximum power from these harvesters, MPPT block is very essential to track the maximum power point. The output voltage of the transducer is sometimes AC current which cannot be delivered to the load without rectification, so AC-DC block does this function to limit the current that derived from the transducer. DC-DC converter manages the voltage that derived from the AC-DC converter to match this voltage with the load need. In our project, we designed every block at the transistor level and collect them together to get the overall function of the system. After this, a layout for the whole system has been produced. Using software tools and putting all our effort made all the system from the transducer to any application we want to turn on.

This report will first introduce the model for transducer using COMSOL(Piezoelectric model). Then, the energy management unit and its simulations using Cadence virtuoso will be presented containing AC to DC converter, MPPT and DC to DC converter. Concerning each block, a brief preview will be done to show previous work then our work will be presented. Then, a layout for the whole system will be presented with its area. Finally, all the system with its amazing results will be showed.

Planning (Gantt chart)

This project to be carried out has been much planned. Before its beginning, a general planning was done for months, to give us an idea of how much time we could dedicate to each task. This planning would be constantly revised, but it would allow us to organize the time we had. Once this general planning was designed, an organization of objectives per week began. This method attempted to increase efficiency, since small objectives had to be accomplished every day, which resulted in constant progress.

We can see the whole distribution of tasks and the times in which they have been carried out in a much more intuitive way in the Gantt Diagram that follows:



WBS	Tasks	Task Lead	Start	End	Duration (Days)	% Complete	Working Days	Days Complete	Days Remaining
1	Litrature Review		11/01/17	1/04/18	65	100%	47	65	0
1.1	Transducer	Osama	11/20/17	12/29/17	40	100%	30	40	0
1.2	AC-DC	Mohamed & Karim	11/01/17	1/04/18	65	100%	47	65	0
1.3	MPPT	Karim & Aya	11/01/17	1/04/18	65	100%	47	65	0
1.4	DC-DC	Alaa	11/01/17	1/04/18	65	100%	47	65	0
1.5	Verilog(system design)	Yasmin	11/01/17	12/10/17	40	100%	28	40	0
2	Testing existing designs		1/01/18	2/04/18	35	100%	25	35	0
2.1	Transducer	Osama	12/20/17	1/18/18	30	100%	22	30	0
2.2	AC-DC	Mohamed & Karim	1/01/18	2/09/18	40	100%	30	40	0
2.3	MPPT	Karim	1/01/18	2/09/18	40	100%	30	40	0
2.4	DC-DC	Alaa	1/01/18	2/09/18	40	100%	30	40	0
2.5	Batteries and applications	Aya & Mohamed	1/01/18	2/09/18	40	100%	30	40	0
2.6	Verilog(system design)	Yasmin	1/01/18	1/30/18	30	100%	22	30	0
3	Implementing designs		2/10/18	3/11/18	30	100%	20	30	0
3.1	Transducer	Osama	1/20/18	2/28/18	40	100%	28	40	0
3.2	AC-DC	Mohamed & Karim	2/01/18	3/12/18	40	100%	28	40	0
3.3	MPPT	Karim	2/10/18	3/21/18	40	100%	28	40	0
3.4	DC-DC	Alaa	2/01/18	3/07/18	35	100%	25	35	0
3.5	Layout	Yasmin & Aya	2/10/18	3/11/18	30	100%	20	30	0
4	Simulations and Modifications		3/10/18	5/18/18	70	100%	50	70	0
4.1	Transducer	Osama	3/01/18	4/09/18	40	100%	28	40	0
4.2	AC-DC	Mohamed & Karim	3/10/18	5/13/18	65	100%	45	65	0
4.3	MPPT	Karim	3/10/18	5/13/18	65	100%	45	65	0
4.4	DC-DC	Alaa & Osama	3/10/18	5/13/18	65	100%	45	65	0
4.5	Layout	Yasmin & Aya	3/10/18	5/18/18	70	100%	50	70	0
5	Writing	All	5/20/18	6/08/18	20	100%	15	20	0

Figure 1: Timeline of the project

1 Introduction

This first chapter describes the project expressed as a report. A basic ingredient is for sure the motivation for what the project is done and developed. Once there is a good and powerful reason to do the project, there is the need of fixing some goals to achieve. After that it is important to think on how the project will be and what is the project going to include, defining the limits coordinated with the execution time. Then, it is almost the time to collect the main conclusions that have been reached. Finally, it is very important to set the basic layout of the whole report.

1.1 Motivation

The trend in the whole world right now is IOT systems. All the countries and corporations compete to provide a constant and life-long energy sources to these systems and different wearable devices. But it is not that easy, as there are a lot of problems related to the instability of the energy sources, most devices used in the systems are remote so it is almost impossible to change its batteries from time to time and beside all of that they are usually insufficient in energy. Many solutions have been presented but the most popular and effective solution is energy harvesting. So that a renewable energy will be provided without worrying of changing any batteries. Hearing and reading about that make it impossible to us to not get excited about this topic. The information through internet and coming from some interesting articles and references made us think in a complete power management system for a transducer of our own. Our most important motivations are the followings:

1. The project is ambitious and rigorous, with innovative processes and interesting results, based on teamwork.
2. Si-ware challenge has been the main motivation. A big corporation support and sponsor the project.
3. The topic is a good one for being part of the final university project. All time spent in the report and using software tools will for sure have its reward and can be then reflected in the academic record.
4. Getting a funding from a big corporation like NTRA makes us believe this project is really a promising project that can be related directly to industry.
5. Personal satisfaction is also a motivation to go further in the project. Learning to do all processes, approaches, conclusions and overcoming problems ourselves are skills that can only be learned by working hard on something you like.

1.2 Objectives

Regarding the objectives to achieve, we have listed all of them divided in two sections; fixed steps to accomplish with the design application and general goals related with the project.

System design goals:

- Design a piezoelectric transducer model that gives different AC voltages at different frequencies.
- Design AC-DC converter to convert the AC voltage efficiently to constant DC voltage.
- Design MPPT to trace the maximum power that the harvester can produce.
- Design DC-DC converter to control the input voltage and provide an appropriate voltage to the application.
- Creating the layout for the whole system.

General goals:

- Be part of the project from the start, continue the whole process and see its own conclusions.
- Learn and experience how to design, simulate and produce a layout for a functional system.
- Learn how to collect all the results in a professional report summarize all that has been done and providing ideas for future research.
- Overcome all problems and obstacles during the project.
- Teamwork relation and planning to reach the same purposes.

1.3 Methodology

In every project, methodology followed is one of the most relevant key points. It is based on a detailed and well-planned organization which aims to achieve small goals constantly.

To do so, Facebook application has been a very useful tool to post all information safe on Internet. Also, beside Facebook Hangout application has been used to provide a communication among members of the project and task division.

Regarding organization, weekly reunions with our supervisor have been very important to take a look in the small goals to achieve, evaluate the process with perspective and reconsider some aspects during the project performance.

Working level should be equilibrated and all the members must take part in all sections and decisions. Even though, there are some tasks from which one of the members is more specialized than the others. So by following this technique:

- Piezoelectric model: Osama was responsible of providing its simulation on COMSOL with perfect results and writing a Verilog-A code to implement it in Cadence virtuoso environment.
- AC-DC converter and MPPT: Karim and Mohamed were responsible of designing and simulating these two blocks combined in only one using Cadence virtuoso.
- DC-DC converter: Alaa and Osama were responsible of designing and simulating this block with putting a cap to represent the battery and a resistance to represent the application at the end of it using Cadence virtuoso.
- The whole system: Alaa and Karim were responsible of combining the different blocks together in one system and making sure that it is a functional system can be used in running different applications using Cadence virtuoso.
- Layout: Aya and Yasmine were responsible of creating the layout of the whole system with running DRC, LVS and PEX using Cadence virtuoso.

It must be said that teamwork has been fundamental. Although everyone was responsible about specific section, each member has understood the whole project equally. Finally, this deal in the report's method implies writing down everything we have done. All reports have been made following a self-made template, the designing and simulating processes are written and described in detail.

1.4 Main conclusions

The most important piece of information that we get out of this project is that energy harvesting systems will invade the world. The trend now in the world is already towards using renewable sources and IOT systems. So, the conclusion of all of that is using energy harvesting system like the one produced from this project. The first conclusion is a piezoelectric small structure can be built easily and gives around 400 uW to support the whole system. The second one is that a very efficient AC-DC converter can be implanted on a chip. MPPT block also is so important in the system as it tracks the maximum point power so minimum energy will be wasted. And finally, to give the application a constant high voltage the DC-DC converter proved that it is very useful in doing this job. Although it wastes some energy, the efficiency of the whole system is still very good. That makes us believe that one day all the energy generators systems in the world will be replaced by a one like this.

1.5 Layout of the report

The report has been well organized to give a description of what have been done during the last ten months, what we have learned and which tools we used to design and simulate our systems. We began by the abstract which gave a brief description of the whole report. Then, a planning

section was presented to show the schedule that has been followed to make this project successful. The report has been divided into five chapters that cover all the research, designing and simulating works.

- Chapter 1: Introduction to the project consists of the motivation, the main objectives, methods we applied in our project and main conclusions. This chapter provides the big picture of the whole project.
- Chapter 2: Literature Survey on previous scientific published work related to our project. It presented also the advantages and disadvantages of the previous works that made us go to specific directions in our project.
- Chapter 3: System architecture of the project with sections that describe the different blocks of the system. The first section describes the piezoelectric module with its simulation. The second section describes the AC-DC converter with its different kinds. The third section describes the MPPT with its different algorithms and its blocks. The fourth section describes the capacitor divider. The fifth section describes the DC-DC converter and its different kinds.
- Chapter 4: Simulation of the AC-DC converter, MPPT and the DC-DC converter.
- Chapter 5: The simulation of the whole system together. The layout of each block then the layout of the blocks combined.
- Chapter 6: Economic analysis of the project after producing its layout and knowing the exact area that can be implanted in.
- Chapter 7: Conclusions of the results from different blocks and from the whole system with comments on them. Recommendations and ideas for coming projects and researches.

2 Literature Review

2.1 Previous works

[1] A Self-Supplied Inertial Piezoelectric Energy Harvester with Power-Management IC: This paper presents a self-supplied energy generator, which includes a MEMS harvester hybridly integrated with its power management circuitry for autonomous charging of an energy reservoir. Power management is achieved with three sub-circuits, MOS switches and an active diode for low-dropout rectification, a shunt pass system to increase harvesting efficiency and a trickle battery charger.

[2] Sensitivity Analysis and Energy Harvesting for a Self-Powered Piezoelectric Sensor: In this article, a self-powered piezoelectric sensor is studied, in which one piece of piezoelectric element is simultaneously used as a sensor and a power generator under vibration environment. The energy is harvested by connecting the piezoelectric material with a diode D1 with forward voltage Vforward

(constant) and a reservoir capacitor Cr. The diode is used as a rectifier to rectify the AC signal from the piezoelectric material into DC signal; the energy can then be stored in the capacitor Cr.

[3] A Low-Power CMOS Piezoelectric Transducer Based Energy Harvesting Circuit for Wearable Sensors for Medical Applications: In this paper, a low-power CMOS full-bridge rectifier is presented as a potential solution for an efficient energy harvesting system for piezoelectric transducers. The energy harvesting circuit consists of two n-channel MOSFETs (NMOS) and two p-channel MOSFETs (PMOS) devices implementing a full-bridge rectifier coupled with a switch control circuit based on a PMOS device driven by a comparator. With a load of 45 kΩ, the output rectifier voltage and the input piezoelectric transducer voltage are 694 mV and 703 mV, respectably, while the VOUT versus VIN conversion ratio is 98.7 % with a PCE of 52.2 %. The energy harvesting circuit has been designed using 130 nm standard CMOS process.

2.2 Advantages

[1] MEMS harvester with CMOS power management circuit are all integrated in only one chip. The system is completely self-supplied by the harvester vibration energy, and has no dependence on a previously charged energy reservoir.

[2] The excitation is a random signal with a big frequency range of 20–400 Hz. The sensitivity difference between the experimental data and simulation results is about 0.005 V/m s2 (11.1 % error) and resonant frequency difference of about 9.4 Hz (4.2 % error).

[3] High voltage conversion efficiency of the whole system. The off-chip components are reduced as much as possible so that this energy harvester can be easily integrated with other complex systems.

2.3 Disadvantages

[1] It can supply only 24.1uW and 63.9uW under 0.5g and 1.0g vibration levels, respectively without any power-management circuitry. Its efficiency is between 50 %-60 %.

[2] Using the diode for rectifying and the capacitor for energy storing makes the power consumed high so the efficiency reduces as the efficiency of the whole system is 1.23 %.

[3] High load resistance which means cannot support applications with low resistances. The output voltage is only 694 mV which is considered very small. Small power conversion efficiency.

3 System architecture

3.1 Piezoelectric transducer

Transducer is a device that converts a non-electrical physical quantity (temperature, sound or vibration) into electrical physical quantity such as converting vibration or light into electrical energy. At the scope of energy harvesting technology, we care about solar, piezoelectric, thermoelectric and RF transducers, each one of them convert non-electrical energy (heat, vibration, light..... etc) into electrical energy. Solar energy transducers provide higher energy density than any other type of transducers. Piezoelectricity is the property of certain materials to induce charges on surfaces when certain stress applied to the material or vibration, these charges generate voltage difference which used to power electronic circuits. The thesis presents a model of vibration energy harvester which designed with bimorph piezoelectric cantilever with end mass which converts the vibration energy applied to the structure into electrical energy. The model is used to find the resonance frequency of the energy harvester, output voltage, harvested power and optimal value of excitation frequency for maximum power transfer. Piezoelectric energy harvester with resonating harvester has the ability to resonate at low frequency and high stress generation. The model is designed and simulated with the finite analysis in COMSOL Multiphysics and the results of harvested power and output voltage are presented here. The vibration energy harvester model is consisting from cantilever deposited by two layers of piezoelectric material with an end mass at the end of the cantilever to lower the resonant frequency. The cantilever is steel substrate sandwiched by two layers of piezoelectric material of Lead Zirconate Titanate (PZT-5H). The top and bottom surfaces of the bimorph form the electrodes that will be wired for the load. Figure shows the schematic of the energy harvester model.

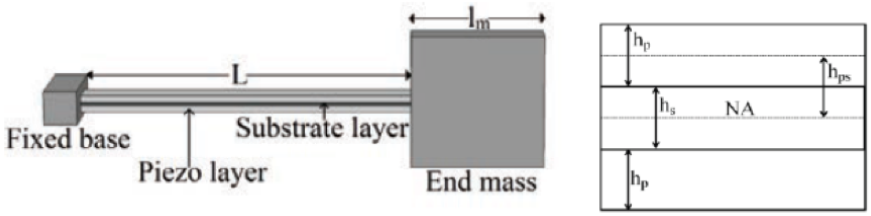


Figure 2: Schematic diagram of the piezoelectric trasnducer model and Cross sectional view.

Finite element analysis using COMSOL Multiphysics is used to model the energy harvester where the piezoelectric layers are connected to load resistance which equivalent to the input impedance of the second block of the system which is the AC/DC block and acceleration of 1g is applied at the end mass. The model is simulated to obtain the output Voltage and harvested power as a function of the excitation frequency. The material properties and Geometric properties of the model are given at table .

Parameter	Description	Value
L	Length of the Cantilever(mm)	25
b	Width of the Cantilever(mm)	8
h_p	Thickness of Piezoelectric layer(mm)	0.15
h_s	Thickness of the substrate layer(mm)	0.1
l_m	Length of end mass(mm)	2.5
l_w	Width of end mass(mm)	2.5
Y_p	Young's modulus of Piezoelectric material(GPa)	105
Y_s	Young's modulus of substrate material(GPa)	105
ρ_s	Mass density of substrate material and end mass(kg/m^3)	7500
ρ_p	Mass density of Piezoelectric material(kg/m^3)	9000
R_load	Load resistance(ohm)	11k

The harvested power of the vibration energy harvester is plotted as a function of the excitation frequency as shown at figure , the maximum power harvested is located at the resonance frequency which is about 149 Hz, as the frequency is deviated from the resonance frequency the harvested power is decreasing.

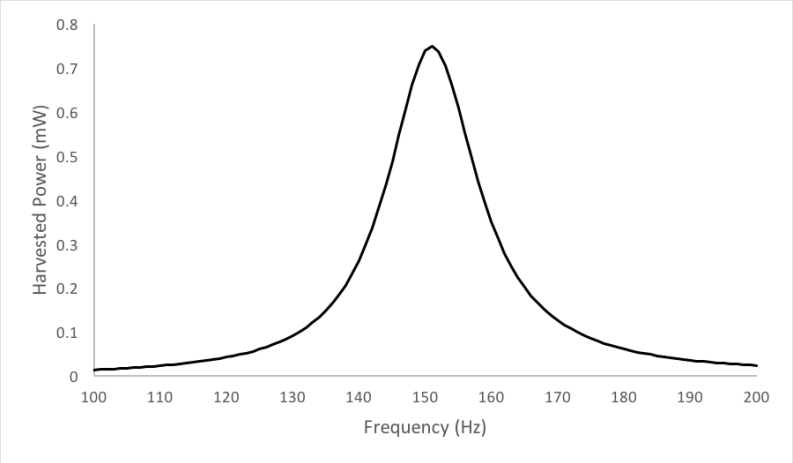


Figure 3: Plot the of harvested power of the transducer versus the excitation frequency.

The harvested power of a piezoelectric film under vibration is depend on the film's geometry, piezoelectric material properties, resonance frequency of the material and the output load, for maximum power density extracted, the material must be vibrated at its resonance frequency, it has been proved that power density decreases when the resonant frequency deviates from the vibration frequency.

Energy Harvesters Modeling:

In order to identify the interaction between the transducer and other system components and to be integrated, we model the vibration energy harvester with lumped elements. Transducer model is represented by discrete circuit elements and analyzed by standard electrical circuit methods such as KCL and KVL. Modeling of the lumped mechanical domain is represented as circuits elements for example, capacitor represent the potential energy at the system, resistor models the dissipation of power and Inductor represents the stored kinetic energy at the system, while the voltage source is

the effort done by the system. Figure shows the circuit model that describe the electromechanical coupling of the piezoelectric harvester at resonance:
$(V_m = \frac{ma}{r^2}, L_m = \frac{m}{r^2}, C_m = \frac{r^2}{k}, R_m = \frac{d}{r^2})$

Where (r) is the electromechanical coupling factor.
(m) is the effective mass of the structure.
(a) is the acceleration acting at the harvester end mass.
(d) is the damping coefficient.
(k) is the stiffness of the system.
(C_p) is the internal capacitance of the piezoelectric material.

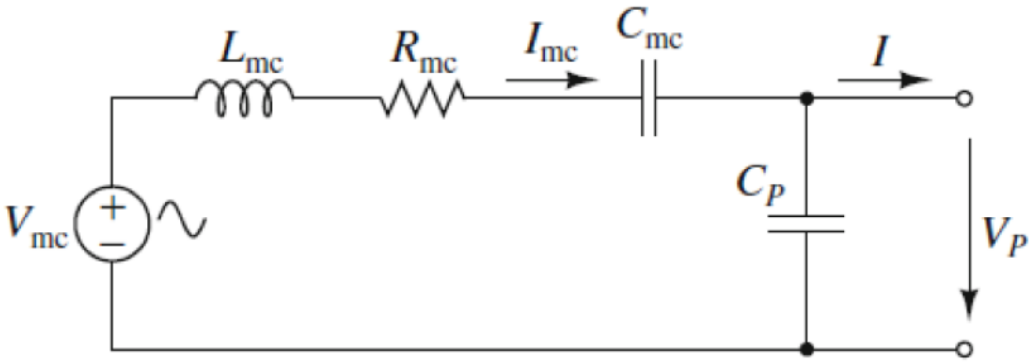


Figure 4: equivalent circuit of the piezoelectric transducer at resonance.

The model is simulated by Verilog A in order to validate the model and incorporate the transducer with the whole system. the results of output voltage from the transducer is compared with the results of COMSOL Multiphysics as shown at Figure which indicates perfect matching between the two models.

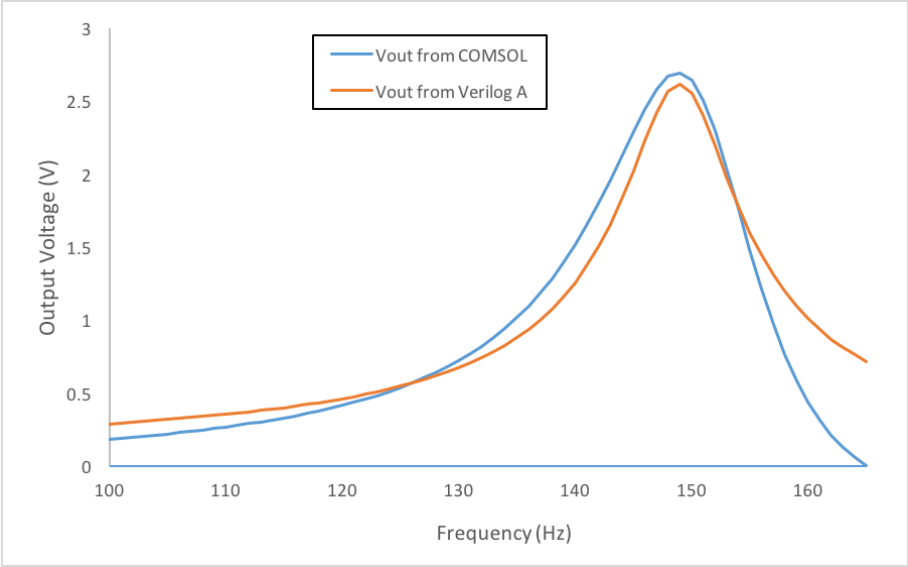


Figure 5: Plot of the output voltage of the transducer versus the excitation frequency for Comsol and Verilog A models.

3.2 AC-DC converter

AC-DC converter is the circuit responsible for changing the Alternative current into direct current. In case of Ac power transducers, the output power is generated in the form of alternating current with a certain frequency. On the other hand, the systems that need to be powered need direct current most of the time, that's why this block is very important in most of the electronic designs, specially energy harvesters.

The idea of Ac-Dc converter is that it controls the direction of the current to make sure that the polarity of the terminals connected to the load is not changing with the changing Ac input signal, this can be done by a single device as the diode which firstly converts –or neglects- the negative part of the input signal and secondly control the direction of the current through the circuit. As mentioned the Ac-Dc converter is changing the input Ac current to make it a Dc one, this can be done by more than one method starting with single diode half wave rectifier which losses around half of the power as it neglects the negative part of the Ac wave passing by the full wave rectifiers, here there are some implementations of Ac-Dc converters.

3.2.1 Bridge full wave rectifier

This design uses four diodes, two diodes at a time, in the first half cycles the current flows through two diodes (D1 and D2) while in the second half cycle the current flows through the two diodes (D3 and D4) , this design has some good points as it passes the current in the two half cycles so the power loss is minimized, on the other hand the voltage drop because of the two transistors is high also the design consists of four diodes not only one.

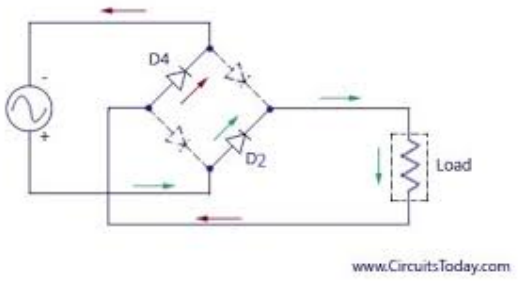


Figure 6: Bridge full-wave rectifier circuit.

3.2.2 Active diode

As illustrated before Ac-Dc converters can be implemented using passive diodes, but nowadays size matters and electronic designs has to be small in order to be integrated in ICs, and until now passive diodes need very large area (off-chip) and suffers from high switching power losses and significant voltage drop compared to the output voltage of the rectifier in low-amplitude vibrations, that's why a lot of designs for AC-DC converter designs that are based on transistors have been proposed.

To replace the passive diode an active diode was created, the active diode does the same as the passive diode by doing its two operations, converts the negative part of the input signal from negative to positive and controlling the direction of the current through the circuit, but as transistors are used they need to be powered, that's why they are called active diodes.

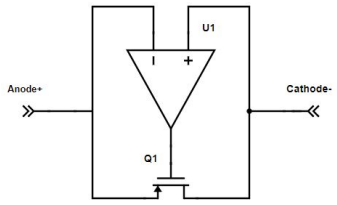


Figure 7: Active diode circuit implementation.

The simple active diode consists of a comparator and a MOS transistor , the comparator compares the voltage potential at the two terminals of the MOS transistor and depending on their values switched the transistor on or off, for instance in this design, the comparator compares the potential at the anode and the cathode , if the potential on the anode is higher than that n the cathode, the output of the comparator will be low which switches the pMOS ON and allows the current to pass from the anode to the cathode , on the other hand if the potential on the anode is lower than that on the cathode , the output will be high and the diode will be turned off.

3.2.3 Hybrid rectifier topology with self-starting up capability

The implemented design consists of two parts, the first is the passive rectifier used for the self-start up operation, it consists of two nMOS diode-connected transistors that kicks in once vibration starts providing AC-DC rectification, where initially the active rectifier is off, as Vs is zero and can't activate it. On the other hand, the active rectifier consists of two active diodes, each one has an nMOS transistor and a comparator. It operates when the harvester powers up Cs, these active diodes eventually eliminate the voltage drop ($\Delta V = V_s - V_{in} = V_{sd} \cong 300mV$) caused by nMOS diode-connected transistors bypassing them, hence increase the output power and voltage. the active diodes have the ability to be turned on and off completely without the use of reverse current control especially when used in vibration harvesting systems where the frequency of vibration is low. Therefore, it is not recommended to implement the reverse current control technique in our target micro-power systems that adds more complexity and power losses in the system.

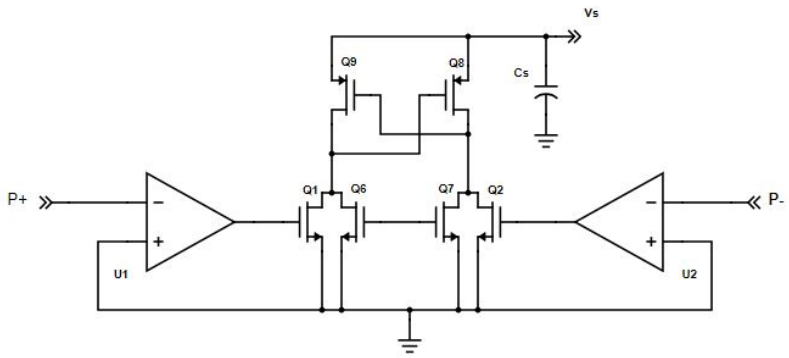


Figure 8: Hybrid rectifier topology with self-starting up capability.

Theory of operation

When $V_{in1} > V_{in2}$, MP1 will be ON as soon as V_{in1} exceeds V_{thp}, while V_{in2} is lower than ground making the output of comparator CMP2 "high", turning right active diode ON which directs current from the V_{in1} to the storage capacitor Cs through MP1. On the other hand, when $V_{in1} < V_{in2}$, MP2 will be ON as soon as V_{in2} exceeds V_{thp}, while V_{in1} is lower than ground making the output of comparator CMP1 "high", activating left active diode which directs current from the V_{in2} to the storage capacitor Cs through MP2.

The optimal output voltage of the transducer, concurrently the maximum harvested power are as follows :

$\Rightarrow P(t) = \frac{2I_pV_s}{\pi} - 4V_s^2 fC_p - I_{CMP}V_s$

$\Rightarrow V_{s,optimal} = \frac{I_p}{4\pi fC_p}$

Ultra-low power Comparator

The comparator implementation is ultra-low power implementation, consists of four parts : current source, current mirror, common-source amplifier and two inverters. The comparator is designed to work in sub-threshold region Current source is designed to drive small current from source in range of nanoamperes, while the use of two inverters was to enhance driving capabilities of the comparator to drive large gate capacitance nMOS switch.

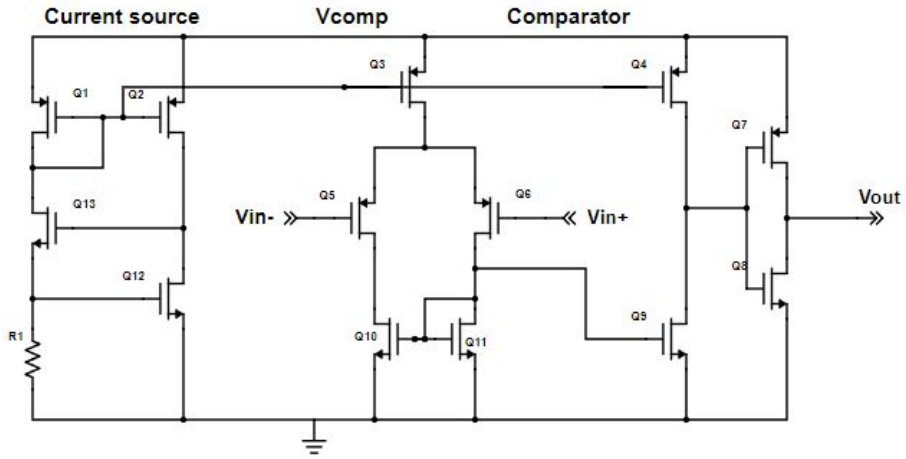


Figure 9: Voltage independent current source and comparator in sub-threshold operation.

3.3 MPPT

Maximum power point tracking which is knowing as MPPT is a technique or an algorithm which is mostly used in solar cells or systems to get the highest power from the cell despite any changes that may affects the cell like atmospheric conditions. MPPT technique plays on keeping the current and voltage on the optimized level to get the highest power from the cell. MPPT is not a technique that uses a mechanical system to get optimum power from cell but it's a fully electrical technique that depends on IV characteristics of the load.

The MPPT simplest idea relative to IV characteristics is to simply put a load resistance that gives the maximum power possible, as by changing the impedance seen by the cell the solar cell will be driven to the operating point where there is maximum power.

There are different algorithms for MPPT such as Artificial Neural Network Control, Fractional Short Circuit Current, Incremental conductance, Perturb and Observe, Fractional Open Circuit Voltage, three Point Weight Comparison, Closed Loop MPP and Fuzzy Control. Each one of those techniques (algorithms) has been proposed to overcome some obstacles (disadvantages regarding power loss and tracking efficiency), also the techniques vary in the complexity, speed and efficiency. Meanwhile in this Thesis report, the implemented MPPT block along with two other techniques will be discussed as they are used widely due to their efficiency and much easier implementation : Perturb and Observe (hill climbing method) and Fractional Open Circuit Voltage.

3.3.1 Perturb and Observe (P&O)

Perturb and observe is one of the simplest techniques as the controller changes the voltage a small change and measure how it affects the power, if then power increases it keep changing the voltage in the same direction until the power reaches the maximum value. There is a disadvantage as this technique does not reach the maximum power point, but it gets too close to the peak point and continue to perturb around it in both directions, also P&O technique does not take into consideration the changes in irradiation level and read it as change in maximum point so the final calculated maximum power point is wrong. The perturbation frequency should not be high, so the system can reach its steady state before the next one. The most efficient hill climbing algorithm is the Variable Step-size, a fully analog MPPT which consumes an average current between 900 nA and 1.3 μA has been realized in fig. [3], the perturbation step is related to the measured amount of deviation from maximum power point.

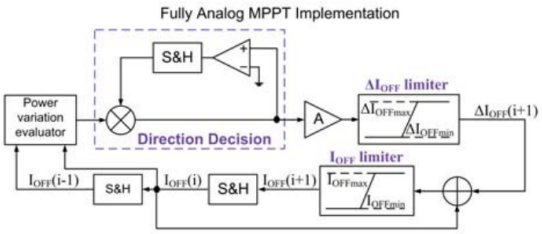


Figure 10: fully analog MPPT implementation depicted from Stanzione, S., Liempd, C. V., Schaijk, R. V., Naito, Y., Yazicioglu, R. F., & Hoof, C. V. (2013). A self-biased 5-to-60V input voltage and 25-to-1600 μW integrated DC-DC buck converter with fully analog MPPT algorithm. 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers. doi:10.1109/isscc.2013.6487643

3.3.2 Fractional Open Circuit Voltage

This method normally requires the converter to be disconnected for a certain duration to allow for the converter's input capacitors to be charged up to VOC. Solutions to this major problem, Fast Fractional MPPT With One-Cycle Detector (shown in fig. [5]) which has a faster MPP tracking time after sensing the than the hill-climbing P&O algorithm because they must change the duty cycle of the switching signal gradually.

Another solution, the indirect open circuit voltage method, using the P&O mode for fine-tuning to the MPP, and the transient mode for direct relocation of the operating point to the new MPP whenever there is a sudden change in the temperature gradient across the structure.

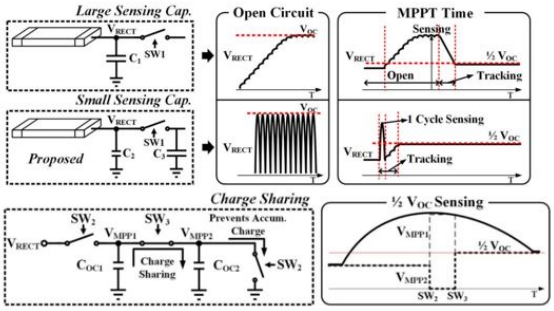


Figure 11: fully Fast Fractional MPPT With One-Cycle Detector, Graph from Shim, M., Kim, J., Jeong, J., Park, S., & Kim, C. (2015). Self-Powered 30 μW to 10 mW Piezoelectric Energy Harvesting System With 9.09 ms/V Maximum Power Point Tracking Time. IEEE Journal of Solid

3.3.3 Implemented MPPT

We are working on a vibration tracking unit for piezoelectric transducers that implements the fractional open circuit MPPT method that has low power overhead in the order of microwatts efficient for micropower applications.

Time-multiplexing mechanism is implemented, adaptively senses the vibration status and directly generates an optimal output reference voltage V_{REF} for the AC-DC rectifier for maximum power harvesting, along with a control block in which a pulse generator is used to generate the tracking pulse to control the time-multiplexing operation, also a control unit that compares the output voltage of the energy harvester with the MPP reference voltage V_{REF} to produce the control signal. Using the mathematical model of the transducer :

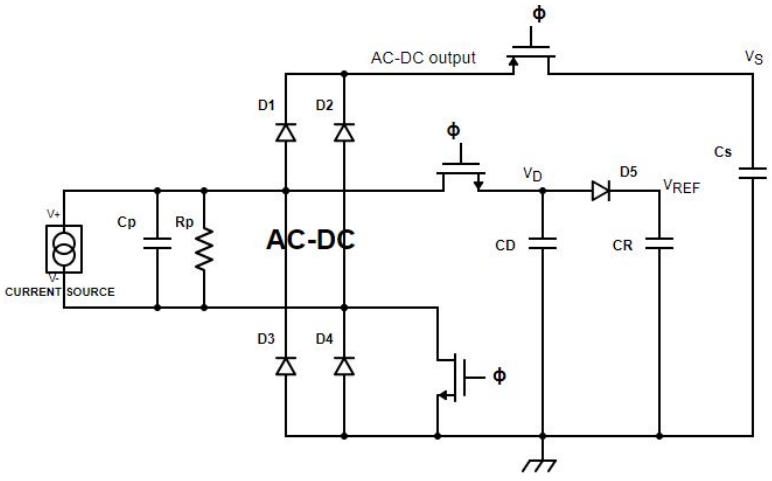


Figure 12: Implemented design of the energy harvester and the tracking unit along with the transducer model (ϕ is the tracking signal).

$$\Rightarrow \frac{dV_D(t)}{dt} + \frac{V_D(t)}{R_p} = I_P * \sin(2\pi f t)$$

$$\Rightarrow V_D(t) = \frac{I_P}{2\pi f C} * \sin(2\pi f t - \frac{\pi}{2}) + \frac{I_p}{2\pi f C} * \exp(\frac{-t}{R_p C}) + V_D(0) * \exp(\frac{-t}{R_p C})$$

Since R_p is very large, $\exp(\frac{-t}{R_p C}) \Rightarrow 1$ and $V_D(0) = 0$.
We conclude that the peak value of V_D occurs at $t = T/2$ which can be approximated to :

$$\Rightarrow V_{D,,peak} = V_D(t = T/2) = \frac{I_P}{\pi f C} = V_{REF} = 0.25 * V_{s,optimal}$$

Where

- $C = C_D + C_p$
- f is the environmental vibration frequency and T is the environmental vibration period.
- I_p is the amplitude of current from the transducer.

If C_D is designed carefully to have $V_{REF} = V_{D,,peak}$, which was found experimentally that C_D should be at least 15 times C_p.
The time needed for the piezo-electric transducer to reverse the current direction is atmost one vibrational cycle from the start of the tracking process and another half-cycle to reach positive peak value on C_D, a total of 1.5T at least is needed for the tracking process to function properly, leading to a tracking signal of pulse width at least 1.5T.

3.3.4 Refreshing Unit

A refreshing unit is used to periodically refresh the previously stored V_{REF} and provide a new refreshed value to the control unit, it is located between the tracking unit and the control unit. It solves the problem when C_R that holds V_{REF} gets a value lower than previous one, C_R can't be discharged because the active diode prevents the current flows from C_R to C_D leading to a wrong V_{REF} value been sent to the control unit.

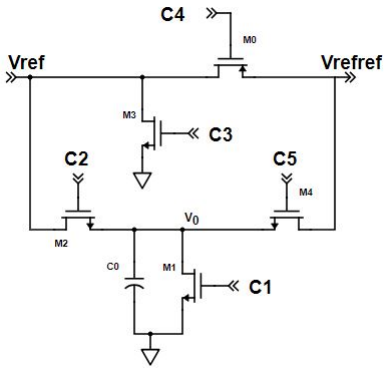


Figure 13: Refreshing unit circuit.

Working principle The refreshing unit consists of 4 nMoS devices, 1 pMOS and a small on-chip capacitor C_0. The operation starts when a new tracking pulse arrives, C_0 is discharged to ground through M_1, then M_2 is turned ON and starts charge sharing between C_0 and C_R, since C_0 is

much smaller than C_R , the voltage on it is close to V_{REF} in a small period of time, then M_3 is turned ON to discharge C_R at the same time when the output of the refreshing unit is connected to C_0 through M_4 and C_R is cut off the output, then enough time left for C_R to be charged with new V_{REF} and kept by it after the tracking pulse goes off, where the output of the refreshing unit is hooked back to C_R through M_0 and disconnected from C_0 by turning off M_4.

3.3.5 Pulse generator

The pulse width of the tracking signal will directly affects the time of energy harvesting from the piezo-electric transducer, hence the duty cycle of the tracking signal should be kept as low as possible. On the other hand, the vibration frequency varies with the environment in real life application, which makes it difficult to design a pulse generator of different frequency values, so we use the the signal from the transducer to generate the tracking signal of pulse width 2 T to assure that the minimum requirement of 1.5 T is satisfied.

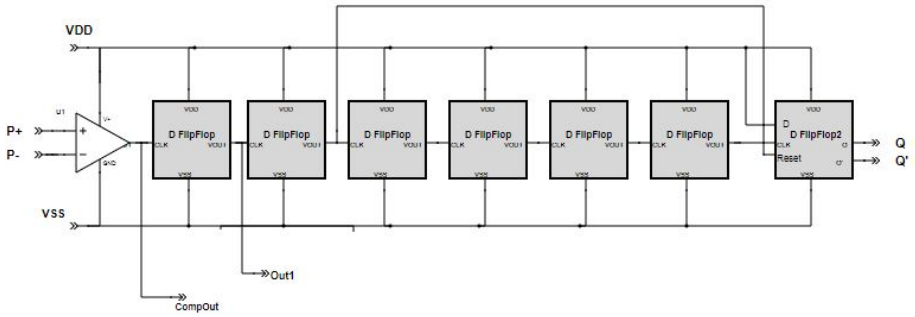


Figure 14: Block diagram of the tracking pulse generator.

Working principle The terminals of the transducer are fed into a comparator that generates pulses that have the same frequency of the ambient vibration. A digital counter and a D-flipflop with asynchronous reset were used to produce a tracking pulse with a fixed duty cycle of 1/64, i.e., around 1.56%.

A 6-bits digital counter is used to divide the frequency of the vibration over 64, the counter consists of a series of 6 D-flipflops, in each one $\bar{Q}$ is connected to to D input and the input signal is connected to clock terminal (Clk), where the output signal will be have half the frequency of the input signal. We used a D-flipflop with asynchronous reset signal that has a period of 4T and pulse width of 2T to generate the tracking signal.

We also used the pulse generator's tracking signal to produce the associated control signals for the Refreshing unit, as shown below, notice that C_4 and C_5 are the same.

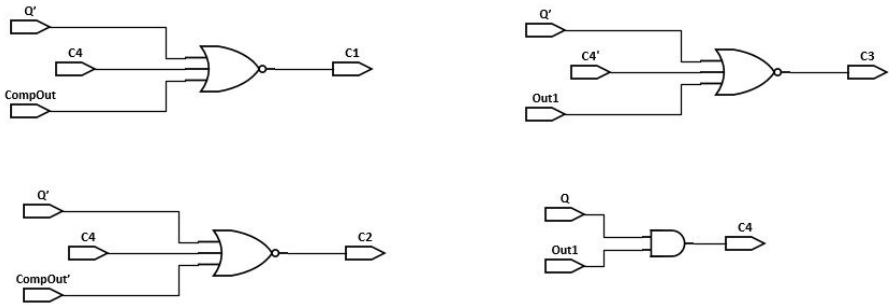


Figure 15: Block diagram of the refreshing unit control signals.

3.3.6 Control unit

The control unit is a voltage band-band controller that keeps the output voltage of the energy harvester to approximately 4 times of V_{REF}. It consists of a Schmitt trigger and a resistor divider which is used to produce V_1 and V_2 to the control unit. The values of the resistors are chosen to make $V_1 = 0.25V_s + \delta v_1$ and $V_2 = 0.25V_s - \delta v_2$, respectively, where δv_1 and δv_2 are two small voltage values which are not critical for the control unit, the values for R_1, R_2 and R_3 are 45kΩ, 370Ω and 15kΩ respectively .

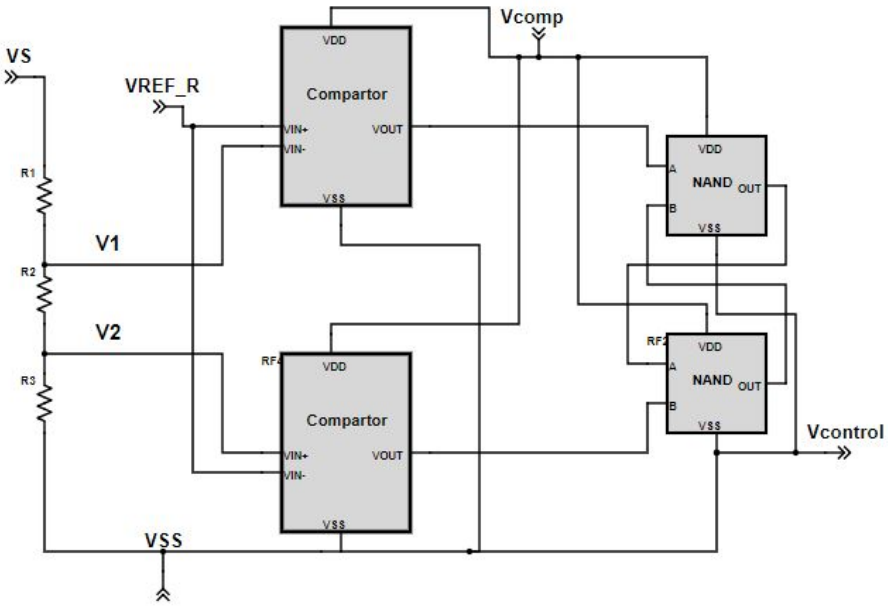


Figure 16: Block diagram of the control unit.

When V_s is charged up to $4V_1$ which is equal to $V_s + 4\delta v_1$, $V_{Control}$ becomes low and turns on the operation state and wakes up the system sleep mode. Power is then transferred to the load. When V_s is lower than $4V_2$ which is equal to $V_s + 4\delta v_2$, $V_{Control}$ becomes high and turns off the system,where the power transfer to the load is stopped. Later, when the harvested power is able

to charge up V_s to $V_s + 4\delta v_1$, the operation cycle discussed above repeats itself again.
The speed of the control unit isn't crucial for proper functioning, which has been proven experimentally, and since the most important design factor is low power consumption, the control unit has been designed to work in sub-threshold region.

3.4 Capacitor divider

To power up the the circuits that operates in sub-threshold region , for instance the comparators, the control unit and pulse generator circuits, we should provide a supply voltage for them of about 1V to reduce the current driven from the source. V_s carry high voltage of about 2.5V (optimal value), so we need to divide this voltage and the first solution is to use resistor divider, but a huge drawback is the power dissipation in resistors that jeopardize the power conversion efficiency, the most important feature in the energy harvester, so another solution is to use a capacitor divider circuit as shown below, the values of C_1 and C_1 are 2μF and 3μF respectively.

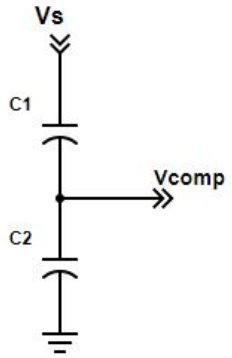


Figure 17: Capacitor divider circuit.

3.5 DC - DC converter

The DC-DC converter is considered as one of the most important electronic circuits that existed in every electronic device such as: cellular phones and laptop computers. Its main function is to convert a DC source from its level of voltage to another level. The designer can decide which to increase this level or decrease it. Most of the devices need a specific level of voltage as too much power may destroy them or too little power may make them can't run. The converter can be seen in different forms. As in Figure. 18, the DC-DC can be in the form of a small electronic circuit that can be implemented on a chip. Also, it can contain discrete components so it will be in the form of a PCP (printed circuit board). If you want an entire device of the converter, it is also available in the market. [4]

Types of DC-DC converter

Figure 18: Forms of DC-DC converter

There are many types of DC-DC converter. This report focus only on three types. These types are [5]:

- Buck Converters (Step down): are used to convert the high input voltage to low output voltage.
- Boost Converters (Step up): are used to convert the low input voltage to high output voltage.
- Charge pump: is used to convert the low input voltage to high output voltage using transistors and capacitors only.

3.5.1 Buck converter

The beginning of thinking to design a buck converter was using voltage divider as in Figure. 19. The problem was the efficiency of the device as it was very small. Another more important problem arose that if the resistance of the next stage is comparable to the load resistance it will cause the voltage to divide again and may be the load that we are interested about doesn't get enough voltage to run. To fix these problems, a large capacitor was added in parallel with the load resistance as in Figure. 20. This capacitor can also control ripple. But if for example a 39 voltage source has been put the capacitor will charge to 13 volt, then when the switch closes, the source current spikes to a huge value and burns out the switch. [6] The next solution was adding an inductor as in Figure. 21 to prevent the huge current spike. But now, if the L has current when the switch attempts to open, the resulting Ldi/dt (voltage) burns out the switch. So, a diode must be added as in Figure. 22 then the switch can open and the inductor current can continue to flow. With high-frequency switching, the load voltage ripple can be reduced to a small value. [6]

It is better to use mosfets instead of diodes whenever it is possible. So the final design of the DC-DC buck converter will be as in Figure. 23.

It has two stages the ON and OFF stages. In the ON stage Q1 is on so the current will begin to increase, and the inductor will produce an opposing voltage across its terminals in response to the changing current. This voltage drop is opposite to the voltage of the source and therefore reduces the net voltage across the load: $V_L = V_{in} - V_{out}$

$V_L = L * \frac{di_L(t)}{dt}$ $\frac{di_L(t)}{dt} = \frac{V_{in} - V_{out}}{L}$

Over time, both the rate of change of current and the voltage across the inductor decrease so the

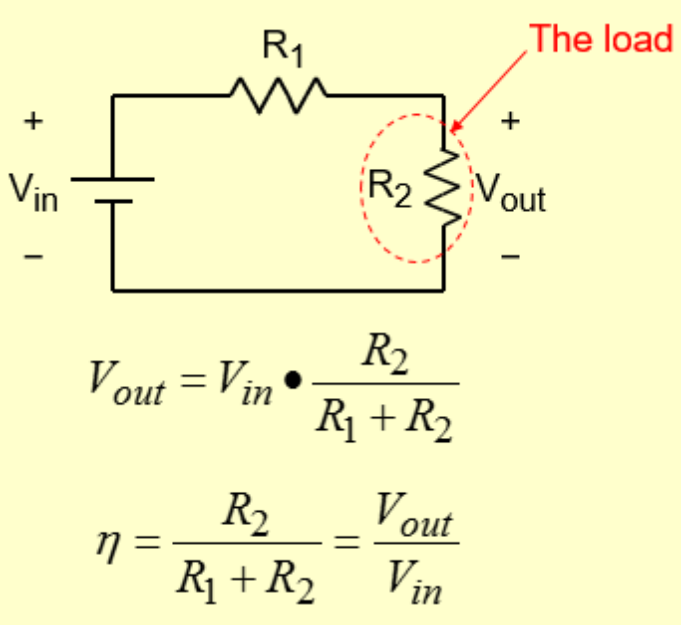


Figure 19: Circuit for voltage divider from EE462L, Spring 2014, DC−DC Buck Converter, Lecture6.ppt.

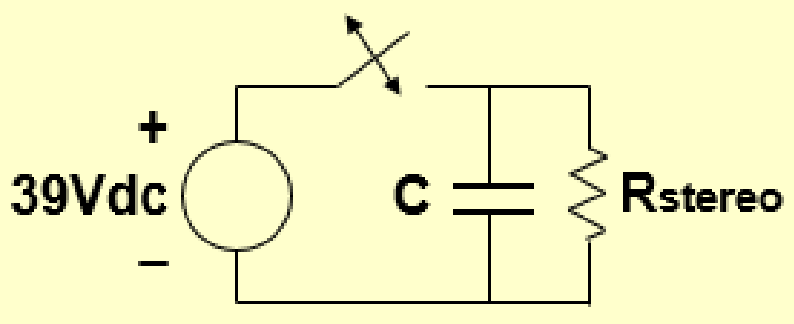


Figure 20: Circuit with large capacitor for storage from EE462L, Spring 2014, DC−DC Buck Converter, Lecture6.ppt.

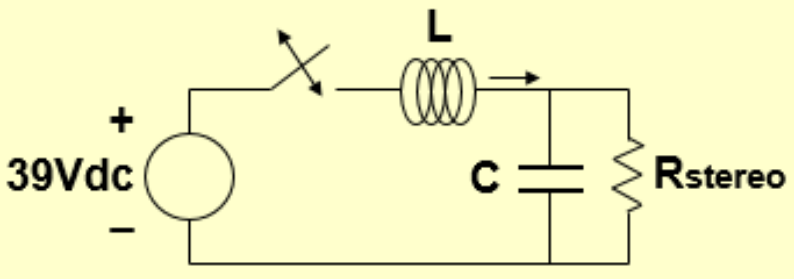


Figure 21: Circuit after including an inductor from EE462L, Spring 2014, DC−DC Buck Converter, Lecture6.ppt.

voltage at the load increase. The inductor will charge up and its voltage equals to the difference between the output and the input. The voltage across the inductor can be represented as in Figure. 24.

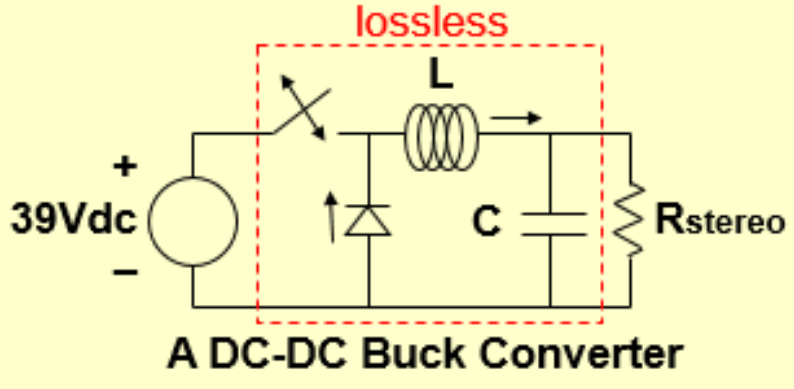


Figure 22: Buck converter from EE462L, Spring 2014, DC−DC Buck Converter, Lecture6.ppt.

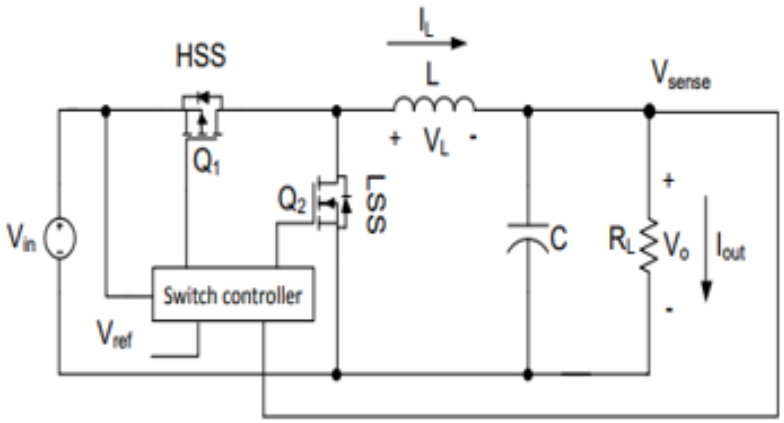


Figure 23: Buck converter using mosfets

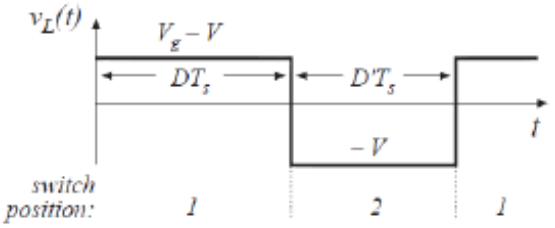


Figure 24: The voltage across the inductor from ELC 612 POWER MANAGEMENT, Lecture 2: DC-DC Converters.ppt, Dr. Faisal Elseddeek, Cairo University.

The ON stage will happen in 0 < t < DT, as T is the period of V_{ref} and D is the duty cycle. So, we can approximate the current of the inductor in the ON stage to: $i_L(ON) = \frac{V_g - V}{L} * DT$

In the OFF stage Q1 is off so the voltage source will be removed from the circuit and the current will decrease. The decreasing current will produce a voltage drop across the inductor so it will become a current Source: $V_L = -V_{out}$

$V_L = L * \frac{di_L(t)}{dt}$ $\frac{di_L(t)}{dt} = \frac{-V_{out}}{L}$

The stored energy in the inductor supports the current that will flow through the load. During

the OFF stage the inductor is discharging its stored energy.

The OFF stage will happen in DT < t < T. So, we can approximate the current of the inductor in the OFF stage to: $i_L(OFF) = \frac{-V}{L} * (1 - D)T$

To obtain the output depending on the input and the duty cycle, the sum of the ON and OFF current must equal to 0: $i_L(ON) + i_L(OFF) = 0$

$\frac{V_g - V}{L} * DT + \frac{-V}{L} * (1 - D)T = 0$

So the value of D will be: $D = \frac{V_{out}}{V_{in}}$

Now, it is easy to design a DC-DC buck converter. [7], [8]

3.5.2 Boost converter

The design of the DC-DC boost converter will be as in Figure. 25.

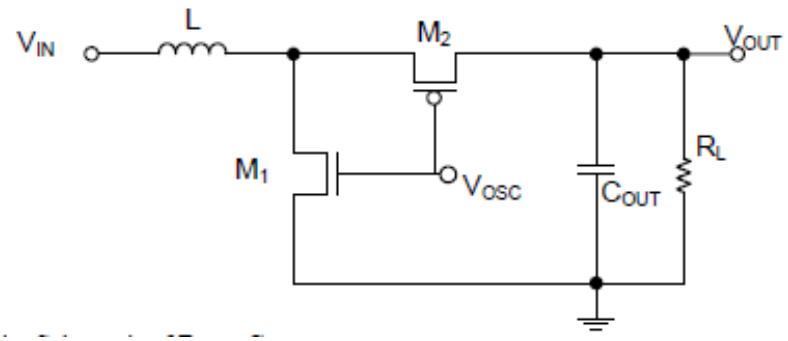


Figure 25: Boost converter

It has two stages the ON and OFF stages. In the ON stage M1 is on so a short circuit will be places passing L to the negative input supply terminal. So, a current flows between the positive and negative supply terminals through L which stores energy. No current flows in the rest of the circuit because M2 is off: $V_L = V_{in}$

$i_c = \frac{-V_{out}}{R_L}$ $\frac{di_L(t)}{dt} = \frac{V_{in}}{L}$

The ON stage will happen in 0 < t < DT, as T is the period of V_{OSC} and D is the duty cycle. So, we can approximate the current of the inductor in the ON stage to: $i_L(t) = \frac{V_{in}}{L} * DT$

In the OFF stage M1 is off and M2 is on so a drop in current causes a drop in the voltage across L. This results in a voltage across the load resistance: $V_L = V_{in} - V_{out}$

$i_c = \frac{i_L - V_{out}}{R_L}$ $\frac{di_L(t)}{dt} = \frac{V_{in} - V_{out}}{L}$

The OFF stage will happen in DT < t < T. So, we can approximate the current of the inductor in the OFF stage to: $i_L(t) = \frac{V_{in} - V_{out}}{L} * (1 - D)T$

The voltage across the inductor can be represented as in Figure. 26.

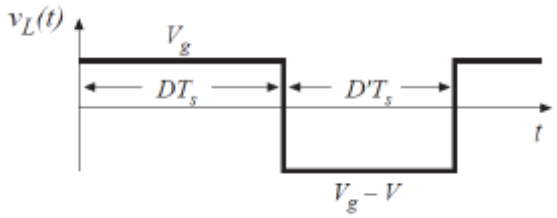


Figure 26: The voltage across the inductor from ELC 612 POWER MANAGEMENT, Lecture 2: DC-DC Converters.ppt, Dr. Faisal Elseddeek, Cairo University.

To obtain the output depending on the input and the duty cycle, the sum of the ON and OFF current must equal to 0: $i_L(ON) + i_L(OFF) = 0$

$\frac{V_{in}}{L} * DT + \frac{V_{in} - V_{out}}{L} * (1 - D)T = 0$

So the value of D will be: $D = \frac{V_{out} - V_{in}}{V_{out}}$

Now, it is easy to design a DC-DC boost converter. [8], [9]

3.5.3 Charge pump

Another design to step up the voltage is using a charge pump. One of most commonly used ones is Dickson charge pump in which diode-connected NMOS is used as charge transfer device as in Figure. 27.

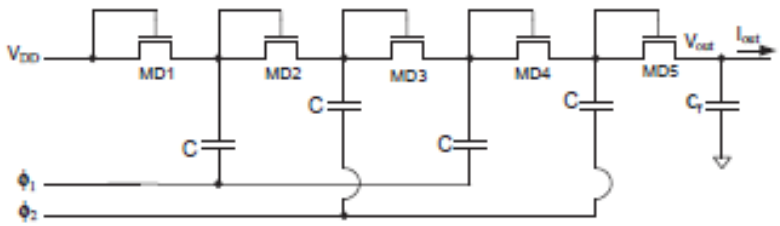


Figure 27: Dickson charge pump from S. Abdelaziz, A. Emira, AG. Radwan, AN. Mohieldin, and AM. Soliman. A low start up voltage charge pump for thermoelectric energy scavenging. In Industrial Electronics (ISIE), 2011 IEEE International Symposium on, pages 71–75. IEEE, 2011.

The voltage gain of each stage in Dickson charge pump is defined as the difference between the output and input voltages of this stage. The minimum VDD is set by the condition: VDD $>$ V_{tn} to obtain a positive voltage step in each stage. So, Dickson charge pump is not suitable for low-voltage applications. Modifications have been added to the Dickson charge pump to enable it to operate at low input voltage levels. By using charge transfer switch (CTS) in parallel with the diode connected device the voltage drop is eliminated. Static CTS technique that shown in Figure. 28 uses the next stage higher voltage as a static control for the CTS's.

Static CTS achieves higher gain than Dickson but it suffers from reverse charge sharing problem due to incompletely turning OFF of the mosfets and this will reduce the efficiency. So, dynamic

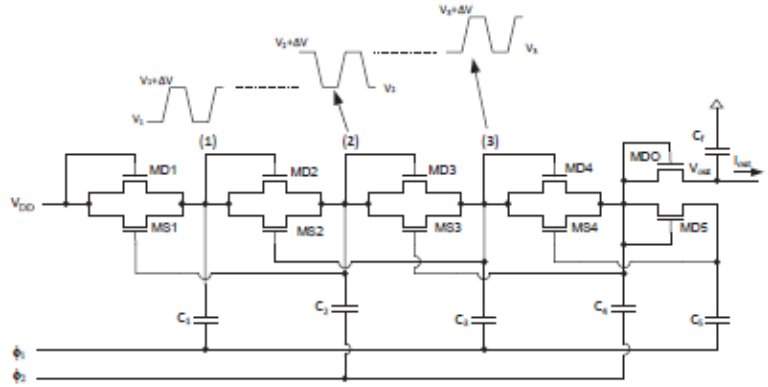


Figure 28: Static CTS charge pump from S. Abdelaziz, A. Emira, AG. Radwan, AN. Mohieldin, and AM. Soliman. A low start up voltage charge pump for thermoelectric energy scavenging. In Industrial Electronics (ISIE), 2011 IEEE International Symposium on, pages 71–75. IEEE, 2011.

control of the CTS's is required. Each CTS will be accompanied by an auxiliary circuit, which contains NMOS and PMOS transistors, so CTS can be off completely in the required period and can be on in the next stage as shown in Figure. 29.

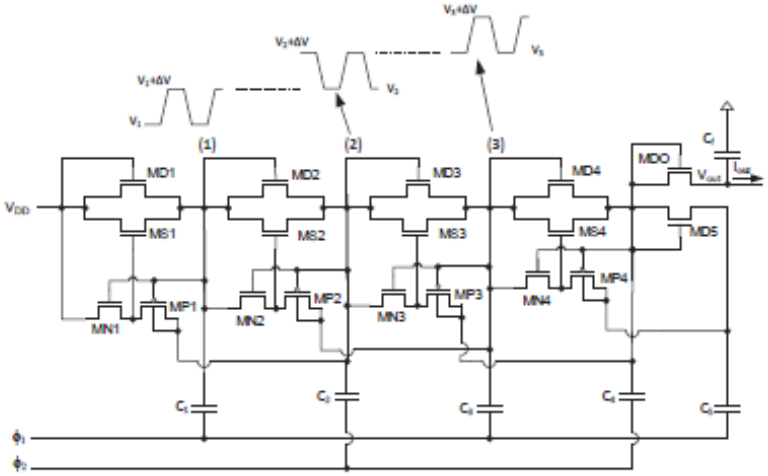


Figure 29: Dynamic CTS charge pump from S. Abdelaziz, A. Emira, AG. Radwan, AN. Mohieldin, and AM. Soliman. A low start up voltage charge pump for thermoelectric energy scavenging. In Industrial Electronics (ISIE), 2011 IEEE International Symposium on, pages 71–75. IEEE, 2011.

But the main problem is that CTS is difficult to turn on in low voltage environment. So, a new charge pump called Pelliconi is proposed as shown in Figure. 30.

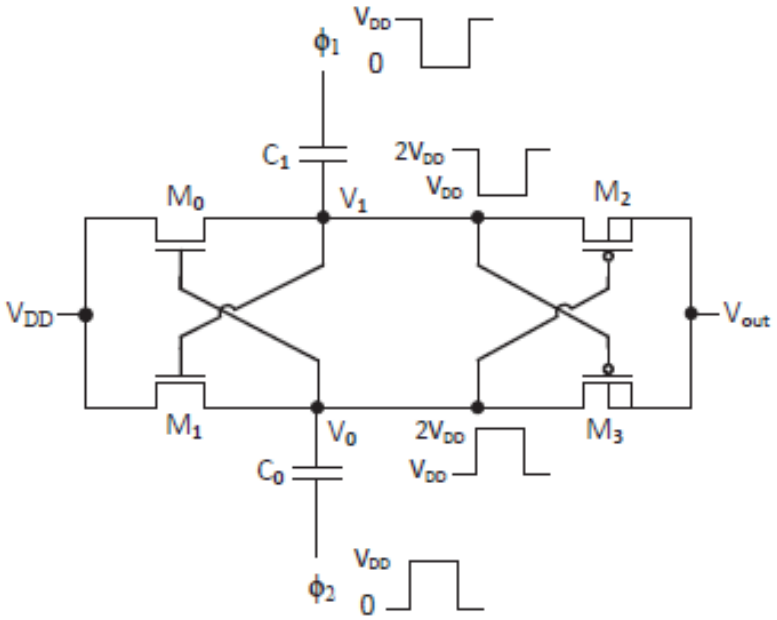


Figure 30: Pelliconi charge pump from S. Abdelaziz, A. Emira, AG. Radwan, AN. Mohieldin, and AM. Soliman. A low start up voltage charge pump for thermoelectric energy scavenging. In Industrial Electronics (ISIE), 2011 IEEE International Symposium on, pages 71–75. IEEE, 2011.

It is clear that Pelliconi is more suitable for low voltage applications. But to use it at very low voltage levels a large number of stages must be cascaded to obtain the desired output voltage. [10]

4 Simulation Results

4.1 AC-DC converter

The final results of AC-DC converter after running PEX are displayed here, below are the waveform of the input and output voltage of the AC-DC converter. The comparator current consumption for wide range of supply voltage values doesn't exceed 10 nA, this very low static current helps minimize the power overhead of the comparators that comprises a large part of the whole system.

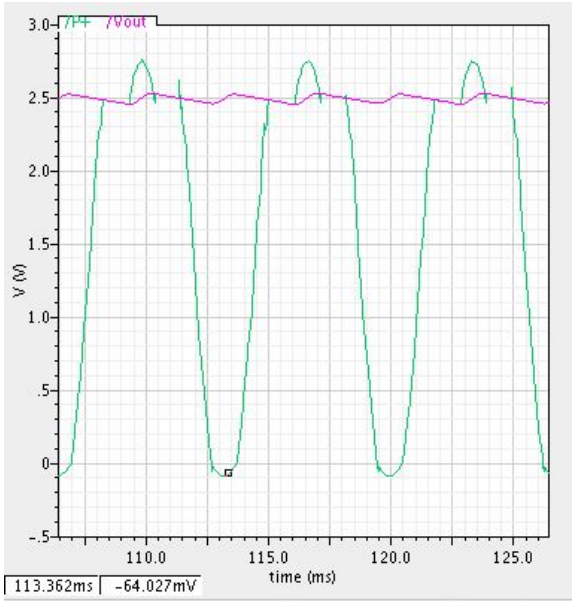


Figure 31: The input (P+) and output voltage of the AC-DC converter.

AC input response At different frequencies in the range of the of the bandwidth of the transducer, different values of input voltages are produced, the response of AC-DC to different values of input voltages is investigated as shown below.

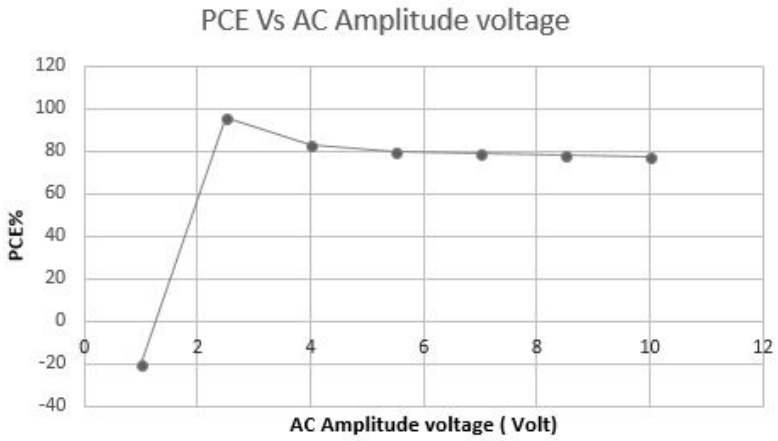


Figure 32: Power conversion efficiency Vs AC Amplitude voltage.

Frequency response The response of frequency variations is investigated, specially for leakage current which increases significantly with the increase of vibration frequency.

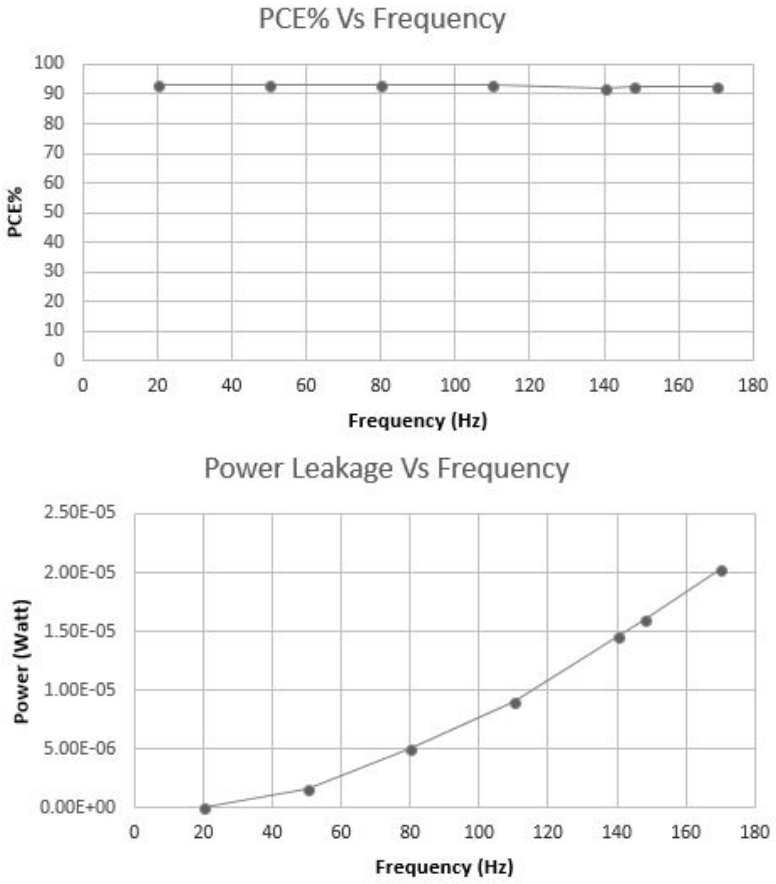


Figure 33: Power conversion efficiency Vs Frequency (up), Power leakage Vs Frequency (bottom)

Load variation response The change in the output resistance affects the power conversion efficiency significantly, as shown below, taking into consideration that the load resistance will represent the DC-DC converter block in the system.

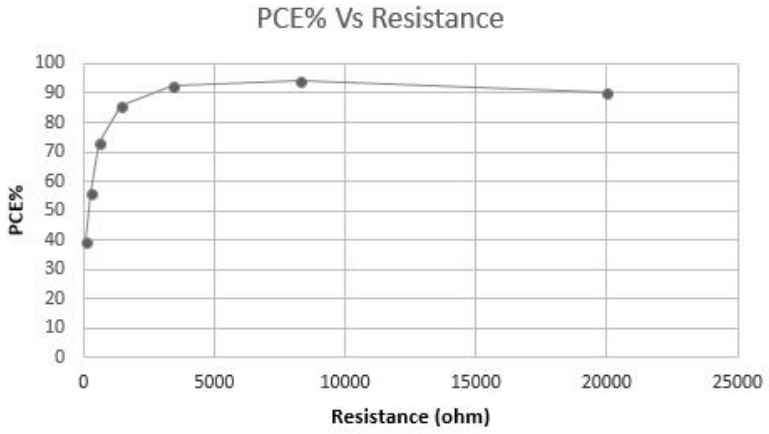


Figure 34: Power conversion efficiency Vs Output resistance.

4.2 MPPT

Tracking Pulse generator The MPPT unit was able to track the optimal voltage for maximum harvesting power, producing V_{REF} nearly equal to 0.25 V_s.

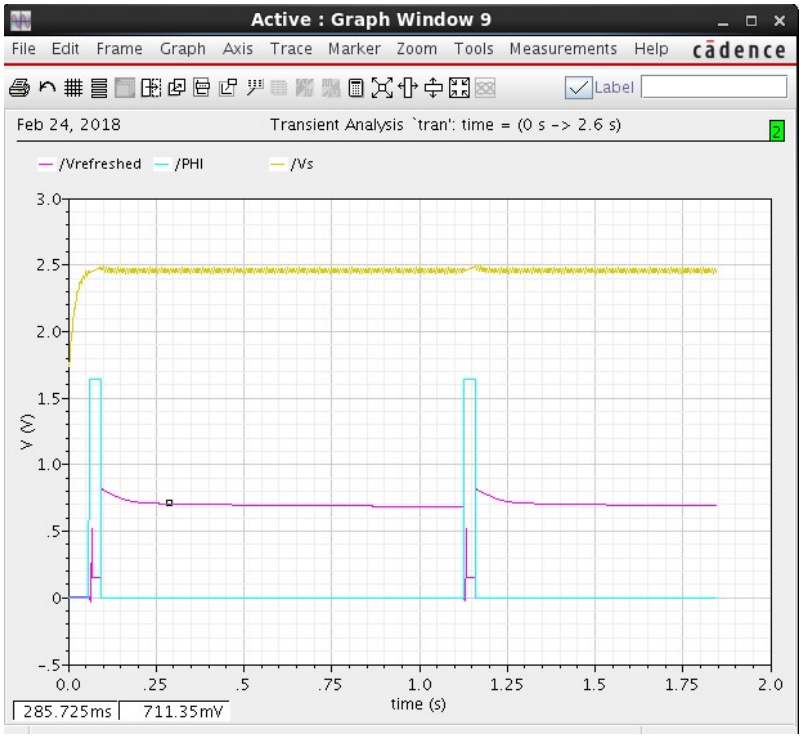


Figure 35: Simulated waveforms of vibration tracking unit, Vrefref ≈ 0.25 Vs.

Refreshing unit control The associated signals that controls the refreshing unit and updates the V_{REF} each tracking process cycle are shown below, as discussed before.

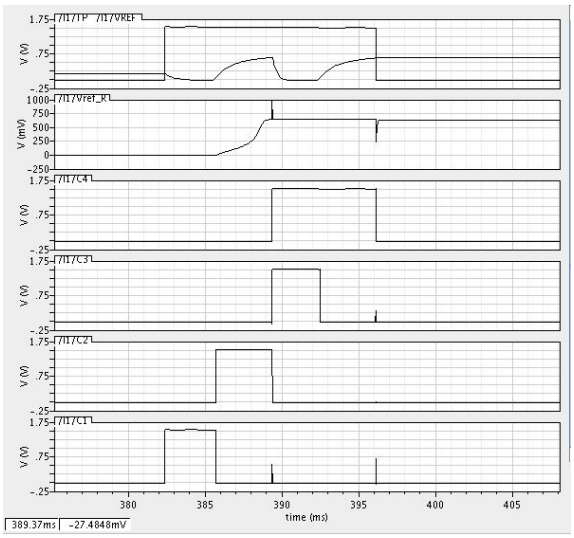


Figure 36: Associated control signals and the operation of the Refreshing unit.

4.3 DC-DC converter

For this system, the input voltage to the DC-DC converter is 2.5 volt and it is required to drive a load at 3.3 volt. So, this system needs a step-up converter. As a result, in this project we will focus on designing boost converter and charge pump.

4.3.1 Boost converter

First, to design the boost converter few constants must be defined:

$V_{in} = 2.5, \quad V_{out} = 3.3, \quad R_{out} = 5000$

So, $I_{out} = \frac{3.3}{5000} = 6.6 * 10^{-4} A = 0.66mA$

We will assume that the converter is not ideal (the real case). So, initially assuming efficiency = E = 60 % = 0.6

Duty cycle: $D = 1 - \frac{V_{in} * E}{V_{out}} = 1 - \frac{2.5 * 0.6}{3.3} = \frac{6}{11} = 0.5455 = 54.55\%$

$I_L = 0.2 * I_{out} * \frac{V_{out}}{V_{in}} = 0.2 * 6.6 * 10^{-4} * \frac{3.3}{2.5} = 1.7424 * 10^{-4} A$

Assuming the period of the square wave (clock) = $T_s = 100ns$, So the frequency will be: $f_s = \frac{1}{T_s} = \frac{1}{100 * 10^{-9}} = 10^7 Hz = 10MHz$

$L = \frac{V_{in} * (V_{out} - Vin)}{I_L * f_s * V_{out}} = \frac{2.5 * (3.3 - 2.5)}{1.7424 * 10^{-4} * 10^7 * 3.3} = 3.478 * 10^{-4} H = 347.83uH$

The desired output voltage ripple = R = 0.01 V

So, $C_{out} = \frac{I_{out} * D}{f_s * R} = \frac{6.6 * 10^{-4} * \frac{6}{11}}{10^7 * 0.01} = 3.6 * 10^{-9} F = 3.6nF$

So, using Cadence virtuoso the boost converter can be designed and simulated correctly as in Figure. 35 then get the efficiency of it. The values of the components can be summarized in table.

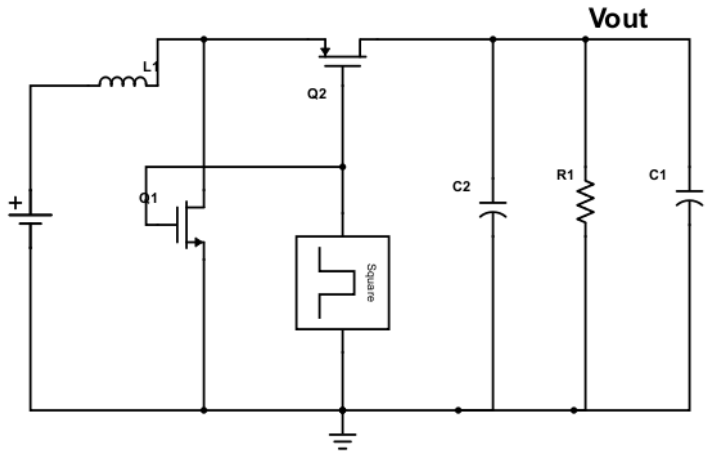


Figure 37: Boost converter simulated using Cadence virtuoso

1.

Component	Value
L1	347.83 uH
Q1	W = 100 um, L = 340 nm
Q2	W = 100 um, L = 300 nm
R1(out)	5 Kohm
C1(battery)	1.5 mF
C2	3.6 nF
Efficiency	4.99 %

Table 1: Values of the components of boost converter

After designing the boost converter, we realized that it is not applicable for this project. That's because it has very low efficiency which will be needed in this system. The values of the inductor and capacitor are also very large so they might be needed to be off chip which will cost more area. So, the ideal solution in this case was to switch to charge pumps.

4.3.2 Dickson charge pump

The main components in any charge pump are transistors and capacitance so it is very simple to implement. However, the disadvantage about it appears when a very small input voltage is needed to rise to a very large output voltage. In this case, a large number of stages are needed so the area and power consumed increase and the efficiency decreases. In this project the step up is only from 2.5 to 3.3. So, it is better to use charge pump. We began with designing the simplest charge pump which is Dickson charge pump as following:

Defining the constants: $V_{in} = 2.5V, \quad V_{out} = 3.3V, \quad R_{out} = 5Kohm, \quad C_{out} = 1.5mF$

$V_g = V_{in} - V_T = 2.5 - 1.1 = 1.4V$

$I_{out} = \frac{V_{out}}{R_{out}} = \frac{3.3}{5000} = 6.6 * 10^{-4}$

$V_{out} = (n+1) * V_g - \frac{n * I_{out}}{f * C}$

As n represents the number of stages and C represents the pump capacitors. So, to keep the area small four stages only and three pump capacitors will be used. We want to implement the capacitors on the chip so their value must not exceed 100 pF. To get the period of the square voltage source (clock), the frequency must be calculated first:

$f = \frac{n * I_{out}}{((n+1) * V_g - V_{out}) * C} = \frac{4 * 6.6 * 10^{-4}}{(5 * 1.4 - 3.3) * 100 * 10^{-12}} = 7.135 * 10^6 Hz = 7.135 MHz$

So the period used will be: $T = \frac{1}{f} = \frac{1}{7.135 * 10^6} = 1.40 * 10^{-7} s = 140.15 ns$

These values has been used in the design in Cadence virtuoso as Figure. 36 shows.

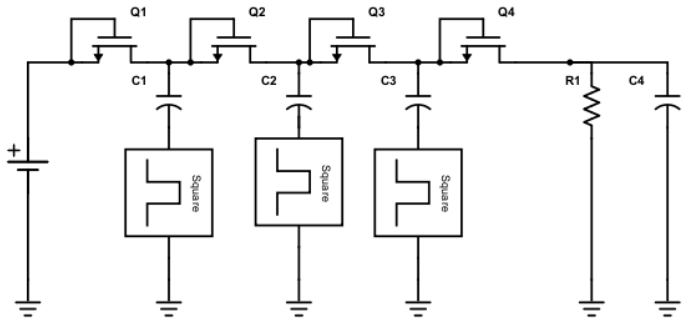


Figure 38: Dickson charge pump simulated using Cadence virtuoso

In the simulation, the value of the period is slightly different. The values of all the components can be summarized in table. 2.

Component	Value
Pump capacitors (C1, C2, C3)	100 pF
All mosfets	W= 100 um, L = 340 nm
n	4
R1(out)	5 Kohm
C4(battery)	1.5 mF
Efficiency	33.08 %

Table 2: Values of the components of Dickson charge pump

The number of stages are small and the area will be good, also the value of the capacitances are small enough to be implemented on the chip. But the main disadvantage in this design is the small efficiency. So, we must switch to another design.

4.3.3 Pelliconi charge pump

The efficiency was needed to be higher so we continue to try another design. One popular design is called Pelliconi. One stage only has been designed that contains four transistors with two capacitances that have smaller values than the capacitors in Dickson so the area is better. The Pelliconi circuit that was designed is shown in Figure 37.

The values of all the components can be summarized in table. 2.

The number of stages are small and the area will be good, also the value of the capacitances are small enough to be implemented on the chip. However, the efficiency can be raised more. So, we tried so many designs but only one gives us the best efficiency with small area.

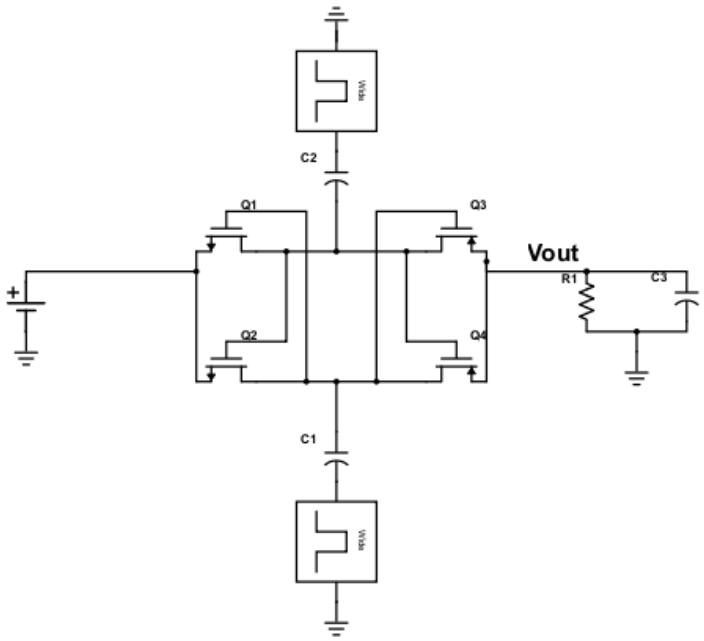


Figure 39: Pelliconi charge pump simulated using Cadence virtuoso

Component	Value
Pump capacitors (C1, C2)	25 pF
All n mosfets (Q1, Q2)	W= 100 um, L = 340 nm
All p mosfets (Q3, Q4)	W= 100 um, L = 300 nm
R1(out)	5 Kohm
C3(battery)	1.5 mF
Efficiency	67.211 %

Table 3: Values of the components of Pelliconi charge pump

4.3.4 Used charge pump

The design that has been used presented before in [11]. The design is shown in Figure 38.

To understand why it is better and give higher efficiency, the Pelliconi design must be investigated also. Assuming the design of simple Pelliconi charge pump and Ignore the existence of CLK C, CLK D, transistor Q4 and transistor Q7 in the figure. As CLK A goes from high to low and CLK B goes from low to high , we expect that transistor Q1(Q2) will be turned off and transistor Q3(Q6) will be turned on simultaneously. But actually the Q1(Q2) will not turned off completely when Q3(Q6) is turned on which provides a leakage path and the voltage holds at the capacitors C1 and C2 will be degraded.

The operation of this charge pump circuit is based on reducing the leakage current between the

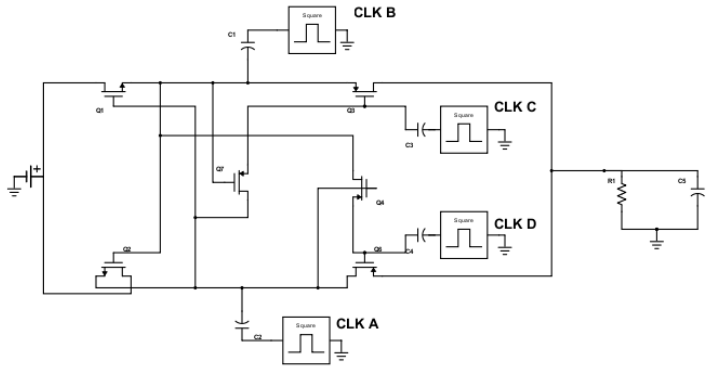


Figure 40: Used charge pump simulated using Cadence virtuoso

transistors during the clock transitions to increase the output voltage and pumping efficiency. The extra clocks (CLK C, CLK D) is to control the time intervals between the clock transitions.

The operation of the charge pump is as following: at the first time interval T1: CLK A, CLK B, CLK C, CLK D are high, low, high and high respectively. At this moment, Q3 is turned off and Q1 is turned on to charge the C1 with VDD as Q1 is turned on to transfer charges from the input to C1. At the same time the C2 is charged to 2 VDD and Q6 is turned on to transfer the voltage from C2 to the output. Q7 is turned on to transfer charges from C2 to C3. Simultaneously, Q2 and Q3 are turned off to cut off the leakage path between C2 and the input and the leakage path between the output and C1 respectively.

At the second and fourth Intervals T2, T4: CLK A, CLK B, CLK C, CLK D are low, low, high and high respectively. At this interval, transistors Q1 and Q3 are turned off as the gate source voltage difference is zero across them. At the same time Q4 and Q7 are turned on to charge the C3 and C4 to 2VDD which keep the PMOS devices (Q3 and Q6) off as the gate voltage across them is higher than their source voltage.

At the third interval T4: CLK A, CLK B, CLK C, CLK D are low, high, high and high respectively. At this moment, Q6 is turned off and Q2 is turned on to charge C2 to be VDD as Q2 is turned on to transfer charges from the input to the C2. At the same time C1 is charged to 2 VDD and Q3 is turned on to transfer the voltage from C1 to the output. Q4 is turned on to transfer charges from C1 to C4. Simultaneously, Q1 and Q6 are turned off to cut off the leakage path between C1 and the input and the leakage path between the output and C2 respectively.

The design has been simulated in cadence virtuoso using the values of the components showing in table. 4.

The design has better efficiency with smaller widths of the mosfets. So, this design achieves the two goals we care most high efficiency with small area.

The layout of the design has been made. After PEX, the result of the efficiency is 91.35 % which

Component	Value
C1, C2	25.08936 pF
C3, C4	25.5705 fF
Q1, Q2	W= 10 um, L = 340 nm
Q3, Q6	W= 10 um, L = 300 nm
Q4, Q7	W = 5 um, L = 300 nm
R1(out)	5 Kohm
C3(battery)	1.5 mF
Frequency of the square voltage	15.625 MHz
Efficiency	73.3 %

Table 4: Values of the components of used charge pump

means the efficiency has increased because of the parasitic capacitance that have been added to the design.

5 The whole system

After defining all the blocks in the architecture, it is now the time to bring them all together in one system.

5.1 Simulation

Each design is put into a block. The all blocks are connected with each other as in Figure 39.

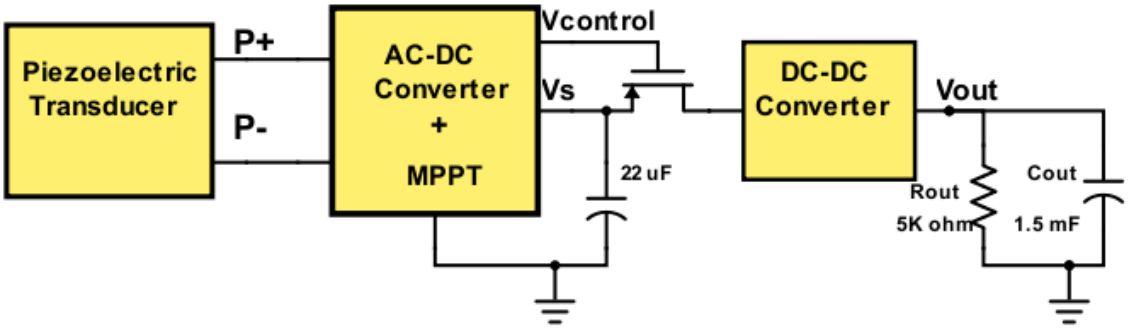


Figure 41: All the blocks connected together

The system capability to self-start when no power was available initially and sustain a stable operation was tested as shown below, demonstrating the ability of the implemented system to be used in battery-less applications.

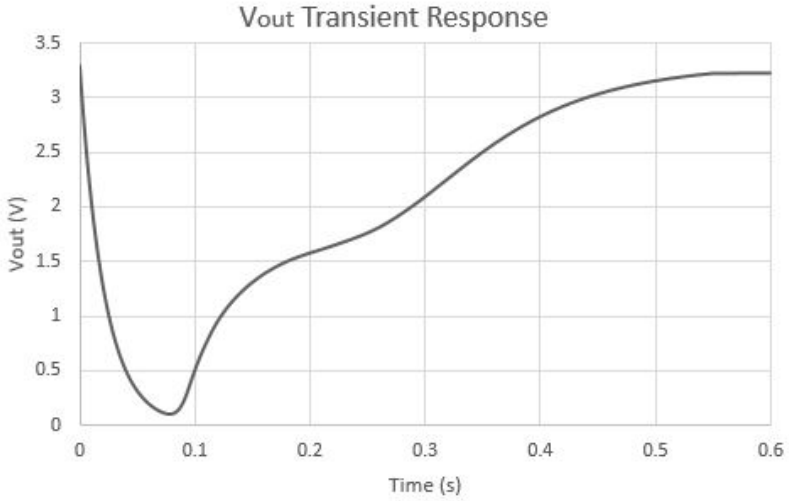


Figure 42: Self-start operation and V_{out} stable at 3.3V.

The first thinking was putting the schematic of the blocks together and simulate. But, the large difference in frequency between AC-DC converter and DC-DC converter made that very hard. The simulation of the two blocks need super-computer with large memory. So, the thinking was made one of the blocks using Verilog-A and the other stays schematic. As a result, the DC-DC converter has been made using Verilog-A and the entire system is simulated. The theoretical power conversion efficiency can be calculated by multiplying the efficiencies of each block: $PCE_{system} = PCE_{AC-DC+MPPT} * PCE_{DC-DC} = 0.88 * 0.73 = 0.6424 = 64.24\%$

Using the simulation we calculated PCE using the following equation:

$PCE_{system} = \frac{P_{res}+P_{cap}}{P_{in}+P_{cap}}$

As the capacitor represents the battery which is considered as an input when it charges the system and an output which it is being charged. The efficiency of the at the resonance frequency = 50 %, and the efficiency changes with the changing of the frequency of the transducer as in Figure 41.

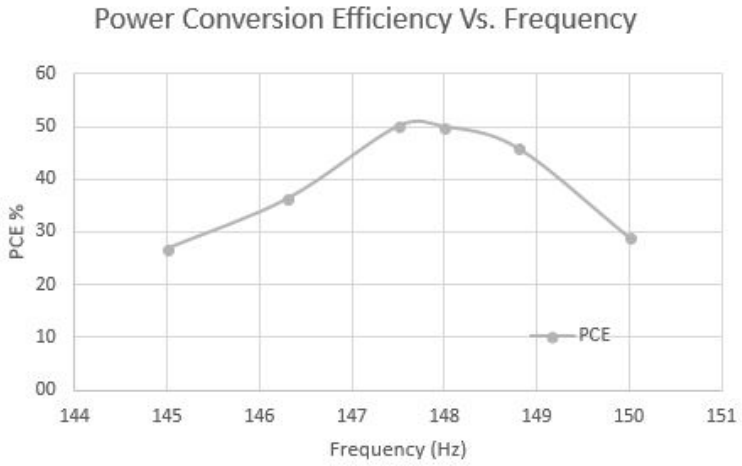


Figure 43: Power conversion efficiency Vs frequency of vibration to Whole system using a Verilog-A model for DC-DC converter.

5.2 Layout

Engineering is not all about Designing we also need to fabricate to use the design in real life, To fabricate a design we need to translate it to layout level. Layout Designed using cadence library UMC 130n. All block layout area and design are in the following figures.

Block	Hight	Width
AC-DC	102.505	103.295
control	46.234	35.895
MPPT	53.28	101.015
Pulse Generator	62.355	44.635
Refresh Circuit	4.9902	7.4754
System AC-DC	113.075	201.72
System DC-DC	254	293
The whole system	350.976	262.877

Table 5: Area of different blocks of the Layout

.

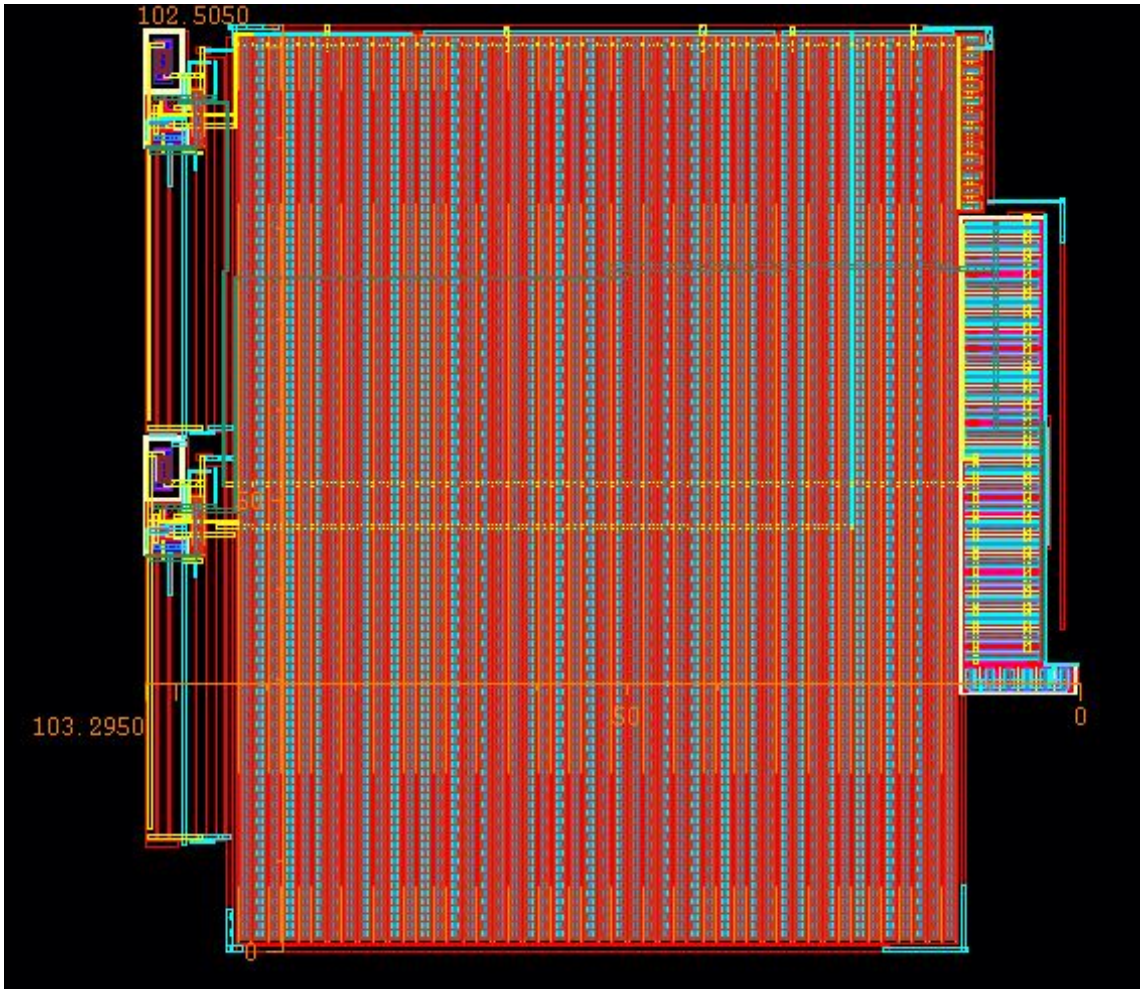


Figure 44: AC-DC Layout

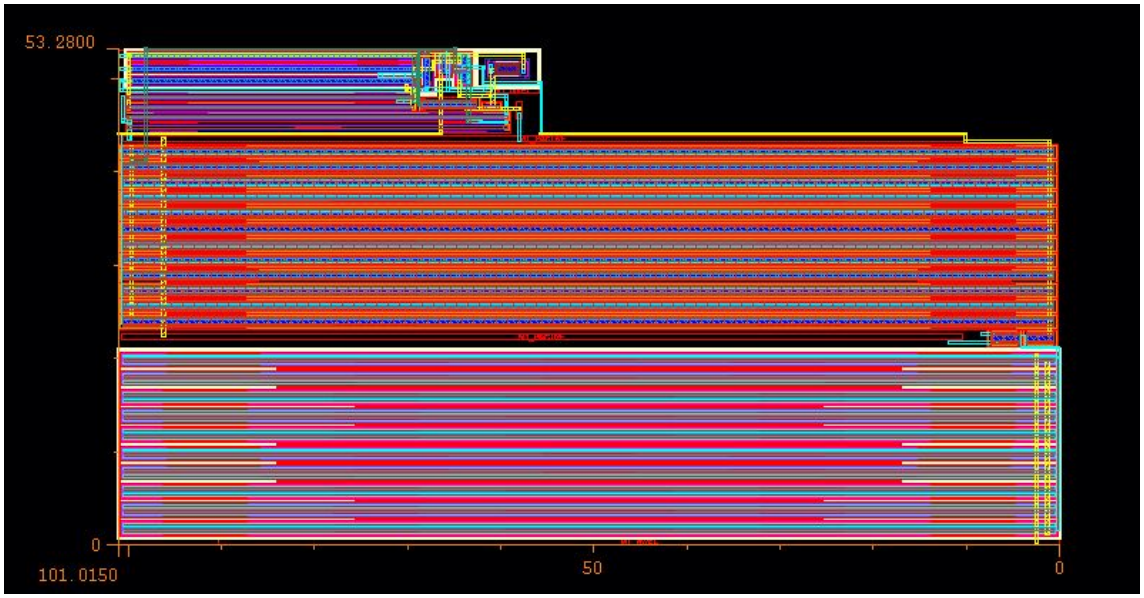


Figure 45: MPPT Layout

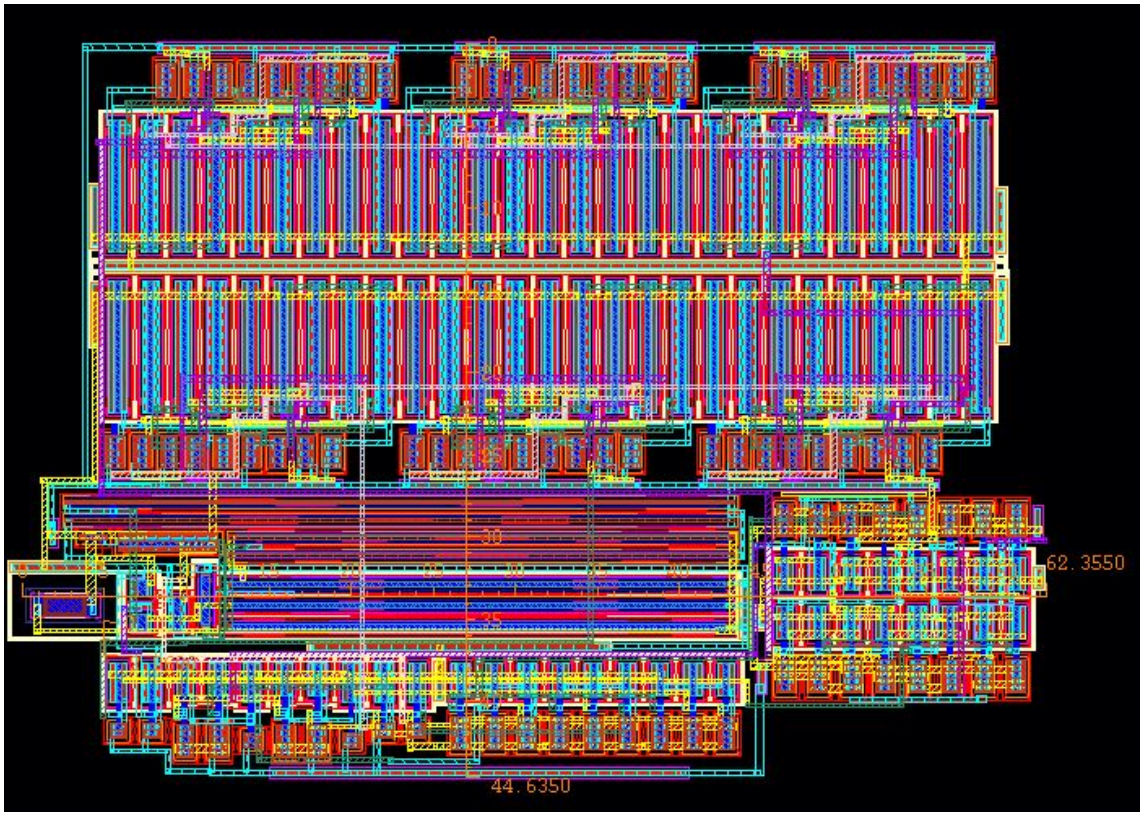


Figure 46: Pulse generator Layout

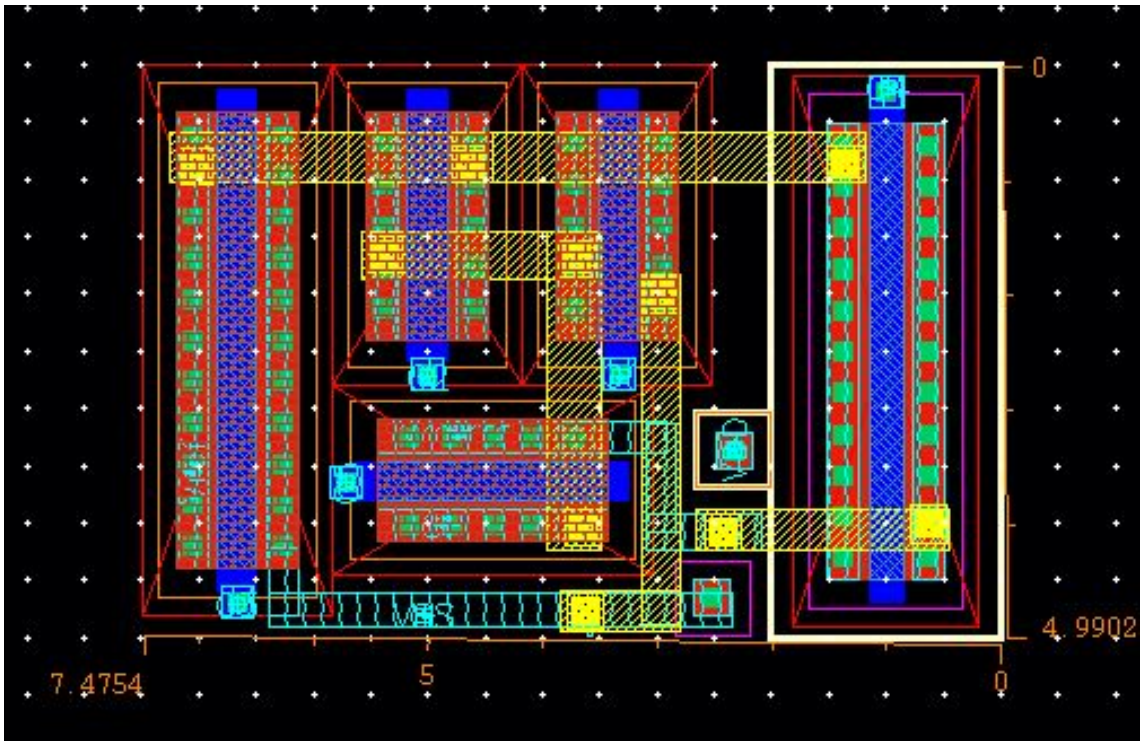


Figure 47: Refresh circuit Layout

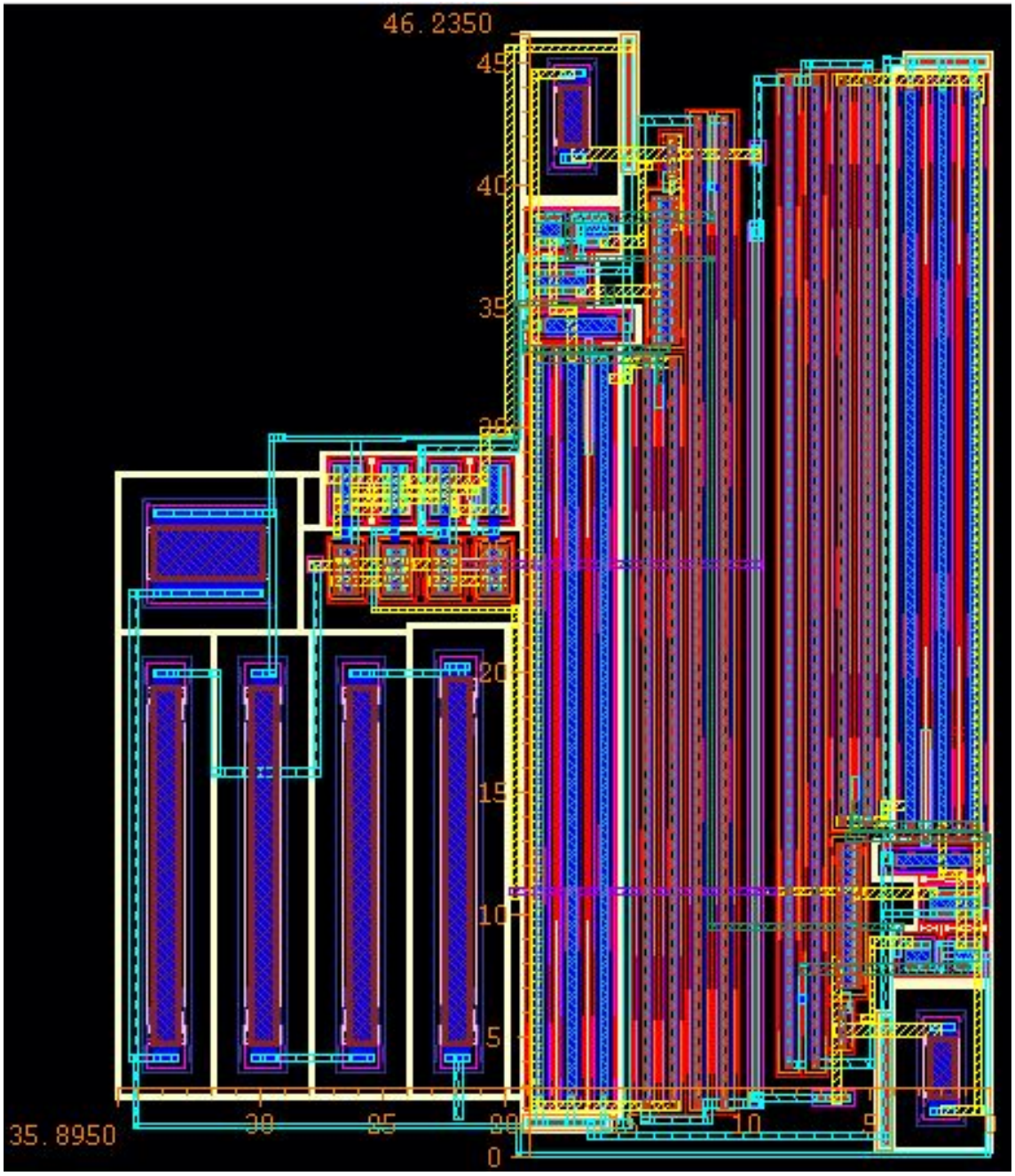


Figure 48: Control circuit Layout

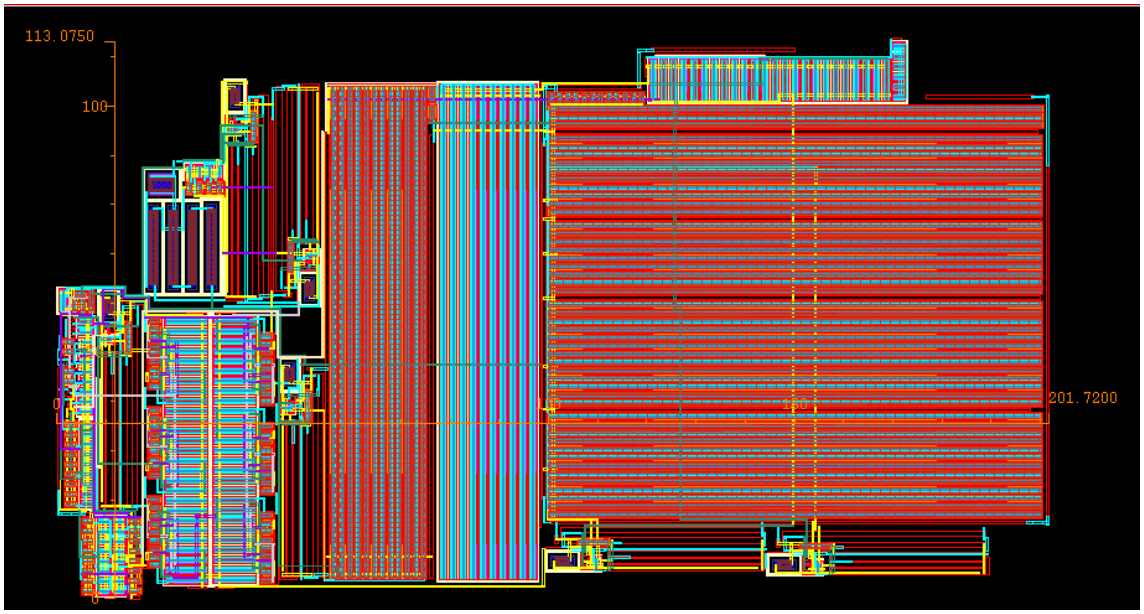
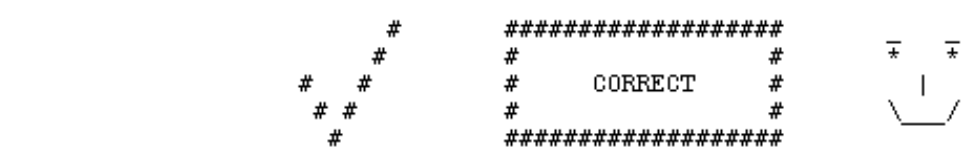


Figure 49: System of AC-DC Layout

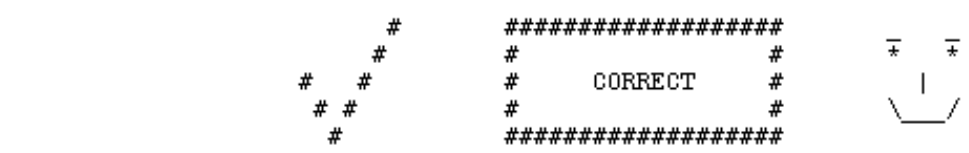
Cell SYS2 Summary (Clean)




```
LAYOUT CELL NAME:          SYS2
SOURCE CELL NAME:          SYS2

--------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                 Layout    Source          Component Type
                 ------    ------          --------------
 Ports:               6         6

 Nets:              143       143

 Instances:         207       152     *     MN (4 pins)
                    176       145     *     MP (4 pins)
                     11        11           R (3 pins)
                 ------    ------
 Total Inst:        394       308

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                 Layout    Source          Component Type
                 ------    ------          --------------
 Ports:               6         6

 Nets:              121       121

 Instances:         117       117          MN (4 pins)
```

Figure 50: System of AC-DC Layout

Cell SYS2 Summary (Clean)




```
LAYOUT CELL NAME:          SYS2
SOURCE CELL NAME:          SYS2

--------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                 Layout    Source          Component Type
                 ------    ------          --------------
 Ports:               6         6

 Nets:              143       143

 Instances:         207       152     *     MN (4 pins)
                    176       145     *     MP (4 pins)
                     11        11           R (3 pins)
                 ------    ------
 Total Inst:        394       308

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                 Layout    Source          Component Type
                 ------    ------          --------------
 Ports:               6         6

 Nets:              121       121

 Instances:         117       117          MN (4 pins)
```

Figure 51: System of AC-DC Layout

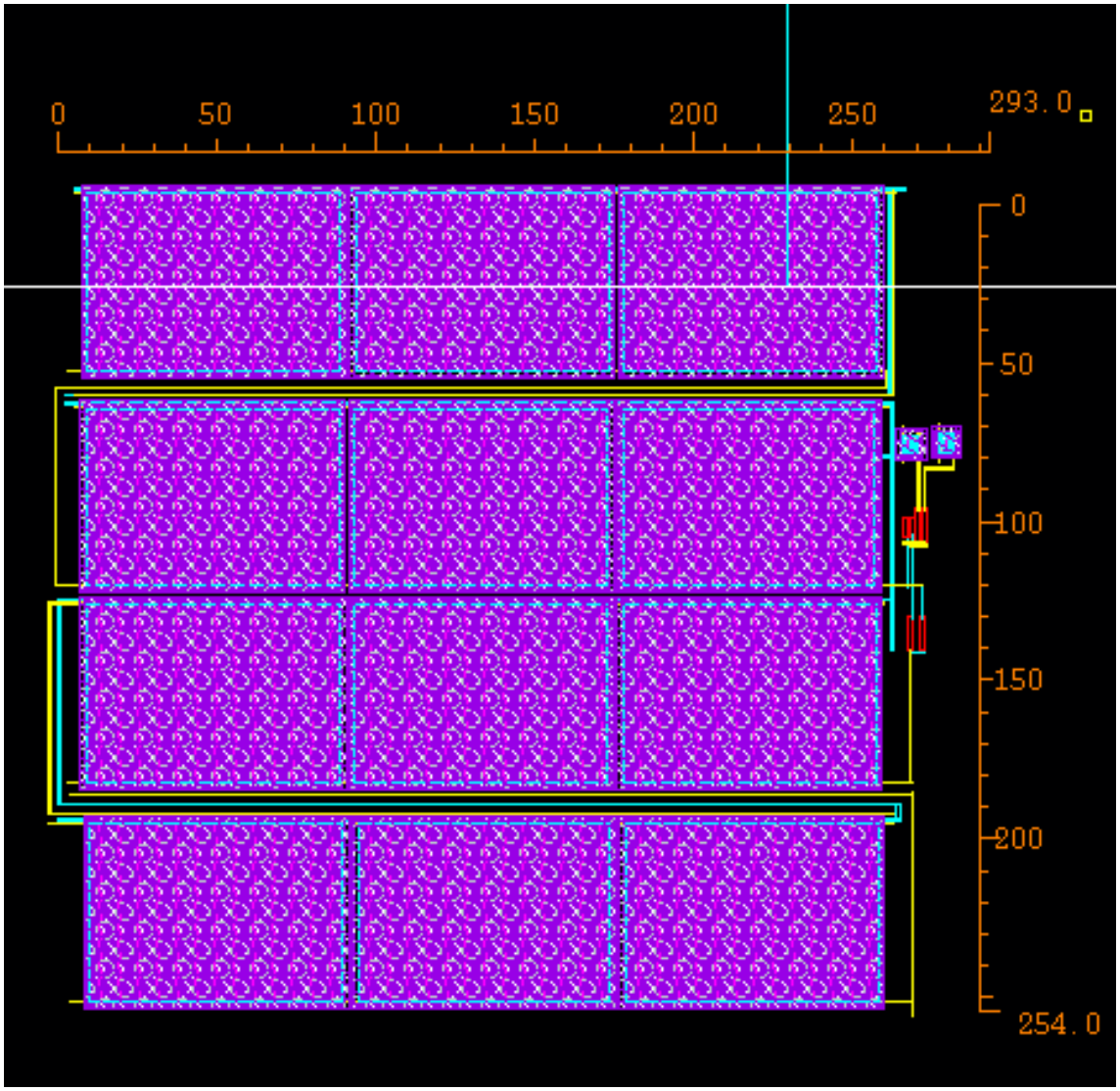


Figure 52: System of DC-DC Layout

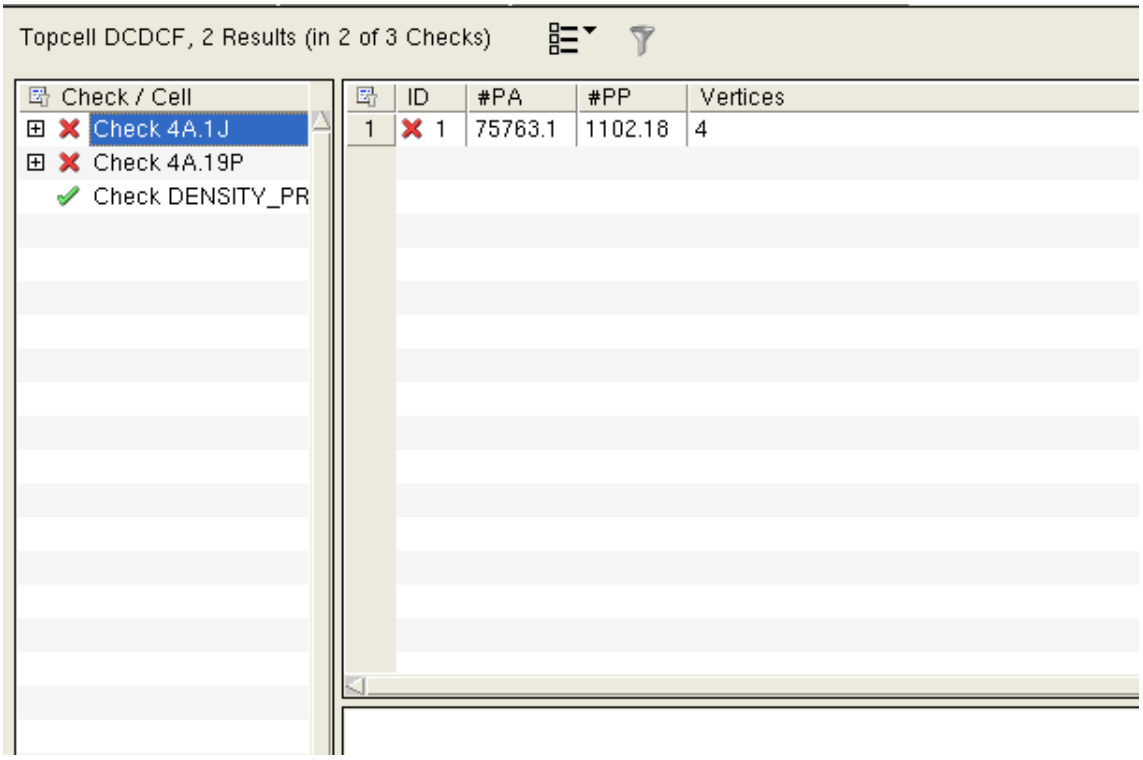


Figure 53: System of DC-DC Layout

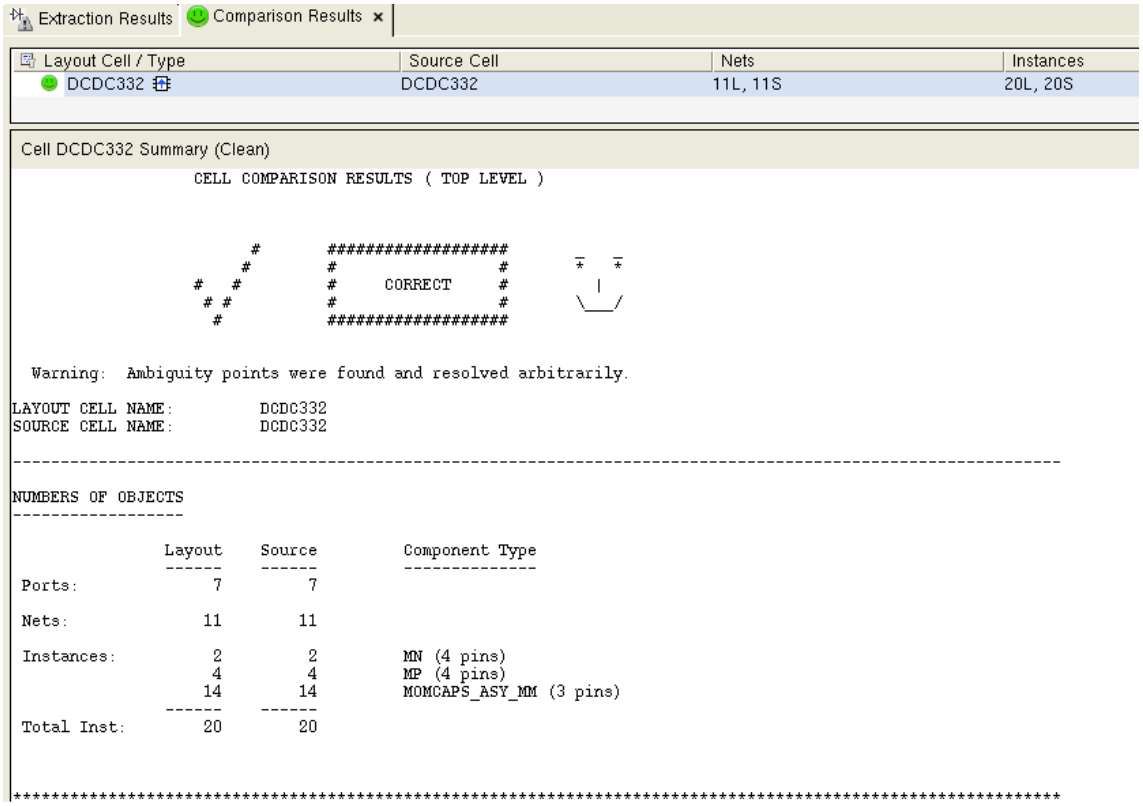


Figure 54: System of DC-DC Layout

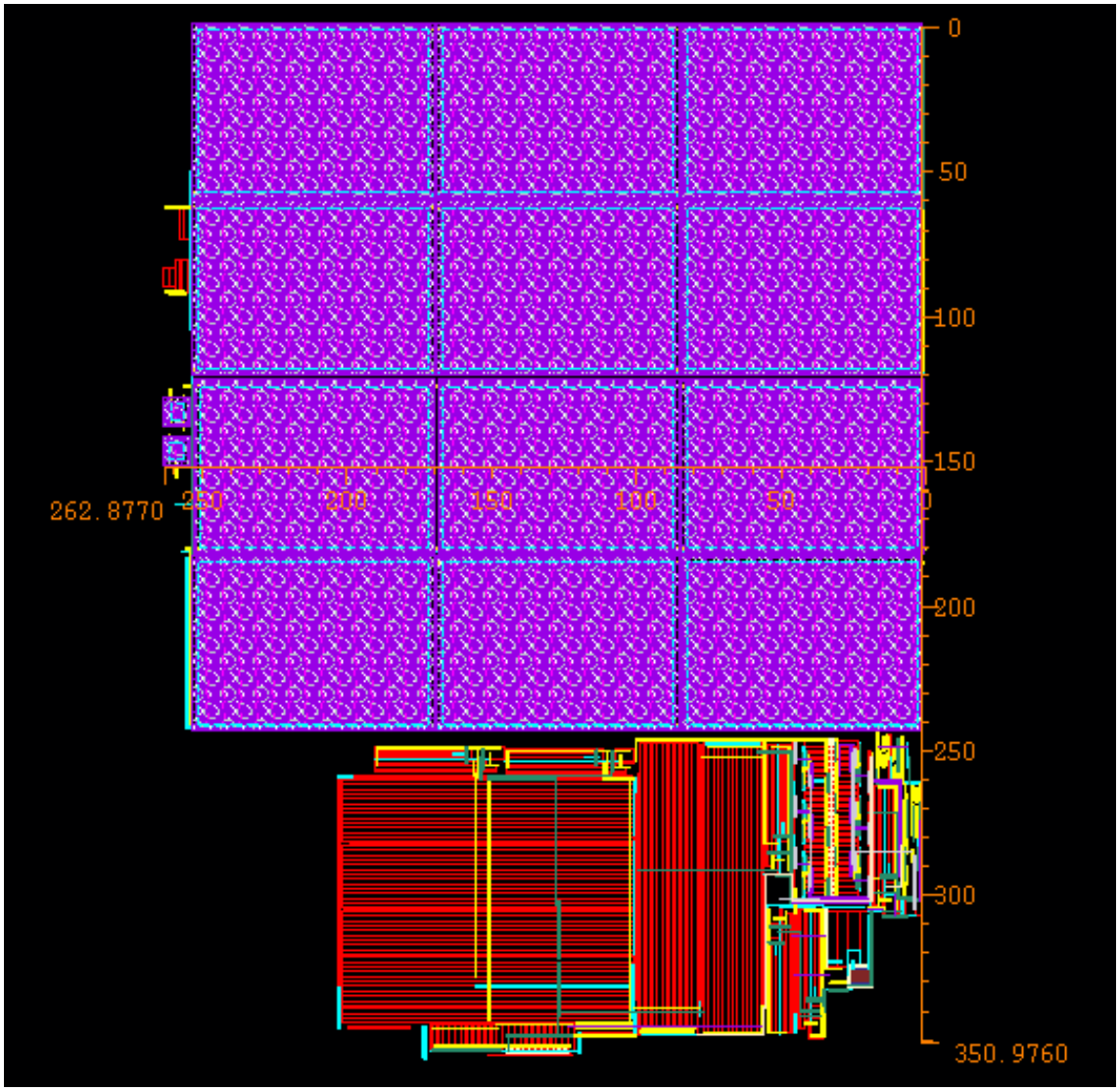


Figure 55: The layout of the whole system

6 Economic Analysis

Engineering is always about dealing with trade offs. The most important and critical trade off is the trade off between quality and cost. This project focused on quality in the previous sections so it is the time to focus on the cost. The area of the whole system using UMC130 library = $230 * 530 um^2$. So, the system will need a chip area of 1 mm x 1 mm which costs 6000 euro. There is an off chip capacitor with value of 22 uF that will cost 0.2762 euro. A 1.5 mF super capacitor will represent the battery and it costs 2.5 euro.

So the whole system's cost = 6000+0.2762+2.5 = 6002.7762 euro = 126538.5223 EGP

That's means the implanted system will cost almost 130,000 EGP to power an application for several years.

7 Conclusions and Recommendations

In the era of IOT in which devices need to communicate with each other, power is a vital issue because the larger number of devices which are wireless connected needs a self-operated, reliable and small power source. Energy harvesters are very efficient solution as they are small sized and harvest energy from the surrounding environment which meets the requirements of the IOT nodes. Piezoelectric is one of the promising energy harvesting methods as they provide an acceptable amount of power by changing the movement energy to electric energy, that's why this project focused on designing and implementing fully integrated piezoelectric energy harvesting system. Each block in the system complete each other as it does its job perfectly. As the MPPT finds the maximum power, the AC-DC converter rectifying the AC input into DC output and the DC-DC controls this output to power the application. Hoping by doing this project, all the IOT systems in the future will use similar systems.

Recommendations for future work

- This project used library UMC130 in Cadence virtuoso but maybe another will be better in this case to increase the speed or more important to reduce the power consumed.
- Using more than one source such as solar, RF and thermoelectric energy in the same time. So that, the system will choose the source that gives the highest power at this time.

References

[1] Ethem Erkan Akakka, Rebecca L Peterson and Khalil Najafi. A self-supplied inertial piezoelectric energy harvester with power-management ic. In Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International, pages 120–121. IEEE, 2011.

[2] T. H. NG and W. H. LIAO. Sensitivity analysis and energy harvesting for a self-powered piezoelectric sensor. Sage Publications Sage CA: Thousand Oaks, CA, Journal of Intelligent Material Systems and Structures, 16(10):785–797, 2005.

[3] Taeho Oh, Syed K.Islam, Mohamad Mahfouz and Gary To. A Low-Power CMOS Piezoelectric Transducer Based Energy Harvesting Circuit for Wearable Sensors for Medical Applications. Multidisciplinary Digital Publishing Institute, Journal of Low Power Electronics and Applications, 7(4):33, 2017.

[4] uk.rs-online. 2018. dcdc-converters-overview. [ONLINE] Available at: https://uk.rs-online.com/web/generalDisplay converters-overview. [Accessed 25 February 2018].

[5] elprocus. 2018. different-types-dc-to-dc-converters. [ONLINE] Available at: https://www.elprocus.com/different-types-dc-to-dc-converters/. [Accessed 25 February 2018].

[6] EE462L, Spring 2014, DC−DC Buck Converter, Lecture6.ppt.

[7] electronoobs. 2018. eng-circuitos-tut10.php. [ONLINE] Available at: http://www.electronoobs.com/eng-circuitos-tut10.php. [Accessed 25 February 2018].

[8] ELC 612 POWER MANAGEMENT, Lecture 2: DC-DC Converters.ppt, Dr. Faisal Elseddeek, Cairo University.

[9] learnabout-electronics. 2018. PSU/psu32.php. [ONLINE] Available at:http: //www.learnabout-electronics.org/PSU/psu32.php. [Accessed 25 February 2018].

[10]S. Abdelaziz, A. Emira, AG. Radwan, AN. Mohieldin, and AM. Soliman. A low start up voltage charge pump for thermoelectric energy scavenging. In Industrial Electronics (ISIE), 2011 IEEE International Symposium on, pages 71–75. IEEE, 2011.

[11] Yi-Hsin Weng, 2009, 'Charge Pump Design in Low-voltage CMOS Technology', Master thesis, College of Electrical and Computer Engineering National Chiao Tung University, Hsinchu, Taiwan, Republic of China.

[12]Lu, C., Tsui, C., Ki, W. (2011). Vibration Energy Scavenging System With Maximum Power Tracking for Micropower Applications. IEEE Transactions On Very Large Scale Integration (VLSI) Systems, 19(11), 2109-2119. doi: 10.1109/tvlsi.2010.2069574

[13]M, R., S, N. (2016). Open Circuit Voltage Based MPPT Tracing For Thermoelectric Generator Fed Non-Inverting Synchronous Buck-Boost Derived Converter – Part II (Hardware Studies). International Journal Of Scientific Research And Education. doi: 10.18535/ijsre/v4i06.14

[14]Shim, M., Kim, J., Jeong, J., Park, S., Kim, C. (2015). Self-Powered 30 μW to 10 mW Piezoelectric Energy Harvesting System With 9.09 ms/V Maximum Power Point Tracking Time. IEEE Journal Of Solid-State Circuits, 50(10), 2367-2379. doi: 10.1109/jssc.2015.2456880

[15]Bond, M., Park, J. (2015). Current-Sensorless Power Estimation and MPPT Implementation for Thermoelectric Generators. IEEE Transactions On Industrial Electronics, 62(9), 5539-5548. doi: 10.1109/tie.2015.2414393

[16]Lei, P., Chang, R., Chia, C., Lee, M. (2015). Low start-up voltage dc–dc converter with negative voltage control for thermoelectric energy harvesting. The Journal Of Engineering, 2015(1), 38-40. doi: 10.1049/joe.2014.0252

[17]M, R., S, N. (2016). Open Circuit Voltage Based MPPT Tracing For Thermoelectric Generator Fed Non-Inverting Synchronous Buck-Boost Derived Converter – Part II (Hardware Studies). International Journal Of Scientific Research And Education. doi: 10.18535/ijsre/v4i06.14

[18]Montecucco, A., Knox, A. (2015). Maximum Power Point Tracking Converter Based on the Open-Circuit Voltage Method for Thermoelectric Generators. IEEE Transactions On Power Electronics, 30(2), 828-839. doi: 10.1109/tpel.2014.2313294

[19]Kim, J., Kim, C. (2013). A DC–DC Boost Converter With Variation-Tolerant MPPT Technique and Efficient ZCS Circuit for Thermoelectric Energy Harvesting Applications. IEEE Transactions On Power Electronics, 28(8), 3827-3833. doi: 10.1109/tpel.2012.2231098

[20] Stanzione, S., van Liempd, C., van Schaijk, R., Naito, Y., Yazicioglu, F., Van Hoof, C. (2013). A High Voltage Self-Biased Integrated DC-DC Buck Converter With Fully Analog MPPT Algorithm for Electrostatic Energy Harvesters. IEEE Journal Of Solid-State Circuits, 48(12), 3002-3010. doi: 10.1109/jssc.2013.2283152

[21]Hehn, T. and Manoli, Y. (n.d.). CMOS circuits for piezoelectric energy harvesters.

[22]Kundu, S. and Nemade, H. (2016). Modeling and Simulation of a Piezoelectric Vibration Energy Harvester. Procedia Engineering, 144, pp.568-575.

[23]Phipps, A. (2010). Modeling and characterization of piezoelectric energy harvesting systems with the pulsed resonant converter. [Gainesville, Fla.]: University of Florida.

Appendix A

Verilog A for piezoelectric transducer:

‘include "constants.vams"

‘include "disciplines.vams"

module PZ-333(vo, vgnd);

parameter real $m = 1.674^{-3}$ from [0:inf);

parameter real $gama = 0.745^{-3}$ from [0:inf);

parameter real $k = 1447.8$ from [0:inf);

parameter real $d = 0.1$ from [0:inf);

parameter real $Cp = 19.5^{-9}$ from [0:inf);

parameter real $a = 72$;

parameter real $freq = 149$;

parameter $ac - mag = 148$;

parameter $ac - phase = 0$;

inout vo,vgnd;

electrical vo,vgnd,v1, vi;

branch (vi,v1)rl, (v1,vo)cap;

real lm,rm,cm;

real icap, ir, icp;

real vm;

analog begin

$lm = m/(gama * gama)$;

$rm = d/(gama * gama)$;

$cm = (gama * gama)/k$;

$vm = m * a/gama$;

$V(vi, vgnd) < +vm * sin(abstime * 2 * ‘M_PI * freq)$;

$V(vi, vgnd) < +ac_stim(”ac”, ac_mag, ac_phase)$;

$V(rl) < +lm * ddt(I(rl))$;

$V(rl) < +rm * I(rl)$;

$I(cap) < +cm * ddt(V(cap));$

$I(vo, vgnd) < +Cp * ddt(V(vo, vgnd));$

$ir = I(rl);$

$icap = V(vi, vgnd);$

end

endmodule